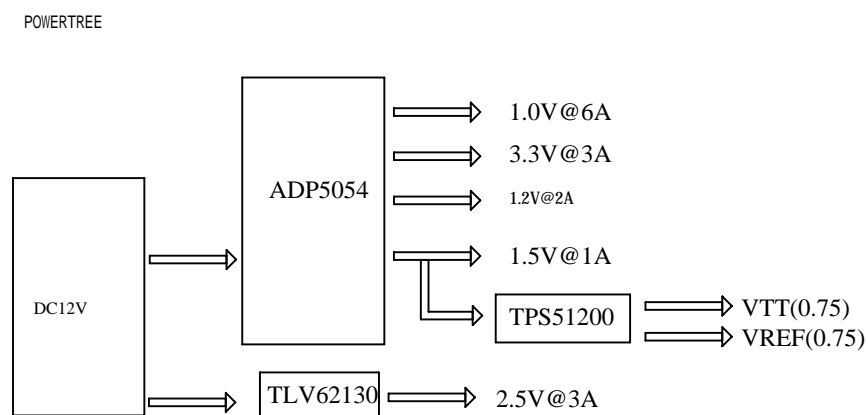
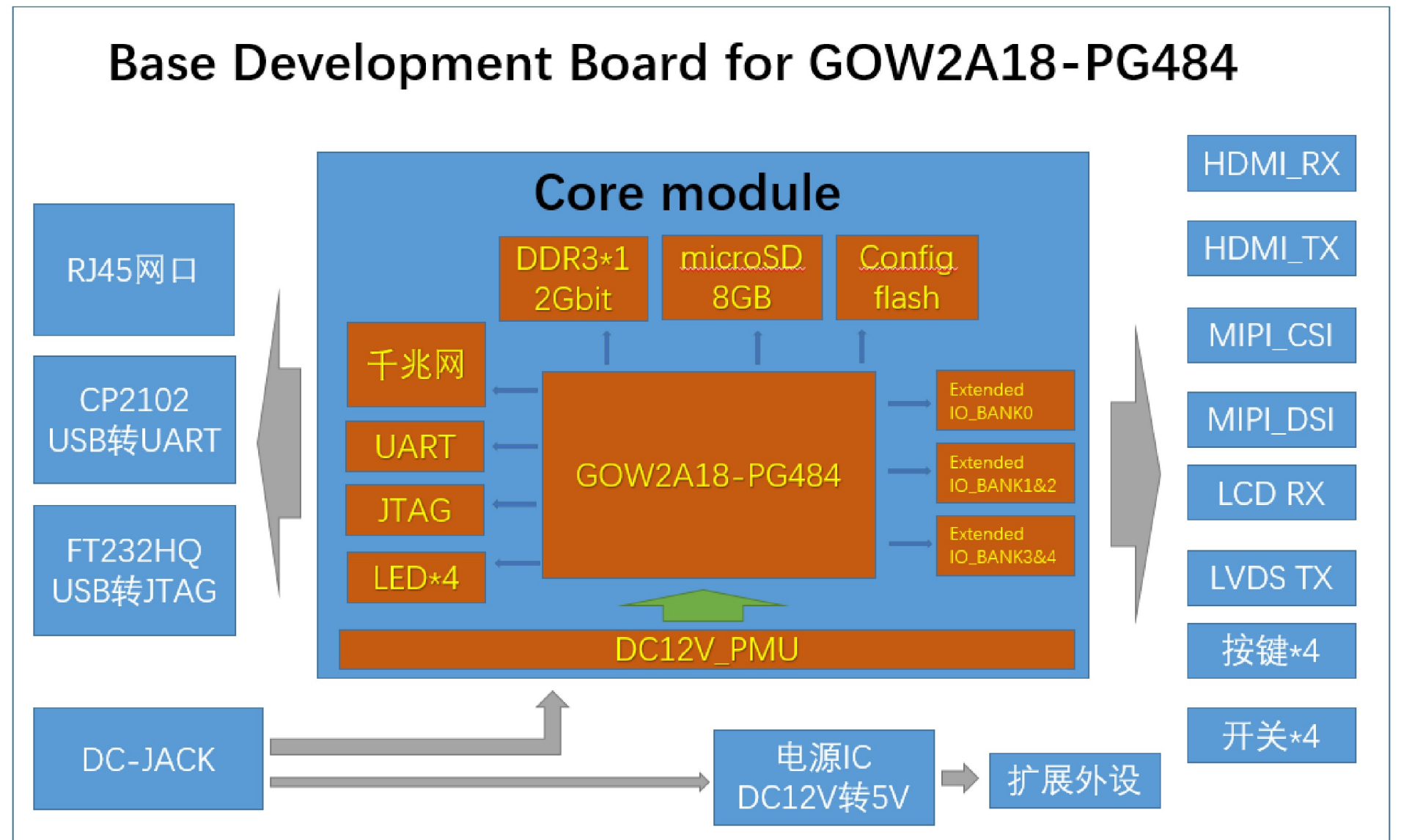


°æ±¼	ÈÕÆÚ	ÐÞ,ÄËµÃ÷
REV1.0	20200807	RELESE
REV1.0	20200813	°Ï±c. ð°a

Block Diagram



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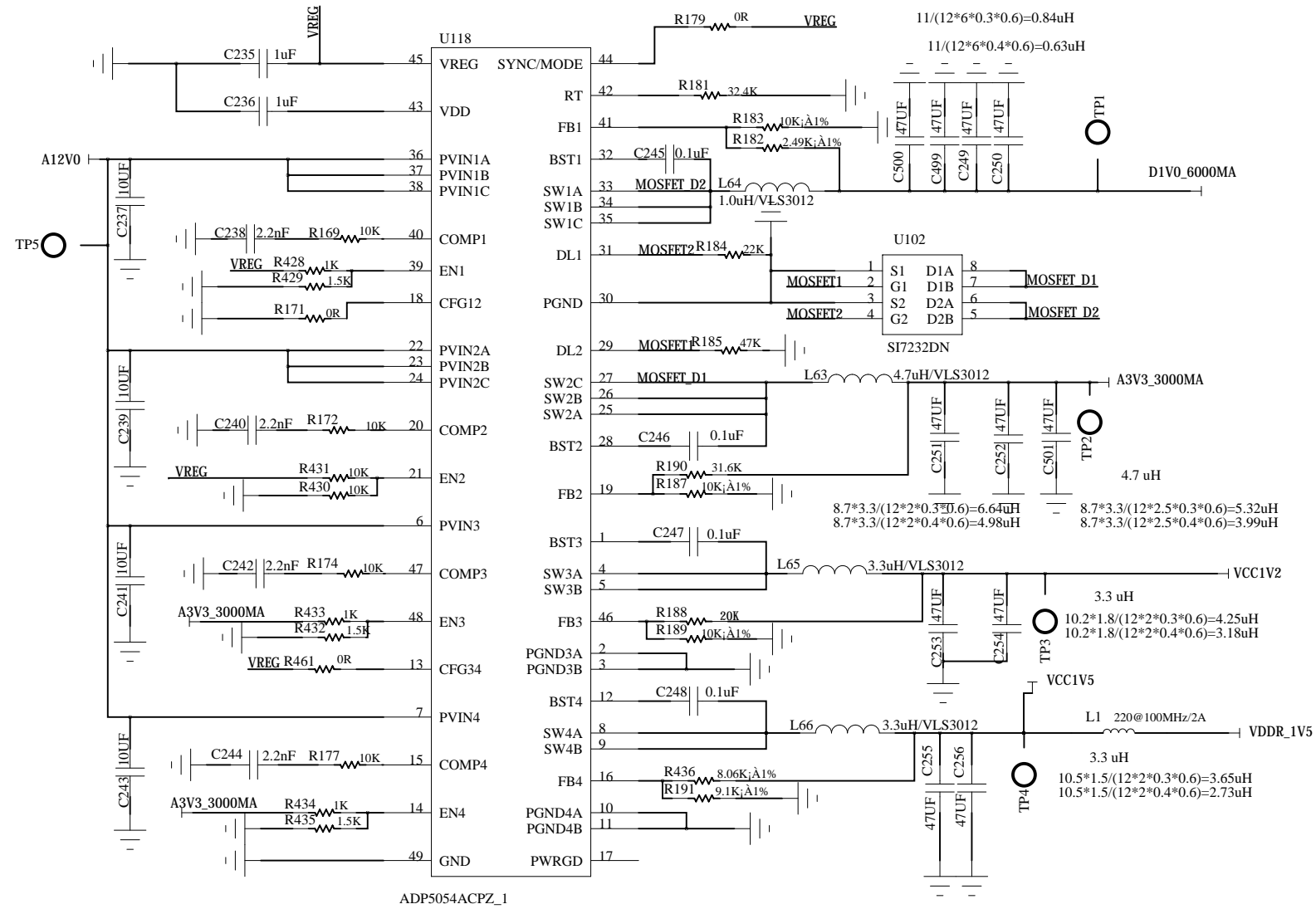
D

C

B

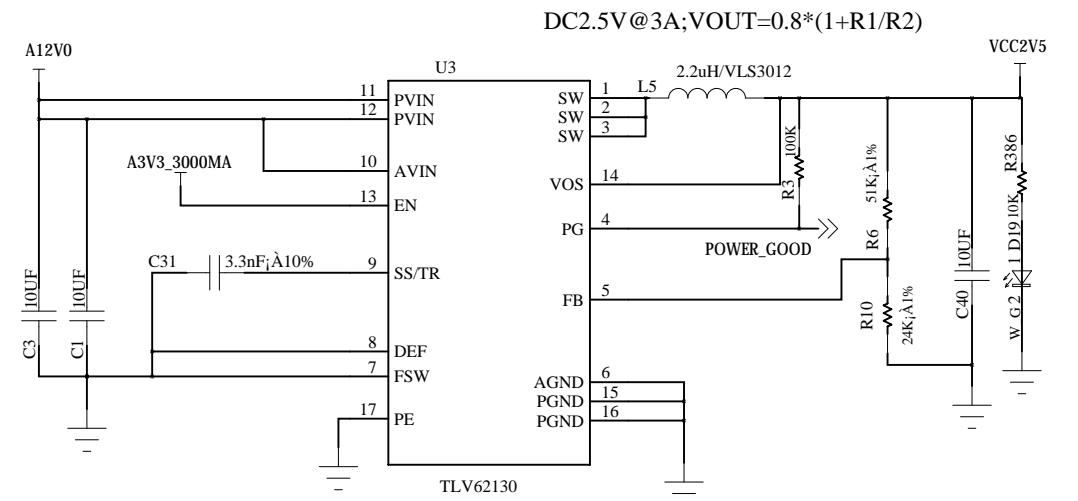
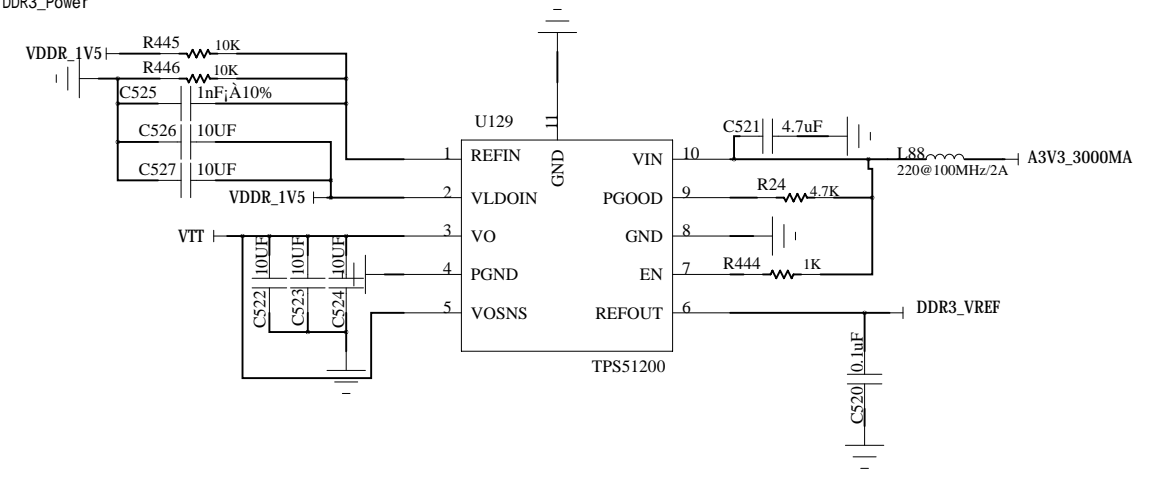
A

POWER Manage

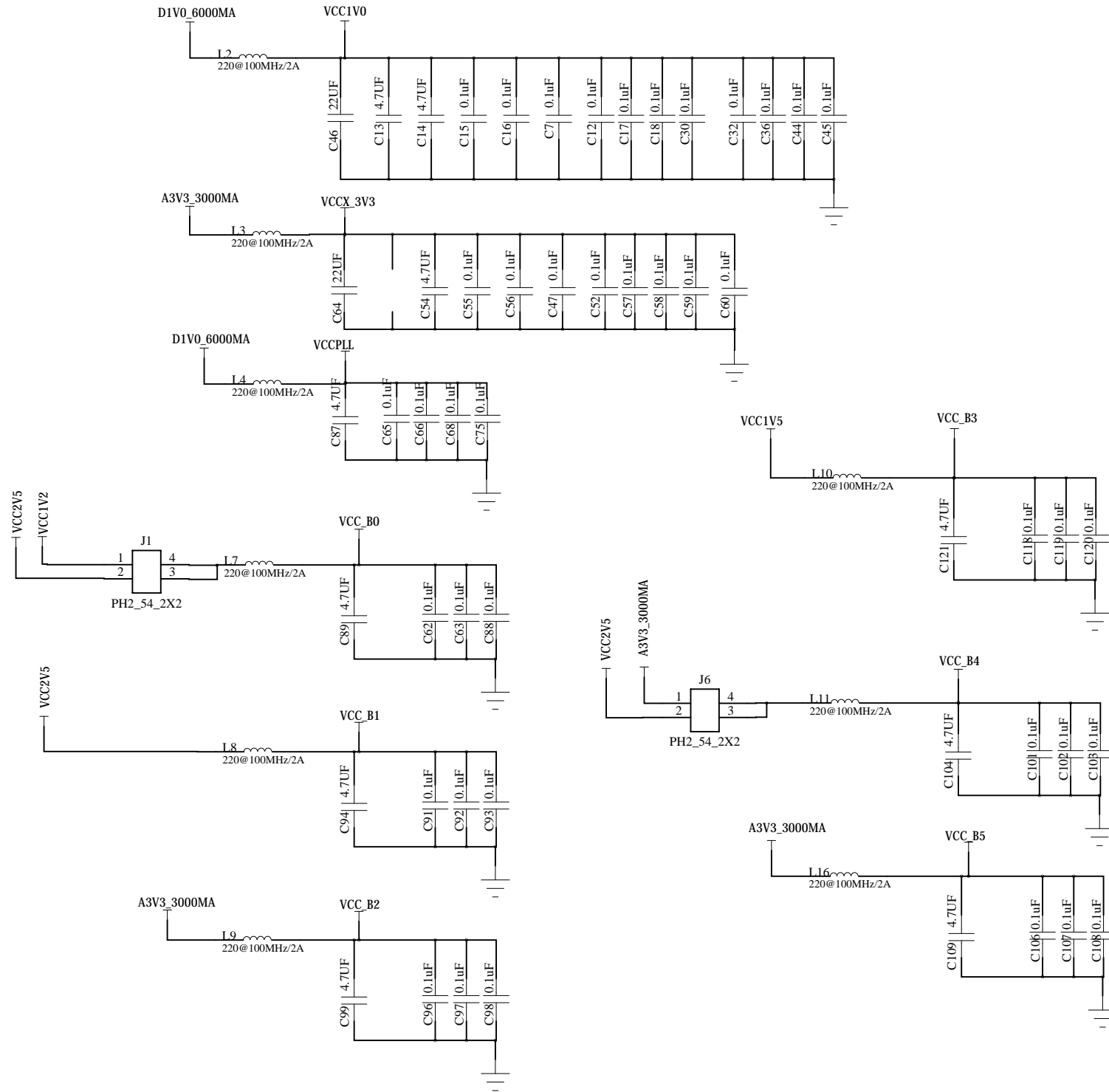
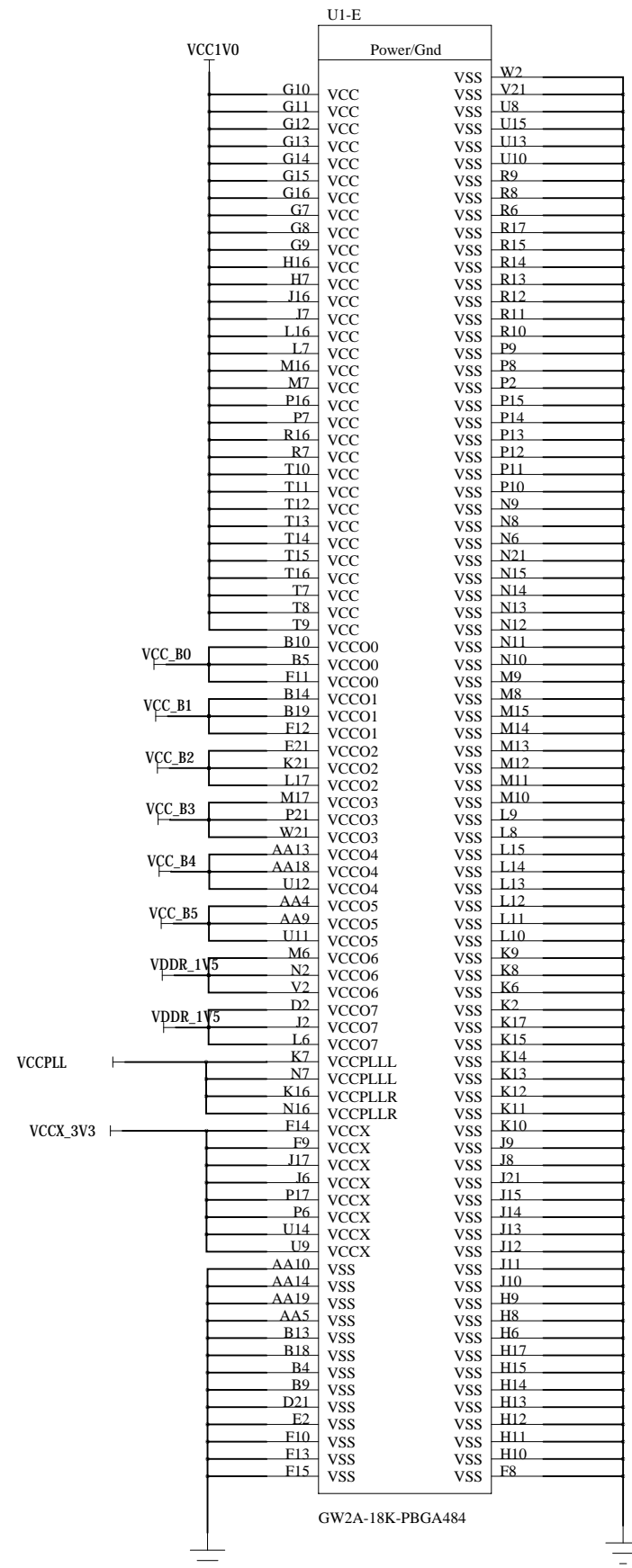


$$V_{OUT} = V_{ref} \cdot \left(1 + \frac{R_{top}}{R_{bot}} \right)$$

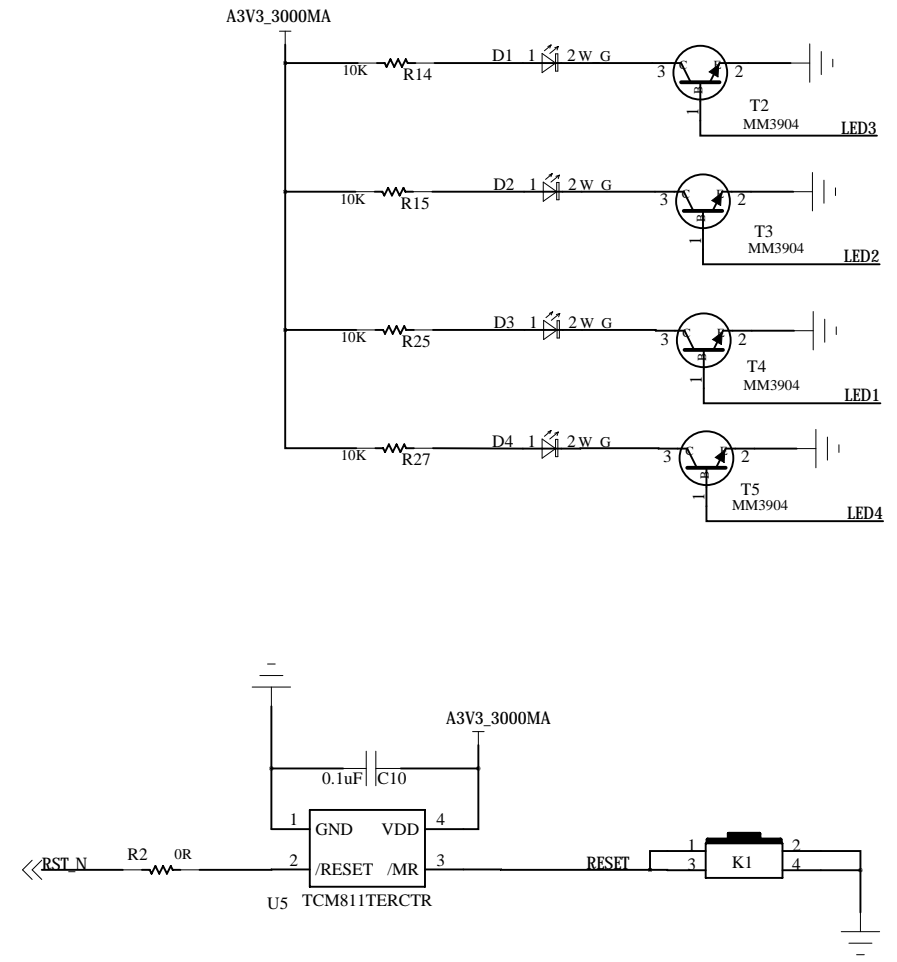
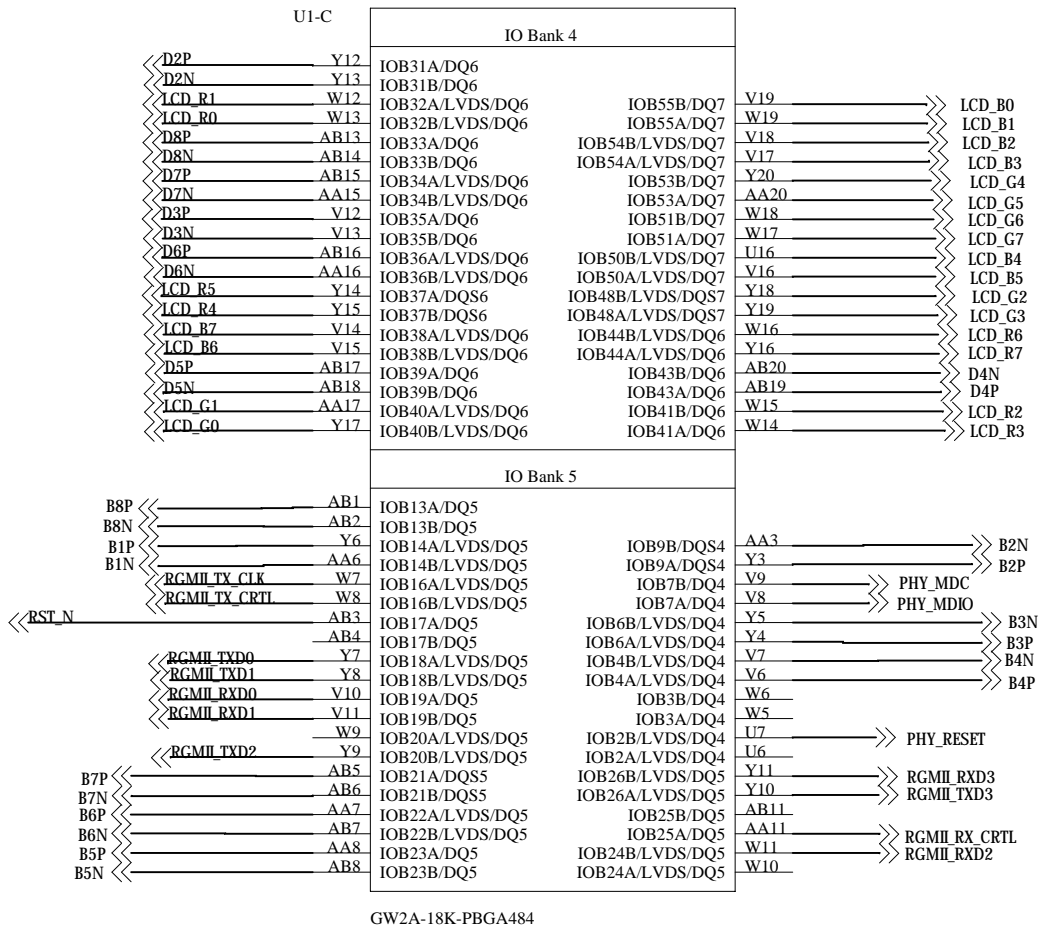
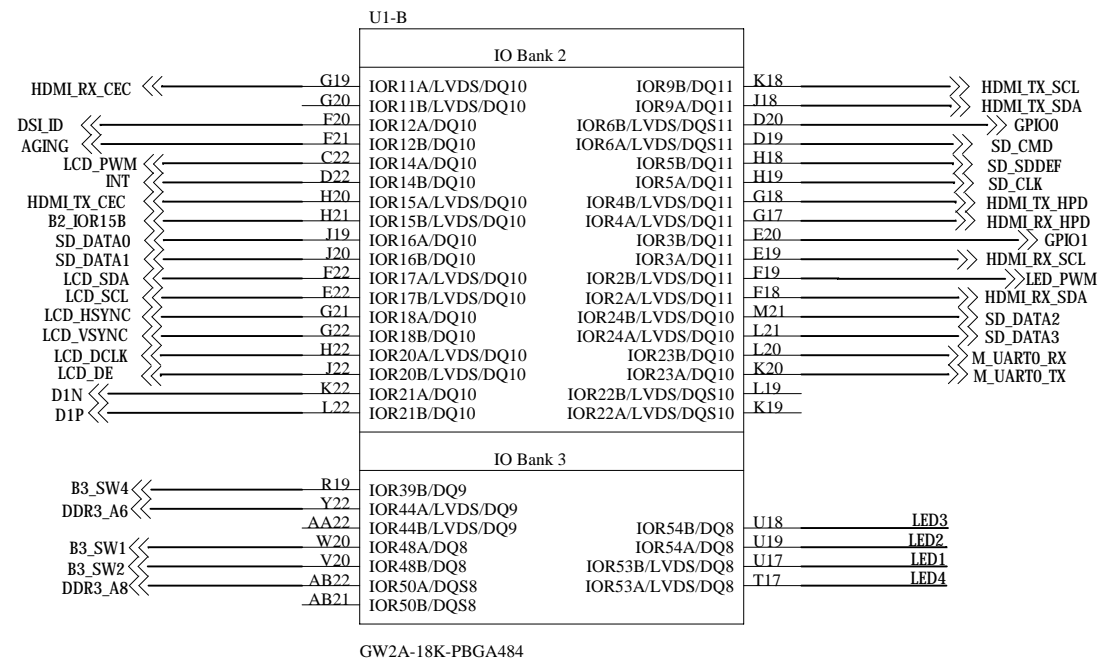
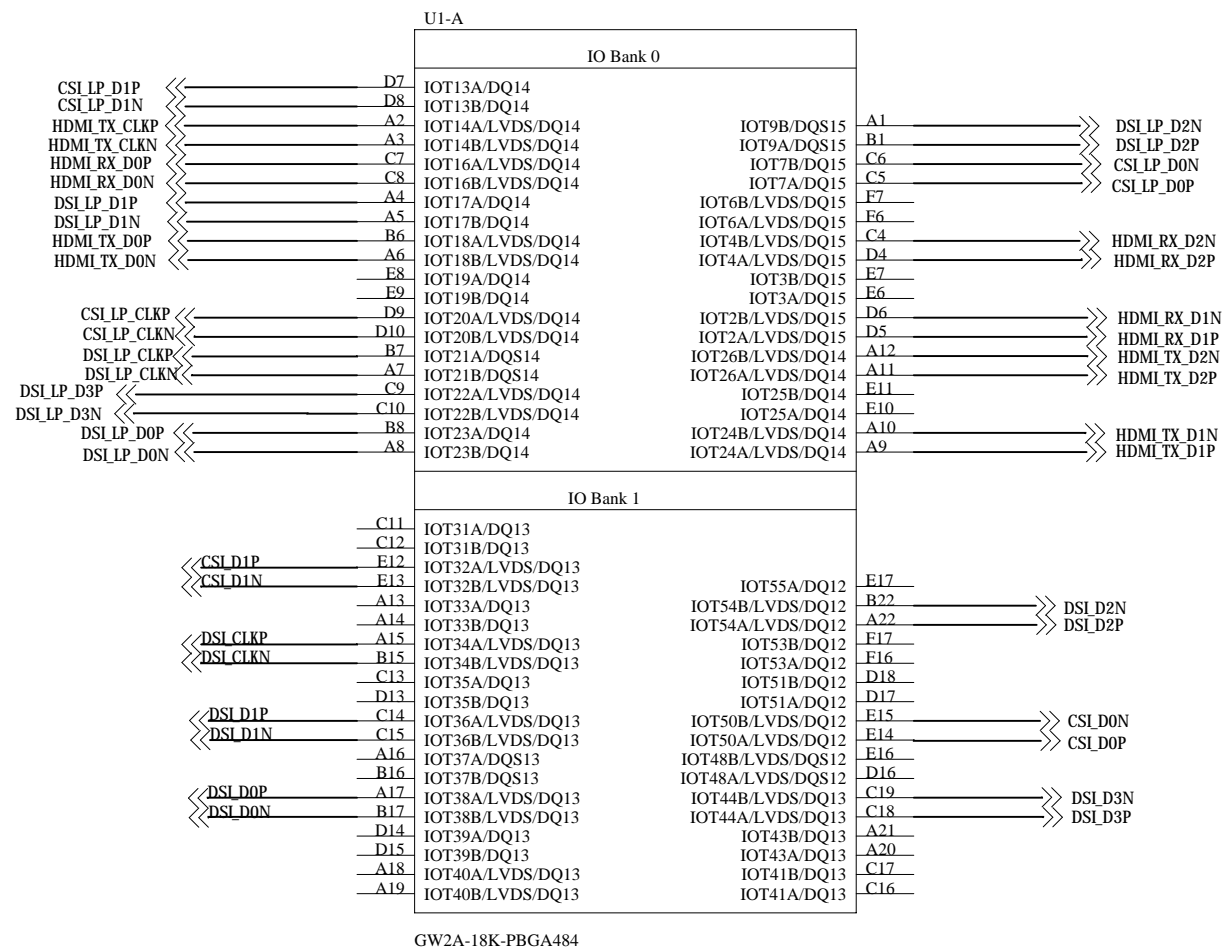
DDR3_Power



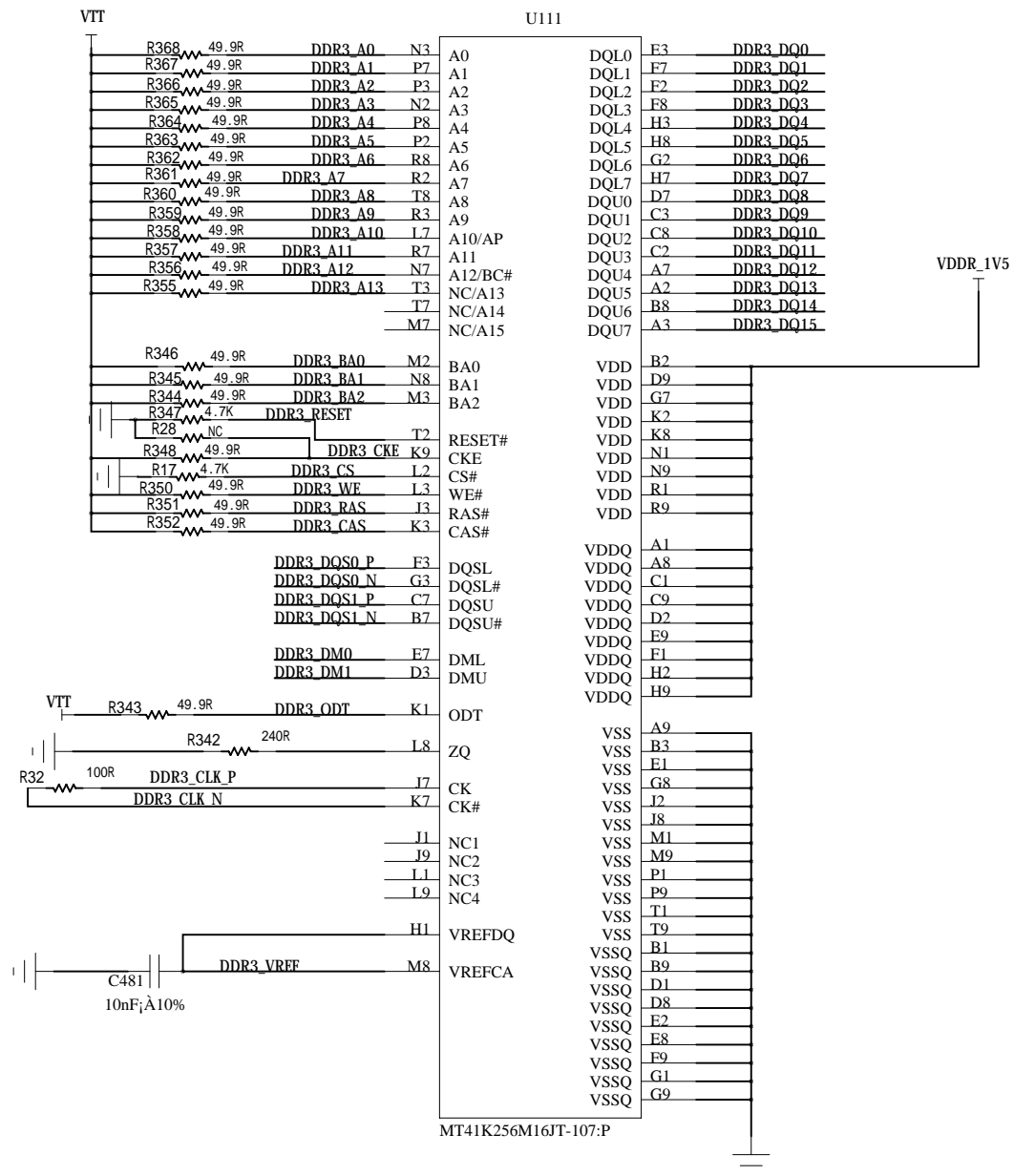
Title: MINI_EYE_GW2A18_PG484	
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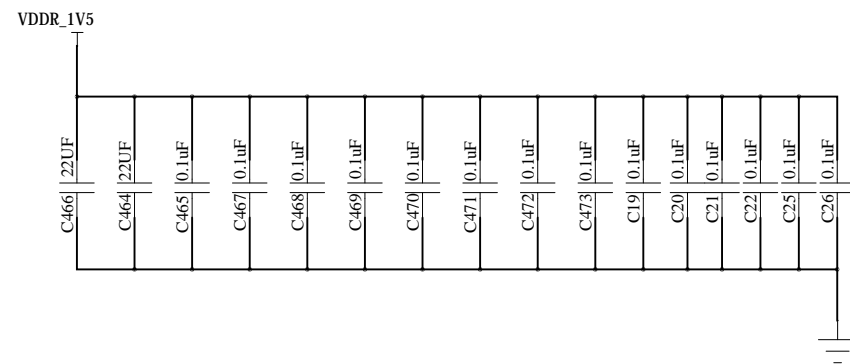


Title: MINI_EYE_GW2A18_PG484	
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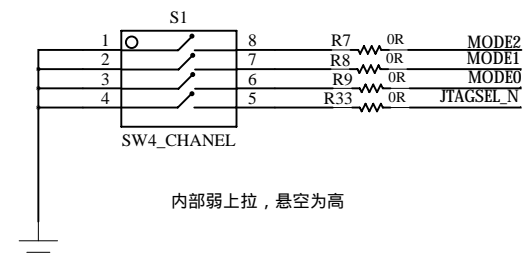
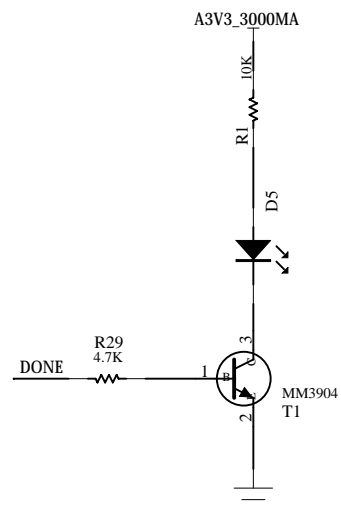
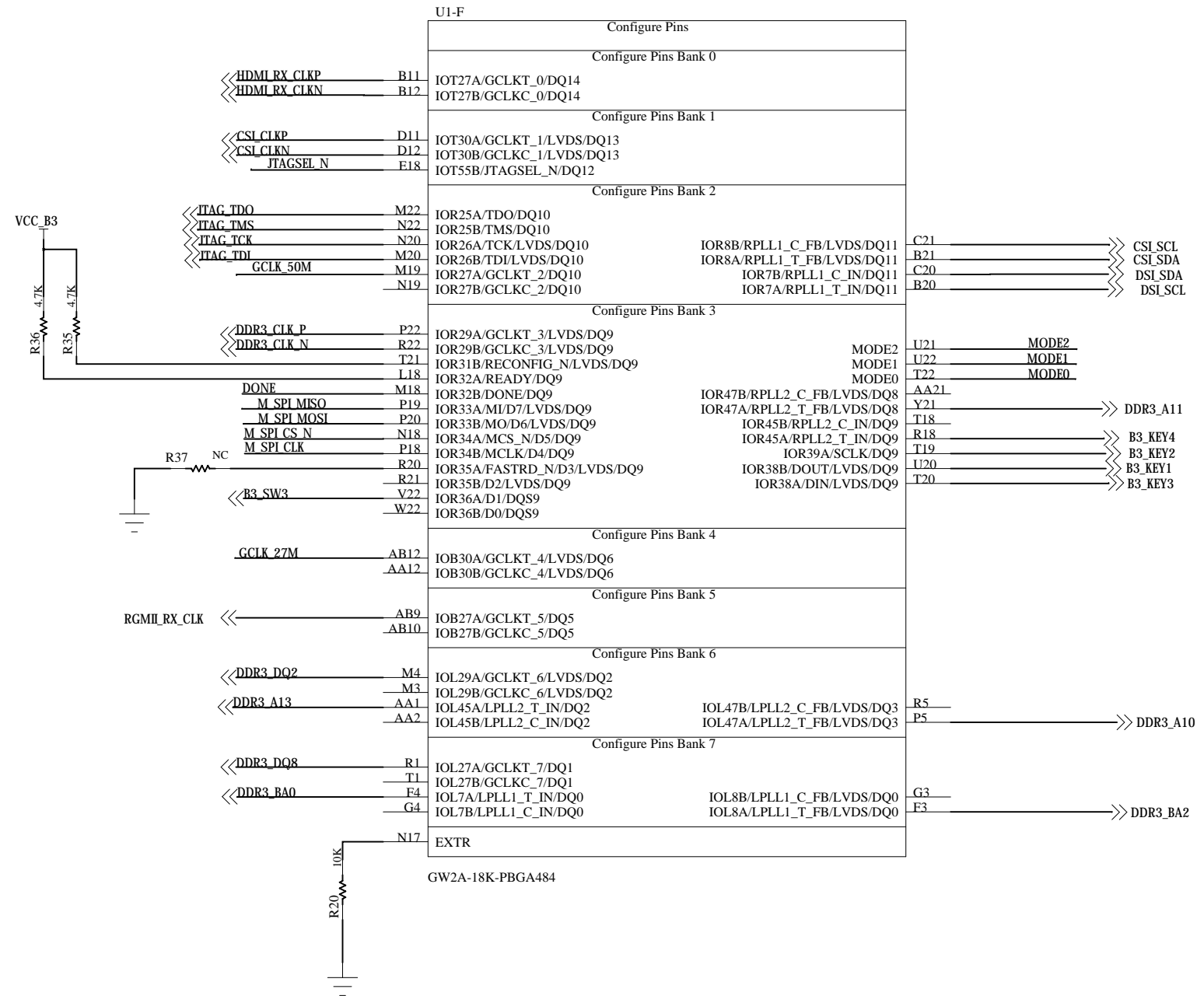
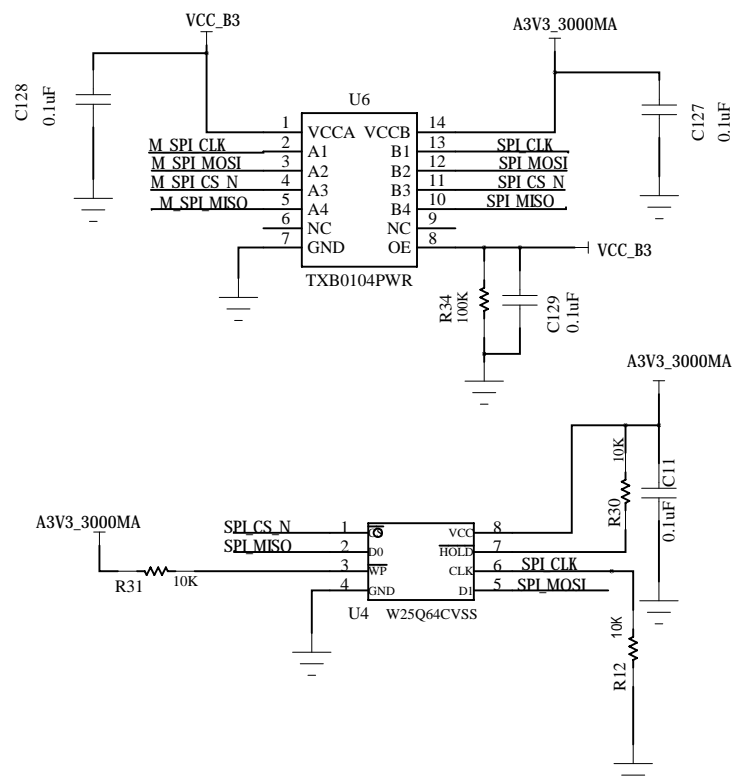
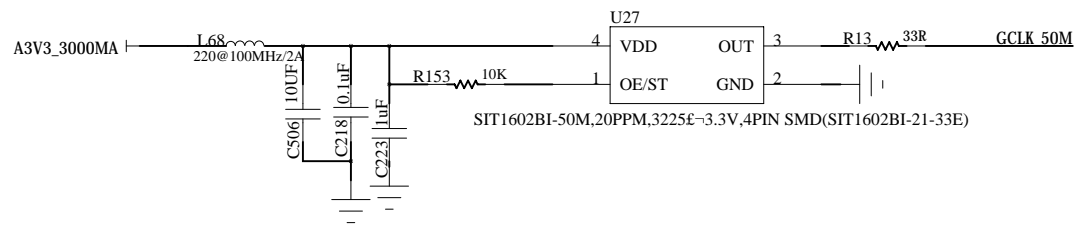
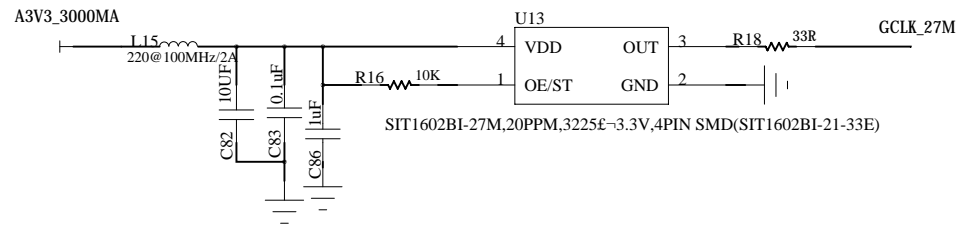
IO Bank 6	
DDR3 DQ5	U1
DDR3 DQ6	U2
DDR3 DQ0	N3
DDR3 DQ3	N5
DDR3 DQ7	R2
DDR3 DM0	W1
DDR3 DQS0_P	R3
DDR3 DQS0_N	R4
DDR3 DQ4	Y1
IO Bank 6	
IOL30A/DQ2	U1
IOL30B/DQ2	U2
IOL31A/LVDS/DQ2	N3
IOL31B/LVDS/DQ2	N5
IOL32A/DQ2	N9
IOL32B/DQ2	T2
IOL33A/LVDS/DQ2	T2
IOL33B/LVDS/DQ2	R2
IOL34A/DQ2	V1
IOL34B/DQ2	W1
IOL35A/LVDS/DQ2	P3
IOL35B/LVDS/DQ2	R3
IOL36A/DQS2	P4
IOL36B/DQS2	R4
IOL38A/LVDS/DQ2	Y1
IOL38B/LVDS/DQ2	Y2
IOL54B/DQ3	T6
IOL54A/DQ3	T5
IOL53B/LVDS/DQ3	U5
IOL53A/LVDS/DQ3	V5
IOL50B/DQS3	W4
IOL50A/DQS3	V4
IOL48B/DQ3	U4
IOL48A/DQ3	T4
IOL44B/LVDS/DQ2	W3
IOL44A/LVDS/DQ2	V3
IOL39B/DQ2	U3
IOL39A/DQ2	T3
IOL9B/DQ0	J5
IOL9A/DQ0	H5
IOL6B/LVDS/DQS0	E3
IOL6A/LVDS/DQS0	E4
IOL5B/DQ0	C3
IOL5A/DQ0	D3
IOL4B/LVDS/DQ0	G5
IOL4A/LVDS/DQ0	G6
IOL3B/DQ0	B2
IOL3A/DQ0	B3
IOL2B/LVDS/DQ0	F5
IOL2A/LVDS/DQ0	E5
IOL26B/LVDS/DQ1	N1
IOL26A/LVDS/DQ1	P1
IOL25B/DQ1	M1
IOL25A/DQ1	M2
IOL24B/LVDS/DQ1	L4
IOL24A/LVDS/DQ1	K4
IOL23B/DQ1	L3
IOL23A/DQ1	K3
IO Bank 7	
IO Bank 7	
IOL11A/LVDS/DQ1	J5
IOL11B/LVDS/DQ1	H5
IOL12A/DQ1	E3
IOL12B/DQ1	E4
IOL14A/DQ1	C3
IOL14B/DQ1	D3
IOL15A/LVDS/DQ1	G5
IOL15B/LVDS/DQ1	G6
IOL16A/DQ1	B2
IOL16B/DQ1	B3
IOL17A/LVDS/DQ1	F5
IOL17B/LVDS/DQ1	E5
IOL18A/DQ1	N1
IOL18B/DQ1	P1
IOL20A/LVDS/DQ1	M1
IOL20B/LVDS/DQ1	M2
IOL21A/DQ1	L4
IOL21B/DQ1	K4
IOL22A/LVDS/DQS1	L3
IOL22B/LVDS/DQS1	K3

GW2A-18K-PBGA484



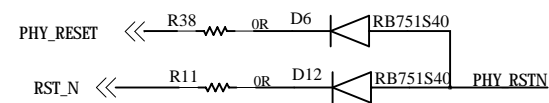
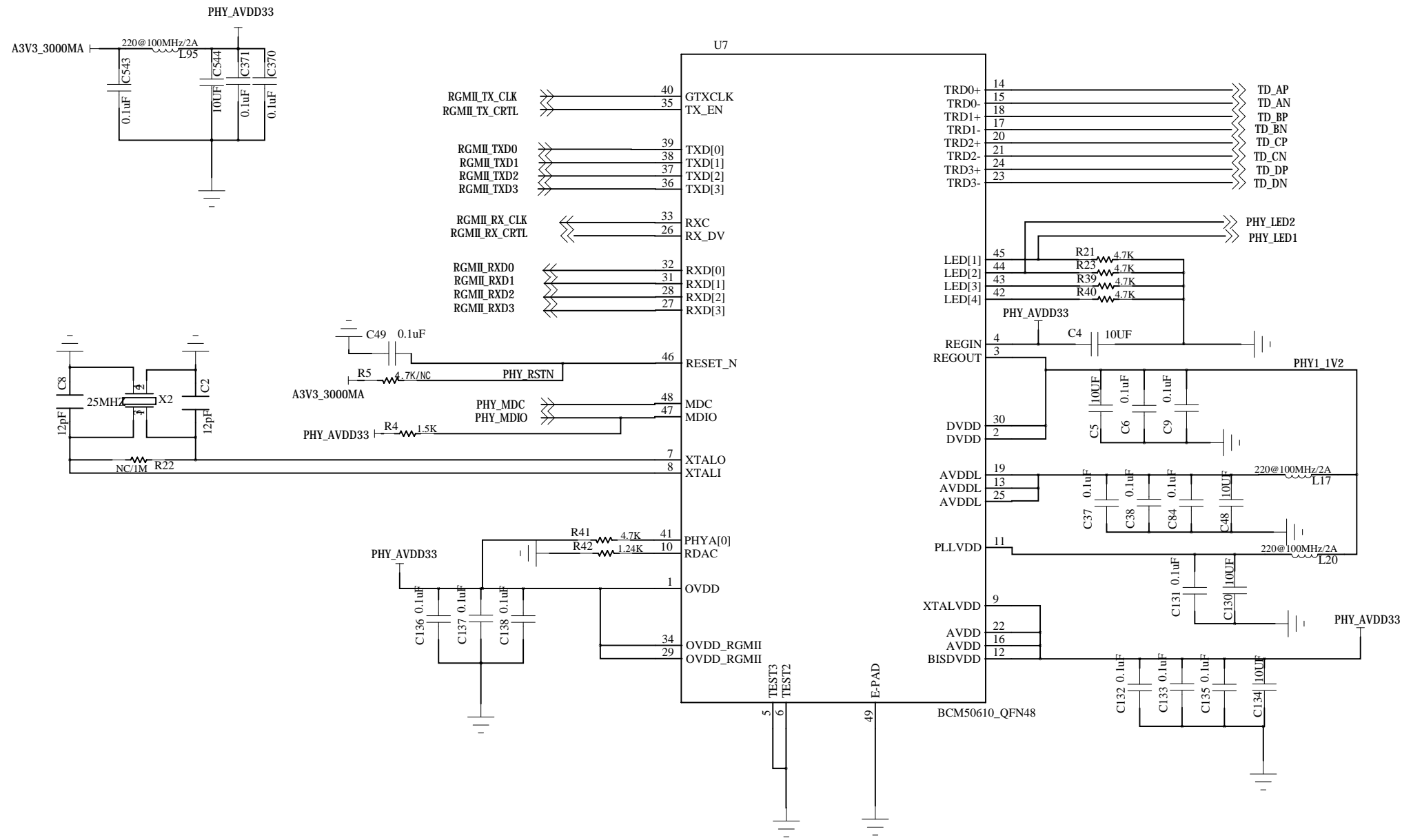
- DDR3_DQ2 << DDR3 DQ2
- DDR3_DQ8 << DDR3 DQ8
- DDR3_BA0 << DDR3 BA0
- DDR3_BA2 << DDR3 BA2
- DDR3_A6 << DDR3 A6
- DDR3_A8 << DDR3 A8
- DDR3_A10 << DDR3 A10
- DDR3_A11 << DDR3 A11
- DDR3_A13 << DDR3 A13
- DDR3_CLK_N << DDR3 CLK N
- DDR3_CLK_P << DDR3 CLK P

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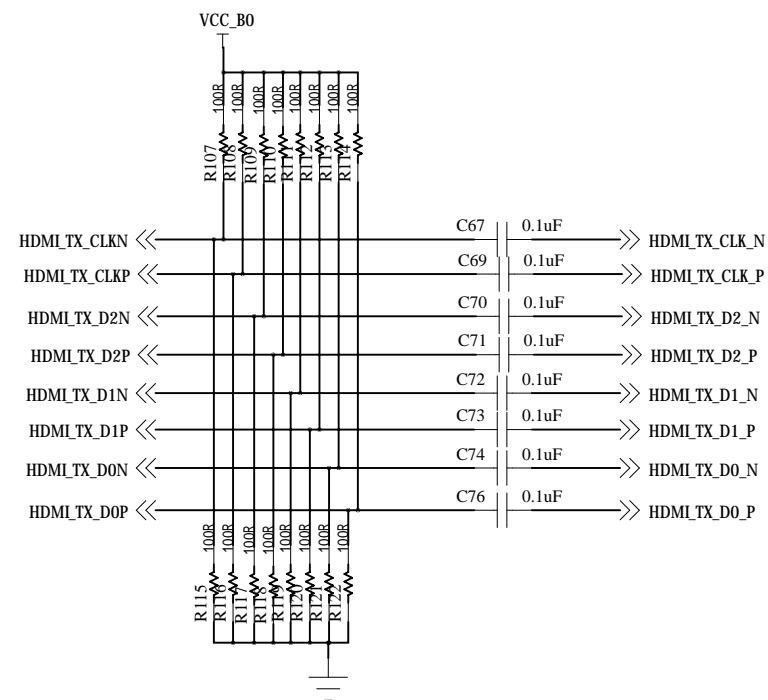
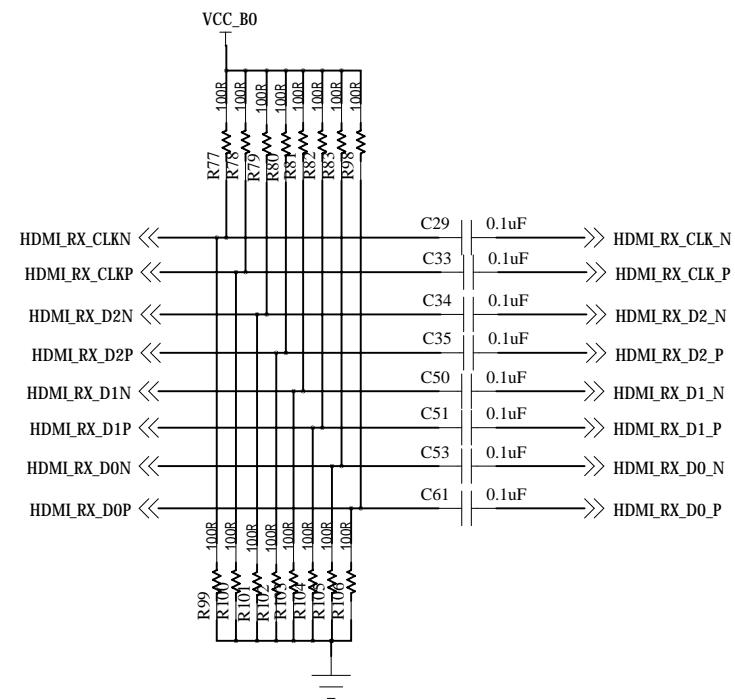
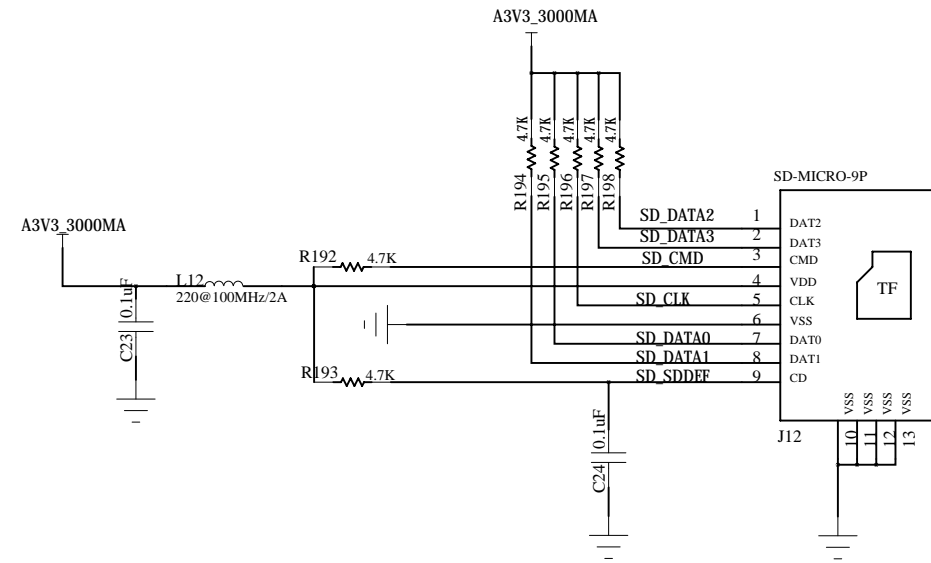
内部弱上拉，悬空为高

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micro_SD



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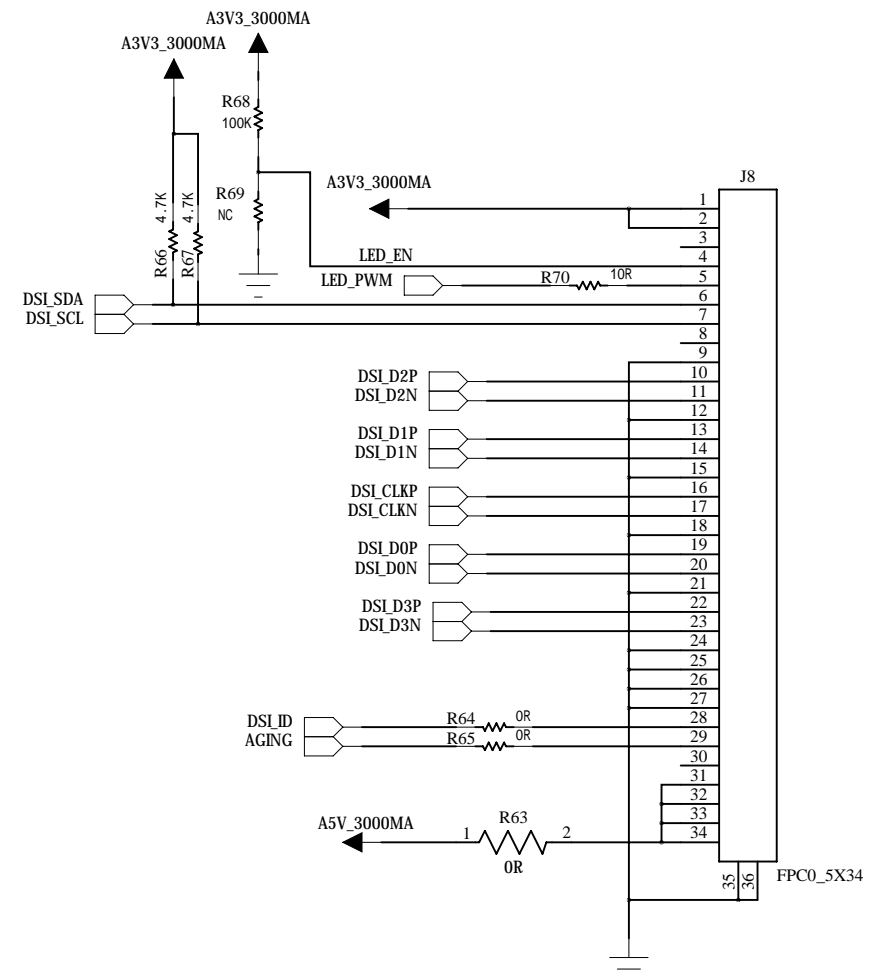
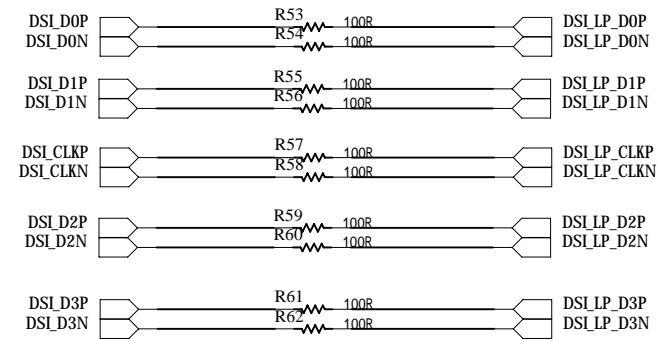
Checked By: Date:

Approved By: Date:

Size A3 Sheet: 2/5

D

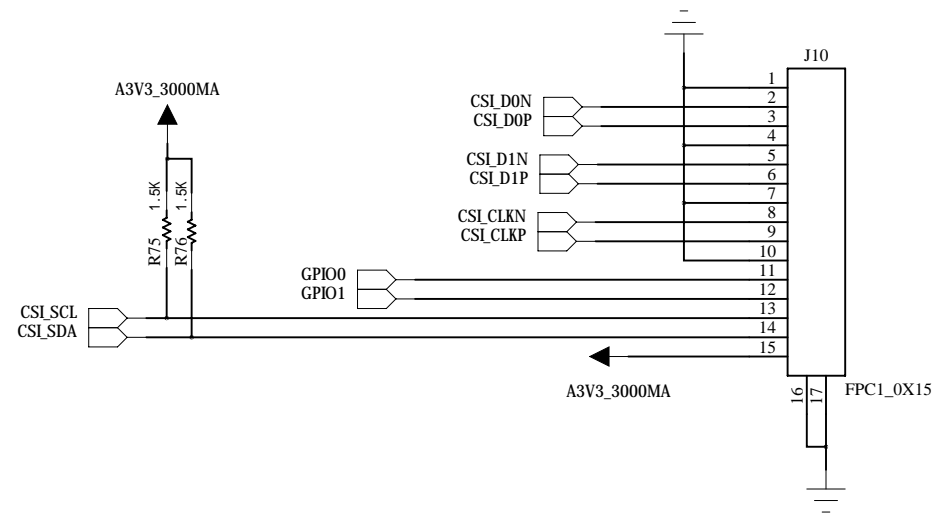
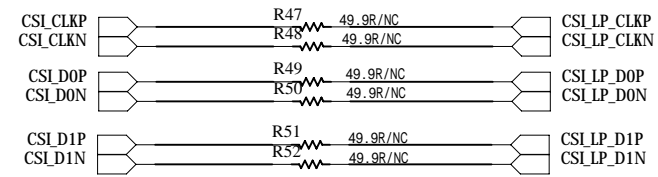
MIPI_DSI



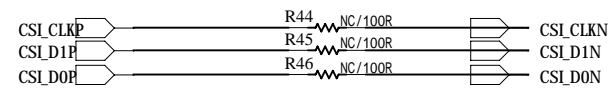
C

B

MIPI_CSI



CSI端接电阻，靠近FPGA



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6

5

4

3

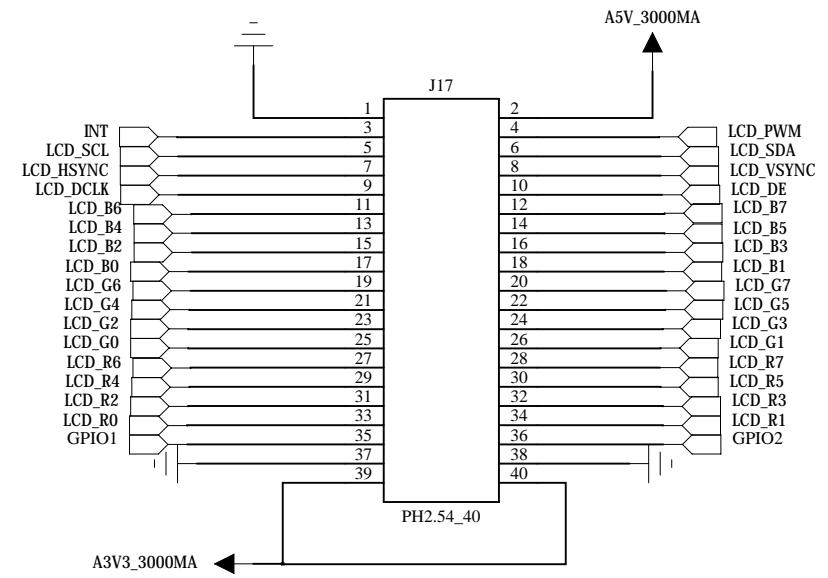
2

1

RGB_LCD

D

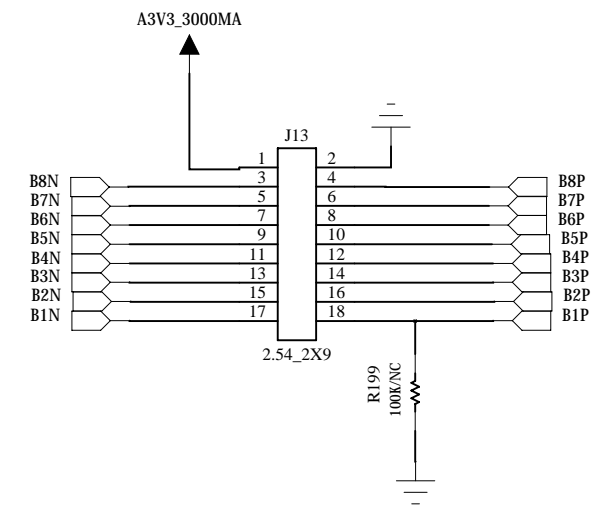
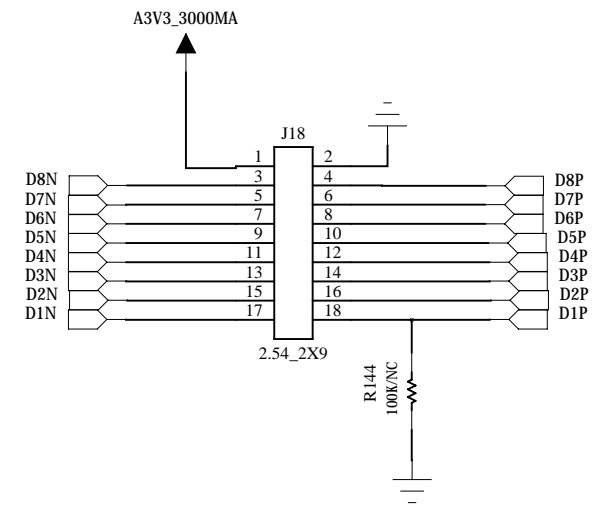
C



Pin11/12——Pin33/34是12对差分对引脚，单数pin为DP，双数pin为DN，可复用为LVDS_TX或其他

B

PMOS

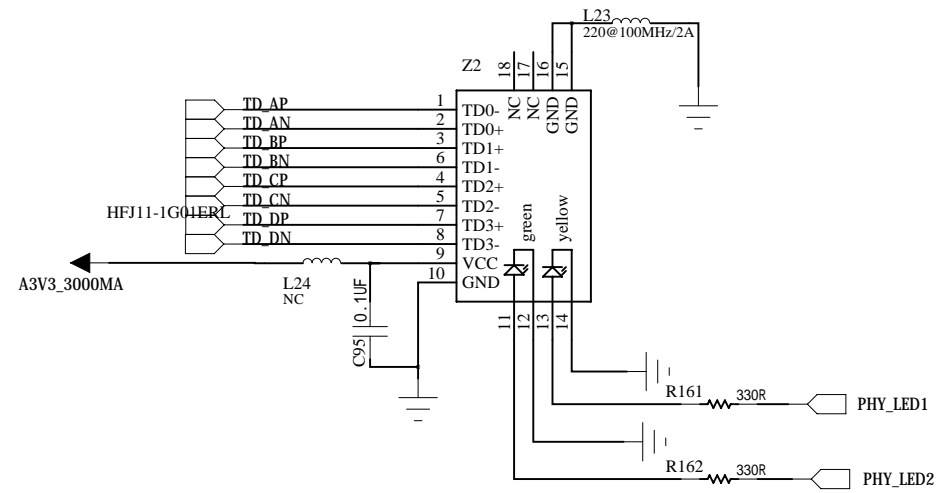


A

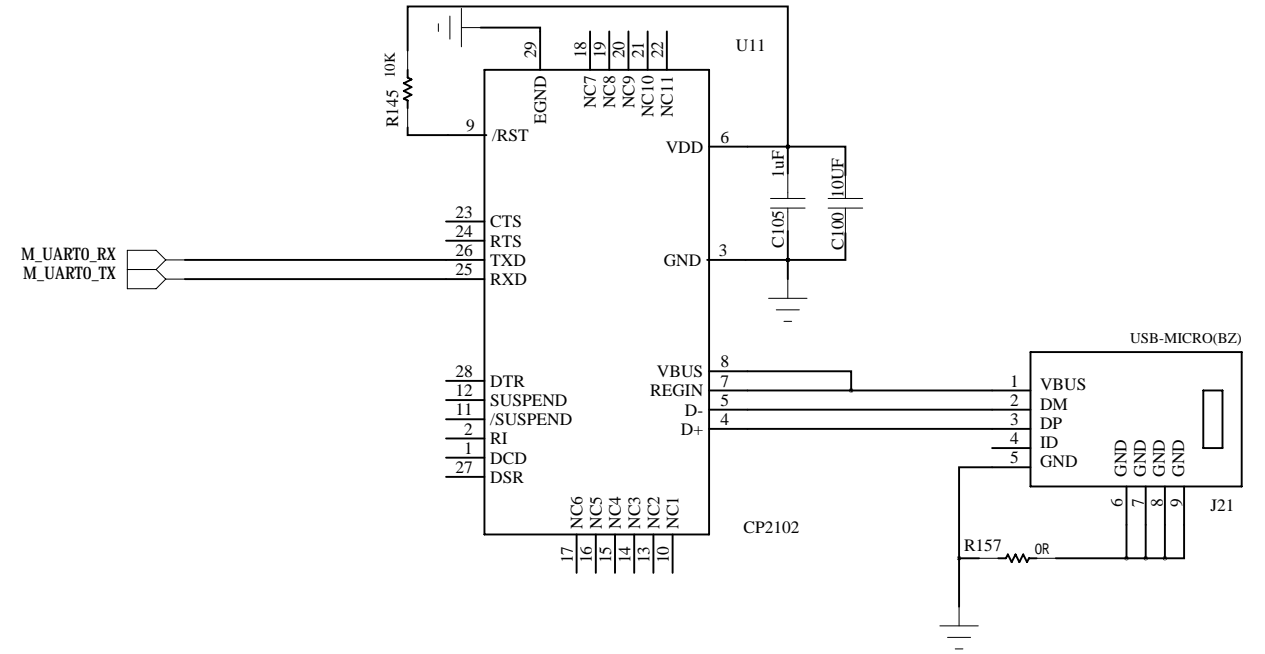
Title: MINI_EYE_GW2A18_PG484	
Drawing No:	Version: V1.0
Drawn By:	Date: 20190312
Checked By:	Date:
Approved By:	Date:
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D

C

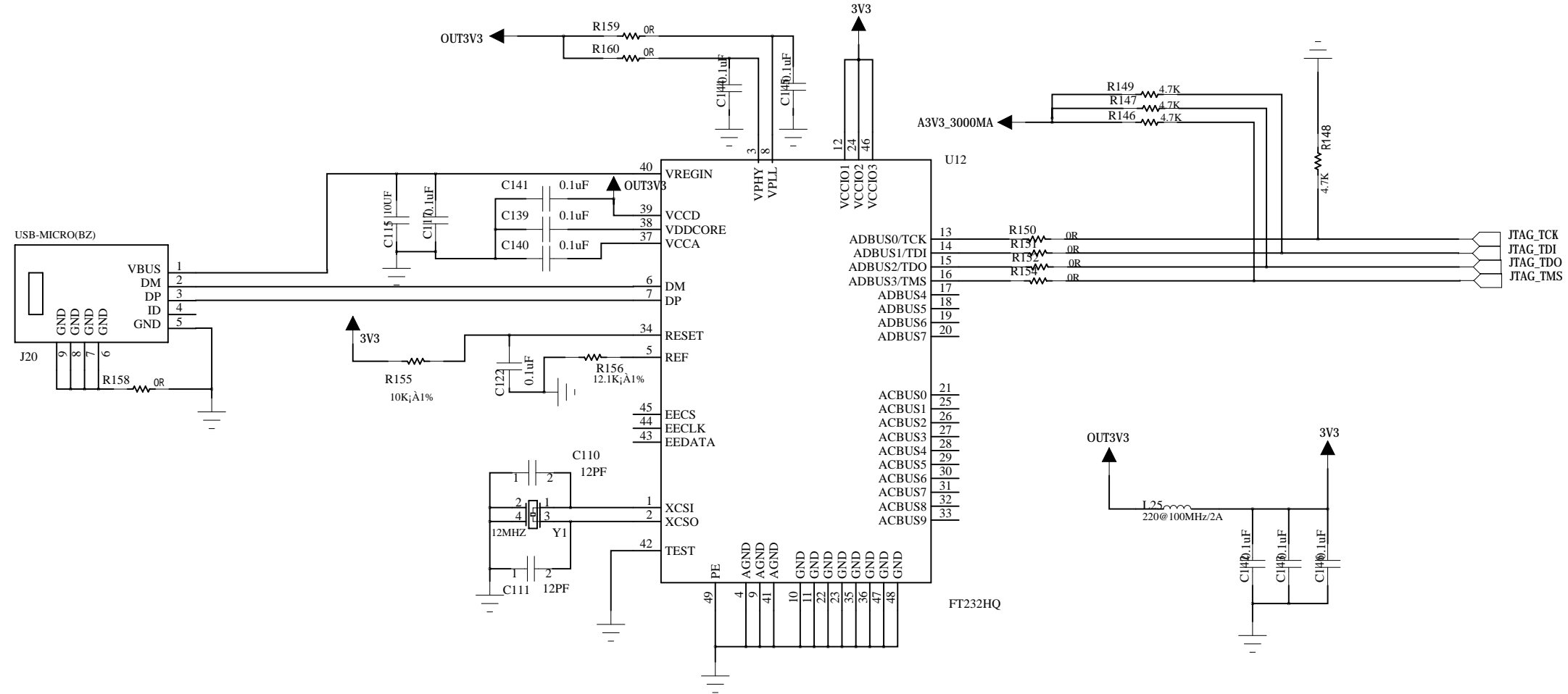


UART-USB



B

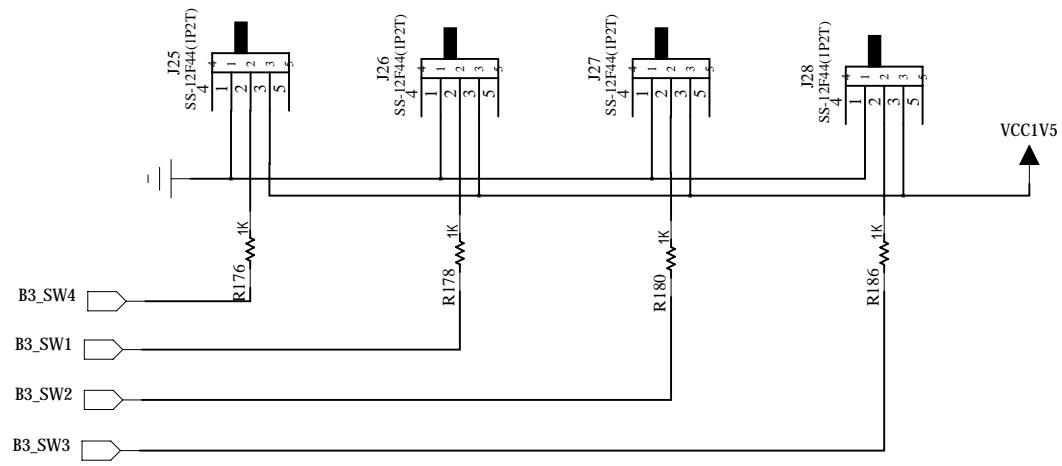
JTAG-USB



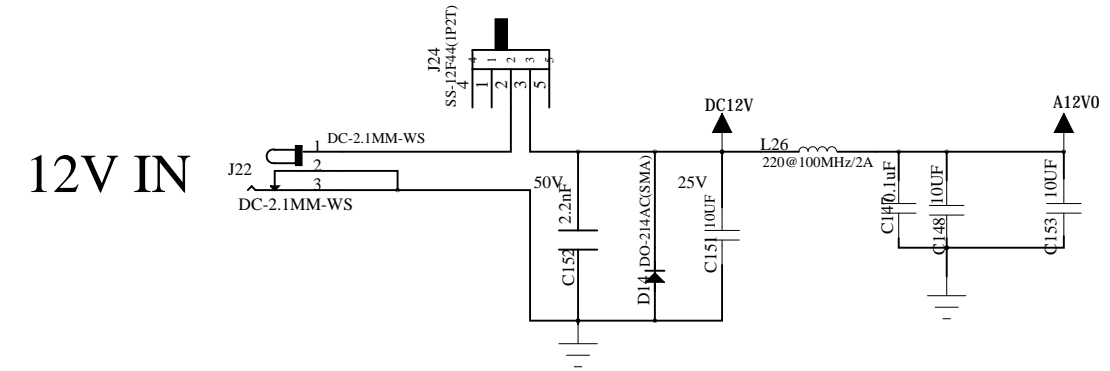
A

Title: MINI_EYE_GW2A18_PG484	
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Size: A3	Sheet: 2/5

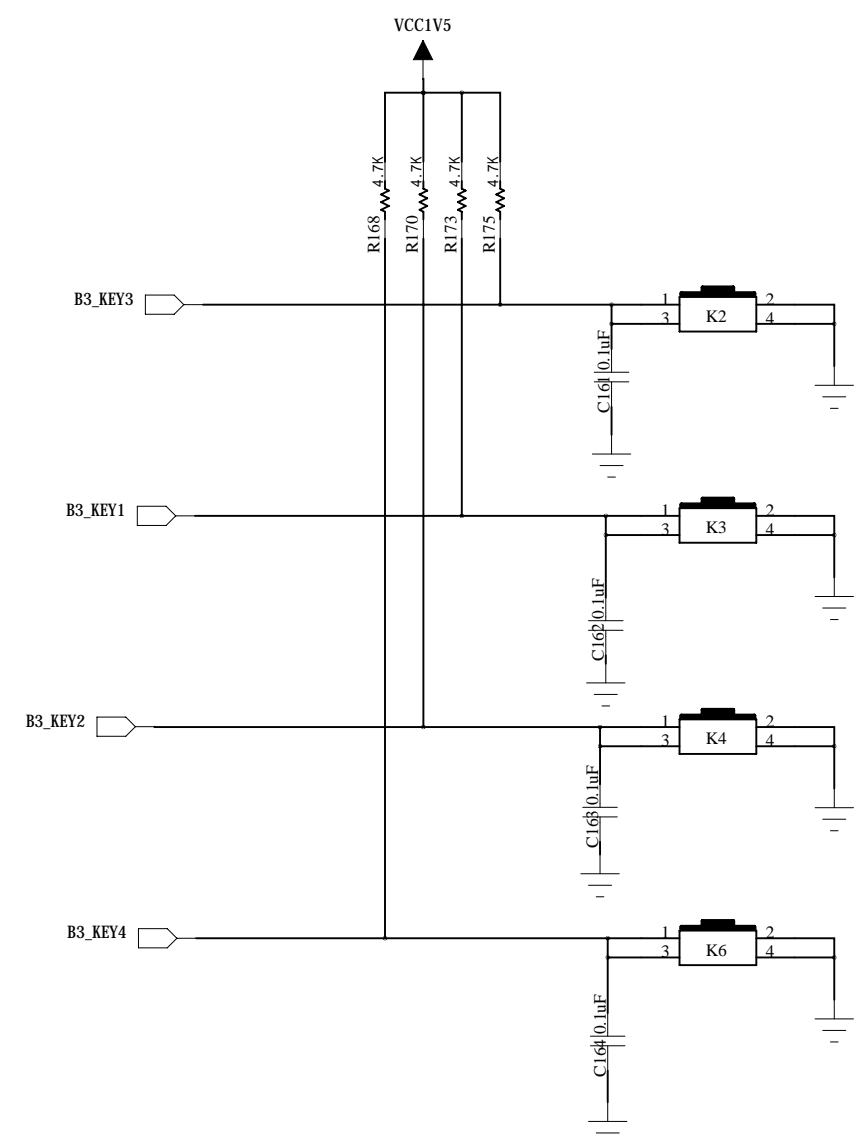
D



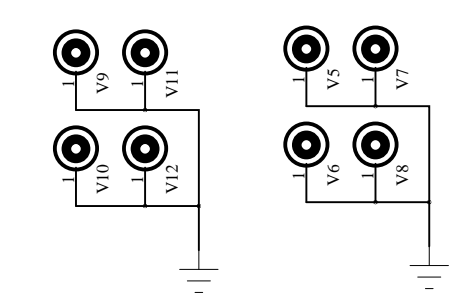
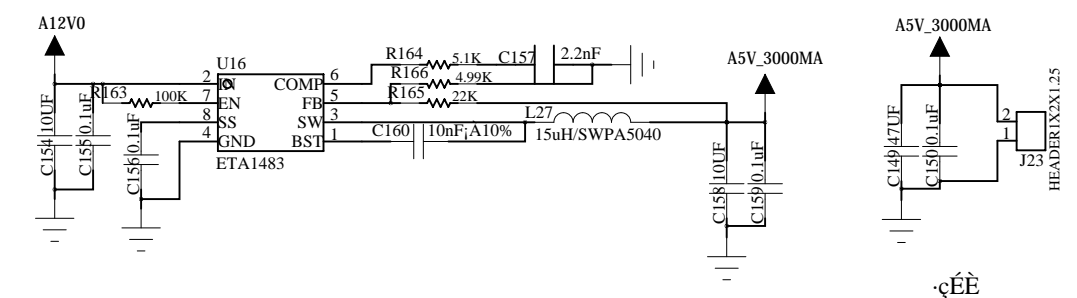
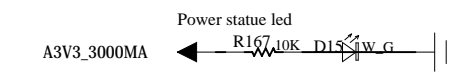
C



B



A



Title: MINI_EYE_GW2A18_PG484	
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