GOWIN高云

智慧逻辑 定制未来

GW2A series of FPGA Products

Data Sheet

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Revision History

Date	Version	Description
08/31/2016	1.00E	Initial version published.
06/01/2018	1.1E	● Information about the multiplexing of the MODE pin added. ● PLL Structure diagram updated.
08/29/2018	1.2E	● MG196 PG256S added. ● Description of the state of GPIOs for blank chips added. ● QN88 information and GW2A-18 PLL list added.
04/02/2019	1.3E	● Recommended Operating Conditions updated. ● Operating temperature changed to Junction temperature. ● The figure of part naming updated. ● The PG256C package added.
04/12/2019	1.4E	The EQ144 package added.
07/02/2019	1.5E	GW2A-55 UG324 added.
09/19/2019	1.6E	● GW2A-18 UG324 added. ● Power supply ramp rates updated.
09/27/2019	1.7E	Junction temperature of automotive operation updated.
10/12/2019	1.8E	● The package sizes of LQ144/EQ144 fixed. ● Part naming examples optimized.
11/12/2019	1.9E	● The number of Maximum I/Os updated. ● Description of IODELAY updated.
12/13/2019	2.0E	● GW2A-18 PG256E added. ● GW2A-55 UG324D added.
03/09/2020	2.1E	GW2A-18C and GW2A-55C added.
04/16/2020	2.1.1E	● I/O Information of GW2A-55 UG324 updated. ● CFU structure view updated. ● Note for “I/O Operating Conditions Recommended” added.
07/07/2020	2.1.2E	● The recommended minimum value of V_{CCX} revised. ● PLL switching characteristics updated. ● Description of package marking examples added.
09/25/2020	2.2E	GW2A-55 UG676 added.
05/25/2021	2.2.1E	Electrical parameters optimized.
07/16/2021	2.3E	GW2A-18 UG484/PG256CF added.
12/27/2021	2.3.1E	● GW2A-18 PG256SF added. ● GW2A-55 UG324F added. ● Description of I/O logic optimized.
02/17/2022	2.3.2E	Information on I/O standards optimized.
05/25/2022	2.3.3E	● Recommended I/O operating conditions updated. ● Power supply ramp rates updated.
09/05/2022	2.3.4E	● The maximum value of the differential input threshold V_{THD} updated. ● Note about DC current limit added. ● Table 3-3 Power Supply Ramp Rates updated. ● Table 3-8 DC Electrical Characteristics over Recommended Operating Conditions updated. ● Figure 2-1 Architecture Overview updated.
09/15/2022	2.4E	● GW2A-55 UG484S added. ● Table 3-5 POR Parameters updated.
10/28/2022	2.5E	GW2A-18 PG484C added.
11/11/2022	2.5.1E	● Table 3-8 DC Electrical Characteristics over Recommended Operating Conditions updated.

Date	Version	Description
		● Section 3.4.4 Byte-enable removed.
01/12/2023	2.5.2E	● Table 3-1 Absolute Max. Ratings updated. ● Table 1-3 Device-Package Combinations, Maximum User I/Os, and True LVDS Pairs updated. ● Table 3-8 DC Electrical Characteristics over Recommended Operating Conditions updated.
03/16/2023	2.6E	● GW2A-18 LQ144 removed. ● Information on Slew Rate removed. ● Table 3-3 Power Supply Ramp Rates updated. ● Note about the default state of GPIOs modified.
05/11/2023	2.6.1E	● 2.4.2Memory Configuration Modes added. ● Table 3-17 External Switching Characteristics updated. ● Table 3-18 I/O Register Parameters Using Dedicated GCLK Input through GCLK Tree without PLL added.
05/25/2023	2.6.2E	● Table 3-13 CFU Timing Parameters updated. ● Table 3-14 BSRAM Timing Parameters updated. ● Table 3-15 DSP Timing Parameters updated.
07/26/2023	2.6.3E	● Table 1-3 Device-Package Combinations, Maximum User I/Os, and True LVDS Pairs updated, correcting the maximum numbers of user IOs of the GW2A-55 device in UG324, UG324F, and UG324D packages. ● Figure 4-3 Package Marking Examples updated. ● Note about the default state of GPIOs optimized.
08/18/2023	2.7E	● The I/O logic output diagram and the I/O logic input diagram combined into Figure 2-5 I/O Logic Input and Output. ● Note for Table 3-8 DC Electrical Characteristics over Recommended Operating Conditions modified. ● Figure 4-3 Package Marking Examples updated. ● Editorial updates.
09/20/2023	2.7.1E	● Information on speed grade C9/I8 removed. ● Section 2.4.6 Power up Conditions removed. ● Table 3-18 I/O Register Parameters Using Dedicated GCLK Input through GCLK Tree without PLL corrected.
03/01/2024	2.7.2E	● “Table 1-1 Product Resources” updated. ● Description of IODELAY module updated. ● Description of DES module optimized. ● Note about ripple added to “Table 3-2 Recommended Operating Conditions”. ● “Table 3-16 Gearbox Timing Parameters” added.

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1 General Description

The GW2A series of FPGA products are the first generation products of the Arora family, featuring high-performance DSP resources, high-speed LVDS interfaces, and abundant BSRAM memory resources. These embedded resources combined with a streamlined FPGA architecture and 55nm process make the GW2A series of FPGA products an ideal solution for high-speed and low-cost applications.

GOWINSEMI provides a new generation of FPGA hardware development environment that supports FPGA synthesis, placement & routing, bitstream generation and download, etc.

1.1 Features

- Lower power consumption
  - 55nm SRAM process
  - Core voltage: 1.0V
  - Supports dynamically turning on/off the clock
- Multiple I/O standards
  - LVCMOS33/25/18/15/12；LVTTL33,SSTL33/25/18 I, II, SSTL15；HSTL18 I, II, HSTL15 I；PCI, LVDS25, RSDS, LVDS25E, BLVDSE, MLVDSE, LVPECLE, RSDSE
  - Input hysteresis options
  - Drive strength options
  - Individual Bus Keeper, Pull-up/Pull-down, and Open Drain options
  - Hot socketing
- High-performance DSP blocks
  - High-performance digital signal processing
  - Supports 9 x 9,18 x 18,36 x 36 bit multipliers and 54-bit accumulators
  - Supports cascading of multipliers
  - Supports pipeline mode and bypass mode
  - Pre-addition operation for the filter function
  - Supports barrel shifters
- Abundant basic logic cells
  - 4-input LUTs (LUT4s)
  - Supports shift registers and shadow SRAMs
- Block SRAMs with multiple modes
  - Supports Dual Port mode, Single Port mode, and Semi-Dual Port mode
- Flexible PLLs
  - Frequency adjustment (multiplication and division) and phase adjustment
  - Supports global clocks
- Configuration
  - JTAG configuration
  - Four GowinCONFIG configuration modes: SSPI,

MSPI, CPU, SERIAL
- Supports programming the SPI Flash directly in JTAG and SSPI modes; For other modes, you can program the SPI Flash using an IP
- Supports bitstream file encryption and security bit settings

1.2 Product Resources

Table 1-1 Product Resources

Device	GW2A-18	GW2A-55
LUT4s	20,736	54,720
Flip-Flops (FFs)	15,552	41,040
Shadow SRAM(SSRAM) Capacity (bits)	40K	106K
Block SRAM(BSRAM) Capacity(bits)	828K	2,520K
Number of BSRAMs	46	140
Multipliers(18 x 18 Multipliers)	48	40
Maximum PLLs[1]	4	6
I/O Banks	8	8
Maximum GPIOs	384	608
Core voltage	1.0V	1.0V

Note!

[1] Different packages support different numbers of PLLs. Up to six PLLs can be supported.

Table 1-2 GW2A-18 PLL List

Package	Device	Available PLLs
EQ144	GW2A-18	PLLL0/PLLL1/PLLR0/PLLR1
MG196	GW2A-18	PLLL0/PLLL1/PLLR0/PLLR1
QN88	GW2A-18	PLLL1/PLLR1
PG256/ PG256S/ PG256C/ PG256CF/ PG256E/ PG256SF	GW2A-18	PLLL0/PLLL1/PLLR0/PLLR1
PG484/ PG484C	GW2A-18	PLLL0/PLLL1/PLLR0/PLLR1
UG324	GW2A-18	PLLL0/PLLL1/PLLR0/PLLR1
UG484	GW2A-18	PLLL0/PLLL1/PLLR0/PLLR1

Table 1-3 Device-Package Combinations, Maximum User I/Os, and True LVDS Pairs

Package	Pitch (mm)	Size (mm)	E-pad Size (mm)	GW2A-18	GW2A-55
QN88	0.4	10 x10	6.74 x 6.74	66（22）	–
EQ144	0.5	20 x 20	9.74 x 9.74	119（34）	–
MG196	0.5	8 x 8	–	114（39）	–
PG256	1.0	17 x 17	–	207（73）	–
PG256S	1.0	17 x 17	–	192（72）	–
PG256SF	1.0	17 x 17	–	192（71）	–
PG256C	1.0	17 x 17	–	190（64）	–
PG256CF	1.0	17 x 17	–	190（65）	–
PG256E	1.0	17 x 17	–	162（29）	–
PG484	1.0	23 x 23	–	319（78）	319（76）
PG484C	1.0	23 x 23	–	355（89）	–
PG1156	1.0	35 x 35	–	–	607（97）
UG324	0.8	15 x 15	–	239（90）	239（86）
UG324F	0.8	15 x 15	–	-	239（86）
UG324D	0.8	15 x 15	–	–	239（71）
UG484	0.8	19 x 19	–	379（94）	–
UG484S	0.8	19 x 19	–	–	344（91）
UG676	0.8	21 x 21	–	–	525（97）

Note!

- The package types in this manual are referred to by abbreviations, see 4.1 Part Naming for more information.
- JTAGSEL_N and JTAG pins cannot be used as GPIOs simultaneously. The number of maximum user I/Os noted in this table is referred to when the four JTAG pins (TCK, TDI, TDO, and TMS) are used as GPIOs. See UG111, GW2A series of FPGA Products Package and Pinout for more details.
- The speed of the JTAG pins multiplexed as GPIOs is less than 40MHz.

2 Architecture

2.1 Architecture Overview

Figure 2-1 Architecture Overview

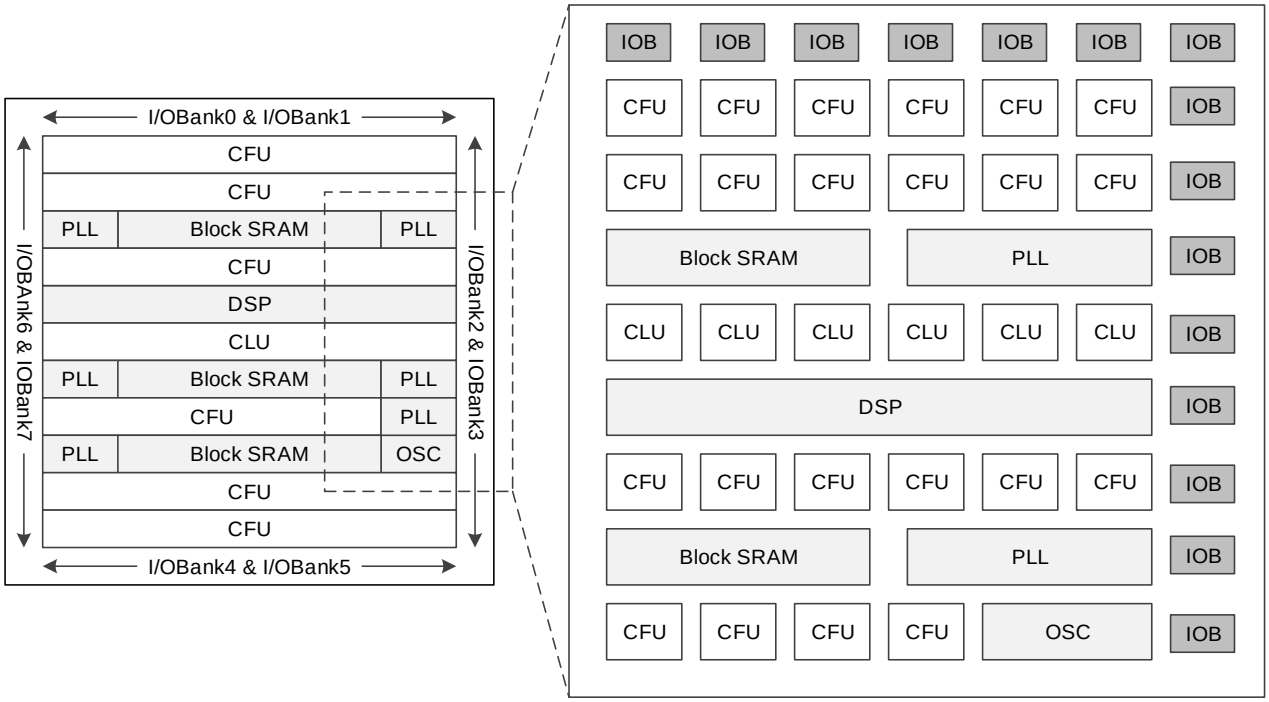


Figure 2-1 shows an overview of the architecture of the GW2A series of FPGA products, see Table 1-1 for more information. The core of the FPGA is an array of logic cells surrounded by IO blocks. Besides, BSRAMs, DSP blocks, PLLs, and an on-chip oscillator are provided.

The Configurable Function Unit (CFU) and the Configurable Logic Unit (CLU) are the two kinds of basic logic blocks that form the core of Gowin FPGAs. Devices with different capacities have different numbers of rows and columns of CFUs/CLUs. For more information, see 2.2 Configurable Function Units.

The I/O resources in the GW2A series of FPGA products are arranged

around the periphery of the devices in groups referred to as banks, which are divided into eight banks, including Bank0 - Bank7. The I/O resources support multiple I/O standards and can be used for regular mode, SDR mode, generic DDR mode, and DDR_MEM mode. For more information, see 2.3 Input/Output Blocks.

BSRAMs are embedded as a row in the GW2A series of FPGA products. Each BSRAM occupies 3 CFU locations. Each BSRAM has a capacity of 18Kbits and supports multiple configuration modes and operation modes. For more information, see 2.4 Block SRAM.

The GW2A series of FPGA products provide DSP blocks. DSP blocks are embedded as a row in the GW2A series of FPGA products. Each DSP block occupies 9 CFU locations. Each DSP block contains two macros, and each macro contains two pre-adders, two 18 x 18 bit multipliers, and one three-input ALU. For more information, see 2.5 Digital Signal Processing.

The GW2A series of FPGA products have embedded PLL resources. PLL blocks provide the ability to synthesize clock frequencies. Frequency adjustment (multiplication and division), phase adjustment, and duty cycle adjustment can be realized by the configuration of parameters. These FPGAs have an embedded programmable on-chip clock oscillator that supports clock frequencies ranging from 2.5 MHz to 105MHz, providing clocking resources for the MSPI mode. For more information, see 2.10 On-chip Oscillator.

There are also abundant Configurable Routing Units (CRUs) that interconnect all the resources within the FPGA. For example, routing resources distributed in CFUs and IOBs interconnect resources in them. Routing resources can be automatically generated by the Gowin software. In addition, the GW2A series of FPGA products also provide abundant dedicated clock resources, long wires (LWs), global set/reset (GSR) resources, programming options, etc. For more details, see 2.5.2 DSP Operation Modes, 2.7 Long Wires, and 2.8 Global Set/Reset.

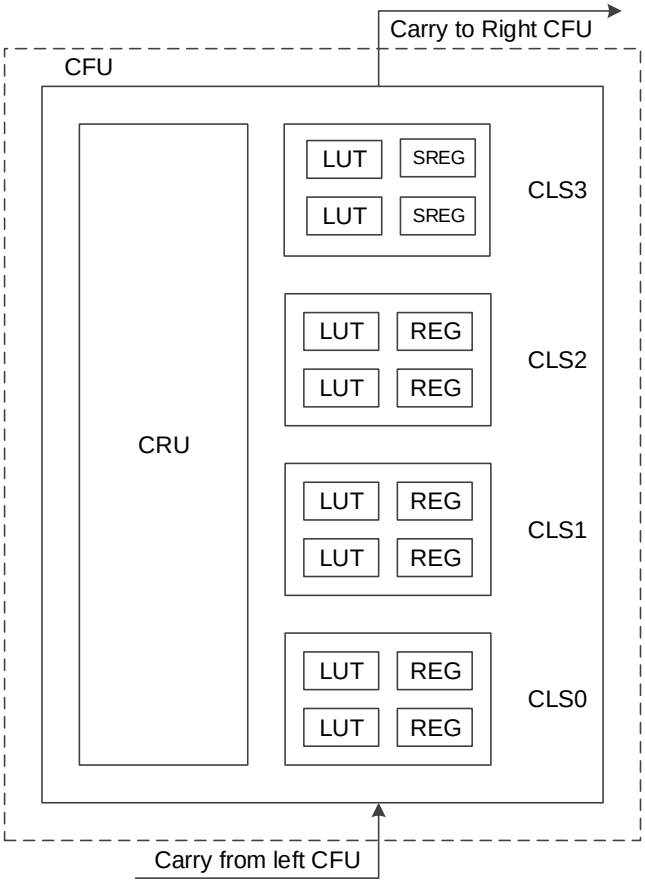
2.2 Configurable Function Units

Configurable Function Units (CFUs) and/or Configurable Logic Units (CLUs) are the basic cells for the core of GOWINSEMI FPGA Products. Each basic cell consists of four Configurable Logic Sections (CLSs) and their routing resource Configurable Routing Units (CRUs). Each of the three CLSs contains two 4-input LUTs and two registers, and the other one only contains two 4-input LUTs, as shown in Figure 2-2 .

The CLSs in the CLUs cannot be configured as SRAMs, but can be configured as basic LUTs, ALUs, and ROMs. The CLSs in the CFUs can be configured as basic LUTs, ALUs, SRAMs, and ROMs according to application scenarios.

For more information on the CFUs, see UG288, Gowin Configurable Function Unit (CFU) User Guide.

Figure 2-2 CFU Structure View



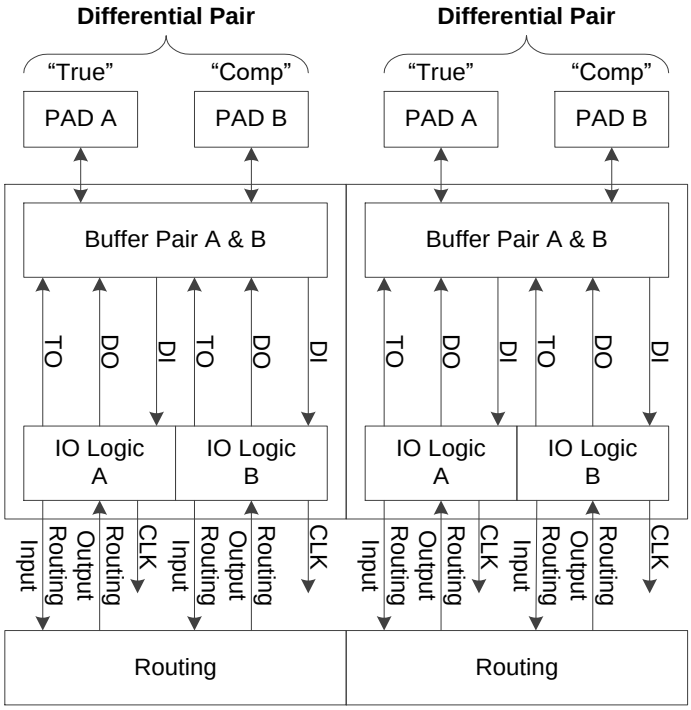
Note!

The SREGs need special patch support. Please contact Gowin's technical support or local office for this patch.

2.3 Input/Output Blocks

The Input/Output Block (IOB) in the GW2A series of FPGA products consists a buffer pair, IO logic, and corresponding routing units. As shown below, each IOB connects to two pins (marked as A and B), which can be used as a differential pair or as two single-ended inputs/outputs.

Figure 2-3 IOB Structure View



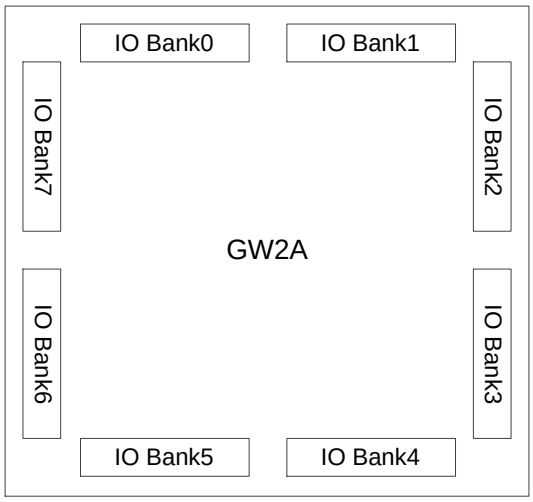
The features of the IOB include:

- V_{CCIO} supplied with each bank
- LVCMOS, PCI, LVTTL, LVDS, SSTL, HSTL, etc.
- Input hysteresis options
- Drive strength options
- Individual Bus Keeper, Pull-up/Pull-down, and Open Drain options
- Hot socketing
- IO logic supports basic mode, SDR mode, DDR mode, etc.
  2.3.1 - 2.3.3 describe I/O standards, I/O logic, and I/O logic modes. For more information about the IOB, please refer to UG289,Gowin Programmable IO (GPIO) User Guide.

2.3.1 I/O Standards

There are eight I/O Banks in the GW2A series of FPGA products, as shown in Figure 2-4. Each Bank has its own I/O power supply V_{CCIO}. V_{CCIO} can be 3.3V, 2.5V, 1.8V, 1.5V, or 1.2V. To support SSTL, HSTL, etc., each bank also has one independent voltage source (V_{REF}) as the reference voltage. You can choose to use the internal V_{REF} (0.5 x V_{CCIO}) or the external V_{REF} input via any IO from the bank. V_{CCX} supports 2.7V and 3.3V.

Figure 2-4 I/O Bank Distribution View of GW2A



Different banks in the GW2A series of FPGA Products support different on-die termination settings, including single-ended resistors and differential resistors. Single-ended resistors are set for SSTL/HSTL input/output and are supported in Bank2/3/6/7. Differential resistors are set for LVDS input and are only supported in Bank 0/1, see UG289, Gowin Programmable IO User Guide for more details.

Note!

During configuration, all GPIOs of the device are high-impedance with internal weak pull-ups. After the configuration is complete, the I/O states are controlled by user programs and constraints. The states of configuration-related I/Os differ depending on the configuration mode.

For the V_{CCIO} requirements of different I/O standards, see Table2-1 and Table 2-2.

Table2-1 Output I/O Standards and Configuration Options

I/O standard (output)	Single-ended/Differential	Bank V_{CCIO}(V)	Drive Strength (mA)	Typical Applications
LVTTL33	Single-ended	3.3	4,8,12,16,24	Universal interface
LVCMOS33	Single-ended	3.3	4,8,12,16,24	Universal interface
LVCMOS25	Single-ended	2.5	4,8,12,16	Universal interface
LVCMOS18	Single-ended	1.8	4,8,12	Universal interface
LVCMOS15	Single-ended	1.5	4,8	Universal interface
LVCMOS12	Single-ended	1.2	4,8	Universal interface
SSTL25_I	Single-ended	2.5	8	Memory interface
SSTL25_II	Single-ended	2.5	8	Memory interface
SSTL33_I	Single-ended	3.3	8	Memory interface
SSTL33_II	Single-ended	3.3	8	Memory interface
SSTL18_I	Single-ended	1.8	8	Memory interface
SSTL18_II	Single-ended	1.8	8	Memory interface
SSTL15	Single-ended	1.5	8	Memory interface

I/O standard (output)	Single-ended/Differential	Bank V_{CCIO}(V)	Drive Strength (mA)	Typical Applications
HSTL18_I	Single-ended	1.8	8	Memory interface
HSTL18_II	Single-ended	1.8	8	Memory interface
HSTL15_I	Single-ended	1.5	8	Memory interface
PCI33	Single-ended	3.3	N/A	PC and embedded system
LVPECL33E	Differential	3.3	16	High-speed data transmission
MLVDS25E	Differential	2.5	16	LCD timing driver interface and column driver interface
BLVDS25E	Differential	2.5	16	Multi-point high-speed data transmission
RSDS25E	Differential	2.5	8	High-speed point-to-point data transmission
LVDS25E	Differential	2.5	8	High-speed point-to-point data transmission
LVDS25	Differential(TLVDS)	2.5/3.3	3.5/2.5/2/1.25	High-speed point-to-point data transmission
RSDS	Differential(TLVDS)	2.5/3.3	2	High-speed point-to-point data transmission
MINILVDS	Differential(TLVDS)	2.5/3.3	2	LCD timing driver interface and column driver interface
PPLVDS	Differential(TLVDS)	2.5/3.3	3.5	LCD row/column driver
SSTL15D	Differential	1.5	8	Memory interface
SSTL25D_I	Differential	2.5	8	Memory interface
SSTL25D_II	Differential	2.5	8	Memory interface
SSTL33D_I	Differential	3.3	8	Memory interface
SSTL33D_II	Differential	3.3	8	Memory interface
SSTL18D_I	Differential	1.8	8	Memory interface
SSTL18D_II	Differential	1.8	8	Memory interface
HSTL18D_I	Differential	1.8	8	Memory interface
HSTL18D_II	Differential	1.8	8	Memory interface
HSTL15D_I	Differential	1.5	8	Memory interface
LVCMOS12D	Differential	1.2	8/4	Universal interface
LVCMOS15D	Differential	1.5	8/4	Universal interface
LVCMOS18D	Differential	1.8	8/12/4	Universal interface
LVCMOS25D	Differential	2.5	8/16/12/4	Universal interface

I/O standard (output)	Single-ended/Differential	Bank V_{CCIO}(V)	Drive Strength (mA)	Typical Applications
LVCMOS33D	Differential	3.3	8/24/16/12/4	Universal interface

Table 2-2 Input I/O Standards and Configuration Options supported by GW2A

I/O standard (input)	Single-ended/Differential	Bank V_{CCIO}(V)	Supports Hysteresis Options?	Needs V_{REF}?
LVTTL33	Single-ended	1.2/1.5/1.8/2.5/3.3	Yes	No
LVCMOS33	Single-ended	1.2/1.5/1.8/2.5/3.3	Yes	No
LVCMOS25	Single-ended	1.2/1.5/1.8/2.5/3.3	Yes	No
LVCMOS18	Single-ended	1.2/1.5/1.8/2.5/3.3	Yes	No
LVCMOS15	Single-ended	1.2/1.5/1.8/2.5/3.3	Yes	No
LVCMOS12	Single-ended	1.2/1.5/1.8/2.5/3.3	Yes	No
SSTL15	Single-ended	1.5/1.8/2.5/3.3	No	Yes
SSTL25_I	Single-ended	2.5/3.3	No	Yes
SSTL25_II	Single-ended	2.5/3.3	No	Yes
SSTL33_I	Single-ended	3.3	No	Yes
SSTL33_II	Single-ended	3.3	No	Yes
SSTL18_I	Single-ended	1.8/2.5/3.3	No	Yes
SSTL18_II	Single-ended	1.8/2.5/3.3	No	Yes
HSTL18_I	Single-ended	1.8/2.5/3.3	No	Yes
HSTL18_II	Single-ended	1.8/2.5/3.3	No	Yes
HSTL15_I	Single-ended	1.5/1.8/2.5/3.3	No	Yes
PCI33	Single-ended	3.3	Yes	No
LVCMOS33OD25	Single-ended	2.5	No	No
LVCMOS33OD18	Single-ended	1.8	No	No
LVCMOS33OD15	Single-ended	1.5	No	No
LVCMOS25OD18	Single-ended	1.8	No	No
LVCMOS25OD15	Single-ended	1.5	No	No
LVCMOS18OD15	Single-ended	1.5	No	No

I/O standard (input)	Single-ended/Differential	Bank V_{CCIO}(V)	Supports Hysteresis Options?	Needs V_{REF}?
LVCMOS15OD12	Single-ended	1.2	No	No
LVCMOS25UD33	Single-ended	3.3	No	No
LVCMOS18UD25	Single-ended	2.5	No	No
LVCMOS18UD33	Single-ended	3.3	No	No
LVCMOS15UD18	Single-ended	1.8	No	No
LVCMOS15UD25	Single-ended	2.5	No	No
LVCMOS15UD33	Single-ended	3.3	No	No
LVCMOS12UD15	Single-ended	1.5	No	No
LVCMOS12UD18	Single-ended	1.8	No	No
LVCMOS12UD25	Single-ended	2.5	No	No
LVCMOS12UD33	Single-ended	3.3	No	No
LVDS25	Differential	2.5/3.3	No	No
RSDS	Differential	2.5/3.3	No	No
MINILVDS	Differential	2.5/3.3	No	No
PPLVDS	Differential	2.5/3.3	No	No
LVDS25E	Differential	2.5/3.3	No	No
MLVDS25E	Differential	2.5/3.3	No	No
BLVDS25E	Differential	2.5/3.3	No	No
RSDS25E	Differential	2.5/3.3	No	No
LVPECL33E	Differential	3.3	No	No
SSTL15D	Differential	1.5/1.8/2.5/3.3	No	No
SSTL25D_I	Differential	2.5/3.3	No	No
SSTL25D_II	Differential	2.5/3.3	No	No
SSTL33D_I	Differential	3.3	No	No
SSTL33D_II	Differential	3.3	No	No
SSTL18D_I	Differential	1.8/2.5/3.3	No	No
SSTL18D_II	Differential	1.8/2.5/3.3	No	No
HSTL18D_I	Differential	1.8/2.5/3.3	No	No
HSTL18D_II	Differential	1.8/2.5/3.3	No	No
HSTL15D_I	Differential	1.5/1.8/2.5/3.3	No	No
LVCMOS12D	Differential	1.2/1.5/1.8/2.5/3.3	No	No
LVCMOS15D	Differential	1.5/1.8/2.5/3.3	No	No
LVCMOS18D	Differential	1.8/2.5/3.3	No	No

I/O standard (input)	Single-ended/Differential	Bank V_{CCIO}(V)	Supports Hysteresis Options?	Needs V_{REF}?
LVCMOS25D	Differential	2.5/3.3	No	No
LVCMOS33D	Differential	3.3	No	No

2.3.2 I/O Logic

Figure 2-5 shows the I/O logic input and output of the GW2A series of FPGA products.

Figure 2-5 I/O Logic Input and Output

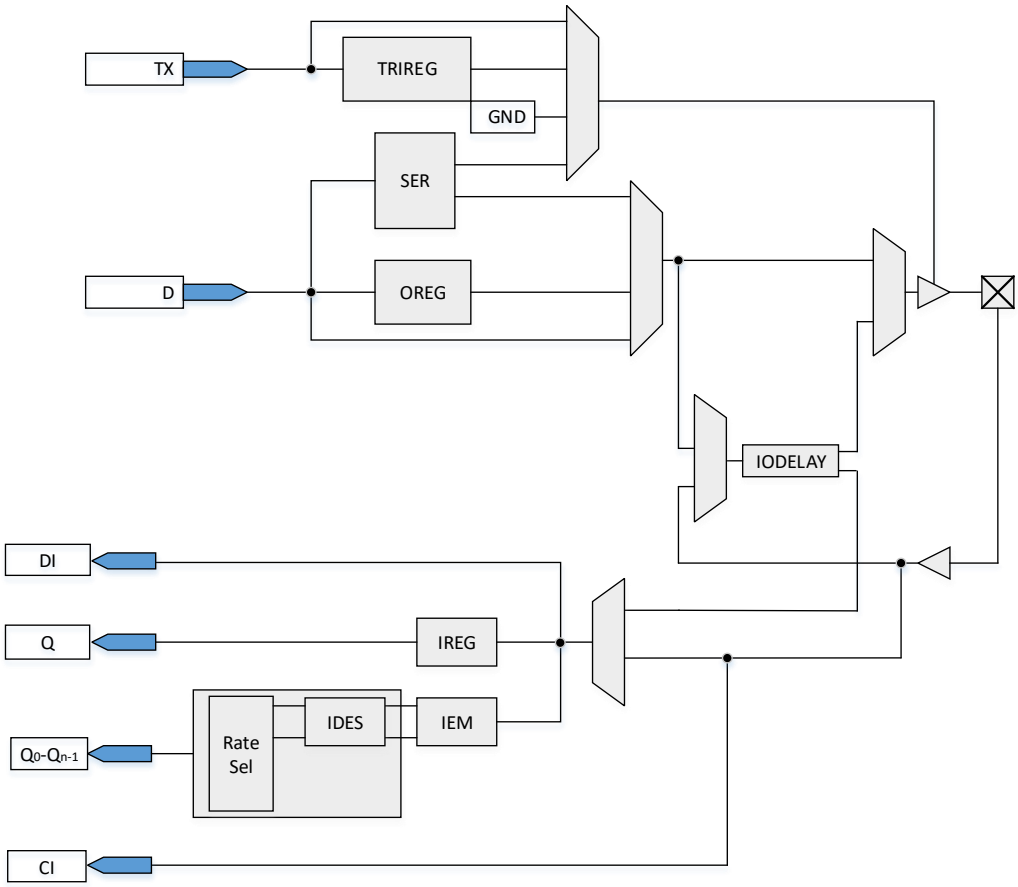


Table 2-3 Port Description

Port	I/O	Description
CI[1]	Input	GCLK input signal. For the number of GCLK input signals, please refer to UG110，GW2A-18 Pinout and UG113，GW2A-55 Pinout .
DI	Input	IO port low-speed input signal input into the fabric directly.
Q	Output	IREG output signal in the SDR module.
Q_0-Q_{n-1}	Output	IDES output signal in the DDR module.

Note!

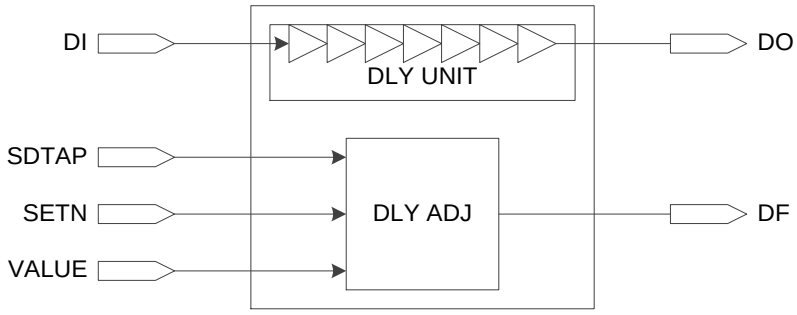
When CI is used as GCLK input, DI, Q, and Q0-Qn-1 cannot be used as I/O input and output.

Descriptions of the I/O logic modules of the GW2A series of FPGA products are presented below.

IODELAY

See Figure 2-6 for an overview of the IODELAY module. Each I/O of the GW2A series of FPGA products has an IODELAY module, providing a total of 128(0~127) steps of delay, with one step of delay time being about 18ps(GW2A-18) or 22ps(GW2A-55).

Figure 2-6 IODELAY Diagram



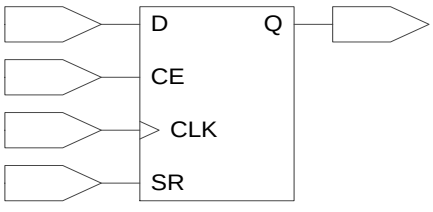
There are two ways to control the delay:

- Static control.
- Dynamic control: can be used with the IEM module to adjust the dynamic sampling window. Please note the IODELAY module cannot be used for both input and output at the same time.

I/O Register

See Figure 2-7 for the I/O register in the GW2A series of FPGA products. Each I/O provides one input register (IREG), one output register (OREG), and one tristate register (TRIREG).

Figure 2-7 I/O Register Diagram



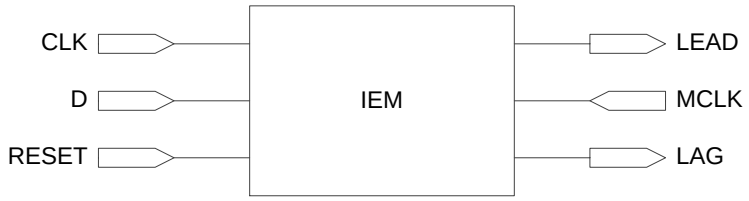
Note!

- CE can be programmed as either active low (0: enable) or active high (1: enable).
- CLK can be programmed as either rising edge triggering or falling edge triggering.
- SR can be programmed as either synchronous/asynchronous SET/RESET or disabled.
- The register can be programmed as a register or a latch.

IEM

The IEM(Input Edge Monitor) module is used to sample data edges and is used in generic DDR mode, as shown in Figure 2-8.

Figure 2-8 IEM Diagram



Deserializer(DES) and Clock Domain Transfer

This series of FPGA products provide a simple deserializer(DES) for input I/O logic to support advanced I/O protocols. The clock domain transfer module of the input clock in DES provides the ability to safely switch the external sampling clock(strobe) domain to the internal continuously running clock domain. There are multiple registers used for data sampling.

The clock domain transfer module offers the following functions:

- Uses the internal continuous clock instead of the discontinuous DQS signal for data sampling. This feature applies to the DDR memory interface.
- For the DDR3 memory interface standard, aligns the DQS signal and data by read-leveling.
- In generic DDR mode, when DQS.RCLK is used for sampling, the clock domain transfer module is also required.

Each DQS module provides WADDR and RADDR signals for the clock domain transfer modules in the same group.

SER

This series of FPGA products provide a simple serializer(SER) for output I/O logic to support advanced I/O protocols.

2.3.3 I/O Logic Modes

The I/O Logic of the GW2A series of FPGA products supports several operation modes. In each operation mode, the I/O (or I/O differential pair) can be configured as output, input, INOUT or tristate output (output signal with tristate control).

2.4 Block SRAM

2.4.1 Introduction

The GW2A series of FPGA products provide abundant block SRAM resources. These memory resources are distributed as blocks throughout the FPGA array in the form of rows. Therefore, they are called block static random access memories (BSRAMs). Each BSRAM block occupies 3 CFU locations. The capacity of each BSRAM can be up to 18,432 bits (18Kbits). There are five operation modes: Single Port mode, Dual Port mode, Semi-Dual Port mode, ROM mode, and FIFO mode.

An abundance of BSRAM resources provide a guarantee for the user's high-performance design. The features of BSRAMs include:

- Up to 18,432 bits per BSRAM
- Clock frequency up to 380MHz (230MHz in Read-before-write mode)
- Supports Single Port mode
- Supports Dual Port mode
- Supports Semi-Dual Port mode
- Provides parity bits
- Supports ROM Mode
- Data widths from 1 to 36 bits
- Mixed clock mode
- Mixed data width mode
- Byte Enable function for 2-byte and above data widths
- Normal read and write
- Read-before-write
- Write-through

2.4.2 Memory Configuration Modes

BSRAMs in the GW2A series of FPGA products support various data widths, see Table 2-4.

Table 2-4 Memory Size Configuration

Single Port Mode	Dual Port Mode	Semi-Dual Port Mode	ROM Mode
16K x 1	16K x 1	16K x 1	16K x 1
8K x 2	8K x 2	8K x 2	8K x 2
4K x 4	4K x 4	4K x 4	4K x 4
2K x 8	2K x 8	2K x 8	2K x 8
1K x 16	1K x 16	1K x 16	1K x 16
512 x 32	-	512 x 32	512 x 32
2K x 9	2K x 9	2K x 9	2K x 9
1K x 18	1K x 18	1K x 18	1K x 18
512 x 36	-	512 x 36	512 x 36

Single Port Mode

The single port mode supports 2 read modes (bypass mode and pipeline mode) and 3 write modes (normal mode, write-through mode, and read-before-write mode). In single port mode, writing to or reading from one port at one clock edge is supported. During the write operation, the written data will be transferred to the output of the BSRAM. When the output register is bypassed, the new data will show up at the same write clock rising edge.

For more information on single port mode, please refer to UG285, Gowin BSRAM & SSRAM User Guide.

Dual Port Mode

The dual port mode supports 2 read modes (bypass mode and pipeline mode) and 2 write modes (normal mode and write-through mode). The applicable operations are as follows:

- Two independent read operations
- Two independent write operations
- An independent read operation and an independent write operation

Note!

It is not recommended to perform simultaneous read access from one port and write access from the other port to the same memory address.

For more information on dual port mode, please refer to UG285, Gowin BSRAM & SSRAM User Guide.

Semi-Dual Port Mode

The semi-dual port mode supports 2 read modes (bypass mode and pipeline mode) and 1 write mode (normal mode). Semi-dual port mode supports simultaneous read and write operations in the form of writing to port A and reading from port B.

Note!

It is not recommended to perform simultaneous read access from one port and write access from the other port to the same memory address.

For more information on semi-dual port mode, please refer to UG285, Gowin BSRAM & SSRAM User Guide.

ROM Mode

BSRAMs can be configured as ROMs. The ROM can be initialized during the device configuration stage, and the ROM data needs to be provided in the initialization file. Initialization is completed during the device power-on process.

Each BSRAM can be configured as one 16Kbits ROM. For more information on ROM mode, please refer to UG285, Gowin BSRAM & SSRAM User Guide.

2.4.3 Mixed Data Width Configuration

The BSRAMs in the GW2A series of FPGA products support mixed

data width operations. In dual port and semi-dual port mode, the data widths for read and write can be different, see Table 2-5 and Table 2-6.

Table 2-5 Dual Port Mixed Read/Write Data Width Configuration

Read Port	Write Port						
	16K x 1	8K x 2	4K x 4	2K x 8	1K x 16	2K x 9	1K x 18
16K x 1	*	*	*	*	*		
8K x 2	*	*	*	*	*		
4K x 4	*	*	*	*	*		
2K x 8	*	*	*	*	*		
1K x 16	*	*	*	*	*		
2K x 9						*	*
1K x 18						*	*

Note!

"*" denotes the modes supported.

Table 2-6 Semi-dual Port Mixed Read/Write Data Width Configuration

Read Port	Write Port								
	16K x 1	8K x 2	4K x 4	2K x 8	1K x 16	512x32	2K x 9	1K x 18	512x36
16K x 1	*	*	*	*	*	*			
8K x 2	*	*	*	*	*	*			
4K x 4	*	*	*	*	*	*			
2K x 8	*	*	*	*	*	*			
1K x 16	*	*	*	*	*	*			
512x32	*	*	*	*	*	*			
2K x 9							*	*	*
1K x 18							*	*	*

Note!

"*" denotes the modes supported.

2.4.4 Parity Bit

There are parity bits in BSRAMs. The 9th bit in each byte can be used as a parity bit to check the correctness of data transmission. It can also be used for data storage.

2.4.5 Synchronous Operation

- All the input registers of BSRAMs support synchronous write.
- The output registers can be used as pipeline registers to improve design performance.
- The output registers are bypass-able.

2.4.6 BSRAM Operation Modes

The BSRAM supports five different operations, including two read modes (Bypass Mode and Pipeline Mode) and three write modes (Normal Mode, Write-Through Mode, and Read-before-Write Mode).

Read Mode

The following two read modes are supported.

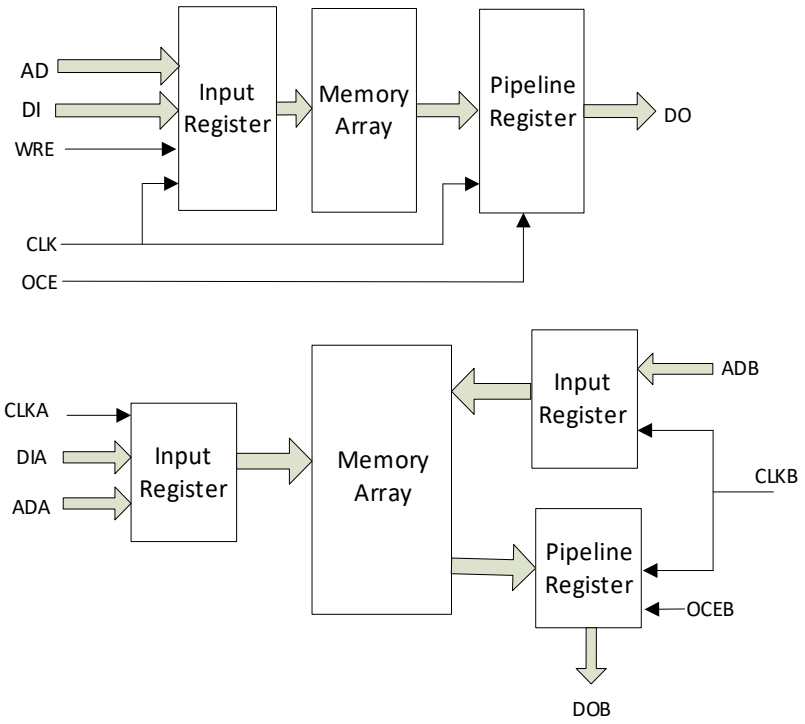
PIPELINE MODE

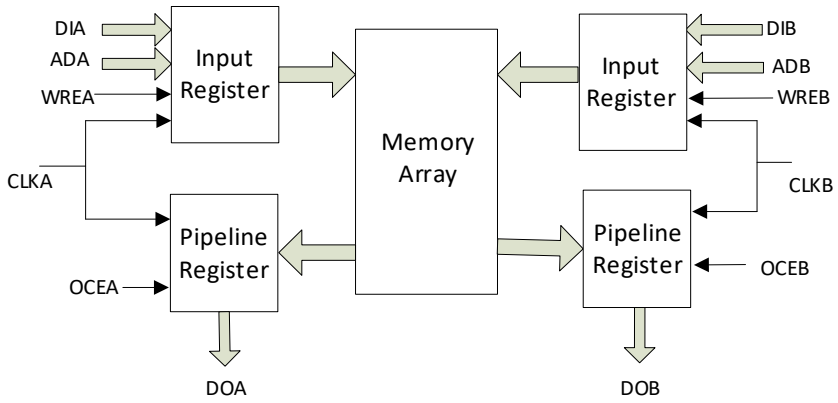
When a synchronous write cycles into a memory array with pipeline registers enabled, the data can be read from pipeline registers in the next clock cycle. The data bus can be up to 36 bits in this mode.

BYPASS MODE

When a synchronous write cycles into a memory array with pipeline registers bypassed, the outputs are registered at the memory array.

Figure 2-9 Pipeline Mode in Single Port Mode, Dual Port Mode, and Semi-dual Port Mode





Write Mode

NORMAL MODE

In this mode, when you write data to one port, the output data of this port does not change. The written data will not appear at the read port.

WRITE-THROUGH MODE

In this mode, when you write data to one port, the written data will appear at the output of this port.

READ-BEFORE-WRITE MODE

In this mode, when you write data to one port, the written data will be stored in the memory according to the address, and the original data in this address will appear at the output of this port.

2.4.7 Clock Mode

Table 2-7 lists the clock modes in different BSRAM modes:

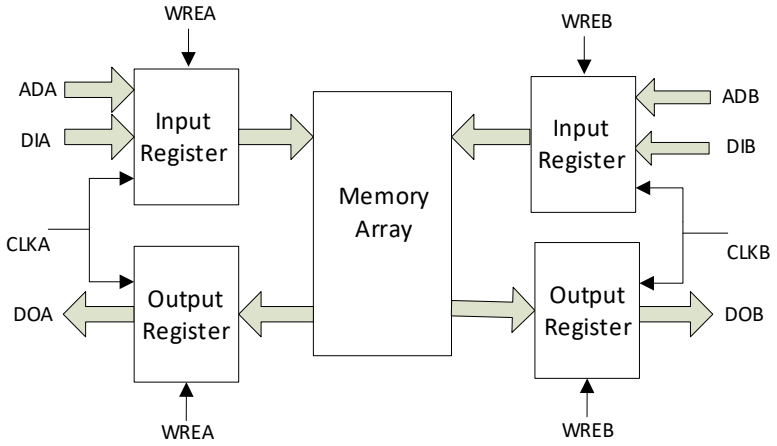
Table 2-7 Clock Modes in Different BSRAM Modes

Clock Mode	BSRAM Mode		
	Dual Port Mode	Semi-Dual Port Mode	Single Port Mode
Independent Clock Mode	Yes	No	No
Read/Write Clock Mode	Yes	Yes	No
Single Port Clock Mode	No	No	Yes

Independent Clock Mode

Figure 2-10 shows the independent clock operation in dual port mode with one clock at each port. CLKA controls all the registers at Port A; CLKB controls all the registers at Port B.

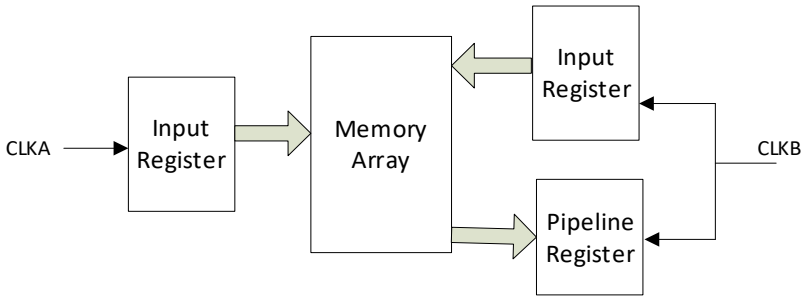
Figure 2-10 Independent Clock Mode



Read/Write Clock Mode

Figure 2-11 shows the read/write clock operation in semi-dual port mode with one clock at each port. The write clock (CLKA) controls data inputs, write addresses and read/write enable signals of Port A. The read clock (CLKB) controls data outputs, read addresses, and read enable signals of Port B.

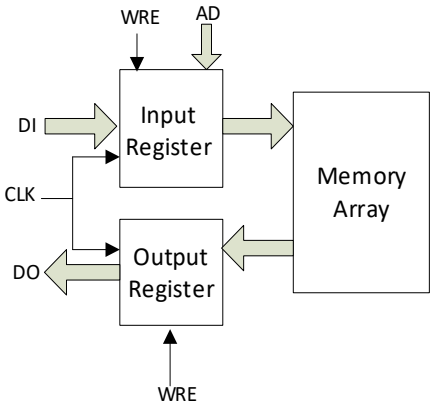
Figure 2-11 Read/Write Clock Mode



Single Port Clock Mode

Figure 2-12 shows the clock operation in single port mode.

Figure 2-12 Single Port Clock Mode



2.5 Digital Signal Processing

GW2A devices provide abundant DSP resources. Gowin's DSP solutions can address high-performance digital signal processing needs such as FIR and FFT designs. The DSP resources have the advantages of stable timing performance, high resource utilization, and low power consumption.

The DSP resources offer the following functions:

- Multipliers with three widths: 9-bit, 18-bit, 36-bit
- 54-bit ALU
- Multipliers cascading to support wider data widths
- Barrel shifters
- Adaptive filtering through signal feedback
- Computing with options to round to a positive number or a prime number
- Supports pipeline mode and bypass mode.

2.5.1 Macro

The DSP blocks are distributed throughout the FPGA array in the form of rows. Each DSP block occupies 9 CFU locations. Each DSP block contains two macros, and each macro contains two pre-adders, two 18 x 18 bit multipliers, and one three-input ALU.

Pre-adder

Each DSP macro contains two pre-adders for implementing pre-addition, pre-subtraction, and shifting.

The pre-adders are located at the first stage with two input ports:

- Parallel 18-bit input B or SBI
- Parallel 18-bit input A or SIA
  Each input port supports pipeline mode and bypass mode.
  Gowin's pre-adders can be used independently as function blocks, which support 9-bit and 18-bit width.

Multiplier

The multipliers are located after the pre-adders. The multipliers can be configured as 9 x 9, 18 x 18, 36 x 18, or 36 x 36. Register mode and bypass mode are supported in both input and output ports. The configuration modes that a macro supports include:

- One 18 x 36 multiplier
- Two 18 x 18 multipliers
- Four 9 x 9 multipliers

Two macros can form one 36 x 36 multiplier

Arithmetic Logic Unit

Each DSP macro contains one 54-bit ALU, which can further enhance multipliers' functions. Register mode and bypass mode are supported in

both input and output ports. The functions include:

- Addition/subtraction operations of multiplier output data/0, data A, and data B
- Addition/subtraction operations of multiplier output data/0, data B, and carry C
- Addition/subtraction operations of data A, data B, and carry C

2.5.2 DSP Operation Modes

Based on the two control signals(ALUSEL[6:0] and ALUMODE[3:0]), the DSP blocks can be configured as different operation modes.

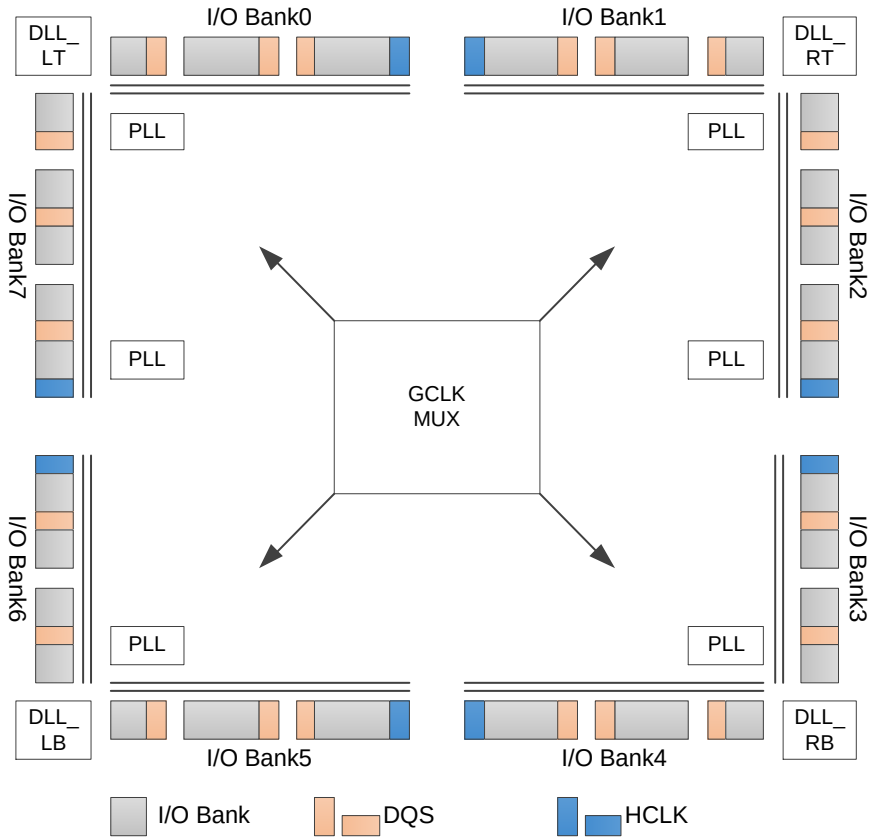
- Multiplier mode
- Multiply accumulator mode
- Multiply-add accumulator mode

For more information on the DSP resources, see UG287, Gowin Digital Signal Processing (DSP) User Guide.

2.6 Clocks

The clock resources and wiring are critical for high-performance applications in FPGA. The GW2A series of FPGA products provide global clocks (GCLKs) which connect to all the registers directly. In addition, high-speed clocks (HCLKs), PLLs, DQSs, etc. are provided.

Figure2-13 GW2A Clock Resources



2.6.1 Global Clocks

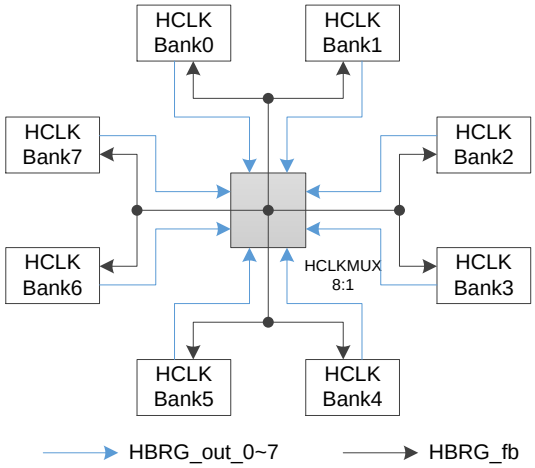
The Global Clock(GCLK) resources are distributed in the device as four quadrants. Each quadrant provides eight GCLKs. The clock sources of GCLKs include dedicated clock input pins and CRUs, and better clock performance can be achieved by using the dedicated clock input pins.

2.6.2 High-speed Clocks

The high-speed clocks (HCLKs) can support high-performance data transfer of I/Os and are mainly suitable for source synchronous data

transfer protocols, see Figure 2-14.

Figure 2-14 GW2A HCLK Distribution



As shown in Figure 2-14, there is an 8:1 HCLKMUX module in the middle of the HCLK. HCLKMUX can send the HCLK signal in any bank to any other bank, which makes the use of HCLK more flexible.

The function modules that are available for the HCLK resources include:

- DHCEN: A dynamic enable module for the high-speed clocks. Its function is similar to DQCE. It is used to turn on/off the high-speed clock signal dynamically.
- CLKDIV/ CLKDIV2: A frequency division module for the high-speed clocks. Each Bank has a CLKDIV. It is used to generate a frequency-divided clock with the same phase as the input clock, which is used in the IO logic mode.
- DCS: A dynamic selector for the high-speed clocks.
- DLLDLY: A dynamic delay adjustment module, used for the clock signals input via the dedicated clock pins.

2.6.3 PLLs

The PLL (Phase-locked Loop) is one kind of feedback control circuit. The frequency and phase of the internal oscillator signal are controlled by the external input reference clock.

PLLs in the GW2A series of FPGA products can provide synthesizable clock frequencies. Frequency adjustment (multiplication and division), phase adjustment, and duty cycle adjustment can be achieved by configuring the parameters.

2.6.4 DDR Memory Interface Clock Management(DQS)

The DQS module of the GW2A series of FPGA products provides the following features to support the clocking requirements of the DDR memory interface:

- Receives DQS inputs, sorts out waveforms and shifts 1/4 phase

- Provides read/write pointers for the input buffer
- Provides a data valid signal for internal logic
- Provides DDR output clock signals
- Supports DDR3 write voltage control

The DQS module supports multiple modes for different I/O interfaces.

For more information on the GCLKs, HCLKs, and DQSs, see UG286, Gowin Clock User Guide.

2.7 Long Wires

As a supplement to the CRU, the GW2A series of FPGA products provide another kind of routing resource - the long wire, which can be used for clock, clock enable, set/reset, or other high fan out signals.

2.8 Global Set/Reset

The GW2A series of FPGA products offer a dedicated global set/reset (GSR) network that connects directly to the device's internal logic and can be used as asynchronous/synchronous set or asynchronous/synchronous reset, with the registers in the CFUs and I/Os being able to be configured independently.

2.9 Programming & Configuration

The GW2A series of FPGA products support SRAM configuration, and the configuration data needs to be re-downloaded upon each power-up. Of course, you can also save the configuration data in an external Flash. After power-up, the GW2A device loads the configuration data from the external Flash to the SRAM.

Besides JTAG, the GW2A series of FPGA products also support GOWINSEMI's own GowinCONFIG configuration modes: SSPI, MSPI, CPU, SERIAL. For more, please refer to UG290, Gowin FPGA Products Programming and Configuration User Guide.

2.10 On-chip Oscillator

The GW2A series of FPGA products have an embedded programmable on-chip clock oscillator that provides a clock source for the MSPI configuration mode. See Table 2-8 for the output frequencies. The on-chip oscillator also provides a clock resource for user designs. Up to 64 clock frequencies can be obtained by setting the parameters. The following formula is used to get the output clock frequency:

f_{out}=250MHz/Param.

Note!

"Param" should be even numbers from 2 to 128.

Table 2-8 Output Frequency Options of the On-chip Oscillator

Mode	Frequency	Mode	Frequency	Mode	Frequency
0	2.5MHz[1]	8	7.8MHz	16	15.6MHz
1	5.4MHz	9	8.3MHz	17	17.9MHz
2	5.7MHz	10	8.9MHz	18	21MHz
3	6.0MHz	11	9.6MHz	19	25MHz
4	6.3MHz	12	10.4MHz	20	31.3MHz
5	6.6MHz	13	11.4MHz	21	41.7MHz
6	6.9MHz	14	12.5MHz	22	62.5MHz
7	7.4MHz	15	13.9MHz	23	125MHz[2]

Note!

- [1] The default frequency is 2.5MHz.
- [2] 125MHz is not available for the MSPI configuration mode.

3 DC and Switching Characteristics

Note!

Please ensure that you use Gowin's devices within the recommended operating conditions and ranges. Data beyond the working conditions and ranges are for reference only. Gowin does not guarantee that all devices will operate normally beyond the operating conditions and ranges.

3.1 Operating Conditions

3.1.1 Absolute Max. Ratings

Table 3-1 Absolute Max. Ratings

Name	Description	Min.	Max.
V_{CC}	Core voltage	-0.5V	1.1V
V_{CCPLL}	PLL Voltage	-0.5V	1.1V
V_{CCIO}	I/O Bank voltage	-0.5V	3.75V
-	I/O Voltage Applied[1]	-0.5V	3.75V
V_{CCX}	Auxiliary voltage	-0.5V	3.75V
Storage Temperature	Storage Temperature	-65℃	+150℃
Junction Temperature	Junction Temperature	-40℃	+125℃

Note!

[1] Overshoot and undershoot of -2V to (V_{IHMAX} + 2)V are allowed for a duration of <20 ns.

3.1.2 Recommended Operating Conditions

Table 3-2 Recommended Operating Conditions

Name	Description	Min.	Max.
V_{CC}	Core voltage	0.95V	1.05V
$V_{CCPLLLx}$	Left PLL Voltage	0.95V	1.05V
$V_{CCPLLRx}$	Right PLL Voltage	0.95V	1.05V
V_{CCIO}	I/O Bank voltage	1.14V	3.6V
V_{CCX}	Auxiliary voltage	2.7V	3.6V

Name	Description	Min.	Max.
T_{JCOM}	Junction temperature (commercial operation)	0℃	+85℃
T_{JIND}	Junction temperature (industrial operation)	-40℃	+100℃

Note!

- The allowable ripples on V_{CC}, V_{CCIO}, and V_{CCX} are 3%, 5%, and 5% respectively. For devices of which the PLL is powered directly with V_{CC}, the ripple on V_{CC} can affect the jitter characteristics of the PLL output clock; 2). The ripple on V_{CCIO} can eventually be passed on to the output waveform of the IO Buffer.
- For more information on the power supplies, please refer to UG110, GW2A-18 Pinout and UG113, GW2A-55 Pinout .

3.1.3 Power Supply Ramp Rates

Table 3-3 Power Supply Ramp Rates

Name	Description	Min.	Typ.	Max.
V_{CC} Ramp	Power supply ramp rates for V_{CC}	0.1mV/μs	-	10mV/μs
V_{CCIO}/V_{CCX} Ramp	Power supply ramp rates for V_{CCIO} and V_{CCX}	0.01mV/μs	-	100mV/μs

Note!

- A monotonic ramp is required for all power supplies.
- All power supplies need to be in the operating range as defined in Table 4-2 before configuration. Power supplies that are not in the operating range need to be adjusted to a faster ramp rate, or you have to delay configuration.

3.1.4 Hot Socketing Specifications

Table 3-4 Hot Socketing Specifications

Name	Description	Condition	I/O Type	Max.
I_{HS}	Input or I/O leakage current	$0<V_{IN}<V_{IH}$(MAX)	I/O	150uA
I_{HS}	Input or I/O leakage current	$0<V_{IN}<V_{IH}$(MAX)	TDI,TDO, TMS,TCK	120uA

3.1.5 POR Specifications

Table 3-5 POR Parameters

Name	Description	Device	Name	Value
V_{POR_UP}	Power on reset ramp up trip point	GW2A-18	V_{CC}	0.8V
			V_{CCX}	2.45V
			V_{CCIO}	0.9V
		GW2A-55	V_{CC}	0.8V
			V_{CCX}	2.45V
			V_{CCIO}	0.9V
V_{POR_DOWN}	Power on reset ramp down trip point	GW2A-18	V_{CC}	0.7V
			V_{CCX}	2.2V
			V_{CCIO}	0.6V
		GW2A-55	V_{CC}	0.7V
			V_{CCX}	2.2V
			V_{CCIO}	0.65V

3.2 ESD performance

Table 3-6 GW2A ESD - HBM

Device	GW2A-18	GW2A-55
QN88	HBM>1,000V	-
EQ144	HBM>1,000V	-
MG196	HBM>1,000V	-
PG256	HBM>1,000V	-
PG256S	HBM>1,000V	-
PG256SF	HBM>1,000V	-
PG256C	HBM>1,000V	-
PG256CF	HBM>1,000V	-
PG256E	HBM>1,000V	-
PG484	HBM>1,000V	HBM>1,000V
PG484C	HBM>1,000V	-
PG1156	-	HBM>1,000V
UG324	HBM>1,000V	HBM>1,000V
UG324D	-	HBM>1,000V
UG324F	-	HBM>1,000V
UG484	HBM>1,000V	-
UG484S	-	HBM>1,000V
UG676	-	HBM>1,000V

Table 3-7 GW2A ESD - CDM

Device	GW2A-18	GW2A-55
QN88	CDM>500V	-
EQ144	CDM>500V	-
MG196	CDM>500V	-
PG256	CDM>500V	-
PG256S	CDM>500V	-
PG256SF	CDM>500V	-
PG256C	CDM>500V	-
PG256CF	CDM>500V	-
PG256E	CDM>500V	-
PG484	CDM>500V	CDM>500V
PG484C	CDM>500V	-
PG1156	-	CDM>500V
UG324	CDM>500V	CDM>500V
UG324D	-	CDM>500V
UG324F	-	CDM>500V
UG484	CDM>500V	-
UG484S	-	CDM>500V
UG676	-	CDM>500V

3.3 DC Electrical Characteristics

3.3.1 DC Electrical Characteristics over Recommended Operating Conditions

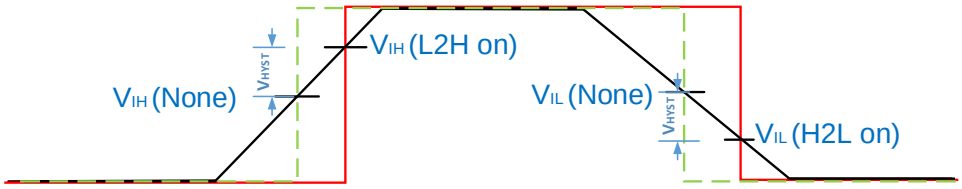
Table 3-8 DC Electrical Characteristics over Recommended Operating Conditions

Name	Description	Condition	Min.	Typ.	Max.
I_{IL},I_{IH}	Input or I/O leakage	$V_{CCIO}<V_{IN}<V_{IH}$(MAX)	-	-	210μA
		0V<V_{IN}<V_{CCIO}	-	-	10μA
I_{PU}	I/O Active Pull-up Current	0<V_{IN}<0.7V_{CCIO}	-30μA	-	-150μA
I_{PD}	I/O Active Pull-down Current	V_{IL}(MAX)<V_{IN}<V_{CCIO}	30μA	-	150μA
I_{BHLS}	Bus Hold Low Sustaining Current	V_{IN}=V_{IL}(MAX)	30μA	-	-

Name	Description	Condition	Min.	Typ.	Max.
I_{BHHS}	Bus Hold High Sustaining Current	V_{IN}=0.7V_{CCIO}	-30μA	-	-
I_{BHLO}	Bus Hold Low Overdrive Current	0≤V_{IN}≤V_{CCIO}	-	-	150μA
I_{BHHO}	Bus Hold High Overdrive Current	0≤V_{IN}≤V_{CCIO}	-	-	-150μA
V_{BHT}	Bus Hold Trip Points	-	V_{IL}(MAX)	-	V_{IH}(MIN)
C1	I/O Capacitance	-	-	5pF	8pF
V_{HYST}	Hysteresis for Schmitt Trigger inputs	V_{CCIO}=3.3V, Hysteresis=L2H[1],[2]	-	240mV	-
		V_{CCIO}=2.5V, Hysteresis=L2H	-	140mV	-
		V_{CCIO}=1.8V, Hysteresis=L2H	-	65mV	-
		V_{CCIO}=1.5V, Hysteresis=L2H	-	30mV	-
		V_{CCIO}=3.3V, Hysteresis=H2L[1],[2]	-	200mV	-
		V_{CCIO}=2.5V, Hysteresis=H2L	-	130mV	-
		V_{CCIO}=1.8V, Hysteresis=H2L	-	60mV	-
		V_{CCIO}=1.5V, Hysteresis=H2L	-	40mV	-
		V_{CCIO}=3.3V,Hysteresis=HIGH[1],[2]	-	440mV	-
		V_{CCIO}=2.5V,Hysteresis=HIGH	-	270mV	-
		V_{CCIO}=1.8V,Hysteresis=HIGH	-	125mV	-
		V_{CCIO}=1.5V,Hysteresis=HIGH	-	70mV	-

Note!

- [1] Hysteresis="NONE", "L2H", "H2L", "HIGH" indicates the Hysteresis options that can be set when setting I/O Constraints in the FloorPlanner tool of Gowin EDA, for more details, see SUG935, Gowin Design Physical Constraints User Guide.
- [2] Enabling the L2H (low to high) option means raising V_{IH} by V_{HYST}; enabling the H2L (high to low) option means lowering V_{IL} by V_{HYST}; enabling the HIGH option means enabling both L2H and H2L options, i.e. V_{HYST}(HIGH) = V_{HYST}(L2H) + V_{HYST}(H2L). The diagram is shown below.



3.3.2 Static Current

Table 3-9 Static Current

Name	Description	Device	Typ.
I_{CC}	V_{CC} current(V_{CC}=1V)	GW2A-55	150mA
		GW2A-18	70mA
I_{CCX}	V_{CCX} current(V_{CCX}=3.3V)	GW2A-55	35mA
		GW2A-18	15mA
I_{CCIO}	V_{CCIO} current (V_{CCIO}=3.3V)	GW2A-55	<2mA
		GW2A-18	<2mA

Note!

Test conditions: V_{CC} =1V, room temperature, speed grade C8/I7.

3.3.3 Recommended I/O Operating Conditions

Table 3-10 Recommended I/O Operating Conditions

Name	V_{CCIO} (V) for Output			V_{REF} (V) for Input		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVTTL33	3.135	3.3	3.6	-	-	-
LVCMOS33	3.135	3.3	3.6	-	-	-
LVCMOS25	2.375	2.5	2.625	-	-	-
LVCMOS18	1.71	1.8	1.89	-	-	-
LVCMOS15	1.425	1.5	1.575	-	-	-
LVCMOS12	1.14	1.2	1.26	-	-	-
SSTL15	1.425	1.5	1.575	0.68	0.75	0.9
SSTL18_I	1.71	1.8	1.89	0.833	0.9	0.969
SSTL18_II	1.71	1.8	1.89	0.833	0.9	0.969
SSTL25_I	2.375	2.5	2.645	1.15	1.25	1.35
SSTL25_II	2.375	2.5	2.645	1.15	1.25	1.35
SSTL33_I	3.135	3.3	3.6	1.3	1.5	1.7
SSTL33_II	3.135	3.3	3.6	1.3	1.5	1.7
HSTL18_I	1.71	1.8	1.89	0.816	0.9	1.08
HSTL18_II	1.71	1.8	1.89	0.816	0.9	1.08
HSTL15	1.425	1.5	1.575	0.68	0.75	0.9
PCI33	3.135	3.3	3.6	-	-	-
LVPECL33E	3.135	3.3	3.6	-	-	-
MLVDS25E	2.375	2.5	2.625	-	-	-
BLVDS25E	2.375	2.5	2.625	-	-	-
RSDS25E	2.375	2.5	2.625	-	-	-
LVDS25E[1]	2.375	2.5	2.625	-	-	-
SSTL15D	1.425	1.5	1.575	-	-	-

Name	V_{CCIO} (V) for Output			V_{REF} (V) for Input		
	Min.	Typ.	Max.	Min.	Typ.	Max.
SSTL18D_I	1.71	1.8	1.89	-	-	-
SSTL18D_II	1.71	1.8	1.89	-	-	-
SSTL25D_I	2.375	2.5	2.625	-	-	-
SSTL25D_II	2.375	2.5	2.625	-	-	-
SSTL33D_I	3.135	3.3	3.6	-	-	-
SSTL33D_II	3.135	3.3	3.6	-	-	-
HSTL15D	1.425	1.575	1.89	-	-	-
HSTL18D_I	1.71	1.8	1.89	-	-	-
HSTL18D_II	1.71	1.8	1.89	-	-	-

Note!

[1] V_{CCIO} of banks using True LVDS is recommended to be set to 2.5V.

3.3.4 Single-ended I/O DC Characteristics

Table 3-11 Single-ended I/O DC Characteristics

Name	V_{IL}		V_{IH}		V_{OL} (Max)	V_{OH} (Min)	I_{OL}[1] (mA)	I_{OH}[1] (mA)
	Min	Max	Min	Max				
LVCMOS33 LVTTL33	-0.3V	0.8V	2.0V	3.6V	0.4V	V_{CCIO}-0.4V	4	-4
							8	-8
							12	-12
							16	-16
							24	-24
					0.2V	V_{CCIO}-0.2V	0.1	-0.1
LVCMOS25	-0.3V	0.7V	1.7V	3.6V	0.4V	V_{CCIO}-0.4V	4	-4
							8	-8
							12	-12
							16	-16
					0.2V	V_{CCIO}-0.2V	0.1	-0.1
LVCMOS18	-0.3V	0.35 x V_{CCIO}	0.65 x V_{CCIO}	3.6V	0.4V	V_{CCIO}-0.4V	4	-4
							8	-8
							12	-12
					0.2V	V_{CCIO}-0.2V	0.1	-0.1
LVCMOS15	-0.3V	0.35 x V_{CCIO}	0.65 x V_{CCIO}	3.6V	0.4V	V_{CCIO}-0.4V	4	-4
							8	-8
					0.2V	V_{CCIO}-0.2V	0.1	-0.1
LVCMOS12	-0.3V	0.35 x V_{CCIO}	0.65 x V_{CCIO}	3.6V	0.4V	V_{CCIO}-0.4V	2	-2
							4	-4
					0.2V	V_{CCIO}-0.2V	0.1	-0.1

Name	V_{IL}		V_{IH}		V_{OL} (Max)	V_{OH} (Min)	I_{OL}[1] (mA)	I_{OH}[1] (mA)
	Min	Max	Min	Max				
PCI33	-0.3V	0.3 x V_{CCIO}	0.5 x V_{CCIO}	3.6V	0.1 x V_{CCIO}	0.9 x V_{CCIO}	1.5	-0.5
SSTL33_I	-0.3V	V_{REF}-0.2V	V_{REF}+0.2V	3.6V	0.7	V_{CCIO}-1.1V	8	-8
SSTL25_I	-0.3V	V_{REF}-0.18V	V_{REF}+0.18V	3.6V	0.54V	V_{CCIO}-0.62V	8	-8
SSTL25_II	-0.3V	V_{REF}-0.18V	V_{REF}+0.18V	3.6V	NA	NA	NA	NA
SSTL18_II	-0.3V	V_{REF}-0.125V	V_{REF}+0.125 V	3.6V	NA	NA	NA	NA
SSTL18_I	-0.3V	V_{REF}-0.125V	V_{REF}+0.125 V	3.6V	0.40V	V_{CCIO}-0.40V	8	-8
SSTL15	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	0.40V	V_{CCIO}-0.40V	8	-8
HSTL18_I	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	0.40V	V_{CCIO}-0.40V	8	-8
HSTL18_II	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	NA	NA	NA	NA
HSTL15_I	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	0.40V	V_{CCIO}-0.40V	8	-8
HSTL15_II	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	NA	NA	NA	NA

Note!

[1] The total DC current limit(sourced and sunk current) of all IOs in the same bank: the total DC current of all IOs in the same bank shall not be greater than n*8mA, where n represents the number of IOs bonded out from a bank.

3.3.5 Differential I/O DC Characteristics

Table 3-12 Differential I/O DC Characteristics

LVDS

Name	Description	Test conditions	Min.	Typ.	Max.	Unit
V_{INA},V_{INB}	Input Voltage	-	0	-	2.4	V
V_{CM}	Input Common Mode Voltage	-	0.05	-	2.35	V
V_{THD}	Differential Input Threshold	Minimum Input Swing	±100	-	±600	mV
I_{IN}	Input Current	Power On or Power Off	-	-	±10	μA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	R_T = 100Ω	-	-	1.6	V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	R_T = 100Ω	0.9	-	-	V
V_{OD}	Output Voltage Differential	(V_{OP} - V_{OM}), R_T=100Ω	250	350	450	mV
ΔV_{OD}	Change in V_{OD} Between High and Low	-	-	-	50	mV
V_{OS}	Output Voltage Offset	(V_{OP} + V_{OM})/2, R_T=100Ω	1.125	1.2	1.375	V

Name	Description	Test conditions	Min.	Typ.	Max.	Unit
ΔV_{OS}	Change in V_{OS} Between High and Low	-	-	-	50	mV
I_S	Short-circuit current	V_{OD} = 0V output short-circuit	-	-	15	mA

3.4 Switching Characteristics

3.4.1 CFU Switching Characteristics

Table 3-13 CFU Timing Parameters

Device	Name	Description	C8/I7		C7/I6		Unit
			Min	Max	Min	Max	
GW2A-18	t_{LUT4_CFU}	LUT4 delay	0.31	0.46	0.39	0.58	ns
	t_{SR_CFU}	Set/Reset to Register output	1.10	1.15	1.37	1.44	ns
	t_{CO_CFU}	Clock to Register output	0.20	0.23	0.25	0.29	ns
GW2A-55	t_{LUT4_CFU}	LUT4 delay	0.31	0.46	0.39	0.58	ns
	t_{SR_CFU}	Set/Reset to Register output	1.10	1.15	1.37	1.44	ns
	t_{CO_CFU}	Clock to Register output	0.20	0.23	0.25	0.29	ns

3.4.2 BSRAM Switching Characteristics

Table 3-14 BSRAM Timing Parameters

Device	Name	Description	C8/I7		C7/I6		Unit
			Min	Max	Min	Max	
GW2A-18	t_{COAD_BSRAM}	Clock to output from read address/data	2.26	2.26	2.83	2.83	ns
	t_{COOR_BSRAM}	Clock to output from output register	0.31	0.31	0.38	0.38	ns
GW2A-55	t_{COAD_BSRAM}	Clock to output from read address/data	2.26	2.26	2.83	2.83	ns
	t_{COOR_BSRAM}	Clock to output from output register	0.31	0.31	0.38	0.38	ns

3.4.3 DSP Switching Characteristics

Table 3-15 DSP Timing Parameters

Device	Name	Description	C8/I7		C7/I6		Unit
			Min	Max	Min	Max	
GW2A-18	t_{COIR_DSP}	Clock to output from input register	0.24	0.25	0.30	0.32	ns
	t_{COPR_DSP}	Clock to output from pipeline register	0.07	0.08	0.09	0.10	ns
	t_{COOR_DSP}	Clock to output from output register	0.04	0.04	0.05	0.05	ns
GW2A-55	t_{COIR_DSP}	Clock to output from input register	0.24	0.25	0.30	0.32	ns

Device	Name	Description	C8/I7		C7/I6		Unit
			Min	Max	Min	Max	
	t_{COPR_DSP}	Clock to output from pipeline register	0.07	0.08	0.09	0.10	ns
	t_{COOR_DSP}	Clock to output from output register	0.04	0.04	0.05	0.05	ns

3.4.4 Gearbox Switching Characteristics

Table 3-16 Gearbox Timing Parameters

Device	Name	Description	Max.	Unit
GW2A-18/55	$FMAX_{IDDR}$	1:2 Gearbox maximum input serial rate	400	Mbps
	$FMAX_{IDES4}$	1:4 Gearbox maximum input serial rate	800	Mbps
	$FMAX_{IDES7}$	1:7 Gearbox maximum input serial rate	1000	Mbps
	$FMAX_{IDESx}$	1:8/1:10 Gearbox maximum input serial rate	1200	Mbps
	$FMAX_{ODDR}$	2:1 Gearbox maximum output serial rate	400	Mbps
	$FMAX_{OSER4}$	4:1 Gearbox maximum output serial rate	800	Mbps
	$FMAX_{OSER7}$	7:1 Gearbox maximum output serial rate	1000	Mbps
	$FMAX_{OSERx}$	8:1/10:1 Gearbox maximum output serial rate	1200	Mbps

3.4.5 Clock and I/O Switching Characteristics

Table 3-17 External Switching Characteristics

Device	Name	Description	C8/I7		C7/I6		Unit
			Min	Max	Min	Max	
GW2A-18	Pin-LUT-Pin Delay[1]	Pin(IOxA) to Pin(IOxB) delay	-	3.83	-	4.59	ns
	$T_{HCLKdly}$	HCLK tree delay	-	0.82	-	0.98	ns
	$T_{GCLKdly}$	GCLK tree delay	-	1.77	-	2.12	ns
GW2A-55	Pin-LUT-Pin Delay[1]	Pin(IOxA) to Pin(IOxB) delay	-	3.83	-	4.59	ns
	$T_{HCLKdly}$	HCLK tree delay	-	1.32	-	1.48	ns
	$T_{GCLKdly}$	GCLK tree delay	-	2.27	-	2.62	ns

Note!

[1] Test conditions：V_{CCIO}=3.3V, V_{CCX}=3.3V, LVCMOS33, 8mA, 15pF load.

Table 3-18 I/O Register Parameters Using Dedicated GCLK Input through GCLK Tree without PLL

Device	Name	Description	C8/I7		C7/I6		Unit
			Min	Max	Min	Max	
GW2A-18	T_{SU}	clock to data setup(using GPIO input register)	-1		-1.1	-	ns
	T_H	clock to data hold(using GPIO input register)	2		2.4	-	ns
	T_{SU_DEL}	clock to data setup(using GPIO input register, with IODELAY enabled and Tap = 0)	-0.6		-0.7	-	ns
	T_{H_DEL}	clock to data hold(using GPIO input register, with IODELAY enabled and Tap = 0)	1.6		2	-	ns
GW2A-55	T_{SU}	clock to data setup(using GPIO input register)	-1.5	-	-1.6	-	ns
	T_H	clock to data hold(using GPIO input register)	2.5	-	2.9	-	ns
	T_{SU_DEL}	clock to data setup(using GPIO input register, with IODELAY enabled and Tap = 0)	-1.1	-	-1.2	-	ns
	T_{H_DEL}	clock to data hold(using GPIO input register,with IODELAY enabled and Tap = 0)	2.1	-	2.5	-	ns

Note!

Test conditions: LVCMOS33, 8mA, 15pF load.

3.4.6 On-chip Oscillator Switching Characteristics

Table 3-19 On-chip Oscillator Switching Characteristics

Name	Description	Min.	Typ.	Max.
f_{MAX}	Output Frequency (0 to+ 85℃)	106.25MHz	125MHz	143.75MHz
	Output Frequency (-40 to +100℃)	100MHz	125MHz	150MHz
t_{DT}	Output Clock Duty Cycle	43%	50%	57%

Name	Description	Min.	Typ.	Max.
t_{OPJIT}	Output Clock Period Jitter	0.01UIPP	0.012UIPP	0.02UIPP

3.4.7 PLL Switching Characteristics

Table 3-20 PLL Switching Characteristics

Device	Speed Grade	Name	Min.	Max.
GW2A-18	C8/I7, C7/I6	CLKIN	3MHZ	500MHZ
		PFD	3MHZ	500MHZ
		VCO	500MHZ	1250MHZ
		CLKOUT	3.90625MHZ	625MHZ
	C6/I5	CLKIN	3MHZ	400MHZ
		PFD	3MHZ	400MHZ
		VCO	400MHZ	1000MHZ
		CLKOUT	3.125MHZ	500MHZ
GW2A-55	C8/I7, C7/I6	CLKIN	3MHZ	500MHZ
		PFD	3MHZ	500MHZ
		VCO	500MHZ	1250MHZ
		CLKOUT	3.90625MHZ	625MHZ
	C6/I5	CLKIN	3MHZ	400MHZ
		PFD	3MHZ	400MHZ
		VCO	400MHZ	1000MHZ
		CLKOUT	3.125MHZ	500MHZ

3.5 Configuration Interface Timing Specification

The GW2A series of FPGA products support multiple GowinCONFIG modes: MSPI, SSPI, SERIAL, CPU. For more information, please refer to UG290, Gowin FPGA Products Programming and Configuration User Guide.

4 Ordering Information

4.1 Part Naming

Figure 4-1 Part Naming – ES

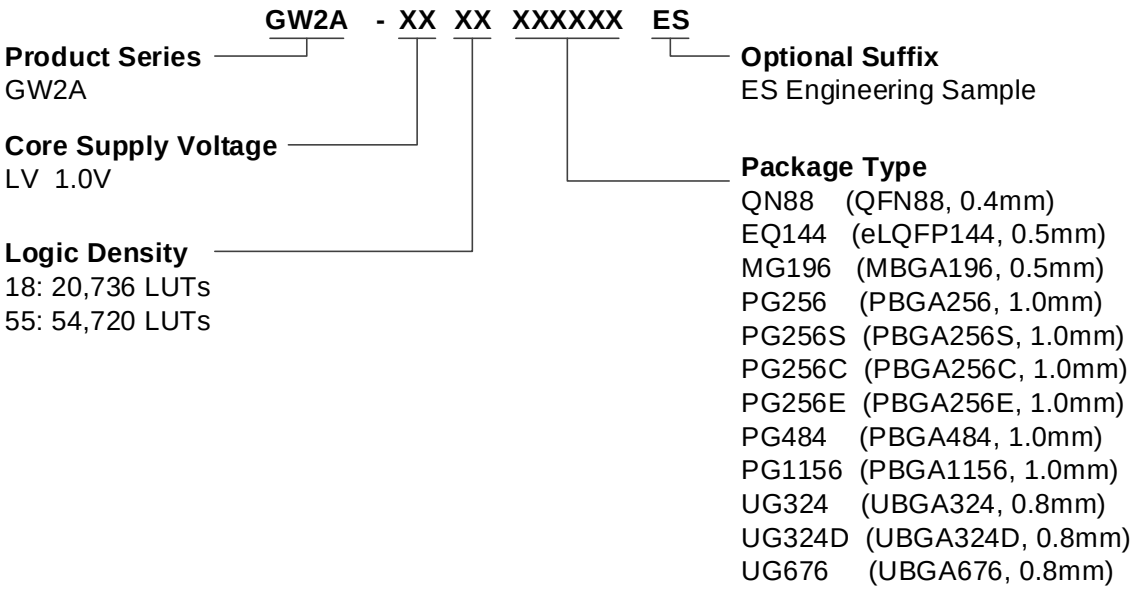
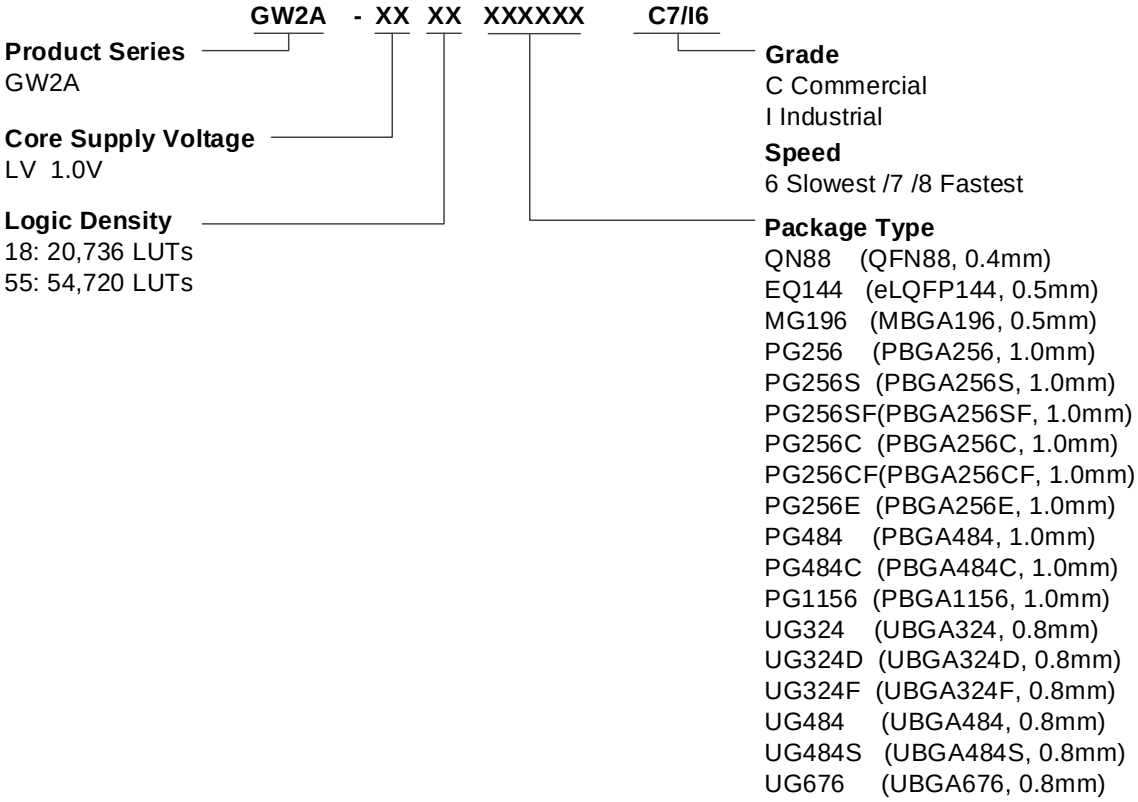


Figure 4-2 Part Naming – Production



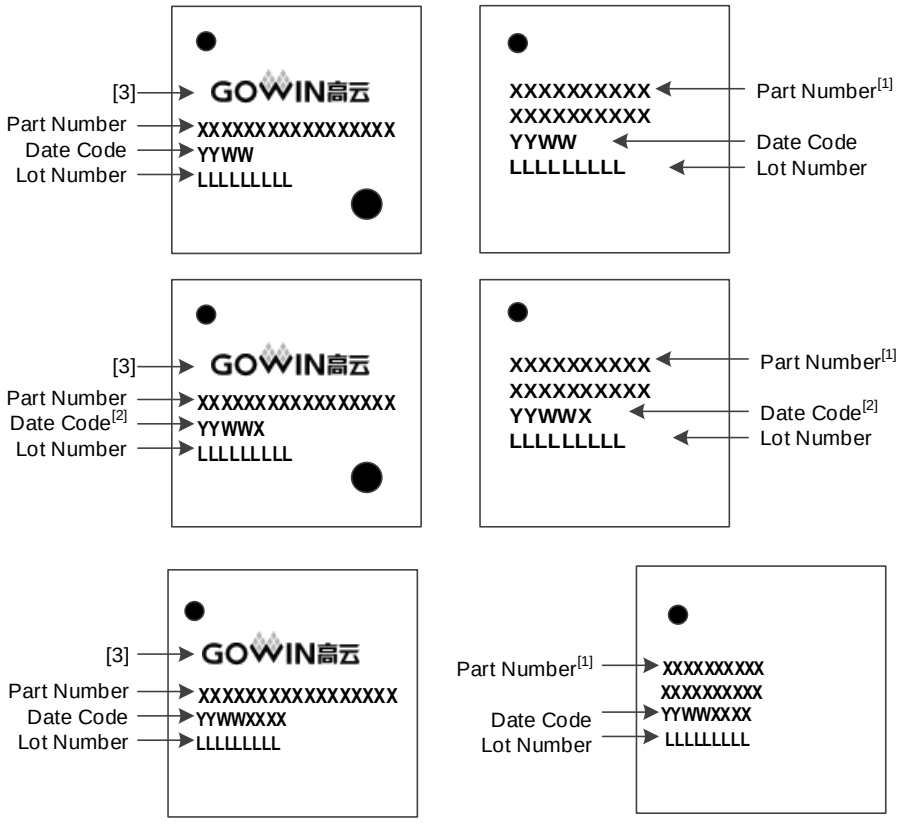
Note!

- For more information about the packages, please refer to 1.2 Product Resources.
- The LittleBee® family devices and Arora family devices of the same speed grade have different speeds.
- Both “C” and “I” are used in Gowin’s part name marking for one device. GOWIN devices are screened using industrial standards, so the same device can be used for both industrial (I) and commercial (C) applications. The maximum temperature of the industrial grade is 100℃, and the maximum temperature of the commercial grade is 85℃. Therefore, if the chip meets speed grade 7 in commercial grade applications, its speed grade will be 6 in industrial grade applications.

4.2 Package Markings

Gowin’s devices have markings on the their surfaces, as shown in Figure 4-3.

Figure 4-3 Package Marking Examples



Note!

- [1] The first two lines in the right figure(s) above are both the “Part Number”.
- [2] The Date Code followed by an “X” is for X version devices.
- [3] Whether the package marking bears the Gowin Logo or not depends on the package type, package size, and Part Number length. The above figure are only examples of the package markings.

5 About This Guide

5.1 Purpose

This data sheet provides a comprehensive overview of the GW2A series of FPGA products, including their features, resources, architecture, AC/DC characteristics, and ordering details. It aims to enhance accessibility and facilitate the effective utilization of Gowin's devices.

5.2 Related Documents

The latest documents are available at www.gowinsemi.com.

- UG290, Gowin FPGA Products Programming and Configuration User Guide
- UG111, GW2A series of FPGA Products Package and Pinout Manual
- UG110, GW2A-18 Pinout
- UG113, GW2A-55 Pinout

5.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are shown in Table 5-1.

Table 5-1 Terminology and Abbreviations

Terminology and Abbreviations	Full Name
ALU	Arithmetic Logic Unit
BSRAM	Block Static Random Access Memory
CFU	Configurable Function Unit
CLS	Configurable Logic Section
CRU	Configurable Routing Unit
DCS	Dynamic Clock Selector
DP	True Dual Port 16K BSRAM
DQCE	Dynamic Quadrant Clock Enable
DSP	Digital Signal Processing
EQ144	ELQFP144
FPGA	Field Programmable Gate Array
GPIO	Gowin Programmable IO
IOB	Input/Output Block
LUT4	4-input Look-up Table
LUT5	5-input Look-up Table
LUT6	6-input Look-up Table
LUT7	7-input Look-up Table
LUT8	8-input Look-up Table
MG	MBGA
PG	PBGA
PLL	Phase-locked Loop
QN	QFN
REG	Register
SDP	Semi Dual Port 16K BSRAM
SP	Single Port 16K BSRAM
SSRAM	Shadow Static Random Access Memory
TDM	Time Division Multiplexing
UG	UBGA

5.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail：support@gowinsemi.com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