Arora V 60K FPGA Products

Data Sheet

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Revision History

Date	Version	Description
05/10/2024	1.0E	Preliminary version.
06/14/2024	1.0E	Initial version released.
06/28/2024	1.1E	● GW5A-60 device information added. ● New packages added: UG324A, UG324S. ● Power supply names unified.
07/19/2024	1.1.1E	● BSRAM description optimized.
08/09/2024	1.1.2E	GW5A-60 PG324C added.

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1 General Description

GOWINSEMI Arora V 60K FPGA products are the 5th-generation of Arora family, with abundant internal resources, a new-architecture and high-performance DSP supporting AI operations, high-speed LVDS interfaces, and abundant BSRAM resources. At the same time, it integrates self-developed DDR3, 12.5Gbps SERDES supporting multiple protocols, and provides a variety of packages. It is suitable for applications such as low power, high performance and compatibility designs.

GOWINSEMI provides a new generation of FPGA hardware development environment that supports FPGA placement & routing, bitstream generation and download, etc.

1.1 Features

- Lower power consumption
  - 22nm SRAM process
  - Core Power (LV version): 0.9V / 1.0V
  - Core voltage (EV version): 1.2V
  - Supports dynamic on/off of clock
- Abundant logic cells
  - Provides up to 59.9K LUT4s
  - Supports shadow SRAMs
- Block SRAMs with multiple modes
  - Supports Dual Port, Single Port, Semi-Dual Port, and ROM
  - Supports bytes write enable
  - Supports ECC detection and error correction
- GW5AT-60 supports multiple transmission protocols such as 270 Mbps to 12.5G bps custom SERDES protocols and 10G Ethernet, etc.
- GW5AT-60 supports PCIe 3.0 hard core
  - Supportsx1, x2, x4 lanes
  - Supports End Point
- Supports MIPI D-PHY RX/TX hardcore
  - Supports MIPI DSI and MIPI CSI-2 RX/TX
  - Up to 2.5 Gbps per MIPI lane(RX/TX)
  - Supports up to four data lanes and one clock lanes, with the max. transmission bandwidth up to 10Gbps
- Supports MIPI C-PHY RX/TX hardcore

  Supports up to 3 three-wire data channels and supports up to 2.5Gsps (=5.75Gbps, RX/TX) data rate per channel.
- GPIO supports MIPI D-PHY RX/TX (MIPI IO)
  - GPIO can be configured as MIPI DSI and MIPI CSI-2 RX/TX interfaces
  - Up to 2.0 Gbps per MIPI lane for MIPI D-PHY RX/TX
- GPIOs Support MIPI C-PHY RX/TX (MIPI IO)
- High performance DSP blocks with a new architecture
  - High performance digital signal processing
  - Supports 27 x 18, 12 x 12, 27 x 36 multiplier and 48-bit accumulator
  - Supports cascading of multipliers
  - Supports pipeline mode and bypass mode
  - Pre-addtion operation for filter function
  - Supports barrel shifter
- Two types of ADCs are integrated: SARADC and ADC Sensor
- Supports various SDRAM interfaces, up to DDR3 1333 Mb/s
- Multiple I/O standards
  - Hysteresis option for input signals
  - Supports drive strengths of 2mA, 4mA, 6mA, 8mA, 12mA, 16mA, etc.

  - Individual Bus Keeper, Pull-up, Pull-down, and Open Drain options
  - Hot Socket
- 16 global clocks, 8 high-performance PLLs, 20 high speed clocks
- MIPI D-PHY, MIPI C-PHY, PLL and ADC modules support Mini Dynamic Re-Program Port (mDRP)
- Configuration & Programming
  - JTAG configuration
  - Multiple GowinConfig configurations: SSPI, MSPI, Master CPU, Slave CPU, Master SERIAL, Slave SERIAL, and PCIe
  - Supports programming the SPI Flash directly in JTAG and SSPI modes; For other modes, you can program the SPI Flash using IP
  - Supports background upgrade
  - Supports bitstream file encryption and security bit settings
  - Supports Configuration Memory Soft Error Recovery (CMSER)
  - Supports OTP, a unique 64-bit DNA identifier for each device

1.2 Product Resources

Table 1-1 Product Resources

Device	GW5AT-60	GW5A-60
LUT4	59904	59904
Flip-Flop (REG)	59904	59904
Distributed Static Random Access Memory SSRAM(Kb)	468	468
Block Static Random Access Memory BSRAM(Kb)	2124[4]	2124[4]
Number of BSRAMs BSRAM	118[4]	118[4]
DSP（27-bit x 18-bit）	118	118
Maximum phase locked loop[1](PLLs)	8	8
Global Clocks	16	16
High-speed Clocks	20	20
Transceivers[2]	4	-
Transceivers Rate	270Mbps - 12.5Gbps	-
PCIe 3.0	1, x1, x2, x4 PCIe 3.0	-
LVDS Gbps	1.25	1.25
DDR3 Mbps	1333	1333
MIPI D-PHY hardcore	2.5Gbps (RX/TX), 4 data lanes 1 clock lanes	2.5Gbps (RX/TX), 4 data lanes 1 clock lanes
MIPI C-PHY Hardcore	2.5Gsps (=5.75Gbps,RX/TX), 3-trios data lanes	2.5Gsps (=5.75Gbps,RX/TX), 3-trios data lanes
ADC	2	2
Number of GPIO banks	11	11
Maximum number of GPIOs[5]	320	320
Core voltage	0.9V/1.0V/1.2V [3]	0.9V/1.0V/1.2V [3]

Note!

- [1] Different packages support different numbers of PLLs, and here is the max. number.
- [2] Different packages support different numbers of Transceivers, and here is the max. number.
- [3] The EV version has a built-in LDO and supports 1.2V V_{CC}.
- [4] The GW5AT-60 ES version supports 72 BSRAM with a capacity of 1296Kb.
- [5] This is the max. number of GPIOs that the device can provide without package limitation. Please refer to Table 1-2 and Table 1-3 for the maximum number of user I/O available in specific packages.

Table 1-2 GW5AT-60 Package Information

Package			Pitch (mm)	Size (mm)	GW5AT-60			
Name	Type	Description			User I/O (True LVDS Pair)	Transceivers[1]	MIPI D- PHY Hardcore	MIPI C-PHY Hardcore
PG484A	PBGA	Wire Bond	1.0	23x23	297(143)	4	–	–
UG225	UBGA	Wire Bond	0.8	13x13	113(53)	4	RX/TX 4 data lanes 1 clock lanes	RX/TX 3-trios data lanes
UG324S	UBGA	Wire Bond	0.8	15x15	198(98)	4	–	–

Note!

[1] Transceivers can reach speeds up to 10.3125 Gbps, and when the rate exceeds 8 Gbps, only on-board interconnects are supported, not backplane applications.

Table 1-3 GW5A-60 Package Information

Package			Pitch (mm)	Size (mm)	GW5A-60		
Name	Type	Description			User I/O (True LVDS Pair)	MIPI D- PHY Hardcore	MIPI C-PHY Hardcore
UG324A	UBGA	Wire Bond	0.8	15x15	222(106)	–	–
UG324S	UBGA	Wire Bond	0.8	15x15	226(110)	–	–
PG324C	PBGA	Wire Bond	1.0	19x19	205 (97)	–	–

2 Architecture

2.1 Architecture

Figure 2-1 Architecture Diagram (GW5A-60)

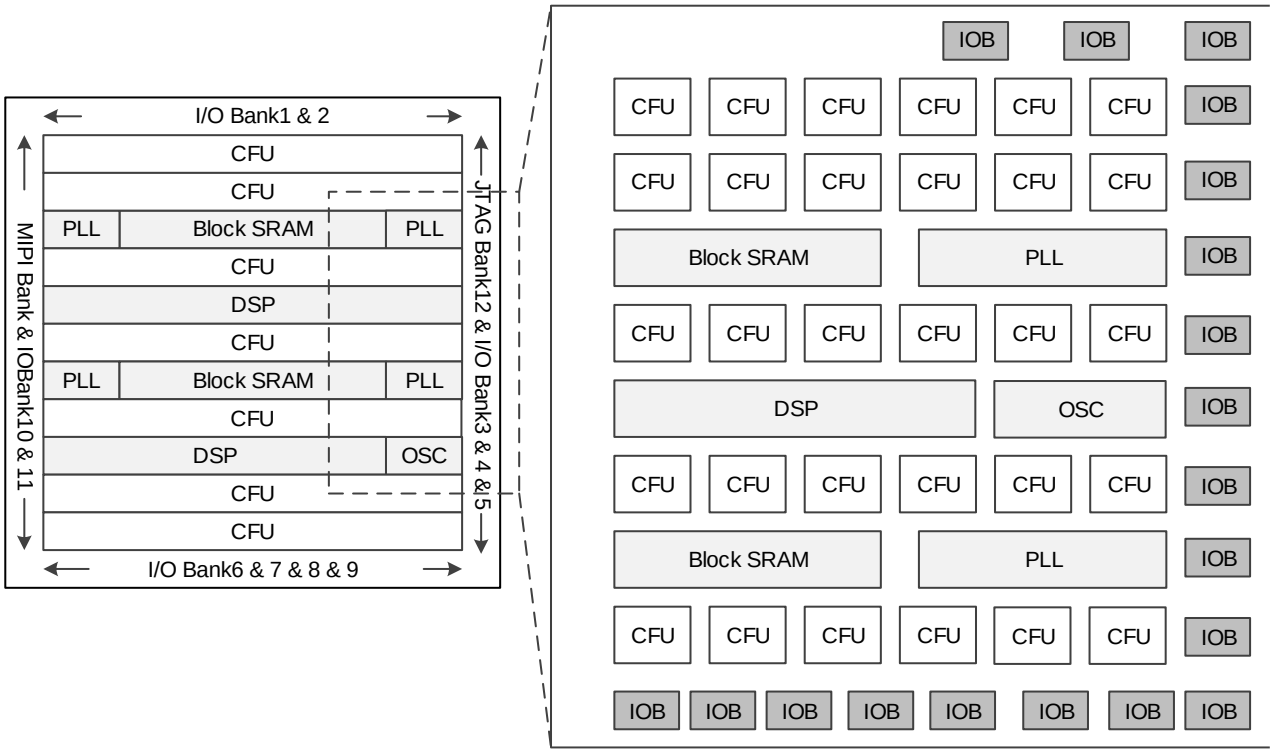


Figure 2-2 Architecture Diagram (GW5AT-60)

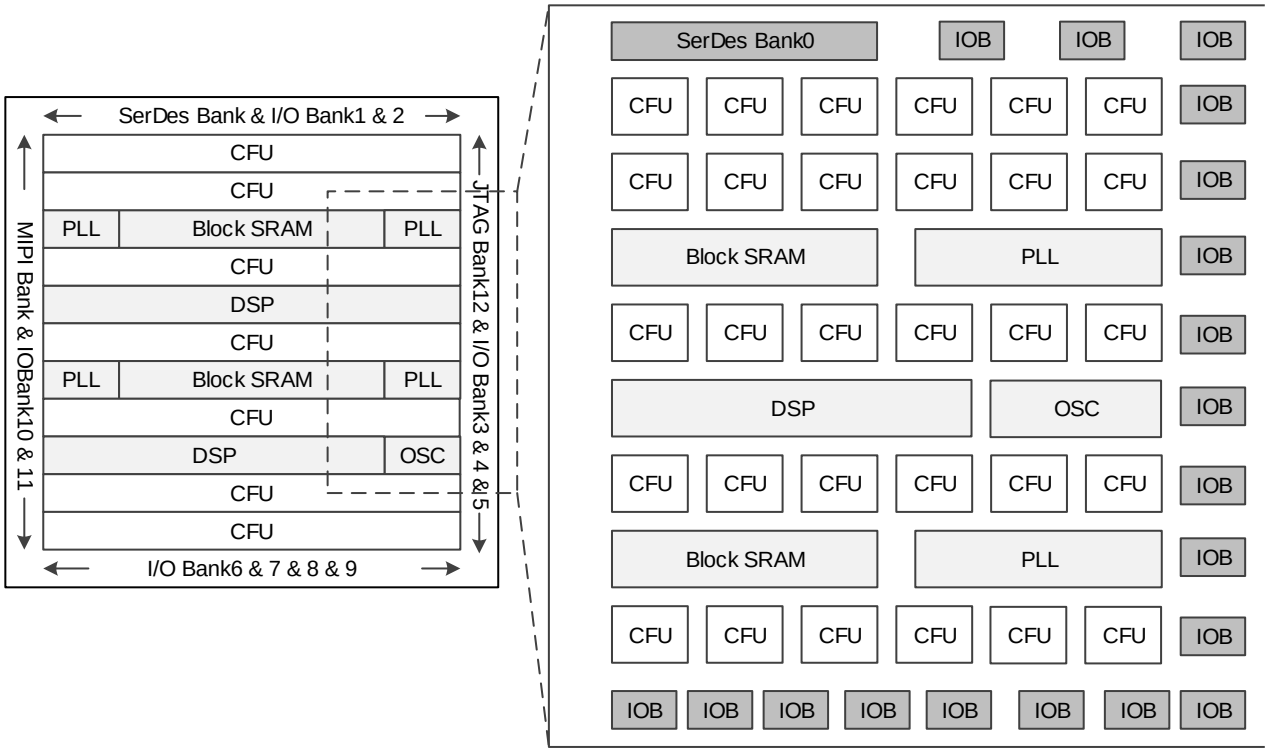


Figure 2-1 is the architecture overview of the GW5A-60 device.

Figure 2-2 is the architecture overview of the GW5AT-60 device.

For the internal resource information, please refer to Table 1-1. The core of the device is an array of Configurable Function Units (CFU) surrounded by IO blocks. Besides, BSRAMs, DSP blocks, Gigabit Transceiver(GW5AT-60), MIPI D-PHY, ADC, PLLs, and on chip oscillators are provided.

Configurable Function Unit (CFU) is the base cell for the array of the Arora V 60K FPGA Products. Devices with different capacities have different numbers of rows and columns. CFU can be configured as LUT4 mode, ALU mode, and memory mode. For more detailed information, see 2.2 Configurable Function Units.

The I/O resources in the Arora V 60K FPGA products are arranged around the periphery of the devices in groups referred to as banks. I/O resources support multiple I/O standards, and support regular mode, SRD mode, generic DDR mode, and DDR_MEM mode. For more detailed information, see 2.3 Input/Output Blocks.

The BSRAM is embedded as a row in Arora V 60K FPGA products. Each BSRAM has 36 Kbits. It consists of two 18 Kbits BSRAMs and supports multiple configuration modes and operation modes. For more detailed information, see 2.4 Block SRAM (BSRAM).

Arora V 60K of FPGA products are embedded with a brand-new DSP, which can meet your high-performance digital signal processing requirements. For details, refer to 2.5 DSP.

Arora V 60K FPGA products include Gigabit Transceiver Quads, each of which supports up to 4 transceivers. For details, refer to 2.6 Gigabit Transceiver and 2.7 PCI Express (PCIe) Controller.

Arora V 60K FPGA products provide a MIPI D-PHY hardcore supporting the “MIPI Alliance Standard for D-PHY Specification(V1.2)”. For details, see 2.8 MIPI D-PHY.

Arora V 60K FPGA products integrate two types of ADCs. For details, see 2.10 ADC.

Arora V 60K FPGA products have embedded PLL resources. PLL blocks provide the ability to synthesize clock frequencies. Frequency adjustment (multiply and division), phase adjustment, and duty cycle can be adjusted using the configuration of parameters. The FPGAs also have an embedded programmable on-chip clock oscillator that supports clock frequencies ranging from 1.67 MHz to 105MHz, providing clocking resources for the MSPI mode. The on-chip clock oscillator also provides programmable user clocks. For more information, see 2.14 On Chip Oscillator.

FPGA provides abundant CRUs, connecting all the resources in FPGA. For example, routing resources distributed in CFU and IOB connect resources in CFU and IOB. Routing resources can automatically be generated by Gowin software. In addition, the Arora V 60K FPGA Products also provide abundant GCLKs, long wires (LW), global set/reset (GSR), and programming options, etc. For more details, see 2.12 Global Set/Reset (GSR) and 2.13 Programming & Configuration.

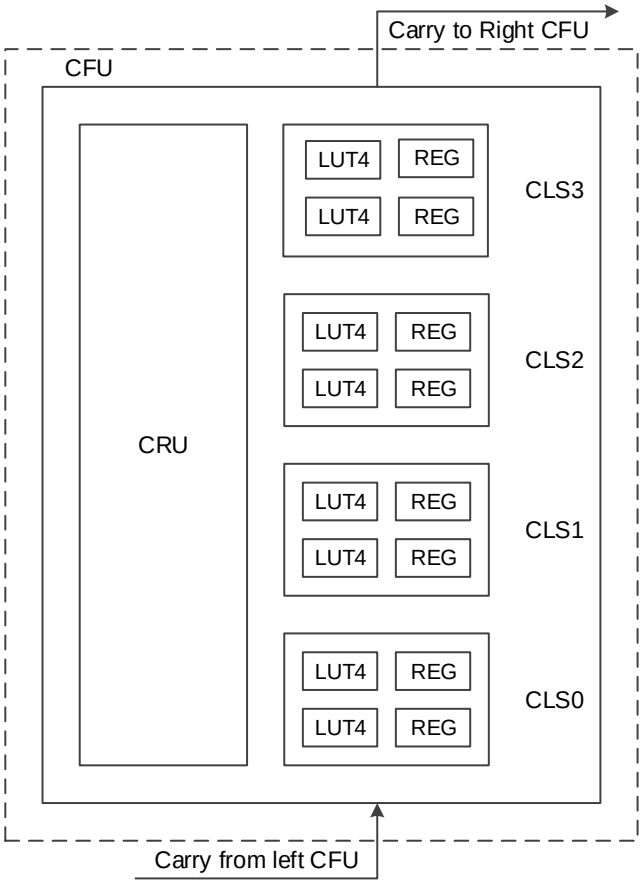
2.2 Configurable Function Units

Configurable Function Units (CFUs) are the basic cells for the array of GOWINSEMI FPGA Products. Each basic cell consists of four Configurable Logic Sections (CLSs) and their routing resource Configurable Routing Units (CRUs). Each CLS includes two 4 input look-up-tables (LUTs) and two registers (REGs), as shown in Figure 2-3 .

CLSs in the CFUs can be configured as basic look-up tables, arithmetic logic units, static random access memories, and read only memories according to application scenarios.

For more details, please see *UG303, Arora V Configurable Function Unit (CFU) User Guide*.

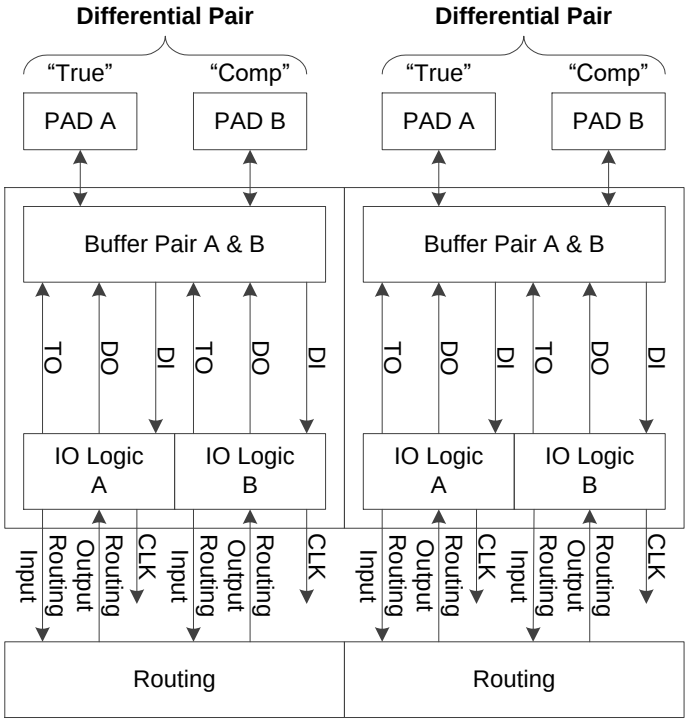
Figure 2-3 CFU Structure View



2.3 Input/Output Blocks

The IOB in the Arora V 60K FPGA products includes IO buffer, IO logic, and its routing units. As shown in Figure 2-4 , each IOB connects to two Pins (Marked as A and B). They can be used as a differential pair or as a single end input/output.

Figure 2-4 IOB Structure View



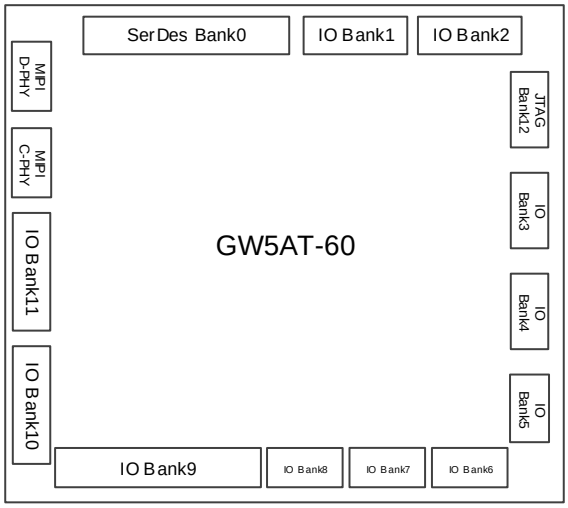
IOB Features:

- V_{CCIO} supplied with each bank
- All banks support True differential input
- Supports multiple levels: LVCMOS, PCI, LVTTL, SSTL, HSTL, LVDS, Mini_LVDS, RSDS, PPDS, BLVDS
- Input hysteresis option
- Output drive strength option
- Slew Rate
- Individual bus keeper, weak pull-up, weak pull-down, and open drain option
- Hot socket
- IO logic supports SDR mode, DDR mode, etc.

2.3.1 I/O Buffer

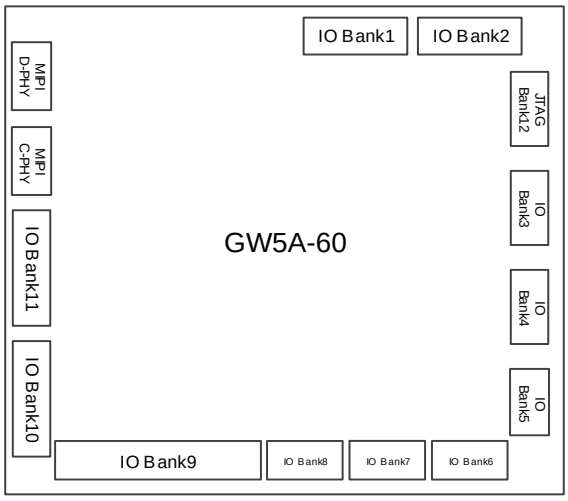
GW5AT-60 has eleven GPIO Banks. Bank12 is a JTAG Bank with four IOs, as shown in Figure 2-5.

Figure 2-5 GW5AT-60 I/O Bank Distribution



GW5A-60 has eleven GPIO Banks. Bank12 is a JTAG Bank with four IOs, as shown in Figure 2-6.

Figure 2-6 GW5A-60 I/O Bank Distribution



Each Bank has independent I/O power supply V_{CCIO}. V_{CCIO} can be set as 3.3V, 2.5V, 1.8V, 1.5V, 1.35V, or 1.2V. The auxiliary voltage V_{CCX} of Arora V 60K FPGA products supports 1.8V, 2.5V, or 3.3V.

Note!

To support SSTL, HSTL, etc., each bank also provides one independent voltage source (VREF) as the reference voltage. You can choose from the internal reference voltage of the bank (0.6V, 0.75V, 0.9V, 1.25V, 1.5V, and (36%,50%,64%)VccIo) or the external reference voltage using any IO from the bank.

Different banks in the Arora V 60K FPGA Products support different on-chip resistor settings, including single-ended resistor and differential resistor. Single-ended resistor is set for SSTL/HSTL I/O. Differential resistor is set for LVDS/PPDS/ RSDS input. For more details, refer to *UG304, Arora V Programmable IO (GPIO) User Guide* .

Note!

Before and during configuration, all GPIOs of the device have weak pull-up by default. The default I/O state is None after configuration is complete and it can be configured via the Gowin software. The status of configuration-related I/Os differs depending on the configuration mode.

I/O Standards and Configuration Options Supported by Arora V 60K FPGA products are listed in Table 2-1 and Table 2-2.

Table 2-1 Output I/O Standards and Configuration Options

I/O output standard	Single-ended/Differential	Bank V_{CCIO}(V)	Output Drive Strength (mA)	Typical Applications
MIPI_CPHY	Differential(TLVDS)	2.5/3.3	2	Mobile Industry Processor Interface
MIPI		1.8/2.5/3.3	2	Mobile Industry Processor Interface
MIPI_3MA	Differential(ELVDS)	1.8	3	Mobile Industry Processor Interface
MIPI_4MA		1.8	4	Mobile Industry Processor Interface
LVDS25	Differential(TLVDS)	2.5/3.3	3.5/2.5/4.5/6	High-speed point-to-point data transmission
BLVDS25		2.5/3.3	3.5/2.5/4.5/6	Multi-point high-speed data transmission
RSDS		2.5/3.3	3.5/2.5/4.5/6	High-speed point-to-point data transmission
MINILVDS		2.5/3.3	3.5/2.5/4.5/6	LCD timing driver interface and column driver interface
PPLVDS		2.5/3.3	3.5/2.5/4.5/6	LCD row/column driver
LVDS25E	Differential	2.5	8/2/4/6/12/16	High-speed point-to-point data transmission
BLVDS25E		2.5	8/2/4/6/12/16	Multi-point high-speed data transmission
MLVDS25E		2.5	8/2/4/6/12/16	LCD timing driver interface and column driver interface
RSDS25E		2.5	8/2/4/6/12/16	High-speed point-to-point data transmission
LVPECL33E		3.3	8/2/4/6/12/16	Universal interface
HSUL12D		1.2	8/2/4/6	LPDDR2
HSUL12D_I		1.2	8/2/4/6	LPDDR2
HSTL15D_I		1.5	8/4/12	Memory interface
HSTL18D_I		1.8	8/2/4/6/12/16	Memory interface
HSTL18D_II		1.8	8/2/4/6/12/16	Memory interface
SSTL12D_I		1.2	8/2/4/6	Memory interface
SSTL135D_I		1.35	8/2/4/6	Memory interface
SSTL15D_I		1.5	8/2/4/6/12	Memory interface
SSTL18D_I		1.8	8/2/4/6/12/16	Memory interface
SSTL18D_II		1.8	8/2/4/6/12/16	Memory interface
SSTL25D_I		2.5	8/2/4/6/12/16	Memory interface
SSTL25D_ II		2.5	8/2/4/6/12/16	Memory interface
SSTL33D_I		3.3	8/2/4/6/12/16	Memory interface
SSTL33D_II		3.3	8/2/4/6/12/16	Memory interface

I/O output standard	Single-ended/Differential	Bank V_{CCIO}(V)	Output Drive Strength (mA)	Typical Applications
LPDDRD	Single-ended	1.8	8/2/4/6/12/16	LPDDR and Mobile DDR
LVCMOS10D		1.0	2/4	Universal interface
LVCMOS12D		1.2	8/2/4/6	Universal interface
LVCMOS15D		1.5	8/2/4/6/12	Universal interface
LVCMOS18D		1.8	8/2/4/6/12/16	Universal interface
LVCMOS25D		2.5	8/2/4/6/12/16	Universal interface
LVCMOS33D		3.3	8/2/4/6/12/16	Universal interface
HSUL12		1.2	8/2/4/6	Memory interface
HSTL12_I		1.2	8/2/4/6	Memory interface
HSTL15_I		1.5	8/2/4/6/12	Memory interface
HSTL18_I		1.8	8/2/4/6/12/16	Memory interface
HSTL18_II		1.8	8/2/4/6/12/16	Memory interface
SSTL12_I		1.2	8/2/4/6	Memory interface
SSTL135_I		1.35	8/2/4/6	Memory interface
SSTL15_I		1.5	8/2/4/6/12	Memory interface
SSTL18_I		1.8	8/2/4/6/12/16	Memory interface
SSTL18_II		1.8	8/2/4/6/12/16	Memory interface
SSTL25_I		2.5	8/2/4/6/12/16	Memory interface
SSTL25_II		2.5	8/2/4/6/12/16	Memory interface
SSTL33_I		3.3	8/2/4/6/12/16	Memory interface
SSTL33_II		3.3	8/2/4/6/12/16	Memory interface
LVCMOS10		1.0	2/4	Universal interface
LVCMOS12		1.2	8/2/4/6	Universal interface
LVCMOS15		1.5	8/2/4/6/12	Universal interface
LVCMOS18		1.8	8/2/4/6/12/16	Universal interface
LVCMOS25		2.5	8/2/4/6/12/16	Universal interface
LVCMOS33/LVTTL33		3.3	8/2/4/6/12/16	Universal interface
LPDDR		1.8	8/2/4/6/12/16	LPDDR and Mobile DDR
PCI33		3.3	8/2/4/6/12/16	PC and embedded system

Table 2-2 Input I/O Standards and Configuration Options

I/O Input Standard	Single-ended/Differential	Bank V_{CCIO}(V)	Hysteresis	Need V_{REF}
MIPI_CPHY	Differential	1.2/1.5/1.8	No	No
MIPI		1.2/1.5/1.8	No	No
ADC_IN		2.5/1.0/1.2/1.5/1.8/3.3	No	No

I/O Input Standard	Single-ended/Differential	Bank V_{CCIO}(V)	Hysteresis	Need V_{REF}
LVDS25		2.5/1.0/1.2/1.5/1.8/3.3	No	No
BLVDS25		2.5/1.0/1.2/1.5/1.8/3.3	No	No
RSDS		2.5/1.0/1.2/1.5/1.8/3.3	No	No
MINILVDS		2.5/1.0/1.2/1.5/1.8/3.3	No	No
PPLVDS		2.5/1.0/1.2/1.5/1.8/3.3	No	No
HSUL12D		1.2/1.0/1.5/1.8/2.5/3.3	No	No
HSTL12D_I		1.2/1.0/1.5/1.8/2.5/3.3	No	No
HSTL15D_I		1.5/1.0/1.2/1.8/2.5/3.3	No	No
HSTL18D_I		1.8/1.0/1.2/1.5/2.5/3.3	No	No
HSTL18D_II		1.8/1.0/1.2/1.5/2.5/3.3	No	No
SSTL135D_I		1.35/1.0/1.2/1.5/1.8/2.5/3.3	No	No
SSTL15D_I		1.5/1.0/1.2/1.8/2.5/3.3	No	No
SSTL18D_I		1.8/1.0/1.2/1.5/2.5/3.3	No	No
SSTL18D_II		1.8/1.0/1.2/1.5/2.5/3.3	No	No
SSTL25D_I		2.5/1.0/1.2/1.5/1.8/3.3	No	No
SSTL25D_ II		2.5/1.0/1.2/1.5/1.8/3.3	No	No
SSTL33D_I		3.3/1.0/1.2/1.5/1.8/2.5	No	No
SSTL33D_ II		3.3/1.0/1.2/1.5/1.8/2.5	No	No
LPDDRD		1.8/1.0/1.2/1.5/2.5/3.3	No	No
LVCMOS10D		1.0/1.2/1.5/1.8/2.5/3.3	No	No
LVCMOS12D		1.2/1.0/1.5/1.8/2.5/3.3	No	No
LVCMOS15D		1.5/1.0/1.2/1.8/2.5/3.3	No	No
LVCMOS18D		1.8/1.0/1.2/1.5/2.5/3.3	No	No
LVCMOS25D		2.5/1.0/1.2/1.5/1.8/3.3	No	No
LVCMOS33D		3.3/1.0/1.2/1.5/2.5/1.8	No	No
HSUL12	Single-ended	1.2	Yes	No
HSTL12_I		1.2	Yes	No
HSTL15_I		1.5	Yes	No
HSTL15_II		1.5	Yes	No
HSTL18_I		1.8	Yes	No
HSTL18_II		1.8	Yes	No
SSTL135_I		1.35	Yes	No
SSTL15_I		1.5	Yes	No
SSTL18_I		1.8	Yes	No
SSTL18_II		1.8	Yes	No
SSTL25_I		2.5	Yes	No
SSTL25_II		2.5	Yes	No
SSTL33_I		3.3	Yes	No

I/O Input Standard	Single-ended/Differential	Bank V_{CCIO}(V)	Hysteresis	Need V_{REF}
SSTL33_II		3.3	Yes	No
LVCMOS10		1.0	Yes	No
LVCMOS12		1.2	Yes	No
LVCMOS15		1.5	Yes	No
LVCMOS18		1.8	Yes	No
LVCMOS25		2.5	Yes	No
LVCMOS33/LVTTL33		3.3	Yes	No
LPDDR		1.8	Yes	No
PCI33		3.3	Yes	No
LVCMOS10UD12		1.2	Yes	No
LVCMOS10UD15		1.5	Yes	No
LVCMOS10UD18		1.8	Yes	No
LVCMOS10UD25		2.5	Yes	No
LVCMOS10UD33		3.3	Yes	No
LVCMOS12OD10		1.0	Yes	No
LVCMOS12UD15		1.5	Yes	No
LVCMOS12UD18		1.8	Yes	No
LVCMOS12UD25		2.5	Yes	No
LVCMOS12UD33		3.3	Yes	No
LVCMOS15OD10		1.0	Yes	No
LVCMOS15OD12		1.2	Yes	No
LVCMOS15UD18		1.8	Yes	No
LVCMOS15UD25		2.5	Yes	No
LVCMOS15UD33		3.3	Yes	No
LVCMOS18OD10		1.0	Yes	No
LVCMOS18OD12		1.2	Yes	No
LVCMOS18OD15		1.5	Yes	No
LVCMOS18UD25		2.5	Yes	No
LVCMOS18UD33		3.3	Yes	No
LVCMOS25OD10		2.5	Yes	No
LVCMOS25OD12		3.3	Yes	No
LVCMOS25OD15		1.5	Yes	No
LVCMOS25OD18		1.8	Yes	No
LVCMOS25UD33		3.3	Yes	No
LVCMOS33OD10		1.0	Yes	No
LVCMOS33OD12		1.2	Yes	No
LVCMOS33OD15		3.3	Yes	No
LVCMOS33OD18		1.8	Yes	No

I/O Input Standard	Single-ended/Differential	Bank V_{CCIO}(V)	Hysteresis	Need V_{REF}
LVCMOS33OD25		2.5	Yes	No
VREF1_DRIVER		1.8/1.2/1.5/2.5/3.3	No	Yes

2.3.2 I/O Logic

Figure 2-7 shows the I/O logic output of Arora V 60K FPGA products.

Figure 2-7 I/O Logic Output

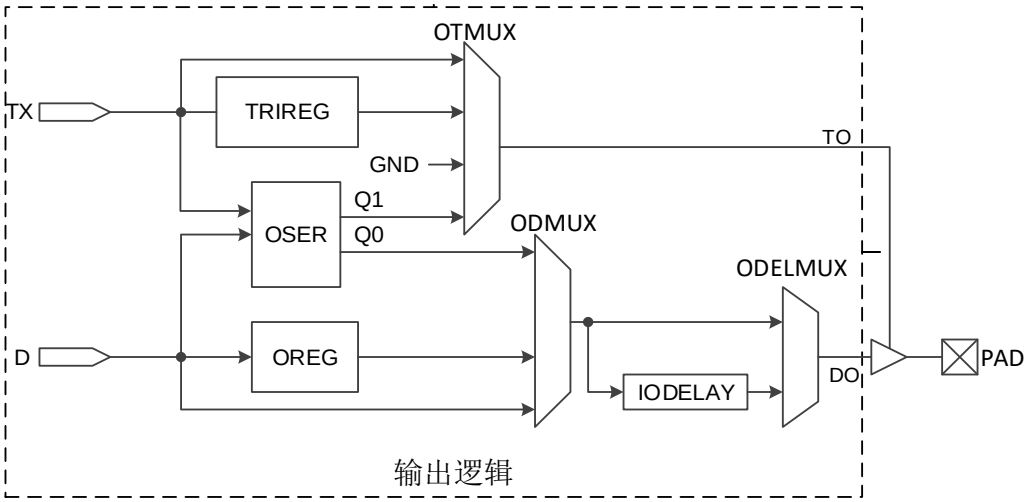
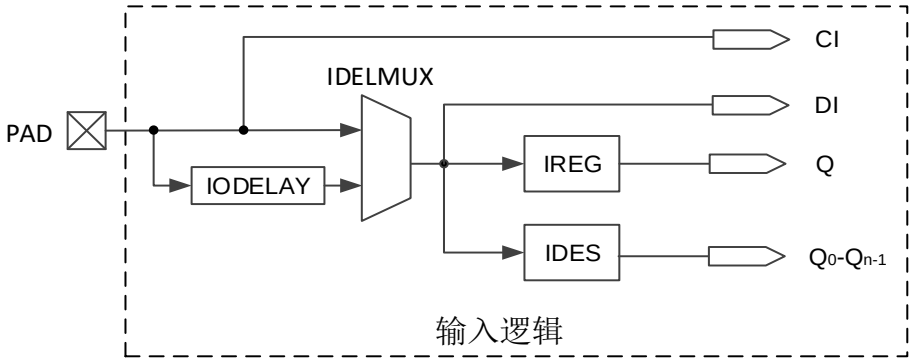


Figure 2-8 shows the I/O logic input of the Arora V 60K FPGA products.

Figure 2-8 I/O Logic Input



The I/O logic module description of Arora V 60K FPGA products are presented below.

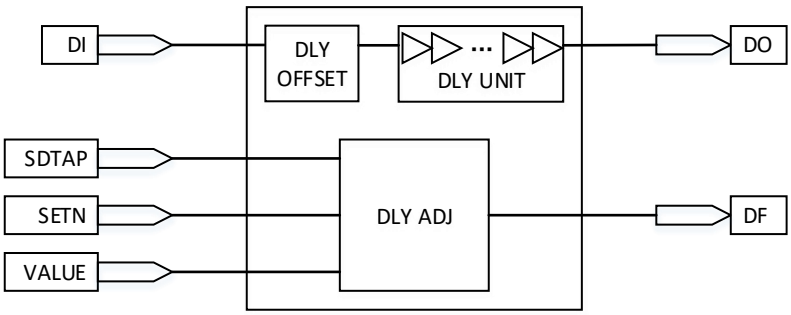
Delay Module

See Figure 2-9 for an overview of the IODELAY. Each I/O contains an IODELAY module, which allows the user to add additional delays to the I/Os to adjust the delay of the input and output signals. The delay time for each step is $T_{dlyunit}$, and the total number of delay steps is DLYSTEP. The total IODELAY delay time is: $T_{totdly} = T_{dlyoffset} + T_{dlyunit} * DLYSTEP$. The total delay reference time is as shown in Table 2-3.

Table 2-3 Total Delay Reference of IODELAY

	Min.	Typ.	Max.
$T_{dlyoffset}$	200 ps	250 ps	300 ps
$T_{dlyunit}$	10 ps	12.5 ps	15 ps
DLYSTEP	0	-	255

Figure 2-9 IODELAY



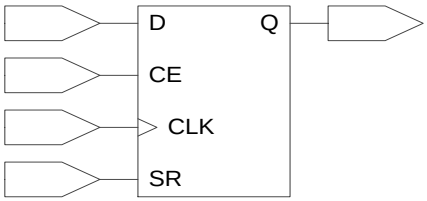
There are three ways to control the delay:

- Static control.
- Dynamic control, which can be combined with logic function circuits to achieve dynamic delay adjustment.
- Adaptive control.

I/O Register

See Figure 2-10 for the I/O Register diagram. Each I/O provides an input register (IREG), an output register(OREG), and a tristate Register(TRIREG).

Figure 2-10 Diagram of I/O registers



Note!

- CE can be either active ow (0: enable) or active high (1: enable).
- CLK can be either rising edge trigger or falling edge trigger.
- SR can be either synchronous/asynchronous SET or RESET or disable.
- The registers can be programmed as registers(DFFs) or latches.

DES and SER

Arora V 60K FPGA Products support serialization and deserialization of various ratios, as listed in the following table:

Table 2-4 Serialization/Deserialization

	Ratios Supported
Input Logic	1:2 / 1:4 / 1:7 / 1:8 / 1:10 / 1:14 / 1:16 / 1:32
Output Logic	2:1 / 4:1/ 7:1 / 8:1 / 10:1 / 16:1 / 14:1

2.3.3 I/O Logic Modes

The I/O Logic in Arora V 60K FPGA products supports several modes. In each operation, the I/O (or I/O differential pair) can be configured as output, input, and INOUT or tristate output (output signal with tristate control).

For further details about the I/O logic modes, refer to *UG304, Arora V Programmable IO (GPIO) User Guide* .

2.4 Block SRAM (BSRAM)

2.4.1 Introduction

Arora V 60K FPGA products provide abundant block SRAM resources. These memory resources are distributed throughout the FPGA array in the form of rows. Therefore, they are called block static random access memories (BSRAMs). There are five operation modes: Single Port mode, Dual Port mode, Semi-Dual Port mode, Semi-Dual Port mode with ECC function, and ROM mode.

An abundance of BSRAM resources provide a guarantee for the user's high-performance design. BSRAM's features:

- The capacity of a BSRAM is 18 Kbits, can be configured up to 36 Kbits
- Clock frequency up to 380MHz (230 MHz in Read-before-Write mode)
- Supports Single Port mode
- Supports Dual Port mode
- Supports Semi-Dual Port Mode
- Supports ECC detection and error correction Function
- Supports ROM Mode
- Data width up to 72bits
- Supports byte-enable
- Dual Port and Semi-Dual Port support independent clocks and independent data width
- Read mode supports Register Output and Bypass Output
- Write mode supports Normal, Read-before-write, and Write-Through
- Input registers support synchronous writes

2.4.2 Configuration Mode

BSRAMs in the Arora V 60K FPGA products support various data widths. See Table 2-5.

Table 2-5 Memory Size Configuration

Capacity	Single Port Mode	Dual Port Mode	Semi-Dual Port Mode	Semi-Dual Port Mode with ECC Function	Read Only Mode
16Kbits	16K x 1	16K x 1	16K x 1	–	16K x 1
	8K x 2	8K x 2	8K x 2	–	8K x 2
	4K x 4	4K x 4	4K x 4	–	4K x 4
	2K x 8	2K x 8	2K x 8	–	2K x 8
	1K x 16	1K x 16	1K x 16	–	1K x 16

Capacity	Single Port Mode	Dual Port Mode	Semi-Dual Port Mode	Semi-Dual Port Mode with ECC Function	Read Only Mode
18Kbits	512 x 32	–	512 x 32	–	512 x 32
	2K x 9	2K x 9	2K x 9	–	2K x 9
	1K x 18	1K x 18	1K x 18	–	1K x 18
	512 x 36	–	512 x 36	–	512 x 36
36Kbits	–	–	–	512 x 72	–

For more information on Single Port mode, Dual Port mode, Semi-Dual Port mode, Semi-Dual Port with ECC Function, and ROM mode, please refer to *UG300，Arora V BSRAM & SSRAM User Guide*.

Semi-DualSemi-DualSemi-Dual

2.4.3 Semi-DualSemi-DualSemi-DualSemi-DualECC

The BSRAM of GW5AT-60 has a built-in ECC hardcore module, which is mainly used for data detection and correction during data transfer and storage. The features are as follows:

- ECC error detection and correction only supported in SDP 512 x 64 mode
- Supports 1-bit error correction and 2-bit error alarm in 64-bit SRAM data
- 72-bit ECC module contains 64-bit data bits and 8-bit parity bits;
- Bit 31 and bit 63 support 1-bit and 2-bit error injection

2.5 DSP

Arora V 60K of FPGA Products provide brand new DSP resources. This DSP solution can meet user demands for high performance digital signal processing design, such as FIR, FFT, etc. The DSP blocks have the advantages of stable timing performance, high resource utilization, and low power consumption.

The features of DSP are as follows.

- Can be configured as 12 x 12, 27 x 28, and 27 x 36 signed multipliers
- 48-bit ALU
- Multipliers cascading to support wider data
- Barrel Shifter
- Adaptive filtering through signal feedback
- Supports pipeline mode and bypass mode.
- All operands for arithmetic operation are signed numbers

Each DSP consists of three stages:

- PADD
- MULT
- Arithmetic Logic Unit

2.5.1 PADD

Each DSP features one PADD(pre-adder) for implementing pre-addition, pre-subtraction, and shifting.

PADD locates at the first stage with two inputs:

- 26-bit input C;
- Parallel 26-bit input A or SIA.

Each input end supports pipeline mode and bypass mode.

2.5.2 MULT

Each DSP block has one 27 x 18 multiplier M0 and one 12 x 12 multiplier M1. The multipliers are located after the pre-adders to implement multiplication operations, and both the inputs and outputs support register mode and bypass mode.

Multiplier M0 can be configured as:

- One 27 x 18 multiplier
- One 12 x 12 multiplier
- Two DSPs can form a 27 x 36 multiplier

Multiplier M1 can only be configured as one 12 x 12 multiplier.

When multiplier M0 and multiplier M1 are both configured as a 12 x 12 multiplier and the ALU is enabled, 12 x 12 SUM mode can be achieved.

2.5.3 Arithmetic Logic Unit

Each Macro has one four-input 48-bit ALU, which can further enhance MULT's functions. Register mode and bypass mode are supported both in the inputs and outputs. The ALU supports the addition/subtraction operations of multiplier M0 output, multiplier M1 output (48bit operand D), ALU cascade input CASI and ALU output feedback, or static PRE_LOAD value.

2.5.4 Operating Mode

Multiple operation modes of the DSP can be realized by control signals. Operation Modes:

- Multiplier
- Accumulator
- MULTADDALU

For more information on DSP Blocks, see *UG305E, Arora V Digital Signal Processing (DSP) User Guide*.

2.6 Gigabit Transceivers

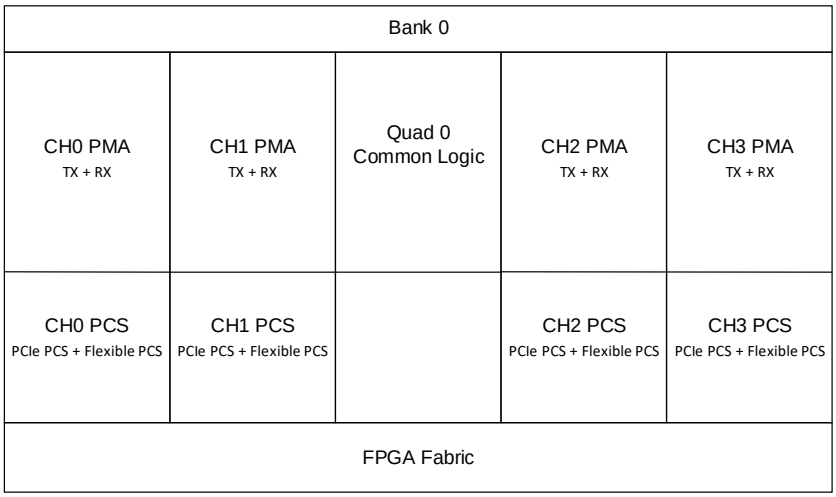
Arora V 60K FPGA products support one Transceiver Quad. Each Quad supports up to four transceivers, and each transceiver is comprised of one TX and one RX, with the data rate raging from 270Mbps to 12.5Gbps, and supports flexible PMA and PCS.

Figure 2-11 shows the structure view of Transceiver Quad. The protocols supported are as follows:

- PCI Express, V3.0 (2.5 Gbps /5.0 Gbps)
- 10 Gigabit Attachment Unit Interface (XAUI) (3.125Gbps)

- RXAUI (Reduced XAUI) (6.25Gbps)
- CEI-6G-SR (6.375Gbps)
- SATA Rev3.2 (6Gbps/3Gbps/1.5Gbps) (need soft IP support)
- Serial GMII(SGMII) (1.25Gbps)
- CPRI (need soft IP support; soft IP available)
- JESD204B (need soft IP support; soft IP available)
- Rapid-IO (need soft IP support; soft IP available)
- 1000Base-X (need soft IP support; soft IP available)
- 10G-Base-R (need soft IP support; soft IP available)
- SDI-TX/RX (need soft IP support; soft IP available)
- SLVS-EC(RX) (need soft IP support; soft IP available)
- Interlaken

Figure 2-11 Gigabit Transceiver Architecture View



PMA

- Each PMA contains 4 lanes. Each lane supports simultaneous sending and receiving of data, including independent TX and RX, and supports different rates of sending and receiving.
- Each Quad shares two PLLS (one is LC PLL, the other is ring oscillator PLL)
- Transmitter through tracking of spread reference clock.
- Lane driver with programmable transmitter equalization with 1 tap pre-cursor and 1 tap post-cursor to improve signal integrity.
- Voltage mode/current mode lane driver with board AC coupling.
- Programmable continuous time linear equalizer (CTLE) with auto-adaption.

- Receiver CDR track SSC data and tolerance +/- 5000ppm variation.
- Beacon signaling generation and detection for PCI Express.

PCS

- Dedicated hard PCIe PCS
- Flexible PCS to support PCS customization
- 8b/10b/64b/66b encoder/decoder
- Supports TX channel bonding
- Supports RX channel bonding and CTC
- Utilize IF FIFO to simply user system design
- Supports flexible parallel data widths of 8/10/16/20/32/40/64/80 bits

2.7 PCI Express (PCIe) Controller

GW5AT-60 includes one integrated block for PCI Express technology. It allows custom FPGA-to-FPGA communication via the PCI Express protocol, and to attach ASSP Endpoint devices, such as Ethernet Controllers or Fiber Channel HBAs (Host Bus Adapter), to the FPGA.

Features of the PCIe integrated block are as follows:

- Dedicated hard core IP, Compliant to the PCI Express Base Specification 3.0
- Supportsx1, x2, x4 lanes
- Supports End Point
- Supports Gen1 (2.5 GT/s), Gen2 (5 GT/s), and Gen3 (8 GT/s)
- Up to six BARs, resizable
- Lane reversal
- Lane reversal
- Supports CrossLink connection mode
- Supports Multicast
- Supports ARI (Alternative Routing-ID Interpretation)
- Supports IDO (ID-based Ordering)
- Retimer (extension device) presence detection
- Supports TPH (TLP Processing Hints)
- Supports ACS (Access Control Services)
- Supports DPC (Downstream Port Containment)
- Supports PTM (Precision Time Measurement)
- Supports Autonomous link speed/width change
- Supports MAC controller with individual AHB bus for register

- Two physical functions
- Supports advanced configuration options, Advanced Error Reporting (AER), and End-to-End Cyclic Redundancy Check (ECRC)
- Configurable parameters: channel width, maximum payload size, FPGA logical interface speeds, reference clock frequency, base address register decoding and filtering, etc.

For more information on PCIe Controller, see *IPUG1020E, Arora V PCIe Controller User Guide*.

2.8 MIPI D-PHY

2.8.1 Hardcore MIPI D-PHY

Arora V 60K FPGA products provide a MIPI D-PHY hardcore supporting MIPI D-PHY RX and MIPI D-PHY TX. The dedicated D-PHY core supports MIPI DSI and CSI-2 mobile video interfaces for cameras and displays. The main features of the FIFO IP are as follows:

- In line with *MIPI Supported Standard for D-PHY Specification*, version 1.2;
- High Speed RX/TX up to 10 Gbps with four data lanes.
- One MIPI Quad supports up to four data lanes and one clock lane.
- Bidirectional Low-power (LP) mode at up to 10Mbps per lane
- Built-in HS Sync, bit and lane alignment
- 1:8 and 1:16 deserialization modes to FPGA fabric's user interface
- Supports MIPI DSI and MIPI CSI-2 link layers.

For more information on Gowin MIPI D-PHY, pleae refer to *UG296, Arora V Hardened MIPI D-PHY RX TX User Guide*.

2.8.2 GPIOs Support MIPI D-PHY RX/TX (MIPI IO)

The GPIOs support MIPI IO mode. MIPI D-PHY RX/TX implemented by using MIPI IO mode supports MIPI DSI and CSI-2 interfaces for cameras and displays in both transmitting and receiving modes. MIPI D-PHY provides a physical layer definition. The MIPI IO mode support for Arora V 60K FPGA products is as listed in the table below.

Table 2-6 MIPI IO Mode Support List for Arora V 60K FPGA Products

MIPI RX	All Banks (except JTAG Bank)
MIPI TX	All Banks (except JTAG Bank)

The main features of the FIFO IP are as follows:

- MIPI Alliance Standard for D-PHY Specification, Version 1.2
- High Speed RX and TX at up to 2.0Gbps per MIPI lane
- Supports unidirectional High-speed (HS) mode
- Supports bidirectional Low-power operation mode
- Deserializes and serializes high-speed data into byte data packets
- Supports MIPI D-PHY TX 8:1 mode and 16:1 mode
- Supports MIPI D-PHY RX 1:8 mode and 1:16 mode
- Supports IO Types of ELVDS, TLVDS, and MIPI IO
- Control data is transmitted in LP mode at a data rate of 10 Mb/s.

For more detailed information, please refer to *IPUG948E，MIPI D-PHY RX TX Advance User Guide.*

2.9 MIPI C-PHY

2.9.1 Hardcore MIPI C-PHY

The Arora V 60K FPGA products offer the hard-core MIPI C-PHY RX and TX, featuring highly efficient data transfer rates, and is primarily suited for high-speed serial interfaces between cameras and image processors.

- MIPI Alliance Standard for C-PHY Specification, Version 1.2.
- One MIPI Quad supports up to 3 three-wire data channels and supports up to 2.5Gsps (=5.75Gbps, RX/TX) data rate per channel.
- MIPI C-PHY RX supports high-speed mode and automatic interrupt control.
- MIPI C-PHY TX supports high-speed mode
- Bidirectional Low mode with data rates up to 10Mbps
- High speed RX mode supports De-skew function
- RX supports a linear equalizer with a maximum Delta peak > 8dB
- Supports ALP mode (optional)

2.10 ADC

To meet different application needs, Arora V 60K FPGA products integrate two types of ADCs: SARADC and ADC Sensor.

2.10.1 SARADC

SARADC is a 13bit ADC for high-speed signal sampling, which is capable of meeting high-precision reference voltage requirements, and is usually used in scenarios requiring high precision. The main features are as follows:

- 13bits SAR ADC with sample rates from 100K ~ 5MSPS (optional up to 10MSPS)
- Supports single-ended and differential inputs. Single-ended input signal range: 0-1V. Differential signal range: -1V to 1V.
- Supports off-chip and on-chip voltage reference sources, configurable.
- SNR > 60dB. INL: +/- 2LSB; DNL: +/- 1LSB.
- Supports range calibration and bias calibration.
- Supports single and continuous sampling.
- Supports MDRP interface configuration.

2.10.2 ADC Sensor

ADC sensor is a Delta-sigma structure ADC with on-chip temperature

sensing unit, which can meet the on-chip temperature monitoring and digital quantization. ADC sensor is a low-cost solution to meet the needs of lower-speed signal monitoring with an integrated reference voltage source. The deviation due to reference voltage can also be solved by auto-calibration.

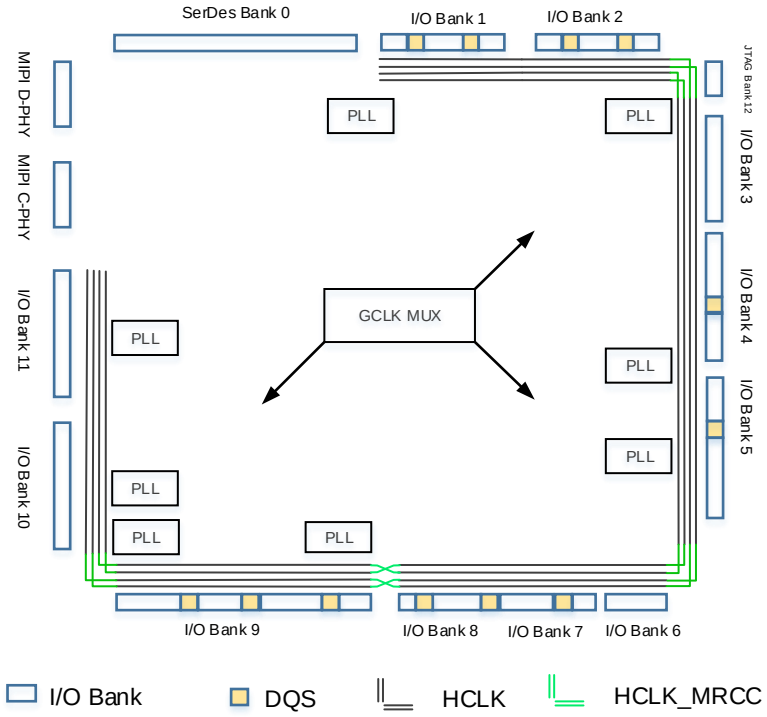
The main features are as follows:

- 10bits Delta-sigma ADC with oversampled signal frequency <10MHz.
- Signal input range: 0-1V.
- Integrates on-chip reference voltage source.
- Temperature detection accuracy: +/-4°C.
- Voltage detection accuracy: +/-5mV.
- Supports single and continuous sampling.
- Supports chip temperature measurement.
- Supports MDRP interface configuration.

2.11 Clock

The clock resources and wiring are critical for high-performance applications in FPGA. Arora V 60K FPGA products provide the global clock network(GCLK) which connects to all the device resources directly. In addition to the GCLK, PLL, HCLK, DDR memory interface, and DQS, etc. are also provided.

Figure 2-12 GW5AT-60 Clock Resources



Please refer to 2.11.1 ~ 2.11.4 for a brief introduction. For further detailed information on the GCLK, HCLK, DDR memory interface, and DQS, see *UG306, Arora V Clock User Guide*.

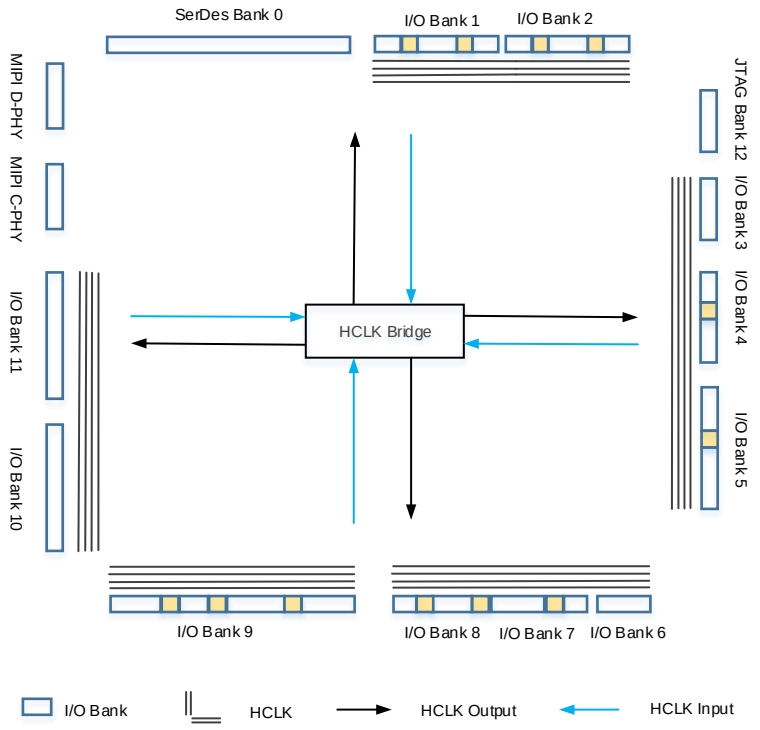
2.11.1 Global Clock

Arora V 60K FPGA products provide 16 global clocks. The clock source of GCLK comes from dedicated clock pins, PLL outputs, SERDES clocks, HCLK outputs, and common routing resources. Using a dedicated clock input pin provides better clock performance and enables driving of the global.

2.11.2 High-speed Clock

HCLK is the high-speed clock with low jitter and low skew. It can support high-performance I/O data transfer and is mainly suitable for source synchronous data transfer protocols. One bank supports 4 HCLKs, as shown in Figure 2-13.

Figure 2-13 GW5AT-60 HCLK Distribution



HCLK can provide user with the function modules as follows:

- Dynamic high-speed clock enable module. Able to dynamically turn on/off the high-speed clock signal.
- High speed clock frequency division module, generating a divided clock of the input clock. Used in the IO logic mode.
- Dynamic high speed clock selector.
- Dynamic delay adjustment module, producing the clock signal for the dedicated clock pin input.
- HCLK Bridge, able to send HCLK clock signals to any of the Banks. In addition, the HCLK clock signal can span to the clock tree of the adjacent IO Bank after entering from the IO Bank.

Note!

For high speed signals of the same source, it is recommended to put them in the same IO Bank to achieve a minimum skew between signals.

2.11.3 Phase-locked Loop

PLL (Phase-locked Loop) is one kind of a feedback control circuit. The frequency and phase of the internal oscillator signal is controlled by the external input reference clock.

The PLL module can provide synthesizable clock frequencies. Frequency adjustment (multiply and division), phase adjustment, and duty cycle adjustment can be achieved by configuring the parameters.

The PLL module features are as follows:

- Supports seven clock outputs
- Integer PLL, the first clock output and feedback clock output support 1/8 fractional output division
- Supports phase shift and duty cycle adjustment
- Frequency Lock detection
- Supports spread spectrum clock generation (IP required)
- VCO frequency range: 800 MHz ~ 2000 MHz
- CLKIN frequency range: 19 MHz ~ 800 MHz.

2.11.4 DDR Memory Interface Clock Management DQS

The DQS module provides the following features to support the clock requirements of the DDR memory interface:

- Receive DQS input, sort out waveform and shift 1/4 phase
- Provide a read / write pointer for input cache
- Provide valid data for internal logic
- Provide DDR output clock signal
- Support DDR3 write voltage control

The DQS module supports multiple operating modes to meet the needs of different I/O interfaces.

2.11.5 Long Wire

As an effective complement to CRUs, the Arora V 60K FPGA products provide flexible and rich long-wire (LW) resources. LW can be used as a control wire to provide clock enable (CE) for DFF, set/reset signal; it can also be used as logic winding and as a common data signal.

2.12 Global Set/Reset (GSR)

A global set/rest (GSR) network is built in the Arora V 60K FPGA product. There is a direct connection to core logic. It can be used as asynchronous/synchronous set. The registers in CFU and I/O can be individually configured to use GSR.

2.13 Programming & Configuration

The Arora V 60K FPGA products support SRAM configuration. Each time the device is powered on, the bitstream needs to be downloaded to configure the device. You can also save the configuration data in an external Flash. After power-up, the GW5AT device loads configuration data from the external Flash into the SRAM.

Besides JTAG, the Arora V 60K of FPGA products also support GowinCONFIG configuration modes: SSPI, MSPI, Slave CPU, Slave

SERIAL, and PCIe. The FPGAs also support background programming, datastream file encryption and security bit setting, SEU detection and error correction, and OTP. For the detailed information, please refer to *UG718, Arora V 60K FPGA Products Programming and Configuration User Guide*.

Background Upgrade

The Arora V 60K FPGA products support background upgrade by JTAG/SSPI/QSSPI or using the goConfig I2C IP / goConfig JTAG IP, that is, the device supports programming the embedded Flash or the external Flash without affecting the existing working state, the device can work Normally according to the original configuration during the programming process. And after the programming is completed, trigger RECONFIG_N with a low level or use “Reboot” to complete the online upgrade. This feature applies to the applications requiring long online time and irregular upgrades.

Bitstream File Encryption & Security Bit Setting

The Arora V 60K of FPGA products support bitstream data encryption with 128-bit AES encryption algorithm. At the same time, GOWINSEMI adds CRC and sets security bits in the bitstream file of FPGA products by default in order to guarantee the safe and accurate transmission of configuration data. During the data configuration process, the input data is verified in real time for errors, and the device cannot be woken up by incorrect data. After the configuration of the bitstream with security bit is complete, data readback cannot be performed.

SEU Handler

The configuration SRAM integrates a SEU handler module, which supports configuration memory soft error recovery (CMSER) and are mainly used for data detection and correction of the FPGA configuration data. It is disabled by default. The features are as follows:

- Supports ECC and CRC error detection and correction.
- The SEU function can be enabled or disabled by user logic, or the function can be enabled automatically upon program wakeup
- ECC supports 2-bit error location report and error correction [1] and 4-bit error alarm in each SRAM Frame

  Note!

  - [1]Support for 2-bit error location reporting and error correction under certain conditions, please refer to the *UG297, Arora V SEU Handler User Guide for details* .
  - [1] SEU Handler can support faster error correction. Please contact local technical support for details.
- CRC supports any bit error alarm
- Supports 1-bit error injection at any position, two errors per SRAM Frame
- The detection and error correction function of SRAM in this storage area will be automatically turned off when the user turns on the SSRAM storage function

OTP

Arora Ⅴ 60K FPGA products provide a 128-bit OTP space and support one-time programming. Bit0 ~ Bit31 is the user space, which can be used to store security and other important information. Bit32~Bit95 is the DNA space, which stores the 64-bit unique identification information of the device.

2.14 On Chip Oscillator

There is an internal oscillator in each of the Arora □60K FPGA products. During the configuration process, it can provide a clock for the MSPI mode. The on-chip oscillator also provides a clock resource for user designs. Up to 64 clock frequencies can be obtained by setting the parameters. The following formula is employed to get the output clock frequency:

f_{out}=210MHz/Param。

Note!

“Param” is the configuration parameter. It is 3 or an even number between 2 and 126.

3 AC/DC Characteristic

Note!

You should ensure GOWINSEMI® products are always used within recommended operating conditions and range. Data beyond the working conditions and range are for reference only. GOWINSEMI® does not guarantee that all devices will operate as expected beyond the standard operating conditions and range.

3.1 Operating Conditions

3.1.1 Absolute Max. Ratings

Table 3-1 Absolute Max. Ratings

Name	Description	Min.	Max.
FPGA Logic			
V_{CC}	Core voltage, LV	-0.5V	1.05V
	Core voltage, EV	-0.5V	3.75V
V_{CCIO}	I/O Bank voltage	-0.5V	3.75V
V_{CCX}	Auxiliary voltage	-0.5V	3.75V
$V_{\_EFUSE}$	eFuse writing voltage	-0.5V	2.07V
Gigabit Transceiver			
V_{DDHA_Q*}	Analog high power supply	-0.5V	1.98V
V_{DDA_Q*}	Analog core power supply	-0.5V	1.05V
V_{DDT_Q*}	TX power supply	-0.5V	1.05V
V_{DDD_Q*}	Digital power supply	-0.5V	1.05V
MIPI			
V_{DDA_MIPI}	Analog core power supply	-0.5V	1.05V
V_{DDX_MIPI}	Analog auxiliary voltage power supply	-0.5V	3.75V
V_{DDD_MIPI}	Digital power supply	-0.5V	1.05V
V_{DD12_MIPI}	MIPI LP power supply	-0.5V	1.32V
ADC			
V_{CC_ADC}	ADC power supply	-0.5V	2.07V

Name	Description	Min.	Max.
Temperature			
Storage Temperature	Storage Temperature	-65 ℃	+150℃
Junction Temperature	Junction Temperature	-40 ℃	+125℃

3.1.2 Recommended Operating Conditions

Table 3-2 Recommended Operating Conditions

Name	Description	Min.	Max.
FPGA Logic			
V_{CC}	Core voltage, LV	0.855V	1.03V
	Core voltage, EV	1.14V	1.8V
V_{CCIO}	I/O Bank voltage	1V	3.465V
V_{CCX}[1]	Auxiliary voltage	1.71V	3.465V
$V_{\_EFUSE}$ [2]	eFuse writing voltage	1.62V	1.98V
Gigabit Transceiver			
V_{DDHA_Q*}	Analog high power supply	1.71V	1.89V
V_{DDA_Q*}	Analog core power supply	0.87V	1.03V
V_{DDT_Q*}	TX power supply	0.87V	1.03V
V_{DDD_Q*}	Digital power supply	0.87V	1.03V
MIPI			
V_{DDA_MIPI}	Analog core power supply	0.87V	1.03V
V_{DDX_MIPI}	Analog auxiliary voltage power supply	1.71V	3.465V
V_{DDD_MIPI}	Digital power supply	0.87V	1.03V
V_{DD12_MIPI}	MIPI LP power supply	1.14V	1.32V
ADC			
V_{CC_ADC}	ADC power supply	1.62V	1.98V
Temperature			
T_{JCOM}	Junction temperature Commercial operation	0℃	+85℃
T_{JIND}	Junction temperature Industrial operation	-40℃	+100℃

Note！

- [1] When internal differential termination resistors are required, Vccx must be greater than or equal to 3V; the IO input-output Fmax is limited when Vccx=1.8V, and Vccx needs to be greater than or equal to 2.5V for input-output applications with Fmax greater than 600Mbps.
- [2] When V_{EFUSE} is not required, this power supply can be connected to either GND or floating.
- If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.

3.1.3 Power Supply Ramp Rates

Table 3-3 Power Supply Ramp Rates

Name	Description	Min.	Typ.	Max.
V_{CC} Ramp	Power supply ramp rates	0.1mV/μs	TBD	15mV/μs

3.1.4 Hot Socket Specifications

Table 3-4 Hot Socket Specifications

Name	Description	Condition	I/O	Max.
I_{HS}	Input or I/O leakage current	$V_{IN}=V_{IL}$ (MAX)	I/O	150uA
I_{HS}	Input or I/O leakage current	$V_{IN}=V_{IL}$ (MAX)	TDI, TDO, TMS,TCK	120uA

3.1.5 POR Specifications

Table 3-5 POR Paramrters

Name	Description	Name	Typ.
POR Voltage	Power on reset voltage	V_{CC}	0.69V
		V_{CCX}	1.5V
		V_{CCIO} (Bank3/5/12)	1.05V

3.2 ESD performance

Table 3-6 GW5AT ESD - HBM

Device	HBM
GW5AT-60	HBM ≥ 2000V (GPIO) HBM ≥ 1000V (Gigabit Transceiver , MIPI C-PHY, MIPI D-PHY)
GW5A-60	HBM ≥ 2000V (GPIO) HBM ≥ 1000V (MIPI C-PHY, MIPI D-PHY)

Table 3-7 GW5AT ESD - CDM

Device	CDM
GW5AT-60	CDM≥ 500V
GW5A-60	CDM≥ 500V

3.3 DC Characteristics

3.3.1 DC Electrical Characteristics over Recommended Operating Conditions

Table 3-8 DC Electrical Characteristics over Recommended Operating Conditions

Name	Description	Condition	Min.	Typ.	Max.
I_{IL},I_{IH}	Input or I/O leakage	$V_{CCIO}<V_{IN}<V_{IH}$(MAX)	-		210uA
		$0V<V_{IN}<V_{CCIO}$	-		10uA
I_{PU}	I/O Active Pull-up Current	$0<V_{IN}<0.7V_{CCIO}$, Pull Strength=Strong	-		-400uA
		$0<VIN<0.7V_{CCIO}$, Pull Strength=Medium			-150uA
		$0<VIN<0.7V_{CCIO}$, Pull Strength=Weak			-50uA
I_{PD}	I/O Active Pull-down Current	V_{IL}(MAX)$<V_{IN}<V_{CCIO}$, Pull Strength=Strong	-		400uA
		V_{IL}(MAX)$<V_{IN}<V_{CCIO}$, Pull Strength=Medium			150uA
		V_{IL}(MAX)$<V_{IN}<V_{CCIO}$, Pull Strength=Weak			50uA
C1	I/O Capacitance			5 pF	8 pF
V_{HYST}	Hysteresis for Schmitt Trigger inputs	V_{CCIO}=3.3V, Hysteresis=ON	-	400mV	
		V_{CCIO}=2.5V, Hysteresis=ON	-	250mV	
		V_{CCIO}=1.8V, Hysteresis=ON	-	150mV	
		V_{CCIO}=1.5V, Hysteresis=ON	-	130mV	
		V_{CCIO}=1.2V, Hysteresis=ON		40mV	

3.3.2 Static Current

Table 3-9 Static Current

Name	Description	LV/UV	Typ.[1]
I_{CC}	Core Current	LV version	80 mA
I_{CCX}	V_{CCX} current (V_{CCX}=2.5V)	LV version	5 mA
I_{CCIO}	I/O Bank voltage (V_{CCIO}=2.5V)	LV version	1 mA

Note!

[1] The test condition for the typical value is 25℃.

3.3.3 Recommended I/O Operating Conditions

Table 3-10 I/O Operating Conditions Recommended

Name	Output V_{CCIO} (V)			Input V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVTTL33	3.135	3.3	3.465	-	-	-
LVCMOS33	3.135	3.3	3.465	-	-	-
LVCMOS25	2.375	2.5	2.625	-	-	-
LVCMOS18	1.71	1.8	1.89	-	-	-
LVCMOS15	1.425	1.5	1.575	-	-	-
LVCMOS12	1.14	1.2	1.26	-	-	-
SSTL15	1.425	1.5	1.575	0.68	0.75	0.9
SSTL18_I	1.71	1.8	1.89	0.833	0.9	0.969
SSTL18_II	1.71	1.8	1.89	0.833	0.9	0.969
SSTL25_I	2.375	2.5	2.645	1.15	1.25	1.35
SSTL25_II	2.375	2.5	2.645	1.15	1.25	1.35
SSTL33_I	3.135	3.3	3.465	1.3	1.5	1.7
SSTL33_II	3.135	3.3	3.465	1.3	1.5	1.7
HSTL18_I	1.71	1.8	1.89	0.816	0.9	1.08
HSTL18_II	1.71	1.8	1.89	0.816	0.9	1.08
HSTL15	1.425	1.5	1.575	0.68	0.75	0.9
PCI33	3.135	3.3	3.465	-	-	-
LVPECL33E	3.135	3.3	3.465	-	-	-
MLVDS25E	2.375	2.5	2.625	-	-	-
BLVDS25E	2.375	2.5	2.625	-	-	-
RSDS25E	2.375	2.5	2.625	-	-	-
LVDS25E[1]	2.375	2.5	2.625	-	-	-
SSTL15D	1.425	1.5	1.575	-	-	-
SSTL18D_I	1.71	1.8	1.89	-	-	-
SSTL18D_II	1.71	1.8	1.89	-	-	-
SSTL25D_I	2.375	2.5	2.625	-	-	-
SSTL25D_II	2.375	2.5	2.625	-	-	-
SSTL33D_I	3.135	3.3	3.465	-	-	-
SSTL33D_II	3.135	3.3	3.465	-	-	-
HSTL15D	1.425	1.575	1.89	-	-	-
HSTL18D_I	1.71	1.8	1.89	-	-	-
HSTL18D_II	1.71	1.8	1.89	-	-	-

Note!

V_{CCIO} of Banks with True LVDS is recommended to be set to 2.5 V.

3.3.4 Single ended I/O DC Characteristic

Table 3-11 Single-ended I/O DC Characteristic

Name	V_{IL}		V_{IH}		V_{OL} (Max)	V_{OH} (Min)	I_{OL}[1] (mA)	I_{OH}[1] (mA)
	Min	Max	Min	Max				
LVCMOS33 LVTTL33	-0.3V	0.8V	2.0V	3.45V	0.4V	V_{CCIO}-0.4V	2	-2
							4	-4
							6	-6
							8	-8
							12	-12
							16	-16
					0.2V	V_{CCIO}-0.2V	0.1	-0.1
LVCMOS25	-0.3V	0.7V	1.7V	V_{CCIO}+0.3	0.4V	V_{CCIO}-0.4V	2	-2
							4	-4
							6	-6
							8	-8
							12	-12
							16	-16
					0.2V	V_{CCIO}-0.2V	0.1	-0.1
LVCMOS18	-0.3V	0.35 x V_{CCIO}	0.65 x V_{CCIO}	V_{CCIO}+0.3	0.4V	V_{CCIO}-0.4V	2	-2
							4	-4
							6	-6
							8	-8
							12	-12
							16	-16
					0.2V	V_{CCIO}-0.2V	0.1	-0.1
LVCMOS15	-0.3V	0.35 x V_{CCIO}	0.65 x V_{CCIO}	V_{CCIO}+0.3	0.4V	V_{CCIO}-0.4V	2	-2
							4	-4
							6	-6
							8	-8
							12	-12
					0.2V	V_{CCIO}-0.2V	0.1	-0.1
LVCMOS12	-0.3V	0.35 x V_{CCIO}	0.65 x V_{CCIO}	V_{CCIO}+0.3	0.4V	V_{CCIO}-0.4V	2	-2
							4	-4
							6	-6
							8	-8
					0.2V	V_{CCIO}-0.2V	0.1	-0.1
LVCMOS10	-0.3	0.35 x V_{CCIO}	0.65 x V_{CCIO}	1.1V	0.4V	V_{CCIO}-0.4V	2	-2
							4	-4

Name	V_{IL}		V_{IH}		V_{OL} (Max)	V_{OH} (Min)	I_{OL}[1] (mA)	I_{OH}[1] (mA)
	Min	Max	Min	Max				
PCI33	-0.3V	0.3 x V_{CCO}	0.5 x V_{CCO}	V_{CCO}+0.3	0.1x V_{CCO}	0.9 x V_{CCO}	1.5	-0.5
SSTL33_I	-0.3V	V_{REF}-0.2V	V_{REF}+0.2V	V_{CCO}+0.3	V_{CCO}/2-0.6	V_{CCO}/2+0.6	8	-8
SSTL33_II	-0.3V	V_{REF}-0.2V	V_{REF}+0.2V	V_{CCO}+0.3	V_{CCO}/2-0.8	V_{CCO}/2+0.8	13.4	-13.4
SSTL25_I	-0.3V	V_{REF}-0.15V	V_{REF}+0.15V	V_{CCO}+0.3	V_{CCO}/2-0.61	V_{CCO}/2+0.61	8	-8
SSTL25_II	-0.3V	V_{REF}-0.15V	V_{REF}+0.15V	V_{CCO}+0.3	V_{CCO}/2-0.81	V_{CCO}/2+0.81	13.4	-13.4
SSTL18_I	-0.3V	V_{REF}-0.125V	V_{REF}+0.125 V	V_{CCO}+0.3	V_{CCO}/2-0.47	V_{CCO}/2+0.47	8	-8
SSTL18_II	-0.3V	V_{REF}-0.125V	V_{REF}+0.125 V	V_{CCO}+0.3	V_{CCO}/2-0.6	V_{CCO}/2+0.6	13.4	-13.4
SSTL15_I	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	V_{CCO}+0.3	V_{CCO}/2-0.175	V_{CCO}/2+0.175	8	-8
SSTL135_I	-0.3	V_{REF}-0.09V	V_{REF}+0.09V	V_{CCO}+0.3	V_{CCO}/2-0.15	V_{CCO}/2+0.15	8	-8
SSTL12_I	-0.3	V_{REF}-0.1V	V_{REF}+0.1V	V_{CCO}+0.3	0.2 x V_{CCO}	0.8 x V_{CCO}	0.1	-0.1
HSTL18_I	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	V_{CCO}+0.3	0.40V	V_{CCO}-0.40V	8	-8
HSTL18_II	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	V_{CCO}+0.3	0.40V	V_{CCO}-0.40V	16	-16
HSTL15_I	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	V_{CCO}+0.3	0.40V	V_{CCO}-0.40V	8	-8
HSTL15_II	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	V_{CCO}+0.3	0.40V	V_{CCO}-0.40V	8	-8
HSTL12_I	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	V_{CCO}+0.3	0.2 x V_{CCO}	0.8 x V_{CCO}	8	-8
HSUL12	-0.3	V_{REF}-0.13V	V_{REF}+ 0.13V	V_{CCO}+0.3	0.2 x V_{CCO}	0.8 x V_{CCO}	0.1	-0.1

Note!

[1] The total DC current limit (sourced and sinked) of all IOs in the same bank: the total DC current of all IOs in the same bank shall not be greater than n*8mA, where n represents the number of IOs bonded out from a bank.

3.3.5 Differential I/O DC Characteristic

Table 3-12 Differential I/O DC Characteristic

Name	Description	Conditions	Min.	Typ.	Max.	Unit
V_{ICM}	Input Common Mode Voltage	Half the Sum of the Two Inputs	0.05		2.35	V
V_{ID}	Differential Input Threshold	Difference Between the Two Inputs	±100	±350	±600	mV
I_{IN}	Input Current	Power On or Power Off			20	μA
V_{OD}	Output Voltage Differential	(V_{OP} - V_{OM}), R_T = 100Ω	250	350	600	mV
ΔV_{OD}	Change in VOD Between High and Low				50	mV
V_{OS}	Output Voltage Offset	(V_{OP} + V_{OM})/2, R_T = 100Ω	1.000	1.250	1.425	V
ΔV_{OS}	Change in VOS Between High and Low				50	mV
I_S	Short-circuit current	V_{OD} = 0V output short-circuit			12	mA

3.4 AC Switching Characteristics

3.4.1 Gearbox Switching Characteristics

Table 3-13 Gearbox Timing Parameters

Name	Description	Max.	Unit
FMAXIDDR	1:2 Gearbox maximum serial input rate	400	Mbps
$FMAX_{IDES4}$	1:4 Gearbox IO maximum input frequency	800	Mbps
$FMAX_{IDESx}$	1:8 / 1:10 Gearbox maximum serial input rate	2000	Mbps
$FMAX_{IDES14}$	1:14 Gearbox maximum serial input rate	2000	Mbps
$FMAX_{IDES16}$	1:16 Gearbox IO maximum input frequency	2000	Mbps
$FMAX_{IDES32}$	1:32 Gearbox IO maximum input frequency	2000	Mbps
$FMAX_{ODDR}$	2:1 Gearbox maximum serial output rate	400	Mbps
$FMAX_{OSER4}$	4:1 Gearbox maximum serial output rate	800	Mbps
$FMAX_{OSERx}$	8:1/10:1 Gearbox maximum serial output rate	2000	Mbps
$FMAX_{OSERx}$	8:1/10:1 Gearbox maximum serial output rate	2000	Mbps
$FMAX_{OSER16}$	16:1 Gearbox maximum serial output rate	2000	Mbps

3.4.2 On chip Oscillator Switching Characteristics

Table 3-14On chip Oscillator Switching Characteristics

Name	Description	Min.	Typ.	Max.
f_{MAX}	Output Frequency (0 to + 85° C)	199.5 MHz	210 MHz	220.5 MHz
	Output Frequency (-40 to +100° C)	189 MHz	210 MHz	231 MHz
t_{DT}	Output Clock Duty Cycle	-	50%	-

3.4.3 PLL Switching Characteristics

Table 3-15 PLL Switching Characteristic

Parameter	Description	Speed Grade		Unit	Note
		-1	-2		
F_{INMAX}	Maximum Input Clock Frequency	800	800	MHz	
F_{INMIN}	Minimum Input Clock Frequency	19	19	MHz	
F_{PFDMAX}	Maximum Frequency at the Phase Frequency Detector	400	400	MHz	
F_{PFDMIN}	Minimum Frequency at the Phase Frequency Detector	19	19	MHz	
$F_{INJITTER}$	Maximum Input Clock Period Jitter	< 20% of clock input period or 1 ns Max			
F_{Induty}	Minimum Allowable Input Duty Cycle: 19– 49MHz	25	25	%	
	Minimum Allowable Input Duty Cycle: 50– 199MHz	30	30	%	
	Minimum Allowable Input Duty Cycle: 200– 399MHz	35	35	%	
F_{VCOMIN}	Minimum PLL VCO Frequency	800	800	MHz	
F_{VCOMAX}	Maximum PLL VCO Frequency	1600	1600	MHz	
F_{BW}	Low PLL Bandwidth at Typical	1	1	MHz	
	High PLL Bandwidth at Typical	4	4	MHz	
$T_{STATPHAOFFSET}$	Static Phase Offset of the PLL Outputs	+/- 50	+/-50	ps	
$T_{JITTER\_CCJ\_HCLK}$	PLL Output cycle-cycle Jitter Thru HCLK≥100MHz	<300	<300	ps	3
	PLL Output cycle-cycle Jitter Thru HCLK <100MHz	<30	<30	MUI	
	PLL Output cycle-cycle Jitter Thru PCLK ≥ 100MHz	<400	<400	ps	
	PLL Output cycle-cycle Jitter Thru PCLK <100MHz	<40	<40	MUI	
$T_{JITTER\_PJ\_PCLK}$	PLL Output period Jitter Thru HCLK ≥ 100MHz	<300	<300	ps	
	PLL Output period Jitter Thru HCLK < 100MHz	<30	<30	MUI	
	PLL Output period Jitter Thru PCLK ≥ 100MHz	<400	<400	ps	
	PLL Output period Jitter Thru PCLK < 100MHz	<40	<40	MUI	
$T_{OUTDUTY}$	PLL Output Clock Duty Cycle Precision	<50	<50	MUI	1.4
$T_{LOCKMAX}$	PLL Maximum Lock Time	1	1	ms	
F_{OUTMAX}	PLL Maximum Output Frequency	800	800	MHz	
F_{OUTMIN}	PLL Minimum Output Frequency	6.25	6.25	MHz	2
$T_{EXTFDVAR}$	External Clock Feedback Variation	< 20% of clock input period or 1 ns Max			
$RST_{MINPULSE}$	Minimum Reset Pulse Width	10	10	ns	

Note!

- This test data is derived from integer frequency divider outputs.
- In Cascade mode, multiple dividers can be serially connected to achieve a reduced output frequency.

- The level of output jitter correlates with the input source; this dataset is based on a low-jitter crystal as the source.
- The observed duty cycle on IOs is influenced by the Clock Tree.

3.5 Gigabit Transceiver

3.5.1 Gigabit Transceiver DC Specifications

Table 3-16 Gigabit Transceiver DC Specifications

Name	Description	Condition	Min.	Typ.	Max.	Units
$VOUT_{diff\_p2p}$	Differential peak-to-peak output voltage	Transmitter output swing is set to maximum setting	–	–	V_{dda}	mV
$VOUT_{cm}$	DC common mode output voltage	Equation based		$V_{dda}/2$		mV
R_{src_term}	Differential output resistance		–	100	–	Ω
$T_{intrapairskew}$	Transmitter output pair (TXP and TXN) intra-pair skew		–	2	12	ps
VIN_{diff_p2p}	Differential peak-to-peak input voltage (external AC coupled)		200	–	2000	mV
VIN	Absolute input voltage	DC coupled VDDT = 0.9V	–300	–	V_{dda}	mV
VIN_{CM}	Common mode input voltage	DC coupled VDDT = 0.9V	–	–	500	mV
R_{Term}	Differential input resistance		–	100	–	Ω
C_{EXT}	Recommended external AC coupling capacitor		–	100	–	nF

3.5.2 Gigabit Transceiver Switching Characteristics

Table 3-17 Transmitter and Receiver Data Rate Perfromance

Name/Description	Condition	C1		C2		Unit
		Flip Chip	Wire Bond	Flip Chip	Wire Bond	
On board application(chip to chip)[1]	Max. data rate (typical Voltage)	10.3125	8	12.5	8	Gbps
	Min. data rate[3]	270	270	270	270	Mbps
Backplane[2]	Max. data rate (typical Voltage)	8	8	8	8	Gbps
	Min. data rate[4]	270	270	270	270	Mbps

Note!

- [1] Less channel loss for chip-chip applications.

- [2] For backplance applications, the maximum channel loss should be within PCIE 3.0 standard.
- [3] [4] The oversampling logic should be enabled.

Table 3-18 PLL Performance

Name/Description	Condition	C1 / C2		Unit
		Min	Max	
Channel PLL	Recommended Operating Conditions	1.25	6.5	GHz
Quad PLL 0	Recommended Operating Conditions	1.25	6.5	GHz
Quad PLL 1	Recommended Operating Conditions	3.8	6.5	GHz
Output lane divider[1]	1/2/4/8			

Note!

[1] Lower rates can be achieved by using an output lane divider.

Table 3-19 Reference Clock Switching Characteristics

Name	Description	Condition	C0 / C1 / C2			Units
			Min.	Typ.	Max.	
$F_{GREFCLK}$	Reference clock frequency range		20	–	800	MHz
$T_{RREFCLK}$	Reference clock rise time	20% – 80%	–	200	–	ps
$T_{FREFCLK}$	Reference clock fall time	80% – 20%	–	200	–	ps
$T_{DCREFCLK}$	Reference clock duty cycle	Transceiver PLL only	40	50	60	%

Table 3-20 PLL Lock Time Adaptation

Name	Description	C0 / C1 / C2			Units
		Min.	Typ.	Max.	
$T_{GPLLLOCK}$	Initial PLL lock	–	–	2	ms

3.6 Configuration Interface Timing Specification

Arora V 60K FPGA Products support multiple GowinCONFIG modes: SSPI, MSPI, Master CPU, Slave CPU, Master SERIAL, Slave SERIAL and PCIe. For further detailed information, please refer to *UG718E, Arora V 60K FPGA Products Programming and Configuration Guide*.

4 Ordering Information

4.1 Part Name

Figure 4-1 Part Naming Examples–ES

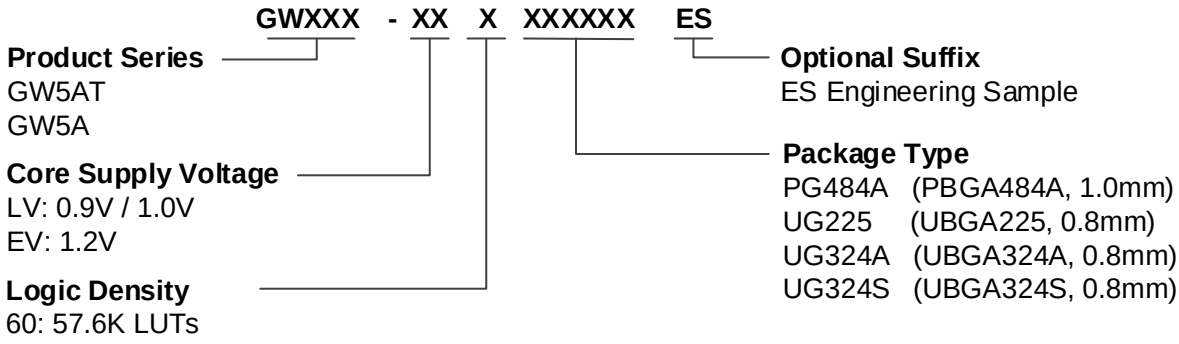
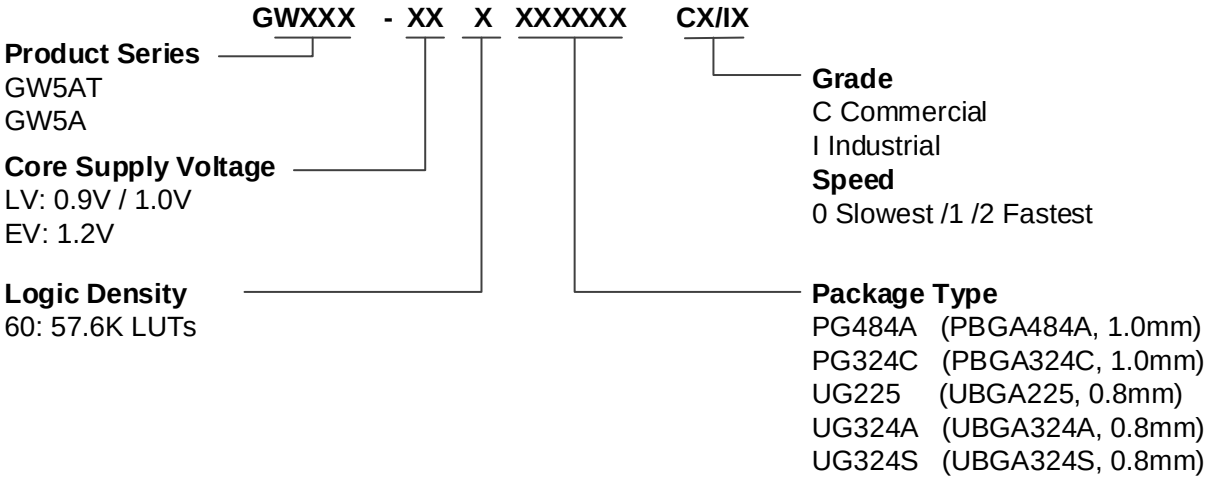


Figure 4-2 Part Naming Examples–Production



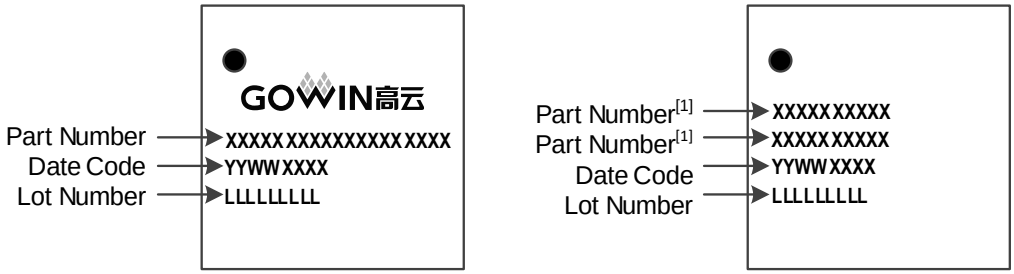
Note!

- For the further detailed information about the package information, please refer to 1.2General Description.
- The LittleBee family devices and Arora family devices of the same speed grade have different speeds.
- Both “C” and “I” are used in GOWIN part name marking for one device, such as C2/I1, C1/I0, etc. GOWIN devices are screened using industrial standards, so one same device can be used for both industrial (I) and commercial (C) applications. The maximum temperature of the industrial grade is 100℃, and the maximum temperature of the commercial grade is 85℃. Therefore, if the same chip meets the speed grade 2 in the commercial grade application, the speed grade is 1 in the industrial grade application.

4.2 Package Mark

The device information of GOWINSEMI is marked on the chip surface, as shown in Figure 4-3.

Figure 4-3 Package Mark Examples



Note!

[1] The first two lines in the right figure above are the “Part Number”.

5 About This Guide

5.1 Purpose

This data sheet describes the features, product resources, structure, AC/DC characteristics, and the ordering information of the Arora V 60K of FPGA products, making it easier for users to understand the Arora V 60K FPGA products, which will help in the selection and usage of the device.

5.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- UG718, Arora V 60K FPGA Products Programming and Configuration User Guide
- UG984, GW5AT & GW5AST series of FPGA Products Schematic Manual
- UG1222, GW5AT-60 Pinout
- UG1229, GW5A-60 Pinout

5.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 5-1.

Table 5-1 Terminology and Abbreviations

Terminology and Abbreviations	Full Name
ADC	Analog to Digital Converter
AER	Advanced Error Reporting
ALP	Adaptive Low Power
ALU	Arithmetic Logic Unit
BSRAM	Block Static Random Access Memory
CFU	Configurable Function Unit

Terminology and Abbreviations	Full Name
CLS	Configurable Logic Section
CMSER	Configuration Memory Soft Error Recovery
CRU	Configurable Routing Unit
CSI	Camera Serial Interface
CTC	Clock Tolerance Compensation
CTLE	Continuous Time Linear Equalizer
DCS	Dynamic Clock Selector
DFF	D Flip-floor
DNA	Device Identifier
DNL	Differential Non-Linearity
DP	True Dual Port 16K BSRAM
DSI	Display Serial Interface
DSP	Digital Signal Processing
ECC	Error Correction Code
ECRC	End-to-End Cyclic Redundancy Check
ESD	Electro-Static Discharge
FIFO	First In First Out
FPG	FCPBGA
FPGAs	Field Programmable Gate Array
GCLK	Global Clock
GPIO	Gowin Programmable IO
GSR	Global Set/Reset
HCLK	High Speed Clock
INL	Integral Non-Linearity
IOB	Input/Output Block
LUT	Look-up Table
LW	Long Wire
mDRP	Mini Dynamic Re-Program Port
MIPI	Mobile Industry Processor Interface
OTP	One Time Programmable
PCIe	Peripheral Component Interface Express
PCS	Physical Coding Sublayer
PLL	Phase-locked Loop
PMA	Physical Medium Attachment Sublayer
REG	Register
SDP	Semi-Dual Port 16K BSRAM
SEU	Single Event Upset
SP	Single Port 16K BSRAM

Terminology and Abbreviations	Full Name
SSRAM	Shadow Static Random Access Memory
TDM	Time Division Multiplexing

5.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com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