Arora V FPGA Products Overview

GOWINSEMI Arora V FPGA products are the 5th-generation of Arora family. It adopts advanced 22nm SRAM technology, integrates 12.5Gbps high-speed SerDes interface, PCIe hard core, MIPI D-PHY and C-PHY hard core, the latest generation of embedded ARM® core processor Cortex-M4 / RiscV AE350_SOC, PSRAM and NOR FLASH memory chips, supports DDR3 interface, and is available in various pin packages for low-power, high-performance and compatibility design applications.

Arora V FPGA products currently include GW5A Series, GW5AT Series, GW5AS Series, GW5AST Series, GW5AR Series, GW5ART Series, GW5ANT Series and GW5ANRT Series, covering 15K, 25K, 45K, 60K, 75K and 138K LUT device products.

- GW5A Series: Supports MIPI D-PHY hard cores and currently includes 25K, 60K and 138K LUT devices.
- GW5AT Series: 12.5Gbps SERDES with support for multiple protocols, PCIe hard core, MIPI D-PHY, and C-PHY hard core. Currently includes 15K, 60K, 75K and 138K LUT devices.
- GW5AS series: GW5AS-25 integrates the latest generation of embedded ARM® core Processor Cortex-M4 and MIPI D-PHY hard core. GW5AS-138 integrates the RiscVAE350_SOC hard core processor and the MIPI D-PHY hard core.
- GW5AST Series: Integrates the RiscVAE350_SOC hard core processor, 12.5Gbps SERDES with support for multiple protocols, PCIe hard, and MIPI D-PHY hard cores. 138K LUT devices are currently supported.
- GW5AR Series: Supports MIPI D-PHY hard core and PSRAM memory chips. 25K LUT devices are currently supported.
- GW5ART Series: 12.5Gbps SERDES with support for multiple protocols, PCIe hard core, MIPI D-PHY and C-PHY hard core and PSRAM storage chip. 15K LUT devices are currently supported.
- GW5ANT Series: 12.5Gbps SERDES with support for multiple protocols, PCIe hard core, MIPI D-PHY and C-PHY hard core, and NOR FLASH storage chip. 15K LUT devices are currently supported.
- GW5ANRT Series: 12.5Gbps SERDES with support for multiple

protocols, PCIe hard core, MIPI D-PHY and C-PHY hard core, PSRAM storage chip, and NOR FLASH storage chip. 15K LUT devices are currently supported.

GOWINSEMI provides a new generation of FPGA hardware development environment that supports FPGA placement & routing, bitstream generation and download, etc.

For more details about the Arora V FPGA products, please refer to the datasheets as below:

- DS981, Arora V 138K& 75K of FPGA Products Data Sheet
- DS1225, Arora V 60K FPGA Products Data User Guide
- DS1103, Arora V 25K FPGA Products Data User Guide
- DS1118, Arora V 15K FPGA Products Data User Guide

Features

- Adopts advanced 22nm SRAM technology, supports 0.9 V / 1.0 V / 1.2 V core power supply
- Up to 138K LUT4s, supports shadow SRAMs
- Block SRAMs with multiple modes, up to 36Kbits per BSRAM
- High performance DSP blocks with a new architecture, supports 27 x 18, 12 x 12, 27 x 36 multiplier and 48-bit accumulator
- Supports multiple transmission protocols such as 270 Mbps to 12.5G bps custom SERDES protocols and 10G Ethernet, etc.
- Dedicated PCIe hard core, Compliant to the PCI Express Base Specification 3.0
- Supports MIPI D-PHY and C-PHY hardcore
- Integrates the latest generation of embedded ARM® core Processor Cortex-M4/ Integrates RiscV AE350_SOC
- Integrates PSRAM and NOR PSRAM memory chip
- Integrates nnew and flexible X-channel oversampling ADC with high accuracy, SARADC and ADC sensor
- Supports various SDRAM interfaces, up to DDR3 1333 Mb/s
- Multiple I/O standards
- Supports GCLK, PLL, HCLK, DDR memory interface, and DQS, etc.
- Supports multiple configuration modes, background programming, datastream file encryption and security bit setting, SEU detection check function, and OTP
- Available in a variety of pin packages, all in a lead-free process

Product Resources and Package Information

GW5A series

Table 1 GW5A series of FPGA Products Information List

Device	GW5A-25	GW5A-60	GW5A-138
LUT4	23040	59904	138240
Flip-Flop (REG)	23040	59904	138240
Shadow Static Random Access Memory SSRAM(Kb)	180	468	1080
Block Static Random Access Memory BSRAM(Kb)	1008	2124	6120
Number of BSRAMs BSRAM	56	118	340
DSP（27-bit x 18-bit）	28	118	298
Maximum phase locked loop[1](PLLs)	6	8	12
Global Clocks	16	16	16
High-speed Clocks	16	20	24
LVDS Gbps	1.25	1.25	1.25
DDR3 Mbps	1066	1333	1333
MIPI DPHY hard core	2.5Gbps (RX/TX), 4 data lanes 1 clock lanes	2.5Gbps (RX/TX), 4 data lanes 1 clock lanes	2.5Gbps (RX) 8 data lanes 2 clock lanes
MIPI C-PHY Hardcore	-	2.5Gsps (=5.75Gbps,RX/TX), 3-trios data lanes	-
ADC	1	2	2
Number of GPIO banks	8[2]	11	6
Maximum number of GPIOs	239	320	312
Core voltage	0.9V/1.0V/1.2V[3]	0.9V/1.0V/1.2V [3]	0.9V/1.0V

Note!

- [1] Different packages support different numbers of PLLs, and here is the max. number.
- [2] In addition to GPIO Banks, there is one JTAG Bank wiht four I/Os and one Config Bank with one I/O.
- [3] The EV version has a built-in LDO and supports 1.2V V_{CC}.

Table 2 GW5A-25 Package Information

Package	Pitch (mm)	Size (mm)	GW5A-25	
			I/O (True LVDS Pair)	MIPI D- PHY Hardcore
LQ100	0.5	14 x 14	80 (36)	–
LQ144	0.5	20 x 20	109 (50)	–
MG121N	0.5	6 x 6	82 (36)	RX/TX, Configurable 4 data lanes 1 clock lanes
MG196S	0.5	8 x 8	114 (53)	–
PG196S	1.0	15 x 15	110 (48)	RX/TX, Configurable 4 data lanes 1 clock lanes
PG256C	1.0	17 x 17	191 (90)	–
PG256	1.0	17 x 17	184 (88)	RX/TX, Configurable 4 data lanes 1 clock lanes
PG256S	1.0	17 x 17	194 (93)	–
UG225S	0.8	13 x 13	168 (80)	–
UG256C	0.8	14 x 14	191 (90)	–
UG324	0.8	15 x 15	222 (104)	RX/TX, Configurable 4 data lanes 1 clock lanes
UG324F	0.8	15 x 15	223 (108)	RX/TX, Configurable 4 data lanes 1 clock lanes
UG324S	0.8	15 x 15	239 (116)	–

Table 3 GW5A-60 Package Information

Package			Pitch (mm)	Size (mm)	GW5A-60		
Name	Type	Description			User I/O (True LVDS Pair)	MIPI D- PHY Hardcore	MIPI C-PHY Hardcore
UG324A	UBGA	Wire Bond	0.8	15x15	222(106)	–	–
UG324S	UBGA	Wire Bond	0.8	15x15	226(110)	–	–

Table 4 GW5A-138 Package Information

Package	Pitch (mm)	Size (mm)	GW5A-138	
			I/O (True LVDS Pair)	MIPI D- PHY Hardcore
UG324A	0.8	15 x 15	221 (106)	-–

GW5AT series

Table 5 GW5AT series of FPGA Products Information List

Device	GW5AT-15	GW5AT-60	GW5AT-75	GW5AT-138
LUT4	15120	59904	86688	138240
Flip-Flop (REG)	15120	59904	86688	138240
Distributed Static Random Access Memory SSRAM(Kb)	118.125	468	677	1080
Block Static Random Access Memory BSRAM(Kb)	630	2124[4]	4608	6120
Number of BSRAMs BSRAM	35	118[4]	256	340
DSP（27-bit x 18-bit）	28	118	213	298
DSP Lite	12	-	-	-
Maximum phase locked loop[1](PLLs)	2	8	12	12
Global Clocks	16	16	16	16
High-speed Clocks	2	20	24	24
TransceiVers[2]	4	4	8	8
TransceiVers Rate	270Mbps - 12.5Gbps	270Mbps - 12.5Gbps	270Mbps - 12.5Gbps	270Mbps - 12.5Gbps
PCIe 3.0	1, x1, x2, x4 PCIe 3.0	1, x1, x2, x4 PCIe 3.0	1, x1, x2, x4, x8 PCIe 3.0	1, x1, x2, x4, x8 PCIe 3.0
LVDS Gbps	1.25	1.25	1.25	1.25
DDR3 Mbps	–	1333	1333	1333
MIPI D-PHY hardcore	2.5Gbps (RX/TX), 4 data lanes 1 clock lanes	2.5Gbps (RX/TX), 4 data lanes 1 clock lanes	2.5Gbps (RX) 8 data lanes 2 clock lanes	2.5Gbps (RX) 8 data lanes 2 clock lanes
MIPI C-PHY Hardcore	2.5Gsps (=5.75Gbps,RX/TX), 3-trios data lanes	2.5Gsps (=5.75Gbps,RX/TX), 3-trios data lanes	-	-
ADC	1	2	2	2
Number of GPIO banks	4	11	6	6
Maximum number of GPIOs[5]	53	320	312	312
Core voltage	0.9V/1.0V[6]	0.9V/1.0V/1.2V [3]	0.9V/1.0V[6]	0.9V/1.0V[6]

Note!

- [1] Different packages support different numbers of PLLs, and here is the max. number.
- [2] Different packages support different number of Transceivers, and here is the max. number.
- [3] The EV version has a built-in LDO and supports 1.2V V_{CC}.
- [4] The GW5AT-60 ES version supports 72 BSRAM with a capacity of 1296Kb.

- [5] This is the max. number of GPIOs that the device can provide without package limitation. Please refer to Table 6, Table 7, Table 8 and Table 9 for the maximum number of user I/O available in specific packages.
- [6] It is recommended to use 0.9V for Vcc, 1.0V tends to increase power consumption.

Table 6 GW5AT-138 Package Information

Package			Pitch (mm)	Size (mm)	GW5AT-138		
Name	Type	Description			I/O (True LVDS Pair)	Transceiv-ers[1]	MIPI D- PHY Hardcore
FPG676A	FCPBGA	Flip Chip	1.0	27 x 27	311 (150)	8	RX 8 data lanes 2 clock lanes
PG676A	PBGA	Wire Bond	1.0	27 x 27	311 (150)	8	RX 8 data lanes 2 clock lanes
PG484A	PBGA	Wire Bond	1.0	23 x 23	291 (143)	4	–
PG484	PBGA	Wire Bond	1.0	23 x 23	271 (133)	4	RX 8 data lanes 2 clock lanes
UG324A	UBGA	Wire Bond	0.8	15x15	141(68)	4	RX 8 data lanes 2 clock lanes

Note!

- [1] Transceivers in the PBGA package can reach speeds up to 10.3125 Gbps, and when the rate exceeds 8 Gbps, only on-board interconnects are supported, not backplane applications.
- [1] Transceivers in the FCPBGA package can reach speeds up to 12.5 Gbps.

Table 7 GW5AT-75 Package Information

Package			Pitch (mm)	Size (mm)	GW5AT-75		
Name	Type	Description			I/O (True LVDS Pair)	Transceiv-ers[1]	MIPI D- PHY Hardcore
UG484	UBGA	Wire Bond	0.8	19x19	311(150)	8	RX 8 data lanes 2 clock lanes

Note!

[1] Transceivers in the UBGA package can reach speeds up to 10.3125 Gbps, and when the rate exceeds 8 Gbps, only on-board interconnects are supported, not backplane applications.

Table 8 GW5AT-60 Package Information

Package			Pitch (mm)	Size (mm)	GW5AT-60			
Name	Type	Description			I/O (True LVDS Pair)	Transceivers[1]	MIPI D- PHY Hardcore	MIPI C-PHY Hardcore
PG484A	PBGA	Wire Bond	1.0	23x23	297(143)	4	–	–
UG225	UBGA	Wire Bond	0.8	13x13	113(53)	4	RX/TX 4 data lanes 1 clock lanes	RX/TX 3-trios data lanes
UG324S	UBGA	Wire Bond	0.8	15x15	198(98)	4	–	–

Note!

[1] Transceivers in the UBGA package can reach speeds up to 10.3125 Gbps, and when the rate exceeds 8 Gbps, only on-board interconnects are supported, not backplane applications.

Table 9 GW5AT-15 Package Information

Package			Pitch (mm)	Size (mm)	GW5AT-15			
Name	Type	Desc-ription			I/O (True LVDS Pair)	Transce-ivers[1]	MIPI D- PHY Hardcore	MIPI C-PHY Hardcore
MG132	MBGA	Wire Bond	0.5	8 x 8	53(25)	4	RX/TX 4 data lanes 1 clock lanes	RX/TX 3-trios data lanes

Note!

[1] Transceivers in the MBGA package can reach speeds up to 10.3125 Gbps, and when the rate exceeds 8 Gbps, only on-board interconnects are supported, not backplane applications.

GW5AS series

Table 10 GW5AS series of FPGA Products Information List

Device	GW5AS-25	GW5AS-138
LUT4	23040	138240
Flip-Flop (REG)	23040	138240
Shadow Static Random Access Memory SSRAM(Kb)	180	1080
Block Static Random Access Memory BSRAM(Kb)	1008	6120
Number of BSRAMs BSRAM	56	340
Flash (bits)	1 M	–
Hard core processor	Cortex-M4	RiscV AE350_SOC
DSP（27-bit x 18-bit）	28	298
Maximum phase locked loop[1](PLLs)	6	12
Global Clocks	16	16
High-speed Clocks	16	24
LVDS Gbps	1.25	1.25
DDR3 Mbps	1066	1333
MIPI DPHY hard core	2.5Gbps (Rx/Tx), 4 data lanes 1 clock lanes	2.5Gbps (RX) 8 data lanes 2 clock lanes
ADC[2]	FPGA: 1 Cortex-M4: 3	2
Number of GPIO banks	8[3]	6
Maximum number of I/Os	239	312
Core voltage	0.9V/1.0V/1.2V[4]	0.9V/1.0V

Note!

- [1] Different packages support different numbers of PLLs, and here is the max. number.
- [2] In the GW5AS-25 device, 1 ADC is embedded in the FPGA and 3 ADCs are embedded in the Cortex-M4 `system`.
- [3] In addition to GPIO Banks, there is one JTAG Bank wiht four I/Os and one Config Bank with one I/O.
- [4] The EV version of the GW5AS-25 device has a built-in LDO and can support 1.2V VCC.

Table 11 GW5AS-25 Package Information

Package			Pitch (mm)	Size (mm)	GW5AS-25	
Name	Type	Description			I/O(True LVDS Pair)	MIPI D-PHY hardcore
UG256	UBGA	Wire Bond	0.8	14x14	144 (68)	RX/TX, Configurable 4 data lanes 1 clock lanes

Table 12 GW5AS-138 Package Information

Package			Pitch (mm)	Size (mm)	GW5AS-138	
Name	Type	Description			I/O (True LVDS Pair)	MIPI D- PHY Hardcore
UG324A	UBGA	Wire Bond	0.8	15 x 15	222 (106)	—

GW5AST series

Table 13 GW5AST of FPGA Products Information List

Device	GW5AST-138
LUT4	138240
Flip-Flop (REG)	138240
Shadow Static Random Access Memory SSRAM(Kb)	1080
Block Static Random Access Memory BSRAM(Kb)	6120
Number of BSRAMs BSRAM	340
DSP（27-bit x 18-bit）	298
Maximum phase locked loop[1](PLLs)	12
Global Clocks	16
High-speed Clocks	24
Transceivers	8
TransceiVers Rate	270Mbps - 12.5Gbps
PCIe 3.0	1, x1, x2, x4, x8 PCIe 3.0
LVDS Gbps	1.25
DDR3 Mbps	1333
MIPI DPHY hard core	2.5Gbps (RX) 8 data lanes 2 clock lanes
Hard core processor	Risc V AE350_SOC
ADC	2
Number of GPIO banks	6
Maximum number of I/Os	312
Core voltage	0.9V/1.0V

Note!

[1] Different packages support different numbers of PLLs, and here is the max. number.

Table 14 GW5AST-138 Package Information

Package			Pitch (mm)	Size (mm)	GW5AST-138		
Name	Type	Description			I/O (True LVDS Pair)	Transceiv-ers[1]	MIPI D- PHY Hardcore
FPG676A	FCPBGA	Flip Chip	1.0	27 x 27	312 (150)	8	RX 8 data lanes 2 clock lanes
PG676A	PBGA	Wire Bond	1.0	27 x 27	312 (150)	8	RX 8 data lanes 2 clock lanes
PG484A	PBGA	Wire Bond	1.0	23 x 23	297 (143)	4	—

GW5AR series

Table 15 GW5AR of FPGA Products Information List

Device	GW5AR-25
LUT4	23040
Flip-Flop (REG)	23040
Shadow Static Random Access Memory SSRAM(Kb)	180
Block Static Random Access Memory BSRAM(Kb)	1008
Number of BSRAMs BSRAM	56
PSRAM (units)	2
Single PSRAM (bits)	8M X 8bits
DSP（27-bit x 18-bit）	28
Maximum phase locked loop[1](PLLs)	6
Global Clocks	16
High-speed Clocks	16
LVDS Gbps	1.25
DDR3 Mbps	1066
MIPI DPHY hard core	2.5Gbps (RX/TX), 4 data lanes 1 clock lanes
ADC	1
Number of GPIO banks	8[2]
Maximum number of GPIOs	239
Core voltage	0.9V/1.0V

Note!

- [1] Different packages support different numbers of PLLs, and here is the max. number.
- [2] In addition to GPIO Banks, there is one JTAG Bank wiht four I/Os and one Config Bank with one I/O.

Table 16 GW5AR series Package Information

Package	Pitch (mm)	Size (mm)	GW5AR-25	
			I/O (True LVDS Pair)	MIPI D-PHY hardcore
UG256P	0.8	14x14	178 (86)	RX/TX, Configurable 4 data lanes 1 clock lanes

GW5ART series

Table 17 GW5ART series of FPGA Products Information List

Device	GW5ART-15
LUT4	15120
Flip-Flop (REG)	15120
Shadow Static Random Access Memory SSRAM(Kb)	118.125
Block Static Random Access Memory BSRAM(Kb)	630
Number of BSRAMs BSRAM	35
PSRAM (units)	2(CM90P) 1(MG132P)
Single PSRAM (bits)	64M
DSP (27-bit x 18-bit)	28
DSP Lite	12
Maximum phase locked loop[1](PLLs)	2
Global Clocks	16
High-speed Clocks	2
Transceivers[2]	4
TransceiVers Rate	270Mbps - 12.5Gbps
PCIe3.0 Hardcore	1, x1, x2, x4 PCIe 3.0
LVDS Gbps	1.25
DDR3 Mbps	1333
MIPI D-PHY hardcore	2.5Gbps (RX/TX), 4 data lanes 1 clock lanes
MIPI C-PHY Hardcore	2.5Gsps (=5.75Gbps,RX/TX), 3-trios data lanes
ADC	1
Number of GPIO banks	4
Maximum number of GPIOs[3]	53
Core voltage	0.9V/1.0V[4]

Note!

- [1] Different packages support different numbers of PLLs, and here is the max. number.
- [2] Different packages support different number of Transceivers, and here is the max. number.
- [3] This is the max. number of GPIOs that the device can provide without package limitation. Please refer to Table 18 for the maximum number of user I/O available in specific packages.
- [4] It is recommended to use 0.9V for Vcc, 1.0V tends to increase power consumption.

Table 18 GW5ART-15 Package Information

Package			Pitch (mm)	Size (mm)	GW5ART-15			
Name	Type	Description			I/O (True LVDS Pair)	Transc-eivers[1]	MIPI D- PHY Hardcore	MIPI C-PHY Hardcore
CM90P	CM	Wire Bond	0.5	5.3 x 4.9	23(11)	4	RX/TX 4 data lanes 1 clock lanes	–
CM90PF	CM	Wire Bond	0.5	5.3 x 4.9	23 (11)	4	–	RX/TX 3 个三线数据通道
MG132P	MBGA	Wire Bond	0.5	8 x 8	38(18)	4	RX/TX 4 data lanes 1 clock lanes	RX/TX 3-trios data lanes

Note!

[1] Transceivers in the MBGA package can reach speeds up to 10.3125 Gbps, and when the rate exceeds 8 Gbps, only on-board interconnects are supported, not backplane applications.

GW5ANT series

Table 19 GW5ANT series of FPGA Products Information List

Device	GW5ANT-15
LUT4	15120
Flip-Flop (REG)	15120
Shadow Static Random Access Memory SSRAM(Kb)	118.125
Block Static Random Access Memory BSRAM(Kb)	630
Number of BSRAMs BSRAM	35
NOR Flash (bits)	8M
DSP（27-bit x 18-bit）	28
DSP Lite	12
Maximum phase locked loop[1](PLLs)	2
Global Clocks	16
High-speed Clocks	2
Transceivers[2]	4
TransceiVers Rate	270Mbps - 12.5Gbps
PCIe3.0 Hardcore	1, x1, x2, x4 PCIe 3.0
LVDS Gbps	1.25
DDR3 Mbps	1333
MIPI D-PHY hardcore	2.5Gbps (RX/TX), 4 data lanes 1 clock lanes
MIPI C-PHY Hardcore	2.5Gsps (=5.75Gbps,RX/TX), 3-trios data lanes
ADC	1
Number of GPIO banks	4
Maximum number of GPIOs[3]	53
Core voltage	0.9V/1.0V[4]

Note!

- [1] Different packages support different numbers of PLLs, and here is the max. number.
- [2] Different packages support different number of Transceivers, and here is the max. number.
- [3] This is the max. number of GPIOs that the device can provide without package limitation. Please refer to Table 20 for the maximum number of user I/O available in specific packages.
- [4] It is recommended to use 0.9V for Vcc, 1.0V tends to increase power consumption.

Table 20 GW5ANT series Package Information

Package			Pitch (mm)	Size (mm)	GW5ANT-15			
Name	Type	Description			I/O (True LVDS Pair)	Transce-ivers[1]	MIPI D- PHY Hardcore	MIPI C-PHY Hardcore
MG132	MBGA	Wire Bond	0.5	8 x 8	47(22)	4	RX/TX 4 data lanes 1 clock lanes	RX/TX 3-trios data lanes

Note!

[1] Transceivers in the MBGA package can reach speeds up to 10.3125 Gbps, and when the rate exceeds 8 Gbps, only on-board interconnects are supported, not backplane applications.

GW5ANRT series

Table 21 GW5ANRT of FPGA Products Information List

Device	GW5ANRT-15
LUT4	15120
Flip-Flop (REG)	15120
Shadow Static Random Access Memory SSRAM(Kb)	118.125
Block Static Random Access Memory BSRAM(Kb)	630
Number of BSRAMs BSRAM	35
PSRAM (units)	1
Single PSRAM (bits)	64M
NOR Flash (bits)	8M
DSP（27-bit x 18-bit）	28
DSP Lite	12
Maximum phase locked loop[1](PLLs)	2
Global Clocks	16
High-speed Clocks	2
Transceivers[2]	4
TransceiVers Rate	270Mbps - 12.5Gbps
PCIe 3.0 Hardcore	1, x1, x2, x4 PCIe 3.0
LVDS Gbps	1.25
DDR3 Mbps	1333
MIPI D-PHY hardcore	2.5Gbps (RX/TX), 4 data lanes 1 clock lanes
MIPI C-PHY Hardcore	2.5Gsps (=5.75Gbps,RX/TX), 3-trios data lanes
ADC	1
Number of GPIO banks	4
Maximum number of GPIOs[3]	53
Core voltage	0.9V/1.0V[4]

Note!

- [1] Different packages support different numbers of PLLs, and here is the max. number.
- [2] Different packages support different number of Transceivers, and here is the max. number.
- [3] This is the max. number of GPIOs that the device can provide without package limitation. Please refer to Table 22 for the maximum number of user I/O available in specific packages.
- [4] It is recommended to use 0.9V for Vcc, 1.0V tends to increase power consumption.

Table 22 GW5ANRT-15 Package Information

Package			Pitch (mm)	Size (mm)	GW5ANRT-15			
Name	Type	Description			I/O (True LVDS Pair)	Transce-ivers[1]	MIPI D- PHY Hardcore	MIPI C-PHY Hardcore
MG132P	MBGA	Wire Bond	0.5	8 x 8	32(16)	4	RX/TX 4 data lanes 1 clock lanes	RX/TX 3-trios data lanes

Note!

[1] Transceivers in the MBGA package can reach speeds up to 10.3125 Gbps, and when the rate exceeds 8 Gbps, only on-board interconnects are supported, not backplane applications.

Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find related documents at www.gowinsemi.com.

- DS981, Arora V 138K& 75K of FPGA Products Data Sheet
- DS1225, Arora V 60K FPGA Products Data User Guide
- DS1103, Arora V 25K FPGA Products Data User Guide
- DS1118, Arora V 15K FPGA Products Data User Guide
- UG983, GW5AT series of FPGA Products Package and Pinout Manual
- UG1101, GW5A series of FPGA Products Package and Pinout Manual
- UG1102, GW5AST series of FPGA Products Package and Pinout Manual
- UG1106, GW5AS series of FPGA Products Package and Pinout Manual
- UG1109, GW5AR series of FPGA Products Package and Pinout Manual
- UG1119, FPGA series of FPGA Products Package and Pinout Manual
- UG300，Arora V BSRAM & SSRAM User Manual
- UG303, Arora V Configurable Function Unit (CFU) User Guide
- UG304, Arora V Input/Output (GPIO) User Guide
- UG287, Arora V DSP Module User Guide
- UG286, Arora V Clock　Clock User Guide.
- UG296, Arora V Hardened MIPI D-PHY RX TX User Guide
- UG297, Arora V SEU Handler User Guide
- UG299，Arora V ADC User Guide
- UG984E, UG984& GW5AST series of FPGA Products Schematic Manual
- UG984E, UG984& GW5AST series of FPGA Products Schematic Manual
- UG704E, Arora V 138K& 138K FPGA Products Programming and Configuration User Guide
- UG704E, Arora V FPGA Products Programming and Configuration User Guide
- UG704E, Arora V 25K FPGA Products Programming and Configuration User Guide
- UG982, GW5AT-138 Pinout
- UG986, GW5AST-138 Pinout

- UG1107, GW5AS-138 Pinout
- UG1221, GW5AT-75 Pinout
- UG1222, GW5AT-60 Pinout
- UG1229,GW5A-60 Pinout
- UG985, GW5A-25 Pinout
- UG1115, GW5AS-25 Pinout
- UG1110E, GW5AR-25 Pinout
- UG1224E, GW5AT-15 Pinout
- UG1120E, GW5ART-15 Pinout
- UG1226, GW5ANT-15 Pinout
- UG1227, GW5ANRT-15 Pinout

Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

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Revision History

Date	Version	Description
06/14/2024	1.0E	Initial version published.
06/28/2024	1.1E	● GW5A-60 UG324A and UG324S added. ● GW5ART-15 CM90PF added.
07/19/2024	1.1.1E	● The user I/O info. of GW5AT-138 FPG676A / PG676A / PG484A / PG484 updated. ● The user I/O info. of GW5A-25 MG121N updated.

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