



# GW1NSR Series of FPGA Products

## **Datasheet**

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Date	Version	Description
		<p>modifying I<sub>OL</sub> and I<sub>OH</sub> of LVCMOS12 standard.</p> <ul style="list-style-type: none"> <li>● “Table 3-15 Gearbox Timing Parameters” optimized.</li> <li>● “Table 3-24 GW1NSR-4 User Flash Parameters<sup>[1], [4], [5]</sup>” updated.</li> <li>● “Figure 4-5 Package Marking Examples” updated.</li> <li>● Note about default state of GPIOs optimized.</li> <li>● Description of MIPI input/output updated.</li> <li>● Description of IODELAY module updated.</li> <li>● Description of background upgrade added.</li> <li>● Description of HCLK optimized.</li> <li>● Note on functional description of dual port BSRAM and semi-dual port BSRAM modified.</li> <li>● Description of PSRAM updated.</li> <li>● Description of MIPI IO optimized.</li> </ul>
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# 1 General Description

The GW1NSR FPGAs are members of the 1 series of the LittleBee family. The GW1NR devices are system-in-package chips with memory chips integrated into them based on the GW1NS devices. The GW1NSR series consists of the GW1NSR-4C device(embedded with an ARM Cortex-M3 processor) and the GW1NSR-4 device.

The GW1NSR-4C device is based on the ARM Cortex-M3 processor and has the minimum memory required to implement system functions. Its adaptable and flexible embedded FPGA logic modules enable the implementation of diverse peripheral control tasks, along with delivering excellent computing capabilities and advanced exception handling. Seamlessly integrating a programmable logic device with an embedded processor, the GW1NSR-4C device is compatible with a range of peripheral standards, resulting in substantial cost savings for users. This makes it a highly versatile choice, suitable for a wide array of applications spanning industrial control, communications, IoT, servo drives, and consumer electronics, among others.

In addition, the GW1NS series FPGA products boast high performance, low power consumption, a small pin count, flexible usage, instant-on, low-cost, non-volatility, enhanced security, and a wide range of packaging options.

Gowin provides an advanced FPGA hardware development environment that supports FPGA synthesis, placement & routing, bitstream generation and download, etc.

## 1.1 Features

- Lower power consumption
  - 55nm embedded Flash technology
  - Core voltage: 1.2V
  - GW1NSR-4C/4 support LV version only
  - Supports dynamically turning on/off the clock
- Integrated with HyperRAM/PSRAM memory chips
- Integrated with NOR Flash
- Hard core processor
  - 32-bit Arm Cortex-M3 processor
  - ARM v7-M Thumb2 architecture optimized for small-footprint embedded applications

- System timer (SysTick), providing a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism
- Thumb compatible, Thumb-2 instruction set processor core for high code density
- GW1NSR-4C supports up to 80 MHz operation
- Hardware-division and single-cycle-multiplication
- Integrated nested vectored interrupt controller (NVIC) providing deterministic interrupt handling
- 26 interrupts with eight priority levels
- Memory protection unit (MPU), providing a privileged mode for protecting operation system functionality
- Unaligned data access, enabling data to be efficiently packed into memory
- Atomic bit manipulation (bit-banding), delivering maximum memory utilization and streamlined peripheral control
- Timer0 and Timer1
- UART0 and UART1
- watchdog
- Debug port: JTAG and TPIU
- User Flash (GW1NSR-4)
  - NOR Flash
  - 256Kbits storage space
  - Data width:32bits
  - 10,000 write cycles
  - Greater than 10 years of data retention at +85°C
- Configuration Flash
  - NOR Flash
  - 10,000 write cycles
  - Greater than 10 years of data retention at +85°C
- Multiple I/O standards
  - LVCMOS33/25/18/15/12; LVTTTL33, SSTL33/25/18 I, SSTL33/25/18 II, SSTL15; HSTL18 I, HSTL18 II, HSTL15 I; PCI, LVDS25, RSDS, LVDS25E, BLVDSE, MLVDSE, LVPECLE, RSDSE
  - Input hysteresis options
  - Drive strength options
  - Individual Bus Keeper, Pull-up/Pull-down, and Open Drain options
  - Hot socketing
- MIPI D-PHY RX/TX Implemented by Using GPIOs
  - Supports MIPI CSI-2 and MIPI DSI RX/TX with a data rate of up to 1.2Gbps per lane
  - Three IO types are available: TLVDS, ELVDS, and MIPI IO.
- Abundant basic logic cells
  - 4-input LUTs (LUT4s)
  - Supports shift registers
- Block SRAMs with multiple modes
  - Supports Dual Port mode, Single Port mode, and Semi-Dual Port mode
- Flexible PLLs
  - Frequency adjustment (multiplication and division) and phase adjustment
  - Supports global clocks
- Built-in Flash programming
  - Instant-on

- Supports security bit operation
- Supports AUTO BOOT and DUAL BOOT
- Configuration
- JTAG configuration
- Multiple GowinCONFIG configuration modes: AUTO BOOT, DUAL BOOT, SSPI, MSPI, CPU, SERIAL

## 1.2 Product Resources

Table 1-1 Product Resources

Device	GW1NSR-4	GW1NSR-4C
LUT4s	4,608	4,608
Flip-Flops (FFs)	3,456	3,456
Block SRAM (BSRAM) Capacity (bits)	180K	180K
Number of BSRAMs	10	10
Multiplier (18 x 18 Multiplier)	16	16
User Flash (bits)	256K	-
PSRAM (bits)	64M	64M
HyperRAM (bits)	-	64M
NOR FLASH (bits)	-	32M
PLLs	2	2
OSC	1, $\pm 5\%$ tolerance	1, $\pm 5\%$ tolerance
Hard core processor	-	Cortex-M3
I/O Banks	4	4
Maximum GPIOs <sup>[1]</sup>	106	106
Core voltage	1.2V	1.2V

**Note!**

<sup>[1]</sup> This is the maximum number of GPIOs the device can provide without package limitation. Please refer to Table 1-3 for the maximum number of user I/Os available for the specific packages.

## 1.3 Package Information

Table 1-2 Package-Memory Combinations

Device	Package	Memory Type	Capacity	Width
GW1NSR-4	MG64P	PSRAM	64Mb	16 bits
GW1NSR-4C	MG64P	PSRAM	64Mb	16 bits
	QN48P	HyperRAM		8 bits
	QN48G	NOR FLASH	32Mb	1 bit

Table 1-3 Device-Package Combinations and Maximum User I/Os (True LVDS Pairs)

Package	Pitch (mm)	Size (mm)	GW1NSR-4	GW1NSR-4C
MG64P	0.5	4.2 x 4.2	55(8)	55(8)
QN48G	0.4	6 x 6	-	39(4)
QN48P	0.4	6 x 6	-	39(4)

**Note!**

- JTAGSEL\_N and JTAG pins cannot be used as GPIOs simultaneously. However, when mode [2:0] = 001, the JTAGSEL\_N pin is always a GPIO, in other words the JTAGSEL\_N pin and the four JTAG pins (TCK, TMS, TDI, TDO) can be used as GPIOs simultaneously. See [UG863, GW1NSR series of FPGA Products Package and Pinout User Guide](#) for more details.
- The package types in this manual are referred to by acronyms, see [4.1 Part Naming](#) for more information.
- For more information, see [UG864, GW1NSR-4 Pinout](#) and [UG865, GW1NSR-4C Pinout](#).

# 2 Architecture

## 2.1 Architecture Overview

Figure 2-1 Architecture Overview of GW1NSR-4

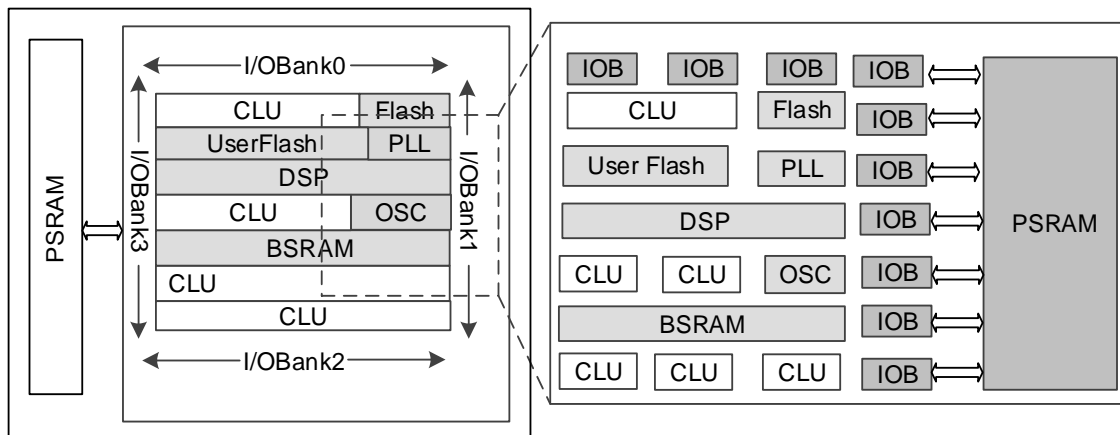
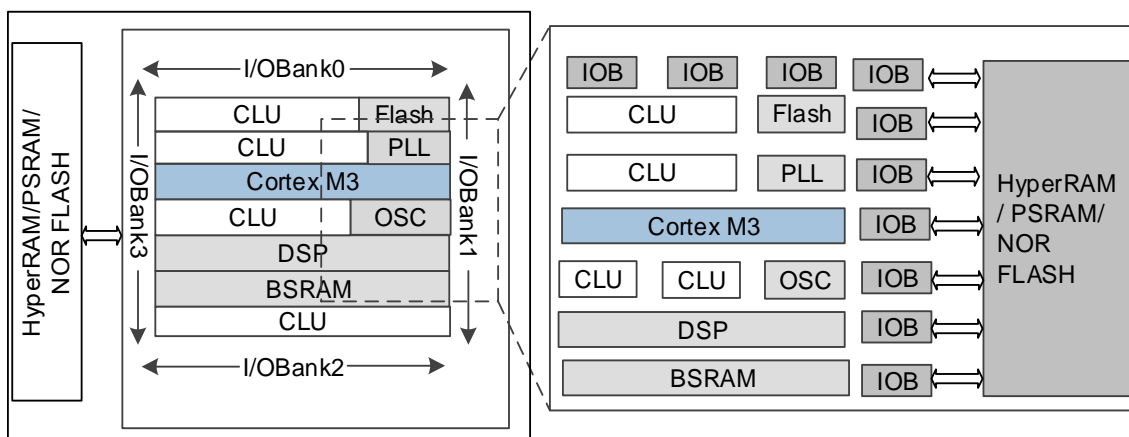


Figure 2-2 Architecture Overview of GW1NSR-4C



The GW1NSR device is a system-in-package(SIP) chip that combines the GW1NS device and a memory chip. For the features and overview of PSRAM, see [2.2 PSRAM](#). For the features and overview of HyperRAM, see [2.3 HyperRAM](#). For the features and overview of NOR FLASH, see

## 2.4 NOR FLASH.

The core of the GW1NSR device is an array of logic cells surrounded by IO blocks. Besides, BSRAMs, DSP blocks, PLLs, an on-chip oscillator, and Flash resources allowing for instant-on are provided. In addition, GW1NSR-4C has an embedded Cortex-M3 processor, see Table 1-1.

The Configurable Logic Units (CLUs) are the basic logic blocks that form the core of GW1NSR FPGAs. Devices with different capacities have different numbers of rows and columns of CFUs/CLUs. For more information, see 2.5 Configurable Function Units.

The I/O resources in the GW1NSR series of FPGA products are arranged around the periphery of the devices in groups referred to as banks. The I/O resources support multiple I/O standards and can be used for regular mode, SDR mode, and generic DDR mode. For more information, see 2.6 Input/Output Blocks.

BSRAMs are arranged in row(s) inside the GW1NSR series of FPGA products. Each BSRAM occupies 3 CLU locations. There are two uses of BSRAMs, but the two uses cannot be used at the same time. Firstly, they function as the SRAM resources for the Cortex-M3 processor system. The capacity of each BSRAM is 16Kbits, and the total capacity is 128Kbits(GW1NSR-4/4C). Secondly, they can be utilized for user storage. The capacity of each BSRAM is 18Kbits, and the total capacity is 180Kbits(GW1NSR-4/4C). And in this case multiple configuration modes and operation modes are supported. For more information, see 2.7 Block SRAM.

GW1NSR-4 has built-in User Flash memory resources, ensuring data retention even when powered off. See 2.8 User Flash (GW1NSR-4) for more information.

The GW1NSR series of FPGA products provide DSP blocks. Each DSP block contains two macros, and each macro contains two pre-adders, two 18 x 18 bit multipliers, and one three-input ALU. For more information, see 2.9 Digital Signal Processing.

The GW1NSR series of FPGA products have embedded PLL resources. The PLLs can provide synthesizable clock frequencies. Frequency adjustment (multiplication and division), phase adjustment, and duty cycle adjustment can be realized by configuring the parameters. In addition, a programmable on-chip oscillator is provided. For more information, see 2.12 Clocks and 2.16 On-chip Oscillator.

The embedded configuration Flash resources in GW1NSR FPGAs support instant-on and security bit operations, catering to AUTO BOOT and DUAL BOOT configuration modes. For more information, see 2.15 Programming & Configuration.

The Cortex-M3 processor supports 30 MHz program loading when the system starts up and supports higher speed data/instructions transmission. The AHB expansion bus facilitates communication with external storage devices. The APB bus also facilitates communication with external devices, such as UART. GPIO interfaces are convenient for



communicating with the external interfaces. The FPGA can be programmed to realize controller functions across different interfaces / standards, such as SPI, I<sup>2</sup>C, I3C, etc. For more information, see [2.11 Cortex-M3](#).

## 2.2 PSRAM

### Features

- Clock frequency: 166 MHz
- Double Data Rate
- 32Mb capacity for each PSRAM
- 8-bit data width for each PSRAM
- Read-write data strobe (RWDS)
- Temperature compensated refresh
- Partial array self-refresh (PASR)
- Hybrid sleep mode
- Deep power down(DPD)
- Drive strengths: 35, 50, 100, and 200 Ohm
- Burst access
- Burst lengths: 16/32/64/128
- Status/control registers
- 1.8V power supply

Please refer to the corresponding pinout manual for the power supply of the PSRAM.

The IP Core Generator integrated in the Gowin Software supports a PSRAM controller IP that can interface to both embedded and external PSRAMs. This controller IP can be used for the PSRAM power-up initialization, read calibration, etc. For more information, please refer to [\*IPUG525, Gowin PSRAM Memory Interface IP User Guide\*](#).

## 2.3 HyperRAM

### Features

- Clock frequency: 200 MHz
- Double Data Rate
- Clock: supports single-ended clock and differential clock
- Supports chip select
- Data width: 8bits
- Supports hardware reset
- Read-write data strobe (RWDS)
  - Bidirectional Data Strobe / Mask

- Output at the start of all transactions to indicate refresh latency
- Output during read transactions as Read Data Strobe
- Input during write transactions as Write Data Mask
- Die Stack Address
- Performance and Power
  - Configurable output drive strength
  - Power saving modes: Hybrid Sleep Mode and Deep Power Down
- Configurable Burst characteristics
  - Linear burst
  - Wrapped burst lengths: 16 bytes, 32 bytes, 64 bytes, and 128 bytes
  - Hybrid burst: one wrapped burst followed by linear burst
- Array Refresh Modes: Full Array Refresh and Partial Array Refresh
- Power Supply: 1.7V~2.0V

For the power supply of the HyperRAM, please refer to [UG865, GW1NSR-4C Pinout](#).

The IP Core Generator integrated in the Gowin Software supports a HyperRAM controller IP that can interface to both embedded and external HyperRAMs. This controller IP can be used for the HyperRAM power-up initialization, read calibration, etc. For more information, please refer to [IPUG944, Gowin HyperRAM Memory Interface IP User Guide](#).

## 2.4 NOR FLASH

The SoC with the package suffix of “G”, such as QN48G, is embedded with NOR Flash.

### Features

- 32 Mbits of storage, 256 bytes per page
- Supports SPI
- Clock frequency: 120 MHz
- Continuous read with 8/16/32/64 bytes wrap
- Software/Hardware Write Protection:
  - Entire/partial write protection via software settings
  - Top/bottom block protection
- Minimum 100,000 program/erase cycles
- Fast program/erase operations:
  - Page program time: 0.5ms
  - Sector erase time: 45ms
  - Block erase time: 0.15s/0.25s

- Chip erase time: 12s
- Flexible Architecture:
  - Sector: 4K bytes
  - Block: 32/64K bytes
  - Erase/Program Suspend/Resume
- Lower power consumption:
  - Stand-by current: 12uA
  - Power down current: 1uA
- Security Features
  - 128-bit unique ID for each device
  - 3x1024-Byte security registers with OTP Lock
- Data retention: 20 years

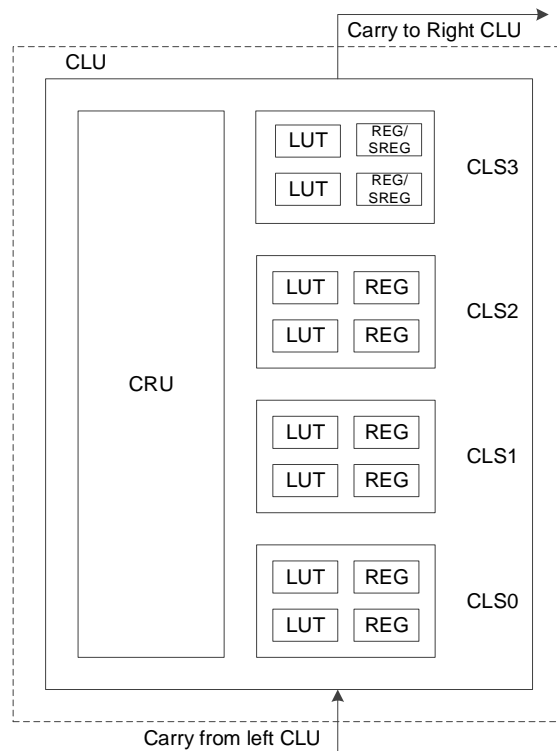
Gowin provides a universal SPI NOR Flash Interface IP allowing for interconnection with the SPI NOR Flash chip. For more information, see [\*IPUG945, Gowin SPI Nor Flash Interface IP User Guide\*](#).

## 2.5 Configurable Function Units

Configurable Function Units (CFUs) and/or Configurable Logic Units (CLUs) are the basic cells that make up the core of Gowin FPGAs. Each basic cell consists of four Configurable Logic Sections (CLSs) and their routing resource Configurable Routing Units (CRUs), with three of the CLSs each containing two 4-input LUTs and two registers, and the remaining one only containing two 4-input LUTs, as shown in Figure 2-3.

The CLSs in the CLUs cannot be configured as SRAMs, but can be configured as basic LUTs, ALUs, and ROMs. The CLSs in the CFUs can be configured as basic LUTs, ALUs, SRAMs, and ROMs according to application scenarios.

For more information on the CFUs/CLUs, see [\*UG288, Gowin Configurable Function Unit \(CFU\) User Guide\*](#).

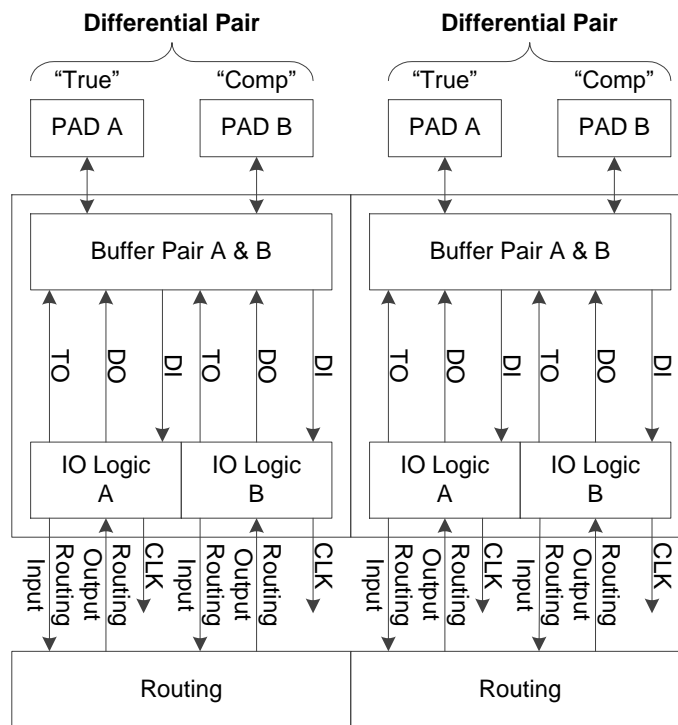
**Figure 2-3 CLU Structure View****Note!**

The SREGs need special patch support. Please contact Gowin's technical support or local office for this patch.

## 2.6 Input/Output Blocks

The Input/Output Block (IOB) in the GW1NSR series of FPGA products consists of a buffer pair, IO logic, and corresponding routing units. As shown in the figure below, each IOB connects to two pins (marked as A and B), which can be used as a differential pair or as two single-ended inputs/outputs.

Figure 2-4 IOB Structure View



The features of the IOB include:

- $V_{CCIO}$  supplied to each bank
- LVCMOS, PCI, LVTTTL, LVDS, SSTL, HSTL, etc. Bank3 of GW1NSR-4C/4 only supports single-ended LVCMOS input/output and LVDS25E differential output
- Input hysteresis options
- Drive strength options
- Individual Bus Keeper, Pull-up/Pull-down, and Open Drain options
- Hot socketing(except Bank3 of GW1NSR-4C/4)
- IO logic supports basic mode, SDR mode, DDR mode, etc.
- Bank0/Bank1 of GW1NSR-4C/4 can support MIPI input by using MIPI IO type.
- Bank2 of GW1NSR-4C/4 can support MIPI output by using MIPI IO type.
- Bank0/Bank1/Bank2 of GW1NSR-4C/4 support I3C.

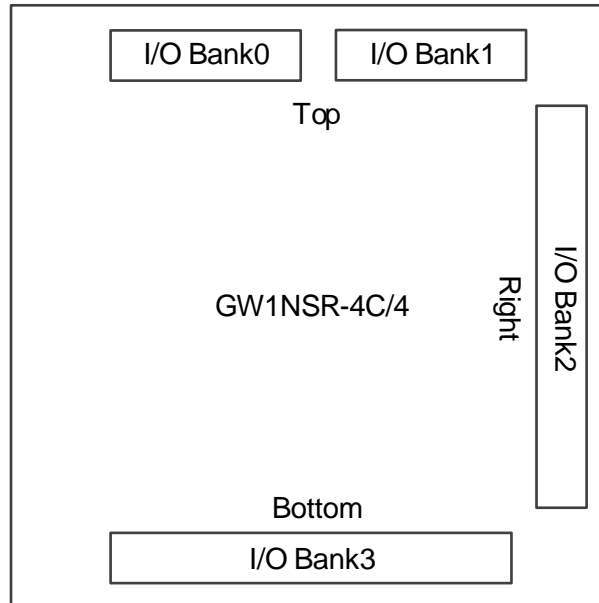
2.6.1~ 2.6.4 describe I/O standards, true LVDS design, I/O logic, and I/O logic modes. For more information about the IOB, please refer to [UG289, Gowin Programmable IO \(GPIO\) User Guide](#).

## 2.6.1 I/O Standards

There are four I/O banks in the GW1NSR series of FPGA products, as shown in Figure 2-5. Each bank has its own I/O power supply  $V_{CCIO}$ .

To support SSTL, HSTL, etc., each bank also has one independent voltage source ( $V_{REF}$ ) as the reference voltage. You can choose to use the internal  $V_{REF}$  ( $0.5 \times V_{CCIO}$ ) or the external  $V_{REF}$  input via any IO from the bank.

Figure 2-5 I/O Bank Distribution View of GW1NSR-4C/4



The GW1NSR FPGAs support LV version.

The GW1NSR FPGAs support 1.2V  $V_{CC}$  (core voltage).

$V_{CCX}$ (auxiliary voltage) can be set to 1.8V, 2.5V, or 3.3V, and  $V_{CCIO}$ (I/O bank voltage) can be set to 1.2V, 1.5V, 1.8V, 2.5V, or 3.3V as needed.

**Note!**

- For GW1NSR-4C/4,  $V_{CCIO0}/V_{CCIO1}$  need to be set to 1.2V when Bank0/Bank1 are used for MIPI input, and  $V_{CCIO2}$  needs to be set to 1.2V when Bank2 is used for MIPI output. The MIPI speed with  $V_{CCX}$  set to 1.8V is only 60% of the MIPI speed with  $V_{CCX}$  set to 2.5V/3.3V.
- During configuration, all GPIOs of the device are high-impedance with internal weak pull-ups. After the configuration is complete, the I/O states are controlled by user programs and constraints. The states of configuration-related I/Os differ depending on the configuration mode.

For the  $V_{CCIO}$  requirements of different I/O standards, see Table 2-1 and Table 2-2.

Table 2-1 Output I/O Standards and Configuration Options Supported by GW1NSR Series of FPGA Products

I/O Type (output)	Single-ended/Differential	Bank $V_{CCIO}$ (V)	Drive Strength (mA)	Typical Applications
LVC MOS33/ LV TTL33	Single-ended	3.3	4/8/12/16/24	Universal interface
LVC MOS25	Single-ended	2.5	4/8/12/16	Universal interface
LVC MOS18	Single-ended	1.8	4/8/12	Universal interface
LVC MOS15	Single-ended	1.5	4/8	Universal interface

I/O Type (output)	Single-ended/Differential	Bank V <sub>CCIO</sub> (V)	Drive Strength (mA)	Typical Applications
LVCMOS12	Single-ended	1.2	4/8	Universal interface
SSTL25_I	Single-ended	2.5	8	Memory interface
SSTL25_II	Single-ended	2.5	8	Memory interface
SSTL33_I	Single-ended	3.3	8	Memory interface
SSTL33_II	Single-ended	3.3	8	Memory interface
SSTL18_I	Single-ended	1.8	8	Memory interface
SSTL18_II	Single-ended	1.8	8	Memory interface
SSTL15	Single-ended	1.5	8	Memory interface
HSTL18_I	Single-ended	1.8	8	Memory interface
HSTL18_II	Single-ended	1.8	8	Memory interface
HSTL15_I	Single-ended	1.5	8	Memory interface
PCI33	Single-ended	3.3	4/8	PC and embedded system
LVPECL33E	Differential	3.3	16	High-speed data transmission
MVLDS25E	Differential	2.5	16	LCD timing driver interface and column driver interface
BLVDS25E	Differential	2.5	16	Multi-point high-speed data transmission
RSDS25E	Differential	2.5	8	High-speed point-to-point data transmission
LVDS25E	Differential	2.5	8	High-speed point-to-point data transmission
MIPI	Differential (MIPI)	1.2	3.5	Mobile Industry Processor Interface
LVDS25	Differential (True LVDS)	2.5/3.3	2/2.5/3.5/6	High-speed point-to-point data transmission
RSDS	Differential (True LVDS)	2.5/3.3	2	High-speed point-to-point data transmission
MINILVDS	Differential (True LVDS)	2.5/3.3	2	LCD timing driver interface and column driver interface
PPLVDS	Differential (True LVDS)	2.5/3.3	3.5	LCD row/column driver
SSTL15D	Differential	1.5	8	Memory interface
SSTL25D_I	Differential	2.5	8	Memory interface
SSTL25D_II	Differential	2.5	8	Memory interface
SSTL33D_I	Differential	3.3	8	Memory interface
SSTL33D_II	Differential	3.3	8	Memory interface
SSTL18D_I	Differential	1.8	8	Memory interface

I/O Type (output)	Single-ended/Differential	Bank V <sub>CCIO</sub> (V)	Drive Strength (mA)	Typical Applications
SSTL18D_II	Differential	1.8	8	Memory interface
HSTL18D_I	Differential	1.8	8	Memory interface
HSTL18D_II	Differential	1.8	8	Memory interface
HSTL15D_I	Differential	1.5	8	Memory interface
LVC MOS12D	Differential	1.2	4/8	Universal interface
LVC MOS15D	Differential	1.5	4/8	Universal interface
LVC MOS18D	Differential	1.8	4/8/12	Universal interface
LVC MOS25D	Differential	2.5	4/8/12/16	Universal interface
LVC MOS33D	Differential	3.3	4/8/12/16/24	Universal interface

**Table 2-2 Input I/O Standards and Configuration Options Supported by GW1NSR Series of FPGA Products**

I/O Type (input)	Single-ended/Differential	Bank V <sub>CCIO</sub> (V)	Hysteresis Options Supported?	V <sub>REF</sub> Required?
LVC MOS33/ LV TTL33	Single-ended	3.3	Yes	No
LVC MOS25	Single-ended	2.5	Yes	No
LVC MOS18	Single-ended	1.8	Yes	No
LVC MOS15	Single-ended	1.5	Yes	No
LVC MOS12	Single-ended	1.2	Yes	No
SSTL15	Single-ended	1.5	No	Yes
SSTL25_I	Single-ended	2.5	No	Yes
SSTL25_II	Single-ended	2.5	No	Yes
SSTL33_I	Single-ended	3.3	No	Yes
SSTL33_II	Single-ended	3.3	No	Yes
SSTL18_I	Single-ended	1.8	No	Yes
SSTL18_II	Single-ended	1.8	No	Yes
HSTL18_I	Single-ended	1.8	No	Yes
HSTL18_II	Single-ended	1.8	No	Yes
HSTL15_I	Single-ended	1.5	No	Yes
LVC MOS33OD25	Single-ended	2.5	No	No
LVC MOS33OD18	Single-ended	1.8	No	No



I/O Type (input)	Single-ended/Differential	Bank V <sub>CCIO</sub> (V)	Hysteresis Options Supported?	V <sub>REF</sub> Required?
LVC MOS33OD15	Single-ended	1.5	No	No
LVC MOS25OD18	Single-ended	1.8	No	No
LVC MOS25OD15	Single-ended	1.5	No	No
LVC MOS18OD15	Single-ended	1.5	No	No
LVC MOS15OD12	Single-ended	1.2	No	No
LVC MOS25UD33	Single-ended	3.3	No	No
LVC MOS18UD25	Single-ended	2.5	No	No
LVC MOS18UD33	Single-ended	3.3	No	No
LVC MOS15UD18	Single-ended	1.8	No	No
LVC MOS15UD25	Single-ended	2.5	No	No
LVC MOS15UD33	Single-ended	3.3	No	No
LVC MOS12UD15	Single-ended	1.5	No	No
LVC MOS12UD18	Single-ended	1.8	No	No
LVC MOS12UD25	Single-ended	2.5	No	No
LVC MOS12UD33	Single-ended	3.3	No	No
PCI33	Single-ended	3.3	Yes	No
VREF1_DRIVER	Single-ended (Vref Input)	1.2/1.5/1.8/2.5/3.3	No	Yes
MIPI	Differential (MIPI)	1.2	No	No
LVDS25	Differential	2.5/3.3	No	No
RS DS	Differential	2.5/3.3	No	No
MINILVDS	Differential	2.5/3.3	No	No
PPLVDS	Differential	2.5/3.3	No	No
LVDS25E	Differential	2.5/3.3	No	No
MLVDS25E	Differential	2.5/3.3	No	No
BLVDS25E	Differential	2.5/3.3	No	No
RS DS25E	Differential	2.5/3.3	No	No
LVPECL33E	Differential	3.3	No	No
SSTL15D	Differential	1.5	No	No
SSTL25D_I	Differential	2.5	No	No
SSTL25D_II	Differential	2.5	No	No

I/O Type (input)	Single-ended/Differential	Bank V <sub>CCIO</sub> (V)	Hysteresis Options Supported?	V <sub>REF</sub> Required?
SSTL33D_I	Differential	3.3	No	No
SSTL33D_II	Differential	3.3	No	No
SSTL18D_I	Differential	1.8	No	No
SSTL18D_II	Differential	1.8	No	No
HSTL18D_I	Differential	1.8	No	No
HSTL18D_II	Differential	1.8	No	No
HSTL15D_I	Differential	1.5	No	No
LVC MOS12D	Differential	1.2	No	No
LVC MOS15D	Differential	1.5	No	No
LVC MOS18D	Differential	1.8	No	No
LVC MOS25D	Differential	2.5	No	No
LVC MOS33D	Differential	3.3	No	No

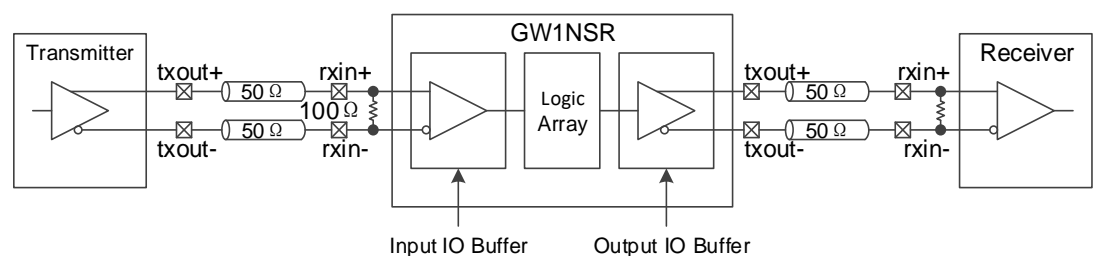
## 2.6.2 True LVDS Design

Bank2 of GW1NSR-4C/4 supports true LVDS output. In addition, LVDS25E, MLVDS25E, BLVDS25E, etc. are supported.

For more information about true LVDS, see [UG864, GW1NSR-4 Pinout](#), [UG865, GW1NSR-4C Pinout](#).

True LVDS input needs a 100Ω termination resistor, see Figure 2-6 for the reference design. Bank0/1 of the GW1NSR-4C/4 devices support programmable on-chip 100Ω input differential termination resistors, see [UG289, Gowin Programmable IO User Guide](#).

Figure 2-6 True LVDS Design



For information about termination for LVDS25E, MLVDS25E, and BLVDS25E, please refer to [UG289, Gowin Programmable IO User Guide](#).

## 2.6.3 I/O Logic

Figure 2-7 shows the I/O logic input and output of the GW1NSR series of FPGA products.

Figure 2-7 I/O Logic Input and Output

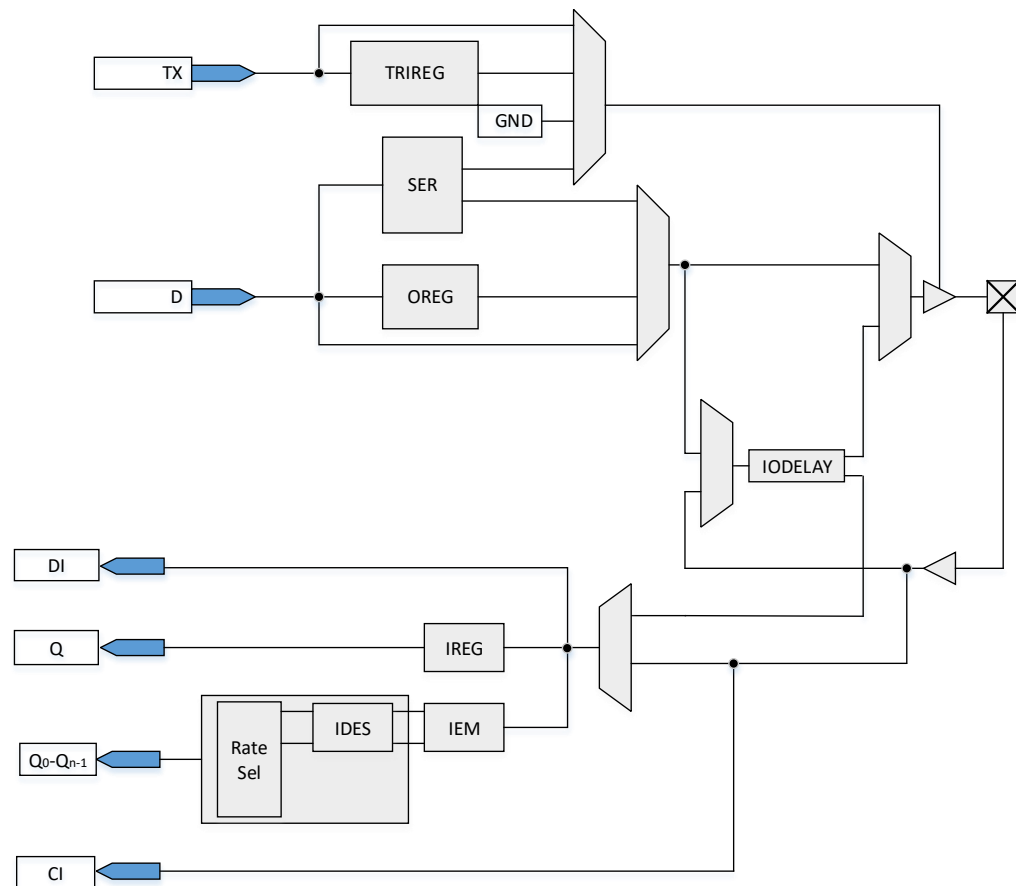


Table 2-3 Port Description

Port	I/O	Description
CI <sup>[1]</sup>	Input	GCLK input signal. For the number of GCLK input signals, please refer to <a href="#">UG864, GW1NSR-4 Pinout</a> and <a href="#">UG865, GW1NSR-4C Pinout</a> .
DI	Input	IO port low-speed input signal input into the fabric directly.
Q	Output	IREG output signal in the SDR module.
Q0-Qn-1	Output	IDES output signal in the DDR module.

**Note!**

<sup>[1]</sup> When CI is used as GCLK input, DI, Q, and Q0-Qn-1 cannot be used as I/O input and output.

Descriptions of the I/O logic modules of the GW1NSR series of FPGA products are presented below.

**IODELAY**

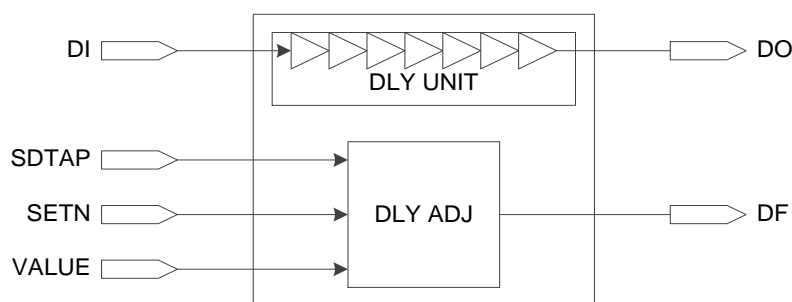
See Figure 2-8 for an overview of the IODELAY module. Each I/O of the GW1NSR series of FPGA products contains the IODELAY module, through which you can add additional delays to the I/O to adjust the delay of the signal. The delay time of each step is  $T_{dlyunit}$ , and the number of steps is DLYSTEP. The total delay time of IODELAY can be calculated as

follows:  $T_{\text{totdly}} = T_{\text{dlyoffset}} + T_{\text{dlyunit}} * \text{DLYSTEP}$ . See Table 2-4 for the total delay time.

**Table 2-4 Total Delay of IODELAY Module**

	Min.	Typ.	Max.
$T_{\text{dlyoffset}}$	450ps	500ps	550ps
$T_{\text{dlyunit}}$	-	30ps	-
DLYSTEP	0	-	127

**Figure 2-8 IODELAY Diagram**



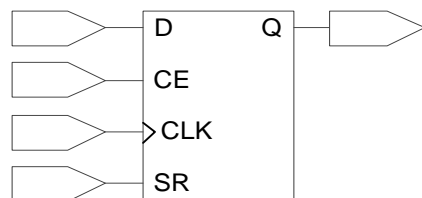
There are two ways to control the delay:

- Static control.
- Dynamic control: can be used with the IEM module to adjust the dynamic sampling window. The IODELAY module cannot be used for both input and output at the same time.

### I/O Register

See Figure 2-9 for the I/O register in the GW1NSR series of FPGA products. Each I/O provides one input register (IREG), one output register (OREG), and one tristate register (TRIREG).

**Figure 2-9 I/O Register Diagram**



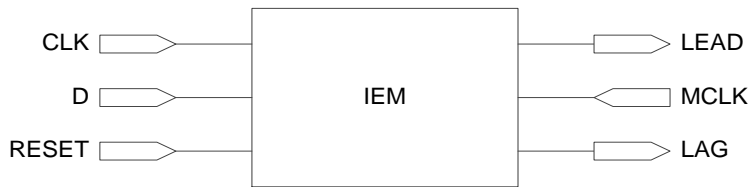
#### Note!

- CE can be programmed as either active low (0: enable) or active high (1: enable).
- CLK can be programmed as either rising edge triggering or falling edge triggering.
- SR can be programmed as either synchronous/asynchronous SET/RESET or disabled.
- The register can be programmed as a register or a latch.

## IEM

The IEM(Input Edge Monitor) module is used to sample data edges and is used in generic DDR mode, as shown in Figure 2-10.

Figure 2-10 IEM Diagram



## DES

This series of FPGA products provide a simple deserializer(DES) for input I/O logic to support advanced I/O protocols.

## SER

This series of FPGA products provide a simple serializer(SER) for output I/O logic to support advanced I/O protocols.

## 2.6.4 I/O Logic Modes

The I/O Logic of the GW1NSR series of FPGA products supports several operation modes. In each operation mode, the I/O (or I/O differential pair) can be configured as output, input, INOUT or tristate output (output signal with tristate control).

## 2.7 Block SRAM

### 2.7.1 Introduction

The GW1NSR series of FPGA products provide abundant block SRAM resources. These memory resources are distributed as blocks throughout the FPGA array in the form of rows. Therefore, they are called block static random access memories (BSRAMs).

BSRAMs serve two main purposes.

1. They function as the SRAM resources for the Cortex-M3 processor system. The capacity of a BSRAM when used as the SRAM for Cortex-M3 is 16Kbits (2K-Byte). The Gowin software supports the configuration of SRAM resources, offering options like 2K-Byte, 4K-Byte, and 8K-Byte. Any unused BSRAMs are available for user storage.
2. They can also be used exclusively for FPGA data storage, and each BSRAM can be configured to a maximum of 18,432 bits (18Kbits). There are four configuration modes: Single Port mode, Dual Port mode, Semi-Dual Port mode, and ROM mode.

The abundant BSRAM resources are available for implementing high-performance designs. The features of BSRAMs include:

- Up to 18,432 bits per BSRAM
- Clock frequency up to 190MHz

- Supports Single Port mode
- Supports Dual Port mode
- Supports Semi-Dual Port mode
- Provides parity bits
- Supports ROM Mode
- Data widths from 1 to 36 bits
- Mixed clock mode
- Mixed data width mode
- Normal Read and Write
- Read-before-write
- Write-through

For more information on the BSRAMs, see [UG285, Gowin BSRAM & SSRAM User Guide](#).

## 2.7.2 BSRAM Configuration Modes

BSRAMs in the GW1NSR series of FPGA products support various data widths, see Table 2-5.

Table 2-5 BSRAM Size Configuration

Single Port Mode	Dual Port Mode	Semi-Dual Port Mode	ROM Mode
16K x 1	16K x 1	16K x 1	16K x 1
8K x 2	8K x 2	8K x 2	8K x 2
4K x 4	4K x 4	4K x 4	4K x 4
2K x 8	2K x 8	2K x 8	2K x 8
1K x 16	1K x 16	1K x 16	1K x 16
512 x 32	-	512 x 32	512 x 32
2K x 9	2K x 9	2K x 9	2K x 9
1K x 18	1K x 18	1K x 18	1K x 18
512 x 36	-	512 x 36	512 x 36

### Single Port Mode

The single port mode supports 2 read modes (bypass mode and pipeline mode) and 3 write modes (normal mode, write-through mode, and read-before-write mode). In single port mode, writing to or reading from one port is supported. During the write operation, the written data will be transferred to the output of the BSRAM. When the output register is bypassed, the new data will show up at the same write clock rising edge.

For more information on single port mode, please refer to [UG285, Gowin BSRAM & SSRAM User Guide](#).

### Dual Port Mode

The Dual Port mode supports 2 read modes (Bypass mode and Pipeline mode) and 2 write modes (Normal mode and Write-through

mode). The applicable operations are as follows:

- Two independent read operations
- Two independent write operations
- An independent read operation and an independent write operation

**Note!**

Performing read and write operations to the same address at the same time is not allowed.

For more information on semi-dual port mode, please refer to [UG285, Gowin BSRAM & SSRAM User Guide](#).

### **Semi-Dual Port Mode**

The semi-dual port mode supports 2 read modes (Bypass mode and Pipeline mode) and 1 write mode (Normal mode). Semi-dual Port mode supports simultaneous read and write operations in the form of writing to port A and reading from port B.

**Note!**

Performing read and write operations to the same address at the same time is not allowed.

For more information on semi-dual port mode, please refer to [UG285, Gowin BSRAM & SSRAM User Guide](#).

### **ROM Mode**

BSRAMs can be configured as ROMs. The ROM can be initialized during the device configuration stage, and the ROM data needs to be provided in the initialization file. Initialization is completed during the device power-on process.

Each BSRAM can be configured as one 16Kbit ROM. For more information on ROM mode, please refer to [UG285, Gowin BSRAM & SSRAM User Guide](#).

## **2.7.3 Mixed Data Width Configuration**

The BSRAMs in the GW1NSR series of FPGA products support mixed data width operations. In dual port mode and semi-dual port mode, the data widths for read and write can be different, see Table 2-6 and Table 2-7.

Table 2-6 Dual Port Mixed Read/Write Data Width Configuration

Read Port	Write Port						
	16K x 1	8K x 2	4K x 4	2K x 8	1K x 16	2K x 9	1K x 18
16K x 1	*	*	*	*	*		
8K x 2	*	*	*	*	*		
4K x 4	*	*	*	*	*		
2K x 8	*	*	*	*	*		
1K x 16	*	*	*	*	*		
2K x 9						*	*
1K x 18						*	*

**Note!**

“\*” denotes the modes supported.

Table 2-7 Semi-dual Port Mixed Read/Write Data Width Configuration

Read Port	Write Port								
	16K x 1	8K x 2	4K x 4	2K x 8	1K x 16	512 x 32	2K x 9	1K x 18	512 x 36
16K x 1	*	*	*	*	*	*			
8K x 2	*	*	*	*	*	*			
4K x 4	*	*	*	*	*	*			
2K x 8	*	*	*	*	*	*			
1K x 16	*	*	*	*	*	*			
512x32	*	*	*	*	*	*			
2K x 9							*	*	*
1K x 18							*	*	*

**Note!**

“\*” denotes the modes supported.

## 2.7.4 Parity Bit

There are parity bits in BSRAMs. The 9th bit in each byte can be used as a parity bit to check the correctness of data transmission. It can also be used for data storage.

## 2.7.5 Synchronous Operation

- All the input registers of BSRAMs support synchronous write.
- The output registers can be used as pipeline registers to improve design performance.
- The output registers are bypass-able.

## 2.7.6 BSRAM Operation Modes

The BSRAM supports five different operations, including two read modes (Bypass mode and Pipeline mode) and three write modes (Normal mode, Write-through mode, and Read-before-write mode).



## Read Mode

The following two read modes are supported.

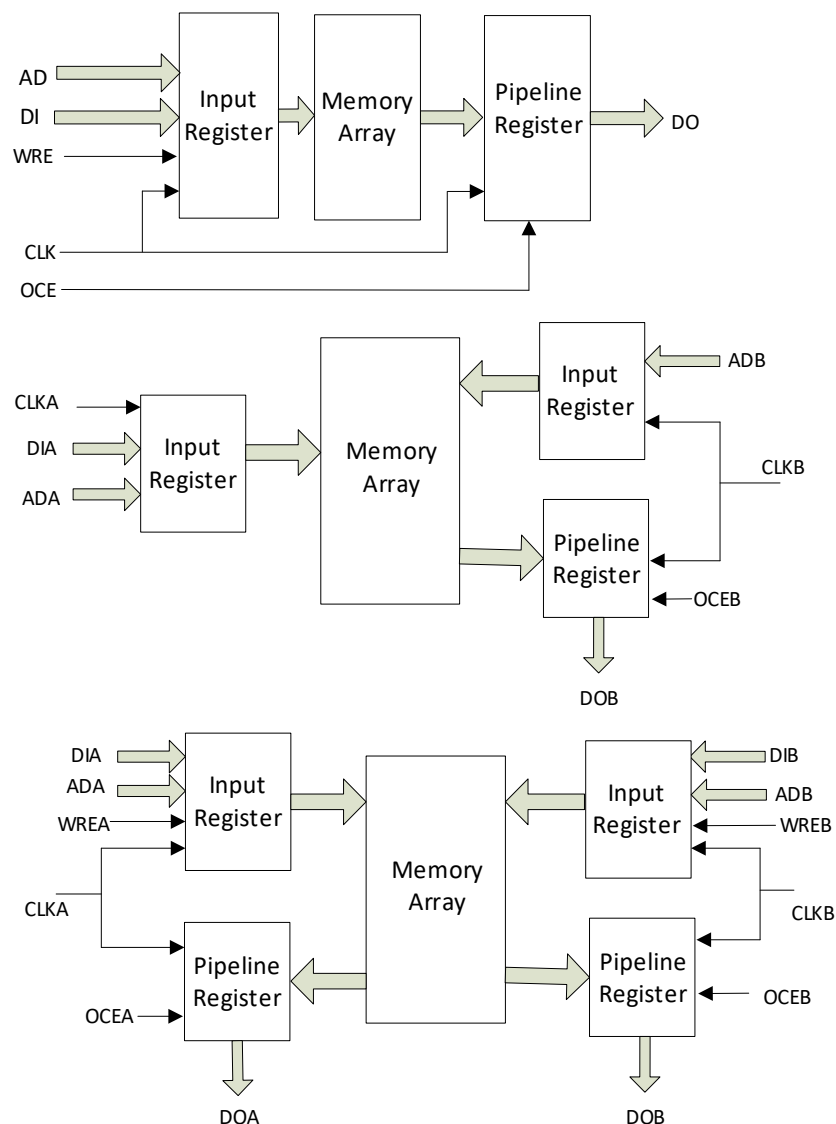
### PIPELINE MODE

When a synchronous write cycles into a memory array with pipeline registers enabled, the data can be read from pipeline registers in the next clock cycle. The data bus can be up to 36 bits in this mode.

### BYPASS MODE

When a synchronous write cycles into a memory array with pipeline registers bypassed, the outputs are registered at the memory array.

**Figure 2-11 Pipeline Mode in Single Port Mode, Dual Port Mode, and Semi-dual Port Mode**



## Write Mode

### NORMAL MODE

In this mode, when you write data to one port, the output data of this port does not change. The written data will not appear at the read port.

**WRITE-THROUGH MODE**

In this mode, when you write data to one port, the written data will appear at the output of this port.

**READ-BEFORE-WRITE MODE**

In this mode, when you write data to one port, the written data will be stored in the memory according to the address, and the original data in this address will appear at the output of this port.

**2.7.7 Clock Mode**

Table 2-8 lists the clock modes in different BSRAM modes:

**Table 2-8 Clock Modes in Different BSRAM Modes**

Clock Mode			Dual Port Mode	Semi-Dual Port Mode	Single Port Mode
Independent Mode	Clock		Yes	No	No
Read/Write Mode	Clock		Yes	Yes	No
Single Port Mode	Port Clock		No	No	Yes

**Independent Clock Mode**

Figure 2-12 shows the independent clocking operations in dual port mode with one clock at each port. CLKA controls all the registers at Port A; CLKB controls all the registers at Port B.

**Figure 2-12 Independent Clock Mode**

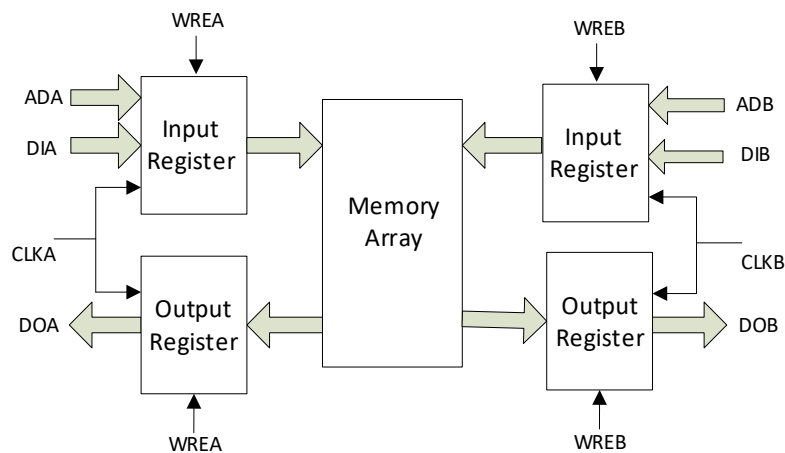
**Read/Write Clock Mode**

Figure 2-13 shows the read/write clocking operations in semi-dual port mode with one clock at each port. The write clock (CLKA) controls data inputs, write addresses and read/write enable signals of Port A. The read clock (CLKB) controls data outputs, read addresses, and read enable signals of Port B.

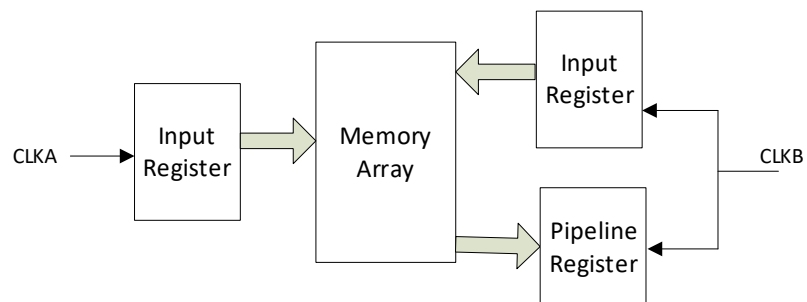
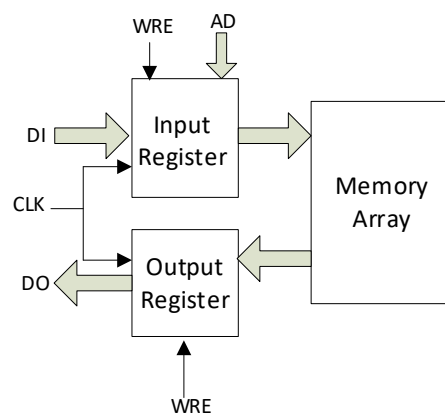
**Figure 2-13 Read/Write Clock Mode****Single Port Clock Mode**

Figure 2-14 shows the clocking operation in single port mode.

**Figure 2-14 Single Port Clock Mode**

## 2.8 User Flash (GW1NSR-4)

The capacity of the User Flash in GW1NSR-4 is 32KB. The User Flash consists of row memories and column memories. One row memory consists of 64 column memories. The capacity of one column memory is 32 bits, and the capacity of one row memory is  $64 \times 32 = 2048$  bits. Page erase is supported, and the capacity of one page is 2048 bytes, that is, one page contains 8 rows. The key features include:

- NOR Flash
- 10,000 write cycles
- Greater than 10 years of data retention at +85°C
- Data width: 32 bits
- Capacity: 128 rows x 64 columns x 32 = 256 Kbits
- Page erase capability: 2,048 bytes per page
- Fast Page Erase/Word Program Operation
- Clock frequency: 40 MHz
- Word Program Time:  $\leq 16\mu\text{s}$
- Page Erase Time:  $\leq 120\text{ ms}$
- Current
  - Read current/duration: 2.19mA/25ns ( $V_{CC}$ ) & 0.5mA/25ns ( $V_{CCX}$ )(MAX)
  - Program/erase operation: 12/12mA(MAX)

For more information about the User Flash in GW1NSR-4, please refer to [UG295, Gowin User Flash User Guide](#). For the correspondence between User Flash primitives and devices supported, please refer to Table 3-1 Devices Supported of [UG295, Gowin User Flash User Guide](#).

## 2.9 Digital Signal Processing

GW1NSR-4C/4 provide abundant DSP resources. Gowin's DSP solutions can address high-performance digital signal processing needs such as FIR and FFT designs. The DSP resources have the advantages of stable timing performance, high resource utilization, and low power consumption.

The DSP resources offer the following functions:

- Multipliers with three widths: 9-bit, 18-bit, 36-bit
- 54-bit ALU
- Multipliers cascading to support wider data widths
- Barrel shifters
- Adaptive filtering through signal feedback
- Computing with options to round to a positive number or a prime

number

- Supports pipeline mode and bypass mode.

## 2.9.1 Macro

The DSP blocks are distributed throughout the FPGA array in the form of rows. Each DSP block contains two macros, and each macro contains two pre-adders, two 18 x 18 bit multipliers, and one three-input ALU.

### Pre-adder

Each DSP macro contains two pre-adders for implementing pre-addition, pre-subtraction, and shifting.

The pre-adders are located at the first stage and have two input ports:

- Parallel 18-bit input B or SBI;
- Parallel 18-bit input A or SIA.

#### Note!

Each input port supports pipeline mode and bypass mode.

Gowin's pre-adders can be used independently as function blocks, which support 9-bit and 18-bit widths.

### Multiplier

The multipliers are located after the pre-adders. The multipliers can be configured as 9 x 9, 18 x 18, 36 x 18, or 36 x 36. Register mode and bypass mode are supported in both input and output ports. The configuration modes that a macro supports include:

- One 18 x 36 multiplier
- Two 18 x 18 multipliers
- Four 9 x 9 multipliers

#### Note!

Two macros can form one 36 x 36 multiplier.

### Arithmetic Logic Unit

Each DSP macro contains one 54-bit ALU, which can further enhance multipliers' functions. Register mode and bypass mode are supported in both input and output ports. The functions include:

- Addition/subtraction operations of multiplier output data/0, data A, and data B.
- Addition/subtraction operations of multiplier output data/0, data B, and carry C.
- Addition/subtraction operations of data A, data B, and carry C.

## 2.9.2 DSP Operation Modes

- Multiplier mode
- Multiply accumulator mode

- Multiply-add accumulator mode

For more information on the DSP resources, see [UG287, Gowin Digital Signal Processing \(DSP\) User Guide](#).

## 2.10 MIPI D-PHY RX/TX Implemented by Using GPIOs

When implementing soft MIPI D-PHY RX/TX with GPIOs, three IO types are available: TLVDS, ELVDS, and MIPI IO.

All GW1NSR FPGAs support the TLVDS/ELVDS types. To implement MIPI D-PHY with the TLVDS/ELVDS types, you need to emulate MIPI HS and MIPI LP by using LVDS25(E)+LVCMOS12 and need to add external resistors.

Some GW1NSR FPGAs support the MIPI IO type. The MIPI IO has an internal resistor network and supports automatic switching between HS and LP. The support list of the MIPI IO type is shown in Table 2-9.

For information on IO type selection and off-chip termination, please refer to “4 Functional Description” in [IPUG948, Gowin MIPI D-PHY RX TX Advance User Guide](#).

Table 2-9 List of GW1NSR series of FPGA Products that Support MIPI IO Type

MIPI Input/Output	GW1NSR-4	GW1NSR-4C
MIPI Input	Bank0/1	Bank0/1
MIPI Output	Bank2	Bank2

The key features of the soft MIPI D-PHY RX/TX include:

- MIPI Alliance Standard for D-PHY Specification, Version 1.2
- High Speed RX and TX at up to 4.8Gbps
- Supports up to 4 data lanes and 1 clock lane
- Supports multiple PHYs(if there are enough IOs available)
- Supports bidirectional low-power (LP) mode
- Supports MIPI DSI and MIPI CSI-2 link layers
- Supports built-in HS Sync, bit and lane alignment
- Supports MIPI D-PHY RX 1:8 and 1:16 deserialization modes
- Supports IO Types of ELVDS, TLVDS, MIPI IO, etc.
- Bank0/Bank1/Bank2 of GW1NSR-4C/4 support I3C

For more information, see [IPUG948, Gowin MIPI D-PHY RX TX Advance User Guide](#).

## 2.11 Cortex-M3

### 2.11.1 Introduction

GW1NSR-4C is a system-on-chip FPGA device that incorporates a microprocessor system hard core, Gowin FPGA fabric, and other standard peripherals and hard cores, including BSRAM resources and PLL/OSC clocking resources. The embedded microprocessor system contains a

low-power, low-cost and high-performance ARM Cortex-M3 32-bit RISC core. The flexible FPGA fabric serves as user programmable peripherals, or soft-core IPs.

The embedded microprocessor system consists of a processor block and an associated bus system that connects to standard peripherals. The FPGA fabric contains rich programmable logic resources offering a flexible architecture that allows the user to achieve multiple peripherals by calling soft-core IPs, such as SPI, I<sup>2</sup>C. The microprocessor system only interfaces with the FPGA fabric and JTAG config-core internally with no access to the I/O blocks of GW1NSR-4C.

The bus system consists of an AHB-Lite Bus, an AHB2APB bridge bus, and two APB buses (APB1 and APB2).

The microprocessor system accesses the FPGA sub-memory system through the AHB bus. The system includes a controller that implements read-only operations of 32KB of Flash resources and read/write operations of a maximum of 16KB of BSRAM resources. Upon Power-On boot loading, Cortex-M3 loads instructions and data that are pre-stored in the Flash-ROM before initiating the execution.

In addition, there are two AHB bus extension ports: INTEXP0 and TARGEXP0. Each of these AHB extension ports provides a 128-bit AHB bus interconnecting to any high-speed User programmable peripherals implemented within the FPGA. A GPIO block interconnects the AHB bus with the FPGA fabric to allow the user to implement general purpose I/O functions in the FPGA.

In terms of the two APB Bus (APB1 and APB2), APB1 interconnects with two timers (Timer0 and Timer1), two UARTs (Uart0 and Uart1), and one watchdog. The two UARTs connect to the FPGA directly. The two timers and the watchdog are controlled and used within the microprocessor system and are accessed through registers. The APB2 bus connects directly to the FPGA.

The processor block consists of a Cortex-M3 core, bus matrix, Nested Vector Interrupt Controller (NVIC), Debug Access Port (DAP), and time stamp, etc.

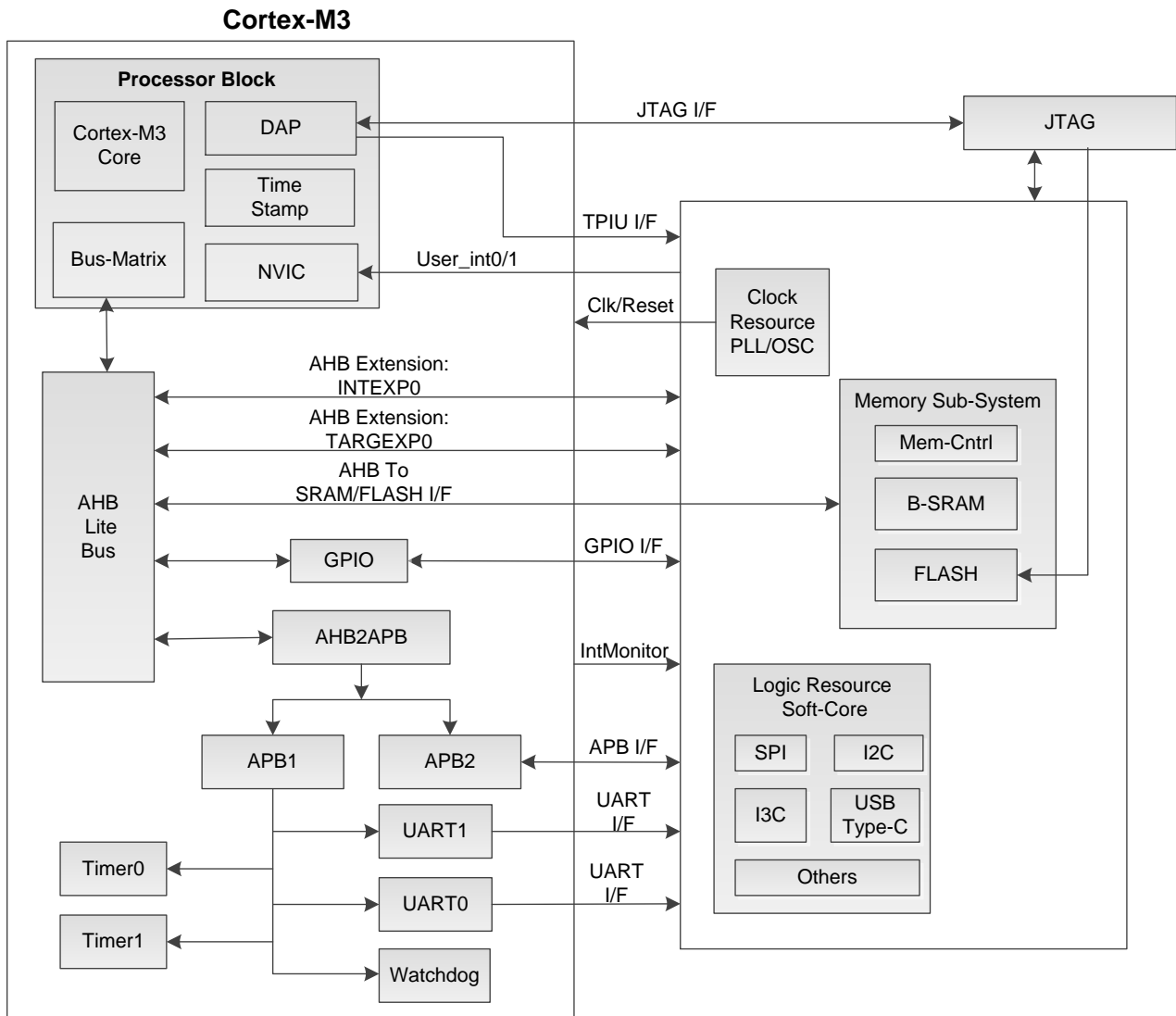
The Cortex-M3 core accesses the bus system through the bus matrix.

Six user interrupts are supported. The DAP contains the JTAG DAP and the Trace-Port-Interface-Unit (TPIU).

The microprocessor system also provides an interrupt monitor signal, which combines GPIO interrupts as well as APB1 peripherals (UART0, UART1, Timer0, Timer1, Watchdog) interrupts, back to the FPGA fabric to report the current run-time interrupt status of the microprocessor system. FPGA fabric takes advantage of its rich Clocking Resource (PLL, OSC) and provides the Main Clock, Power-On Reset and System Reset signals to the embedded microprocessor system.

See Figure 2-15 for the Cortex-M3 architecture.

Figure 2-15 Cortex-M3 Architecture



### 2.11.2 Cortex-M3

#### Features

- Compact core
- Thumb-2 instruction set, delivering the high-performance expected of an ARM core
- Associated with 32 bits and 16 bits devices; typically, in the range of a few kilobytes of memory for microcontroller class applications
- Rapid application execution through Harvard architecture characterized by separate buses for instructions and data
- Exception and Interrupt handling, implemented through register operations
- Deterministic, fast interrupt processing
- Memory protection unit (MPU), providing a privileged mode for protecting operation system functionality



- Migration from the ARM7 processor family for better performance and power efficiency
- Full-featured debug solution
  - JTAG Debug Port
  - Flash Patch and Breakpoint (FPB) unit for implementing breakpoints
  - Data Watchpoint and Trigger (DWT) unit for implementing watchpoints, trigger resources, and system profiling
  - Instrumentation Trace Macrocell (ITM) for printf style debugging
  - Trace Port Interface Unit (TPIU) for bridging to a Trace Port

### 2.11.3 Bus-Matrix

The bus-matrix is used to connect the Cortex-M3 processor and debug port with an external AHB bus. **Connections between the bus-matrix and the AHB bus:**

- ICode bus: 32bit AHBLite bus, used for fetching instructions and vectors from code space.
- DCode bus: 32bit AHBLite bus, used for data loading/storage and debug access.
- System bus: 32bit AHBLite bus, used for fetching instructions and vectors from system space, data loading/storage and debug access.
- APB: 32bit APB bus, used for external space data loading/storage and debug access.

The bus-matrix also controls the following functions.

- Unaligned accesses: converts the unaligned processor access to aligned access.
- Bit-banding: converts the alias access of Bit\_band to Bit\_band space access.
- Write buffer: the bus-matrix contains one write-buffer, ensuring that the processor core is not affected by bus delay.

### 2.11.4 NVIC

The features of NVIC include:

- Supports up to 26 interrupts
- Supports 6 user interrupts
- A programmable priority level of 0-7 for each interrupt. A higher level corresponds to a lower priority; as such level 0 is the highest interrupt priority
- Level and pulse detection of interrupt signals
- Dynamic reprioritization of interrupts
- The processor automatically stacks its state on exception entry and

unstacks this state on exception exit, with no instruction overhead

**Table 2-10 NVIC Interrupt Vector Table**

Address	Name	Type	Description
0x00000000	_StackTop	Read only	Top of interrupt stack
0x00000004	Reset_Handler	Read only	Reset interrupt
0x00000008	NMI_Handler	Read only	NMI interrupt
0x0000000C	HardFault_Handler	Read only	Hard fault interrupt
0x00000010	MemMange_Handler	Read only	MPU fault interrupt
0x00000014	BusFault_Handler	Read/Wr ite	Bus fault interrupt
0x00000018	UsageFault_Handler	Read only	Usage fault interrupt
0x0000002C	SVC_Handler	Read/Wr ite	SVCall interrupt
0x00000030	DebugMon_Handler	Read only	Debug monitor interrupt
0x00000038	PendSV_Handler	Read/ Write/ Read only	Pending interrupt
0x0000003C	SysTick_Handler	Read/Wr ite	System timer interrupt
External interrupt			
0x00000040	UART0_Handler	Read/Wr ite	UART0 receive and transmit interrupt
0x00000044	USER_INT0_Handler	Read/Wr ite	User interrupt 0
0x00000048	UART1_Handler	Read/Wr ite	UART1 receive and transmit interrupt
0x0000004C	USER_INT1_Handler	Read/Wr ite	User interrupt 1
0x00000050	USER_INT2_Handler	Read/Wr ite	User interrupt 2
0x00000058	PORT0_COMB_Handler	Read/Wr ite	GPIO0 interrupt
0x0000005C	USER_INT3_Handler	Read/Wr ite	User interrupt 3
0x00000060	TIMER0_Handler	Read/Wr ite	TIMER0 interrupt
0x00000064	TIMER1_Handler	Read/Wr ite	TIMER1 interrupt
0x0000006C	I2C_Handler	Read/Wr ite	I2C interrupt
0x00000070	UARTOVF_Handler	Read/Wr ite	UART0/UART1 overflow interrupt
0x00000074	USER_INT4_Handler	Read/Wr ite	User interrupt 4
0x00000078	USER_INT5_Handler	Read/Wr ite	User interrupt 5

Address	Name	Type	Description
0x00000080	PORT0_0_Handler	Read/Wr ite	GPIO0 pin0 interrupt
0x00000084	PORT0_1_Handler	Read/Wr ite	GPIO0 pin1 interrupt
0x00000088	PORT0_2_Handler	Read/Wr ite	GPIO0 pin2 interrupt
0x0000008C	PORT0_3_Handler	Read/Wr ite	GPIO0 pin3 interrupt
0x00000090	PORT0_4_Handler	Read/Wr ite	GPIO0 pin4 interrupt
0x00000094	PORT0_5_Handler	Read/Wr ite	GPIO0 pin5 interrupt
0x00000098	PORT0_6_Handler	Read/Wr ite	GPIO0 pin6 interrupt
0x0000009C	PORT0_7_Handler	Read/Wr ite	GPIO0 pin7 interrupt
0x000000A0	PORT0_8_Handler	Read/Wr ite	GPIO0 pin8 interrupt
0x000000A4	PORT0_9_Handler	Read/Wr ite	GPIO0 pin9 interrupt
0x000000A8	PORT0_10_Handler	Read/Wr ite	GPIO0 pin10 interrupt
0x000000AC	PORT0_11_Handler	Read/Wr ite	GPIO0 pin11 interrupt
0x000000B0	PORT0_12_Handler	Read/Wr ite	GPIO0 pin12 interrupt
0x000000B4	PORT0_13_Handler	Read/Wr ite	GPIO0 pin13 interrupt
0x000000B8	PORT0_14_Handler	Read/Wr ite	GPIO0 pin14 interrupt
0x000000BC	PORT0_15_Handler	Read/Wr ite	GPIO0 pin15 interrupt

### 2.11.5 Boot Loader

The boot loader loads the initial stack pointer value from the program memory, and branches to the reset handler that the reset vector specifies in the program memory.

The current boot loader is based on UART Message Monitor which is easy to interface as a communication port with PC host. Below is an example of how to deploy the boot loader:

- Power-on reset to enter the reset handler to call the boot loader.
- Set UART0 registers, such as BAUDIV and CTRL, to configure the appropriate baud rate for transmission and reception.
- Begin Flash loader subroutine execution such as memory test, timer0, and timer1 tests etc.
- Write a 0x4 character (EOP) to terminate the program.

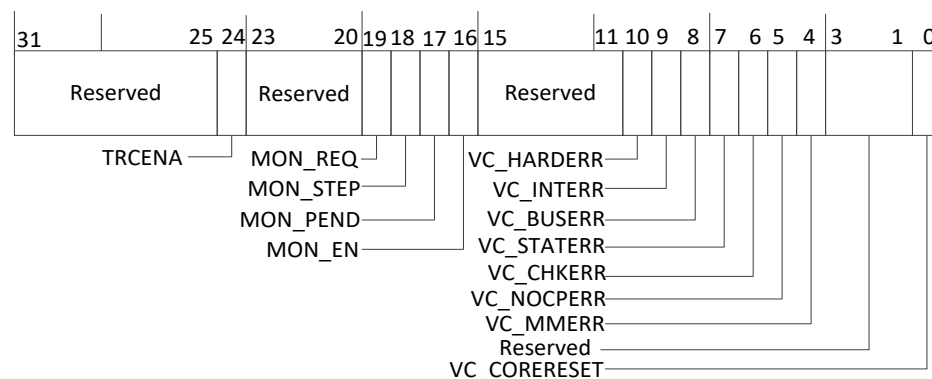
### 2.11.6 TimeStamp

A 48-bit timestamp counter is included in the ITM. It is clock gated and

enabled by the Trace Enable (TRCENA) bit of DEMCR (Debug Exception and monitor control register), which is a global enable bit that enables both the Data Watch Trace (DWT) and Instrumentation Trace Module (ITM) on behalf of the debug of the Cortex-M3 microprocessor. The time stamp generator is used during the debug process to set up the break point and marching step, etc.

**Figure 2-16 DEMCR Register**

**DEMCR寄存器**



**Note!**

TRCENA is the global enable for DWT and ITM:

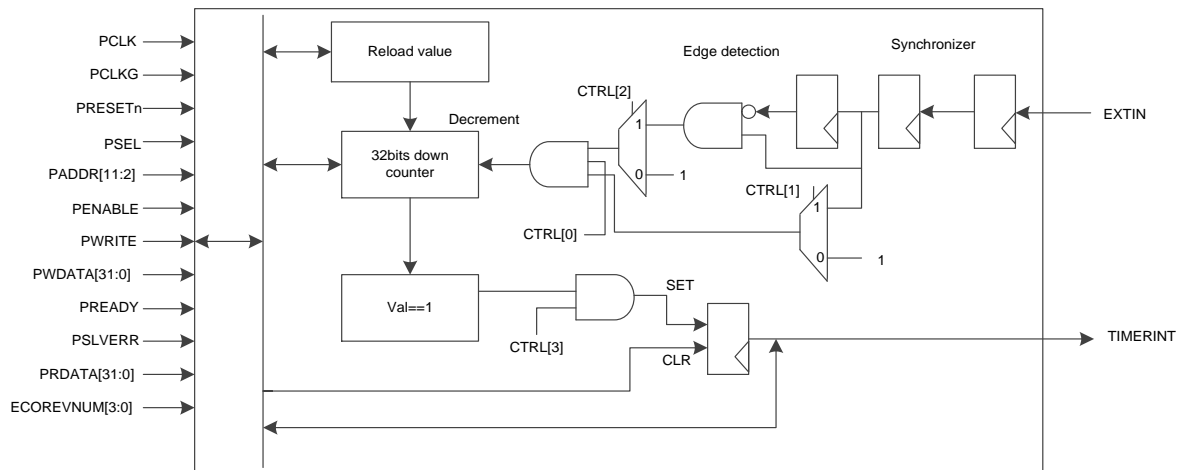
- 0: DWT and ITM units disabled.
- 1: DWT and ITM units enabled.

## 2.11.7 Timer

GW1NSR-4C offers an embedded microprocessor system that contains two synchronous standard timers: Timer0 and Timer1. These can be accessed and controlled through the APB1 bus.

Timer0 and Timer1 are 32-bit down-counters with the following features:

- Users can generate an interrupt request signal, TIMERINT, when the counter reaches 0. The interrupt request is held until it is cleared by writing to the INTCLEAR Register.
- Users can employ the zero-to-one transition of the external input signal, EXTIN, as a timer enable.
- If the timer count reaches 0 and, at the same time, the software clears a previous interrupt status, the interrupt status is set to 1.
- The external clock, EXTIN, must be slower than half of the peripheral clock because it is sampled by a double flip-flop before going through edge-detection logic when the external inputs act as a clock.
- Timer0: EXTIN is hard-wired to GPIO[1].
- Timer1: EXTIN is hard-wired to GPIO[6].

**Figure 2-17 Timer0/Timer1 Structure View**

The Timer0/Timer1 registers are shown in the following table. The base address of Timer0 is 0x40000000 and the base address of Timer1 is 0x40001000.

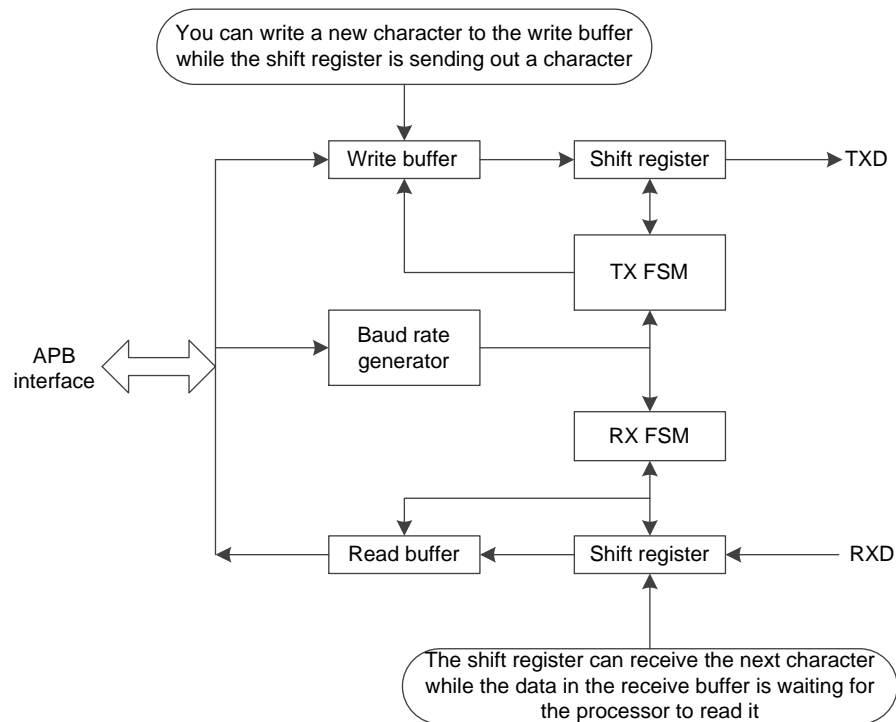
**Table 2-11 Timer0/ Timer1 Registers**

Name	Base Offset	Type	Width	Reset Value	Description
CTRL	0x000	Read/Write	4	0x0	[3]: System timer interrupt enable [2]: Select external input as clock [1]: Select external input as enable [0]: Enable
VALUE	0x004	Read/Write	32	0x00000000	Current value
RELOAD	0x008	Read/Write	32	0x00000000	Reload value. Write to this register to set the current value.
INTSTATUS/ INTCLEAR	0x00C	Read/Write	1	0x0	[0]: Timer interrupt. Write 1 to clear.

### 2.11.8 UART

The microprocessor system of GW1NSR-4C is embedded with two UARTs: UART0 and UART1. These can be accessed and controlled through the APB1 bus. The max. baud rate supported is 921.6Kbits/s.

UART0 and UART1 support 8 bits communication without parity and one stop bit.

**Figure 2-18 APB UART Buffering**

UART0 and UART support a high-speed test mode. When CTRL[6] is set to 1, the serial data is transmitted at one bit per clock cycle. This enables you to send text messages in a much shorter simulation time. The APB interface always sends an “OK” response with no wait state. You must program the baud rate divider register BAUDDIV before enabling the UART.

The BAUDTICK output pulses at a frequency of 16 times that of the programmed baud rate. You can use this external signal for capturing UART data in a synchronous environment. The TXEN output signal indicates the status of CTRL[0]. You can use this signal to switch a bidirectional I/O pin in a silicon device to UART data output mode automatically when the UART transmission feature is enabled.

The buffer overrun status in the STATE field is used to drive the overrun interrupt signals. Therefore, clearing the buffer overrun status de-asserts the overrun interrupt, and clearing the overrun interrupt bit also clears the buffer overrun status bit in the STATE field.

The UART0/UART1 registers are shown in the following table. The base address of UART0 is 0X40004000 and the base address of UART1 is 0X40005000.

**Table 2-12 UART0/ UART1 Registers**

Name	Base Offset	Type	Width	Reset Value	Description
DATA	0x000	Read/Write	8	0x--	8-bit data Read: received data. Write: transmitted data.
STATE	0x004	Read/Write	4	0x0	[3]: RX buffer overrun, write 1 to clear. [2]: TX buffer overrun, write 1 to clear. [1]: RX buffer full, read-only. [0]: TX buffer full, read-only.
CTRL	0x008	Read/Write	7	0x00	[6]: High-speed test mode for TX only. [5]: RX overrun interrupt enable. [4]: TX overrun interrupt enable. [3]: RX interrupt enable. [2]: TX interrupt enable. [1]: RX enable. [0]: TX enable.
INTSTATUS/ INTCLEAR	0x00C	Read/Write	4	0x0	[3]: RX overrun interrupt, write 1 to clear. [2]: TX overrun interrupt, write 1 to clear. [1]: RX interrupt, write 1 to clear. [0]: TX interrupt, write 1 to clear.
BAUDDIV	0x010	Read/Write	20	0x00000	[19:0]: Baud rate divider. The minimum number is 16.

### 2.11.9 Watchdog

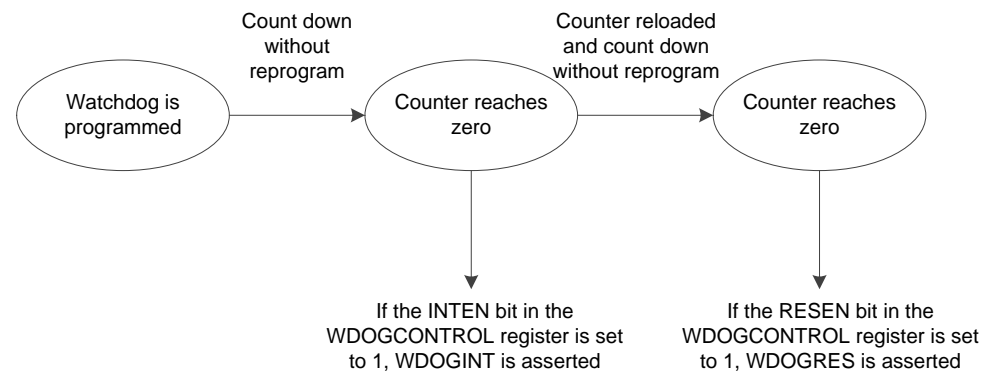
The microprocessor system of GW1NSR-4C is embedded with a watchdog, which can be accessed and controlled through the APB1 bus.

The watchdog module is based on a 32-bit down-counter that is initialized from the reload register, WDOGLOAD.

The watchdog module generates a regular interrupt, WDOGINIT, depending on a programmed value. The counter decrements by one on each positive clock edge of WDOGCLK when the clock enable, WDOGCLKEN, is active high. The watchdog monitors the interrupt and asserts a reset request WDOGRES signal when the counter reaches 0, and the counter is stopped. On the next enabled WDOGCLK clock edge, the counter is reloaded from the WDOGLOAD register and the countdown sequence continues.

The watchdog module applies a reset to a system in the event of a software failure, providing a way to recover from software crashes. For example, if the interrupt is not cleared and the counter reaches 0 again, the watchdog module triggers a system reset.

The Watchdog operation is shown in the following figure.

**Figure 2-19 Watchdog Operation**

The watchdog registers are shown in the following table. The watchdog base address is 0x40008000.

**Table 2-13 Watchdog Registers**

Name	Base Offset	Type	Width	Reset Value	Description
WDOGLOAD	0x00	Read/Write	32	0xFFFFFFFF	Watchdog Load Register
WDOGVALUE	0x04	Read only	32	0xFFFFFFFF	Watchdog Value Register
WDOGCONTROL	0x08	Read/Write	2	0x0	Watchdog Control Register [1]: [0]:
WDOGINTCLR	0x0C	Write only	-	0x-	Watchdog Interrupt Clear Register
WDOGRIS	0x10	Read only	1	0x0	Watchdog Raw Interrupt Status Register
WDOGMIS	0x14	Read only	1	0x0	Watchdog Interrupt Status Register
WDOGLOCK	0xC00	Read/Write	32	0x0	Watchdog Lock Register
WDOGTCR	0xF00	Read/Write	1	0x0	Watchdog Integration Test Control Register
WDOGTOP	0xF04	Write only	2	0x0	Watchdog Integration Test Output Set Register
WDOGPERIPHID4	0XFD0	Read only	8	0x04	Peripheral ID Register 4
WDOGPERIPHID5	0XFD4	Read only	8	0x00	Peripheral ID Register 5
WDOGPERIPHID6	0XFD8	Read only	8	0x00	Peripheral ID Register 6
WDOGPERIPHID7	0XFDC	Read only	8	0x00	Peripheral ID Register 7
WDOGPERIPHID0	0XFE0	Read only	8	0x24	Peripheral ID Register 0
WDOGPERIPHID1	0XFE4	Read only	8	0XB8	Peripheral ID Register 1
WDOGPERIPHID2	0XFE8	Read only	8	0X1B	Peripheral ID Register 2
WDOGPERIPHID3	0XFEC	Read only	8	0X00	Peripheral ID Register 3



Name	Base Offset	Type	Width	Reset Value	Description
WDOGPCELLID0	0XFF0	Read only	8	0X0D	Component ID Register 0
WDOGPCELLID1	0XFF4	Read only	8	0XF0	Component ID Register 1
WDOGPCELLID2	0XFF8	Read only	8	0X05	Component ID Register 2
WDOGPCELLID3	0XFFC	Read only	8	0XB1	Component ID Register 3

### 2.11.10 GPIO

The microprocessor system of GW1NSR-4C communicates with the GPIO block through the AHB bus. The GPIO block interconnects with the FPGA. The GPIO block provides a 16-bit I/O interface with the following features:

- Programmable interrupt generation capability. You can configure each bit of the I/O pins to generate interrupts.
- Bit masking supports the use of address values.
- Registers for alternate function switching with pin multiplexing support.
- Thread safe operation by providing separate set and clear addresses for control registers.

The GPIO registers are shown in the following table. The base address of GPIO is 0x40010000.

**Table 2-14 GPIO Registers**

Name	Base Offset	Type	Width	Reset Value	Description
DATA	0x0000	Read/Write	16	0x----	Data value [15:0]
DATAOUT	0x0004	Read/Write	16	0x0000	Data output register value [15:0]
OUTENSET	0x0010	Read/Write	16	0x0000	Output enable set [15:0] Write 1: Sets the output enable bit. Write 0: No effect. Read 1: Indicates the signal direction as output. Read 0: Indicates the signal direction as input.
OUTENCLR	0x0014	Read/Write	16	0x0000	Output enable clear [15:0]
ALTFUNCSET	0x0018	Read/Write	16	0x0000	Alternative function set [15:0] Write 1: Sets the ALTFUNC bit. Write 0: No effect. Read 0: GPIO as I/O Read 1: ALTFUNC Function
ALTFUNCCLR	0x001C	Read/Write	16	0x0000	Alternative function clear [15:0]
INTENSET	0x0020	Read/Write	16	0x0000	Interrupt enable set [15:0] Write 1: Sets the enable bit. Write 0: No effect.

Name	Base Offset	Type	Width	Reset Value	Description
					Read 0: Interrupt disabled. Read 1: Interrupt enabled.
INTENCLR	0x0024	Read/Write	16	0x0000	Interrupt enable clear [15:0] Write 1: Clears the enable bit. Write 0: No effect. Read 0: Interrupt disabled. Read 1: Interrupt enabled.
INTTYPESET	0x0028	Read/Write	16	0x0000	Interrupt type set [15:0]
INTTYPECLR	0x002C	Read/Write	16	0x0000	Interrupt type clear [15:0]
INTPOLSET	0x0030	Read/Write	16	0x0000	Interrupt polarity set [15:0]
INTPOLCLR	0x0034	Read/Write	16	0x0000	Interrupt polarity clear [15:0]
INTSTATUS/ INTCLEAR	0x0038	Read/Write	16	0x0000	Read interrupt status register Write 1: Clears the interrupt request
MASKLOWBYTE	0x0400- 0x07FC	Read/Write	16	0x0000	–
MASKHIGHBYTE	0x0800- 0x0BFC	Read/Write	16	0x0000	–
Reserved	0x0C00- 0x0FCF	–	–	–	Reserved

### 2.11.11 Debug Access Port

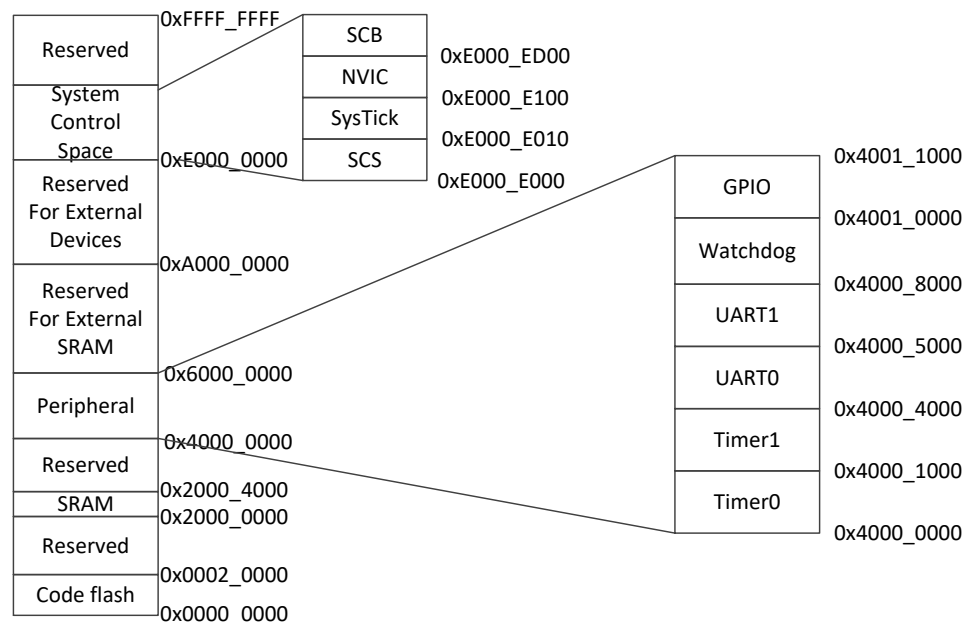
The Cortex-M3 processor contains a DAP that consists of a JTAG interface and a TPIU interface. Both of them interface to the FPGA Fabric. The JTAG-DAP is based on the IEEE1149.1 Joint Test Action Group Boundary-Scan Standard.

JTAG-DP functions consist of the following three parts:

- JTAG-DP state machine
- Instruction register (IR) and the related IR scan chain, which are used to control JTAG and the current register actions
- DR register and the related DR scan chain, which connect with the JTAG-DP register.

## 2.11.12 Memory Mapping

Figure 2-20 Memory Mapping



## 2.11.13 Application

The Gowin software supports the call of Cortex-M3. For more information, please refer to [IPUG932, Gowin EMPU\(GW1NS-4C\) Hardware Design Reference Manual](#).

## 2.12 Clocks

The clock resources and wiring are critical for high-performance applications in FPGA. The GW1NSR series of FPGA products provide global clocks (GCLKs) which connect to all the registers directly. In addition, high-speed clocks (HCLKs), PLLs, etc. are provided.

For more information on the GCLKs, HCLKs, PLLs, see [UG286, Gowin Clock User Guide](#).

### 2.12.1 Global Clocks

The Global Clock(GCLK) resources are distributed across multiple quadrants within the GW1NSR series of FPGA products (Automotive). Each quadrant provides eight GCLKs. The clock sources of GCLKs include dedicated clock input pins and CRUs, and better clock performance can be achieved by using the dedicated clock input pins.

### 2.12.2 PLLs

The PLL (Phase-locked Loop) is a feedback control circuit. The frequency and phase of the internal oscillator signal are controlled by the external input reference clock.

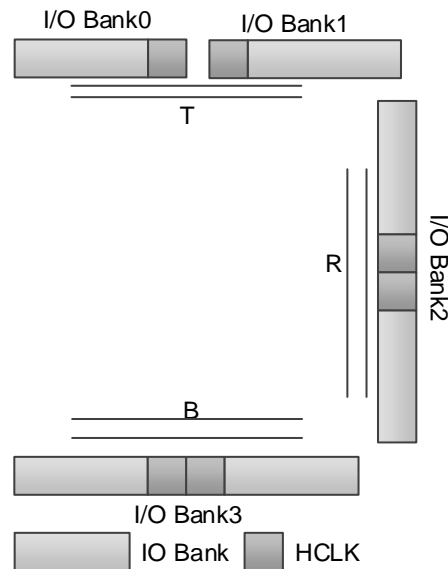
PLLs in the GW1NSR series of FPGA products can provide synthesizable clock frequencies. Frequency adjustment (multiplication and

division), phase adjustment, and duty cycle adjustment can be achieved by configuring the parameters.

### 2.12.3 High-speed Clocks

The high-speed clocks (HCLKs) are designed to facilitate high-performance I/O data transmission and are specifically tailored for source synchronous data transmission protocols. The GW1NSR-4C/4 devices have two HCLKs on each side, see Figure 2-21.

Figure 2-21 GW1NSR-4/4C HCLK Distribution



## 2.13 Long Wires

As a supplement to the CRU, the GW1NSR series of FPGA products provide another kind of routing resource - the long wire, which can be used for clock, clock enable, set/reset, or other high fan-out signals.

## 2.14 Global Set/Reset

The GW1NSR series of FPGA products offer a dedicated global set/reset (GSR) network that connects directly to the device's internal logic and can be used as asynchronous/synchronous set or asynchronous/synchronous reset, with the registers in the CLUs and I/Os being able to be configured independently.

## 2.15 Programming & Configuration

The GW1NSR series of FPGA products support SRAM configuration and Flash programming. Flash programming includes on-chip Flash programming and off-chip Flash programming.

In addition to JTAG, the GW1NSR series of FPGA products also support Gowin's own GowinCONFIG configuration modes: AUTO BOOT, SSPI, MSPI, DUAL BOOT, SERIAL, and CPU. All the GW1NSR FPGAs support JTAG mode and AUTO BOOT mode. For more information, please refer to UG290, Gowin FPGA Products Programming and Configuration User Guide.

### 2.15.1 SRAM Configuration

If SRAM configuration is used, the configuration data needs to be re-downloaded after each power-up.

### 2.15.2 Flash Programming

The Flash programming data is stored in the on-chip Flash. Each time the device is powered up, the configuration data is transferred from the Flash to the SRAM. Configuration can be completed within a few milliseconds after power-up, which is why this kind of configuration is also known as "instant on".

In addition, the GW1NSR series of FPGA products support off-chip Flash programming and DUAL BOOT. For more information, please refer to UG290, Gowin FPGA Products Programming and Configuration User Guide.

The GW1NSR series of FPGA products support the feature of background upgrade. That is to say, you can program the on-chip Flash or off-chip Flash via the JTAG<sup>[1]</sup> interface without affecting the current working state. During programming, the device works according to the previous configuration. After the programming is done, you can trigger RECONFIG\_N<sup>[2]</sup> with a low level to complete the upgrade. This feature is suitable for the applications requiring long online time and irregular upgrades.

**Note!**

- <sup>[1]</sup>For the GW1NSR-4C device, the JTAG background upgrade feature is not available if its embedded Cortex-M3 is used.
- <sup>[2]</sup> As a configuration pin, RECONFIG\_N is an input pin with internal weak pull-up, but as a GPIO, RECONFIG\_N can only be used for output. For more information, please refer to UG290, Gowin FPGA Products Programming and Configuration User Guide.

## 2.16 On-chip Oscillator

The GW1NSR series of FPGA products have an embedded programmable on-chip clock oscillator which provides a clock source for the MSPI configuration mode with a tolerance of  $\pm 5\%$ .

The on-chip oscillator of the GW1NSR-4C/4 device supports user-

configurable power saving mode.

The on-chip oscillator also provides a clock resource for user designs. Up to 64 clock frequencies can be obtained by setting the parameters.

The following formula is used to get the output clock frequency of the on-chip oscillator of GW1NSR-4C/4:

$$f_{\text{out}} = f_{\text{osc}} / \text{Param}$$

**Note!**

For C7/I6 speed grade devices,  $f_{\text{osc}}$  is 260MHz; for other speed grade devices,  $f_{\text{osc}}$  is 250MHz. "Param" should be even numbers from 2 to 128.

The table below lists some frequencies provided by the on-chip oscillator for  $f_{\text{osc}} = 250 \text{ MHz}$ .

**Table 2-15 Output Frequency Options of the On-chip Oscillator of GW1NSR-4/4C**

Mode	Frequency	Mode	Frequency	Mode	Frequency
0	2.5MHz <sup>[1]</sup>	8	7.8MHz	16	15.6MHz
1	5.4MHz	9	8.3MHz	17	17.9MHz
2	5.7MHz	10	8.9MHz	18	21MHz
3	6.0MHz	11	9.6MHz	19	25MHz
4	6.3MHz	12	10.4MHz	20	31.3MHz
5	6.6MHz	13	11.4MHz	21	41.7MHz
6	6.9MHz	14	12.5MHz	22	62.5MHz
7	7.4MHz	15	13.9MHz	23	125MHz <sup>[2]</sup>

**Note!**

- <sup>[1]</sup> Default frequency.
- <sup>[2]</sup> This is not available for the MSPI configuration mode.

# 3 DC and Switching Characteristics

## Note!

Please ensure that you use Gowin's devices within the recommended operating conditions and ranges. Data beyond the working conditions and ranges are for reference only. Gowin does not guarantee that all devices will operate normally beyond the operating conditions and ranges.

## 3.1 Operating Conditions

### 3.1.1 Absolute Max. Ratings

Table 3-1 Absolute Max. Ratings

Name	Description	Min.	Max.
V <sub>CC</sub>	Core voltage	-0.5V	1.32V
V <sub>CCIOx</sub>	I/O Bank voltage	-0.5V	3.75V
V <sub>CCX</sub>	Auxiliary voltage(LV version)	-0.5V	3.75V
-	I/O voltage applied <sup>[1]</sup>	-0.5V	3.75V
Storage Temperature	Storage temperature	-65°C	+150°C
Junction Temperature	Junction temperature	-40°C	+125°C

## Note!

<sup>[1]</sup> Overshoot and undershoot of -2V to (V<sub>IHMAX</sub> + 2)V are allowed for a duration of <20 ns.

### 3.1.2 Recommended Operating Conditions

Table 3-2 Recommended Operating Conditions

Name	Description	Min.	Max.
V <sub>CC</sub>	Core voltage	1.14V	1.26V
V <sub>CCX</sub>	Auxiliary voltage(LV version)	1.71V	3.6V
V <sub>CCIOx</sub>	I/O Bank voltage (LV version)	1.14V	3.6V
T <sub>JCOM</sub>	Junction temperature for commercial operations	0°C	+85°C
T <sub>JIND</sub>	Junction temperature for industrial operations	-40°C	+100°C

## Note!

- For more information on the power supplies, please refer to [UG864, GW1NSR-4 Pinout](#) and [UG865, GW1NSR-4C Pinout](#).

- The allowable ripples on  $V_{CC}$ ,  $V_{CCIO}$ , and  $V_{CCX}$  are 3%, 5%, and 5% respectively. 1). For devices of which the PLL is powered directly with  $V_{CC}$ , the ripple on  $V_{CC}$  can affect the jitter characteristics of the PLL output clock; 2). The ripple on  $V_{CCIO}$  can eventually be passed on to the output waveform of the IO Buffer.

### 3.1.3 Power Supply Ramp Rates

Table 3-3 Power Supply Ramp Rates

Name	Description	Min.	Typ.	Max.
$V_{CC}$ Ramp	Power supply ramp rates for $V_{CC}$	0.6mV/ $\mu$ s	-	6mV/ $\mu$ s
$V_{CCX}$ Ramp	Power supply ramp rates for $V_{CCX}$	0.6mV/ $\mu$ s	-	10mV/ $\mu$ s
$V_{CCIO}$ Ramp	Power supply ramp rates for $V_{CCIO}$	0.1mV/ $\mu$ s	-	10mV/ $\mu$ s

**Note!**

- A monotonic ramp is required for all power supplies.
- All power supplies need to be in the operating range as defined in Table 4-2 before configuration. Power supplies that are not in the operating range need to be adjusted to a faster ramp rate, or you have to delay configuration.

### 3.1.4 Hot Socketing Specifications

Table 3-4 Hot Socketing Specifications

Name	Description	Condition	I/O Type	Max.
$I_{HS}$	Input or I/O leakage current	$0 < V_{IN} < V_{IH}(MAX)$	I/O	150uA
$I_{HS}$	Input or I/O leakage current	$0 < V_{IN} < V_{IH}(MAX)$	TDI, TDO, TMS, TCK	120uA

### 3.1.5 POR Specifications

Table 3-5 POR Parameters

Name	Description	Min.	Max.
POR Voltage	Power on reset voltage of $V_{CC}$	TBD	TBD



## 3.2 ESD performance

Table 3-6 GW1NSR ESD - HBM

Device	QN48	MG64
GW1NSR-4C	HBM>1,000V	HBM>1,000V
GW1NSR-4	-	HBM>1,000V

Table 3-7 GW1NSR ESD - CDM

Device	QN48	MG64
GW1NSR-4C	CDM>500V	CDM>500V
GW1NSR-4	-	CDM>500V

## 3.3 DC Electrical Characteristics

### 3.3.1 DC Electrical Characteristics over Recommended Operating Conditions

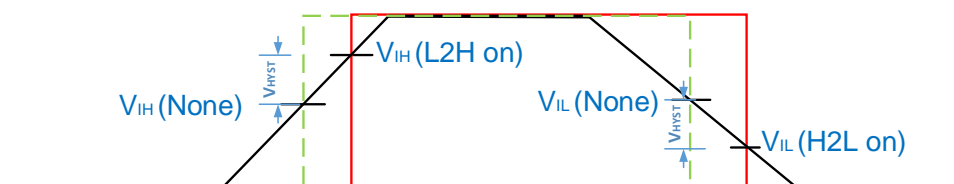
Table 3-8 DC Electrical Characteristics over Recommended Operating Conditions

Name	Description	Condition	Min.	Typ.	Max.
$I_{IL}, I_{IH}$	Input or I/O leakage current	$V_{CCIO} < V_{IN} < V_{IH}(\text{MAX})$	-	-	210 $\mu$ A
		$0V < V_{IN} < V_{CCIO}$	-	-	10 $\mu$ A
$I_{PU}$	I/O Active Pull-up Current	$0 < V_{IN} < 0.7V_{CCIO}$	-30 $\mu$ A	-	-150 $\mu$ A
$I_{PD}$	I/O Active Pull-down Current	$V_{IL}(\text{MAX}) < V_{IN} < V_{CCIO}$	30 $\mu$ A	-	150 $\mu$ A
$I_{BHLS}$	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL}(\text{MAX})$	30 $\mu$ A	-	-
$I_{BHHS}$	Bus Hold High Sustaining Current	$V_{IN} = 0.7V_{CCIO}$	-30 $\mu$ A	-	-
$I_{BHLO}$	Bus Hold Low Overdrive Current	$0 \leq V_{IN} \leq V_{CCIO}$	-	-	150 $\mu$ A
$I_{BHHO}$	Bus Hold High Overdrive Current	$0 \leq V_{IN} \leq V_{CCIO}$	-	-	-150 $\mu$ A
$V_{BHT}$	Bus Hold Trip Points		$V_{IL}(\text{MAX})$	-	$V_{IH}(\text{MIN})$
C1	I/O Capacitance			5pF	8pF
$V_{HYST}$	Hysteresis for Schmitt Trigger inputs	$V_{CCIO} = 3.3V$ , Hysteresis= L2H <sup>[1],[2]</sup>	-	200mV	-
		$V_{CCIO} = 2.5V$ , Hysteresis= L2H	-	125mV	-
		$V_{CCIO} = 1.8V$ , Hysteresis= L2H	-	60mV	-
		$V_{CCIO} = 1.5V$ , Hysteresis= L2H	-	40mV	-
		$V_{CCIO} = 1.2V$ , Hysteresis= L2H	-	20mV	-
		$V_{CCIO} = 3.3V$ , Hysteresis= H2L <sup>[1],[2]</sup>	-	200mV	-
		$V_{CCIO} = 2.5V$ , Hysteresis= H2L	-	125mV	-
		$V_{CCIO} = 1.8V$ , Hysteresis= H2L	-	60mV	-
		$V_{CCIO} = 1.5V$ , Hysteresis= H2L	-	40mV	-
		$V_{CCIO} = 1.2V$ , Hysteresis= H2L	-	20mV	-

Name	Description	Condition	Min.	Typ.	Max.
		$V_{CCIO}=3.3V$ , Hysteresis= HIGH <sup>[1],[2]</sup>	-	400mV	-
		$V_{CCIO}=2.5V$ , Hysteresis= HIGH	-	250mV	-
		$V_{CCIO}=1.8V$ , Hysteresis= HIGH	-	120mV	-
		$V_{CCIO}=1.5V$ , Hysteresis= HIGH	-	80mV	-
		$V_{CCIO}=1.2V$ , Hysteresis= HIGH	-	40mV	-

**Note!**

- <sup>[1]</sup> Hysteresis="NONE", "L2H", "H2L", "HIGH" indicates the Hysteresis options that can be set when setting I/O Constraints in the FloorPlanner tool of Gowin EDA, for more details, see [SUG935. Gowin Design Physical Constraints User Guide](#).
- <sup>[2]</sup> Enabling the L2H (low to high) option means raising  $V_{IH}$  by  $V_{HYST}$ ; enabling the H2L (high to low) option means lowering  $V_{IL}$  by  $V_{HYST}$ ; enabling the HIGH option means enabling both L2H and H2L options, i.e.  $V_{HYST}(HIGH) = V_{HYST}(L2H) + V_{HYST}(H2L)$ . The diagram is shown below.



### 3.3.2 Static Current

Table 3-9 Static Current<sup>[1]</sup>

Name	Description	Device type	Device	C7/I6	C6/I5	C5/I4
$I_{CC}$	$V_{CC}$ current ( $V_{CC}=1.2V$ )	LV version	GW1NSR-4/4C	12mA	2.8mA	2.8mA
$I_{CCX}$	$V_{CCX}$ current ( $V_{CCX}=2.5V$ )	LV version	GW1NSR-4/4C	-	1.2mA	1.2mA
	$V_{CCX}$ current ( $V_{CCX}=3.3V$ )	LV version	GW1NSR-4/4C	3mA	-	-
$I_{CCIO}$ <sup>[2]</sup>	$V_{CCIO}$ current ( $V_{CCIO}=2.5V$ )	LV version	GW1NSR-4/4C	1mA	0.7mA	0.7mA

**Note!**

- <sup>[1]</sup> The values in the table are typical values at 25°C.
- <sup>[2]</sup> There are two PSRAMs integrated in GW1NSR-4/4C MG64P, and the  $V_{CCIO}$  static current will increase by  $300\mu A \times 2=600\mu A$  when it is used. There is one HyperRAM integrated in GW1NSR-4C QN48P, and the  $V_{CCIO}$  static current will increase by  $220\mu A$  when it is used. There is one NOR Flash integrated in GW1NSR-4C QN48G, and the  $V_{CCIO}$  static current will increase by  $40\mu A$  when it is used.

### 3.3.3 Recommended I/O Operating Conditions

Table 3-10 Recommended I/O Operating Conditions

Name	V <sub>CCIO</sub> (V) for Output			V <sub>REF</sub> (V) for Input		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVTTTL33	3.135	3.3	3.6	-	-	-
LVC MOS33	3.135	3.3	3.6	-	-	-
LVC MOS25	2.375	2.5	2.625	-	-	-
LVC MOS18	1.71	1.8	1.89	-	-	-
LVC MOS15	1.425	1.5	1.575	-	-	-
LVC MOS12	1.14	1.2	1.26	-	-	-
SSTL15	1.425	1.5	1.575	0.68	0.75	0.9
SSTL18_I	1.71	1.8	1.89	0.833	0.9	0.969
SSTL18_II	1.71	1.8	1.89	0.833	0.9	0.969
SSTL25_I	2.375	2.5	2.645	1.15	1.25	1.35
SSTL25_II	2.375	2.5	2.645	1.15	1.25	1.35
SSTL33_I	3.135	3.3	3.6	1.3	1.5	1.7
SSTL33_II	3.135	3.3	3.6	1.3	1.5	1.7
HSTL18_I	1.71	1.8	1.89	0.816	0.9	1.08
HSTL18_II	1.71	1.8	1.89	0.816	0.9	1.08
HSTL15	1.425	1.5	1.575	0.68	0.75	0.9
PCI33	3.135	3.3	3.6	-	-	-
LVPECL33E	3.135	3.3	3.6	-	-	-
MLVDS25E	2.375	2.5	2.625	-	-	-
BLVDS25E	2.375	2.5	2.625	-	-	-
RSDS25E	2.375	2.5	2.625	-	-	-
LVDS25E	2.375	2.5	2.625	-	-	-
SSTL15D	1.425	1.5	1.575	-	-	-
SSTL18D_I	1.71	1.8	1.89	-	-	-
SSTL18D_II	1.71	1.8	1.89	-	-	-
SSTL25D_I	2.375	2.5	2.625	-	-	-
SSTL25D_II	2.375	2.5	2.625	-	-	-
SSTL33D_I	3.135	3.3	3.6	-	-	-
SSTL33D_II	3.135	3.3	3.6	-	-	-
HSTL15D	1.425	1.575	1.89	-	-	-
HSTL18D_I	1.71	1.8	1.89	-	-	-
HSTL18D_II	1.71	1.8	1.89	-	-	-

### 3.3.4 Single-ended I/O DC Characteristics

Table 3-11 Single-ended I/O DC Characteristics

Name	V <sub>IL</sub>		V <sub>IH</sub>		V <sub>OL</sub> (Max)	V <sub>OH</sub> (Min)	I <sub>OL</sub> <sup>[1]</sup> (mA)	I <sub>OH</sub> <sup>[1]</sup> (mA)
	Min	Max	Min	Max				
LVCMOS33 LVTTTL33	-0.3V	0.8V	2.0V	3.6V	0.4V	V <sub>CCIO</sub> -0.4V	4	-4
							8	-8
							12	-12
							16	-16
							24	-24
					0.2V	V <sub>CCIO</sub> -0.2V	0.1	-0.1
LVCMOS25	-0.3V	0.7V	1.7V	3.6V	0.4V	V <sub>CCIO</sub> -0.4V	4	-4
							8	-8
							12	-12
					0.2V	V <sub>CCIO</sub> -0.2V	0.1	-0.1
LVCMOS18	-0.3V	0.35*V <sub>CCIO</sub>	0.65*V <sub>CCIO</sub>	3.6V	0.4V	V <sub>CCIO</sub> -0.4V	4	-4
							8	-8
							12	-12
					0.2V	V <sub>CCIO</sub> -0.2V	0.1	-0.1
LVCMOS15	-0.3V	0.35*V <sub>CCIO</sub>	0.65*V <sub>CCIO</sub>	3.6V	0.4V	V <sub>CCIO</sub> -0.4V	4	-4
					0.2V	V <sub>CCIO</sub> -0.2V	0.1	-0.1
LVCMOS12	-0.3V	0.35*V <sub>CCIO</sub>	0.65*V <sub>CCIO</sub>	3.6V	0.4V	V <sub>CCIO</sub> -0.4V	4	-4
					0.2V	V <sub>CCIO</sub> -0.2V	0.1	-0.1
PCI33	-0.3V	0.3*V <sub>CCIO</sub>	0.5*V <sub>CCIO</sub>	3.6V	0.1*V <sub>CCIO</sub>	0.9*V <sub>CCIO</sub>	1.5	-0.5
SSTL33_I	-0.3V	V <sub>REF</sub> -0.2V	V <sub>REF</sub> +0.2V	3.6V	0.7	V <sub>CCIO</sub> -1.1V	8	-8
SSTL25_I	-0.3V	V <sub>REF</sub> -0.18V	V <sub>REF</sub> +0.18V	3.6V	0.54V	V <sub>CCIO</sub> -0.62V	8	-8
SSTL25_II	-0.3V	V <sub>REF</sub> -0.18V	V <sub>REF</sub> +0.18V	3.6V	NA	NA	NA	NA
SSTL18_II	-0.3V	V <sub>REF</sub> -0.125V	V <sub>REF</sub> +0.125V	3.6V	NA	NA	NA	NA
SSTL18_I	-0.3V	V <sub>REF</sub> -0.125V	V <sub>REF</sub> +0.125V	3.6V	0.40V	V <sub>CCIO</sub> -0.40V	8	-8
SSTL15	-0.3V	V <sub>REF</sub> -0.1V	V <sub>REF</sub> + 0.1V	3.6V	0.40V	V <sub>CCIO</sub> -0.40V	8	-8
HSTL18_I	-0.3V	V <sub>REF</sub> -0.1V	V <sub>REF</sub> + 0.1V	3.6V	0.40V	V <sub>CCIO</sub> -0.40V	8	-8
HSTL18_II	-0.3V	V <sub>REF</sub> -0.1V	V <sub>REF</sub> + 0.1V	3.6V	NA	NA	NA	NA
HSTL15_I	-0.3V	V <sub>REF</sub> -0.1V	V <sub>REF</sub> + 0.1V	3.6V	0.40V	V <sub>CCIO</sub> -0.40V	8	-8
HSTL15_II	-0.3V	V <sub>REF</sub> -0.1V	V <sub>REF</sub> + 0.1V	3.6V	NA	NA	NA	NA

**Note!**

<sup>[1]</sup> The total DC current limit(sourced and sunk current) of all IOs in the same bank: the total DC current of all IOs in the same bank shall not be greater than n\*8mA, where n represents the number of IOs bonded out from a bank.

### 3.3.5 Differential I/O DC Characteristics

Table 3-12 Differential I/O DC Characteristics (LVDS)

Name	Description	Test conditions	Min.	Typ.	Max.	Unit
$V_{INA}, V_{INB}$	Input Voltage		0	-	2.15	V
$V_{CM}$	Input Common Mode Voltage	Half the Sum of the Two Inputs	0.05	-	2.1	V
$V_{THD}$	Differential Input Threshold	Difference Between the Two Inputs	$\pm 100$	-	$\pm 600$	mV
$I_{IN}$	Input Current	Power On or Power Off	-	-	$\pm 20$	$\mu A$
$V_{OH}$	Output High Voltage for $V_{OP}$ or $V_{OM}$	$R_T = 100\Omega$	-	-	1.60	V
$V_{OL}$	Output Low Voltage for $V_{OP}$ or $V_{OM}$	$R_T = 100\Omega$	0.9	-	-	V
$V_{OD}$	Output Voltage Differential	$(V_{OP} - V_{OM}), R_T = 100\Omega$	250	350	450	mV
$\Delta V_{OD}$	Change in $V_{OD}$ Between High and Low		-	-	50	mV
$V_{OS}$	Output Voltage Offset	$(V_{OP} + V_{OM})/2, R_T = 100\Omega$	1.125	1.20	1.375	V
$\Delta V_{OS}$	Change in $V_{OS}$ Between High and Low		-	-	50	mV
$I_S$	Short-circuit current	$V_{OD} = 0V$ outputs short-circuited	-	-	15	mA

## 3.4 Switching Characteristics

### 3.4.1 CLU Switching Characteristics

Table 3-13 CLU Timing Parameters

Name	Description	Speed Grade		Unit
		Min	Max	
$t_{LUT4\_CLU}$	LUT4 delay	-	0.674	ns
$t_{SR\_CLU}$	Set/Reset to Register output	-	1.86	ns
$t_{CO\_CLU}$	Clock to Register output	-	0.76	ns

### 3.4.2 Clock and I/O Switching Characteristics

Table 3-14 External Switching Characteristics

Name	C5/I4		C6/I5		Unit
	Min	Max	Min	Max	
HCLK Tree delay	0.8	1.4	0.5	1.2	ns
PCLK Tree delay(GCLK0~5)	1.4	2.6	1.0	2.2	ns
PCLK Tree delay(GCLK6~7)	1.8	3.2	1.4	2.9	ns
Pin-LUT-Pin Delay	3.4	5	3	4.5	ns

### 3.4.3 Gearbox Switching Characteristics

Table 3-15 Gearbox Timing Parameters

Name	Description	Typ.	Unit
FMAX <sub>IDDR</sub>	1:2 Gearbox maximum serial input rate	400	Mbps
FMAX <sub>IDES4</sub>	1:4 Gearbox maximum serial input rate	800	Mbps
FMAX <sub>IDES7</sub>	1:7 Gearbox maximum serial input rate	1000	Mbps
FMAX <sub>IDESx</sub>	1:8/1:10/1:16 Gearbox maximum serial input rate	1100	Mbps
FMAX <sub>ODDR</sub>	2:1 Gearbox maximum serial output rate	400	Mbps
FMAX <sub>OSER4</sub>	4:1 Gearbox maximum serial output rate	800	Mbps
FMAX <sub>OSER7</sub>	7:1 Gearbox maximum serial output rate	1000	Mbps
FMAX <sub>OSERx</sub>	8:1/10:1/16:1 Gearbox maximum serial output rate	1100	Mbps

Table 3-16 Single-ended IO Fmax

Name	Fmax	
	Min.(MHz)	
	Drive Strength = 4mA	Drive Strength > 4mA
LVTTL33	150	300
LVC MOS33	150	300
LVC MOS25	150	300
LVC MOS18	150	300
LVC MOS15	150	200
LVC MOS12	150	150

**Note!**

Test load = 30pF.

### 3.4.4 BSRAM Switching Characteristics

Table 3-17 BSRAM Timing Parameters

Name	Description	Speed Grade		Unit
		Min	Max	
t <sub>COAD</sub> _BSRAM	Clock to output time of read address/data	-	5.10	ns
t <sub>COOR</sub> _BSRAM	Clock to output time of output register	-	0.56	ns

### 3.4.5 DSP Switching Characteristics

Table 3-18 DSP Timing Parameters

Name	Description	Speed Grade		Unit
		Min	Max	
t <sub>COIR</sub> _DSP	Clock to output time of input register	-	4.80	ns
t <sub>COPR</sub> _DSP	Clock to output time of pipeline register	-	2.40	ns
t <sub>COOR</sub> _DSP	Clock to output time of output register	-	0.84	ns

### 3.4.6 On-chip Oscillator Switching Characteristics

Table 3-19 On-chip Oscillator Parameters

Name	Description		Min.	Typ.	Max.
f <sub>MAX</sub>	On-chip Oscillator Output Frequency (0 ~ +85°C)	GW1NSR-4/4C	118.75MHz	125MHz	131.25MHz
	On-chip Oscillator Output Frequency (-40 ~ +100°C)	GW1NSR-4/4C	112.5MHz	125MHz	137.5MHz
t <sub>DT</sub>	Output Clock Duty Cycle		43%	50%	57%
t <sub>OPJIT</sub>	Output Clock Period Jitter		0.01UIPP	0.012UIPP	0.02UIPP

### 3.4.7 PLL Switching Characteristics

Table 3-20 PLL Parameters

Device	Speed Grade	Name	Min.	Max.
GW1NSR-4/ GW1NSR-4C	C7/I6 C6/I5	CLKIN	3MHz	400MHz
		PFD	3MHz	400MHz
		VCO	400MHz	1200MHz
		CLKOUT	3.125MHz	600MHz
	C5/I4	CLKIN	3MHz	320MHz
		PFD	3MHz	320MHz
		VCO	320MHz	960MHz
		CLKOUT	2.5MHz	480MHz

## 3.5 Cortex-M3 AC/DC Characteristics

### 3.5.1 DC Electrical Characteristics

Table 3-21 Current Characteristics

Symbol	Description	Specification		Unit
		Min.	Max.	
I <sub>VCC</sub>	Max. current of VCC	-	100	mA
I <sub>VSS</sub>	Max. current of VSS	-	-100	mA
I <sub>INJ</sub>	Leakage current	-	+/-5	mA

### 3.5.2 AC Electrical Characteristics

Table 3-22 Clock Parameters

Symbol	Description	Device	Specification		Unit
			Min.	Max.	
f <sub>HCLK</sub>	AHB clock frequency	GW1NSR-4C	0	80	MHz
f <sub>PCLK</sub>	APB clock frequency	GW1NSR-4C	0	80	MHz



## 3.6 User Flash Characteristics(GW1NSR-4)

### 3.6.1 DC Electrical Characteristics

Table 3-23 GW1NSR-4 User Flash DC Characteristics<sup>[1], [4]</sup>

Name	Parameter	Max.		Unit	Wake-up time	Condition
		V <sub>CC</sub> <sup>[3]</sup>	V <sub>CCX</sub>			
Read mode(w/l 25ns)	I <sub>CC1</sub> <sup>[2]</sup>	2.19	0.5	mA	NA	Minimum clock period, 100% duty cycle, VIN = "1/0"
Write mode		0.1	12	mA	NA	–
Erase mode		0.1	12	mA	NA	–
Page erase mode		0.1	12	mA	NA	–
Static current read (25-50ns)	I <sub>CC2</sub>	980	25	μA	NA	XE=YE=SE="1", between T=T <sub>acc</sub> and T=50ns, the I/O current is 0mA. After T=50ns, the internal timer turns off read mode, and the I/O current turns out to be the standby current.
Standby mode	I <sub>SB</sub>	5.2	20	μA	0	V <sub>SS</sub> , V <sub>CCX</sub> , and V <sub>CC</sub>

**Note!**

- <sup>[1]</sup> These values are average DC currents and the peak currents will be higher than these average currents.
- <sup>[2]</sup> I<sub>CC1</sub> calculation in different cycle time of T<sub>new</sub>.
  - T<sub>new</sub> < T<sub>acc</sub>: not allowed.
  - T<sub>new</sub> = T<sub>acc</sub>: see the table above.
  - T<sub>acc</sub> < T<sub>new</sub> - 50ns: I<sub>CC1</sub> (new) = (I<sub>CC1</sub> - I<sub>CC2</sub>)(T<sub>acc</sub>/T<sub>new</sub>) + I<sub>CC2</sub>
  - T<sub>new</sub> > 50ns: I<sub>CC1</sub> (new) = (I<sub>CC1</sub> - I<sub>CC2</sub>)(T<sub>acc</sub>/T<sub>new</sub>) + 50ns\*I<sub>CC2</sub>/T<sub>new</sub> + I<sub>SB</sub>
  - t > 50ns: I<sub>CC2</sub> = I<sub>SB</sub>
- <sup>[3]</sup> V<sub>CC</sub> must be greater than 1.08V from time zero of the wake-up time.

### 3.6.2 AC Electrical Characteristics

Table 3-24 GW1NSR-4 User Flash Parameters<sup>[1], [4], [5]</sup>

User Mode	Parameter	Symbol	Min.	Max.	Unit
Access time	WC1	$T_{acc}^{[2]}$	-	25	ns
	TC		-	22	ns
	BC		-	21	ns
	LT		-	21	ns
	WC		-	25	ns
Program/Erase to data storage setup time		$T_{nvs}$	5	-	$\mu s$
Data storage hold time		$T_{nvh}$	5	-	$\mu s$
Data storage hold time(mass erase)		$T_{nvh1}$	100	-	$\mu s$
Data storage to program setup time		$T_{pgs}$	10	-	$\mu s$
Program hold time		$T_{pgh}$	20	-	ns
Program time		$T_{prog}$	8	16	$\mu s$
Write prepare time		$T_{wpr}$	>0	-	ns
Write hold time		$T_{whd}$	>0	-	ns
Control to program/erase setup time		$T_{cps}$	-10	-	ns
SE to read control setup time		$T_{as}$	0.1	-	ns
Positive pulse width of SE		$T_{pws}$	5	-	ns
Address/data setup time		$T_{ads}$	20	-	ns
Address/data hold time		$T_{adh}$	20	-	ns
Data hold time		$T_{dh}$	0.5	-	ns
Address hold time in read mode	WC1	$T_{ah}$	25	-	ns
	TC	-	22	-	ns
	BC	-	21	-	ns
	LT	-	21	-	ns
	WC	-	25	-	ns
Negative pulse width of SE		$T_{nws}$	2	-	ns
Recovery time		$T_{rcv}$	10	-	$\mu s$
Data storage time		$T_{hv}^{[3]}$	-	6	ms
Erase time		$T_{erase}$	100	120	ms
Mass erase time		$T_{me}$	100	120	ms
Wake-up time of power-down to standby		$T_{wk\_pd}$	7	-	$\mu s$
Standby hold time		$T_{sbh}$	100	-	ns
$V_{CC}$ setup time		$T_{ps}$	0	-	ns
$V_{CCX}$ hold time		$T_{ph}$	0	-	ns

**Note!**

- <sup>[1]</sup> The values are simulation data and are subject to change.
- <sup>[2]</sup> After XADR, YADR, XE, and YE are valid,  $T_{acc}$  starts at the rising edge of SE. DOUT will be kept before the next valid read operation starts.

- <sup>[3]</sup>  $T_{hv}$  is the cumulative time from the start of the write operation to the next data erase operation. The same address cannot be written twice before the next erase; the same memory cell cannot be written twice before the next erase. This limitation is for security reasons.
- <sup>[4]</sup> All waveforms have a 1ns rising time and a 1ns falling time.
- <sup>[5]</sup> Control signals(X, YADR, XE, and YE) need to be held for at least  $T_{acc}$ , which starts at the rising edge of SE.

### 3.6.3 Timing Diagrams

Figure 3-1 Read Timing

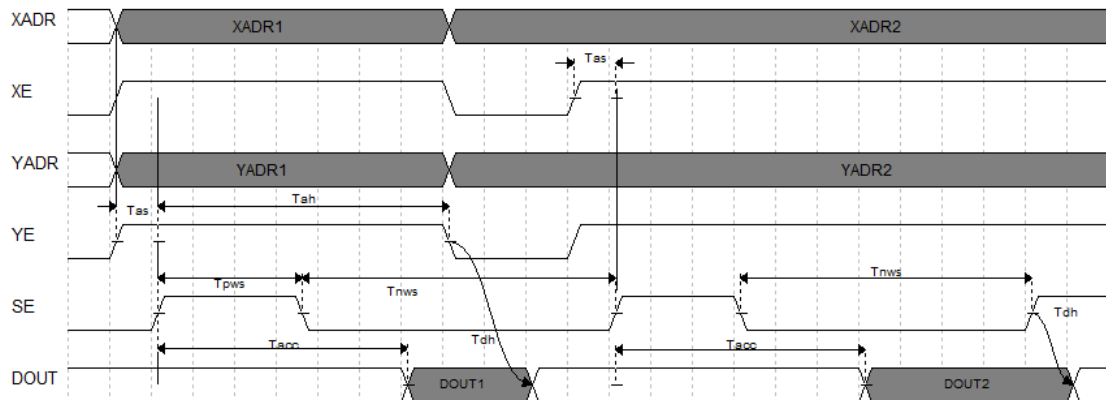
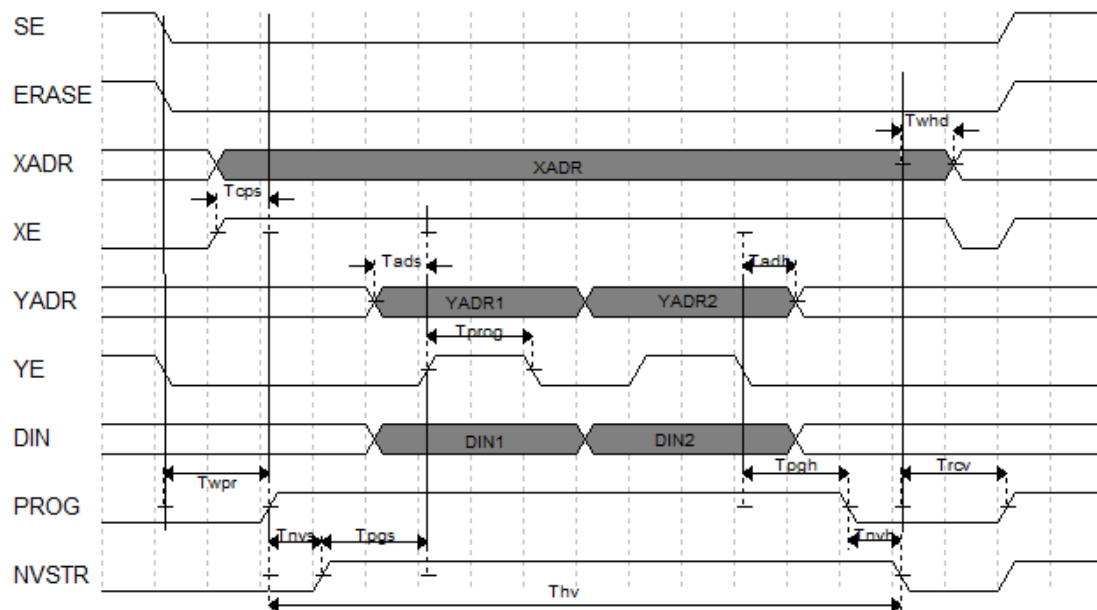
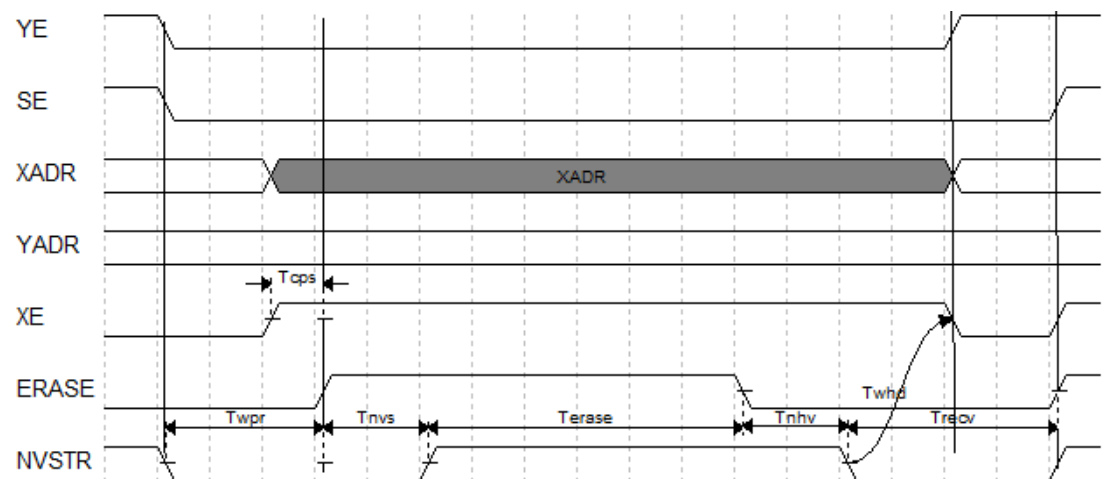


Figure 3-2 Program Timing



**Figure 3-3 Erase Timing**

### 3.7 Configuration Interface Timing Specification

The GW1NSR series of FPGA products support 6 GowinCONFIG modes: AUTO BOOT, SSPI, MSPI, DUAL BOOT, SERIAL, and CPU. For more information, please refer to [UG290, Gowin FPGA Products Programming and Configuration User Guide](#).

# 4 Ordering Information

## 4.1 Part Naming

### Note!

- For more information about the packages, please refer to [1.2 Product Resources](#) and [1.3 Package Information](#).
- The LittleBee family devices and Arora family devices of the same speed grade have different speeds.
- Both “C” and “I” are used in Gowin’s part name marking for one device. GOWIN devices are screened using industrial standards, so the same device can be used for both industrial (I) and commercial (C) applications. The maximum temperature of the industrial grade is 100°C, and the maximum temperature of the commercial grade is 85°C. Therefore, if the chip meets speed grade 6 in commercial grade applications, its speed grade will be 5 in industrial grade applications.

Figure 4-1 Part Naming Examples for GW1NSR-4 Devices- ES

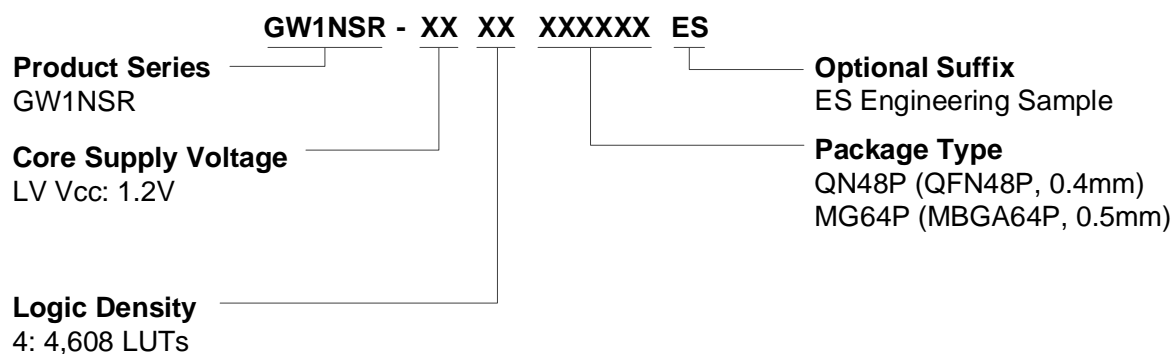


Figure 4-2 Part Naming Examples for GW1NSR-4C Devices- ES

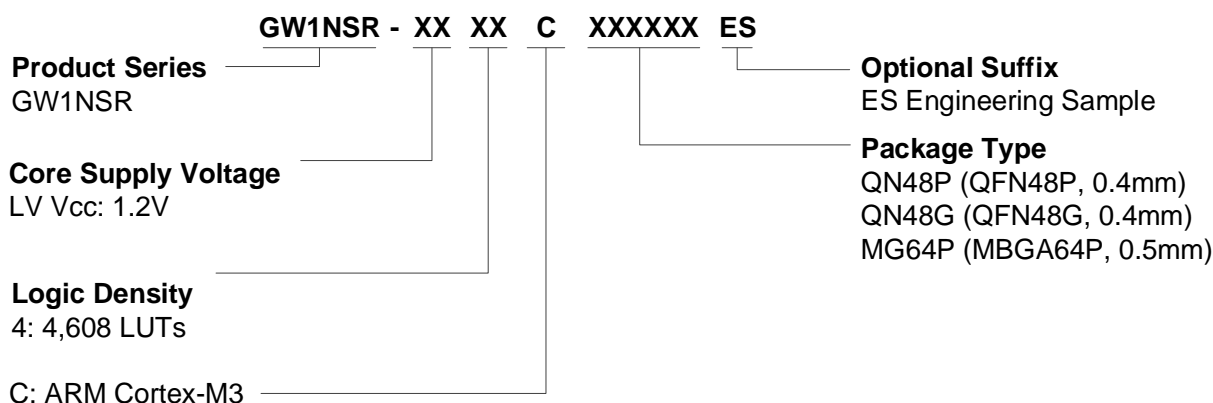


Figure 4-3 Part Naming Examples for GW1NSR-4 Devices - Production

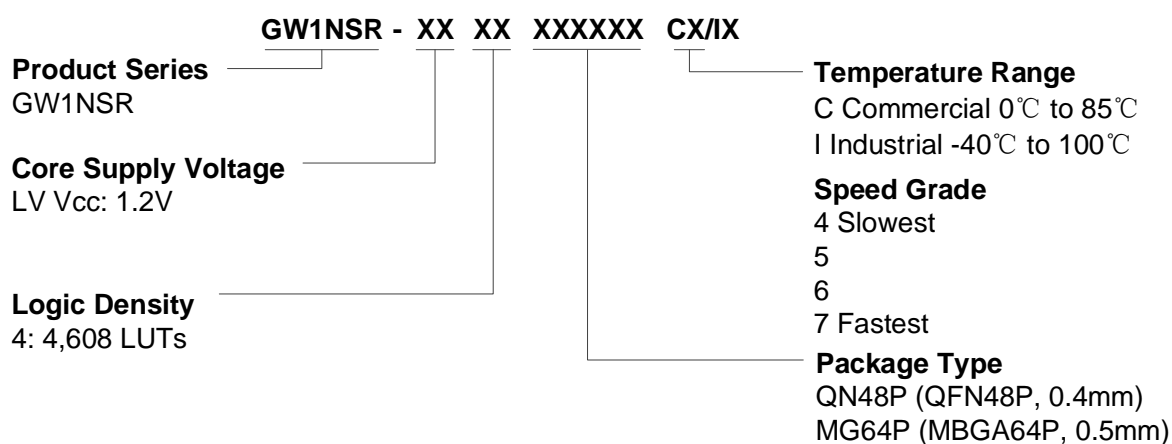
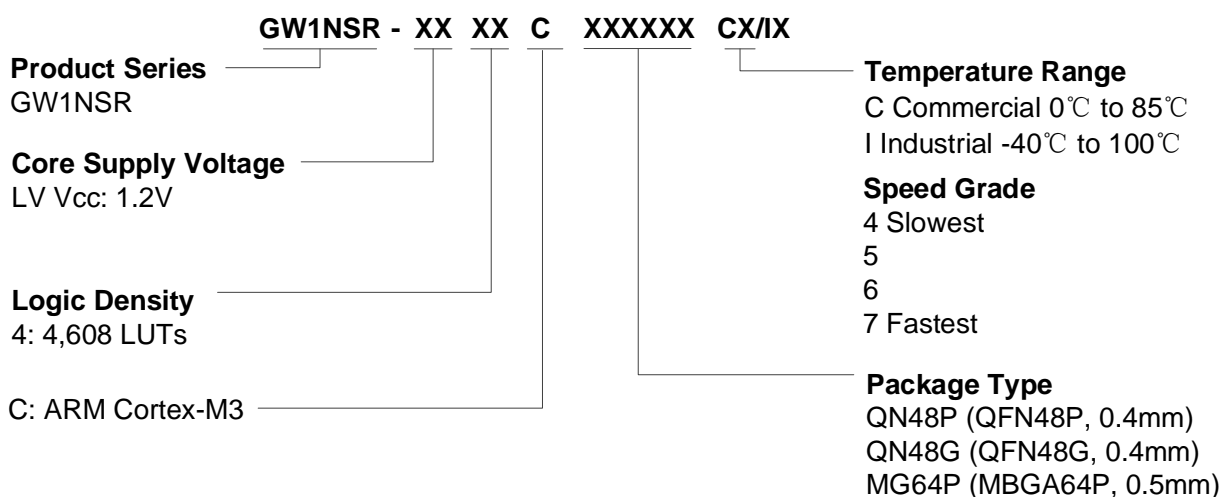


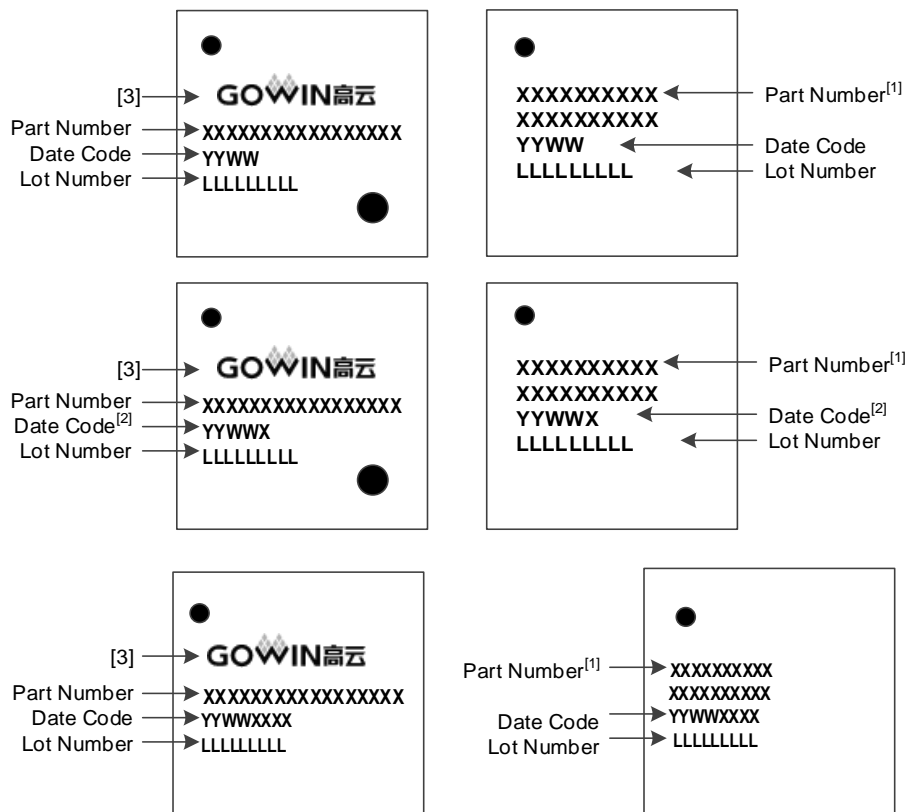
Figure 4-4 Part Naming Examples for GW1NSR-4C Devices - Production



## 4.2 Package Markings

Gowin's devices have markings on the their surfaces, as shown in Figure 4-5.

Figure 4-5 Package Marking Examples



### Note!

- <sup>[1]</sup> The first two lines in the right figure(s) above are both the “Part Number”.
- <sup>[2]</sup> The fifth character of the Date Code denotes the version of the device.
- <sup>[3]</sup> Whether the package marking bears the Gowin Logo or not depends on the package type, package size, and Part Number length. The above figure are only examples of the package markings.

# 5 About This Manual

## 5.1 Purpose

This data sheet provides a comprehensive overview of the GW1NSR series of FPGA products, including their features, resources, architecture, AC/DC characteristics, and ordering details.

## 5.2 Related Documents

The latest documents are available at [www.gowinsemi.com](http://www.gowinsemi.com).

- [UG863, GW1NSR series of FPGA Products Package & Pinout User Guide](#)
- [UG864, GW1NSR-4 Pinout](#)
- [UG865, GW1NSR-4C Pinout](#)

## 5.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are shown in Table 5-1.

Table 5-1 Terminology and Abbreviations

Terminology and Abbreviations	Full Name
AHB	Advanced High performance Bus
ALU	Arithmetic Logic Unit
APB	Advanced Peripheral Bus
ARM	Advanced RISC Machine
BSRAM	Block Static Random Access Memory
CFU	Configurable Function Unit
CLS	Configurable Logic Section
CRU	Configurable Routing Unit
DAP	Debug Access Port
DCS	Dynamic Clock Selector
DNL	Differential Nonlinearity
DP	True Dual Port 16K BSRAM



Terminology and Abbreviations	Full Name
DQCE	Dynamic Quadrant Clock Enable
DWT	Data Watchpoint Trace
FPGA	Field Programmable Gate Array
GPIO	Gowin Programmable Input/output
INL	Integral Nonlinearity
IOB	Input/Output Block
ITM	Instrumentation Trace Macrocell
LSB	Least Significant Bit
LUT4	4-input Look-up Table
MG	MBGA
NVIC	Nested Vector Interrupt Controller
PHY	Physical Layer
PLL	Phase-locked Loop
QN	QFN
REG	Register
SAR	Successive Approximation Register
SDP	Semi Dual Port 16K BSRAM
SFDR	Spurious-freeDynamic Range
SINAD	Signal to Noise And Distortion
SoC	System on Chip
SP	Single Port 16K BSRAM
SSRAM	Shadow Static Random Access Memory
TDM	Time Division Multiplexing
Timer	Timer
TimeStamp	TimeStamp
TPIU	Trace Port Interface Unit
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
Watchdog	Watchdog

## 5.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: [www.gowinsemi.com](http://www.gowinsemi.com)

E-mail: [support@gowinsemi.com](mailto:support@gowinsemi.com)

