GW1NSE series of SecureFPGA Products

DataSheet

DS871-1.04E, 07/21/2022

Disclaimer

GOWINSEMI assumes no liability and provides no warranty (either expressed or implied) and is not responsible for any damage incurred to your hardware, software, data, or property resulting from usage of the materials or intellectual property except as outlined in the GOWINSEMI Terms and Conditions of Sale. GOWINSEMI may make changes to this document at any time without prior notice. Anyone relying on this documentation should contact GOWINSEMI for the current documentation and errata.

Revision History

Date	Version	Description
11/22/2019	1.0E	Initial version published.
08/13/2020	1.01E	● PLL Parameters optimized. ● Figures of Part Naming optimized.
11/27/2020	1.02E	The Max. operating frequency of ARM Cortex-M3 updated.
11/18/2021	1.03E	The description of I/O standards updated.
07/21/2022	1.04E	● Recommended operating conditions updated. ● The maximum value of the differential input threshold V_{THD} updated. ● Note about USB 2.0 PHY added.

Contents

List of Figures

List of Tables

1 About This Guide

1.1 Purpose

This data sheet describes the features, product resources and structure, AC/DC characteristics, timing specifications of the configuration interface, and the ordering information of the GW1NSE series of FPGA product. It is designed to help you understand the GW1NSE series of SecureFPGA products quickly and select and use devices appropriately.

1.2 Related Documents

The latest user guides are available on GOWINSEMI Website. You can find the related documents atwww.gowinsemi.com.cn:

- DS871, GW1NSE series of SecureFPGA products Data Sheet
- UG290, Gowin FPGA products Programming and Configuration User Guide
- UG874, GW1NSE series of SecureFPGA products Package and Pinout
- UG872, GW1NSE-2C Pinout

1.3 Abbreviations and Terminology

The abbreviations and terminologies used in this manual are set out in Table 1-1 below.

Table 1-1 Abbreviations and Terminology

Abbreviations and Terminology	Name
FPGA	Field Programmable Gate Array
SoC	System on Chip
ARM	Advanced RISC Machine
AHB	Advanced High performance Bus
APB	Advanced Peripheral Bus
Timer	Timer
UART	Universal Asynchronous Receiver/Transmitter
NVIC	Nested Vector Interrupt Controller
DAP	Debug Access Port
Watchdog	Watchdog
TimeStamp	TimeStamp
DWT	Data Watchpoint Trace
ITM	Instrumentation Trace Module
TUIP	Trace Port Interface Unit
USB	Universal Serial Bus
PHY	Physical Layer
ADC	Analog to Digital Converter
SAR	Successive Approximation Register
SFDR	Spurious-free Dynamic Range
SINAD	Signal to Noise And Distortion
LSB	Least Significant Bit
INL	Integral Nonlinearity
DNL	Differential Nonlinearity
CFU	Configurable Function Unit
CLS	Configurable Logic Section
CRU	Configurable Routing Unit
LUT4	4-input Look-up Tables
LUT5	5-input Look-up Tables
LUT6	6-input Look-up Tables
LUT7	7-input Look-up Tables
LUT8	8-input Look-up Tables
REG	Register
ALU	Arithmetic Logic Unit

Abbreviations and Terminology	Name
IOB	Input/Output Block
SSRAM	Shadow Static Random Access Memory
BSRAM	Block Static Random Access Memory
SP	Single Port 16K BSRAM
SDP	Semi Dual Port 16K BSRAM
DP	True Dual Port 16K BSRAM
DQCE	Dynamic Quadrant Clock Enable
DCS	Dynamic Clock Selector
PLL	Phase-locked Loop
GPIO	Gowin Programmable IO
QN	QFN
LQ	LQFP
TDM	Time Division Multiplexing
OTP	One-Time-Programmable

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com.cn

E-mail: support@gowinsemi.com

2 General Description

GW1NSE series of SecureFPGA products provide a Root of Trust based on SRAM PUF technology. Each device is factory provisioned with a unique key pair that is never exposed outside of the device or to the internal development space. The Intrinsic ID BroadKey-Pro security library is provided with GOWIN SecureFPGA devices allowing easy integration of common security features into user applications. The GOWIN SecureFPGA feature set is widely applicable and can used for a variety of consumer and industrial IoT, edge, and server management applications.

GW1NSE series of SecureFPGA products onsist of the same hardware architecture as that of GW1NS-2C/4C devices, and cover all features of GW1NS-2C/4C devices. In addition, GW1NSE-2C SecuredFPGA has an OTP (One-Time-Programmable) Authentication Code pre-stored in its internal Non-volatile 128KB User Flash memory other than the regular GW1NS-2C has none.

GOWINSEMI provides a new generation of FPGA hardware development environment through market-oriented independent research and development that supports the GW1NSE series of SecureFPGA products and applies to FPGA synthesizing, layout, place and routing, data bitstream generation and download, etc.

2.1 Features

- Lower power consumption
  - 55nm embedded flash technology
  - Core voltage: 1.2V
  - GW1NSE-2C supports LX and UX
  - GW1NSE-4C supports LV
  - Clock dynamically turns on and off
- Hard core processor
  - Cortex-M3 32-bit RISC
  - ARM3v7M architecture optimized for small-footprint embedded applications
  - System timer (SysTick), providing a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control

mechanism
  - Thumb compatible Thumb-2-only instruction set processor core for high code density
  - GW1NSE-2C supports up to 30 MHz operating frequency
  - GW1NSE-4C supports up to 80 MHz operating frequency
  - Hardware-division and single-cycle-multiplication
  - Integrated nested vectored interrupt controller (NVIC) providing deterministic interrupt handling
  - 26 interrupts with eight priority levels
  - Memory protection unit (MPU), providing a privileged mode for protecting operation system functionality
  - Unaligned data access, enabling data to be efficiently packed into memory
  - Atomic bit manipulation (bit-banding), delivering maximum memory utilization and streamlined peripheral control
  - Timer0 and Timer1
  - UART0 and UART1
  - Watchdog
  - Debug port: JTAG and TPIU
- Provdes OTP Authentication code
- USB2.0 PHY
  - 480Mbps data speed, compatible with USB1.1 1.5/12Mbps data speed
  - Plug and play
  - Hot socket
- ADC
  - Eight channels
  - 12-bit SAR AD conversion
  - Slew Rate: 1MHz
  - Dynamic range: >81 dB SFDR，>62 db SINAD
  - Linear performance: INL<1 LSB, DNL<0.5 LSB, no missing codes
- User Flash
  - 128K Byte storage space embedded in GW1NSE-2C
  - 32K Byte storage space embedded in GW1NSE-4C
  - 32-bit data width
- Provide a Root of Trust based on SRAM PUF technology
- Multiple I/O Standards
  - LVCMOS33/25/18/15/12; LVTTL33, SSTL33/25/18 I, SSTL33/25/18 II, SSTL15; HSTL18 I, HSTL18 II, HSTL15 I; PCI, LVDS25, RSDS, LVDS25E, BLVDSE
  - MLVDSE, LVPECLE, RSDSE
  - Input hysteresis option
  - Supports 4mA,8mA,16mA,24mA, etc. drive options
  - Slew Rate option
  - Output drive strength option
  - Individual Bus Keeper, Weak Pull-up, Weak Pull-down, and Open Drain option
  - Hot Socket
  - BANK0 supports MIPI input
  - BANK2 supports MIPI output

  - BANK0 and BANK2 support I3C
- Abundant Slices
  - Four input LUT (LUT4)
  - Double-edge flip-flops
  - Supports shifter register
- Block SRAM with multiple modes
  - Supports Dual Port, Single Port, and Semi Dual Port
  - Supports bytes write enable
- Flexible PLLs
  - Frequency adjustment (multiply and division) and phase adjustment
  - Supports global clock
- Built-in Flash programming
  - Instant-on
  - Supports security bit operation
  - Supports AUTO BOOT and DUAL BOOT
- Configuration
  - JTAG configuration
  - Supports on-chip DUAL BOOT configuration mode
  - Multiple GowinCONFIG configuration modes: AUTOBOOT, SSPI, MSPI, CPU, SERIAL

2.2 Product Resources

Table 2-1 Product Resources

Device	GW1NSE-2C	GW1NSE-4C
LUT4	1,728	4608
Flip-Flop (FF)	1,296	3456
Block SRAM BSRAM(bits)	72K	180K
BSRAM quantity BSRAM	4	10
SSRAM (bits)	4608	0
User Flash (bits)	1024	256
18X18 Multiplier	-	16
PLLs	1	2
OSC	1, ±5% accuracy	1, ±5% accuracy
Hard core processor	Cortex-M3	Cortex-M3
USB 2.0 PHY	1	0
ADC[1]	8	0
Total number of I/O banks	4	3
Max. I/O	102	106
Core voltage	1.2V	1.2V

Note!

[1]Up to eight-channel ADC can be supported. For the detailed infotmation, please refer to Table 2-2 GW1NSE-2C Package Information.

2.3 Package Information

Table 2-2 GW1NSE-2C Package Information

Internal Resources	Package	
	QN48	LQ144
LUT4	Yes	Yes
FF	Yes	Yes
BSRAM	Yes	Yes
SSRAM	Yes	Yes
User Flash	Yes	Yes
PLL	Yes	Yes
OSC	Yes	Yes
Cortex-M3	Yes	Yes
USB2.0 PHY[1]	N/A	Yes
ADC[2]	8	8

Note!

[1] The USB 2.0 PHY is only supported on part numbers with speed grade C7 and above.
[2] The Number refers to the number of channels supported by this package.

Table 2-3 Package Information, Max. User I/O, and LVDS Pairs

Package	Pitch(mm)	Size(mm)	GW1NSE-2C	GW1NSE-4C
QN48	0.4	6 x 6	39(7)	-
LQ144	0.5	20 x 20	91(11)	-

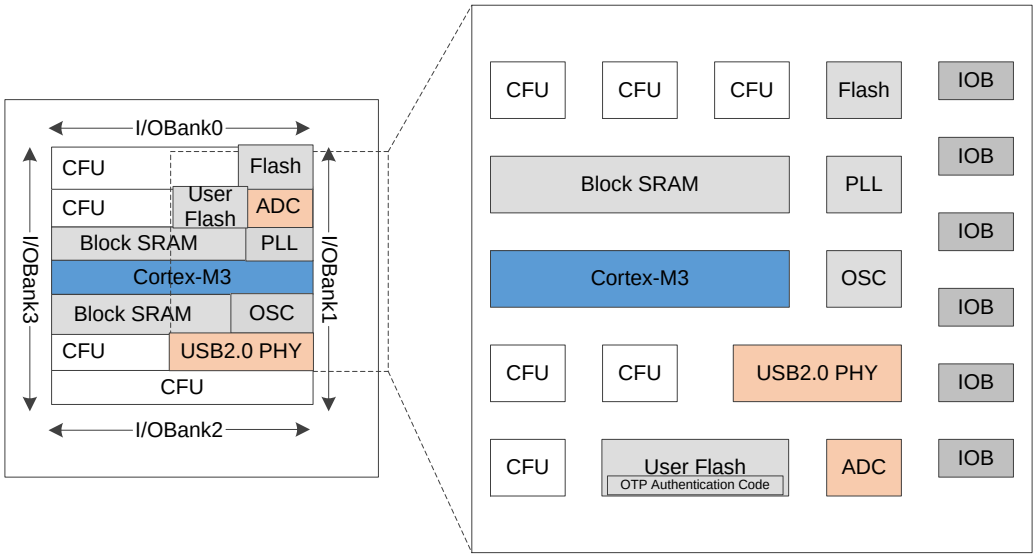
Note!

- JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The Max. User I/O noted in this table is referred to when the four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O. When mode [2:0] = 001, JTAGSEL_N and the four JTAG pins (TCK, TDI, TDO, and TMS) can be used as GPIO simultaneously, and the Max. user I/O is increased by one. See *UG874, GW1NSE series of SecureFPGA products Package and Pinout* for more details;
- The package types in this data sheet are written with abbreviations. See 5.1Part Nam.
- Please refer to *UG872, GW1NSE-2C Pinout* for further detailed information.

3 Architecture

3.1 Architecture Overview

Figure 3-1 GW1NSE-2C Architecture Overview



GW1NSE series of SecureFPGA products include CFU, BSRAM, PLL, User Flash, on-chip oscillator, downloaded flash resources, USB2.0 PHY, and ADC. GW1NSE-2C also includes Cortex-M3, See Table 2-1 and Table 2-2 for more detailed information.

The configurable function unit (CFU) is the base cell for the array of the GW1NSE series of SecureFPGA products. Devices with different capacities have different numbers of rows and columns. CFU can be configured as LUT4 mode and ALU mode, and Memory mode. For more detailed information, see 3.2 Configurable Function Unit.

The I/O resources in the GW1NSE series of SecureFPGA products are arranged around the periphery of the devices in groups referred to as banks, including Bank0, Bank1, Bank2, and Bank3. The I/O resources support multiple level standards, and support basic mode, SRD mode, and generic DDR mode. For more detailed information, see 3.3 IOB.

The BSRAM is embedded as a row in the GW1NSE series of SecureFPGA products. In the FPGA array, each BSRAM occupies three columns of CFU. BSRAM has two usages; however, these cannot be employed simultaneously. One is for the Cortex-M3 processor SRAM, which is used for memory data read/write. The capacity of SRAM can be configured as 2K-Byte/4K-Byte/8K-Byte via Gowin YunYuan software. The unused BSRAM can also be the FPGA storage resources. The other one usage is for user SRAM. One BSRAM capacity is 18 Kbits. It supports multiple configuration modes and operation modes. For further details, please refer to 3.4 Block SRAM (BSRAM).

The User Flash is embedded in the GW1NSE series of SecureFPGA products, without loss of data even if powered off. The User Flash used in GW1NSE-2C has three usages; however, these cannot be used simultaneously. One is used for Cortex-M3 processor ARM programs storage. In this way, the User Flash can only be read and cannot be written. One is used as the non-volatile memory resource. One is used for the DUAL BOOT mode of FPGA. See 3.5 User Flash (GW1NSE-2C) for more detailed information. The User Flash used in GW1NSE-4C has two usages and they cannot be used simultaneously. One is used for Cortex-M3 processor ARM programs storage. In this way, the User Flash can only be read and cannot be written. One is used as the non-volatile memory resource. See 3.6 User Flash (GW1NSE-4C) for more detailed information.

GW1NSE series of SecureFPGA products provide a Root of Trust based on SRAM PUF technology. SecuredFPGA has an OTP (One-Time-Programmable) Authentication Code pre-stored in its internal Non-volatile 128KB User Flash memory. See 3.7 OTP Authentication Code for further detailed information.

GW1NSE provides PLLs. PLL blocks provide the ability to synthesize clock frequencies. Frequency adjustment (multiply and division), phase adjustment, and duty cycle can be adjusted using the configuration of parameters. There is an internal programmable on-chip oscillator in each of the GW1NSE series of the FPGA product. The on-chip oscillator supports the clock frequencies ranging from 2.5 MHz to 120MHz, providing the clock resource for the MSPI mode. It also provides clock resource for user designs with the clock precision reaching ±5%. For more detailed information, see 3.11 Clock.

The Flash resources embedded in the GW1NSE series of SecureFPGA products are used for built-in Flash programming, support instant start and security bit operation, and support AUTO BOOT and DUAL BOOT programming modes. For more detailed information, see 4.8 Configuration Interface Timing Specification.

The Cortex-M3 hard-core processor is embedded in GW1NSE-2C. It supports 30 MHz program loading when the system starts up and supports higher speed data/instructions transmission. The AHB expansion bus facilitates communication with external storage devices. The APB bus also facilitates communication with external devices, such as UART. GPIO interfaces are convenient for communicating with the external interfaces. FPGA can be programmed to realize controller functions across different

interfaces / standards, such as SPI, I^2C, I^3C, etc. For more detailed information, see 3.8 Cortex-M3.

USB2.0 PHY is embedded in the GW1NSE series of SecureFPGA products. FPGA logics can be programmed to realize USB controllers with specific functions. For more detailed information, see 3.9 USB2.0 PHY.

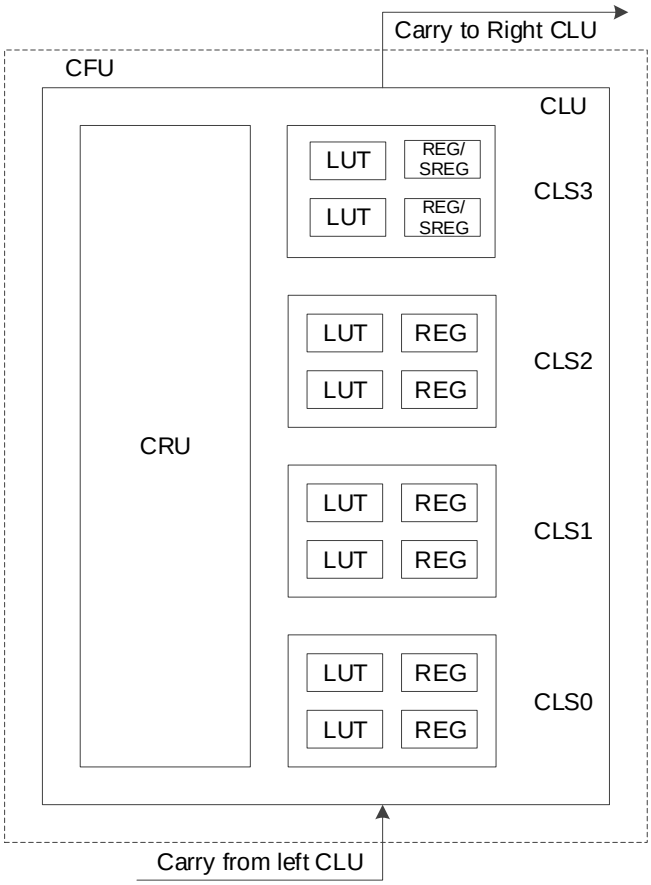
An ADC is embedded in the GW1NSE series of SecureFPGA products. It is a successive-approximation ADC with eight-channel data conversion, high dynamic performance, high precision, low power consumption, and low cost. For more detailed information, see 3.10 ADC.

FPGA provides abundant CRUs, connecting all the resources in FPGA. For example, routing resources distributed in CFU and IOB connect resources in CFU and IOB. Routing resources can automatically be generated by Gowin software. In addition, the GW1NSE series of SecureFPGA products also provide abundant GCLKs, long wires (LW), global set/reset (GSR), and programming options, etc. For more detailed information, see 3.11 Clock, 3.12 Long Wire (LW) and 3.13 Global Set/Reset (GSR).

3.2 Configurable Function Unit

The configurable function unit (CFU) is the base cell for the array of the GW1NSE series of SecureFPGA products. Each CFU consists of a configurable logic unit (CLU) and its routing resource configurable routing unit (CRU). In each CLU, there are four Configurable Logic Sections (CLS). Each CLS contains look-up tables (LUT) and registers, as shown in Figure 3-2 below.

Figure 3-2 CFU Structure



Note!

SERG needs special patch supporting. Please contact Gowin technical support or local O ffice for this patch.

3.2.1 CLU

The CLU supports three operation modes: basic logic mode, ALU mode, and memory mode.

- Basic Logic Mode

Each LUT can be configured as one four input LUT. A higher input number of LUT can be formed by combining LUT4 together.

  - Each CLS can form one five input LUT5.
  - Two CLSs can form one six input LUT6.
  - Four CLSs can form one seven input LUT7.
  - Eight CLSs (two CLUs) can form one eight input LUT8.

- ALU Mode

When combined with carry chain logic, the LUT can be configured as the ALU mode to implement the following functions.

  - Adder and subtractor
  - Up/down counter
  - Comparator,including greater-than, less-than, and not-equal-to
  - MULT

Register

Each Configurable Logic Section (CLS0~CLS2) has two registers (REG), as shown in Figure 3-3 below.

Figure 3-3 Register in CLS

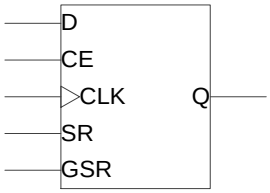


Table 3-1 Register Description in CFU

Signal	I/O	Description
D	I	Data input [1]
CE	I	CLK enable, can be high or low effective [2]
CLK	I	Clock, can be rising edge or falling edge trigging [2]
SR	I	Set/Reset, can be configured as [2]: ● Synchronized reset ● Synchronized set ● Asynchronous reset ● Asynchronous set ● Non
GSR[3,4]	I	Global Set/Reset, can be configured as[4]: ● Asynchronous reset ● Asynchronous set ● Non
Q	O	Register

Note!

- [1]The source of the signal D can be the output of a LUT, or the input of the CRU; as such, the register can be used alone when LUTs are in use.
- [2]CE/CLK/SR in CFU is independent.
- [3]In the GW1NSE series of SecureFPGA products, GSR has its own dedicated network.
- [4]When both SR and GSR are effective, GSR has higher priority.

3.2.2 CRU

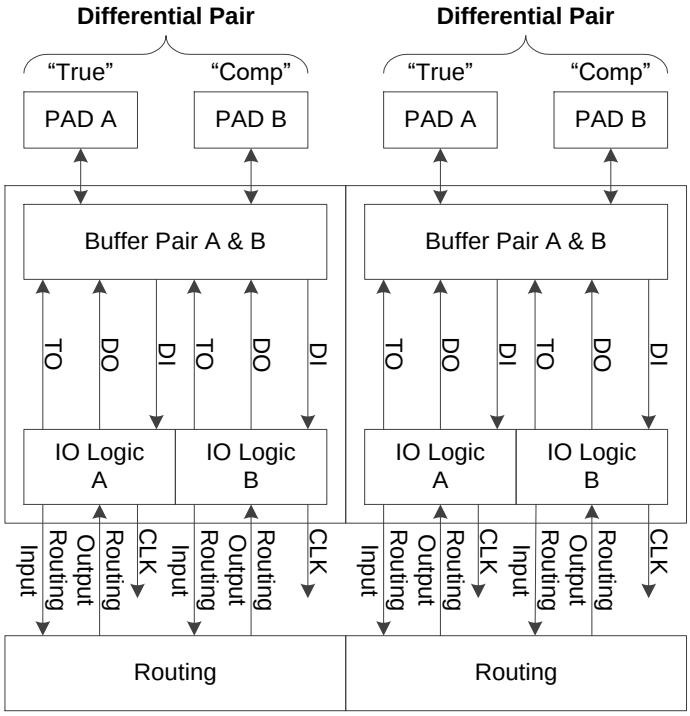
The main functions of the CRU are as follows:

- Input selection: Select input signals for the CFU.
- Configurable routing: Connect the input and output of the CFUs, including inside the CFU, CFU to CFU, and CFU to other functional blocks in FPGA.

3.3 IOB

The IOB in the GW1NSE series of SecureFPGA products includes IO buffer, IO logic, and its routing unit. As shown in Figure 3-4, each IOB connects to two pins (Marked A and B). They can be used as a differential pair or as two single-end input/output.

Figure 3-4 IOB Structure View



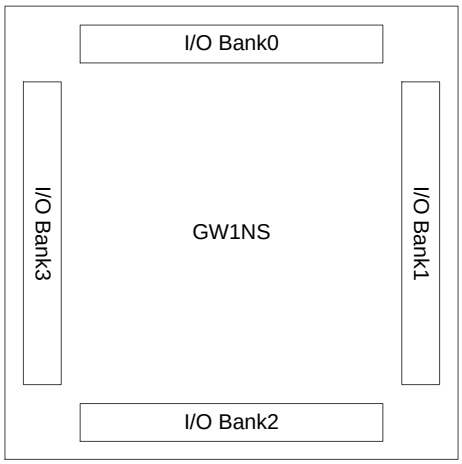
IOB Features:

- V_{CCO} supplied with each bank
- LVCMOS, PCI, LVTTL, LVDS, SSTL, and HSTL
- Input hysteresis option
- Output drive strength option
- Slew rate option
- Individual Bus Keeper, Weak Pull-up, Weak Pull-down, and Open Drain option
- Hot socket
- IO logic supports basic mode, SRD mode, and generic DDR mode
- BANK0 supports MIPI input
- BANK2 supports MIPI output
- BANK0 and BANK2 support I3C

3.3.1 I/O Buffer

There are four IO Banks in the GW1NSE series of SecureFPGA products, as shown in Figure 3-5. To support SSTL, HSTL, etc., each bank also provides one independent voltage source (V_{REF}) as referenced voltage. The user can choose from the internal reference voltage of the bank (0.5 x V_{CCO}) or the external reference voltage using any IO from the bank.

Figure 3-5 GW1NSE I/O Bank Distribution



The GW1NSE series of SecureFPGA products support LX and UX.

The core voltage of the GW1NSE series of SecureFPGA products is 1.2V;

LX has no linear voltage regulator, and V_{CCX} needs to be set to 1.8V. The I/O Bank voltage V_{CCO} can be set as 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V according to requirements.

UX has linear voltage regulator, and V_{CCX} needs to be set to 2.5 V. The I/O Bank voltage V_{CCO} can be set as 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V according to requirements.

Note!

- For both LX and UX devices, V_{CCO2} needs to be set as 1.2 V when BANK2 MIPI output is used, and the MIPI output speed of LX devices can ony reach 60% of that of UX devices.
- By default, the Gowin Programmable IO is tri-stated weak pull-up.

For the V_{CCO} requirements of different I/O standards, see Table 3-2 and Table 3-3.

Table 3-2 Output I/O Standards and Configuration Options

I/O output standard	Single/Differ	Bank V_{CCO} (V)	Driver Strength (mA)
LVCMOS33/ LVTTL33	Single end	3.3	4,8,12,16,24
LVCMOS25	Single end	2.5	4,8,12,16
LVCMOS18	Single end	1.8	4,8,12
LVCMOS15	Single end	1.5	4,8
LVCMOS12	Single end	1.2	4,8
SSTL25_I	Single end	2.5	8
SSTL25_II	Single end	2.5	8
SSTL33_I	Single end	3.3	8
SSTL33_II	Single end	3.3	8
SSTL18_I	Single end	1.8	8
SSTL18_II	Single end	1.8	8
SSTL15	Single end	1.5	8
HSTL18_I	Single end	1.8	8
HSTL18_II	Single end	1.8	8
HSTL15_I	Single end	1.5	8
PCI33	Single end	3.3	8/4
LVPECL33E	Differential	3.3	16
MVLDS25E	Differential	2.5	16
BLVDS25E	Differential	2.5	16
RSDS25E	Differential	2.5	8
LVDS25E	Differential	2.5	8
MIPI	Differential（MIPI）	1.2	N/A
LVDS25	Differential（True LVDS）	2.5/3.3	N/A
RSDS	Differential（True LVDS）	2.5/3.3	N/A
MINILVDS	Differential（True LVDS）	2.5/3.3	N/A
PPLVDS	Differential（True LVDS）	2.5/3.3	N/A
SSTL15D	Differential	1.5	8
SSTL25D_I	Differential	2.5	8
SSTL25D_II	Differential	2.5	8
SSTL33D_I	Differential	3.3	8
SSTL33D_II	Differential	3.3	8
SSTL18D_I	Differential	1.8	8
SSTL18D_II	Differential	1.8	8
HSTL18D_I	Differential	1.8	8
HSTL18D_II	Differential	1.8	8

I/O output standard	Single/Differ	Bank V_{CCO} (V)	Driver Strength (mA)
HSTL15D_I	Differential	1.5	8
LVCMOS12D	Differential	1.2	4,8
LVCMOS15D	Differential	1.5	4,8
LVCMOS18D	Differential	1.8	4,8,12
LVCMOS25D	Differential	2.5	4,8,12,16
LVCMOS33D	Differential	3.3	4,8,12,16,24

Table 3-3 Input I/O Standards and Configuration Options

I/O Input Standard	Single/Differ	Bank V_{CCO} (V)	Hysteresis	Need V_{REF}
LVCMOS33/ LVTTL33	Single end	1.2/1.5/1.8/2.5/3.3	Yes	No
LVCMOS25	Single end	1.2/1.5/1.8/2.5/3.3	Yes	No
LVCMOS18	Single end	1.2/1.5/1.8/2.5/3.3	Yes	No
LVCMOS15	Single end	1.2/1.5/1.8/2.5/3.3	Yes	No
LVCMOS12	Single end	1.2/1.5/1.8/2.5/3.3	Yes	No
SSTL15	Single end	1.5/1.8/2.5/3.3	No	Yes
SSTL25_I	Single end	2.5/3.3	No	Yes
SSTL25_II	Single end	2.5/3.3	No	Yes
SSTL33_I	Single end	3.3	No	Yes
SSTL33_II	Single end	3.3	No	Yes
SSTL18_I	Single end	1.8/2.5/3.3	No	Yes
SSTL18_II	Single end	1.8/2.5/3.3	No	Yes
HSTL18_I	Single end	1.8/2.5/3.3	No	Yes
HSTL18_II	Single end	1.8/2.5/3.3	No	Yes
HSTL15_I	Single end	1.5/1.8/2.5/3.3	No	Yes
LVCMOS33OD25	Single end	2.5	No	No
LVCMOS33OD18	Single end	1.8	No	No
LVCMOS33OD15	Single end	1.5	No	No
LVCMOS25OD18	Single end	1.8	No	No
LVCMOS25OD15	Single end	1.5	No	No
LVCMOS18OD15	Single end	1.5	No	No
LVCMOS15OD12	Single end	1.2	No	No
LVCMOS25UD33	Single end	3.3	No	No
LVCMOS18UD25	Single end	2.5	No	No
LVCMOS18UD33	Single end	3.3	No	No
LVCMOS15UD18	Single end	1.8	No	No
LVCMOS15UD25	Single end	2.5	No	No
LVCMOS15UD33	Single end	3.3	No	No
LVCMOS12UD15	Single end	1.5	No	No
LVCMOS12UD18	Single end	1.8	No	No
LVCMOS12UD25	Single end	2.5	No	No
LVCMOS12UD33	Single end	3.3	No	No
PCI33	Single end	3.3	Yes	No
VREF1_DRIVER	Single end (Vref Input)	1.2/1.5/1.8/2.5/3.3	No	Yes
MIPI	Differential (MIPI)	1.2	No	No
LVDS25	Differential	2.5/3.3	No	No

I/O Input Standard	Single/Differ	Bank V_{CCO} (V)	Hysteresis	Need V_{REF}
RSDS	Differential	2.5/3.3	No	No
MINILVDS	Differential	2.5/3.3	No	No
PPLVDS	Differential	2.5/3.3	No	No
LVDS25E	Differential	2.5/3.3	No	No
MLVDS25E	Differential	2.5/3.3	No	No
BLVDS25E	Differential	2.5/3.3	No	No
RSDS25E	Differential	2.5/3.3	No	No
LVPECL33E	Differential	3.3	No	No
SSTL15D	Differential	1.5/1.8/2.5/3.3	No	No
SSTL25D_I	Differential	2.5/3.3	No	No
SSTL25D_II	Differential	2.5/3.3	No	No
SSTL33D_I	Differential	3.3	No	No
SSTL33D_II	Differential	3.3	No	No
SSTL18D_I	Differential	1.8/2.5/3.3	No	No
SSTL18D_II	Differential	1.8/2.5/3.3	No	No
HSTL18D_I	Differential	1.8/2.5/3.3	No	No
HSTL18D_II	Differential	1.8/2.5/3.3	No	No
HSTL15D_I	Differential	1.5/1.8/2.5/3.3	No	No
LVCMOS12D	Differential	1.2/1.5/1.8/2.5/3.3	No	No
LVCMOS15D	Differential	1.5/1.8/2.5/3.3	No	No
LVCMOS18D	Differential	1.8/2.5/3.3	No	No
LVCMOS25D	Differential	2.5/3.3	No	No
LVCMOS33D	Differential	3.3	No	No

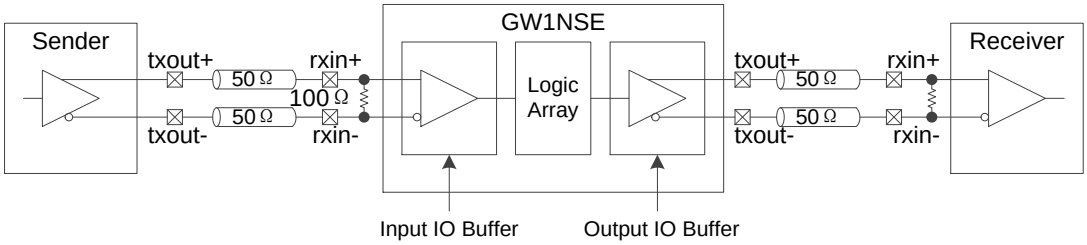
3.3.2 True LVDS Design

BANK1/2/3 in the GW1NSE series of SecureFPGA products support true LVDS output, but BANK1/2/3 do not support internal 100Ω input differential matched resistance. Bank0 supports internal 100Ω input differential matched resistance, but does not support true LVDS output. BANK0/1/2/3 support LVDS25E, MLVDS25E, BLVDS25E, etc. For more detailed information about different levels, please refer to *UG289, Gowin Programmable IO User Guide.*

For more detailed information about true LVDS, please refer to *UG872, GW1NSE-2C Pinout*.

True LVDS input I/O needs external 100Ω terminal resistance for matching. See Figure 3-6 for the true LVDS design.

Figure 3-6 True LVDS Design



For more detailed information about LVDS25E, MLVDS25E, and BLVDS25E on IO terminal matched resistance, please refer to *UG289, Gowin Programmable IO User Guide*.

3.3.3 I/O Logic

Figure 3-7 shows the I/O logic output of the GW1NSE series of SecureFPGA products.

Figure 3-7 I/O Logic Input

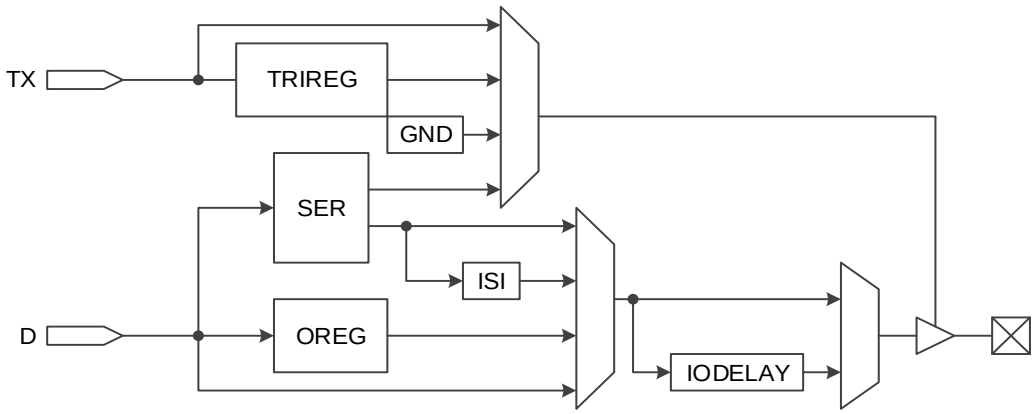


Figure 3-8 shows the I/O logic input of the GW1NSE series of SecureFPGA products.

Figure 3-8 I/O Logic Input

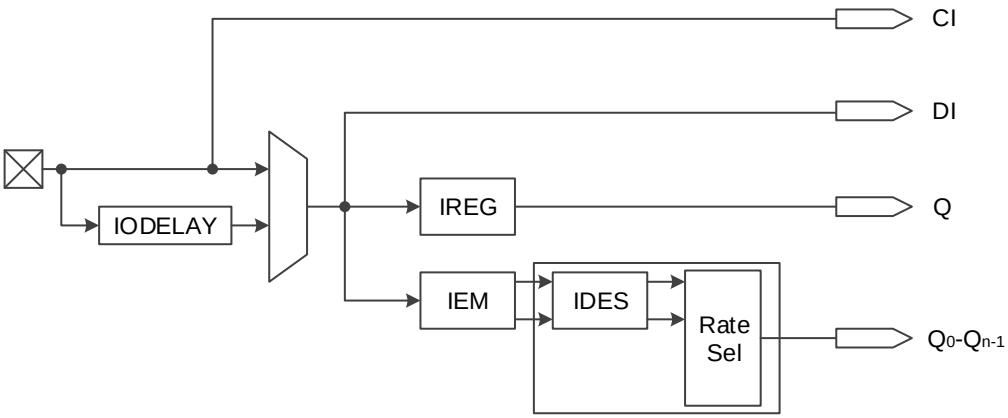


Table 3-1 Port Descsription

Ports	I/O	Description
CI[1]	Input	GCLK input signal. For the number of GCLK input signals, please refer to *UG872*, *GW1NSE-2C Pinout*.
DI	Input	IO port low-speed input signal, entering into Fabric directly.
Q	Output	IREG output signal in SDR module.
Q_0-Q_{n-1}	Output	IDES output signal in DDR module.

Note!

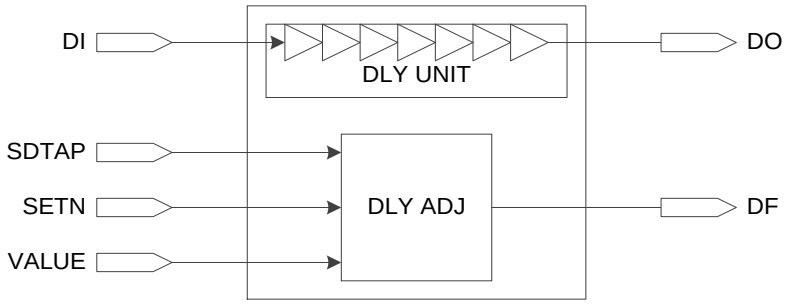
When CI is used as GCLK input, DI, Q, and Q_0-Q_{n-1} cannot be used as I/O input and output.

A description of the I/O logic modules of the GW1NSE series FPGA products is presented below.

IODELAY

See Figure 3-9 for an overview of the IODELAY. Each I/O of the GW1NSE series of SecureFPGA products has an IODELAY cell. A total of 128(0~127) step delay is provided, with one-step delay time of about 30ps.

Figure 3-9 IODELAY



There are two ways to control the delay cell:

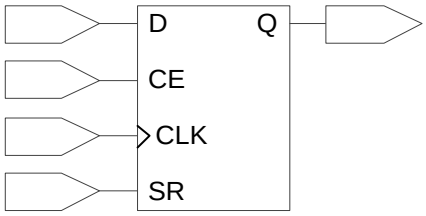
- Static control:

- Dynamic control: usually used to sample delay window together with IEM. The IODELAY cannot be used for both input and output at the same time

I/O Register

See Figure 3-10 for the I/O register in the GW1NSE series of SecureFPGA products. Each I/O provides one input register (IREG), one output register (OREG), and a tristate Register (TRIREG).

Figure 3-10 Register Structure in I/O Logic



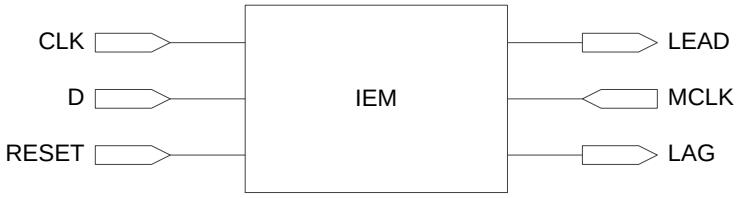
Note!

- CE can be either active ow (0: enable)or active high (1: enable).
- CLK can be either rising edge trigger or falling edge trigger.
- SR can be either synchronous/asynchronous SET or RESET or disable.
- The register can be programmed as register or latch.

IEM

IEM is for sampling clock edge and is used in the generic DDR mode. See Figure 3-11 for the IEM structure.

Figure 3-11 IEM Structure



De-serializer DES

The GW1NSE series of SecureFPGA products provide a simple Serializer SER for each output I/O to support advanced I/O protocols.

Serializer SER

The GW1NSE series of SecureFPGA products provide a simple Serializer SER for each output I/O to support advanced I/O protocols.

3.3.4 I/O Logic Modes

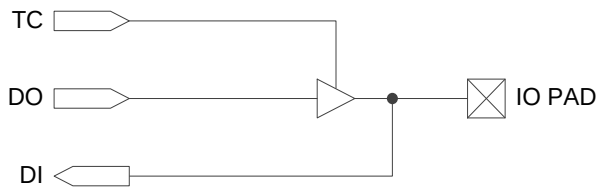
The I/O Logic in the GW1NSE series of SecureFPGA products supports several modes. In each operation, the I/O (or I/O differential pair) can be configured as output, input, and INOUT or tristate output (output signal with tristate control).

Not all the device pins support I/O logic. GW1NSE-2C pins IOL6 (A, B, C…. J) does not support IO logic.

Basic Mode

In basic mode, the I/O Logic is as shown in Figure 3-12, and the TC, DO, and DI signals can connect to the internal cores directly through CRU.

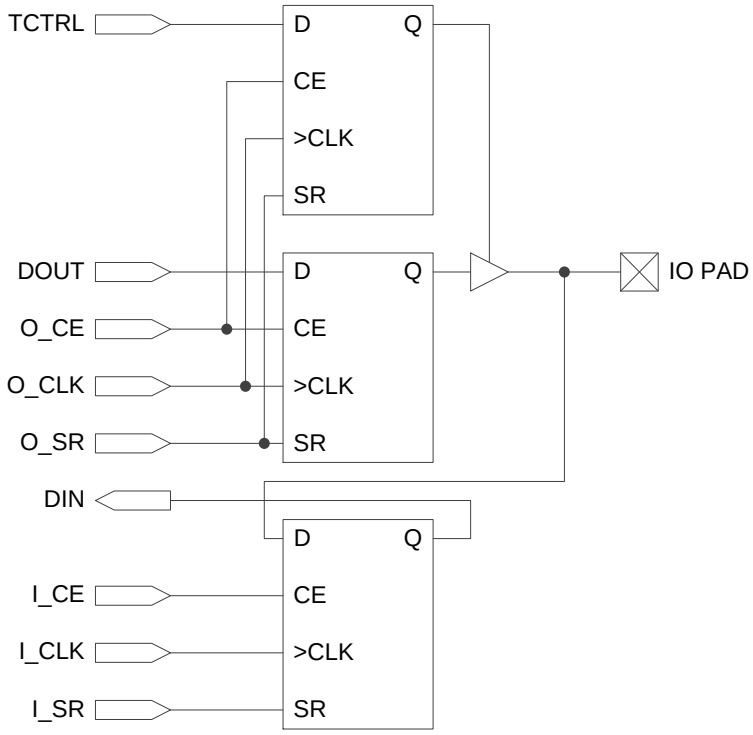
Figure 3-12 I/O Logic in Basic Mode



SDR Mode

In comparison with the basic mode, SDR utilizes the IO register, as shown in Figure 3-13. This can effectively improve IO timing.

Figure 3-13 I/O Logic in SDR Mode



Note!

- CLK enable O_CE and I_CE can be configured as active high or active low;
- O_CLK and I_CLK can be either rising edge trigger or falling edge trigger;
- Local set/reset signal O_SR and I_SR can be either Synchronized reset,Synchronized set, Asynchronous reset, Asynchronous set, or no-function;
- I/O in SDR mode can be configured as basic register or latch.

Generic DDR Mode

Higher speed IO protocols can be supported in generic DDR mode.

Figure 3-14 shows the generic DDR input, with a speed ratio of the internal logic to PAD 1:2.

Figure 3-14 I/O Logic in DDR Input Mode

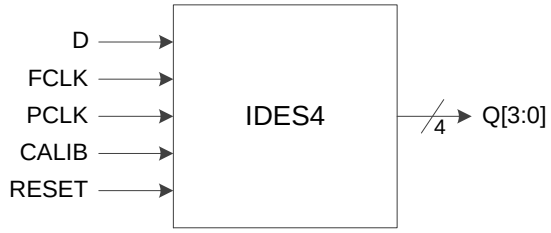
Figure 3-15 shows generic DDR output, with a speed ratio of PAD to FPGA internal logic 2:1.

Figure 3-15 I/O Logic in DDR Output Mode

IDES4

In IDES4 mode, the speed ratio of the PAD to FPGA internal logic is 1:4.

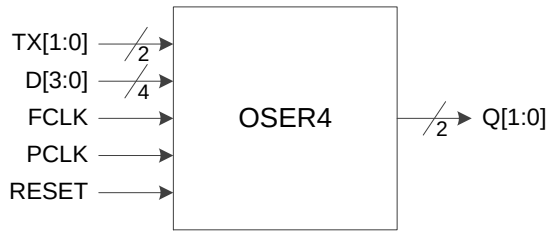
Figure 3-16 I/O Logic in IDES4 Mode



OSER4 Mode

In OSER4 mode, the speed ratio of the PAD to FPGA internal logic is 4:1.

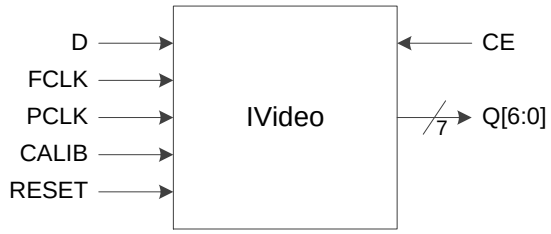
Figure 3-17 I/O Logic in OSER4 Mode



IVideo Mode

In IVideo mode, the speed ratio of the PAD to FPGA internal logic is 1:7.

Figure 3-18 I/O Logic in IVideo Mode



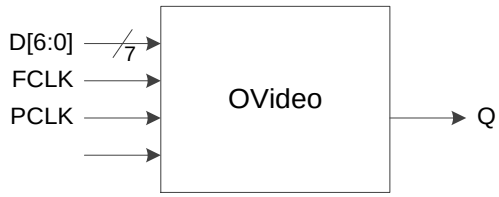
Note!

IVideo and IDES8/10 will occupy the neighboring I/O logic. If the I/O logic of a single port is occupied, the pin can only be programmed in SDR or BASIC mode.

OVideo Mode

In OVideo mode, the speed ratio of the PAD to FPGA internal logic is 7:1.

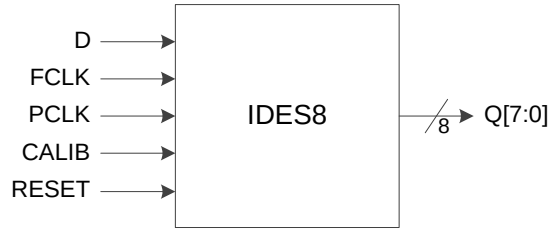
Figure 3-19 I/O Logic in OVideo Mode



IDES8 Mode

In IDES8 mode, the speed ratio of the PAD to FPGA internal logic is 1:8.

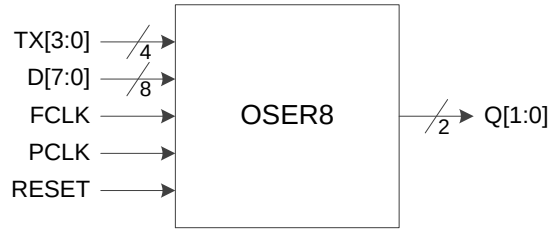
Figure 3-20 I/O Logic in IDES8 Mode



OSER8 Mode

In OSER8 mode, the speed ratio of the PAD to FPGA internal logic is 8:1.

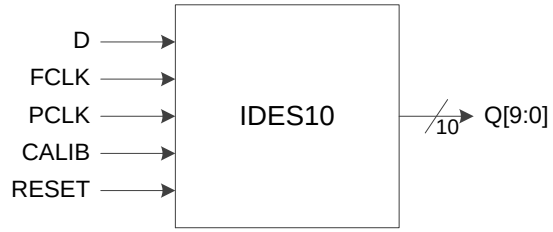
Figure 3-21 I/O Logic in OSER8 Mode



IDES10 Mode

In IDES10 mode, the speed ratio of the PAD to FPGA internal logic is 1:10.

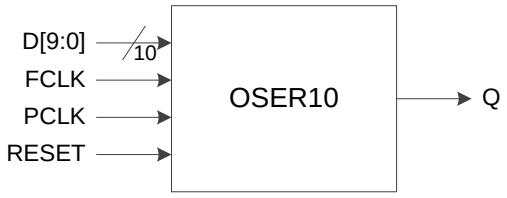
Figure 3-22 I/O Logic in IDES10 Mode



OSER10 Mode

In OSER10 mode, the speed ratio of the PAD to FPGA internal logic is 10:1.

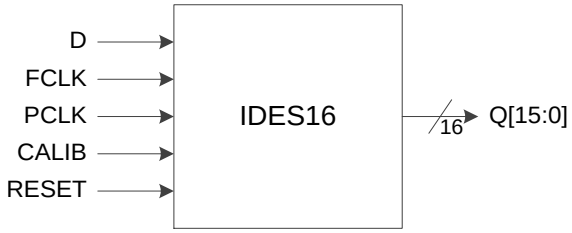
Figure 3-23 I/O Logic in OSER10 Mode



IDES16 Mode

In IDES16 mode, the speed ratio of the PAD to FPGA internal logic is 1:16.

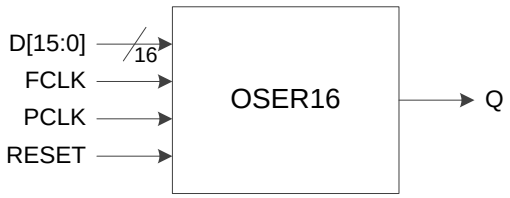
Figure 3-24 I/O Logic in IDES16 Mode



OSER16 Mode

In OSER16 mode, the speed ratio of the PAD to FPGA internal logic is 16:1.

Figure 3-25 I/O Logic in OSER16 Mode



3.4 Block SRAM (BSRAM)

3.4.1 Introduction

The GW1NSE series of SecureFPGA products provide abundant SRAM. The Block SRAM (BSRAM) is embedded as a row in the FPGA array and is different from SSRAM (Shadow SRAM). Each BSRAM occupies three columns of CFU in the FPGA array.

BSRAM supports two usages:

- Used for Cortex-M3 SRAM, providing high-speed read/write functions for Cortex-M3 to ensure system operation. One BSRAM capacity is 16 Kbits (2K-Byte). The capacity of SRAM can be configured as 2K-Byte/4K-Byte/8K-Byte via Gowin YunYuan software. The unused BSRAM can also be the FPGA storage resources.
- Used for FPGA data storage. Each BSRAM can be configured up to

18,432 bits (18Kbits). There are 5 operation modes: Single Port, Dual Port, Semi Dual Port, ROM, and FIFO.

An abundance of BSRAM resources provide a guarantee for the user's high-performance design. BSRAM features:

- Max.18,432 bits per BSRAM
- BSRAM itself can run at 190MHz at max
- Single Port
- Dual Port
- Semi Dual Port
- Parity bits
- ROM
- Data width from 1 to 36 bits
- Mixed clock mode
- Mixed data width mode
- Enable Byte operation for double byte or above
- Asynchronous reset, Synchronous reset
- Normal Read and Write Mode
- Read-before-write Mode
- Write-through Mode

3.4.2 Configuration Mode

The BSRAM mode in the GW1NSE series of SecureFPGA products supports different data bus widths. See Table 3-4.

Table 3-4 Memory Size Configuration

Single Port Mode	Dual Port Mode	Semi-Dual Port Mode	Read Only
16K x 1	16K x 1	16K x 1	16K x 1
8K x 2	8K x 2	8K x 2	8K x 2
4K x 4	4K x 4	4K x 4	4K x 4
2K x 8	2K x 8	2K x 8	2K x 8
1K x 16	1K x 16	1K x 16	1K x 16
512 x 32	-	512 x 32	512 x 32
2K x 9	2K x 9	2K x 9	2K x 9
1K x 18	1K x 18	1K x 18	1K x 18
512 x 36	-	512 x 36	512 x 36

Single Port Mode

In the single port mode, BSRAM can write to or read from one port at one clock edge. During the write operation, the data can show up at the output of BSRAM. NORMAL-WRITE MODE and Write–through Mode can be supported. When the output register is bypassed, the new data will show at the same write clock rising edge.

For further information about Single Port Block Memory ports and the related description, please refer to UG285, Gowin BSRAM & SSRAM User Guide.

Dual Port Mode

BSRAM support dual port mode. The applicable operations are as follows:

- Two independent read
- Two independent write
- An independent read and an independent write at different clock frequencies

For further information about Dual Port Block Memory ports and the related description, please refer to UG285, Gowin BSRAM & SSRAM User Guide.

Semi-Dual Port Mode

Semi-Dual Port supports read and write at the same time on different ports, but it is not possible to write and read to the same port at the same time. The system only supports write on Port A, read on Port B.

For further information about Semi-Dual Port Block Memory ports and the related description, please refer to UG285, Gowin BSRAM & SSRAM User Guide.

Read Only

BSRAM can be configured as ROM. The ROM can be initialized during the device configuration stage, and the ROM data needs to be provided in the initialization file. Initialization completes during the device power-on process.

Each BSRAM can be configured as one 16 Kbits ROM. For further information about Read Only Port Block Memory ports and the related description, please refer to UG285, Gowin BSRAM & SSRAM User Guide.

3.4.3 Mixed Data Bus Width Configuration

The BSRAM in the GW1NSE series of SecureFPGA products supports mixed data bus width operation. In the dual port and semi-dual port modes, the data bus width for read and write can be different. For the configuration options that are available, please see Table 3-5 and Table 3-6 below.

Table 3-5 Dual Port Mixed Read/Write Data Width Configuration

Read Port	Write Port						
	16K x 1	8K x 2	4K x 4	2K x 8	1K x 16	2K x 9	1K x 18
16K x 1	Yes	Yes	Yes	Yes	Yes	N/A	N/A
8K x 2	Yes	Yes	Yes	Yes	Yes	N/A	N/A
4K x 4	Yes	Yes	Yes	Yes	Yes	N/A	N/A
2K x 8	Yes	Yes	Yes	Yes	Yes	N/A	N/A
1K x 16	Yes	Yes	Yes	Yes	Yes	N/A	N/A
2K x 9	N/A	N/A	N/A	N/A	N/A	Yes	Yes
1K x 18	N/A	N/A	N/A	N/A	N/A	Yes	Yes

Table 3-6 Semi Dual Port Mixed Read/Write Data Width Configuration

Read Port	Write Port								
	16K x 1	8K x 2	4K x 4	2K x 8	1K x 16	512 x 32	2K x 9	1K x 18	512 x 36
16K x 1	Yes	Yes	Yes	Yes	Yes	Yes	N/A	N/A	N/A
8K x 2	Yes	Yes	Yes	Yes	Yes	Yes	N/A	N/A	N/A
4K x 4	Yes	Yes	Yes	Yes	Yes	Yes	N/A	N/A	N/A
2K x 8	Yes	Yes	Yes	Yes	Yes	Yes	N/A	N/A	N/A
1K x 16	Yes	Yes	Yes	Yes	Yes	Yes	N/A	N/A	N/A
512x32	Yes	Yes	Yes	Yes	Yes	Yes	N/A	N/A	N/A
2K x 9	N/A	N/A	N/A	N/A	N/A	N/A	Yes	Yes	Yes
1K x 18	N/A	N/A	N/A	N/A	N/A	N/A	Yes	Yes	Yes

3.4.4 Byte-enable

The BSRAM in the GW1NSE series of SecureFPGA products supports byte-enable. For data longer than a byte, the additional bits can be blocked, and only the selected portion can be written into. The blocked bits will be retained for future operation. Read/write enable ports (WREA, WREB), and byte-enable parameter options can be used to control the BSRAM write operation.

3.4.5 Parity Bit

There are parity bits in BSRAMs. The 9th bit in each byte can be used as a parity bit to check the correctness of data transmission. It can also be used for data storage.

3.4.6 Synchronous Operation

- All the input registers of BSRAM support synchronous write;

- The output registers can be used as pipeline register to improve design performance;
- The output registers are bypass-able.

3.4.7 Power up Conditions

BSRAM initialization is supported when powering up. During the power-up process, BSRAM is in standby mode, and all the data outputs are “0”. This also applies in ROM mode.

3.4.8 BSRAM Operation Modes

BSRAM supports five different operations, including two read operations (Bypass Mode and Pipeline Read Mode) and three write operations (Normal Write Mode, Write-through Mode, and Read-before-write Mode).

Read Mode

Read data from the BSRAM via output registers or without using the registers.

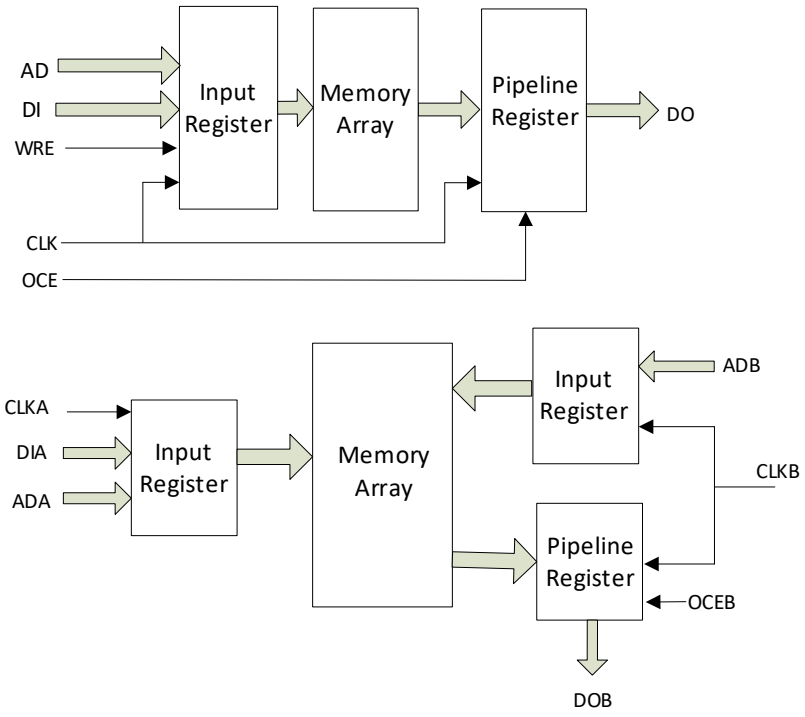
Pipeline Mode

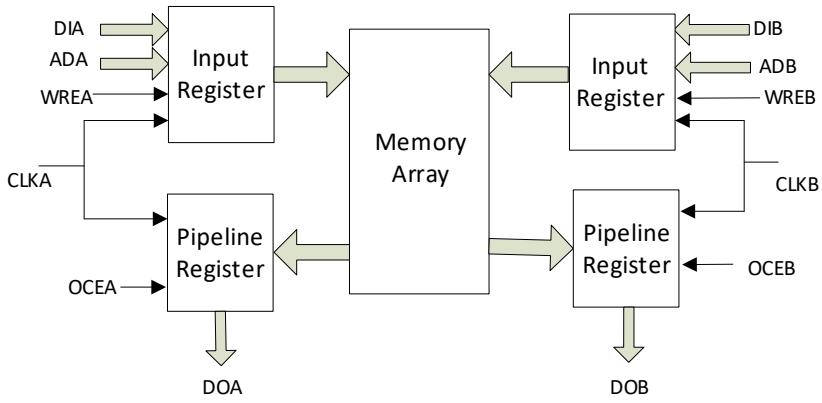
While writing in the BSRAM, the output register and pipeline register are also being written. The data bus can be up to 36 bits in this mode.

Bypass Mode

The output register is not used. The data is kept in the output of memory array.

Figure 3-26 Pipeline Mode in Single Port, Dual Port and Semi-Dual Port





Write Mode

NORMAL WRITE MODE

In this mode, when the user writes data to one port, and the output data of this port does not change. The data written in will not appear at the read port.

WRITE-THROUGH MODE

In this mode, when the user writes data to one port, and the data written in will also appear at the output of this port.

READ-BEFORE-WRITE MODE

In this mode, when the user writes data to one port, and the data written in will be stored in the memory according to the address. The original data in this address will appear at the output of this port.

3.4.9 Clock Operations

Table 3-7 lists the clock operations in different BSRAM modes:

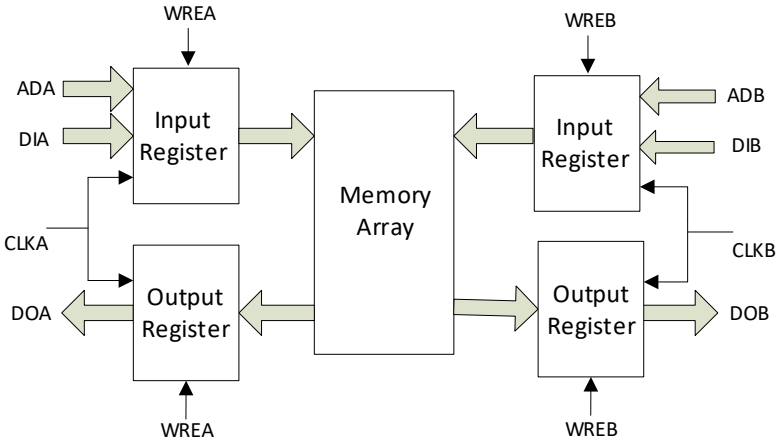
Table 3-7 Clock Operations in Different BSRAM Modes

Clock Operations	Dual Port Mode	Semi-Dual Port Mode	Single Port Mode
Independent Clock Mode	Yes	No	No
Read/Write Clock Mode	Yes	Yes	No
Single Port Clock Mode	No	No	Yes

Independent Clock Mode

Figure 3-27 shows the independent clocks in dual port mode with each port with one clock. CLKA controls all the registers at Port A; CLKB controls all the registers at Port B.

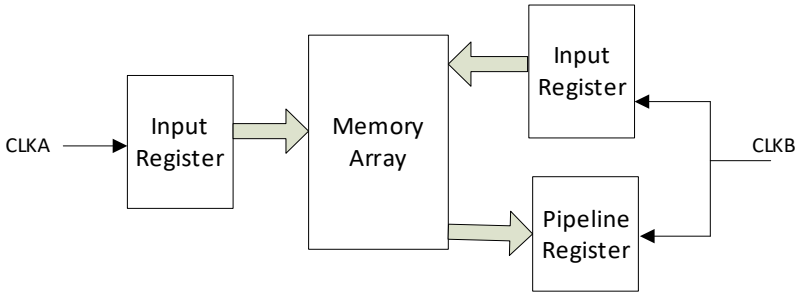
Figure 3-27 Independent Clock Mode



Read/Write Clock Operation

Figure 3-28 shows the read/write clock operations in the semi-dual port mode with one clock at each port. The write clock (CLKA) controls Port A data inputs, write address and read/write enable signals. The read clock (CLKB) controls Port B data output, read address, and read enable signals.

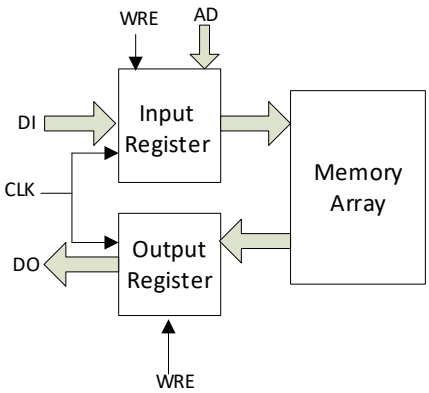
Figure 3-28 Read/Write Clock Mode



Single Port Clock Mode

Figure 3-29shows the clock operation in single port mode.

Figure 3-29 Single Port Clock Mode



3.5 User Flash (GW1NSE-2C)

GW1NSE series of SecureFPGA products offer 128 KB User Flash with the following functions:

- Used for Cortex-M3 programming memory. User Flash can only be read and does not support the other two functions;
- Offers non-volatile memory for users and does not support the other two functions;
- In DUAL BOOT mode, on-chip downloaded flash is the primary memory for data bitstream; user flash is used as the secondary memory for data bitstream; the user flash used for this function does not support the other two functions.

Main features are as follows:

- 32 bits data input/output
- Page architecture
- 128 x 32 bits page size
- 256 pages in total
- Fast read, write, and erase
- Read access time 30ns
- Write time 30us
- Page erasure time 2ms
- Macro erasure time 10ms
- Lower power consumption
- IDLE 100uA
- Read operation current 60 uA/MHz
- Write operation current 2.4mA
- Erase operation current 2.4 mA
- 100,000 write/erase cycles
- Minimum10 years data retention

For further detailed information of the embedded user Flash, please refer to UG295, Gowin User Flash User Guide.

3.6 User Flash (GW1NSE-4C)

GW1NSE-4C offers 32 KB User Flash with the following two usages and they cannot be used simultaneously.

- One is used for Cortex-M3 processor ARM programs storage. In this way, the User Flash can only be read and cannot be written.
- One is used as the non-volatile memory resource.

The user Flash memory is composed of row memory and column memory. One row memory is composed of 64 column memories. The capacity of one column memory is 32 bits, and the capacity of one row memory is 64*32=2048 bits. Page erase is supported, and one page capacity is 2048 bytes, i.e., one page includes 8 rows. The features are shown below:

- 10,000 write cycles
- Greater than10 years Data Retention at +85 ℃

- Data Width: 32
- Capacity: 128 rows x 64 columns x 32 = 256kbits
- Page Erase Capability: 2,048 bytes per page
- Fast Page Erasure/Word Programming Operation
- Clock frequency: 40 MHz
- Word Programming Time:≤16 μs
- Page Erasure Time:≤120 ms
- Electric current
  - Read current/duration:2.19 mA/25 ns (V_{CC}) & 0.5 mA/25 ns (V_{CCX}) (MAX)
  - Program / Erase operation: 12/12 mA(MAX)

For further detailed information of the embedded user Flash, please refer to UG295, Gowin User Flash User Guide.

3.7 OTP Authentication Code

During the factory authentication provisioning process, the Authentication Code, which is based on SRAM PUF (Physical Un-clone-able Factor), is pre-stored in the internal Non-volatile 128KB User Flash memory of SecureFPGA.

After provisioning, user can create their own secure application software, which is compiled and linked with the IID Secure Software library with various encrypt / decrypt / Private-Key-Generation / Public-Key-Generation / Secure-Communication, etc. All the application functions rely on the pre-stored unique and unchanged Authentication Code for activation.

OTP Authentication Code features are as follows:

- PUF Based Secure Element
  - Root key pair generated based on intrinsic properties of internal device SRAM
  - Key pair never stored in device and re-generated each power up
- Intrinsic ID Broadkey Pro Security Library
  - Includes device identification, encryption and symmetric and asymmetric key generation
  - Example code for calling user functions
- Factory Provisioning
  - Device initialized with a key pair based on SRAM PUF
  - Private key never exposed during the manufacturing process
  - CSR and Certificate generated for each individual device
- Common User Applications
  - Secure Boot
  - Key and Signature Generation
  - Encryption/Decryption

3.8 Cortex-M3

3.8.1 Introduction

GW1NSE-2C/GW1NSE-4C is a system-on-chip FPGA device that incorporates a microprocessor system hard core, Gowin FPGA fabric, and other standard peripherals and featured hard cores, including USB2.0 PHY,

ADC, 128 K-Byte Flash, 8 KB Block RAM, PLL, and OSC. The embedded microprocessor system contains a low-power, low-cost and high-performance ARM Cortex-M3 32-bit RISC. The flexible FPGA fabric serves as user programmable peripherals, or soft-core IPs.

The embedded microprocessor system consists of the processor block, with ARM Cortex-M3 32-bit RISC core and associated supporting bus system that connects to harden standard peripherals. The FPGA fabric contains a rich programmable logic resource called a Configured Functional Unit (CFU). This offers a flexible architecture that allows the user to employ peripherals with the microprocessor system. This can be achieved either by parameterized soft-core IPs or customized Verilog design to go through Gowin EDA Design Software from Synthesis, FPGA Place Rout to bit-file download into GW1NSE-2C. The microprosessor system only interfaces with the FPGA fabric and JTAG config-core internally with no access to the I/O Blocks of GW1NSE-2C.

The bus system consists of AHB-Lite Bus, AHB2APB Bridge, and two APB Bus: APB1 and APB2.

The microprocessor system relies on AHB bus to access FPGA side sub-memory system which has a pre-implemented sub-memory system controller for read-only-access 128 KB Flash-ROM and read/write-access 8 KB BSRAM. Upon Power-On boot loading, Cortex-M3 loads instructions and data that are pre-stored in the Flash-ROM, and transfers it to the BSRAM before initiating the execution.

In addition, there are two AHB bus extension ports: INTEXP0 and TARGEXP0. Each of these AHB extension ports provides a 126-bit AHB bus interconnecting to any high-speed User programmable peripherals implemented within the FPGA. A GPIO block interconnects the AHB bus with the FPGA fabric to allow the user to implement general purpose I/O functions in FPGA.

In terms of the two APB Bus (APB1 and APB2), APB1 interconnects with two timers (Timer0 and Timer1), two UARTs (Uart0 and Uart1), and one watchdog. Two UARTs connect to the FPGA directly. The two timers and the watchdog are controlled and used within the microprocessor system and are accessed through REG. The APB2 bus connects directly to the FPGA.

The processor block consists of Cortex-M3 core, bus matrix, Nested Vector Interrupt Controller (NVIC), Debug Access Port (DAP), and time stamp.

The Cortex-M3 core relies on the bus-matrix to access its supporting bus system (AHB-Lite Bus, AHB2APB Bridge, and two APB Bus: APB1 and APB2).

NVIC offers USER_INT0 and USER_INT1, serving as interrupt requests to NVIC from user implementing peripherals in FPGA fabric. The DAP contains JTAG DAP and also Trace-Port-Interface-Unit (TPIU).

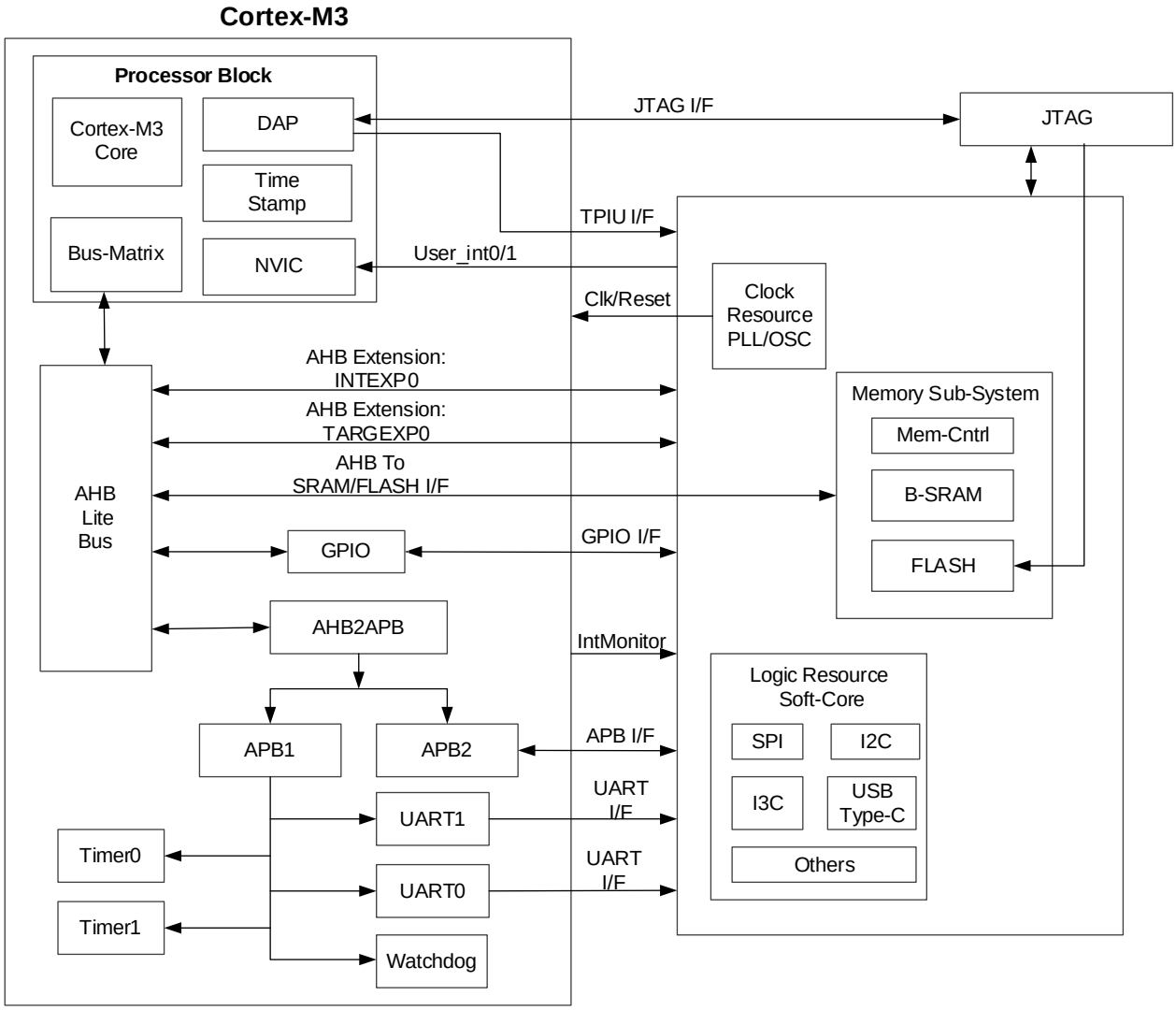
The Microprocessor System also provides an interrupt monitor signal, which combines GPIO interrupts as well as APB1 peripherals (UART0,

UART1, Timer0, Timer1, Watchdog) interrupts, back to the FPGA fabric to report the current run-time interrupt Status of the Microprocessor System.

FPGA fabric takes advantage of its rich Clocking Resource (PLL, OSC) and provides the Main Clock, Power-On Reset and System Reset signals to the embedded microprocessor system.

See Figure 3-30 for the Cortex-M3 architecture.

Figure 3-30 Cortex-M3 Architecture



3.8.2 Cortex-M3

Features of the microprocessor system embedded in GW1NSE-2C/GW1NSE-4C are as follows:

- Compact core
- Thumb-2 instruction set, delivering the high-performance expected of an ARM core in the memory size usually
- Associated with 8 bits and 16 bits devices; typically, in the range of a few kilobytes of memory for microcontroller class applications
- Rapid application execution through Harvard architecture characterized by separate buses for instruction and data

- Achieves exceptional interrupt handling, by implementing the register manipulations required for handling an interrupt in hardware.
- Deterministic, fast interrupt processing.
- Memory protection unit (MPU), providing a privileged mode for protecting operation system functionality
- Migration from the ARM7™ processor family for better performance and power efficiency
- Full-featured debug solution
  - JTAG Debug Port (JTAG)
  - Flash Patch and Breakpoint (FPB) unit for implementing breakpoints
  - Data Watchpoint and Trigger (DWT) unit for implementing watchpoints, trigger resources, and system profiling
  - Instrumentation Trace Macrocell (ITM) for support of print style debugging
  - Trace Port Interface Unit (TPIU) for bridging to a Trace Port Analyzer

3.8.3 Bus-Matrix

The bus-matrix is used to connect the Cortex-M3 processor and debug port with an external AHB bus. **Connections between bus-matrix and AHB bus:**

- ICode bus: 32bit AHBLite bus, used for fetching instructions and vectors from code space;
- DCode bus: 32bit AHBLite bus, used for data loading/storage and debug access;
- System bus: 32bit AHBLite bus, used for fetching instructions and vectors from system space, data loading/storage and debug access;
- APB: 32bit APB bus, used for external space data loading/storage and debug access.

The bus-matrix controls the following functions as below:

- Unaligned accesses: Converts the unaligned processor access to aligned access;
- Bit-banding: converts the alias access of Bit_band to Bit_band space access;
- Write buffer: Bus-matrix contains one write-buffer, ensuring that the processor core is not affected by bus delay.

3.8.4 NVIC

NVIC features:

- Supports low-latency interrupt processing up to 26 interrupts
- Two external user defined interrupts: USER_INT0 and USER_INT1
- A programmable priority level of 0-7 for each interrupt. A higher level corresponds to a lower priority; as such level 0 is the highest interrupt priority
- Low-latency exception and interrupt handling

- Dynamic reprioritization of interrupts
- The processor automatically stacks its state on exception entry and unstacks this state on exception exit, with no instruction overhead.

Table 3-8 NVIC Address Table

Address	Name	Type	Description
0x00000000	_StackTop	Read only	Top of stack interrupt
0x00000004	Reset_Handler	Read only	Reset interrupt
0x00000008	NMI_Handler	Read only	NMI interrupt
0x0000000C	HardFault_Handler	Read only	Hard fault interrupt
0x00000010	MemMange_Handler	Read only	MPU fault interrupt
0x00000014	BusFault_Handler	Read/Write	Bus fault interrupt
0x00000018	UsageFault_Handler	Read only	Usage fault interrupt
0x0000002C	SVC_Handler	Read/Write	SVCall interrupt
0x00000030	DebugMon_Handler	Read only	Debug monitor interrupt
0x00000038	PendSV_Handler	Read / Write / Read only	Pending interrupt
0x0000003C	SysTick_Handler	Read/Write	System timer interrupt
External interrupt			
0x00000040	UART0_Handler	Read/Write	UART0 reception and sending interrupt
0x00000048	UART1_Handler	Read/Write	UART1 reception and sending interrupt
0x00000058	PORT0_COMB_Handler	Read/Write	GPIO0 interrupt
0x00000060	TIMER0_Handler	Read/Write	TIMER0 interrupt
0x00000064	TIMER1_Handler	Read/Write	TIMER1 interrupt
0x00000070	UARTOVF_Handler	Read/Write	UART0/UART1 overflow interrupt
0x00000074	USER_INT0	Read/Write	Flash system error interrupt
0x00000078	USER_INT1	Read/Write	Embedded flash interrupt
0x00000080	PORT0_0_Handler	Read/Write	GPIO0 Pin 0 interrupt
0x00000084	PORT0_1_Handler	Read/Write	GPIO0 Pin 1 interrupt
0x00000088	PORT0_2_Handler	Read/Write	GPIO0 Pin 2 interrupt
0x0000008C	PORT0_3_Handler	Read/Write	GPIO0 Pin 3 interrupt
0x00000090	PORT0_4_Handler	Read/Write	GPIO0 Pin 4 interrupt
0x00000094	PORT0_5_Handler	Read/Write	GPIO0 Pin 5 interrupt
0x00000098	PORT0_6_Handler	Read/Write	GPIO0 Pin 6 interrupt
0x0000009C	PORT0_7_Handler	Read/Write	GPIO0 Pin 7 interrupt
0x000000A0	PORT0_8_Handler	Read/Write	GPIO0 Pin 8 interrupt
0x000000A4	PORT0_9_Handler	Read/Write	GPIO0 Pin 9 interrupt
0x000000A8	PORT0_10_Handler	Read/Write	GPIO0 Pin 10 interrupt
0x000000AC	PORT0_11_Handler	Read/Write	GPIO0 Pin 11 interrupt
0x000000B0	PORT0_12_Handler	Read/Write	GPIO0 Pin 12 interrupt
0x000000B4	PORT0_13_Handler	Read/Write	GPIO0 Pin 13 interrupt
0x000000B8	PORT0_14_Handler	Read/Write	GPIO0 Pin 14 interrupt

Address	Name	Type	Description
0x000000BC	PORT0_15_Handler	Read/Write	GPIO0 Pin 15 interrupt

3.8.5 Boot Loader

The boot loader loads the initial stack pointer value from the program memory, and branches to the reset handler that the reset vector specifies in the program memory.

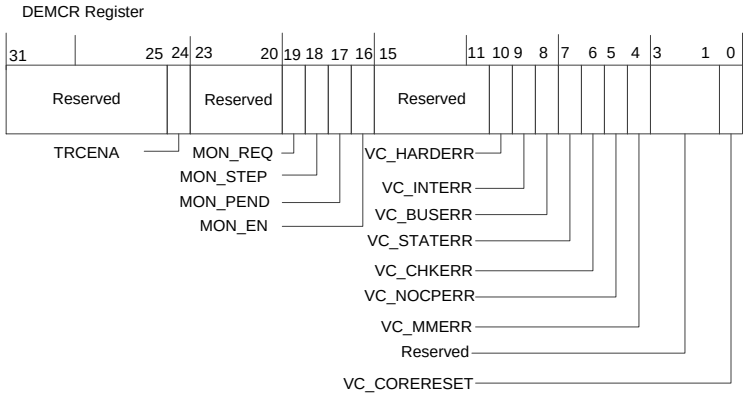
The current boot loader is based on UART Message Monitor which is easy to interface as a communication port with PC host. Below is an example of how to deploy the boot loader:

- Power-on reset to enter the reset handler to call the boot loader;
- Setup UART0 registers, such as BAUDIV and CTRL, to program the appropriate TX speed rate for the send and receive function;
- Begin Flash loader subroutine execution such as memory test, timer0, and timer1 tests etc;
- Write a 0x4 character (EOP) to terminate the program.

3.8.6 TimeStamp

A 48 bits timestamp counter is included and connected to the ITM. It is clock gated and enabled by the Trace Enable (TRCENA) bit of DEMCR (0xE000EDFC) Debug Exception and monitor control register, which is a global enable bit that enables both the Data Watch Trace (DWT) and Intrumental Trace Module (ITM) on behalf of the debug of the Cortex-M3 microprocessor. The time stamp generator is used during the debug process to set up the break point and marching step, etc.

Figure 3-31 DEMCR Register



Note!

TRCENA is the global enable for DWT and ITM features:

- 0: DWT and ITM units disabled.
- 1: DWT and ITM units enabled.

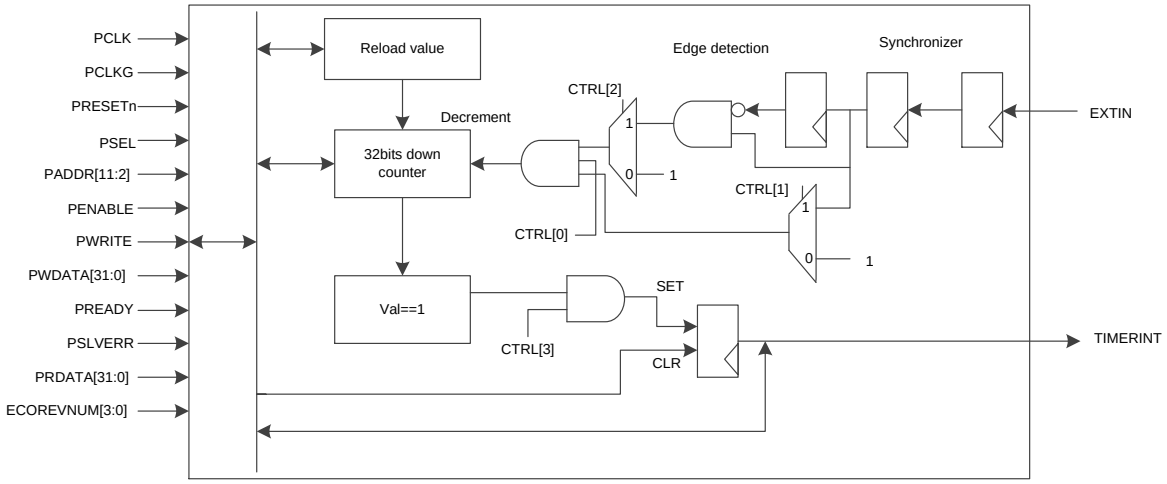
3.8.7 Timer

GW1NSE-2C/GW1NSE-4C offers an embedded microprocessor system that contains two synchronous standard timers: Timer0 and Timer1. These can be accessed and controlled through APB1 bus.

Timer0 and Timer1 are 32 bits down-counter with the following features:

- Users can generate an interrupt request signal, TIMERINT, when the counter reaches 0. The interrupt request is held until it is cleared by writing to the INTCLEAR Register.
- Users can employ the zero-to-one transition of the external input signal, EXTIN, as a timer enable.
- If the timer count reaches 0 and, at the same time, the software clears a previous interrupt status, the interrupt status is set to 1.
- The external clock, EXTIN, must be slower than half of the peripheral clock because it is sampled by a double flip-flop before going through edge-detection logic when the external inputs act as a clock.
- Timer0: EXTIN is hard-wired to GPIO[1]
- Timer1: EXTIN is hard-wired to GPIO[6]

Figure 3-32 Timer0/ Timer1 Structure View



The Timer0/Timer1 register is as shown in Table 3-18. The Timer0 base address is 0 x 40000000, and the Timer1 base address is 0x40001000.

Table 3-9 Timer0/Timer1 Register

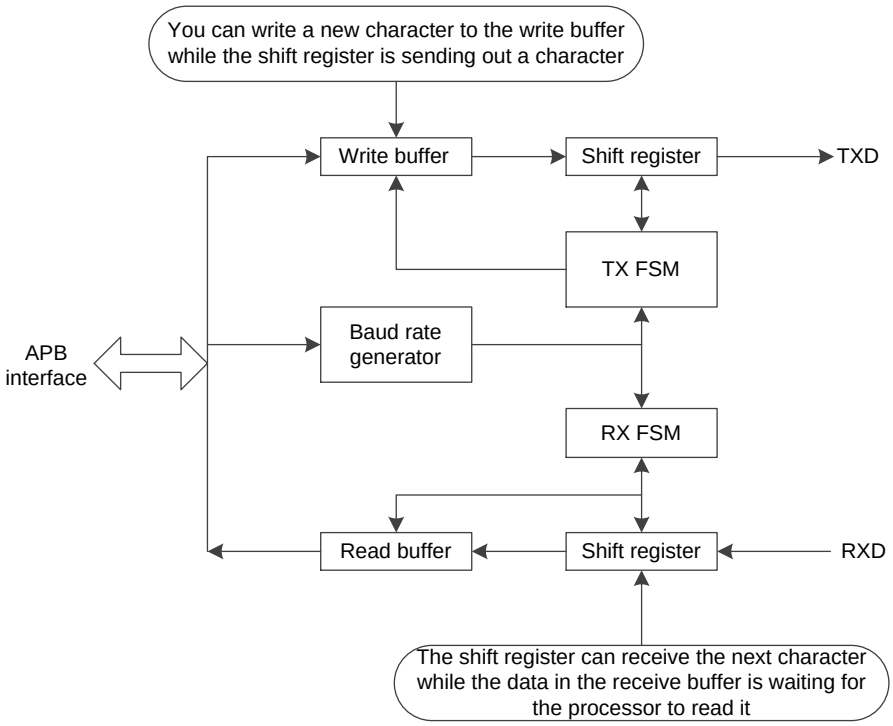
Name	Base Offset	Type	Data Width	Reset Value	Description
CTRL	0x000	Read/Write	4	0x0	[3]: System timer interrupt enable [2]: Select external input as clock [1]: Select external input as enable [0]: Enable
VALUE	0x004	Read/Write	32	0x00000000	Current value
RELOAD	0x008	Read/Write	32	0x00000000	Reload value. Write to this register to set the current value.
INTSTATUS/ INTCLEAR	0x00C	Read/Write	1	0x0	[0]: Timer interrupt. Write one to clear.
PID4	0XFD0	Read only	8	0x04	Peripheral ID Register 4
PID5	0XFD4	Read only	8	0x00	Peripheral ID Register 5
PID6	0XFD8	Read only	8	0x00	Peripheral ID Register 6
PID7	0XFDC	Read only	8	0x00	Peripheral ID Register 7
PID0	0XFE0	Read only	8	0x22	Peripheral ID Register 0
PID1	0XFE4	Read only	8	0XB8	Peripheral ID Register 1
PID2	0XFE8	Read only	8	0X1B	Peripheral ID Register 2
PID3	0XFEC	Read only	8	0X00	Peripheral ID Register 3
CID0	0XFF0	Read only	8	0X0D	Component ID Register 0
CID1	0XFF4	Read only	8	0XF0	Component ID Register 1
CID2	0XFF8	Read only	8	0X05	Component ID Register 2
CID3	0XFFC	Read only	8	0XB1	Component ID Register 3

3.8.8 UART

The GW1NSE-2C/GW1NSE-4C embedded with microprocessor system contains two UART: UART0 and UART1. These can be accessed and controlled through APB1 bus, it supports Max. baud rate of 921.6Kbits/s.

UART0 and UART1 support 8 bits communication without parity and one stop bit.

Figure 3-33 APB UART Buffering



UART0 and UART support a high-speed test mode. When CTRL[6] is set to 1, the serial data is transmitted at one bit per clock cycle. This enables you to send text messages in a much shorter simulation time. The APB interface always sends an "OK" response with no wait state. You must program the baud rate divider register BAUDDIV before enabling the UART.

The BAUDTICK output pulses at a frequency of 16 times that of the programmed baud rate. You can use this external signal for capturing UART data in a synchronous environment. The TXEN output signal indicates the status of CTRL[0]. You can use this signal to switch a bidirectional I/O pin in a silicon device to UART data output mode automatically when the UART transmission feature is enabled.

The buffer overrun status in the STATE field is used to drive the overrun interrupt signals. Therefore, clearing the buffer overrun status de-asserts the overrun interrupt, and clearing the overrun interrupt bit also clears the buffer overrun status bit in the STATE field.

See Table 3-19 for the UART Register Description. The UART0 base address is 0x40004000, and the UART1 base address is 0x40005000.

Table 3-10 UART0/UART1 Register

Name	Base Offset	Type	Data Width	Reset Value	Description
DATA	0x000	Read/Write	8	0x--	8 bits data Read: Received data. Write: Transmit data.
STATE	0x004	Read/Write	4	0x0	[3]: RX buffer overrun, write 1 to clear. [2]: TX buffer overrun, write 1 to clear. [1]: RX buffer full, read-only. [0]: TX buffer full, read-only.
CTRL	0x008	Read/Write	7	0x00	[6]：High-speed test mode for TX only. [5]：RX overrun interrupt enable. [4]：TX overrun interrupt enable. [3]：RX interrupt enable. [2]：TX interrupt enable. [1]：RX enable. [0]：TX enable.
INTSTATUS/ INTCLEAR	0x00C	Read/Write	4	0x0	[3]：RX overrun interrupt, write 1 to clear. [2]：TX overrun interrupt, write 1 to clear. [1]：RX interrupt, write 1 to clear. [0]：TX interrupt, write 1 to clear.
BAUDDIV	0x010	Read/Write	20	0x00000	[19:0]: Baud rate divider. The minimum number is 16.
PID4	0XFD0	Read only	8	0x04	Peripheral ID Register 4
PID5	0XFD4	Read only	8	0x00	Peripheral ID Register 5
PID6	0XFD8	Read only	8	0x00	Peripheral ID Register 6
PID7	0XFDC	Read only	8	0x00	Peripheral ID Register 7
PID0	0XFE0	Read only	8	0x21	Peripheral ID Register 0
PID1	0XFE4	Read only	8	0XB8	Peripheral ID Register 1
PID2	0XFE8	Read only	8	0X1B	Peripheral ID Register 2
PID3	0XFEC	Read only	8	0X00	Peripheral ID Register 3
CID0	0XFF0	Read only	8	0X0D	Component ID Register 0
CID1	0XFF4	Read only	8	0XF0	Component ID Register 1
CID2	0XFF8	Read only	8	0X05	Component ID Register 2
CID3	0XFFC	Read only	8	0XB1	Component ID Register 3

3.8.9 Watchdog

The GW1NSE-2C/GW1NSE-4C embedded with microprocessor system contains one watchdog module. This can be accessed and controlled through the APB1 bus.

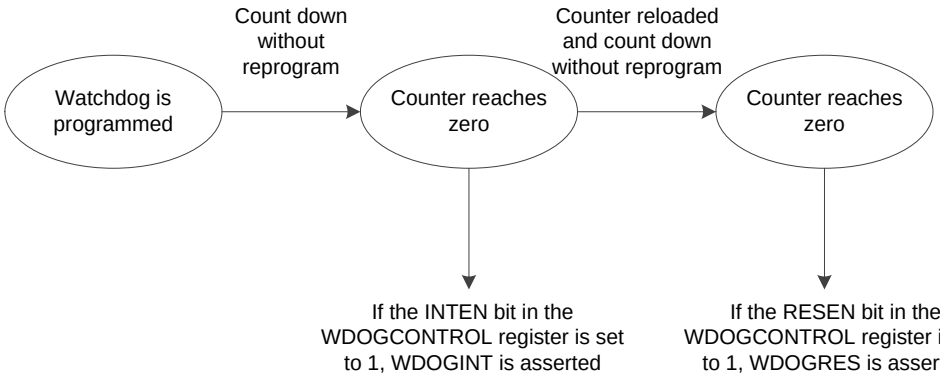
The APB watchdog module is based on a 32 bits down-counter that is initialized from the reload register, WDOGLOAD.

The watchdog module generates a regular interrupt, WDOGINT, depending on a programmed value. The counter decrements by one on each positive clock edge of WDOGCLK when the clock enable, WDOGCLKEN, is HIGH. The watchdog monitors the interrupt and asserts a reset request WDOGRES signal when the counter reaches 0, and the counter is stopped. On the next enabled WDOGCLK clock edge, the counter is reloaded from the WDOGLOAD register and the countdown sequence continues.

The watchdog module applies a reset to a system in the event of a software failure, providing a way to recover from software crashes. For example, if the interrupt is not cleared by the time the counter next reaches 0, the watchdog module initiates the reset signal.

Watchdog operates as follows.

Figure 3-34 Watchdog Operation



The watchdog register is as shown in Table 3-20. The watchdog base address is 0x40008000.

Table 3-11 Watchdog Register

Name	Base Offset	Type	Data Width	Reset Value	Description
WDOGLOAD	0x00	Read/Write	32	0xFFFFFFFF	Watchdog Load Register
WDOGVALUE	0x04	Read only	32	0xFFFFFFFF	Watchdog Value Register
WDOGCONTROL	0x08	Read/Write	2	0x0	Watchdog Control Register [1]： [0]：
WDOGINTCLR	0x0C	Write only	-	0x-	Watchdog Clear Interrupt Register
WDOGRIS	0x10	Read only	1	0x0	Watchdog Raw Interrupt Status Register
WDOGMIS	0x14	Read only	1	0x0	Watchdog Interrupt Status Register
WDOGLOCK	0xC00	Read/Write	32	0x0	Watchdog Lock Register
WDOGTCR	0xF00	Read/Write	1	0x0	Watchdog Integration Test Control Register
WDOGTOP	0xF04	Write only	2	0x0	Watchdog Integration Test Output Set Register
WDOGPERIPHID4	0XFD0	Read only	8	0x04	Peripheral ID Register 4
WDOGPERIPHID5	0XFD4	Read only	8	0x00	Peripheral ID Register 5
WDOGPERIPHID6	0XFD8	Read only	8	0x00	Peripheral ID Register 6
WDOGPERIPHID7	0XFDC	Read only	8	0x00	Peripheral ID Register 7
WDOGPERIPHID0	0XFE0	Read only	8	0x24	Peripheral ID Register 0
WDOGPERIPHID1	0XFE4	Read only	8	0XB8	Peripheral ID Register 1
WDOGPERIPHID2	0XFE8	Read only	8	0X1B	Peripheral ID Register 2
WDOGPERIPHID3	0XFEC	Read only	8	0X00	Peripheral ID Register 3
WDOGPCELLID0	0XFF0	Read only	8	0X0D	Component ID Register 0
WDOGPCELLID1	0XFF4	Read only	8	0XF0	Component ID Register 1
WDOGPCELLID2	0XFF8	Read only	8	0X05	Component ID Register 2
WDOGPCELLID3	0XFFC	Read only	8	0XB1	Component ID Register 3

3.8.10 GPIO

The GW1NSE-2C/GW1NSE-4C microprocessor system communicates with the GPIO block through the AHB bus. The GIPO block interconnects with the FPGA. GPIO provides a 16 bits I/O interface with the following properties:

- Programmable interrupt generation capability. You can configure each bit of the I/O pins to generate interrupts;
- Bit masking support using address values;
- Registers for alternate function switching with pin multiplexing support;
- Thread safe operation by providing separate set and clear addresses for control registers.

The GPIO register is as shown in Table 3-21. The GPIO base address is 0 x 40010000.

Table 3-12 GPIO Register

Name	Base Offset	Type	Data Width	Reset Value	Description
DATA	0x0000	Read/Write	16	0x----	Data value [15:0]
DATAOUT	0x0004	Read/Write	16	0x0000	Data output register value [15:0]
OUTENSET	0x0010	Read/Write	16	0x0000	Output enable set [15:0] Write 1: Set the output enable bit. Write 0: No effect. Read 1: Indicates the signal direction as output. Read 0: Indicates the signal direction as input.
OUTENCLR	0x0014	Read/Write	16	0x0000	Output enable clear [15:0]
ALTFUNCSET	0x0018	Read/Write	16	0x0000	Alternative function set [15:0] Write 1: Sets the ALTFUNC bit. Write 0: No effect. Read 0: GPIO as I/O Read 1: ALTFUNC Function
ALTFUNCCLR	0x001C	Read/Write	16	0x0000	Alternative function clear [15:0]
INTENSET	0x0020	Read/Write	16	0x0000	Interrupt enable set [15:0] Write 1: Sets the enable bit. Write 0: No effect. Read 0: Interrupt disabled. Read 1: Interrupt enabled.
INTENCLR	0x0024	Read/Write	16	0x0000	Interrupt enable clear [15:0] Write 1: Clear the enable bit. Write 0: No effect. Read 0: Interrupt disabled. Read 1: Interrupt enabled.

Name	Base Offset	Type	Data Width	Reset Value	Description
INTTYPESET	0x0028	Read/Write	16	0x0000	Interrupt type set [15:0]
INTTYPECLR	0x002C	Read/Write	16	0x0000	Interrupt type clear [15:0]
INTPOLSET	0x0030	Read/Write	16	0x0000	Polarity-level, edge interrupt request configuration [15:0]
INTPOLCLR	0x0034	Read/Write	16	0x0000	Polarity-level, edge interrupt request configuration [15:0]
INTSTATUS/ INTCLEAR	0x0038	Read/Write	16	0x0000	Read interrupt status register Write 1: Clear the interrupt request
MASKLOWBYTE	0x0400-0x07FC	Read/Write	16	0x0000	–
MASKHIGHBYTE	0x0800-0x0BFC	Read/Write	16	0x0000	–
Reserved	0x0C00-0x0FCF	–	–	–	Reserved
PID4	0XFD0	Read only	8	0x04	Peripheral ID Register 4
PID5	0XFD4	Read only	8	0x00	Peripheral ID Register 5
PID6	0XFD8	Read only	8	0x00	Peripheral ID Register 6
PID7	0XFDC	Read only	8	0x00	Peripheral ID Register 7
PID0	0XFE0	Read only	8	0x20	Peripheral ID Register 0
PID1	0XFE4	Read only	8	0XB8	Peripheral ID Register 1
PID2	0XFE8	Read only	8	0X1B	Peripheral ID Register 2
PID3	0XFEC	Read only	8	0X00	Peripheral ID Register 3
CID0	0XFF0	Read only	8	0X0D	Component ID Register 0
CID1	0XFF4	Read only	8	0XF0	Component ID Register 1
CID2	0XFF8	Read only	8	0X05	Component ID Register 2
CID3	0XFFC	Read only	8	0XB1	Component ID Register 3

3.8.11 Debug Access Port

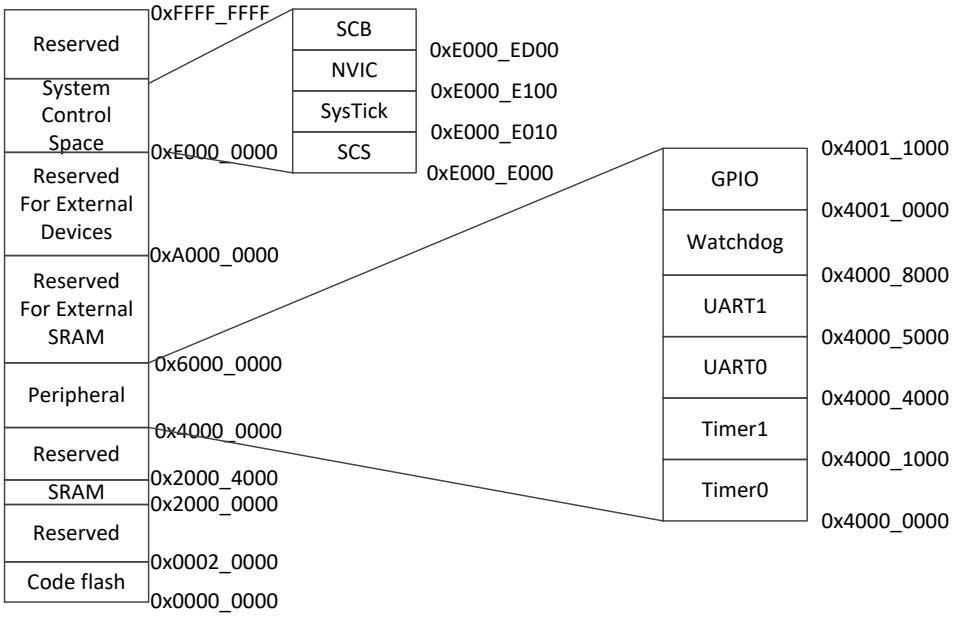
The Cortex-M3 processor block contains a DAP that consist of a JTAG DAP and a TPIU port. Both interface to the FPGA Fabric. The JTAG-DAP is based on the IEEE1149.1 Joint Test Action Group Boundary-Scan Standard.

JTAG-DP functions consist of the following three parts:

- JTAG-DP sate machine
- Instruction register (IR) and the related IR scan chain, which are used to control JTAG and the current register actions
- DR register and the related DR scan chain, which connect with the JTAG-DP register.

3.8.12 Memory Mapping

Figure 3-35 Memory Mapping



3.8.13 Ports Signal Description

Table 3-13 Cortex-M3 Ports Signal

Port Name	I/O	Description
Clock and Reset signal		
FCLK	I	Clock signal
PORESETN	I	Power on reset
SYSRESETN	I	System Reset
GPIO signals		
IOEXPOUTPUTO [15:0]	O	GPIO output
IOEXPOUTPUTENO [15:0]	O	GPIO output enable
IOEXPINPUTI [15:0]	I	GPIO input
UART signal		
UART0TXDO	O	UART0 sends signals
UART1TXDO	O	UART1 sends signals
UART0BAUDTICK	O	UART0 Baud rate clock
UART1BAUDTICK	O	UART0 Baud rate clock
UART0RXDI	I	UART0 receives signals
UART1RXDI	I	UART1 receives signals
AHB Lite TO SRAM signals		
MTXHRESETN	O	SRAM reset signal
SRAM0ADDR [12:0]	O	SRAM read/write address
SRAM0WREN	O	SRAM read/write enable

Port Name	I/O	Description
SRAM0WDATA [31:0]	O	SRAM writes data
SRAM0CS	O	SRAM chip select
SRAM0RDATA	I	SRAM reads data
AHB Lite TO Flash interface signals		
TARGFLASH0HSEL	O	Flash transmits the select signals
TARGFLASH0HADDR [28:0]	O	Flash transmits read/write address
TARGFLASH0HTRANS [1:0]	O	Flash transmission types
TARGFLASH0HWRITE	O	Flash transmits read/write enable
TARGFLASH0HSIZE [2:0]	O	Flash transmits data width
TARGFLASH0HBURST [2:0]	O	Flash transmits burst length configuration signals
TARGFLASH0HPROT [3:0]	O	Flash transmits protection and control types
TARGFLASH0MEMATTR [1:0]	O	Flash transmits memory attributes
TARGFLASH0EXREQ	O	Flash transmits exclusive request
TARGFLASH0HMASTER [3:0]	O	Flash transmits master selection
TARGFLASH0HWDATA [31:0]	O	Flash transmits the written data
TARGFLASH0HMASTLOCK	O	Flash transmits the locked signals
TARGFLASH0HREADYMUX	O	Flash transmission done
TARGFLASH0HAUSER	O	Flash transmits user read/write address
TARGFLASH0HWUSER [3:0]	O	Flash transmits the user's written data
TARGFLASH0HRDATA [31:0]	I	Flash transmits the readout data
TARGFLASH0HRUSER [2:0]	I	Flash transmits the user readout data
TARGFLASH0HRESP	I	Flash transmits the slave response
TARGFLASH0EXRESP	I	Flash transmits the exclusive response
TARGFLASH0HREADYOUT	I	The feedback signal of the Flash transmission done
AHB Lite TARGEXP0 extension interface signals		
TARGEXP0HSEL	O	Flash transmits the selected signals
TARGEXP0HADDR [31:0]	O	Flash transmits read/write address
TARGEXP0HTRANS [1:0]	O	Transmission extension types
TARGEXP0HWRITE	O	Read/write enable transmission extension
TARGEXP0HSIZE [2:0]	O	Data width transmission extension
TARGEXP0HBURST [2:0]	O	Burst types transmission extension
TARGEXP0HPROT [3:0]	O	Protection types transmission extension
TARGEXP0MEMATTR [1:0]	O	Memory attributes transmission extension
TARGEXP0EXREQ	O	Exclusive request transmission extension
TARGEXP0HMASTER [3:0]	O	Master selection transmission

Port Name	I/O	Description
		extension
TARGEXP0HWDATA [31:0]	O	Written data transmission extension
TARGEXP0HMASTLOCK	O	Locked signals transmission extension, used for bit band
TARGEXP0HREADYMUX	O	Transmission extension done
TARGEXP0HAUSER	O	User read/write address transmission extension
TARGEXP0HWUSER [3:0]	O	User written data transmission extension
TARGEXP0HRDATA [31:0]	I	Read-out data transmission extension
TARGEXP0HREADYOUT	I	The feedback signal of transmission extension done
TARGEXP0HRESP	I	The slave response transmission extension
TARGEXP0EXRESP	I	The exclusive response transmission extension
TARGEXP0HRUSER [2:0]	I	The user read-out data transmission extension
AHB Lite INTEXP0 initialization extension interface		
INITEXP0HRDATA [31:0]	O	Initialization of read-out data transmission extension
INITEXP0HREADY	O	Initialization of normal indication transmission extension
INITEXP0HRESP	O	Initialization of response transmission extension
INITEXP0EXRESP	O	Initialization of exclusive response transmission extension
INITEXP0HRUSER [2:0]	O	Initialization of the user read-out data transmission extension
INITEXP0HSEL	I	Initialization of the selected signals transmission extension
INITEXP0HADDR [31:0]	I	Initialization of the read/write address transmission extension
INITEXP0HTRANS [1:0]	I	Initialization of transmission extension types
INITEXP0HWRITE	I	Initialization of read/write enable transmission extension
INITEXP0HSIZE [2:0]	I	Initialization of data width transmission extension
INITEXP0HBURST [2:0]	I	Initialization of burst types setting transmission extension
INITEXP0HPROT [3:0]	I	Initialization of protection types transmission extension
INITEXP0MEMATTR [1:0]	I	Initialization of memory attributes transmission extension
INITEXP0EXREQ	I	Initialization of exclusive request

Port Name	I/O	Description
		transmission extension
INITEXP0HMASTER [3:0]	I	Initialization of master selection transmission extension
INITEXP0HWDATA [31:0]	I	Initialization of written data transmission extension
INITEXP0HMASTLOCK	I	Initialization of master locked signals transmission extension
INITEXP0HAUSER	I	Initialization of user read/write address transmission extension
INITEXP0HWUSER	I	Initialization of user's written data transmission extension
APB interface signal		
APBTARGEXP2PSTRB [3:0]	O	APB transmission of write gate
APBTARGEXP2PPROT [2:0]	O	APB transmission of protection types
APBTARGEXP2PSEL	O	APB transmission of slave selection
APBTARGEXP2PENABLE	O	The second clock cycle of APB transmission
APBTARGEXP2PADDR [11:0]	O	APB transmission of write address
APBTARGEXP2PWRITE	O	APB transmission of read/write enable
APBTARGEXP2PWDATA [31:0]	O	APB transmission of the written data
APBTARGEXP2PRDATA [31:0]	I	APB transmission of the readout data
APBTARGEXP2PREADY	I	Pulled down if slave needs extra waiting
APBTARGEXP2PSLVERR	I	SLVERR response
System reset response signal		
MTX_HRESET_N	O	Automatically activated by SYSRESETN, indicating MCU to start from Flash
JTAG debug port signal		
DAPTDO	O	JTAG data output
DAPJTAGNSW	O	Output 1’b1，JTAG mode
DAPNTDOEN	O	Control signals of JTAG data output pins
DAPSWDITMS	I	JTAG status selection
DAPTDI	I	JTAG data input
DAPNTRST	I	JTAG reset signal
DAPSWCLKTCK	I	JTAG clock signal
TRACE interface signal		
TPIUTRACEDATA[3:0]	O	Trace output data
TPIUTRACECLK	O	Trace output Clock
Interrupt request signal		
USER_INT0	I	Flash error interrupt request

Port Name	I/O	Description
USER_INT1	I	Flash interrupt request
Monitor signal of interrupt status		
INTMONITOR	O	Monitor signal of peripherals interrupt

3.9 USB2.0 PHY

3.9.1 Features

GW1NSE series of SecureFPGA products contains USB2.0 PHY, with the features as below:

- 480Mbps data speed, compatible with USB1.1 1.5/12Mbps data speed
- Plug and play
- Hot socket

3.9.2 Interfaces and Ports Signal

The USB2.0 PHY module includes UTMI+digital and UTMI+AFE (Analog Front End), which are mainly used to connect the USB controller and USB PHY.

Table 3-14 USB2.0 PHY Ports Signal

Port Name	I/O	Description
CLK	O	Used for receiving and sending clock signals Data bit width is 8bit : 60MHz Data bit width is 16bit : 30MHz
RESET	I	Reset signal, active-high.
XCVRSEL	I	Transceiver select. This signal selects between the LS, FS, and HS transceivers: 2’b00: HS Transceiver 2’b01: FS Transceiver 2’b10: LS Transceiver 2’b11: Send a LS packet on a FS bus or receive a LS packet.
TERMSEL	I	Termination select. This signal selects between the FS and HS terminations: 0: HS termination enabled 1: FS termination enabled
SUSPENDM	I	Suspend.
LINESTATE[1:0]	O	Line state. These signals reflect the current state of the single ended receivers. 2’b00：SE0 2’b01：’J’ state 2’b10：’K’ state 2’b11：SE1
CLKSEL [1:0]	I	Operational mode. These signals select between various operational modes: 2’b00: Normal operation 2’b01：Non-driving

Port Name	I/O	Description
		2'b10：Disable bit stuffing and NRZI encoding 2'b11：Normal operation without automatic generation of start and end signals
DP	IO	USB data pin
DM	IO	USB data pin
DATAIN[7:0]	I	Lower 8 bits USB sends data input
DATAIN[15:8]	I	Higher 8 bits USB sends data input
TXVLD	I	Lower 8 bits sends data enable signal, DATAIN[7:0] data valid indication
TXVLDH	I	Higher 8 bits sends data enable signal, DATAIN[15:8] data valid indication
TXREADY	O	Transmit data ready.
DATAOUT[7:0]	O	Lower 8 bits USB receives data output
DATAOUT[15:8]	O	Higher 8 bits USB receives data output
RXVLD	O	Lower 8 bits receives data enable signal, DATAIN[7:0] data valid indication
RXVLDH	O	Higher 8 bits receives data enable signal, DATAIN[15:8] data valid indication
RXACTIVE	O	Receive active. Indicates that the receive state machine has detected SYNC and is active.
RXERROR	O	Receive Error. High-level indicates that a receive error has been detected.
IDPULLUP	I	Signal that enables the sampling of the analog Id line, active-high.
IDDIG	O	Indicates whether the connected plug is a mini-A or mini-B. 0：mini-A 1：mini-B
SESSVLD	O	Indicates if the session for an A/B-peripheral is valid. 0：Vbus < 0.8V 1：Vbus > 2V
VBUSVLD	O	Indicates if the voltage on Vbus is at a valid level for operation (4.4V < Vth < 4.75V). 0：Vbus < 4.4V 1：Vbus > 4.75V
ADPSNS	O	Indicates the voltage on Vbus. 0：Vbus < 0.2 V 1：Vbus > 0.55V
ADP_PRBEN	I	Enables/disables the ADP Probe comparator. 1：enable 0：disable
ADPPRB	O	Indicates the voltage on Vbus. 0：Vbus < 0.6V 1：Vbus > 0.75V

Port Name	I/O	Description
CHARGVBUS	I	This signal enables charging Vbus. 0：do not charge Vbus through a resistor 1：charge Vbus through a resistor
DISCHARGEVBUS	I	This signal enables charging Vbus. 0: do not discharge Vbus through a resistor 1: discharge Vbus through a resistor
DPPD	I	This signal enables the 15k Ohm pull-down resistor on the DP line. 0: Pull-down resistor not connected to DP 1: Pull-down resistor connected to DP
DMPD	I	This signal enables the 15k Ohm pull-down resistor on the DM line. 0: Pull-down resistor not connected to DM 1: Pull-down resistor connected to DM
HOSTDIS	O	This signal is used for all types of peripherals connected to it. It is only valid when DPPD and DMPD are 1. 0: there is peripherals connected 1: there is no peripheral connected
TXBITSTUFFEN	I	Indicates if the data on the DataOut[7:0] lines needs to be bitstuffed or not. 0: Bitstuffing is disabled 1: Bitstuffing is enabled
TXBITSTUFFENH	I	Indicates if the data on the DataOut[15:8] lines needs to be bitstuffed or not. 0: Bitstuffing is disabled 1: Bitstuffing is enabled
FSLSSERIAL	I	0: FS and LS packets are sent using the parallel interface. 1: FS and LS packets are sent using the serial interface.
TXENN	I	Active low enable signal. Only used when FSLSSERIAL is set to 1b.
TXDAT	I	Serial data. Only used when FSLSSERIAL is set to 1.
TXSE0	I	Force single-ended zero. Only used when FSLSSERIAL is set to 1.
RXDP	O	Single-ended receive data. This signal is only valid when FSLSSERIAL is set to 1.
RXDM	O	Single-ended receive data. This signal is only valid when FSLSSERIAL is set to 1.
RXRCV	O	Single-ended receive data. This signal is only valid when FSLSSERIAL is set to 1.
VBUS	IO	VBUS signal
ID	I	ID signal
XIN	I	Crystal in signals, supported range is 12MHZ~24MHZ.
XOUT	O	Crystal out signals

Port Name	I/O	Description
REXT	I	1% precision 12.7K pull-down register
LBKERR	O	0: no BIST error 1: Error during BIST occurs
INTCLK	I	Clock signals provided internally of the SoC.
CLKRDY	O	Observation/debug signal to show that the internal PLL has locked and is ready.
CLK480PAD	O	480 MHZ clock output for observation
Scan signals		
SCANCLK	I	Clock signals for scan mode
SCANEN	I	Select to shift mode
SCANMODE	I	High effective signal to enter scan mode
TRESETN	I	Low effective reset signal for scan mode.
SCANIN1	I	Scan chain input
SCANIN2	I	Scan chain input
SCANIN3	I	Scan chain input
SCANIN4	I	Scan chain input
SCANIN5	I	Scan chain input
SCANIN6	I	Scan chain input
SCANOUT1	O	Scan chain output
SCANOUT2	O	Scan chain output
SCANOUT3	O	Scan chain output
SCANOUT4	O	Scan chain output
SCANOUT5	O	Scan chain output
SCANOUT6	O	Scan chain output

Table 3-15 USB2.0 PHY Parameters

Name	Description
DATABUS16_8	Selects between 8 bits and 16 bits data transfers. 1: 16 bits data path operation enabled. CLK is 30MHz. 0: 8 bits data path operation enabled. CLK is 60MHz.
ADP_PRBEN	Enables/disables the ADP probe comparator.
TEST_MODE[0]	Enables/disables BIST test
TEST_MODE[4] TEST_MODE[1]	BIST modes selection 2'b00：high speed BIST mode 2'b01：full speed BIST mode 2'b10：low speed BIST mode 2'b11：Low speed packet on FSBUS BIST
TEST_MODE[2]	0: 8 bits interface BIST 1: 16 bits interface BIST
TEST_MODE[3]	0: digital loop back BIST 1: analog loop back BIST
HSDRV1	High speed drive adjustment. Please connect to 0 for normal operation.
HSDRV0	High speed drive adjustment. Please connect to 0 for normal operation.
CLK_SEL	Source select for clock 0: external crystal oscillator XIN/XOUT 1：SoC internal clock INTCLK
M[3：0]	Used for test, M division factor, default value 0 0：1 frequency division 1：disabled 2：2 frequency division 3：3 frequency division ..... 15：15 frequency division
N[5：0]	Used for test, N division factor, default value 0 Supports 2 - 63 0 and 1: disabled 2：2 frequency division 3：3 frequency division ..... 63：63 frequency division
C[1：0]	Used for test, charge pump current control signal, default 40uA 2'b00：30uA 2'b01：40uA 2'b10：50uA 2'b11：60uA
FOC_LOCK	Used for test, default 0 0: LOCK is generated by PLL lock detector 1: LOCK is always high(always lock)

3.10 ADC

3.10.1 Features

GW1NSE series of SecureFPGA products integrate an eight-channel single-ended 12 bits SAR ADC. It is a medium-speed ADC with low-power, low-leakage current, and high-speed.

The dynamic performance is as below:

- Slew Rate: Max. 1MHz
- Dynamic range: >81 dB SFDR，>62 db SINAD
- Linear performance: INL<1 LSB, DNL<0.5 LSB, no missing codes

3.10.2 Port Signal

Table 3-16 ADC Port Signal

Port Name	I/O	Description
CLK	I	Clock input signal. fclk is greater than or equal to 16 times of sampling frequency Max. Clock frequency: 16MHz
PD	I	Power down signal, output 0 when the signal value is 1.
SoC	I	Sampling frequency, max. Frequency is 1MHz.
S[2：0]	I	Channel selection signal
CH[7:0]	I	Eight-channel analog input
EOC	O	End conversion.
B[11：0]	O	A/D conversion result

Table 3-17 Channel Selection Truth Table

S[2：0]	Selected Input Channel
3’b111	CH[7]
3’b110	CH[6]
3’b101	CH[5]
3’b100	CH[4]
3’b011	CH[3]
3’b010	CH[2]
3’b001	CH[1]
3’b000	CH[0]

3.11 Clock

The clock resources and wiring are critical for high-performance applications in FPGA. The GW1NSE series of SecureFPGA products provide the global clock network (GCLK), which connects to all the registers directly. Besides the global clock network, the GW1NSE series of SecureFPGA products provide high-speed clock HCLK. PLL, etc are also provided.

For further detailed information, please refer to UG286, Gowin Clock User Guide.

3.11.1 Global Clock

The GCLK is distributed in the GW1NSE series of SecureFPGA products as two quadrants: L and R. Each quadrant provides eight GCLKs. The optional clock resources of GCLK can be pins or CRU. Users can employ dedicated pins as clock resources to achieve better timing.

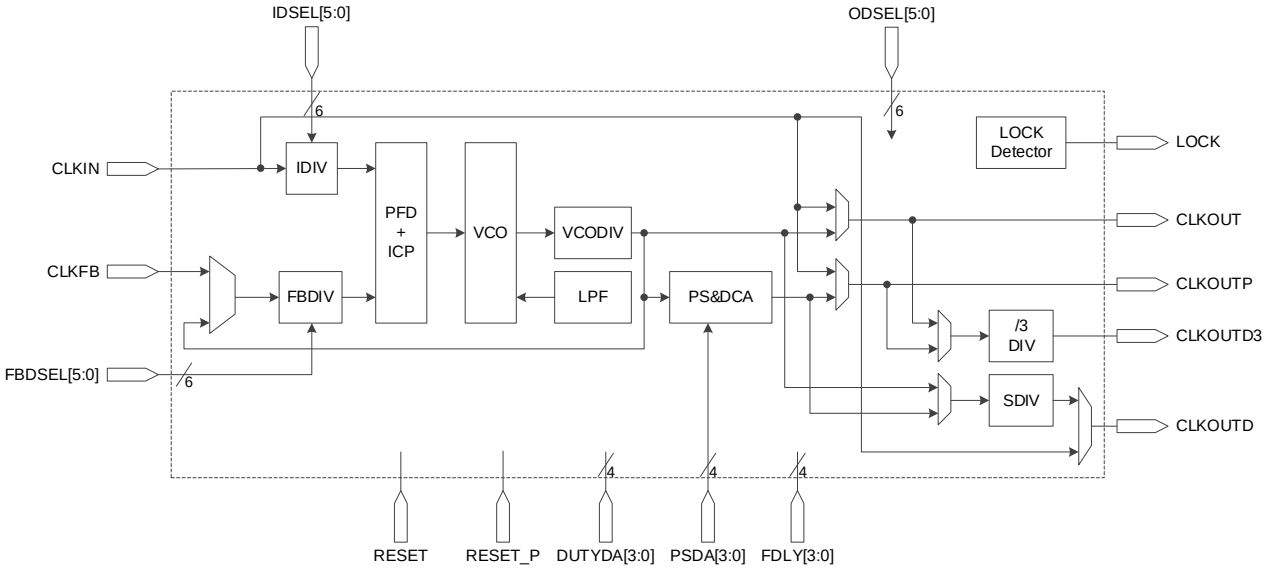
3.11.2 PLL

Phase-locked Loop (PLL) is one kind of a feedback control circuit. The frequency and phase of the internal oscillator signal is controlled by the external input reference clock.

PLL blocks provide the ability to synthesize clock frequencies. Frequency adjustment (multiply and division), phase adjustment, and duty cycle can be adjusted by configuring the parameters.

See Figure 3-36 for the PLL structure.

Figure 3-36 PLL Structure



See Table 3-18 for a definition of the PLL ports.

Table 3-18 Definition of the PLL Ports

Port Name	Signal	Description
CLKIN [5:0]	I	Reference clock input
CLKFB	I	Feedback clock input
RESET	I	PLL reset
RESET_P	I	PLL Power Down
IDSEL [5:0]	I	Dynamic IDIV control: 1~64
FBDSEL [5:0]	I	Dynamic FBDIV control:1~64
PSDA [3:0]	I	Dynamic phase control (rising edge effective)
DUTYDA [3:0]	I	Dynamic duty cycle control (falling edge effective)
FDLY[3:0]	I	CLKOUTP dynamic delay control
CLKOUT	O	Clock output with no phase and duty cycle adjustment
CLKOUTP	O	Clock output with phase and duty cycle adjustment
CLKOUTD	O	Clock divider from CLKOUT and CLKOUTP (controlled by SDIV)
CLKOUTD3	O	clock divider from CLKOUT and CLKOUTP (controlled by DIV3 with the constant division value 3)
LOCK	O	PLL lock status: 1: locked, 0: unlocked

The PLL reference clock source can come from an external PLL pin or from internal routing GCLK, HCLK, or general data signal. PLL feedback signal can come from the external PLL feedback input or from internal routing GCLK, HCLK, or general data signal.

For the PLL features please refer to Table 4-20 PLL Parameters.

PLL can adjust the frequency of the input clock CLKIN (multiply and division). The formulas for doing so are as follows:

- $f_{CLKOUT} = (f_{CLKIN} * FBDIV)/IDIV$
- $f_{VCO} = f_{CLKOUT} * ODIV$
- $f_{CLKOUTD} = f_{CLKOUT}/SDIV$
- $f_{PFD} = f_{CLKIN}/IDIV = f_{CLKOUT}/FBDIV$

Note!

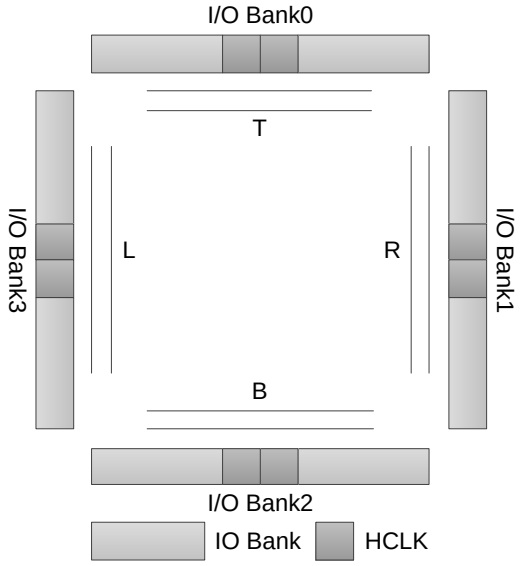
- f_{CLKIN}: The frequency of the input clock CLKIN
- f_{CLKOUT}: The clock frequency of CLKOUT and CLKOUTP
- $f_{CLKOUTD}$: The clock frequency of CLKOUTD, and CLKOUTD is the clock CLKOUT after division
- f_{PFD}: PFD Phase Comparison Frequency, and the minimum value of f_{PFD} should be no less than 3MHz

Adjust IDIV, FBDIV, ODIV, and SDIV to achieve the required clock frequency.

3.11.3 HCLK

HCLK is the high-speed clock in the GW1NSE series of SecureFPGA products. It can support high-performance data transfer and is mainly suitable for source synchronous data transfer protocols. See Figure Figure 3-37.

Figure 3-37 GW1NSE-2C HCLK Distribution



3.12 Long Wire (LW)

As a supplement to CRU, the GW1NSE series of SecureFPGA products provide another routing resource, Long Wire, which can be used as clock, clock enable, set/reset, or other high fan out signals.

3.13 Global Set/Reset (GSR)

A global set/rest (GSR) network is built into the GW1NSE series of SecureFPGA products. There is a direct connection to core logic. It can be used as asynchronous/synchronous set or asynchronous/synchronous reset. The registers in CFU and I/O can be individually configured to use GSR.

3.14 Programming Configuration

The GW1NSE series of SecureFPGA products support SRAM and Flash. The Flash programming mode supports on-chip Flash and off-chip Flash. GW1NSE-2C supports DUAL BOOT, providing a selection for users to backup data to off-chip Flash according to requirements.

Besides JTAG, the GW1NSE series of SecureFPGA products also supports GOWINSEMI's own configuration mode: GowinCONFIG (AUTO BOOT, SSPI, MSPI, DUAL BOOT, SERIAL, and CPU). All the devices support JTAG and AUTO BOOT. For more detailed information, please refer to *UG290*, *Gowin FPGA Products Programming and Configuration User Guide*.

3.14.1 SRAM Configuration

When you adopt SRAM to configure the device, every time the device is powered on, the bit stream file needs to be downloaded to configure the deviece.

3.14.2 Flash Configuration

The Flash configuration data is stored in the on-chip flash. Each time the device is powered on, the configuration data is transferred from the Flash to the SRAM, which controls the working of the device. This mode can complete configuration within a few ms, and is referred to as “Quick Start”. The GW1NSE series of SecureFPGA products also support off-chip Flash configuration and dual-boot. Please refer to UG290, *Gowin FPGA Products Programming and Configuration User Guide* for more detailed information.

3.15 On Chip Oscillator

There is an internal oscillator in each of the GW1NSE series of SecureFPGA products. This provides a programmable user clock that offers clock precision of ±5%. During the configuration process, it can provide a clock for the MSPI mode. See Table 3-19 for GW1NSE series of SecureFPGA products output frequency.

Table 3-19 Oscillator Output Frequency Options

Mode	Frequency	Mode	Frequency	Mode	Frequency
0	2.5MHz[1]	8	7.5MHz	16	15.0MHz
1	5.4MHz	9	8.0MHz	17	17.1MHz
2	5.7MHz	10	8.6MHz	18	20.0MHz
3	6.0MHz	11	9.2MHz	19	24.0MHz
4	6.3MHz	12	10.0MHz	20	30.0MHz
5	6.6MHz	13	10.9MHz	21	40.0MHz
6	6.9MHz	14	12.0MHz	22	60.0MHz
7	7.4MHz	15	13.3MHz	23	120MHz[2]

Note!

- [1] Default frequency
- [2] 125MHz is not suitable for MSPI.

The on-chip oscillator also provides a clock resource for user designs. Up to 64 clock frequencies can be obtained by setting the parameters.

The following formula is employed to get the GW1NSE-2C output clock frequency: fout=240 MHz/Param.

“Param” is the configuration parameter with a range of 2~128. It supports even number only.

4 AC/DC Characteristic

Note!

Please ensure that you use GOWINSEMI devices within the recommended operating conditions and range. Data beyond the working conditions and range are for reference only. GOWINSEMI does not guarantee that all devices will operate normally beyond the operating conditions and range.

4.1 Operating Conditions

4.1.1 Absolute Max. Ratings

Table 4-1 Absolute Max. Ratings

Name	Description	Min.	Max.
V_{CC}	Core voltage	-0.5V	1.32V
V_{CCO}	I/O Bank Power	-0.5V	3.75V
V_{CCX}	LX Auxiliary voltage	-0.5V	1.98V
	UX Auxiliary voltage	-0.5V	3.75V
Storage Temperature	Storage Temperature	-65℃	+150℃
Junction Temperature	Junction Temperature	-40℃	+125℃

4.1.2 Recommended Operating Conditions

Table 4-2 Recommended Operating Conditions

Name	Description	Min.	Max.
V_{CC}	Core voltage	1.14V	1.26V
V_{CCOx}	LX I/O Bank Power	1.14V	1.89V
	UX I/O Bank Power UX V_{CCX} needs to be greater than or equal to V_{CCOx}	1.14V	3.6V
	LV I/O Bank Power	1.14V	3.6V
V_{CCX}	LX Auxiliary voltage	1.71V	1.89V
	UX Auxiliary voltage	2.375V	3.6V
	LV Auxiliary voltage	1.71V	3.6V
T_{JCOM}	Junction temperature Commercial operation	0 ℃	+85 ℃
T_{JIND}	Junction temperature Industrial operation	-40 ℃	+100 ℃

Note!

For the recommended power requirements of different packages, please refer to *UG872, GW1NSE-2C Pinout.*

4.1.3 Power Supply Ramp Rates

Table 4-3 Power Supply Ramp Rates

Name	Description	Min.	Typ.	Max.
T_{RAMP}	Power supply ramp rates for all power supplies	0.6mV/μs	-	6mV/μs

4.1.4 Hot Socket Specifications

Table 4-4 Hot Socket Specifications

Name	Description	Condition	I/O	Max.
I_{HS}	Input or I/O leakage current	$0<V_{IN}<V_{IH}$(MAX)	I/O	150uA
I_{HS}	Input or I/O leakage current	$0<V_{IN}<V_{IH}$(MAX)	TDI,TDO, TMS,TCK	120uA

4.1.5 POR Specification

Table 4-5 POR Voltage

Name	Description	Min.	Max.
POR voltage	Power on reset voltage of Vcc	TBD	TBD

4.2 ESD

Table 4-6 GW1NSE ESD - HBM

Device	CS36	QN32	QN48	LQ144
GW1NSE-2C	HBM>1,000V	HBM>1,000V	HBM>1,000V	HBM>1,000V
GW1NSE-4C	HBM>1,000V	HBM>1,000V	HBM>1,000V	HBM>1,000V

Table 4-7 GW1NSE ESD - CDM

Device	CS36	QN32	QN48	LQ144
GW1NSE-2C	CDM>500V	CDM>500V	CDM>500V	CDM>500V
GW1NSE-4C	CDM>500V	CDM>500V	CDM>500V	CDM>500V

4.3 DC Electrical Characteristics

4.3.1 DC Electrical Characteristics over Recommended Operating Conditions

Table 4-8 DC Electrical Characteristics over Recommended Operating Conditions

Name	Description	Condition	Min.	Typ.	Max.
I_{IL},I_{IH}	Input or I/O leakage	$V_{CCO}<V_{IN}<V_{IH}$ (MAX)	-	-	210μA
		$0V<V_{IN}<V_{CCO}$	-	-	10μA
I_{PU}	I/O Active Pull-up Current	$0<V_{IN}<0.7V_{CCO}$	-30 μA	-	-150 μA
I_{PD}	I/O Active Pull-down Current	V_{IL} (MAX)$<V_{IN}<V_{CCO}$	30μA	-	150μA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN}=V_{IL}$ (MAX)	30μA	-	-
I_{BHHO}	Bus Hold High Sustaining Current	$V_{IN}=0.7V_{CCO}$	-30 μA	-	-
I_{BHLO}	Bud HoldLow Overdrive Current	$0\le V_{IN}\le V_{CCO}$	-	-	150μA
I_{BHHO}	BusHoldHigh Overdrive Current	$0\le V_{IN}\le V_{CCO}$	-	-	-150 μA
V_{BHT}	Bus hold trip points		V_{IL} (MAX)	-	V_{IH} (MIN)
C1	I/O Capacitance			5pF	8pF
V_{HYST}	Hysteresis for Schmitt Trigge inputs	V_{CCO}=3.3V, Hysteresis= Large	-	482mV	-
		V_{CCO}=2.5V, Hysteresis= Large	-	302mV	-
		V_{CCO}=1.8V, Hysteresis= Large	-	152mV	-
		V_{CCO}=1.5V, Hysteresis= Large	-	94mV	-
		V_{CCO}=3.3V, Hysteresis= Small	-	240mV	-
		V_{CCO}=2.5V, Hysteresis= Small	-	150mV	-
		V_{CCO}=1.8V, Hysteresis= Small	-	75mV	-
		V_{CCO}=1.5V, Hysteresis= Small	-	47mV	-

4.3.2 Static Supply Current

Table 4-9 Static Supply Current

Name	Description	LV/UV	Device	Min.	Typ.	Max.
I_{CC}	Core current V_{CC}=1.2V	UX	GW1NSE-2C	TBD	TBD	TBD
I_{CCX}	V_{CCX} current （V_{CCX}=3.3V)	UX	GW1NSE-2C	TBD	TBD	TBD
	V_{CCX} current （V_{CCX}=2.5V)	UX	GW1NSE-2C	TBD	TBD	TBD
I_{CCO}	I/O Bank current (V_{CCO}=2.5V)	UX	GW1NSE-2C	TBD	TBD	TBD
I_{CC}	Core current under load （V_{CCX}=1.2V）	UX	GW1NSE-2C	TBD	TBD	TBD
I_{CCX}	Core current under load （VCCX=3.3V）	UX	GW1NSE-2C	TBD	TBD	TBD
I_{CCO}	I/O Bank current under load(VCCO=2.5V)	UX	GW1NSE-2C	TBD	TBD	TBD

4.3.3 Recommended I/O Operating Conditions

Table 4-10 Recommended I/O Operating Conditions

Name	Output V_{CCO} (V)			Input V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVTTL33	3.135	3.3	3.6	-	-	-
LVCMOS33	3.135	3.3	3.6	-	-	-
LVCMOS25	2.375	2.5	2.625	-	-	-
LVCMOS18	1.71	1.8	1.89	-	-	-
LVCMOS15	1.425	1.5	1.575	-	-	-
LVCMOS12	1.14	1.2	1.26	-	-	-
SSTL15	1.425	1.5	1.575	0.68	0.75	0.9
SSTL18_I	1.71	1.8	1.89	0.833	0.9	0.969
SSTL18_II	1.71	1.8	1.89	0.833	0.9	0.969
SSTL25_I	2.375	2.5	2.645	1.15	1.25	1.35
SSTL25_II	2.375	2.5	2.645	1.15	1.25	1.35
SSTL33_I	3.135	3.3	3.6	1.3	1.5	1.7
SSTL33_II	3.135	3.3	3.6	1.3	1.5	1.7
HSTL18_I	1.71	1.8	1.89	0.816	0.9	1.08
HSTL18_II	1.71	1.8	1.89	0.816	0.9	1.08
HSTL15	1.425	1.5	1.575	0.68	0.75	0.9
PCI33	3.135	3.3	3.6	-	-	-
LVPECL33E	3.135	3.3	3.6	-	-	-
MLVDS25E	2.375	2.5	2.625	-	-	-
BLVDS25E	2.375	2.5	2.625	-	-	-
RSDS25E	2.375	2.5	2.625	-	-	-
LVDS25E	2.375	2.5	2.625	-	-	-
SSTL15D	1.425	1.5	1.575	-	-	-
SSTL18D_I	1.71	1.8	1.89	-	-	-
SSTL18D_II	1.71	1.8	1.89	-	-	-
SSTL25D_I	2.375	2.5	2.625	-	-	-
SSTL25D_II	2.375	2.5	2.625	-	-	-
SSTL33D_I	3.135	3.3	3.6	-	-	-
SSTL33D_II	3.135	3.3	3.6	-	-	-
HSTL15D	1.425	1.575	1.89	-	-	-
HSTL18D_I	1.71	1.8	1.89	-	-	-
HSTL18D_II	1.71	1.8	1.89	-	-	-

4.3.4 Single - Ended DC Electrical Characteristic

Table 4-11 IOB Single - Ended DC Electrical Characteristic

Name	V_{IL}		V_{IH}		V_{OL} (Max)	V_{OH} (Min)	I_{OL} (mA)	I_{OH} (mA)
	Min	Max	Min	Max				
LVCMOS33 LVTTL33	-0.3V	0.8V	2.0V	3.6V	0.4V	V_{CCO}-0.4V	4	-4
							8	-8
							12	-12
							16	-16
							24	-24
					0.2V	V_{CCO}-0.2V	0.1	-0.1
LVCMOS25	-0.3V	0.7V	1.7V	3.6V	0.4V	V_{CCO}-0.4V	4	-4
							8	-8
							12	-12
							16	-16
					0.2V	V_{CCO}-0.2V	0.1	-0.1
LVCMOS18	-0.3V	0.35 x V_{CCO}	0.65 x V_{CCO}	3.6V	0.4V	V_{CCO}0.4V	4	-4
							8	-8
							12	-12
					0.2V	V_{CCO}-0.2V	0.1	-0.1
LVCMOS15	-0.3V	0.35 x V_{CCO}	0.65 x V_{CCO}	3.6V	0.4V	V_{CCO}-0.4V	4	-4
							8	-8
					0.2V	V_{CCO}-0.2V	0.1	-0.1
LVCMOS12	-0.3V	0.35 x V_{CCO}	0.65 x V_{CCO}	3.6V	0.4V	V_{CCO}-0.4V	2	-2
							6	-6
					0.2V	V_{CCO}-0.2V	0.1	-0.1
PCI33	-0.3V	0.3 x V_{CCO}	0.5 x V_{CCO}	3.6V	0.1 x V_{CCO}	0.9 x V_{CCO}	1.5	-0.5
SSTL33_I	-0.3V	V_{REF}-0.2V	V_{REF}+0.2V	3.6V	0.7	V_{CCO}-1.1V	8	-8
SSTL25_I	-0.3V	V_{REF}-0.18V	V_{REF}+0.18V	3.6V	0.54V	V_{CCO}-0.62V	8	-8
SSTL25_II	-0.3V	V_{REF}-0.18V	V_{REF}+0.18V	3.6V	NA	NA	NA	NA
SSTL18_II	-0.3V	V_{REF}-0.125V	V_{REF}+0.125V	3.6V	NA	NA	NA	NA
SSTL18_I	-0.3V	V_{REF}-0.125V	V_{REF}+0.125V	3.6V	0.40V	V_{CCO}-0.40V	8	-8
SSTL15	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	0.40V	V_{CCO}-0.40V	8	-8
HSTL18_I	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	0.40V	V_{CCO}-0.40V	8	-8
HSTL18_II	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	NA	NA	NA	NA
HSTL15_I	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	0.40V	V_{CCO}-0.40V	8	-8
HSTL15_II	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	NA	NA	NA	NA

4.3.5 I/O Differential Electrical Characteristics

Table 4-12 I/O Differential Electrical Characteristics

LVDS25

Name	Description	Condition	Min.	Typ.	Max.	Unit
V_{INA},V_{INB}	Input Voltage (Input Voltage)		0	-	2.4	V
V_{CM}	Input Common Mode Voltage (Input Common Mode Voltage)	Half the Sum of the Two Inputs	0.05	-	2.35	V
V_{THD}	Differential Input Threshold	Difference Between the Two Inputs	± 100	-	±600	mV
I_{IN}	Input Current	Power On or Power Off	-	-	± 10	μA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	R_T = 100Ω	-	-	1.60	V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	R_T = 100Ω	0.9	-	-	V
V_{OD}	Output Voltage Differential	(V_{OP} - V_{OM}), R_T = 100Ω	250	350	450	mV
ΔV_{OD}	Change in V_{OD} Between High and Low		-	-	50	mV
V_{OS}	Output Voltage Offset	(V_{OP} + V_{OM})/2, R_T = 100Ω	1.125	1.20	1.375	V
ΔV_{OS}	Change in V_{OS} Between High and Low		-	-	50	mV
I_S	Short-circuit current	V_{OD} = 0V output short-circuit	-	-	15	mA

4.4 Switching Characteristic

4.4.1 I/O Speed

Table 4-13 I/O Parameters

Name	Description		Min	Max	Unit
f_{MAX}	IO Max. Frequency	GW1NSE-2C	-	150M	Hz
f_{MAX_LVDS}	LVDS Max. Frequency	GW1NSE-2C	-	400M	Hz

4.4.2 CFU Block Internal Timing Parameters

Table 4-14 CFU Block Internal Timing Parameters

Name	Description	Speed Grade		Unit
		Min	Max	
t_{LUT4_CFU}	LUT4 delay	-	0.674	ns
t_{LUT5_CFU}	LUT5 delay	-	1.388	ns
t_{LUT6_CFU}	LUT6 delay	-	2.01	ns
t_{LUT7_CFU}	LUT7 delay	-	2.632	ns
t_{LUT8_CFU}	LUT8 delay	-	3.254	ns
t_{SR_CFU}	Set/Reset to Register output	-	1.86	ns
t_{CO_CFU}	Clock to Register output	-	0.76	ns

4.4.3 Clock and I/O Switching Characteristics

Table 4-15 LUT External Switching Characteristics

Name	Description	Device	-5		-6		Unit
			Min	Max	Min	Max	
Clocks	TBD	TBD	TBD	TBD	TBD	TBD	
Pin-LUT-Pin Delay	TBD	TBD	TBD	TBD	TBD	TBD	
General I/O Pin Parameters	TBD	TBD	TBD	TBD	TBD	TBD	

4.4.4 Gearbox Switching Characteristics

Table 4-16 Gearbox Internal Timing Parameters

Name	Description	Typ.	Unit
FMAXIDDR	2:1 Gearbox maximum input frequency	410	MHz
$FMAX_{IDES4}$	4:1 Gearbox maximum input frequency	410	MHz
$FMAX_{IDES8}$	8:1 Gearbox maximum input frequency	410	MHz
$FMAX_{IVIDEO}$	7:1 Gearbox maximum input frequency	390	MHz
$FMAX_{IDES10}$	10:1 Gearbox maximum input frequency	410	MHz
$FMAX_{ODDR}$	1:2 Gearbox maximum input frequency	355	MHz
$FMAX_{OSER4}$	1:4 Gearbox maximum input frequency	360	MHz
$FMAX_{OSER8}$	1:8 Gearbox maximum input frequency	355	MHz
$FMAX_{OVIDEO}$	1:7 Gearbox maximum input frequency	355	MHz
$FMAX_{OSER10}$	1:10 Gearbox maximum input frequency	355	MHz

4.4.5 BSRAM Switching Characteristics

Table 4-17 BSRAM Internal Timing Parameters

Name	Description	Speed Grade		Unit
		Min	Max	
t_{COAD_BSRAM}	Clock to output from read address/data	-	5.10	ns
t_{COOR_BSRAM}	Clock to output from output register	-	0.56	ns

4.4.6 DSP Switching Characteristics

Table 4-18 DSP Internal Timing Parameters

Name	Description	Speed Grade		Unit
		Min	Max	
t_{COIR_DSP}	Clock to output from output register	-	4.80	ns
t_{COPR_DSP}	Clock to output from output register	-	2.40	ns
t_{COOR_DSP}	Clock to output from output register	-	0.84	ns

4.4.7 On chip Oscillator Output Frequency

Table 4-19 On chip Oscillator Output Frequency

Name	Description		Min.	Typ.	Max.
f_{MAX}	On chip Oscillator Output Frequency (0 ~ +85℃)	GW1NSE-2C	114MHz	120MHz	126MHz
	On chip Oscillator Output Frequency (-40 ~ +100℃)	GW1NSE-2C	108MHz	120MHz	132MHz
t_{DT}	Clock Duty Cycle		43%	50%	57%
t_{OPJIT}	Clock Period Jitter		0.01UIPP	0.012UIPP	0.02UIPP

4.4.8 PLL Parameters

Table 4-20 PLL Parameters

Device	Speed Level	Name	Min.	Max.
GW1NSE-2C	C6/I5	CLKIN	3MHZ	400MHZ
		PFD	3MHZ	400MHZ
		VCO	400MHZ	1200MHZ
		CLKOUT	3.125MHZ	600MHZ
	C5/I4	CLKIN	3MHZ	320MHZ
		PFD	3MHZ	320MHZ
		VCO	320MHZ	960MHZ
		CLKOUT	2.5MHZ	480MHZ
GW1NSE-4C	C6/I5	CLKIN	3MHZ	400MHZ
		PFD	3MHZ	400MHZ
		VCO	400MHZ	1200MHZ
		CLKOUT	3.125MHZ	600MHZ
	C5/I4	CLKIN	3MHZ	320MHZ
		PFD	3MHZ	320MHZ
		VCO	320MHZ	960MHZ
		CLKOUT	2.5MHZ	480MHZ

4.5 Cortex-M3 Electrical Specification

4.5.1 DC Characteristic

Table 4-21 Current Characteristic

Name	Description	Spec.		Unit
		Min.	Max.	
I_{VCC}	Max. current of VCC	-	100	mA
I_{VSS}	Max. current of VSS	-	⩾100	mA
I_{INJ}	Leakage current	-	+/-5	mA

4.5.2 AC Characteristic

Table 4-22 Clock Parameters

Name	Description	Device	Spec.		Unit
			Min.	Max.	
f_{HCLK}	AHB clock frequency	GW1NSE-2C	0	30	MHz
		GW1NSE-4C	0	80	MHz
f_{PCLK}	APB clock frequency	GW1NSE-2C	0	30	MHz
		GW1NSE-4C	0	80	MHz

4.6 User Flash Characteristic

4.6.1 DC Characteristic

Table 4-23 User Flash DC Characteristic

Name	Description	Spec.		Unit
		Min.	Max.	
$IVCC_{read}$	V_{CC} read operation current	-	1.4	mA
$IVCCX_{read}$	V_{CCX} read operation current	-	0.6	mA
$IVCC_{prog}$	V_{CC} write operation current	-	0.2	mA
$IVCCX_{prog}$	V_{CCX} write operation current	-	2.2	mA
$IVCC_{erase}$	V_{CC} erase operation current	-	0.2	mA
$IVCCX_{erase}$	V_{CCX} erase operation current	-	2.3	mA
$I_{IDLE-VCC}$	V_{CC} IDLE current	-	10	uA
$I_{IDLE-VCCX}$	V_{CCX} IDLE current	-	100	uA
I_{LI}	Input leakage current	-	0.1	uA
I_{LO}	Output leakage current	-	0.1	uA
V_{VREF}	Before setting configuration register.	1.14	1.26	V
	After setting configuration register.	1.176	1.224	V
V_{VREF1V}	Before setting configuration register.	0.94	1.06	V
	After setting configuration register.	0.97	1.03	V
V_{IL}	Input low level	-	$0.1*V_{CC}$	V
V_{IH}	Input high level	$0.9*V_{CC}$	-	V
V_{OL}	Output low level	-	$0.1*V_{CC}$	V
V_{OH}	Output high level	$0.9*V_{CC}$	-	V
t_{PROG}	Write operation time	-	30	us
t_{SER}	Page erasure time	-	2	mA
t_{MER}	Macro erasure time	-	10	mA

4.6.2 AC Characteristic

Table 4-24 User Flash Timing Parameters

Name	Description	Spec.		Unit
		Min.	Max.	
tAS	Address set up time	2	-	ns
tHS	Address hold-up time	2	-	ns
tS	Write and erase setup time	5	-	ns
tH	Write and erase hold time	5	-	ns
tDS	Data set up time	5	-	ns
tDH	Data hold-up time	5	-	ns
tAC	Data read time	-	30	ns
tACR		-	80	ns
tHZ	Time from high resistance to OE turning low	3	-	ns
tAE	High-level time of AE	10	-	ns
tAEL	Low-level time of AE	10	-	ns
tAAD	Delay time from AE to AE during read operation	30	-	ns
tAADR	Delay time from AE to AE in readback state	80	-	ns
tTR	Time of TBIT rising edge after NVSTR rising edge	-	100	ns
tTF	Time from NVSTR rising edge to IBIT falling edge during write operation	-	30	us
tTF	Time from NVSTR rising edge to IBIT falling edge during page erasure operation	-	2	ms
tTF	Time from NVSTR rising edge to IBIT falling edge during macro erasure operation	-	10	ms
tNVSTRH	Hold time from NVSTR rising edge to AE rising edge	10	-	ns
tNVSTRL	Hold time from NVSTR rising edge to IBIT falling edge	50	-	ns
tCS	CS setup time	10	-	ns
tRCH	CS hold-up time during read operation	0	-	ns
tWCH	CS hold-up time during write operation	10	-	ns
tECH	CS hold-up time during erasure operation	10	-	ns
tDOH	Time from AE enabled to data output time	5	-	ns
tOS	Read enable setup time	1	-	ns
tOH	Read enable hold-up time	30	-	ns
tOHR	Read enable hold-up time	80	-	ns

-

4.6.3 Operation Timing Diagrams

Figure 4-1 Read Mode

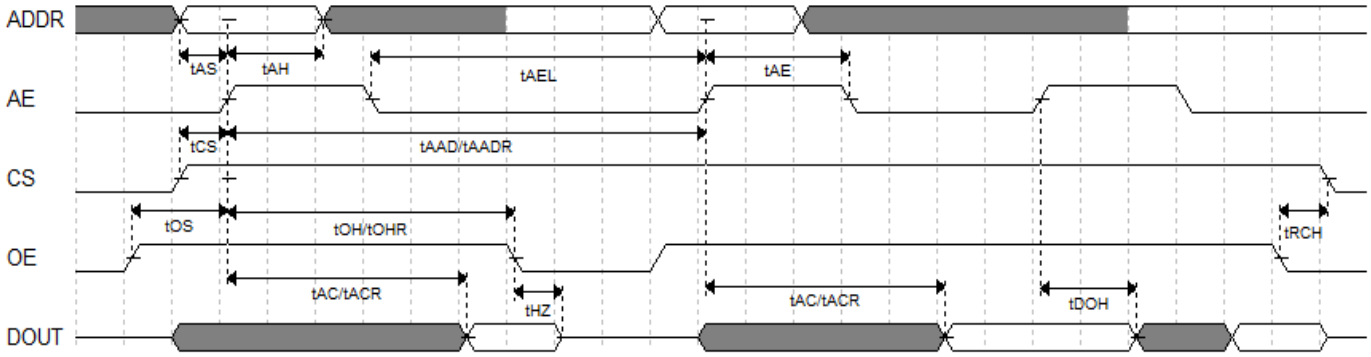


Figure 4-2 Write Mode

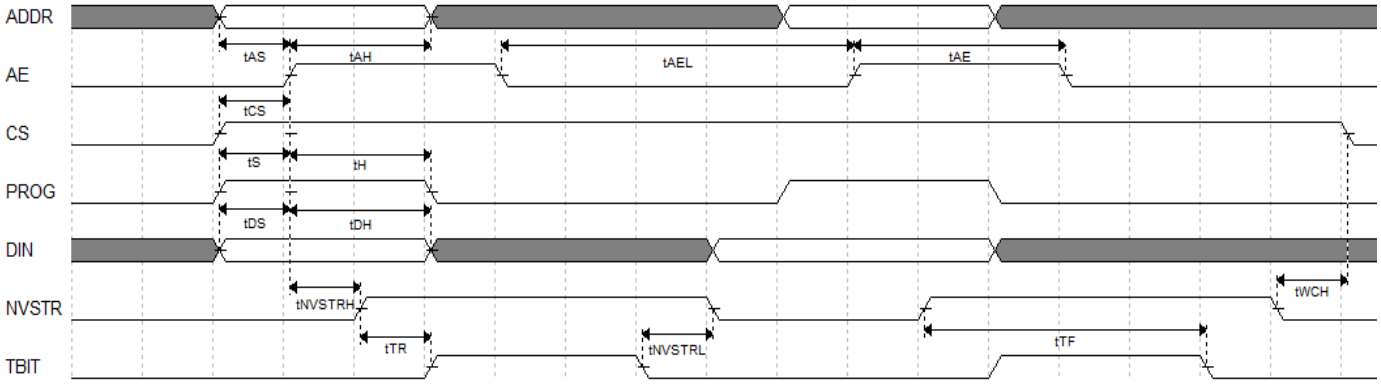


Figure 4-3 Page Erasure Mode

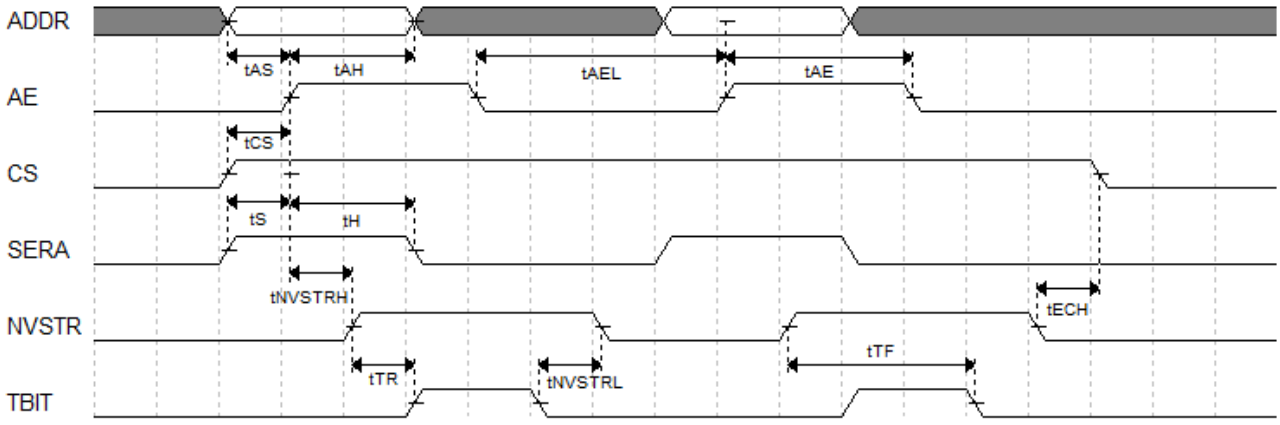
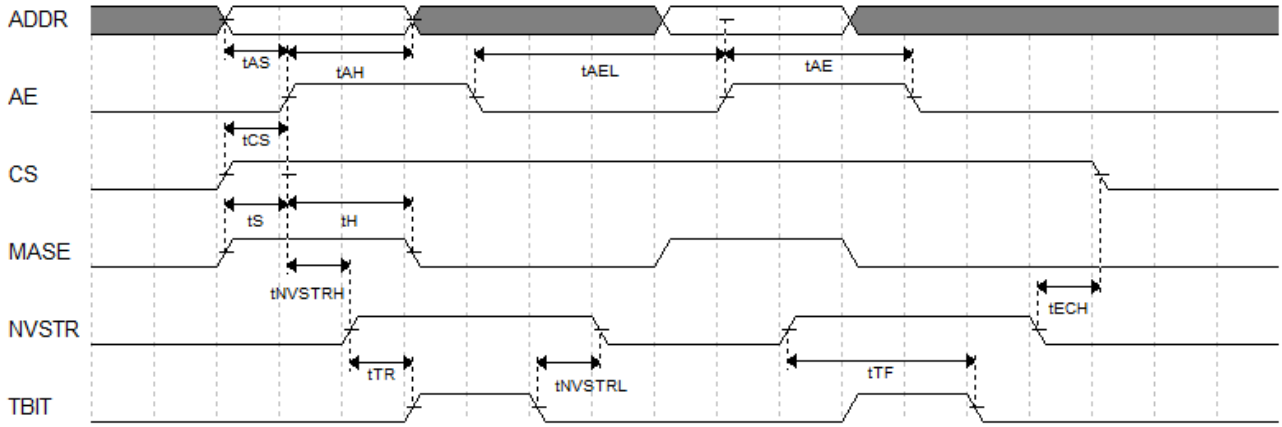


Figure 4-4 Module Rrasure Mode



4.7 ADC Characteristics

4.7.1 ADC Timing

In total, 16 clock cycles are needed for ADC to sample analog input signals and convert them to output digital signals. The first four clock cycles are used to sample and hold; the latter twelve clock cycles are used for the SAR algorithm to generate the required output signals. If the ECO signal becomes high at the 16th clock cycle, the conversion is complete, and the converted digital data will output at the EOC rising edge.

Figure 4-5 ADC Timing

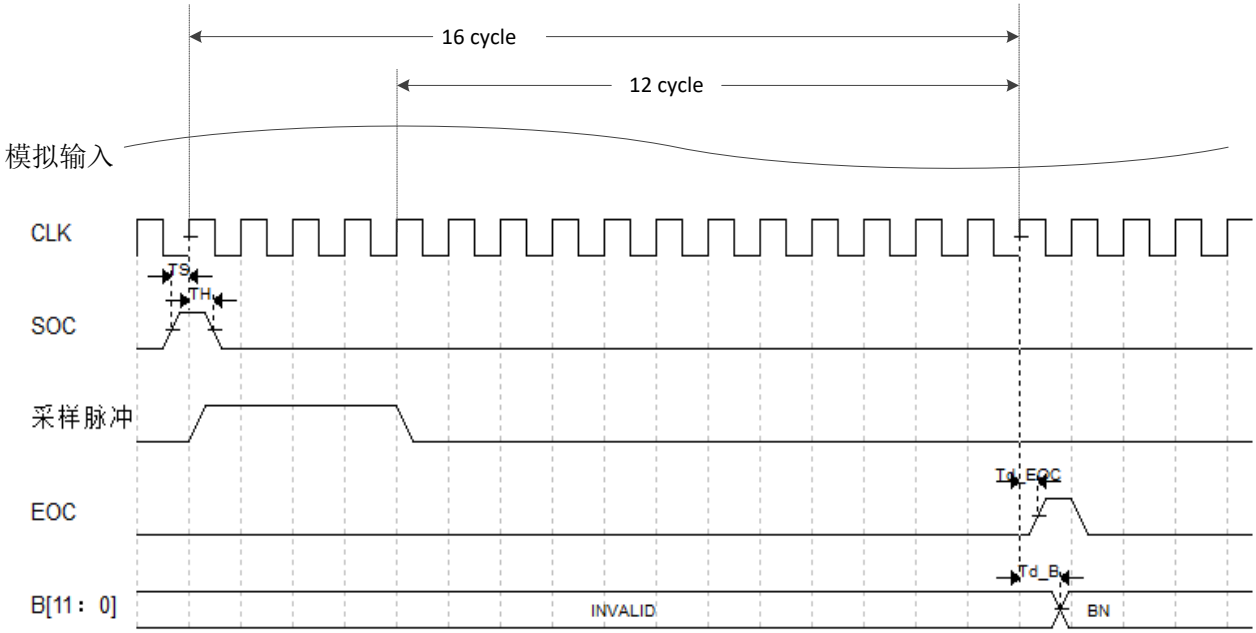


Table 4-25 ADC Timing Parameters

Name	Description	Spec.		Unit
		Min.	Max.	
CLK	Clock cycle	62.5	-	ns
T_S	SoC setup time	0	-	ns
T_H	SoC hold-up time	10	-	ns
T_{D_EOC}	EOC delay time	-	13.5	ns
T_{D_B}	Data-out delay time	-	16	ns

4.7.2 Electrical Characteristic Parameters

Table 4-26 ADC Parameters

Parameter	Description	Spec.			Unit
		Min.	Typ.	Max.	
DC Precision					
O	Data output bits		12		bit
INL	Integral nonlinearity		+/- 0.84		LSB
DNL	Differential nonlinearity		+/- 0.46		LSB
Offset error	Offset error		0.45		%FS
Gain error	Gain error		0.02		%FS
Analog Input					
CH[7:0]	Single-ended input range	0.01*VREF		0.99*VREF	V
CIN	Input capacitance		11.52		pF
Slew Rate					
SoC	Sample frequency			1	MHz
CLK	Main clock			16	MHz
Date-out delay	Date-out delay		12		Clock cycle
Dynamic Characteristic Parameters					
SINAD	Signal Noise Ratio		64.8(Fin=1.47K)		DB
			62.6(Fin=107K)		DB
SFDR	Spurious-free dynamic range		84.9(Fin=1.47K)		DB
			81.7(Fin=107K)		DB
HD2	Second harmonic distortion		-104(Fin=1.47K)		DB
			-87.1(Fin=107K)		DB
HD3	Third harmonic distortion		-94.1(Fin=1.47K)		DB
			-80.6(Fin=107K)		DB
THD	Total harmonic distortion (Fifth)		-87.2(Fin=1.47K)		DB
			-79.3(Fin=107K)		DB
ENOB	Valid data-out bits		10.5(Fin=1.47K)		bit
			10.1(Fin=107K)		bit

Parameter	Description	Spec.			Unit
		Min.	Typ.	Max.	
Reference Voltage					
VREF	Reference Voltage	0.5*V_{CCO0}		V_{CCO0}	V
Digital Input					
V_{IH}	Input high level	0.7*V_{CC}	V_{CC}		V
V_{IL}	Input low level		0	0.3*V_{CC}	V
Digital output B[11:0]					
V_{OH}	Output high level	0.7*V_{CC}			V
V_{OL}	Output low level			0.3*V_{CC}	V
Supply voltage					
V_{CCO0}	Analog/digital voltage	2.97	3.3	3.63	V
V_{CC}	Digital voltage	1.08	1.2	1.32	V
I_{VCCO0}	Analog/digital current		750(Fin=107K)		uA
I_{VCC}	Digital current		4(Fin=107K)		uA
I_{pd}	Turning off current		0.15		mA

4.8 Configuration Interface Timing Specification

The GW1NSE series of SecureFPGA products GowinCONFIG support six configuration modes: AUTO BOOT, SSPI, MSPI, DUAL BOOT, SERIAL, and CPU. For detailed information, please refer to *UG290*, *Gowin FPGA Products Programming and Configuration* User Guide.

5 Ordering Information

5.1 Part Naming

Note!

- For further information about package types and pin number, please refer to 2.2 Product Resources and 2.3 Package Information.
- The LittleBee® family devices and Arora family devices of the same speed level have different speed.
- Both “C” and “I” are used in GOWIN part name marking for one same device. GOWIN devices are screened using industrial standards, so one device can be used for both industrial (I) and commercial (C) applications. The maximum temperature of the industrial grade is 100℃, and the maximum temperature of the commercial grade is 85℃. Therefore, if the chip meets the speed level 6 in commercial grade applications, the speed level is 5 in industrial grade applications.

Figure 5-1 GW1NSE-2C/GW1NSE-4C Part Naming–ES

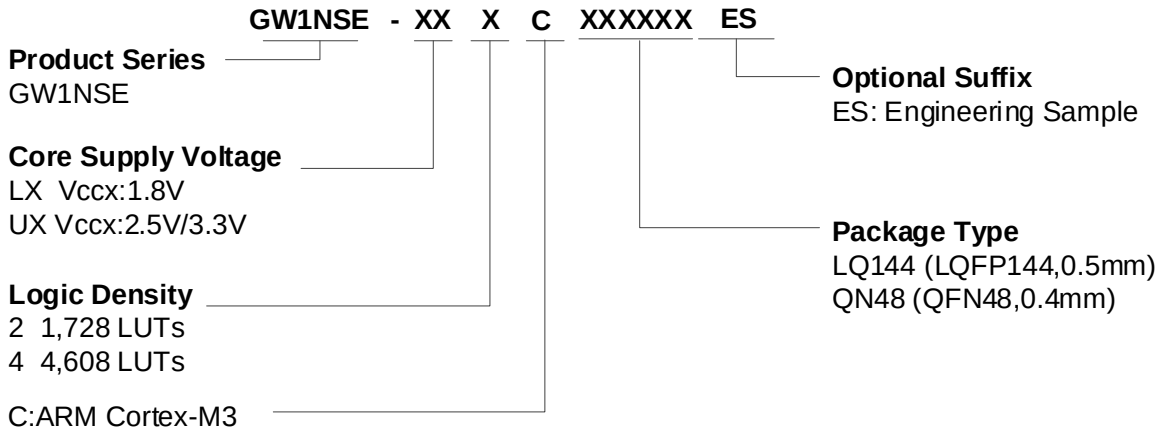
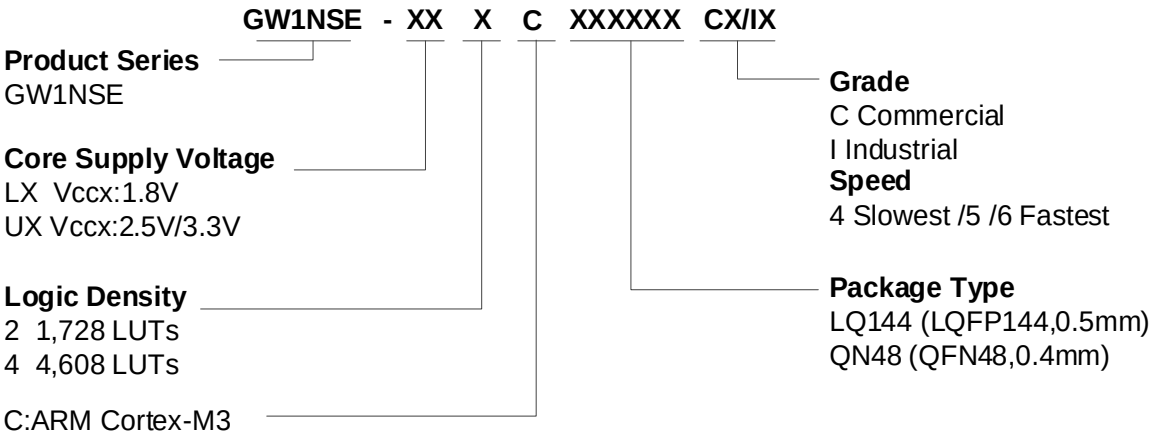


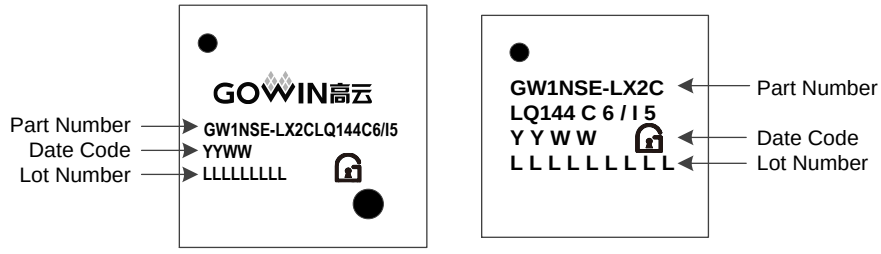
Figure 5-2 GW1NSE-2C/GW1NSE-4C Part Naming–Production



5.2 Package Mark

The device information of GOWINSEMI is marked on the chip surface, as shown in Figure 5-3.

Figure 5-3 GW1NSE-2C/GW1NSE-4C Package Mark



Note!

The first two lines in the right figure above are the "Part Number".


GOWIN
PROGRAMMING FOR THE FUTURE