# GW1NSER Series of SecureFPGA Products

# Datasheet

**DS881-1.1.1E, 05/25/2023**

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## Revision History

| Date | Version | Description |
|---|---|---|
| 11/18/2019 | 1.0E | Initial version published. |
| 08/14/2020 | 1.01E | ● PLL Parameters optimized.<br>● Figures of Part Naming optimized. |
| 11/27/2020 | 1.02E | The Max. operating frequency of ARM Cortex-M3 updated. |
| 11/17/2021 | 1.03E | The description of I/O standards updated. |
| 03/30/2023 | 1.1E | ● Recommended operating conditions updated.<br>● The maximum value of the differential input threshold $V_{THD}$ updated.<br>● Note about DC current limit added.<br>● Figure 3-1 GW1NSER-4C Architecture Overview updated.<br>● Table 3-2 Output I/O Standards and Configuration Options updated.<br>● Table 4-1 Absolute Max. Ratings updated.<br>● Table 4-3 Power Supply Ramp Rates updated.<br>● Table 4-8 DC Electrical Characteristics over Recommended Operating Conditions updated.<br>● Table 4-24 User Flash Timing Parameters updated.<br>● Section 3.7.4 Byte-enable removed.<br>● Description of configuration Flash added..<br>● Information on Slew Rate removed.<br>● Description of true LVDS design modified.<br>● Note about the default state of GPIO modified.<br>● Table 4-14 CLU Block Internal Timing Parameters updated.<br>● The I/O logic output diagram and the I/O logic input diagram combined into Figure 3-7 I/O Logic Input and Output. |
| 05/25/2023 | 1.1.1E | ● 3.7.2 Memory Configuration Mode updated.<br>● Information on User Flash of GW1NSER-4C removed. |

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# 1 About This Guide

## 1.1 Purpose

This data sheet describes the features, product resources and structure, AC/DC characteristics, timing specifications of the configuration interface, and the ordering information of the GW1NSER series of SecureFPGA product. It is designed to help you understand the GW1NSER series of SecureFPGA products quickly and select and use devices appropriately.

## 1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- DS881, GW1NSER series of SecureFPGA products Data Sheet
- UG290, Gowin FPGA Products Programming and Configuration User Guide
- UG884, GW1NSER series of SecureFPGA products Package and Pinout
- UG883, GW1NSER-4C Pinout

# 1.3 Abbreviations and Terminology

The abbreviations and terminology used in this manual are as shown in Table 1-1 below.

**Table 1-1 Abbreviations and Terminology**

| Abbreviations and Terminology | Full Name |
|---|---|
| ADC | Analog to Digital Converter |
| AHB | Advanced High performance Bus |
| ALU | Arithmetic Logic Unit |
| APB | Advanced Peripheral Bus |
| ARM | Advanced RISC Machine |
| BSRAM | Block Static Random Access Memory |
| CFU | Configurable Function Unit |
| CLS | Configurable Logic Section |
| CRU | Configurable Routing Unit |
| DAP | Debug Access Port |
| DCS | Dynamic Clock Selector |
| DNL | Differential Nonlinearity |
| DP | True Dual Port 16K BSRAM |
| DQCE | Dynamic Quadrant Clock Enable |
| DWT | Data Watchpoint Trace |
| FPGA | Field Programmable Gate Array |
| GPIO | Gowin Programmable IO |
| INL | Integral Nonlinearity |
| IOB | Input/Output Block |
| ITM | Instrumentation Trace Module |
| LSB | Least Significant Bit |
| LUT4 | 4-input Look-up Table |
| LUT5 | 5-input Look-up Table |
| LUT6 | 6-input Look-up Table |
| LUT7 | 7-input Look-up Table |
| LUT8 | 8-input Look-up Table |
| MG | MBGA |
| NVIC | Nested Vector Interrupt Controller |
| PHY | Physical Layer |
| PLL | Phase-locked Loop |
| QN | QFN |
| REG | Register |
| SAR | Successive Approximation Register |
| SDP | Semi Dual Port 16K BSRAM |

| Abbreviations and Terminology | Full Name |
|---|---|
| SFDR | Spurious-free Dynamic Range |
| SINAD | Signal to Noise And Distortion |
| SoC | System on Chip |
| SP | Single Port 16K BSRAM |
| SSRAM | Shadow Static Random Access Memory |
| TDM | Time Division Multiplexing |
| Timer | Timer |
| TimeStamp | TimeStamp |
| TUIP | Trace Port Interface Unit |
| UART | Universal Asynchronous Receiver/Transmitter |
| USB | Universal Serial Bus |
| Watchdog | Watchdog |

# 1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

# 2General Description

GW1NSER series of SecureFPGA products provide a Root of Trust based on SRAM PUF technology. Each device is factory provisioned with a unique key pair that is never exposed outside of the device or to the internal development space. The Intrinsic ID BroadKey-Pro security library is provided with GOWIN SecureFPGA devices allowing easy integration of common security features into user applications. The GOWIN SecureFPGA feature set is widely applicable and can used for a variety of consumer and industrial IoT, edge, and server management applications.

GW1NSER series of SecureFPGA products onsist of the same hardware architecture as that of GW1NSR devices. The difference is that GW1NSER devices have an OTP (One-Time-Programmable) Authentication Code pre-stored in its internal Non-volatile Flash memory. The devices with this OTP Authentication Code can be used for the applications of encryption, decryption, key/public key generation, and secure communication, etc.

GOWINSEMI provides a new generation of FPGA hardware development environment through market-oriented independent research and development that supports the GW1NSER series of SecureFPGA products and applies to FPGA synthesizing, layout, place and routing, data bitstream generation and download, etc.

## 2.1 Features

- Lower power consumption
  - 55nm embedded flash technology
  - Core voltage: 1.2V
  - Supports LV
  - Clock dynamically turns on and off
- Integrated with HyperRAM
- Integrated with NOR FLASH
- Hard core processor
  - Cortex-M3 32-bit RISC

- ARM3v7M architecture optimized for small-footprint embedded applications
- System timer (SysTick), providing a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism
- Thumb compatible Thumb-2-only instruction set processor core for high code density
- Supports up to 80 MHz operation
- Hardware-division and single-cycle-multiplication
- Integrated nested vectored interrupt controller (NVIC) providing deterministic interrupt handling
- 26 interrupts with eight priority levels
- Memory protection unit (MPU), providing a privileged mode for protecting operation system functionality
- Unaligned data access, enabling data to be efficiently packed into memory
- Atomic bit manipulation (bit-banding), delivering maximum memory utilization and streamlined peripheral control
- Timer0 and Timer1
- UART0 and UART1
- Watchdog
- Debug port: JTAG and TPIU

- Offers OTP Authentication Code
- Configuration Flash
  - NOR Flash
  - 10,000 write cycles
  - Greater than10 years Data Retention at +85 ℃
- Multiple I/O Standards
  - LVCMOS33/25/18/15/12; LVTTL33, SSTL33/25/18 I, SSTL33/25/18 II, SSTL15; HSTL18 I, HSTL18 II, HSTL15 I; PCI, LVDS25, RSDS, LVDS25E, BLVDSE
  - MLVDSE, LVPECLE, RSDSE
  - Input hysteresis option
  - Supports 4mA,8mA,16mA,24mA,etc. drive options
  - Individual Bus Keeper, Weak Pull-up, Weak Pull-down, and Open Drain option
  - Hot Socket
- MIPI IO - MIPI D-PHY RX/TX

  - BANK0 / BANK1 of GW1NSER-4C supports MIPI I/O input, and MIPI transmission speed can be up to 1.2Gbps
  - BANK2 of GW1NSER-4C supports MIPI I/O output, and MIPI transmission speed can be up to 1.2Gbps
  - Supports I3C
- Abundant Slices
  - Four input LUT (LUT4)
  - Supports shifter register
- Block SRAM with multiple modes
  - Supports Dual Port, Single Port, and Semi Dual Port
  - Supports bytes write enable
- Flexible PLLs
  - Frequency adjustment (multiply and division) and phase adjustment
  - Supports global clock
- Built-in Flash programming
  - Instant-on
  - Supports security bit operation
  - Supports AUTO BOOT and DUAL BOOT
- Configuration
  - JTAG configuration
  - Supports on-chip DUAL BOOT configuration mode
  - Multiple GowinCONFIG configuration modes: AUTOBOOT, SSPI, MSPI, CPU, SERIAL

# 2.2 Product Resources

**Table 2-1 Product Resources**

| Device | GW1NSER-4C |
|---|---|
| LUT4 | 4,608 |
| Flip-Flop (FF) | 3,456 |
| Block SRAM<br>BSRAM (bits) | 180K |
| BSRAM quantity<br>BSRAM | 10 |
| 18 x 18 Multiplier | 16 |
| HyperRAM(bits) | 64M |
| NOR FLASH(bits) | 32M |
| PLLs | 2 |
| OSC | 1,±5% accuracy |
| Hard core processor | Cortex-M3 |
| Total number of I/O banks | 4 |
| Max. I/O | 106 |
| Core voltage | 1.2V |

# 2.3 Package Information

**Table 2-3 Memory Information**

| Device | Package | Memory | Capacity | Bit Width |
|---|---|---|---|---|
| GW1NSER-4C | QN48P | HyperRAM | 64Mb | 8 bits |
| | QN48G | NOR Flash | 32Mb | 1 bit |

**Table 2-2 Package Information, Max. User I/O, and LVDS Pairs**

| Package | Pitch(mm) | Size(mm) | GW1NSER-4C |
|---|---|---|---|
| QN48P | 0.4 | 6 x 6 | 38(4) |
| QN48G | 0.4 | 6 x 6 | 38(4) |

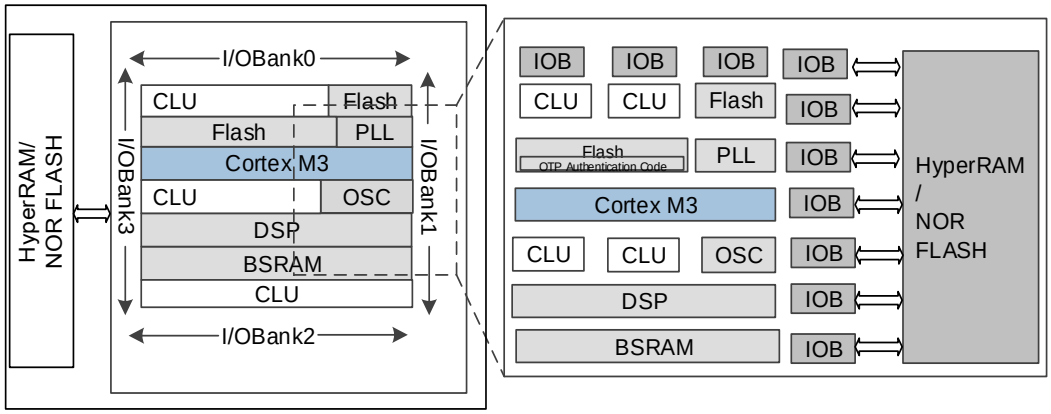
**Note!**

- JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The Max. User I/O noted in this table is referred to when the four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O. When mode [2:0] = 001, JTAGSEL_N and the four JTAG pins (TCK, TDI, TDO, and TMS) can be used as GPIO simultaneously, and the Max. user I/O is increased by one. See UG884, *GW1NSER series of SecureFPGA products Package and Pinout User Guide* for more details.
- The package types in this data sheet are written with abbreviations. See 5.1Part Nam.
- Please refer to UG883, *GW1NSER-4C Pinout*.

# 3 Architecture

## 3.1 Architecture Overview

**Figure 3-1 GW1NSER-4C Architecture Overview**




GW1NSER is one form of SIP chip, integrated with the GW1NSE series of FPGA products and PSRAM chip. For HypeRAM features and overview, see 3.3 HyperRAM. For NOR FLASH features and overview, see 3.4 NOR FLASH.

Except for the basic units of CFU, I/O, GW1NSER series of SecureFPGA products include Cortex-M3, BSRAM, PLL, on-chip oscillator, and configuration Flash resources. See Table 2-1 for more detailed information.

GW1NSER series of SecureFPGA products provide a Root of Trust based on SRAM PUF technology. SecureFPGA has an OTP (One-Time-Programmable) Authentication Code pre-stored in its internal Non-volatile Flash memory. See 3.2 OTP Authentication Code for further detailed information.

Configurable Function Unit (CFU) is the base cell for the array of the GW1NSER series of SecureFPGA products. Devices with different capacities have different numbers of rows and columns. CFU can be configured as LUT4 mode and ALU mode, and Memory mode. For more detailed information, see 3.5 Configurable Function Unit.

The I/O resources in the GW1NSER series of SecureFPGA products

are arranged around the periphery of the devices in groups referred to as banks, including Bank0, Bank1, Bank2, and Bank3. The I/O resources support multiple level standards, and support basic mode, SRD mode, and generic DDR mode. For more detailed information, see 3.6 IOB.

The BSRAM is embedded as a row in the GW1NSER series of SecureFPGA products. In the FPGA array, each BSRAM occupies three columns of CFU. BSRAM has two usages; however, these cannot be employed simultaneously. One is for the Cortex-M3 processor SRAM in SoC devices, which is used for memory data read/write. One BSRAM capacity is 16 Kbits, and the total capacity is 64 Kbits. One is for user storage. One BSRAM capacity is 18 Kbits, and the total capacity is 72 Kbits. It supports multiple configuration modes and operation modes. For further details, please refer to 3.7 Block SRAM (BSRAM).

The DSP is embedded in the GW1NSER series of SecureFPGA products. DSP blocks are embedded as a row in the FPGA array. Each DSP occupies nine CFU columns. Each DSP block contains two Macros, and each Macro contains two pre-adders, two multipliers with 18 by 18 inputs, and a three input ALU54. For more detailed information, see 3.8 DSP.

GW1NSER series of SecureFPGA products provide one PLL. PLL blocks provide the ability to synthesize clock frequencies. Frequency adjustment (multiply and division), phase adjustment, and duty cycle can be adjusted using the configuration of parameters. There is an internal programmable on-chip oscillator in each of the GW1NSER series of SecureFPGA product. The on-chip oscillator supports the clock frequencies ranging from 2.5 MHz to 120MHz, providing the clock resource for the MSPI mode. It also provides clock resource for user designs with the clock precision reaching ±5%. For more detailed information, see 3.10 Clock.

The Flash resources embedded in the GW1NSER series of SecureFPGA products are used for built-in Flash programming, support instant start and security bit operation, and support AUTO BOOT and DUAL BOOT programming modes. For more detailed information, see 4.7 Configuration Interface Timing Specification.

The Cortex-M3 hard-core processor is embedded in the GW1NSER-4C device. It supports 30 MHz program loading when the system starts up and supports higher speed data/instructions transmission. The AHB expansion bus facilitates communication with external storage devices. The APB bus also facilitates communication with external devices, such as UART. GPIO interfaces are convenient for communicating with the external interfaces. FPGA can be programmed to realize controller functions across different interfaces / standards, such as SPI, $I^2C$, $I^3C$, etc. For more detailed information, see 3.9 Cortex-M3.

FPGA provides abundant CRUs, connecting all the resources in FPGA. For example, routing resources distributed in CFU and IOB connect resources in CFU and IOB. Routing resources can automatically be generated by Gowin software. In addition, the GW1NSER series of

SecureFPGA products also provide abundant GCLKs, long wires (LW), global set/reset (GSR), and programming options, etc. For more detailed information, see 3.10 Clock, 3.11 Long Wire (LW) and 3.12 Global Set/Reset (GSR).

## 3.2 OTP Authentication Code

During the factory authentication provisioning process, the Authentication Code, which is based on SRAM PUF (Physical Un-clone-able Factor), is pre-stored in the internal Non-volatile 128KB Flash memory of SecureFPGA.

After provisioning, user can create their own secure application software, which is compiled and linked with the IID Secure Software library with various encrypt / decrypt / Private-Key-Generation / Public-Key-Generation / Secure-Communication, etc. All the application functions rely on the pre-stored unique and unchanged Authentication Code for activation.

OTP Authentication Code features are as follows:

- PUF Based Secure Element
  - Root key pair generated based on intrinsic properties of internal device SRAM
  - Key pair never stored in device and re-generated each power up
- Intrinsic ID Broadkey Pro Security Library
  - Includes device identification, encryption and symmetric and asymmetric key generation
  - Example code for calling user functions
- Factory Provisioning
  - Device initialized with a key pair based on SRAM PUF
  - Private key never exposed during the manufacturing process
  - CSR and Certificate generated for each individual device
- Common User Applications
  - Secure Boot
  - Key and Signature Generation
  - Encryption/Decryption

## 3.3 HyperRAM

**Features**

- Maximum clock rate: 200MHz
- Double-Data Rate (DDR)
- Clock: Supports single-ended clock and differential clock
- Supports chip select

- Data widthe: 8 bits
- Supports hardware reset
- Read-Write Data Strobe (RWDS)
  - Bidirectional Data Strobe / Mask
  - Output at the start of all transactions to indicate refresh latency
  - Output during read transactions as Read Data Strobe
  - Input during write transactions as Write Data Mask
- Die Stack Address

Performance and Power

- Configurable output drive strength
- Power saving modes: Hybrid Sleep Mode and Deep Power Down
- Configurable Burst characteristics
  - Linear burst
  - Wrapped burst lengths: 16 bytes, 32 bytes, 64 bytes, and 128 bytes
  - Hybrid burst: one wrapped burst followed by linear burst
- Array Refresh Modes: Full Array Refresh and Partial Array Refresh
- Power supply voltage: 1.7V~2.0V or 2.7V~3.6V

For the HyperRAM power supply voltage, please refer to UG883, *GW1NSER-4C Pinout*.

The IP Core Generator in Gowin YunYuan software supports both the embedded and external HyperRAM controller IP. This controller IP can be used for the HyperRAM power-up, initialization, read calibration, etc., by following the controller read/write timing. For the further detailed information, please refer to *IPUG944, Gowin HyperRAM Memory Interface IP User Guide*.

# 3.4 NOR FLASH

The SoC with the package suffix of ”G”, such as QN48G, is embedded with NOR FLASH, which is used to store Cortex-M3 programms.

**Features**

- 32Mb of storage, 256 bytes per page;
- Supports SPI;
- Clock frequency: 120MHz;
- Continuous read with 8/16/32/64 bytes wrap;
- Software/Hardware Write Protection
  - All/Partial write protection via software setting
  - Enable/Disable protection with WP#Pin;

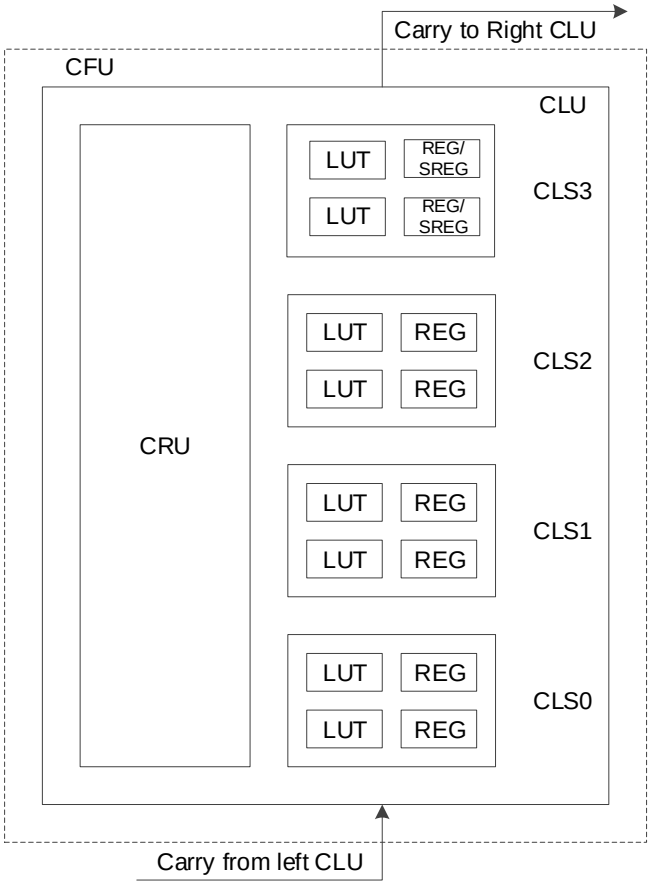
  - Top/Bottom Block protection
- Minimum 100,000 Program/Erase cycles;
- Fast program/ Erase Speed
  - Page program time: 0.7ms;
  - Sector erase time: 90ms;
  - Block erase time: 0.45s;
  - Chip erase time: 20s
- Flexible Architecture
  - Sector: 4K byte
  - Block: 32/64K byte
  - Erase/Program Suspend/Resume
- Low power
  - Stand-by current: 35uA;
  - Power down current: 0.2uA;
- Security Features
  - 128 bits unique ID for each device;
  - 3x1024Byte security registers with OTP Lock
- Data retention: 20 years

Gowin has designed a SPI Nor Flash Interface IP that provides a common command interface for you to interconnect with the SPI Nor Flash chip to fulfill their memory access needs. For further detailed information, please refer to IPUG945, Gowin SPI Nor Flash Interface IP User Guide.

# 3.5 Configurable Function Unit

The configurable function unit (CFU) is the base cell for the array of the GW1NSER series of SecureFPGA products. Each CFU consists of a configurable logic unit (CLU) and its routing resource configurable routing unit (CRU). In each CLU, there are four Configurable Logic Sections (CLS). Each CLS contains look-up tables (LUT) and registers, as shown in Figure 3-2 below.

**Figure 3-2 CFU Structure**




**Note!**

SERG needs special patch supporting. Please contact Gowin technical support or local O ffice for this patch.

## 3.5.1 CLU

The CLU supports three operation modes: basic logic mode, ALU mode, and memory mode.

- Basic Logic Mode

Each LUT can be configured as one four input LUT. A higher input number of LUT can be formed by combining LUT4 together.

  - Each CLS can form one five input LUT5.
  - Two CLSs can form one six input LUT6.
  - Four CLSs can form one seven input LUT7.
  - Eight CLSs (two CLUs) can form one eight input LUT8.

- ALU Mode

When combined with carry chain logic, the LUT can be configured as the ALU mode to implement the following functions.

  - Adder and subtractor
  - Up/down counter

- Comparator,including greater-than, less-than, and not-equal-to
- MULT

**Register**

Each Configurable Logic Section (CLS0~CLS2) has two registers (REG), as shown in Figure 3-3 below.

**Figure 3-3 Register in CLS**

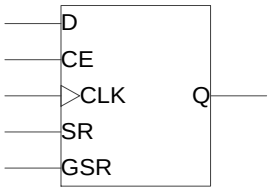



**Table 3-1 Register Description in CFU**

| Signal | I/O | Description |
|---|---|---|
| D | I | Data input [1] |
| CE | I | CLK enable, can be high or low effective [2] |
| CLK | I | Clock, can be rising edge or falling edge trigging [2] |
| SR | I | Set/Reset, can be configured as [2]:<br>● Synchronized reset<br>● Synchronized set<br>● Asynchronous reset<br>● Asynchronous set<br>● Non |
| GSE[3,4] | I | Global Set/Reset, can be configured as[4]:<br>● Asynchronous reset<br>● Asynchronous set<br>● Non |
| Q | O | Register |

**Note!**

- [1] The source of the signal D can be the output of a LUT, or the input of the CRU; as such, the register can be used alone when LUTs are in use.
- [2] CE/CLK/SR in CFU is independent.
- [3] In the GW1NSER series of SecureFPGA products,GSR has its own dedicated network.
- [4] When both SR and GSR are effective, GSR has higher priority.

### 3.5.2 CRU

The main functions of the CRU are as follows:

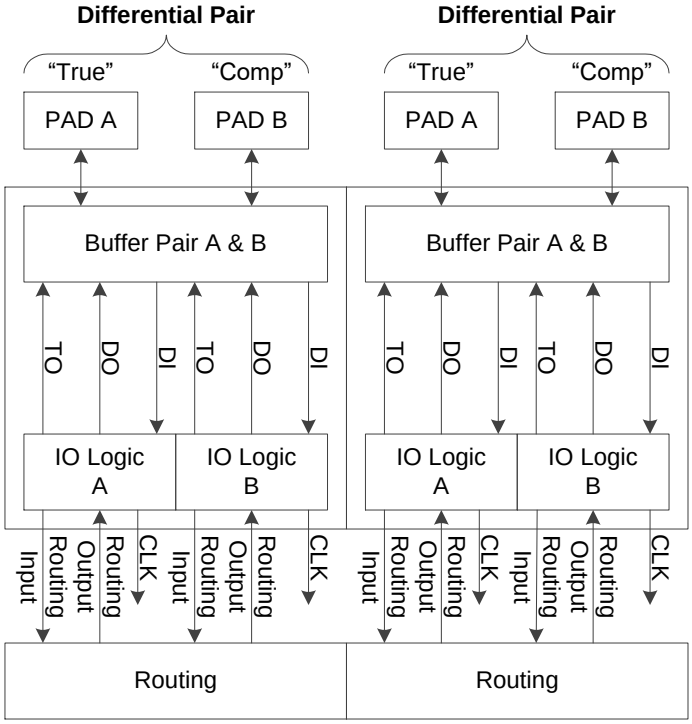
- Input selection: Select input signals for the CFU.
- Configurable routing: Connect the input and output of the CFUs, including inside the CFU, CFU to CFU, and CFU to other functional blocks in FPGA.

## 3.6 IOB

The IOB in the GW1NSER series of SecureFPGA products includes

IO buffer, IO logic, and its routing unit. As shown in Figure 3-4, each IOB connects to two pins (Marked A and B). They can be used as a differential pair or as two single-end input/output.

**Figure 3-4 IOB Structure View**



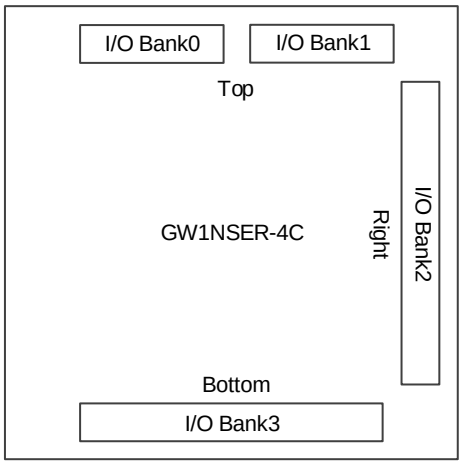

IOB Features:

- $V_{CCIO}$ supplied with each bank
- Supports multiple levels of LVCMOS, PCI, LVTTL, LVDS, SSTL, and HSTL; The BANK3 of GW1NSER-4C only supports Single Port LVCMOS input/output and LVDS25E differential output.
- Input hysteresis option
- Output drive strength option
- Individual Bus Keeper, Weak Pull-up, Weak Pull-down, and Open Drain option
- Supports hot socket, excluding the BANK3 of GW1NSER-4C;
- IO logic supports basic mode, SRD mode, and generic DDR mode
- The BANK0/BANK1 of GW1NSER-4C supports MIPI input
- The BANK2 of GW1NSER-4C supports MIPI output
- The BANK0/BANK1/BANK2 of GW1NSER-4C supports I3C

### 3.6.1 I/O Buffer

There are four IO Banks in the GW1NSER series of SecureFPGA products, as shown in Figure 3-5. To support SSTL, HSTL, etc., each bank also provides one independent voltage source ($V_{REF}$) as referenced voltage. The user can choose from the internal reference voltage of the bank (0.5 x $V_{CCIO}$) or the external reference voltage using any IO from the bank.

**Figure 3-5 GW1NSER-4C I/O Bank Distribution**




GW1NSER-4C supports LV.

The core voltage of the GW1NSER series of SecureFPGA products is 1.2V;

LX has no linear voltage regulator, and $V_{CCX}$ needs to be set to 1.8V. The I/O Bank voltage $V_{CCIO}$ can be set as 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V aCCIOrding to requirements.

UX has linear voltage regulator, and $V_{CCX}$ needs to be set to 2.5 V. The I/O Bank voltage $V_{CCIO}$ can be set as 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V aCCIOrding to requirements.

**Note!**

- $V_{CCIO0}$/$V_{CCIO1}$ needs to be set as 1.2V when BANK0/BANK1 of GW1NSER-4C is used as MIPI input; $V_{CCIO2}$ needs to be set as 1.2V when BANK2 is used as MIPI output, and when $V_{CCX}$ is set as 1.8V, the MIPI speed can only reach 60% of that when $V_{CCX}$ is set as 2.5V/3.3V.
- During configuration, all GPIOs of the device are internally weak pull-up. After the configuration is complete, the I/O state is controlled by user programs and constraints. The state of configuration-related I/Os varies depending on the configuration mode.

For the $V_{CCIO}$ requirements of different I/O standards, see Table 3-2 and Table 3-3.

**Table 3-2 Output I/O Standards and Configuration Options**

| I/O output standard | Single-ended/Differential | Bank $V_{CCIO}$ (V) | Drive Strength (mA) | Typical Application |
|---|---|---|---|---|
| LVCMOS33/ LVTTL33 | Single-ended | 3.3 | 4,8,12,16,24 | Universal interface |
| LVCMOS25 | Single-ended | 2.5 | 4,8,12,16 | Universal interface |

| I/O output standard | Single-ended/Differential | Bank $V_{CCIO}$ (V) | Drive Strength (mA) | Typical Application |
|---|---|---|---|---|
| LVCMOS18 | Single-ended | 1.8 | 4,8,12 | Universal interface |
| LVCMOS15 | Single-ended | 1.5 | 4,8 | Universal interface |
| LVCMOS12 | Single-ended | 1.2 | 4,8 | Universal interface |
| SSTL25_I | Single-ended | 2.5 | 8 | Memory interface |
| SSTL25_II | Single-ended | 2.5 | 8 | Memory interface |
| SSTL33_I | Single-ended | 3.3 | 8 | Memory interface |
| SSTL33_II | Single-ended | 3.3 | 8 | Memory interface |
| SSTL18_I | Single-ended | 1.8 | 8 | Memory interface |
| SSTL18_II | Single-ended | 1.8 | 8 | Memory interface |
| SSTL15 | Single-ended | 1.5 | 8 | Memory interface |
| HSTL18_I | Single-ended | 1.8 | 8 | Memory interface |
| HSTL18_II | Single-ended | 1.8 | 8 | Memory interface |
| HSTL15_I | Single-ended | 1.5 | 8 | Memory interface |
| PCI33 | Single-ended | 3.3 | 8/4 | PC and embedded system |
| LVPECL33E | Differential | 3.3 | 16 | High-speed data transmission |
| MVLDS25E | Differential | 2.5 | 16 | LCD timing driver interface and column driver interface |
| BLVDS25E | Differential | 2.5 | 16 | Multi-point high-speed data transmission |
| RSDS25E | Differential | 2.5 | 8 | High-speed point-to-point data transmission |
| LVDS25E | Differential | 2.5 | 8 | High-speed point-to-point data transmission |
| MIPI | Differential（MIPI） | 1.2 | N/A | Mobile Industry Processor Interface |
| LVDS25 | Differential（True LVDS） | 2.5/3.3 | N/A | High-speed point-to-point data transmission |
| RSDS | Differential（True LVDS） | 2.5/3.3 | N/A | High-speed point-to-point data transmission |
| MINILVDS | Differential（True LVDS） | 2.5/3.3 | N/A | LCD timing driver interface and column driver interface |
| PPLVDS | Differential（True LVDS） | 2.5/3.3 | N/A | LCD row/column driver |
| SSTL15D | Differential | 1.5 | 8 | Memory interface |

| I/O output standard | Single-ended/Differential | Bank $V_{CCIO}$ (V) | Drive Strength (mA) | Typical Application |
|---|---|---|---|---|
| SSTL25D_I | Differential | 2.5 | 8 | Memory interface |
| SSTL25D_II | Differential | 2.5 | 8 | Memory interface |
| SSTL33D_I | Differential | 3.3 | 8 | Memory interface |
| SSTL33D_II | Differential | 3.3 | 8 | Memory interface |
| SSTL18D_I | Differential | 1.8 | 8 | Memory interface |
| SSTL18D_II | Differential | 1.8 | 8 | Memory interface |
| HSTL18D_I | Differential | 1.8 | 8 | Memory interface |
| HSTL18D_II | Differential | 1.8 | 8 | Memory interface |
| HSTL15D_I | Differential | 1.5 | 8 | Memory interface |
| LVCMOS12D | Differential | 1.2 | 4,8 | Universal interface |
| LVCMOS15D | Differential | 1.5 | 4,8 | Universal interface |
| LVCMOS18D | Differential | 1.8 | 4,8,12 | Universal interface |
| LVCMOS25D | Differential | 2.5 | 4,8,12,16 | Universal interface |
| LVCMOS33D | Differential | 3.3 | 4,8,12,16,24 | Universal interface |

**Table 3-3 Input I/O Standards and Configuration Options**

| I/O Input Standard | Single/Differ | Bank $V_{CCIO}$ (V) | Hysteresis | Need $V_{REF}$ |
|---|---|---|---|---|
| LVCMOS33/ LVTTL33 | Single-ended | 1.2/1.5/1.8/2.5/3.3 | Yes | No |
| LVCMOS25 | Single-ended | 1.2/1.5/1.8/2.5/3.3 | Yes | No |
| LVCMOS18 | Single-ended | 1.2/1.5/1.8/2.5/3.3 | Yes | No |
| LVCMOS15 | Single-ended | 1.2/1.5/1.8/2.5/3.3 | Yes | No |
| LVCMOS12 | Single-ended | 1.2/1.5/1.8/2.5/3.3 | Yes | No |
| SSTL15 | Single-ended | 1.5/1.8/2.5/3.3 | No | Yes |
| SSTL25_I | Single-ended | 2.5/3.3 | No | Yes |
| SSTL25_II | Single-ended | 2.5/3.3 | No | Yes |
| SSTL33_I | Single-ended | 3.3 | No | Yes |
| SSTL33_II | Single-ended | 3.3 | No | Yes |
| SSTL18_I | Single-ended | 1.8/2.5/3.3 | No | Yes |
| SSTL18_II | Single-ended | 1.8/2.5/3.3 | No | Yes |
| HSTL18_I | Single-ended | 1.8/2.5/3.3 | No | Yes |
| HSTL18_II | Single-ended | 1.8/2.5/3.3 | No | Yes |
| HSTL15_I | Single-ended | 1.5/1.8/2.5/3.3 | No | Yes |
| LVCMOS33OD25 | Single-ended | 2.5 | No | No |
| LVCMOS33OD18 | Single-ended | 1.8 | No | No |
| LVCMOS33OD15 | Single-ended | 1.5 | No | No |
| LVCMOS25OD18 | Single-ended | 1.8 | No | No |
| LVCMOS25OD15 | Single-ended | 1.5 | No | No |
| LVCMOS18OD15 | Single-ended | 1.5 | No | No |
| LVCMOS15OD12 | Single-ended | 1.2 | No | No |
| LVCMOS25UD33 | Single-ended | 3.3 | No | No |
| LVCMOS18UD25 | Single-ended | 2.5 | No | No |
| LVCMOS18UD33 | Single-ended | 3.3 | No | No |
| LVCMOS15UD18 | Single-ended | 1.8 | No | No |
| LVCMOS15UD25 | Single-ended | 2.5 | No | No |
| LVCMOS15UD33 | Single-ended | 3.3 | No | No |
| LVCMOS12UD15 | Single-ended | 1.5 | No | No |
| LVCMOS12UD18 | Single-ended | 1.8 | No | No |
| LVCMOS12UD25 | Single-ended | 2.5 | No | No |
| LVCMOS12UD33 | Single-ended | 3.3 | No | No |
| PCI33 | Single-ended | 3.3 | Yes | No |
| VREF1_DRIVER | Single-ended (Vref Input) | 1.2/1.5/1.8/2.5/3.3 | No | Yes |
| MIPI | Differential (MIPI) | 1.2 | No | No |
| LVDS25 | Differential | 2.5/3.3 | No | No |
| RSDS | Differential | 2.5/3.3 | No | No |

| I/O Input Standard | Single/Differ | Bank $V_{CCIO}$ (V) | Hysteresis | Need $V_{REF}$ |
|---|---|---|---|---|
| MINILVDS | Differential | 2.5/3.3 | No | No |
| PPLVDS | Differential | 2.5/3.3 | No | No |
| LVDS25E | Differential | 2.5/3.3 | No | No |
| MLVDS25E | Differential | 2.5/3.3 | No | No |
| BLVDS25E | Differential | 2.5/3.3 | No | No |
| RSDS25E | Differential | 2.5/3.3 | No | No |
| LVPECL33E | Differential | 3.3 | No | No |
| SSTL15D | Differential | 1.5/1.8/2.5/3.3 | No | No |
| SSTL25D_I | Differential | 2.5/3.3 | No | No |
| SSTL25D_II | Differential | 2.5/3.3 | No | No |
| SSTL33D_I | Differential | 3.3 | No | No |
| SSTL33D_II | Differential | 3.3 | No | No |
| SSTL18D_I | Differential | 1.8/2.5/3.3 | No | No |
| SSTL18D_II | Differential | 1.8/2.5/3.3 | No | No |
| HSTL18D_I | Differential | 1.8/2.5/3.3 | No | No |
| HSTL18D_II | Differential | 1.8/2.5/3.3 | No | No |
| HSTL15D_I | Differential | 1.5/1.8/2.5/3.3 | No | No |
| LVCMOS12D | Differential | 1.2/1.5/1.8/2.5/3.3 | No | No |
| LVCMOS15D | Differential | 1.5/1.8/2.5/3.3 | No | No |
| LVCMOS18D | Differential | 1.8/2.5/3.3 | No | No |
| LVCMOS25D | Differential | 2.5/3.3 | No | No |
| LVCMOS33D | Differential | 3.3 | No | No |

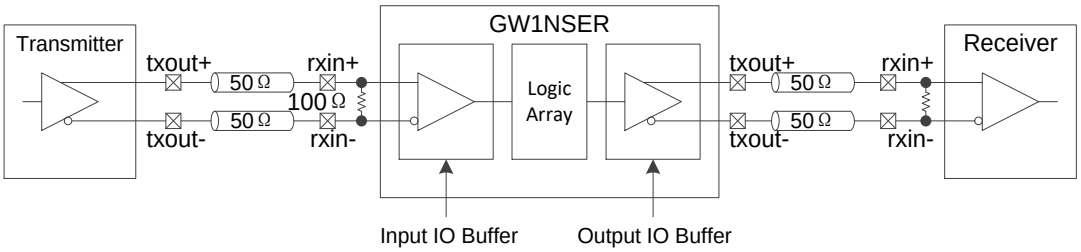
### 3.6.2 True LVDS Design

Bank2 in the GW1NSER-4C device supports true LVDS output.I/Os support LVDS25E, MLVDS25E, BLVDS25E, etc.

For more detailed information about true LVDS, please refer to *UG883, GW1NSER-4C Pinout*.

True LVDS input I/O needs a 100Ω termination resistor. See Figure 3-6 for the true LVDS design. Bank 0/1 of the GW1NSER-4C device support a programmable on-chip 100 ohm input differential termination resistor, see *UG289, Gowin Programable IO User Guide*.

**Figure 3-6 True LVDS Design**




For more information about termination for LVDS25E, MLVDS25E, and BLVDS25E, please refer to *UG289, Gowin Programmable IO User Guide*.

## 3.6.3 I/O Logic

Figure 3-7 shows the I/O logic input and output of the GW1NSER series of SecureFPGA products.

**Figure 3-7 I/O Logic Input and Output**

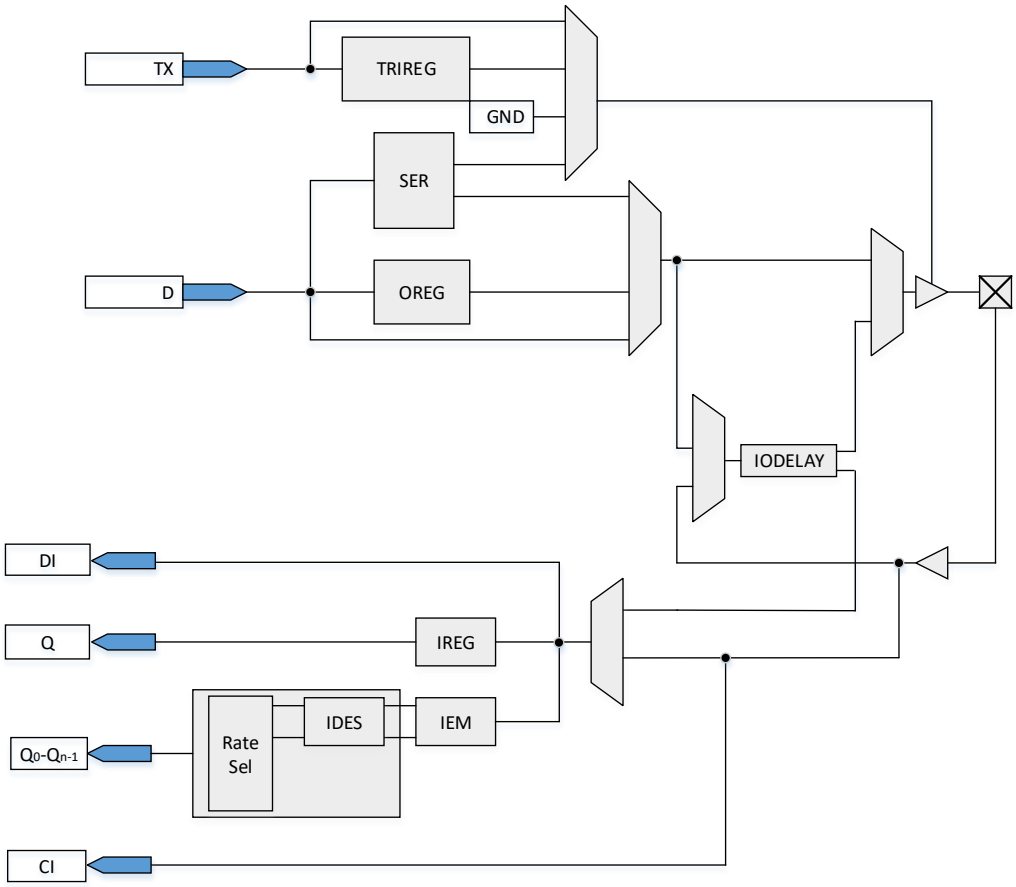



**Table 3-1 Port Descsription**

| Ports | I/O | Description |
|---|---|---|
| CI[1] | Input | GCLK input signal.<br>For the number of GCLK input signals, please refer to UG883, *GW1NSER-4C Pinout*. |
| DI | Input | IO port low-speed input signal, entering into Fabric directly. |
| Q | Output | IREG output signal in SDR module. |
| $Q_0$-$Q_{n-1}$ | Output | IDES output signal in DDR module. |

**Note!**

When CI is used as GCLK input, DI, Q, and $Q_0$-$Q_{n-1}$ cannot be used as I/O input and output.

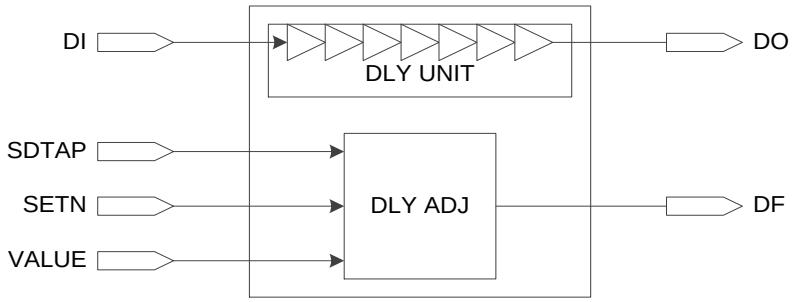
A description of the I/O logic modules of the GW1NSER series of SecureFPGA products is presented below:

### IODELAY

See Figure 3-8 for an overview of the IODELAY. Each I/O of the

GW1NSER series of SecureFPGA products has an IODELAY cell. A total of 128(0~127) step delay is provided, with one-step delay time of about 30ps.

**Figure 3-8 IODELAY**



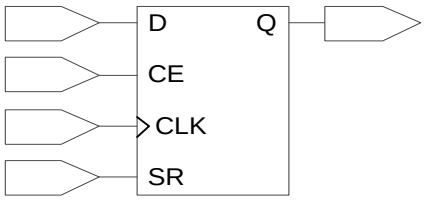

There are two ways to control the delay cell:

- Static control:
- Dynamic control: usually used to sample delay window together with IEM. The IODELAY cannot be used for both input and output at the same time

### I/O Register

See Figure Figure 3-9 for the I/O register in the GW1NSER series of SecureFPGA products. Each I/O provides one input register (IREG), one output register (OREG), and a tristate Register (TRIREG).

**Figure 3-9 Register Structure in I/O Logic**



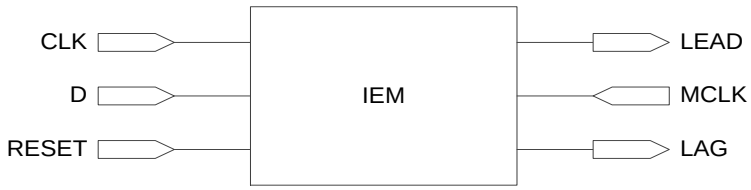

**Note!**

- CE can be either active ow (0: enable)or active high (1: enable).
- CLK can be either rising edge trigger or falling edge trigger.
- SR can be either synchronous/asynchronous SET or RESET or disable.
- The register can be programmed as register or latch.

### IEM

IEM is for sampling clock edge and is used in the generic DDR mode. See Figure 3-10 for the IEM structure.

**Figure 3-10 IEM Structure**



#### De-serializer DES

The GW1NSER series of SecureFPGA products provide a simple Serializer SER for each output I/O to support advanced I/O protocols.

#### Serializer SER

The GW1NSER series of SecureFPGA products provide a simple Serializer SER for each output I/O to support advanced I/O protocols.

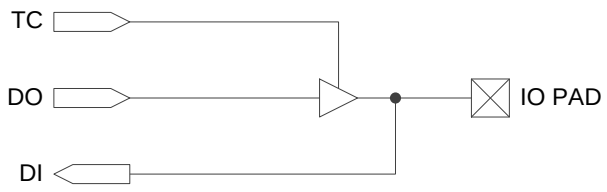
### 3.6.4 I/O Logic Modes

The I/O Logic in the GW1NSER series of SecureFPGA products supports several modes. In each operation, the I/O (or I/O differential pair) can be configured as output, input, and INOUT or tristate output (output signal with tristate control).

#### Basic Mode

In basic mode, the I/O Logic is as shown in Figure 3-11, and the TC, DO, and DI signals can connect to the internal cores directly through CRU.

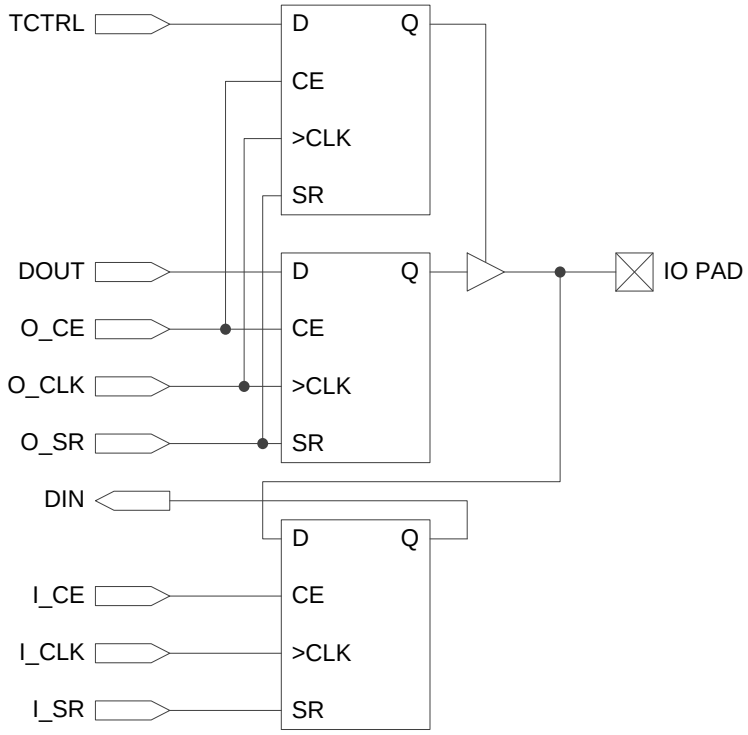
**Figure 3-11 I/O Logic in Basic Mode**




#### SDR Mode

In comparison with the basic mode, SDR utilizes the IO register, as shown in Figure 3-12. This can effectively improve IO timing.

**Figure 3-12 I/O Logic in SDR Mode**




**Note!**

- CLK enable O_CE and I_CE can be configured as active high or active low;
- O_CLK and I_CLK can be either rising edge trigger or falling edge trigger;
- Local set/reset signal O_SR and I_SR can be either Synchronized reset,Synchronized set, Asynchronous reset, Asynchronous set, or no-function;
- I/O in SDR mode can be configured as basic register or latch.

## Generic DDR Mode

Higher speed I/O protocols can be supported in generic DDR mode.

Figure 3-13 shows the generic DDR input, with a speed ratio of the internal logic to PAD 1:2.

**Figure 3-13 I/O Logic in DDR Input Mode**

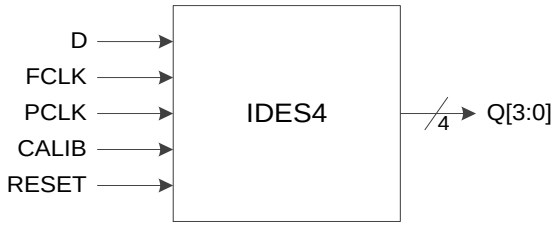

Figure 3-14 shows generic DDR output, with a speed ratio of PAD to FPGA internal logic 2:1.

**Figure 3-14 I/O Logic in DDR Output Mode**

### IDES4

In IDES4 mode, the speed ratio of the PAD to FPGA internal logic is 1:4.

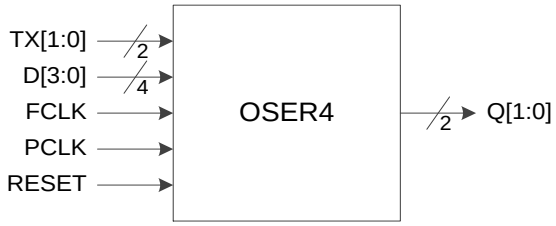
**Figure 3-15 I/O Logic in IDES4 Mode**




### OSER4 Mode

In OSER4 mode, the speed ratio of the PAD to FPGA internal logic is 4:1.

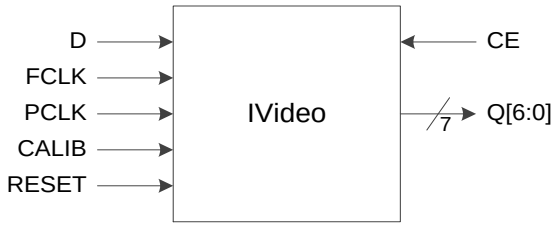
**Figure 3-16 I/O Logic in OSER4 Mode**




### IVideo Mode

In IVideo mode, the speed ratio of the PAD to FPGA internal logic is 1:7.

**Figure 3-17 I/O Logic in IVideo Mode**



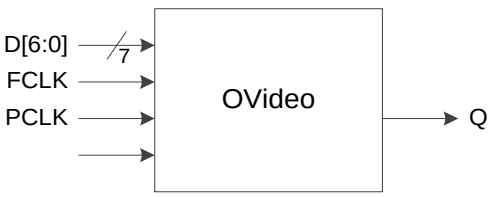

**Note!**

IVideo and IDES8/10 will occupy the neighboring I/O logic. If the I/O logic of a single port is occupied, the pin can only be programmed in SDR or BASIC mode.

### OVideo Mode

In OVideo mode, the speed ratio of the PAD to FPGA internal logic is 7:1.

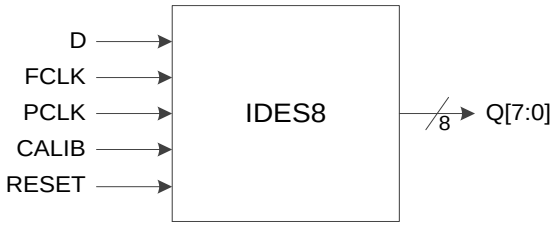
**Figure 3-18 I/O Logic in OVideo Mode**



### IDES8 Mode

In IDES8 mode, the speed ratio of the PAD to FPGA internal logic is 1:8.

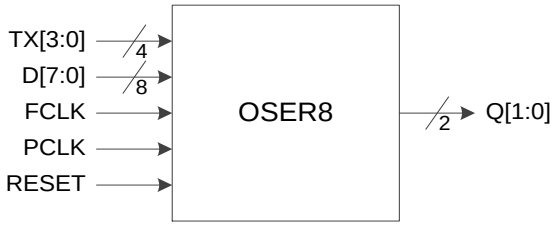
**Figure 3-19 I/O Logic in IDES8 Mode**




### OSER8 Mode

In OSER8 mode, the speed ratio of the PAD to FPGA internal logic is 8:1.

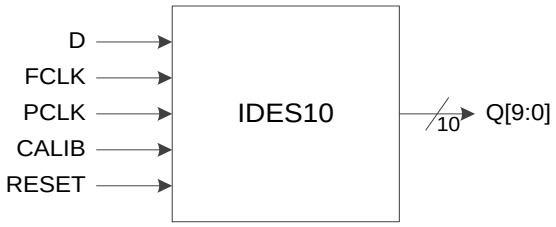
**Figure 3-20 I/O Logic in OSER8 Mode**




### IDES10 Mode

In IDES10 mode, the speed ratio of the PAD to FPGA internal logic is 1:10.

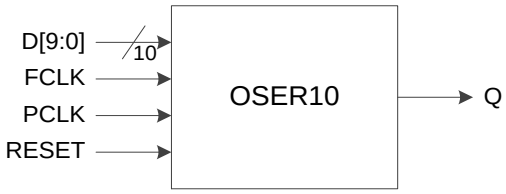
**Figure 3-21 I/O Logic in IDES10 Mode**




### OSER10 Mode

In OSER10 mode, the speed ratio of the PAD to FPGA internal logic is 10:1.

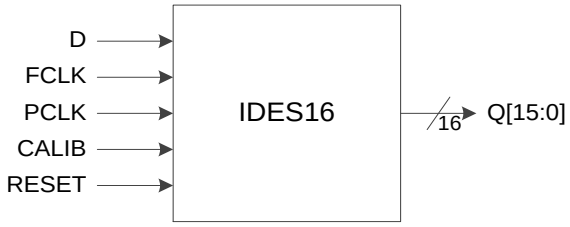
**Figure 3-22 I/O Logic in OSER10 Mode**




### IDES16 Mode

In IDES16 mode, the speed ratio of the PAD to FPGA internal logic is 1:16.

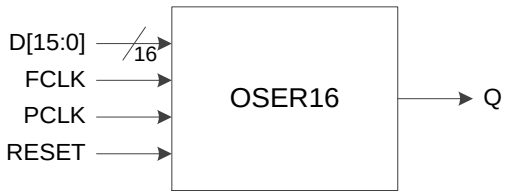
**Figure 3-23 I/O Logic in IDES16 Mode**




## OSER16 Mode

In OSER16 mode, the speed ratio of the PAD to FPGA internal logic is 16:1.

**Figure 3-24 I/O Logic in OSER16 Mode**



# 3.7 Block SRAM (BSRAM)

## 3.7.1 Introduction

GW1NSER series of SecureFPGA products provide abundant SRAM. The Block SRAM (BSRAM) is embedded as a row in the FPGA array and is different from SSRAM (Shadow SRAM). Each BSRAM occupies three columns of CFU in the FPGA array.

BSRAM supports two usages:

1. Used for Cortex-M3 SRAM, providing high-speed read/write functions for Cortex-M3 to ensure system operation. Cortex-M3 reads/writes the data using AHB bus. The data bit width is 32bits. Each BSRAM provides 8 bits data. The address depth is 2048, and the total capacity is 64Kbits. In this way, this BSRAM cannot be used as FPGA data storage.
2. Used for FPGA data storage. Each BSRAM can be configured up to 18,432 bits (18Kbits). In this way, this BSRAM cannot be used as Cortex-M3 SRAM. There are 5 operation modes: Single Port, Dual Port, Semi Dual Port, ROM, and FIFO.

An abundance of BSRAM resources provide a guarantee for the user's high-performance design. BSRAM features:

- Max.18,432 bits per BSRAM
- BSRAM itself can run at 190MHz at max
- Single Port
- Dual Port
- Semi Dual Port
- Parity bits
- ROM
- Data width from 1 to 36 bits
- Mixed clock mode
- Mixed data width mode
- Enable Byte operation for double byte or above
- Normal Read and Write Mode
- Read-before-write Mode
- Write-through Mode

For further detailed information, please refer to UG285, Gowin BSRAM & SSRAM User Guide.

## 3.7.2 Memory Configuration Mode

The BSRAM mode in the GW1NSER series of SecureFPGA products supports different data bus widths. See Table 3-4.

**Table 3-4 Memory Size Configuration**

| Single Port Mode | Dual Port Mode | Semi-Dual Port Mode | Read Only |
|---|---|---|---|
| 16K x 1 | 16K x 1 | 16K x 1 | 16K x 1 |
| 8K x 2 | 8K x 2 | 8K x 2 | 8K x 2 |
| 4K x 4 | 4K x 4 | 4K x 4 | 4K x 4 |
| 2K x 8 | 2K x 8 | 2K x 8 | 2K x 8 |
| 1K x 16 | 1K x 16 | 1K x 16 | 1K x 16 |
| 512 x 32 | - | 512 x 32 | 512 x 32 |
| 2K x 9 | 2K x 9 | 2K x 9 | 2K x 9 |
| 1K x 18 | 1K x 18 | 1K x 18 | 1K x 18 |
| 512 x 36 | - | 512 x 36 | 512 x 36 |

### Single Port Mode

The single port mode can support 2 read modes (bypass mode and pipeline mode) and 3 write modes (normal mode, write-through mode, and read-before-write mode). In the single port mode, BSRAM can write to or read from one port at one clock edge. During the write operation, the data can show up at the output of BSRAM. When the output register is bypassed, the new data will show at the same write clock rising edge.

For further information about Single Port Block Memory ports and the related description, please refer to UG285, Gowin BSRAM & SSRAM User Guide.

### Dual Port Mode

The dual port mode can support 2 read modes (bypass mode and pipeline mode) and 2 write modes (normal mode and write-through mode). The applicable operations are as follows:

- Two independent read
- Two independent write
- An independent read and an independent write at different clock frequencies

**Note!**

It is not recommended to perform simultaneous read access from one port and write access from the other port to the same memory address for all modes of the Dual Port BSRAM.

For further information about Dual Port Block Memory ports and the related description, please refer to UG285, Gowin BSRAM & SSRAM User Guide.

### Semi-Dual Port Mode

The semi-dual port mode can support 2 read modes (bypass mode and pipeline mode) and 1 write mode (normal mode). Semi-Dual Port supports read and write at the same time on different ports, but it is not possible to write and read to the same port at the same time. The system only supports write on Port A, read on Port B.

**Note!**

It is not recommended to perform simultaneous read access from one port and write access from the other port to the same memory address for all modes of the Semi-Dual Port BSRAM.

For further information about Semi-Dual Port Block Memory ports and the related description, please refer to UG285, Gowin BSRAM & SSRAM User Guide.

### Read Only

BSRAM can be configured as ROM. The ROM can be initialized during the device configuration stage, and the ROM data needs to be provided in the initialization file. Initialization completes during the device power-on process.

Each BSRAM can be configured as one 16 Kbits ROM. For further information about Read Only Port Block Memory ports and the related description, please refer to UG285, Gowin BSRAM & SSRAM User Guide.

## 3.7.3 Mixed Data Bus Width Configuration

BSRAM in the GW1NSER series of SecureFPGA products supports mixed data bus width operation. In the dual port and semi-dual port modes, the data bus width for read and write can be different. For the configuration options that are available, please see Table 3-5 and Table 3-6 below.

**Table 3-5 Dual Port Mixed Read/Write Data Width Configuration**

| Read Port | Write Port | | | | | | |
|---|---|---|---|---|---|---|---|
| | 16K x 1 | 8K x 2 | 4K x 4 | 2K x 8 | 1K x 16 | 2K x 9 | 1K x 18 |
| 16K x 1 | * | * | * | * | * | | |
| 8K x 2 | * | * | * | * | * | | |
| 4K x 4 | * | * | * | * | * | | |
| 2K x 8 | * | * | * | * | * | | |
| 1K x 16 | * | * | * | * | * | | |
| 2K x 9 | | | | | | * | * |
| 1K x 18 | | | | | | * | * |

**Note!**

"*"denotes the modes supported.

**Table 3-6 Semi Dual Port Mixed Read/Write Data Width Configuration**

| Read Port | Write Port | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | 16K x 1 | 8K x 2 | 4K x 4 | 2K x 8 | 1K x 16 | 512 x 32 | 2K x 9 | 1K x 18 | 512 x 36 |
| 16K x 1 | * | * | * | * | * | * | | | |
| 8K x 2 | * | * | * | * | * | * | | | |
| 4K x 4 | * | * | * | * | * | * | | | |
| 2K x 8 | * | * | * | * | * | * | | | |
| 1K x 16 | * | * | * | * | * | * | | | |
| 512x32 | * | * | * | * | * | * | | | |
| 2K x 9 | | | | | | | * | * | * |
| 1K x 18 | | | | | | | * | * | * |

**Note!**

"*"denotes the modes supported.

## 3.7.4 Byte-enable

The BSRAM in the GW1NSER series of SecureFPGA products supports byte-enable. For data longer than a byte, the additional bits can be blocked, and only the selected portion can be written into. The blocked bits will be retained for future operation. Read/write enable ports (WREA, WREB), and byte-enable parameter options can be used to control the BSRAM write operation.

## 3.7.5 Parity Bit

There are parity bits in BSRAMs. The 9th bit in each byte can be used as a parity bit to check the correctness of data transmission.It can also be used for data storage.

## 3.7.6 Synchronous Operation

- All the input registers of BSRAM support synchronous write;
- The output registers can be used as pipeline register to improve design performance;
- The output registers are bypass-able.

## 3.7.7 Power up Conditions

BSRAM initialization is supported when powering up. During the power-up process, BSRAM is in standby mode, and all the data outputs are “0”. This also applies in ROM mode.

## 3.7.8 BSRAM Operation Modes

BSRAM supports five different operations, including two read operations (Bypass Mode and Pipeline Read Mode) and three write operations (Normal Write Mode, Write-through Mode, and Read-before-write Mode).

### Read Mode

Read data from the BSRAM via output registers or without using the registers.

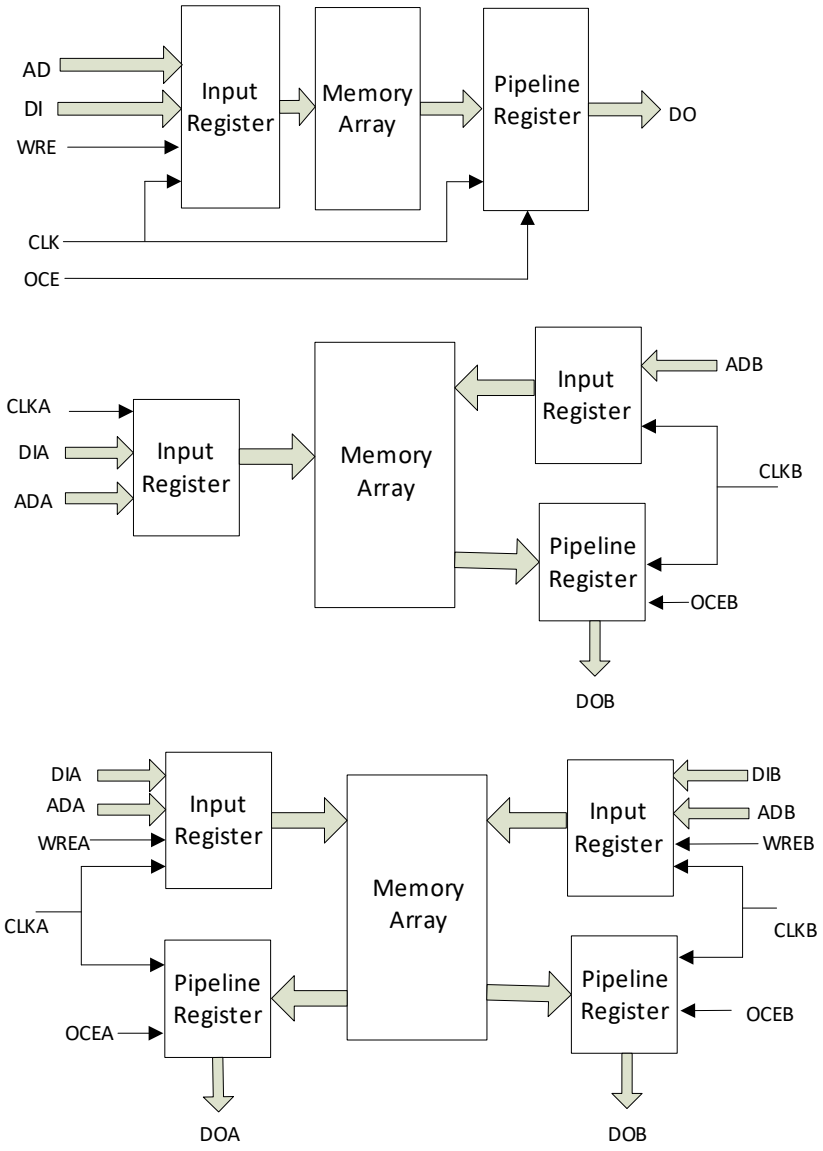
### Pipeline Mode

While writing in the BSRAM, the output register and pipeline register are also being written. The data bus can be up to 36 bits in this mode.

### Bypass Mode

The output register is not used. The data is kept in the output of memory array.

**Figure 3-25 Pipeline Mode in Single Port, Dual Port and Semi-Dual Port**




### Write Mode

#### NORMAL WRITE MODE

In this mode, when the user writes data to one port, and the output

data of this port does not change. The data written in will not appear at the read port.

#### WRITE-THROUGH MODE

In this mode, when the user writes data to one port, and the data written in will also appear at the output of this port.

#### READ-BEFORE-WRITE MODE

In this mode, when the user writes data to one port, and the data written in will be stored in the memory aCCIOrding to the address. The original data in this address will appear at the output of this port.

## 3.7.9 Clock Operations

Table 3-7 lists the clock operations in different BSRAM modes:

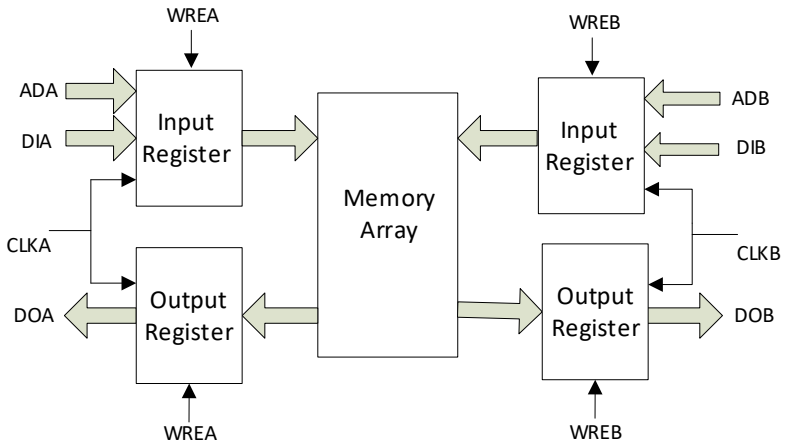
**Table 3-7 Clock Operations in Different BSRAM Modes**

| Clock Operations | Dual Port Mode | Semi-Dual Port Mode | Single Port Mode |
|---|---|---|---|
| Independent Clock Mode | Yes | No | No |
| Read/Write Clock Mode | Yes | Yes | No |
| Single Port Clock Mode | No | No | Yes |

### Independent Clock Mode

Figure 3-26 shows the independent clocks in dual port mode with each port with one clock. CLKA controls all the registers at Port A; CLKB controls all the registers at Port B.

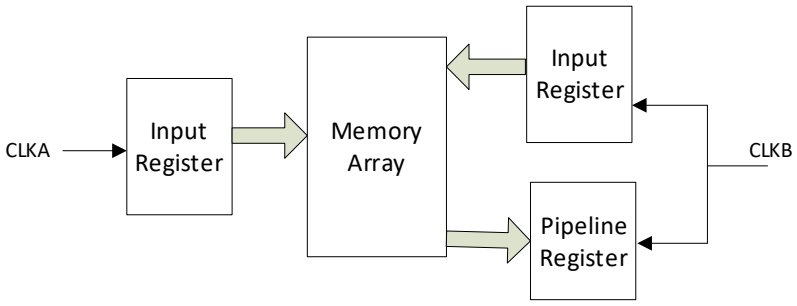
**Figure 3-26 Independent Clock Mode**




### Read/Write Clock Operation

Figure 3-27 shows the read/write clock operations in the semi-dual port mode with one clock at each port. The write clock (CLKA) controls Port A data inputs, write address and read/write enable signals. The read clock (CLKB) controls Port B data output, read address, and read enable signals.

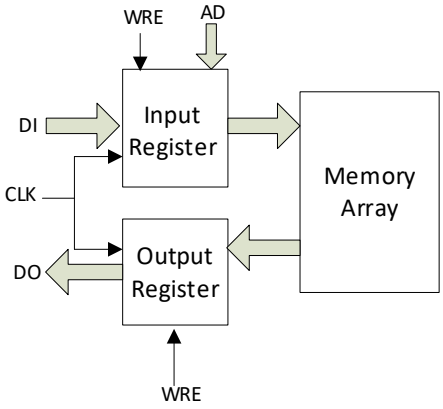
**Figure 3-27 Read/Write Clock Mode**




### Single Port Clock Mode

Figure 3-28 shows the clock operation in single port mode.

**Figure 3-28 Single Port Clock Mode**




# 3.8 DSP

## 3.8.1 Introduction

GW1NSER-4C device offers abundant DSP modules. Gowin DSP solutions can meet user demands for high performance digital signal processing design, such as FIR, FFT, etc. DSP blocks have the advantages of stable timing performance, high-usage, and low-power.

DSP offers the following functions:

- Multiplier with three widths: 9-bit, 18-bit, 36-bit
- 54-bit ALU
- Multipliers cascading to support wider data
- Barrel shifter
- Adaptive filtering through signal feedback
- Computing with options to round to a positive number or a prime number
- Supports pipeline mode and bypass mode.

## 3.8.2 Macro

DSP blocks are embedded as rows in the FPGA array. Each DSP occupies nine CFU columns. Each DSP block contains two Macro, and

each Macro contains two pre-adders, two 18 x 18 bit multipliers, and one three-input ALU.

**PADD**

Each DSP macro features two units of pre-adders to implement pre-add, pre-subtraction, and shifting.

PADD locates at the first stage with two inputs.,

- Parallel 18-bit input B or SBI;
- Parallel 18-bit input A or SIA.

**Note!**

Each input end supports pipeline mode and bypass mode.

GOWINSEMI PADD can be used as function block independently, which supports 9-bit and 18-bit width.

**MULT**

Multipliers locate after the pre-adder. Multipliers can be configured as 9 x 9, 18 x 18, 36 x 18 or 36 x 36. Registered mode and bypass mode are supported both in input and output ports. The configuration modes that a macro supports include:

- One 18 x 36 multiplier
- Two 18 x 18 multipliers
- Four 9 x 9 multipliers

**Note!**

Two adjacent DSP macros can form a 36 x 36 multiplier.

**ALU**

Each Macro has one 54 bits ALU54, which can further enhance MULT's functions. The registered and bypass mode are supported both in input and output ports. The functions are as following:

- Multiplier output data / 0, addition/subtraction operations for data A and data B;
- Multiplier output data / 0, addition/subtraction operations for data B and bit C;
- Addition/subtraction operations for data A, data B, and bit C;

### 3.8.3 DSP Operations

- Multiplier
- Accumulator
- MULTADDALU

For the detailed information, please refer to UG287, Gowin Digital Signal Processing (DSP) User Guide.

# 3.9 Cortex-M3

## 3.9.1 Introduction

GW1NSER-4C is a system-on-chip FPGA device that incorporates a microprocessor system hard core, Gowin FPGA fabric, and other standard peripherals and featured hard cores, including 128 K-Byte Flash, 8 KB Block RAM, PLL, and OSC. The embedded microprocessor system contains a low-power, low-cost and high-performance ARM Cortex-M3 32-bit RISC. The flexible FPGA fabric serves as user programmable peripherals, or soft-core IPs.

The embedded microprocessor system consists of the processor block, with ARM Cortex-M3 32-bit RISC core and associated supporting bus system that connects to harden standard peripherals. The FPGA fabric contains a rich programmable logic resource called a Configured Functional Unit (CFU). This offers a flexible architecture that allows the user to employ peripherals with the microprocessor system. This can be achieved either by parameterized soft-core IPs, I2C or I3C. The microprosessor system only interfaces with the FPGA fabric and JTAG config-core internally with no access to the I/O Blocks of GW1NSER-4C.

The bus system consists of AHB-Lite Bus, AHB2APB Bridge, and two APB Bus: APB1 and APB2.

The microprocessor system relies on AHB bus to access FPGA side sub-memory system which has a pre-implemented sub-memory system controller for read-only-access 128 KB Flash-ROM and read/write-access 8 KB BSRAM. Upon Power-On boot loading, Cortex-M3 loads instructions and data that are pre-stored in the Flash-ROM, and transfers it to the BSRAM before initiating the execution.

In addition, there are two AHB bus extension ports: INTEXP0 and TARGEXP0. Each of these AHB extension ports provides a 126-bit AHB bus interconnecting to any high-speed User programmable peripherals implemented within the FPGA. A GPIO block interconnects the AHB bus with the FPGA fabric to allow the user to implement general purpose I/O functions in FPGA.

In terms of the two APB Bus (APB1 and APB2), APB1 interconnects with two timers (Timer0 and Timer1), two UARTs (Uart0 and Uart1), and one watchdog. Two UARTs connect to the FPGA directly. The two timers and the watchdog are controlled and used within the microprocessor system and are accessed through REG. The APB2 bus connects directly to the FPGA.

The processor block consists of Cortex-M3 core, bus matrix, Nested Vector Interrupt Controller (NVIC), Debug Access Port (DAP), and time stamp.

The Cortex-M3 core relies on the bus-matrix to access its supporting bus system (AHB-Lite Bus, AHB2APB Bridge, and two APB Bus: APB1 and APB2).

GW1NSER-4C offers six user interruptions. The DAP contains JTAG

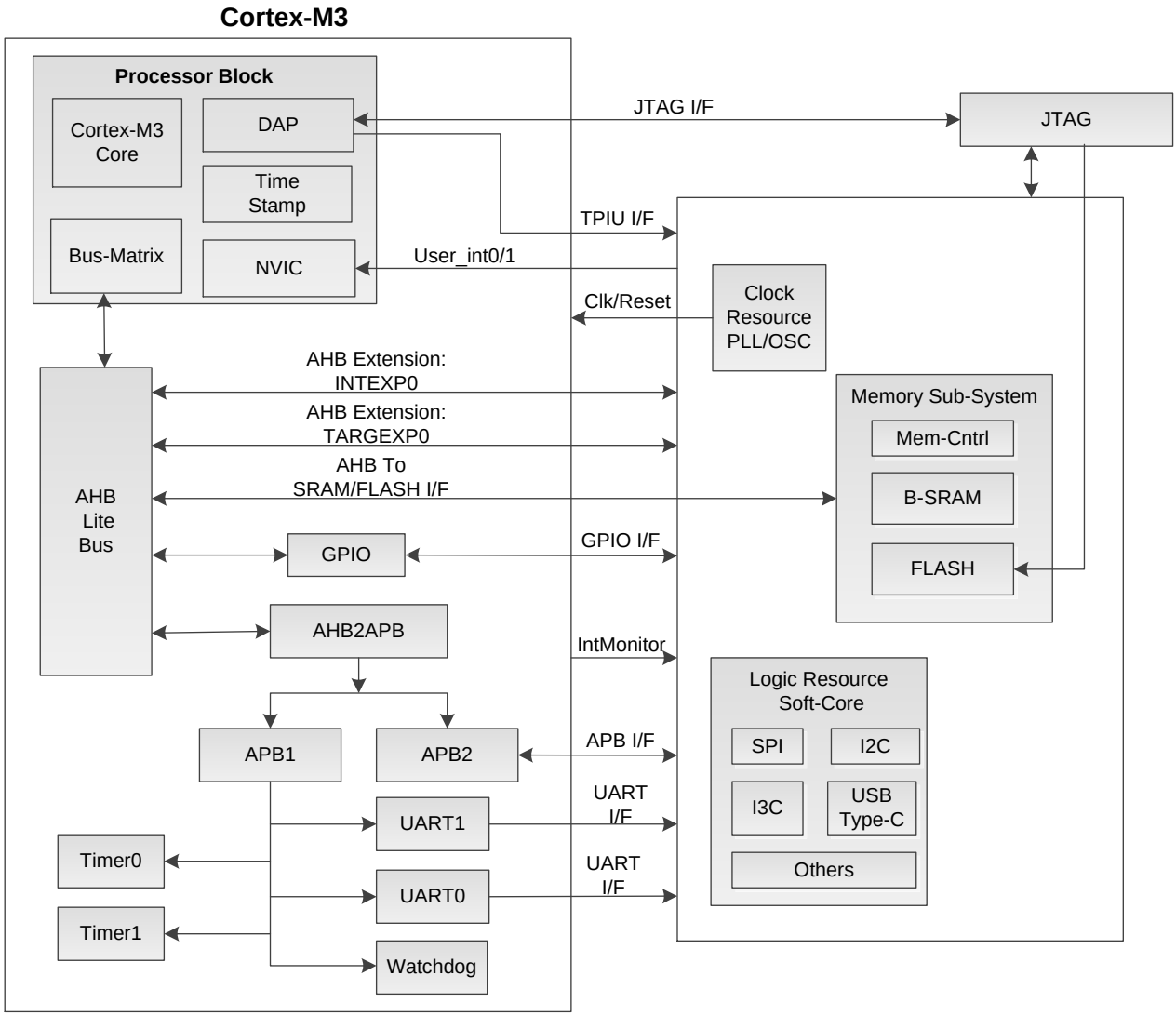
DAP and also Trace-Port-Interface-Unit (TPIU).

The Microprocessor System also provides an interrupt monitor signal, which combines GPIO interrupts as well as APB1 peripherals (UART0, UART1, Timer0, Timer1, Watchdog) interrupts, back to the FPGA fabric to report the current run-time interrupt Status of the Microprocessor System.

FPGA fabric takes advantage of its rich Clocking Resource (PLL, OSC) and provides the Main Clock, Power-On Reset and System Reset signals to the embedded microprocessor system.

See Figure 3-29 for the Cortex-M3 architecture.

**Figure 3-29 Cortex-M3 Architecture**




## 3.9.2 Cortex-M3

### Features

- Compact core
- Thumb-2 instruction set, delivering the high-performance expected of an ARM core in the memory size usually

- Associated with 8 bits and 16 bits devices; typically, in the range of a few kilobytes of memory for microcontroller class applications
- Rapid application execution through Harvard architecture characterized by separate buses for instruction and data
- Achieves exceptional interrupt handling, by implementing the register manipulations required for handling an interrupt in hardware.
- Deterministic, fast interrupt processing.
- Memory protection unit (MPU), providing a privileged mode for protecting operation system functionality
- Migration from the ARM7™ processor family for better performance and power efficiency
- Full-featured debug solution
  - JTAG Debug Port (JTAG)
  - Flash Patch and Breakpoint (FPB) unit for implementing breakpoints
  - Data Watchpoint and Trigger (DWT) unit for implementing watchpoints, trigger resources, and system profiling
  - Instrumentation Trace Macrocell (ITM) for support of print style debugging
  - Trace Port Interface Unit (TPIU) for bridging to a Trace Port Analyzer

### 3.9.3 Bus-Matrix

The bus-matrix is used to connect the Cortex-M3 processor and debug port with an external AHB bus. **Connections between bus-matrix and AHB bus:**

- ICode bus: 32bit AHBLite bus, used for fetching instructions and vectors from code space;
- DCode bus: 32bit AHBLite bus, used for data loading/storage and debug access;
- System bus: 32bit AHBLite bus, used for fetching instructions and vectors from system space, data loading/storage and debug access;
- APB: 32bit APB bus, used for external space data loading/storage and debug access.

The bus-matrix controls the following functions as below:

- Unaligned accesses: Converts the unaligned processor access to aligned access;
- Bit-banding: converts the alias access of Bit_band to Bit_band space access;
- Write buffer: Bus-matrix contains one write-buffer, ensuring that the processor core is not affected by bus delay.

### 3.9.4 NVIC

NVIC features:

- Supports low-latency interrupt processing up to 26 interrupts
- GW1NSER-4C supports six external user defined interrupts
- A programmable priority level of 0-7 for each interrupts. A higher level corresponds to a lower priority; as such level 0 is the highest interrupt priority
- Low-latency exception and interrupt handling
- Dynamic reprioritization of interrupts
- The processor automatically stacks its state on exception entry and unstacks this state on exception exit, with no instruction overhead.

**Table 3-8 NVIC Interrupt Vector Table**

| Address | Name | Type | Description |
|---|---|---|---|
| 0x00000000 | _StackTop | Read only | Top of stack interrupt |
| 0x00000004 | Reset_Handler | Read only | Reset interrupt |
| 0x00000008 | NMI_Handler | Read only | NMI interrupt |
| 0x0000000C | HardFault_Handler | Read only | Hard fault interrupt |
| 0x00000010 | MemMange_Handler | Read only | MPU fault interrupt |
| 0x00000014 | BusFault_Handler | Read/Write | Bus fault interrupt |
| 0x00000018 | UsageFault_Handler | Read only | Usage fault interrupt |
| 0x0000002C | SVC_Handler | Read/Write | SVCall interrupt |
| 0x00000030 | DebugMon_Handler | Read only | Debug monitor interrupt |
| 0x00000038 | PendSV_Handler | Read/ Write/ Read only | Pending interrupt |
| 0x0000003C | SysTick_Handler | Read/Write | System timer interrupt |
| External interrupt | | | |
| 0x00000040 | UART0_Handler | Read/Write | UART0 reception and sending interrupt |
| 0x00000048 | UART1_Handler | Read/Write | UART1 reception and sending interrupt |
| 0x00000058 | PORT0_COMB_Handler | Read/Write | GPIO0 interrupt |
| 0x00000060 | TIMER0_Handler | Read/Write | TIMER0 interrupt |
| 0x00000064 | TIMER1_Handler | Read/Write | TIMER1 interrupt |
| 0x00000070 | UARTOVF_Handler | Read/Write | UART0/UART1 overflow interrupt |
| 0x00000074 | USER_INT0 | Read/Write | Flash system error interrupt |
| 0x00000078 | USER_INT1 | Read/Write | Embedded flash interrupt |
| 0x00000080 | PORT0_0_Handler | Read/Write | GPIO0 Pin 0 interrupt |
| 0x00000084 | PORT0_1_Handler | Read/Write | GPIO0 Pin 1 interrupt |
| 0x00000088 | PORT0_2_Handler | Read/Write | GPIO0 Pin 2 interrupt |

| Address | Name | Type | Description |
|---|---|---|---|
| 0x0000008C | PORT0_3_Handler | Read/Write | GPIO0 Pin 3 interrupt |
| 0x00000090 | PORT0_4_Handler | Read/Write | GPIO0 Pin 4 interrupt |
| 0x00000094 | PORT0_5_Handler | Read/Write | GPIO0 Pin 5 interrupt |
| 0x00000098 | PORT0_6_Handler | Read/Write | GPIO0 Pin 6 interrupt |
| 0x0000009C | PORT0_7_Handler | Read/Write | GPIO0 Pin 7 interrupt |
| 0x000000A0 | PORT0_8_Handler | Read/Write | GPIO0 Pin 8 interrupt |
| 0x000000A4 | PORT0_9_Handler | Read/Write | GPIO0 Pin 9 interrupt |
| 0x000000A8 | PORT0_10_Handler | Read/Write | GPIO0 Pin 10 interrupt |
| 0x000000AC | PORT0_11_Handler | Read/Write | GPIO0 Pin 11 interrupt |
| 0x000000B0 | PORT0_12_Handler | Read/Write | GPIO0 Pin 12 interrupt |
| 0x000000B4 | PORT0_13_Handler | Read/Write | GPIO0 Pin 13 interrupt |
| 0x000000B8 | PORT0_14_Handler | Read/Write | GPIO0 Pin 14 interrupt |
| 0x000000BC | PORT0_15_Handler | Read/Write | GPIO0 Pin 15 interrupt |

### 3.9.5 Boot Loader

The boot loader loads the initial stack pointer value from the program memory, and branches to the reset handler that the reset vector specifies in the program memory.

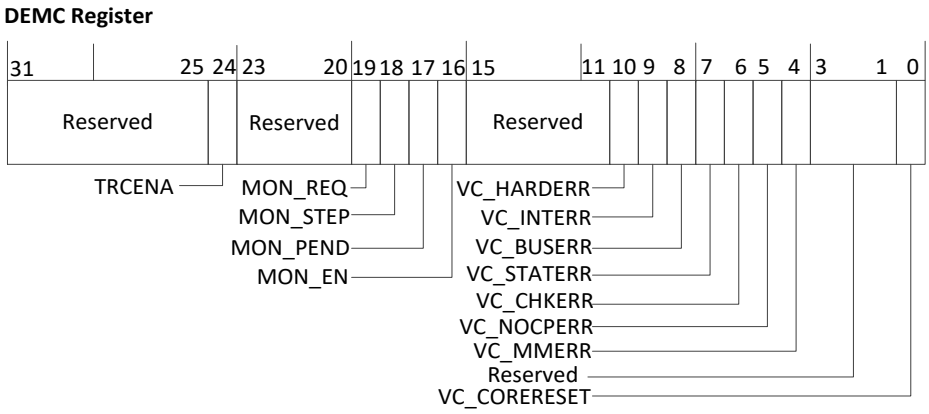
The current boot loader is based on UART Message Monitor which is easy to interface as a communication port with PC host. Below is an example of how to deploy the boot loader:

- Power-on reset to enter the reset handler to call the boot loader;
- Setup UART0 registers, such as BAUDIV and CTRL, to program the appropriate TX speed rate for the send and receive function;
- Begin Flash loader subroutine execution such as memory test, timer0, and timer1 tests etc;
- Write a 0x4 character (EOP) to terminate the program.

### 3.9.6 TimeStamp

A 48 bits timestamp counter is included and connected to the ITM. It is clock gated and enabled by the Trace Enable (TRCENA) bit of DEMCR (0xE000EDFC) Debug Exception and monitor control register, which is a global enable bit that enables both the Data Watch Trace (DWT) and Intrumental Trace Module (ITM) on behalf of the debug of the Cortex-M3 microprocessor. The time stamp generator is used during the debug process to set up the break point and marching step, etc.

**Figure 3-30 DEMCR Register**




**Note!**

TRCENA is the global enable for DWT and ITM features:

- 0: DWT and ITM units disabled.
- 1: DWT and ITM units enabled.

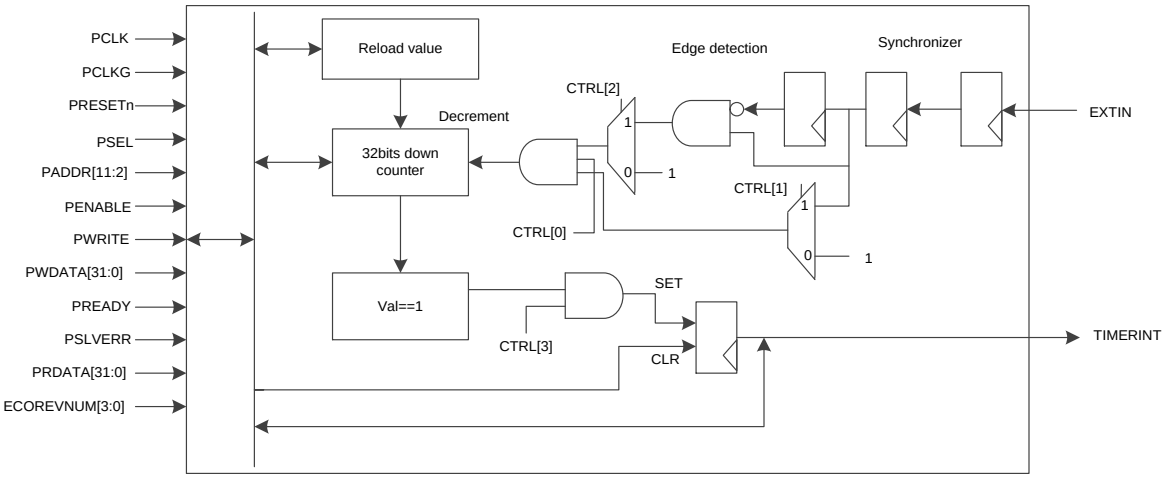
## 3.9.7 Timer

The SoC offers an embedded microprocessor system that contains two synchronous standard timers: Timer0 and Timer1. These can be accessed and controlled through APB1 bus.

Timer0 and Timer1 are 32 bits down-counter with the following features:

- Users can generate an interrupt request signal, TIMERINT, when the counter reaches 0. The interrupt request is held until it is cleared by writing to the INTCLEAR Register.
- Users can employ the zero-to-one transition of the external input signal, EXTIN, as a timer enable.
- If the timer count reaches 0 and, at the same time, the software clears a previous interrupt status, the interrupt status is set to 1.
- The external clock, EXTIN, must be slower than half of the peripheral clock because it is sampled by a double flip-flop before going through edge-detection logic when the external inputs act as a clock.
- Timer0: EXTIN is hard-wired to GPIO[1]
- Timer1: EXTIN is hard-wired to GPIO[6]

**Figure 3-31 Timer0/ Timer1 Structure View**




The Timer0/Timer1 register is as shown in Table 3-18. The Timer0 base address is 0x40000000, and the Timer1 base address is 0x40001000.

**Table 3-9 Timer0/Timer1 Register**

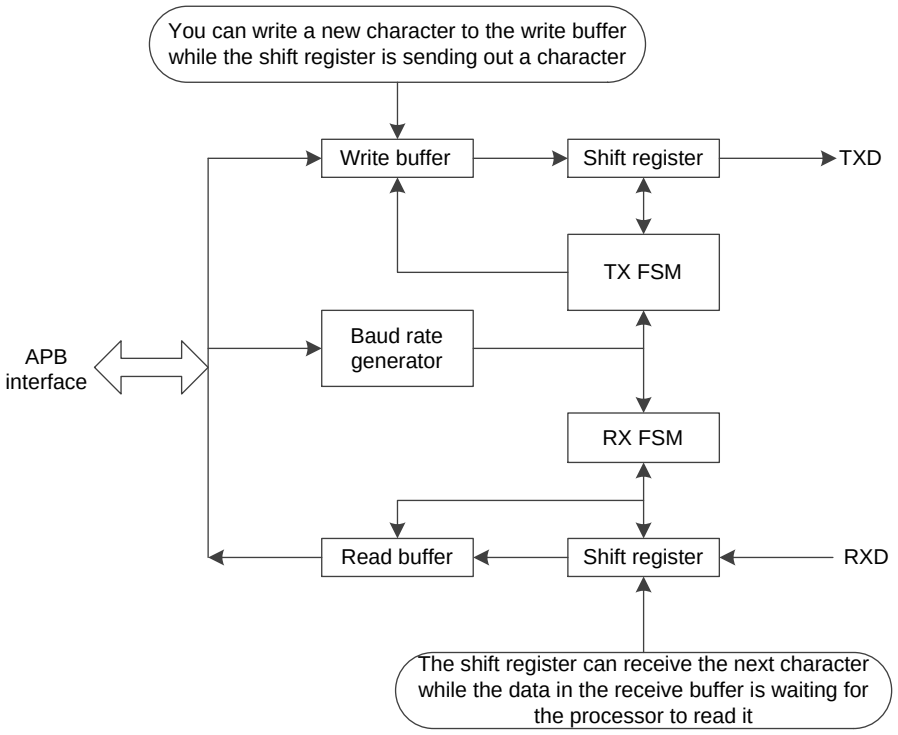
| Name | Base Offset | Type | Data Width | Reset Value | Description |
|---|---|---|---|---|---|
| CTRL | 0x000 | Read/ Write | 4 | 0x0 | [3]: System timer interrupt enable<br>[2]: Select external input as clock<br>[1]: Select external input as enable<br>[0]: Enable |
| VALUE | 0x004 | Read/ Write | 32 | 0x00000000 | Current value |
| RELOAD | 0x008 | Read/ Write | 32 | 0x00000000 | Reload value. Write to this register to set the current value. |
| INTSTATUS /INTCLEAR | 0x00C | Read/ Write | 1 | 0x0 | [0]: Timer interrupt. Write one to clear. |
| PID4 | 0XFD0 | Read only | 8 | 0x04 | Peripheral ID Register 4 |
| PID5 | 0XFD4 | Read only | 8 | 0x00 | Peripheral ID Register 5 |
| PID6 | 0XFD8 | Read only | 8 | 0x00 | Peripheral ID Register 6 |
| PID7 | 0XFDC | Read only | 8 | 0x00 | Peripheral ID Register 7 |
| PID0 | 0XFE0 | Read only | 8 | 0x22 | Peripheral ID Register 0 |
| PID1 | 0XFE4 | Read only | 8 | 0XB8 | Peripheral ID Register 1 |
| PID2 | 0XFE8 | Read only | 8 | 0X1B | Peripheral ID Register 2 |
| PID3 | 0XFEC | Read only | 8 | 0X00 | Peripheral ID Register 3 |
| CID0 | 0XFF0 | Read only | 8 | 0X0D | Component ID Register 0 |
| CID1 | 0XFF4 | Read only | 8 | 0XF0 | Component ID Register 1 |
| CID2 | 0XFF8 | Read only | 8 | 0X05 | Component ID Register 2 |
| CID3 | 0XFFC | Read only | 8 | 0XB1 | Component ID Register 3 |

## 3.9.8 UART

The SoC embedded with microprocessor system contains two UART: UART0 and UART1. These can be accessed and controlled through APB1 bus. The max.baud rate supported is 921.6Kbits/s.

UART0 and UART1 support 8 bits communication without parity and one stop bit.

**Figure 3-32 APB UART Buffering**




UART0 and UART support a high-speed test mode. When CTRL[6] is set to 1, the serial data is transmitted at one bit per clock cycle. This enables you to send text messages in a much shorter simulation time. The APB interface always sends an "OK" response with no wait state. You must program the baud rate divider register BAUDDIV before enabling the UART.

The BAUDTICK output pulses at a frequency of 16 times that of the programmed baud rate. You can use this external signal for capturing UART data in a synchronous environment. The TXEN output signal indicates the status of CTRL[0]. You can use this signal to switch a bidirectional I/O pin in a silicon device to UART data output mode automatically when the UART transmission feature is enabled.

The buffer overrun status in the STATE field is used to drive the overrun interrupt signals. Therefore, clearing the buffer overrun status de-asserts the overrun interrupt, and clearing the overrun interrupt bit also clears the buffer overrun status bit in the STATE field.

See Table 3-19 for the UART Register Description. The UART0 base address is 0x40004000, and the UART1 base address is 0x40005000.

**Table 3-10 UART0/UART1 Register**

| Name | Base Offset | Type | Data Width | Reset Value | Description |
|---|---|---|---|---|---|
| DATA | 0x000 | Read/ Write | 8 | 0x-- | 8 bits data<br>Read: Received data.<br>Write: Transmit data. |
| STATE | 0x004 | Read/ Write | 4 | 0x0 | [3]: RX buffer overrun, write 1 to clear.<br>[2]: TX buffer overrun, write 1 to clear.<br>[1]: RX buffer full, read-only.<br>[0]: TX buffer full, read-only. |
| CTRL | 0x008 | Read/ Write | 7 | 0x00 | [6]：High-speed test mode for TX only.<br>[5]：RX overrun interrupt enable.<br>[4]：TX overrun interrupt enable.<br>[3]：RX interrupt enable.<br>[2]：TX interrupt enable.<br>[1]：RX enable.<br>[0]：TX enable. |
| INTSTATUS /INTCLEAR | 0x00C | Read/ Write | 4 | 0x0 | [3]：RX overrun interrupt, write 1 to clear.<br>[2]：TX overrun interrupt, write 1 to clear.<br>[1]：RX interrupt, write 1 to clear.<br>[0]：TX interrupt, write 1 to clear. |
| BAUDDIV | 0x010 | Read/ Write | 20 | 0x00000 | [19:0]: Baud rate divider. The minimum number is 16. |
| PID4 | 0XFD0 | Read only | 8 | 0x04 | Peripheral ID Register 4 |
| PID5 | 0XFD4 | Read only | 8 | 0x00 | Peripheral ID Register 5 |
| PID6 | 0XFD8 | Read only | 8 | 0x00 | Peripheral ID Register 6 |
| PID7 | 0XFDC | Read only | 8 | 0x00 | Peripheral ID Register 7 |
| PID0 | 0XFE0 | Read only | 8 | 0x21 | Peripheral ID Register 0 |
| PID1 | 0XFE4 | Read only | 8 | 0XB8 | Peripheral ID Register 1 |
| PID2 | 0XFE8 | Read only | 8 | 0X1B | Peripheral ID Register 2 |
| PID3 | 0XFEC | Read only | 8 | 0X00 | Peripheral ID Register 3 |
| CID0 | 0XFF0 | Read only | 8 | 0X0D | Component ID Register 0 |
| CID1 | 0XFF4 | Read only | 8 | 0XF0 | Component ID Register 1 |
| CID2 | 0XFF8 | Read only | 8 | 0X05 | Component ID Register 2 |
| CID3 | 0XFFC | Read only | 8 | 0XB1 | Component ID Register 3 |

### 3.9.9 Watchdog

The SoC embedded with microprocessor system contains one watchdog module. This can be accessed and controlled through the APB1 bus.

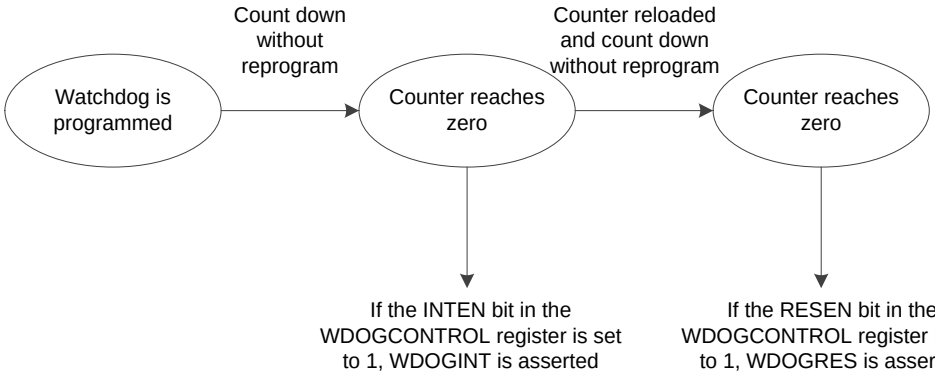
The APB watchdog module is based on a 32 bits down-counter that is initialized from the reload register, WDOGLOAD.

The watchdog module generates a regular interrupt, WDOGINT, depending on a programmed value. The counter decrements by one on each positive clock edge of WDOGCLK when the clock enable, WDOGCLKEN, is HIGH. The watchdog monitors the interrupt and asserts a reset request WDOGRES signal when the counter reaches 0, and the counter is stopped. On the next enabled WDOGCLK clock edge, the counter is reloaded from the WDOGLOAD register and the countdown sequence continues.

The watchdog module applies a reset to a system in the event of a software failure, providing a way to recover from software crashes. For example, if the interrupt is not cleared by the time the counter next reaches 0, the watchdog module initiates the reset signal.

Figure 3-39 below depicts the watchdog operation.

**Figure 3-33 Watchdog Operation**




The watchdog register is as shown in Table 3-20. The watchdog base address is 0x40008000.

**Table 3-11 Watchdog Register**

| Name | Base Offset | Type | Data Width | Reset Value | Description |
|---|---|---|---|---|---|
| WDOGLOAD | 0x00 | Read/ Write | 32 | 0xFFFFFFFF | Watchdog Load Register |
| WDOGVALUE | 0x04 | Read only | 32 | 0xFFFFFFFF | Watchdog Value Register |
| WDOGCONTROL | 0x08 | Read/ Write | 2 | 0x0 | Watchdog Control Register<br>[1]：<br>[0]： |
| WDOGINTCLR | 0x0C | Write only | - | 0x- | Watchdog Clear Interrupt Register |
| WDOGRIS | 0x10 | Read only | 1 | 0x0 | Watchdog Raw Interrupt Status Register |
| WDOGMIS | 0x14 | Read only | 1 | 0x0 | Watchdog Interrupt Status Register |
| WDOGLOCK | 0xC00 | Read/ Write | 32 | 0x0 | Watchdog Lock Register |
| WDOGTCR | 0xF00 | Read/ Write | 1 | 0x0 | Watchdog Integration Test Control Register |
| WDOGTOP | 0xF04 | Write only | 2 | 0x0 | Watchdog Integration Test Output Set Register |
| WDOGPERIPHID4 | 0XFD0 | Read only | 8 | 0x04 | Peripheral ID Register 4 |
| WDOGPERIPHID5 | 0XFD4 | Read only | 8 | 0x00 | Peripheral ID Register 5 |
| WDOGPERIPHID6 | 0XFD8 | Read only | 8 | 0x00 | Peripheral ID Register 6 |
| WDOGPERIPHID7 | 0XFDC | Read only | 8 | 0x00 | Peripheral ID Register 7 |
| WDOGPERIPHID0 | 0XFE0 | Read only | 8 | 0x24 | Peripheral ID Register 0 |
| WDOGPERIPHID1 | 0XFE4 | Read only | 8 | 0XB8 | Peripheral ID Register 1 |
| WDOGPERIPHID2 | 0XFE8 | Read only | 8 | 0X1B | Peripheral ID Register 2 |
| WDOGPERIPHID3 | 0XFEC | Read only | 8 | 0X00 | Peripheral ID Register 3 |
| WDOGPCELLID0 | 0XFF0 | Read only | 8 | 0X0D | Component ID Register 0 |
| WDOGPCELLID1 | 0XFF4 | Read only | 8 | 0XF0 | Component ID Register 1 |
| WDOGPCELLID2 | 0XFF8 | Read only | 8 | 0X05 | Component ID Register 2 |
| WDOGPCELLID3 | 0XFFC | Read only | 8 | 0XB1 | Component ID Register 3 |

## 3.9.10 GPIO

The SoC microprocessor system communicates with the GPIO block through the AHB bus. The GIPO block interconnects with the FPGA. GPIO provides a 16 bits I/O interface with the following properties:

- Programmable interrupt generation capability. You can configure each bit of the I/O pins to generate interrupts;

- Bit masking support using address values;
- Registers for alternate function switching with pin multiplexing support;
- Thread safe operation by providing separate set and clear addresses for control registers.

The GPIO register is as shown in Table 3-21. The GPIO base address is 0x40010000.

**Table 3-12 GPIO Register**

| Name | Base Offset | Type | Data Width | Reset Value | Description |
|---|---|---|---|---|---|
| DATA | 0x0000 | Read/ Write | 16 | 0x---- | Data value [15:0] |
| DATAOUT | 0x0004 | Read/ Write | 16 | 0x0000 | Data output register value [15:0] |
| OUTENSET | 0x0010 | Read/ Write | 16 | 0x0000 | Output enable set [15:0]<br>Write 1: Set the output enable bit.<br>Write 0: No effect.<br>Read 1: Indicates the signal direction as output.<br>Read 0: Indicates the signal direction as input. |
| OUTENCLR | 0x0014 | Read/ Write | 16 | 0x0000 | Output enable clear [15:0] |
| ALTFUNCSET | 0x0018 | Read/ Write | 16 | 0x0000 | Alternative function set [15:0]<br>Write 1: Sets the ALTFUNC bit.<br>Write 0: No effect.<br>Read 0: GPIO as I/O<br>Read 1: ALTFUNC Function |
| ALTFUNCCLR | 0x001C | Read/ Write | 16 | 0x0000 | Alternative function clear [15:0] |
| INTENSET | 0x0020 | Read/ Write | 16 | 0x0000 | Interrupt enable set [15:0]<br>Write 1: Sets the enable bit.<br>Write 0: No effect.<br>Read 0: Interrupt disabled.<br>Read 1: Interrupt enabled. |
| INTENCLR | 0x0024 | Read/ Write | 16 | 0x0000 | Interrupt enable clear [15:0]<br>Write 1: Clear the enable bit.<br>Write 0: No effect.<br>Read 0: Interrupt disabled.<br>Read 1: Interrupt enabled. |
| INTTYPESET | 0x0028 | Read/ Write | 16 | 0x0000 | Interrupt type set [15:0] |
| INTTYPECLR | 0x002C | Read/ Write | 16 | 0x0000 | Interrupt type clear [15:0] |
| INTPOLSET | 0x0030 | Read/ Write | 16 | 0x0000 | Polarity-level, edge interrupt request configuration [15:0] |
| INTPOLCLR | 0x0034 | Read/ Write | 16 | 0x0000 | Polarity-level, edge interrupt request configuration [15:0] |
| INTSTATUS/ INTCLEAR | 0x0038 | Read/ Write | 16 | 0x0000 | Read interrupt status register<br>Write 1: Clear the interrupt request |
| MASKLOWBYTE | 0x0400-0x07FC | Read/ Write | 16 | 0x0000 | – |
| MASKHIGHBYTE | 0x0800-0x0BFC | Read/ Write | 16 | 0x0000 | – |

| Name | Base Offset | Type | Data Width | Reset Value | Description |
|---|---|---|---|---|---|
| Reserved | 0x0C00-0x0FCF | – | – | – | Reserved |
| PID4 | 0XFD0 | Read only | 8 | 0x04 | Peripheral ID Register 4 |
| PID5 | 0XFD4 | Read only | 8 | 0x00 | Peripheral ID Register 5 |
| PID6 | 0XFD8 | Read only | 8 | 0x00 | Peripheral ID Register 6 |
| PID7 | 0XFDC | Read only | 8 | 0x00 | Peripheral ID Register 7 |
| PID0 | 0XFE0 | Read only | 8 | 0x20 | Peripheral ID Register 0 |
| PID1 | 0XFE4 | Read only | 8 | 0XB8 | Peripheral ID Register 1 |
| PID2 | 0XFE8 | Read only | 8 | 0X1B | Peripheral ID Register 2 |
| PID3 | 0XFEC | Read only | 8 | 0X00 | Peripheral ID Register 3 |
| CID0 | 0XFF0 | Read only | 8 | 0X0D | Component ID Register 0 |
| CID1 | 0XFF4 | Read only | 8 | 0XF0 | Component ID Register 1 |
| CID2 | 0XFF8 | Read only | 8 | 0X05 | Component ID Register 2 |
| CID3 | 0XFFC | Read only | 8 | 0XB1 | Component ID Register 3 |

### 3.9.11 Debug Access Port

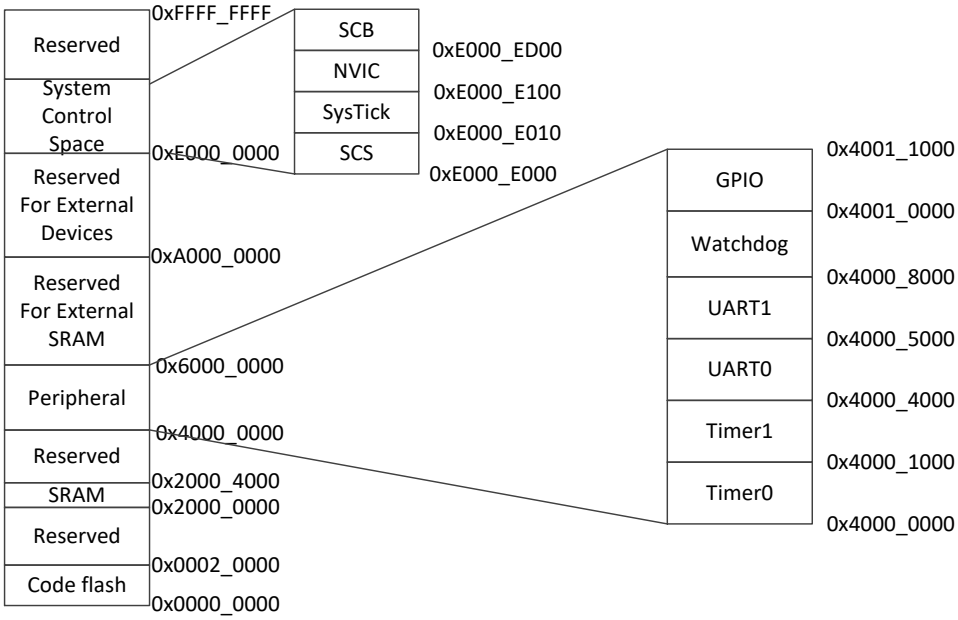
The Cortex-M3 processor block contains a DAP that consist of a JTAG interface and a TPIU interface. Both interface to the FPGA Fabric. The JTAG-DAP is based on the IEEE1149.1 Joint Test Action Group Boundary-Scan Standard.

JTAG-DP functions consist of the following three parts:

- JTAG-DP sate machine
- Instruction register (IR) and the related IR scan chain, which are used to control JTAG and the current register actions
- DR register and the related DR scan chain, which connect with the JTAG-DP register.

## 3.9.12 Memory Mapping

**Figure 3-34 Memory Mapping**




## 3.9.13 Application

Gowin YunYuan software supports the “Cortex-M3” IP call. For further detailed information, please refer to IPUG517, *Gowin_EMPU (GW1NS-2C) Hardware Design Reference Manual.*

# 3.10 Clock

The clock resources and wiring are critical for high-performance applications in FPGA. GW1NSER series of SecureFPGA products provide the global clock network (GCLK) which connects to all the registers directly. Besides the global clock network, the GW1NSER series of SecureFPGA products provide high-speed clock HCLK. PLL, etc are also provided.

For further detailed information, please refer to UG286, Gowin Clock User Guide.

## 3.10.1 Global Clock

The GCLK is distributed in GW1NSER devices as L and R quadrants. Each quadrant provides eight GCLKs. The optional clock resources of GCLK can be pins or CRU. Users can employ dedicated pins as clock resources to achieve better timing.

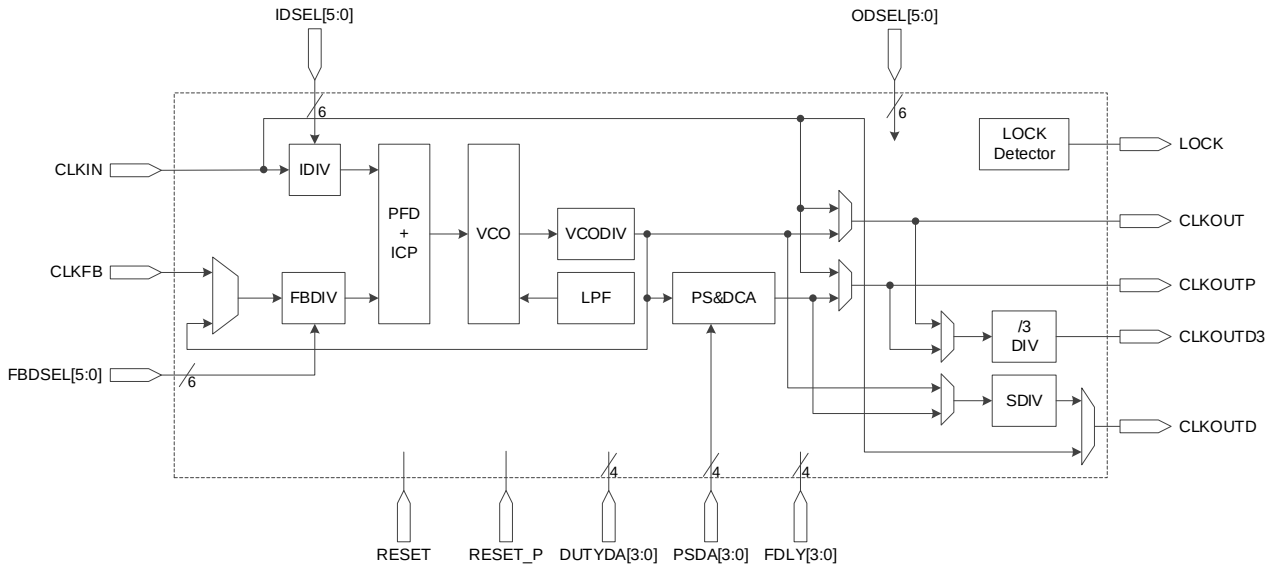
## 3.10.2 PLL

Phase-locked Loop (PLL) is one kind of a feedback control circuit. The frequency and phase of the internal oscillator signal is controlled by the external input reference clock.

PLL blocks provide the ability to synthesize clock frequencies. Frequency adjustment (multiply and division), phase adjustment, and duty cycle can be adjusted by configuring the parameters.

See Figure 3-35 for the PLL structure.

**Figure 3-35 PLL Structure**



See Table 3-13 for a definition of the PLL ports.

**Table 3-13 Definition of the PLL Ports**

| Port Name | Signal | Description |
|---|---|---|
| CLKIN [5：0] | Input | Reference clock input |
| CLKFB | Input | Feedback clock input |
| RESET | Input | PLL reset |
| RESET_P | Input | PLL Power Down |
| IDSEL [5：0] | Input | Dynamic IDIV control: 1~64 |
| FBDSEL [5：0] | Input | Dynamic FBDIV control:1~64 |
| PSDA [3：0] | Input | Dynamic phase control (rising edge effective) |
| DUTYDA [3：0] | Input | Dynamic duty cycle control (falling edge effective) |
| FDLY[3:0] | Input | CLKOUTP dynamic delay control |
| CLKOUT | Output | Clock output with no phase and duty cycle adjustment |
| CLKOUTP | Output | Clock output with phase and duty cycle adjustment |
| CLKOUTD | Output | Clock divider from CLKOUT and CLKOUTP (controlled by SDIV) |
| CLKOUTD3 | Output | clock divider from CLKOUT and CLKOUTP (controlled by DIV3 with the constant division value 3) |
| LOCK | Output | PLL lock status:<br>1: locked,<br>0: unlocked |

The PLL reference clock source can come from an external PLL pin or from internal routing GCLK, HCLK, or general data signal. PLL feedback signal can come from the external PLL feedback input or from internal routing GCLK, HCLK, or general data signal.

For PLL features, please refer to Table 4-20 PLL Parameters.:

PLL can adjust the frequency of the input clock CLKIN (multiply and division). The formulas for doing so are as follows:

- $f_{CLKOUT} = (f_{CLKIN} * FBDIV)/IDIV$
- $f_{VCO} = f_{CLKOUT} * ODIV$
- $f_{CLKOUTD} = f_{CLKOUT}/SDIV$
- $f_{PFD} = f_{CLKIN}/IDIV = f_{CLKOUT}/FBDIV$

**Note!**

- $f_{CLKIN}$: The frequency of the input clock CLKIN
- $f_{CLKOUT}$: The clock frequency of CLKOUT and CLKOUTP
- $f_{CLKOUTD}$: The clock frequency of CLKOUTD, and CLKOUTD is the clock CLKOUT after division
- $f_{PFD}$: PFD Phase Comparison Frequency, and the minimum value of $f_{PFD}$ should be no less than 3MHz.

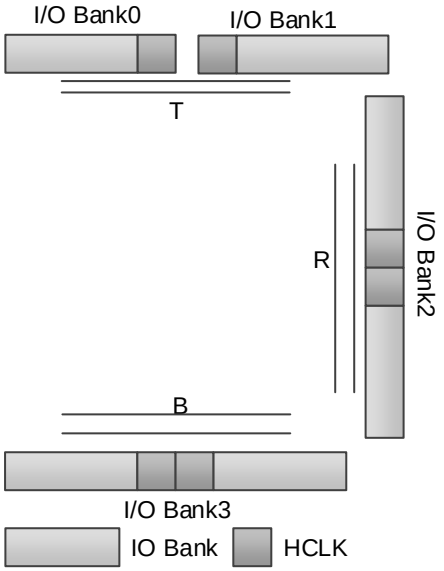
Adjust IDIV, FBDIV, ODIV, and SDIV to achieve the required clock frequency.

## 3.10.3 HCLK

HCLK is the high-speed clock in the GW1NSER series of

SecureFPGA products. It can support high-performance data transfer and is mainly suitable for source synchronous data transfer protocols. See Figure 3-36.

**Figure 3-36 GW1NSER-4C HCLK Distribution**




# 3.11 Long Wire (LW)

As a supplement to the CRU, the GW1NSER series of SecureFPGA products provides another routing resource, Long wire, which can be used as clock, clock enable, set/reset,or other high fan out signals.

# 3.12 Global Set/Reset (GSR)

A global set/rest (GSR) network is built into the GW1NSER series of SecureFPGA product. There is a direct connection to core logic. It can be used as asynchronous/synchronous set or asynchronous/synchronous reset, registers in CFU and I/O can be configured independently.

# 3.13 Programming Configuration

The GW1NSER series of SecureFPGA products support SRAM and Flash. Flash programming mode supports on-chip Flash and off-chip Flash.

Besides JTAG, the GW1NSER series of SecureFPGA products also supports GOWINSEMI's own configuration mode: GowinCONFIG (AUTO BOOT, SSPI, MSPI, DUAL BOOT, SERIAL, and CPU). All the devices support JTAG and AUTO BOOT. For more detailed information, please refer to UG290, *Gowin FPGA Products Programming and Configuration User Guide*.

## 3.13.1 SRAM Configuration

When you adopt SRAM to configure the device, every time the device is powered on, the bit stream file needs to be downloaded to configure the device.

### 3.13.2 Flash Configuration

The Flash configuration data is stored in the on-chip flash. Each time the device is powered on, the configuration data is transferred from the Flash to the SRAM, which controls the working of the device. This mode can complete configuration within a few ms, and is referred to as “Quick Start”. The GW1NSER series of SecureFPGA products also support off-chip Flash configuration and dual-boot. Please refer to UG290, *Gowin FPGA Products Programming and Configuration User Guide* for more detailed information.

## 3.14 On Chip Oscillator

There is an internal oscillator in each of the GW1NSER series of SecureFPGA product. This provides programmable user clock with clock precision ±5%. During the configuration process, it can provide a clock for MSPI mode.

The internal oscillator in GW1NSER-4C device supports user configurable power-saving mode.

The on-chip oscillator also provides a clock resource for user designs. Up to 64 clock frequencies can be obtained by setting the parameters.

The following formula is employed to get the output clock frequency for GW1NSER-4C device: $f_{out}$=210 MHz/Param.

**Note!**

“Param” is the configuration parameter with a range of 2~128. It supports even number only.

The tables below list some frequencies, such as the default frequency, the Max. frequency, and the output decimal frequency for certain parameters.

**Table 3-14 GW1NSER-4C Oscillator Output Frequency Options**

| Mode | Frequency | Mode | Frequency | Mode | Frequency |
|---|---|---|---|---|---|
| 0 | 2.5MHz[1] | 8 | 7.8MHz | 16 | 15.6MHz |
| 1 | 5.4MHz | 9 | 8.3MHz | 17 | 17.9MHz |
| 2 | 5.7MHz | 10 | 8.9MHz | 18 | 21MHz |
| 3 | 6.0MHz | 11 | 9.6MHz | 19 | 25MHz |
| 4 | 6.3MHz | 12 | 10.4MHz | 20 | 31.3MHz |
| 5 | 6.6MHz | 13 | 11.4MHz | 21 | 41.7MHz |
| 6 | 6.9MHz | 14 | 12.5MHz | 22 | 62.5MHz |
| 7 | 7.4MHz | 15 | 13.9MHz | 23 | 125MHz[2] |

**Note!**

- [1] Default frequency
- [2] Not suitable for MSPI programming mode.

# 4 AC/DC Characteristic

**Note!**

Please ensure that you use GOWINSEMI devices within the recommended operating conditions and range. Data beyond the working conditions and range are for reference only. GOWINSEMI does not guarantee that all devices will operate normally beyond the operating conditions and range.

## 4.1 Operating Conditions

### 4.1.1 Absolute Max. Ratings

**Table 4-1 Absolute Max. Ratings**

| Name | Description | Min. | Max. |
|---|---|---|---|
| $V_{CC}$ | Core voltage | -0.5V | 1.32V |
| $V_{CCIOx}$ | I/O Bank Power | -0.5V | 3.75V |
| $V_{CCX}$ | Auxiliary voltage | -0.5V | 3.75V |
| - | I/O Voltage Applied[1] | -0.5V | 3.75V |
| Storage Temperature | Storage Temperature | -65 ℃ | +150 ℃ |
| Junction Temperature | Junction Temperature | -40℃ | +125℃ |

**Note!**

[1] Overshoot and undershoot of -2V to ($V_{IHMAX}$ + 2)V are allowed for a duration of <20 ns.

### 4.1.2 Recommended Operating Conditions

**Table 4-2 Recommended Operating Conditions**

| Name | Description | Min. | Max. |
|---|---|---|---|
| $V_{CC}$ | Core voltage | 1.14V | 1.26V |
| $V_{CCX}$ | Auxiliary voltage | 1.71V | 3.6V |
| $V_{CCIOx}$ | I/O Bank Power | 1.14V | 3.6V |
| $T_{JCOM}$ | Junction temperature Commercial operation | 0 ℃ | +85 ℃ |
| $T_{JIND}$ | Junction temperature Industrial operation | -40 ℃ | +100 ℃ |

**Note!**

For the power supply information for different packages, please refer to UG883, *GW1NSER-4C Pinout*.

### 4.1.3 Power Supply Ramp Rates

**Table 4-3 Power Supply Ramp Rates**

| Name | Description | Min. | Typ. | Max. |
|---|---|---|---|---|
| $V_{CC}$ Ramp | Power supply ramp rates for $V_{CC}$ | 0.6mV/μs | - | 6mV/μs |
| $V_{CCX}$ Ramp | Power supply ramp rates for $V_{CCX}$ | 0.6mV/μs | - | 10mV/μs |
| $V_{CCIO}$ Ramp | Power supply ramp rates for $V_{CCIO}$ | 0.1mV/μs | - | 10mV/μs |

**Note!**

- A monotonic ramp is required for all power supplies.
- All power supplies need to be in the operating range as defined in Table 4 2 before configuration. Power supplies that are not in the operating range need to be adjusted to a faster ramp rate, or you have to delay configuration.

### 4.1.4 Hot Socket Specifications

**Table 4-4 Hot Socket Specifications**

| Name | Description | Condition | Max. |
|---|---|---|---|
| $I_{HS}$ | Input or I/O leakage current | $V_{IN}=V_{IL}$ (MAX) | TBD |

### 4.1.5 POR Specification

**Table 4-5 POR Voltage**

| Name | Description | Min. | Max. |
|---|---|---|---|
| POR Voltage | Power on reset voltage of Vcc | TBD | TBD |

## 4.2 ESD

**Table 4-6 GW1NSER ESD - HBM**

| Device | QN48 |
|---|---|
| GW1NSER-4C | HBM>1,000V |

**Table 4-7 GW1NSER ESD – CDM**

| Device | QN48 |
|---|---|
| GW1NSER-4C | CDM>500V |

## 4.3 DC Electrical Characteristics

### 4.3.1 DC Electrical Characteristics over Recommended Operating Conditions

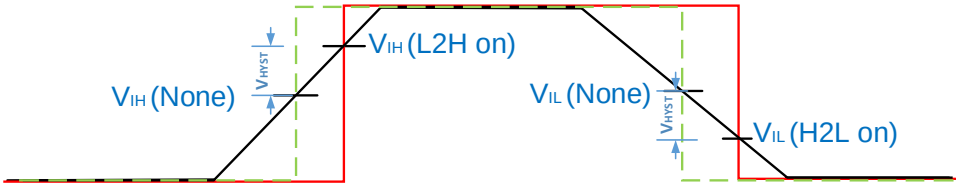
**Table 4-8 DC Electrical Characteristics over Recommended Operating Conditions**

| Name | Description | Condition | Min. | Typ. | Max. |
|---|---|---|---|---|---|
| $I_{IL}$,$I_{IH}$ | Input or I/O leakage | $V_{CCIO}<V_{IN}<V_{IH}$ (MAX) | - | - | 210μA |
| | | $0V<V_{IN}<V_{CCIO}$ | - | - | 10μA |
| $I_{PU}$ | I/O Active Pull-up Current | $0<V_{IN}<0.7V_{CCIO}$ | -30 μA | - | -150 μA |
| $I_{PD}$ | I/O Active Pull-down Current | $V_{IL}$ (MAX)$<V_{IN}<V_{CCIO}$ | 30μA | - | 150μA |
| $I_{BHLS}$ | Bus Hold Low Sustaining Current | $V_{IN}=V_{IL}$ (MAX) | 30μA | - | - |
| $I_{BHHO}$ | Bus Hold High Sustaining Current | $V_{IN}=0.7V_{CCIO}$ | -30 μA | - | - |
| $I_{BHLO}$ | Bud Hold Low Overdrive Current | $0\le V_{IN}\le V_{CCIO}$ | - | - | 150μA |
| $I_{BHHO}$ | Bus Hold High Overdrive Current | $0\le V_{IN}\le V_{CCIO}$ | - | - | -150 μA |
| $V_{BHT}$ | Bus hold trip points | | $V_{IL}$ (MAX) | - | $V_{IH}$ (MIN) |
| C1 | I/O Capacitance | | | 5pF | 8pF |
| $V_{HYST}$ | Hysteresis for Schmitt Trigger inputs | $V_{CCIO}$=3.3V, Hysteresis=L2H[1] | - | 200mV | - |
| | | $V_{CCIO}$=2.5V, Hysteresis= L2H | - | 125mV | - |
| | | $V_{CCIO}$=1.8V, Hysteresis= L2H | - | 60mV | - |

| Name | Description | Condition | Min. | Typ. | Max. |
|---|---|---|---|---|---|
| | | $V_{CCIO}$=1.5V, Hysteresis= L2H | - | 40mV | - |
| | | $V_{CCIO}$=1.2V, Hysteresis= L2H | - | 20mV | - |
| | | $V_{CCIO}$=3.3V, Hysteresis= H2L[1] | - | 200mV | - |
| | | $V_{CCIO}$=2.5V, Hysteresis= H2L | - | 125mV | - |
| | | $V_{CCIO}$=1.8V, Hysteresis= H2L | - | 60mV | - |
| | | $V_{CCIO}$=1.5V, Hysteresis= H2L | - | 40mV | - |
| | | $V_{CCIO}$=1.2V, Hysteresis= H2L | - | 20mV | - |
| | | $V_{CCIO}$=3.3V, Hysteresis= HIGH | - | 400mV | - |
| | | $V_{CCIO}$=2.5V, Hysteresis= HIGH | - | 250mV | - |
| | | $V_{CCIO}$=1.8V, Hysteresis= HIGH | - | 120mV | - |
| | | $V_{CCIO}$=1.5V, Hysteresis= HIGH | - | 80mV | - |
| | | $V_{CCIO}$=1.2V, Hysteresis= HIGH | - | 40mV | - |

**Note!**

- [1] Hysteresis="NONE", "L2H", "H2L", "HIGH" indicates the Hysteresis options that can be set when setting I/O Constraints in the FloorPlanner tool of Gowin EDA, for more details, see *SUG935, Gowin Design Physical Constraints User Guide*.
- [2] Enabling the L2H (low to high) option means raising $V_{IH}$ by $V_{HYST}$; enabling the H2L (high to low) option means lowering $V_{IL}$ by $V_{HYST}$; enabling the HIGH option means enabling both L2H and H2L options, i.e. $V_{HYST}$(HIGH) = $V_{HYST}$(L2H) + $V_{HYST}$(L2H). The diagram is shown below.



## 4.3.2 Static Supply Current

**Table 4-9 Static Supply Current**

| Name | Description | LX/UX | Device | Min. | Typ. | Max. |
|---|---|---|---|---|---|---|
| $I_{CC}$ | Core current under load | LV | GW1NSER-4C | TBD | TBD | TBD |
| $I_{CCX}$ | Core current under load | LV | GW1NSER-4C | TBD | TBD | TBD |
| $I_{CCIO}$ | I/O Bank current under load | LV | GW1NSER-4C | TBD | TBD | TBD |

## 4.3.3 Recommended I/O Operating Conditions

**Table 4-10 Recommended I/O Operating Conditions**

| Name | Output $V_{CCIO}$ (V) | | | Input $V_{REF}$ (V) | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| LVTTL33 | 3.135 | 3.3 | 3.465 | - | - | - |
| LVCMOS33 | 3.135 | 3.3 | 3.465 | - | - | - |
| LVCMOS25 | 2.375 | 2.5 | 2.625 | - | - | - |
| LVCMOS18 | 1.71 | 1.8 | 1.89 | - | - | - |
| LVCMOS15 | 1.425 | 1.5 | 1.575 | - | - | - |
| LVCMOS12 | 1.14 | 1.2 | 1.26 | - | - | - |
| SSTL15 | 1.425 | 1.5 | 1.575 | 0.68 | 0.75 | 0.9 |
| SSTL18_I | 1.71 | 1.8 | 1.89 | 0.833 | 0.9 | 0.969 |
| SSTL18_II | 1.71 | 1.8 | 1.89 | 0.833 | 0.9 | 0.969 |
| SSTL25_I | 2.375 | 2.5 | 2.645 | 1.15 | 1.25 | 1.35 |
| SSTL25_II | 2.375 | 2.5 | 2.645 | 1.15 | 1.25 | 1.35 |
| SSTL33_I | 3.135 | 3.3 | 3.465 | 1.3 | 1.5 | 1.7 |
| SSTL33_II | 3.135 | 3.3 | 3.465 | 1.3 | 1.5 | 1.7 |
| HSTL18_I | 1.71 | 1.8 | 1.89 | 0.816 | 0.9 | 1.08 |
| HSTL18_II | 1.71 | 1.8 | 1.89 | 0.816 | 0.9 | 1.08 |
| HSTL15 | 1.425 | 1.5 | 1.575 | 0.68 | 0.75 | 0.9 |
| PCI33 | 3.135 | 3.3 | 3.465 | - | - | - |
| LVPECL33E | 3.135 | 3.3 | 3.465 | - | - | - |
| MLVDS25E | 2.375 | 2.5 | 2.625 | - | - | - |
| BLVDS25E | 2.375 | 2.5 | 2.625 | - | - | - |
| RSDS25E | 2.375 | 2.5 | 2.625 | - | - | - |
| LVDS25E | 2.375 | 2.5 | 2.625 | - | - | - |
| SSTL15D | 1.425 | 1.5 | 1.575 | - | - | - |
| SSTL18D_I | 1.71 | 1.8 | 1.89 | - | - | - |
| SSTL18D_II | 1.71 | 1.8 | 1.89 | - | - | - |
| SSTL25D_I | 2.375 | 2.5 | 2.625 | - | - | - |
| SSTL25D_II | 2.375 | 2.5 | 2.625 | - | - | - |

| Name | Output $V_{CCIO}$ (V) | | | Input $V_{REF}$ (V) | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| SSTL33D_I | 3.135 | 3.3 | 3.465 | - | - | - |
| SSTL33D_II | 3.135 | 3.3 | 3.465 | - | - | - |
| HSTL15D | 1.425 | 1.575 | 1.89 | - | - | - |
| HSTL18D_I | 1.71 | 1.8 | 1.89 | - | - | - |
| HSTL18D_II | 1.71 | 1.8 | 1.89 | - | - | - |

## 4.3.4 IOB Single - Ended DC Electrical Characteristic

**Table 4-11 IOB Single - Ended DC Electrical Characteristic**

| Name | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ (Max) | $V_{OH}$ (Min) | $I_{OL}$ (mA) | $I_{OH}$ (mA) |
|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | | | | |
| LVCMOS33 LVTTL33 | -0.3V | 0.8V | 2.0V | 3.6V | 0.4V | $V_{CCIO}$-0.4V | 4 | -4 |
| | | | | | | | 8 | -8 |
| | | | | | | | 12 | -12 |
| | | | | | | | 16 | -16 |
| | | | | | | | 24 | -24 |
| | | | | | 0.2V | $V_{CCIO}$-0.2V | 0.1 | -0.1 |
| LVCMOS25 | -0.3V | 0.7V | 1.7V | 3.6V | 0.4V | $V_{CCIO}$-0.4V | 4 | -4 |
| | | | | | | | 8 | -8 |
| | | | | | | | 12 | -12 |
| | | | | | | | 16 | -16 |
| | | | | | 0.2V | $V_{CCIO}$-0.2V | 0.1 | -0.1 |
| LVCMOS18 | -0.3V | 0.35 x $V_{CCIO}$ | 0.65 x $V_{CCIO}$ | 3.6V | 0.4V | $V_{CCIO}$0.4V | 4 | -4 |
| | | | | | | | 8 | -8 |
| | | | | | | | 12 | -12 |
| | | | | | 0.2V | $V_{CCIO}$-0.2V | 0.1 | -0.1 |
| LVCMOS15 | -0.3V | 0.35 x $V_{CCIO}$ | 0.65 x $V_{CCIO}$ | 3.6V | 0.4V | $V_{CCIO}$-0.4V | 4 | -4 |
| | | | | | | | 8 | -8 |
| | | | | | 0.2V | $V_{CCIO}$-0.2V | 0.1 | -0.1 |
| LVCMOS12 | -0.3V | 0.35 x $V_{CCIO}$ | 0.65 x $V_{CCIO}$ | 3.6V | 0.4V | $V_{CCIO}$-0.4V | 2 | -2 |
| | | | | | | | 6 | -6 |
| | | | | | 0.2V | $V_{CCIO}$-0.2V | 0.1 | -0.1 |
| PCI33 | -0.3V | 0.3 x $V_{CCIO}$ | 0.5 x $V_{CCIO}$ | 3.6V | 0.1x $V_{CCIO}$ | 0.9 x $V_{CCIO}$ | 1.5 | -0.5 |
| SSTL33_I | -0.3V | $V_{REF}$-0.2V | $V_{REF}$+0.2V | 3.6V | 0.7 | $V_{CCIO}$-1.1V | 8 | -8 |
| SSTL25_I | -0.3V | $V_{REF}$-0.18V | $V_{REF}$+0.18V | 3.6V | 0.54V | $V_{CCIO}$-0.62V | 8 | -8 |
| SSTL25_II | -0.3V | $V_{REF}$-0.18V | $V_{REF}$+0.18V | 3.6V | NA | NA | NA | NA |
| SSTL18_II | -0.3V | $V_{REF}$-0.125V | $V_{REF}$+0.125V | 3.6V | NA | NA | NA | NA |
| SSTL18_I | -0.3V | $V_{REF}$-0.125V | $V_{REF}$+0.125V | 3.6V | 0.40V | $V_{CCIO}$-0.40V | 8 | -8 |

| Name | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ (Max) | $V_{OH}$ (Min) | $I_{OL}$ (mA) | $I_{OH}$ (mA) |
|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | | | | |
| SSTL15 | -0.3V | $V_{REF}$-0.1V | $V_{REF}$+ 0.1V | 3.6V | 0.40V | $V_{CCIO}$-0.40V | 8 | -8 |
| HSTL18_I | -0.3V | $V_{REF}$-0.1V | $V_{REF}$+ 0.1V | 3.6V | 0.40V | $V_{CCIO}$-0.40V | 8 | -8 |
| HSTL18_II | -0.3V | $V_{REF}$-0.1V | $V_{REF}$+ 0.1V | 3.6V | NA | NA | NA | NA |
| HSTL15_I | -0.3V | $V_{REF}$-0.1V | $V_{REF}$+ 0.1V | 3.6V | 0.40V | $V_{CCIO}$-0.40V | 8 | -8 |
| HSTL15_II | -0.3V | $V_{REF}$-0.1V | $V_{REF}$+ 0.1V | 3.6V | NA | NA | NA | NA |

**Note!**

[1] The total DC current limit (sourced and sinked) of all IOs in the same bank: the total DC current of all IOs in the same bank shall not be greater than n*8mA, where n represents the number of IOs bonded out from a bank.

### 4.3.5 I/O Differential Electrical Characteristics

**Table 4-12 I/O Differential Electrical Characteristics**

LVDS25

| Name | Description | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{INA}$,$V_{INB}$ | Input Voltage (Input Voltage) | | 0 | - | 2.4 | V |
| $V_{CM}$ | Input Common Mode Voltage (Input Common Mode Voltage) | Half the Sum of the Two Inputs | 0.05 | - | 2.35 | V |
| $V_{THD}$ | Differential Input Threshold | Difference Between the Two Inputs | ±100 | - | ±600 | mV |
| $I_{IN}$ | Input Current | Power On or Power Off | - | - | ± 10 | μA |
| $V_{OH}$ | Output High Voltage for $V_{OP}$ or $V_{OM}$ | $R_T$ = 100Ω | - | - | 1.60 | V |
| $V_{OL}$ | Output Low Voltage for $V_{OP}$ or $V_{OM}$ | $R_T$ = 100Ω | 0.9 | - | - | V |
| $V_{OD}$ | Output Voltage Differential | ($V_{OP}$ - $V_{OM}$), $R_T$ = 100Ω | 250 | 350 | 450 | mV |
| $\Delta V_{OD}$ | Change in $V_{OD}$ Between High and Low | | - | - | 50 | mV |
| $V_{OS}$ | Output Voltage Offset | ($V_{OP}$ + $V_{OM}$)/2, $R_T$ = 100Ω | 1.125 | 1.20 | 1.375 | V |
| $\Delta V_{OS}$ | Change in $V_{OS}$ Between High and Low | | - | - | 50 | mV |
| $I_S$ | Short-circuit current | $V_{OD}$ = 0V output short-circuit | - | - | 15 | mA |

## 4.4 Switching Characteristic

### 4.4.1 I/O Speed

**Table 4-13 IO Parameters**

| Name | Description | Min | Max | Unit |
|---|---|---|---|---|
| $f_{MAX}$ | IO Max. Frequency | - | 150M | Hz |
| $f_{MAX\_LVDS}$ | LVDS Max. Frequency | - | 400M | Hz |

### 4.4.2 CLU Block Internal Timing Parameters

**Table 4-14 CLU Block Internal Timing Parameters**

| Name | Description | Speed Grade | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $t_{LUT4\_CLU}$ | LUT4 delay | - | 0.674 | ns |
| $t_{LUT5\_CLU}$ | LUT5 delay | - | 1.388 | ns |
| $t_{LUT6\_CLU}$ | LUT6 delay | - | 2.01 | ns |
| $t_{LUT7\_CLU}$ | LUT7 delay | - | 2.632 | ns |
| $t_{LUT8\_CLU}$ | LUT8 delay | - | 3.254 | ns |
| $t_{SR\_CLU}$ | Set/Reset to Register output | - | 1.86 | ns |
| $t_{CO\_CLU}$ | Clock to Register output | - | 0.76 | ns |

## 4.4.3 Clock and I/O Switching Characteristics

**Table 4-15 LUT External Switching Characteristics**

| Name | Description | Device | -5 | | -6 | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| Clocks | TBD | TBD | TBD | TBD | TBD | TBD | |
| Pin-LUT-Pin Delay | TBD | TBD | TBD | TBD | TBD | TBD | |
| General I/O Pin Parameters | TBD | TBD | TBD | TBD | TBD | TBD | |

## 4.4.4 Gearbox Internal Timing Parameters

**Table 4-16 GearboxInternal Timing Parameters**

| Name | Description | Typ. | Unit |
|---|---|---|---|
| FMAXIDDR | 2:1 Gearbox maximum input frequency | 410 | MHz |
| $FMAX_{IDES4}$ | 4:1 Gearbox maximum input frequency | 410 | MHz |
| $FMAX_{IDES8}$ | 8:1 Gearbox maximum input frequency | 410 | MHz |
| $FMAX_{IVIDEO}$ | 7:1 Gearbox maximum input frequency | 390 | MHz |
| $FMAX_{IDES10}$ | 10:1 Gearbox maximum input frequency | 410 | MHz |
| $FMAX_{ODDR}$ | 1:2 Gearbox maximum input frequency | 355 | MHz |
| $FMAX_{OSER4}$ | 1:4 Gearbox maximum input frequency | 360 | MHz |
| $FMAX_{OSER8}$ | 1:8 Gearbox maximum input frequency | 355 | MHz |
| $FMAX_{OVIDEO}$ | 1:7 Gearbox maximum input frequency | 355 | MHz |
| $FMAX_{OSER10}$ | 1:10 Gearbox maximum input frequency | 355 | MHz |
| $FMAX_{OSER16}$ | 1:16Gearbox maximum input frequency | 750 | MHz |

## 4.4.5 BSRAM Internal Timing Parameters

**Table 4-17 BSRAM Internal Timing Parameters**

| Name | Description | Speed Grade | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $t_{COAD\_BSRAM}$ | Clock to output from read address/data | - | 5.10 | ns |
| $t_{COOR\_BSRAM}$ | Clock to output from output register | - | 0.56 | ns |

## 4.4.6 DSP Internal Timing Parameters

**Table 4-18 DSP Internal Timing Parameters**

| Name | Description | Speed Grade | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $t_{COIR\_DSP}$ | Clock to output from output register | - | 4.80 | ns |
| $t_{COPR\_DSP}$ | Clock to output from output register | - | 2.40 | ns |
| $t_{COOR\_DSP}$ | Clock to output from output register | - | 0.84 | ns |

### 4.4.7 On chip Oscillator Output Frequency

**Table 4-19 On chip Oscillator Output Frequency**

| Name | Description | | Min. | Typ. | Max. |
|---|---|---|---|---|---|
| $f_{MAX}$ | On chip Oscillator Output Frequency (0 ~ +85℃) | GW1NSER-4C/4C | 118.75MHz | 125MHz | 131.25MHz |
| | On chip Oscillator Output Frequency (-40 ~ +100℃) | GW1NSER-4C/4C | 112.5MHz | 125MHz | 137.5MHz |
| $t_{DT}$ | Clock Duty Cycle | | 43% | 50% | 57% |
| $t_{OPJIT}$ | Clock Period Jitter | | 0.01UIPP | 0.012UIPP | 0.02UIPP |

### 4.4.8 PLL Parameters

**Table 4-20 PLL Parameters**

| Device | Speed Level | Name | Min. | Max. |
|---|---|---|---|---|
| GW1NSER-4C | C7/I6<br>C6/I5 | CLKIN | 3MHZ | 400MHZ |
| | | PFD | 3MHZ | 400MHZ |
| | | VCO | 400MHZ | 1200MHZ |
| | | CLKOUT | 3.125MHZ | 600MHZ |
| | C5/I4 | CLKIN | 3MHZ | 320MHZ |
| | | PFD | 3MHZ | 320MHZ |
| | | VCO | 320MHZ | 960MHZ |
| | | CLKOUT | 2.5MHZ | 480MHZ |

## 4.5 Cortex-M3 Electrical Specification

### 4.5.1 DC Characteristic

**Table 4-21 Current Characteristic**

| Name | Description | Spec. | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $I_{VCC}$ | Max. current of VCC | - | 100 | mA |
| $I_{VSS}$ | Max. current of VSS | - | ⩾100 | mA |
| $I_{INJ}$ | Leakage current | - | +/-5 | mA |

### 4.5.2 AC Characteristic

**Table 4-22 Clock Parameters**

| Name | Description | Device | Spec. | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| $f_{HCLK}$ | AHB clockfrequency | GW1NSER-4C | 0 | 80 | MHz |
| $f_{PCLK}$ | APB clockfrequency | GW1NSER-4C | 0 | 80 | MHz |

# 4.6 User Flash Characteristic

## 4.6.1 DC Characteristics

**Table 4-23 User Flash DC Characteristic**

| Name | Param-eter | Max. | | Unit | Wake-up Time | Condition |
|---|---|---|---|---|---|---|
| | | $V_{CC}$[3] | $V_{CCX}$ | | | |
| Read mode (w/l 25ns)[1] | $I_{CC1}$[2] | 2.19 | 0.5 | mA | NA | Min. Clcok period, duty cycle 100%, VIN = “1/0” |
| Write mode | | 0.1 | 12 | mA | NA | - |
| Erase mode | | 0.1 | 12 | mA | NA | - |
| Page Erasure Mode | | 0.1 | 12 | mA | NA | - |
| Read mode static current (25-50ns) | $I_{CC2}$ | 980 | 25 | μA | NA | XE=YE=SE=“1”,between T=Tacc and T=50ns, I/O=0mA; later than T=50ns, read mode is turned off, and I/O current is the current of standby mode. |
| Standby mode | $I_{SB}$ | 5.2 | 20 | μA | 0 | $V_{SS}$, $V_{CCX}$, and $V_{CC}$ |

**Note!**

- [1] Means the average current, and the peak value is higher than the average one.
- [2] Calculated in different $T_{new}$ clock periods.
  - $T_{new} < T_{acc}$ is not allowed
  - $T_{new} = T_{acc}$
  - $T_{acc} < T_{new}$ - 50ns: $I_{CC1}$ (new) = ($I_{CC1}$ - $I_{CC2}$)($T_{acc}/T_{new}$) + $I_{CC2}$
  - $T_{new} > 50ns$: $I_{CC1}$ (new) = ($I_{CC1}$ - $I_{CC2}$)($T_{acc}/T_{new}$) + 50ns x $I_{CC2}/T_{new}$ + $I_{SB}$
  - t > 50ns, $I_{CC2} = I_{SB}$
- [3] $V_{CC}$ must be greater than 1.08V from the zero wake-up time.

## 4.6.2 AC Characteristics

**Table 4-24 User Flash Timing Parameters**

| User Modes | Parameter | Name | Min. | Max. | Unit |
|---|---|---|---|---|---|
| Access time[2] | WC1 | $T_{acc}$[3] | - | 25 | ns |
| | TC | | - | 22 | ns |
| | BC | | - | 21 | ns |
| | LT | | - | 21 | ns |
| | WC | | - | 25 | ns |
| Program/Erase to data storage | | $T_{nvs}$ | 5 | - | μs |
| Data storage hold time | | $T_{nvh}$ | 5 | - | μs |
| Data storage hold time (Overall erase) | | $T_{nvh1}$ | 100 | - | μs |
| Time from data storage to program setup | | $T_{pgs}$ | 10 | - | μs |
| Program hold time | | $T_{pgh}$ | 20 | - | ns |
| Program time | | $T_{prog}$ | 8 | 16 | μs |
| Write ready time | | $T_{wpr}$ | >0 | - | ns |
| Erase hold time | | $T_{whd}$ | >0 | - | ns |
| Time from control signal to write/Erase setup | | $T_{cps}$ | -10 | - | ns |
| Time from SE to read setup | | $T_{as}$ | 0.1 | - | ns |
| E pulse high level time | | $T_{pws}$ | 5 | - | ns |
| Adress/data setup time | | $T_{ads}$ | 20 | - | ns |
| Adress/data hold time | | $T_{adh}$ | 20 | - | ns |
| Data hold-up time | | $T_{dh}$ | 0.5 | - | ns |
| Read mode address hold time[3] | WC1 | $T_{ah}$ | 25 | - | ns |
| | TC | | 22 | - | ns |
| | BC | | 21 | - | ns |
| | LT | | 21 | - | ns |
| | WC | | 25 | - | ns |
| SE pulse low level time | | $T_{nws}$ | 2 | - | ns |
| Recovery time | | $T_{rcv}$ | 10 | - | μs |
| Data storage time | | $T_{hv}$[4] | - | 6 | ms |
| Erasure time | | $T_{erase}$ | 100 | 120 | ms |
| Overall erase time | | $T_{me}$ | 100 | 120 | ms |
| Wake-up time from power down to standby mode | | $T_{wk\_pd}$ | 7 | - | μs |
| Standby hold time | | $T_{sbh}$ | 100 | - | ns |
| $V_{CC}$ setup time | | $T_{ps}$ | 0 | - | ns |
| $V_{CCX}$ hold time | | $T_{ph}$ | 0 | - | ns |

**Note!**

- [1] The parameter values may change;

- [2] The values are simulation data only.
- [3]After XADR, YADR, XE, and YE are valid, $T_{acc}$ start time is SE rising edge. DOUT is kept until the next valid read operation;
- [4]$T_{hv}$ is the time between write and the next erasure.The same address can not be written twice before erasure, so does the same register. This limitation is for safety;
- [5]Both the rising edge time and falling edge time for all waveform is 1ns;
- [6] TX, YADR, XE, and YE hold time need to be $T_{acc}$ at leaset, and $T_{acc}$ start from SE rising edge.

## 4.6.3 Operation Timing Diagrams

**Figure 4-1 User Flash Read Operation**

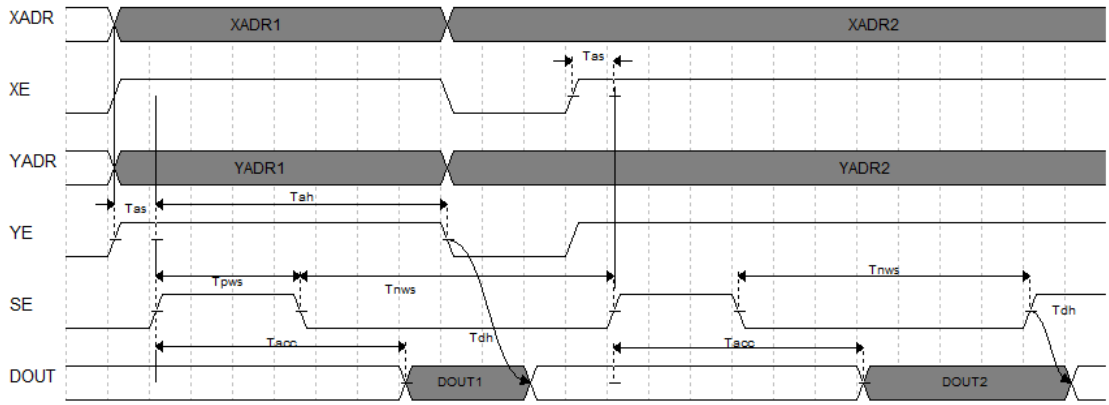



**Figure 4-2 User Flash Program Operation**

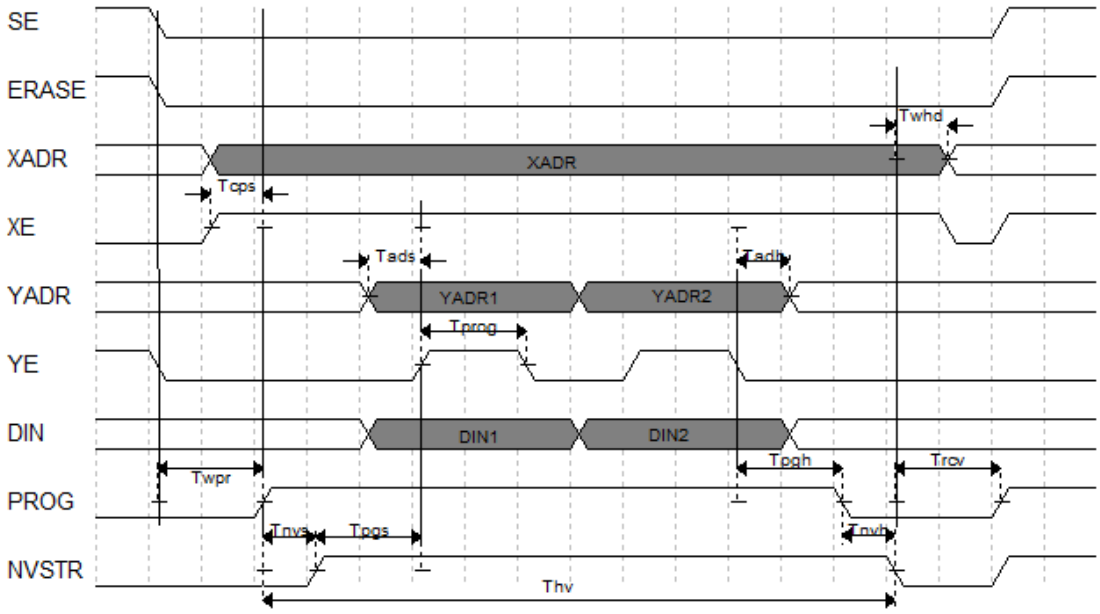
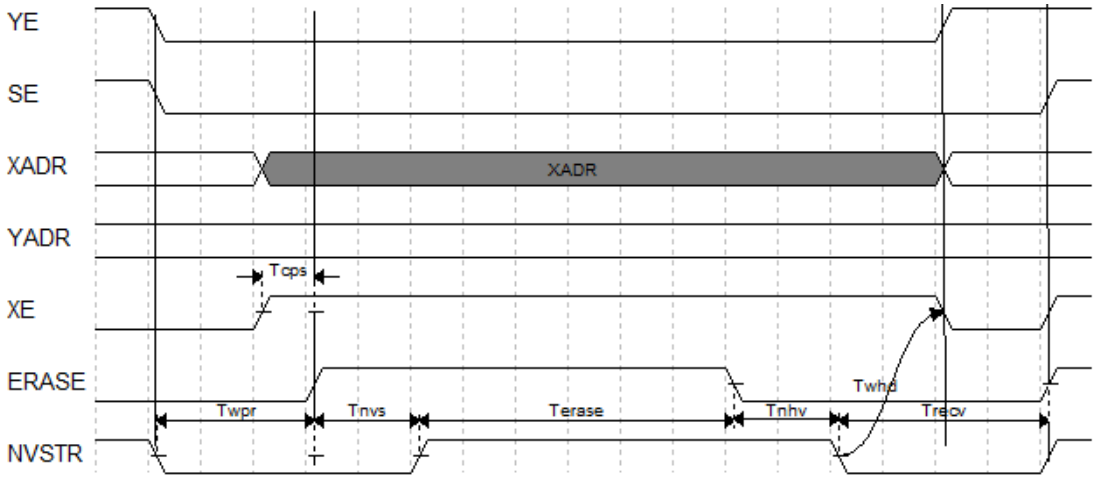


**Figure 4-3 User Flash Erase Operation**




# 4.7 Configuration Interface Timing Specification

The GW1NSER series of SecureFPGA products GowinCONFIG support six configuration modes: AUTO BOOT, SSPI, MSPI, DUAL BOOT, SERIAL, and CPU. For detailed information, please refer to UG290, *Gowin FPGA Products Programming and Configuration* User Guide.

# 5 Ordering Information

## 5.1 Part Naming

**Note!**

- For further information about package type and pin number, please refer to 2.2 Product Resources and 2.3 Package Information.
- The LittleBee® family devices and Arora family devices of the same speed level have different speed.
- Both “C” and “I” are used in GOWIN part name marking for one same device. GOWIN devices are screened using industrial standards, so one device can be used for both industrial (I) and commercial (C) applications. The maximum temperature of the industrial grade is 100℃, and the maximum temperature of the commercial grade is 85℃. Therefore, if the chip meets the speed level 6 in commercial grade applications, the speed level is 5 in industrial grade applications.

**Figure 5-1 Part Naming – ES**

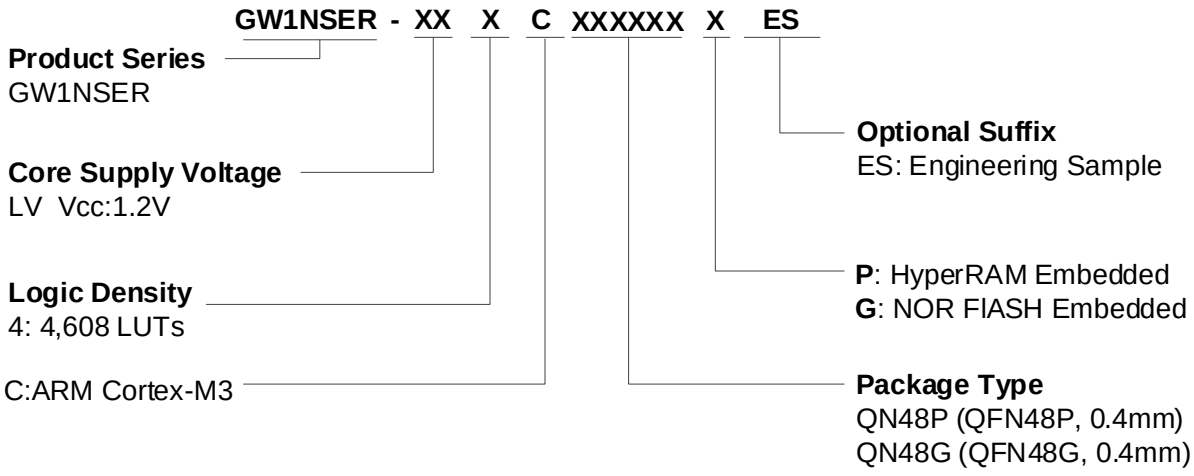
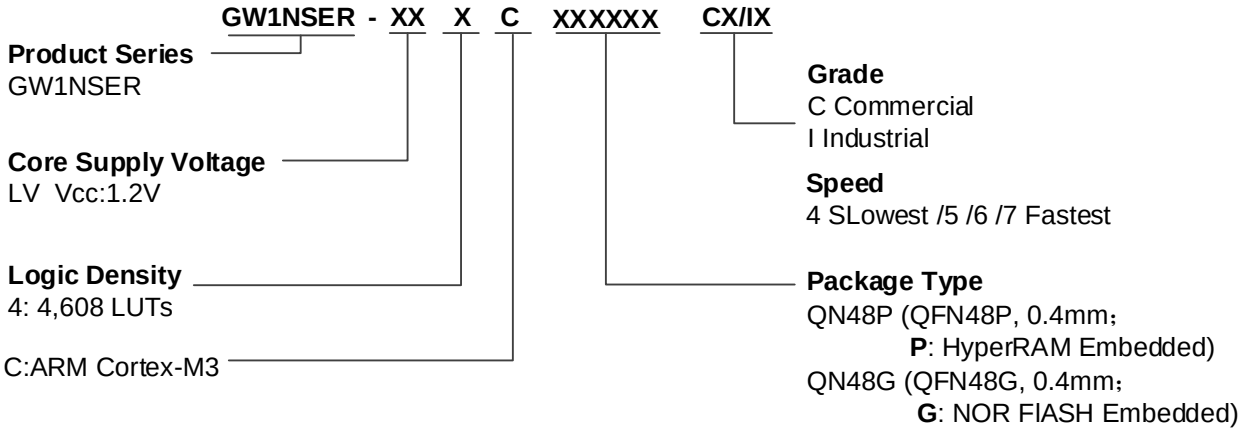


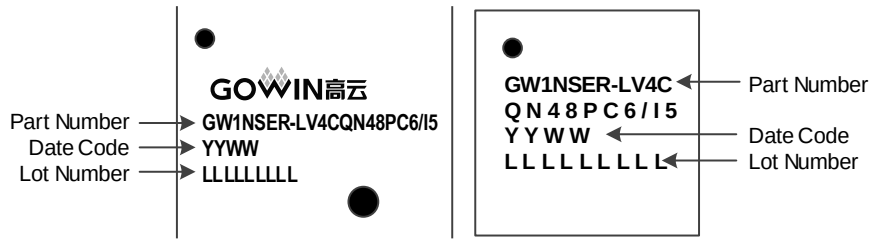
**Figure 5-2 Part Naming–Production**




# 5.2 Package Mark

The device information of GOWINSEMI is marked on the chip surface, as shown in Figure 5-3.

**Figure 5-3 GW1NSER-4C Package Mark**




**Note!**

The first two lines in the Figure above are the "Part Number".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