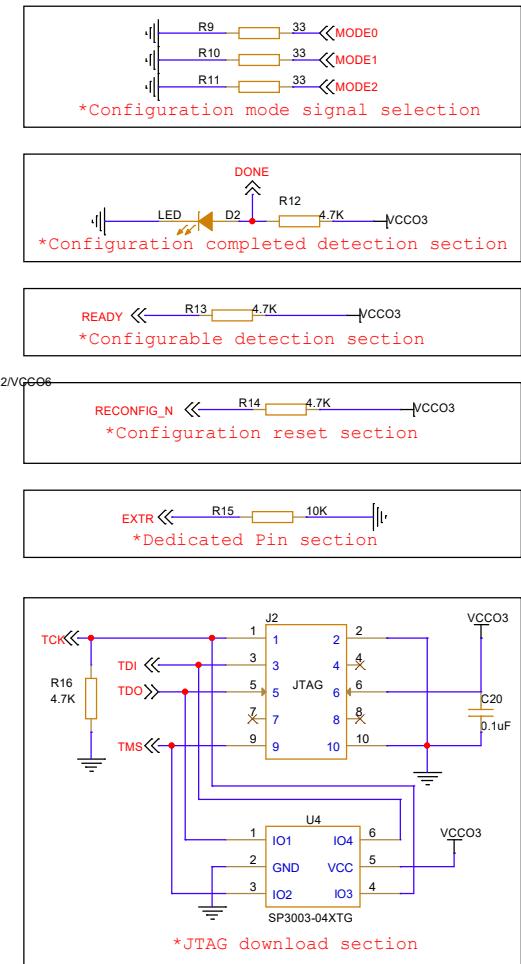
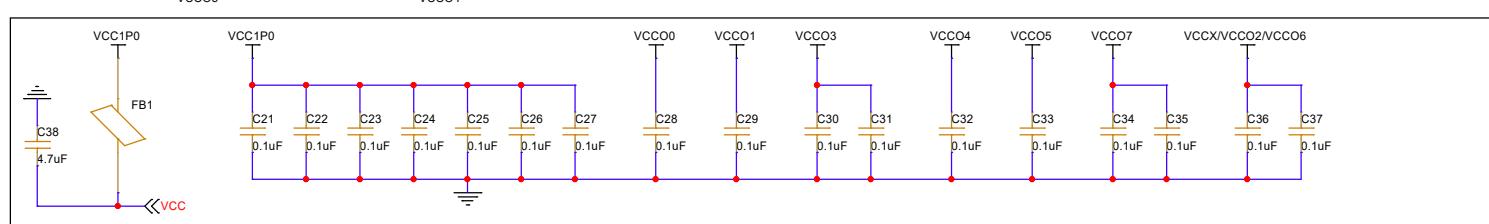
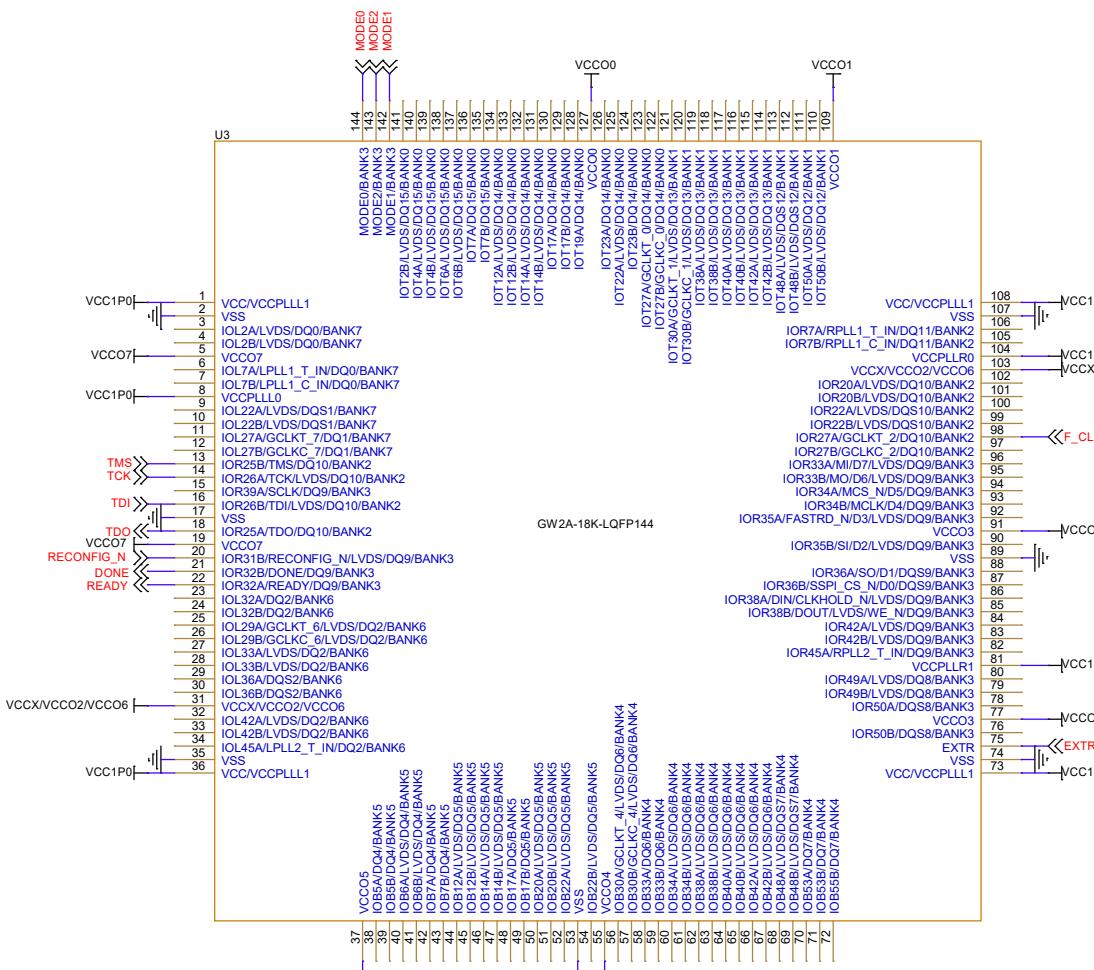
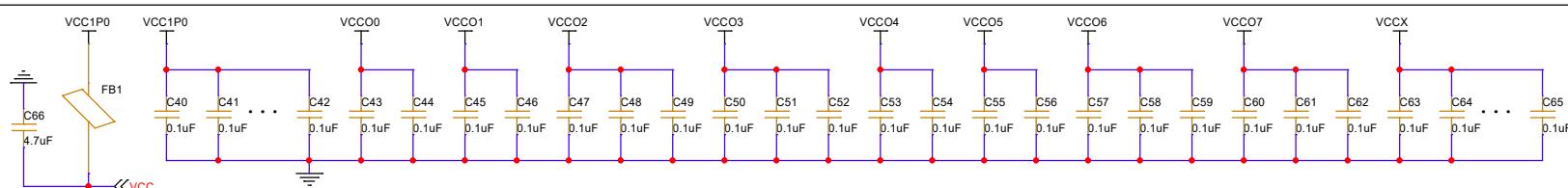
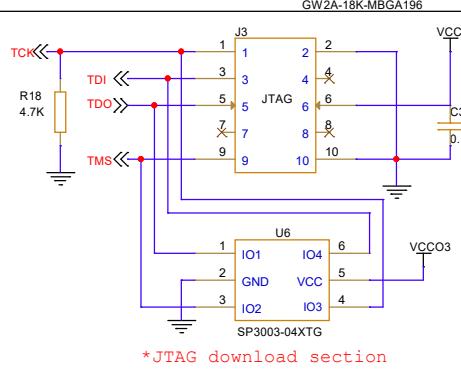
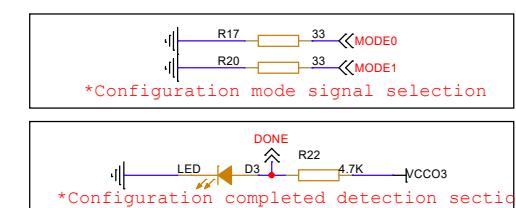
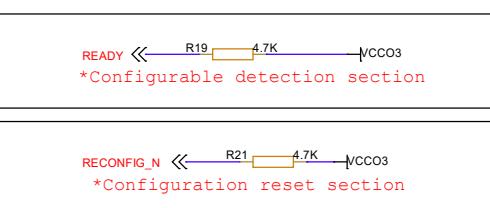
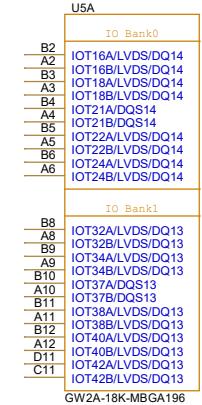
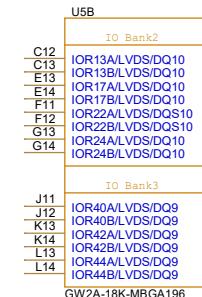
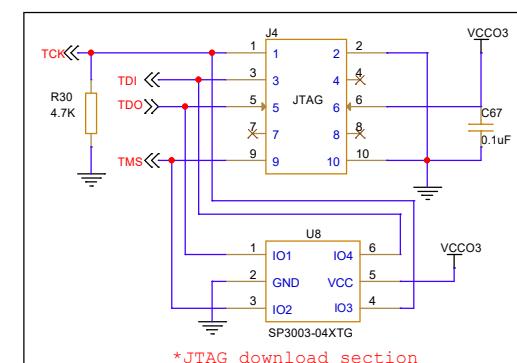
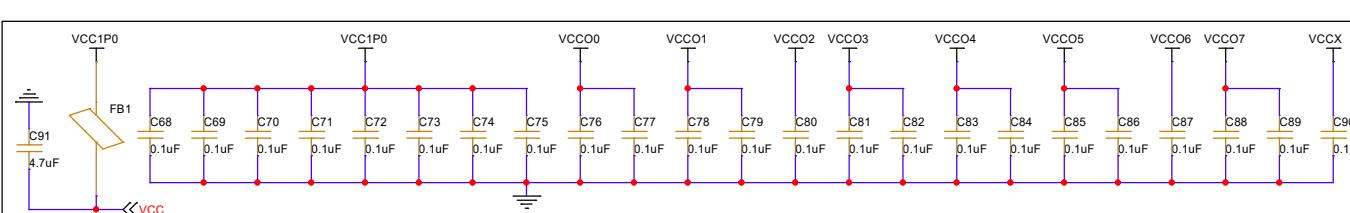
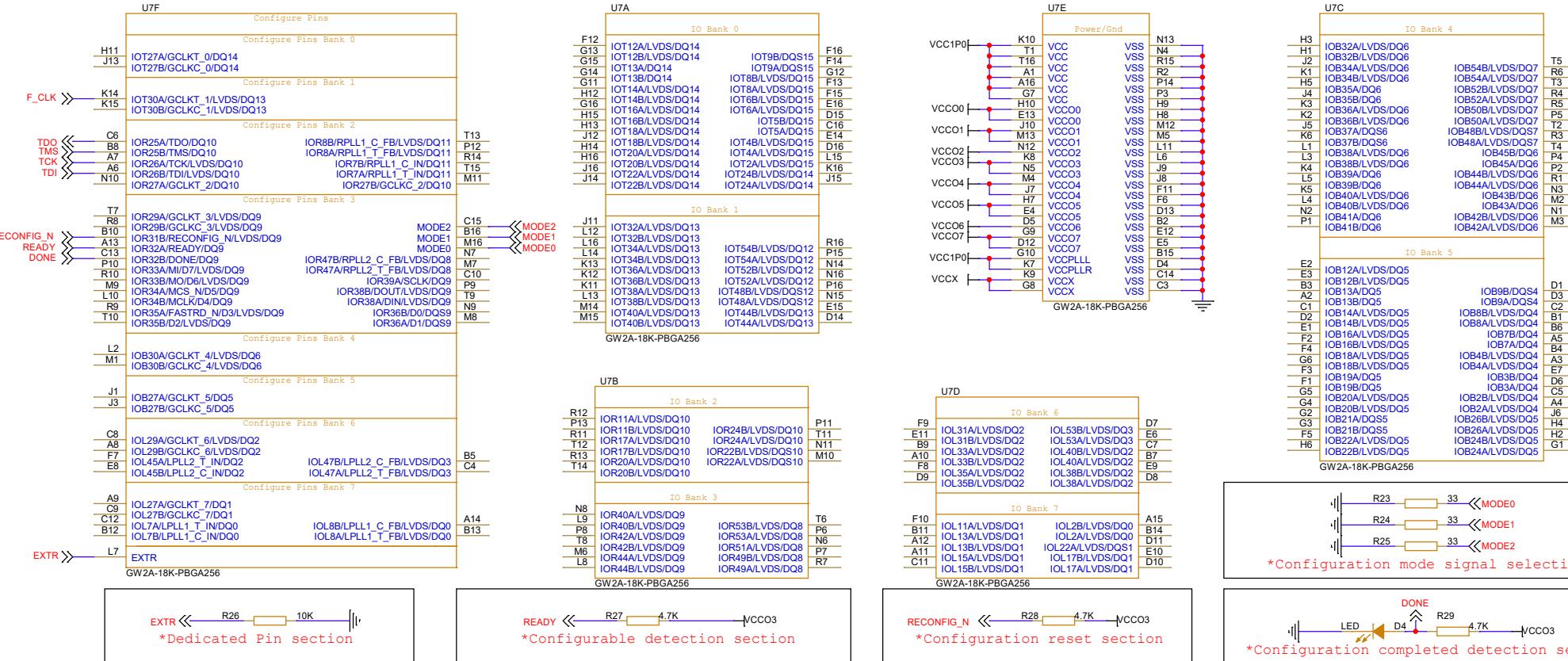


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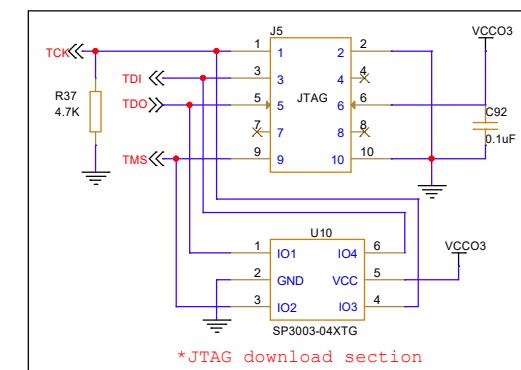
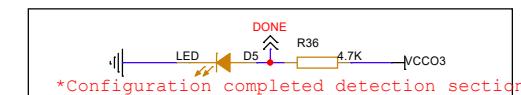
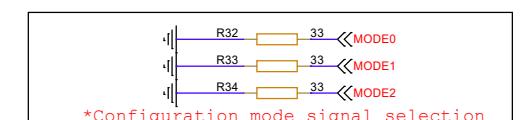
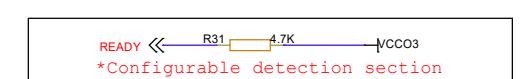
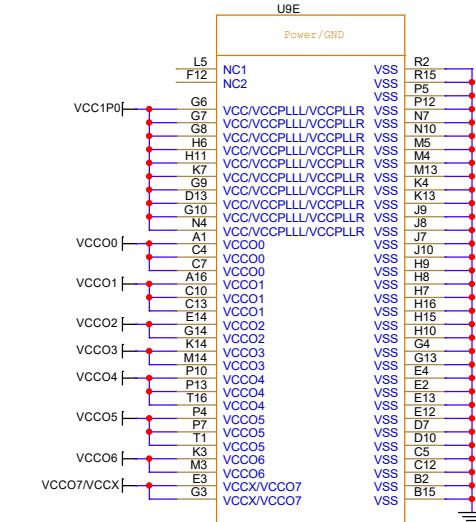
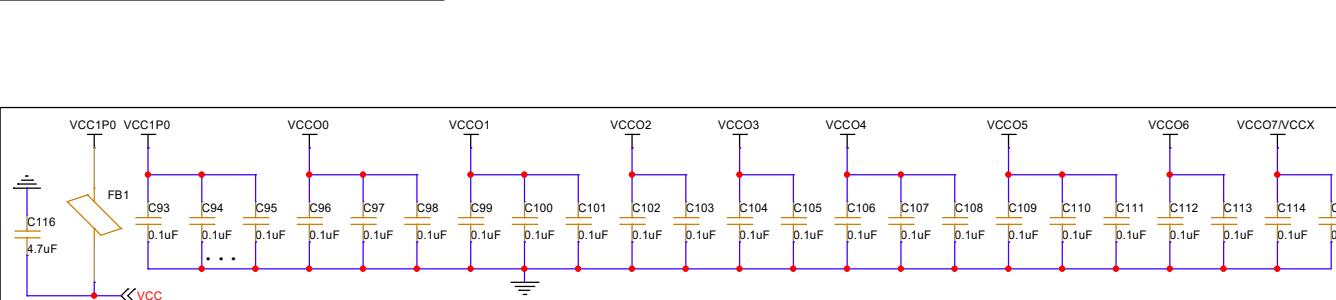
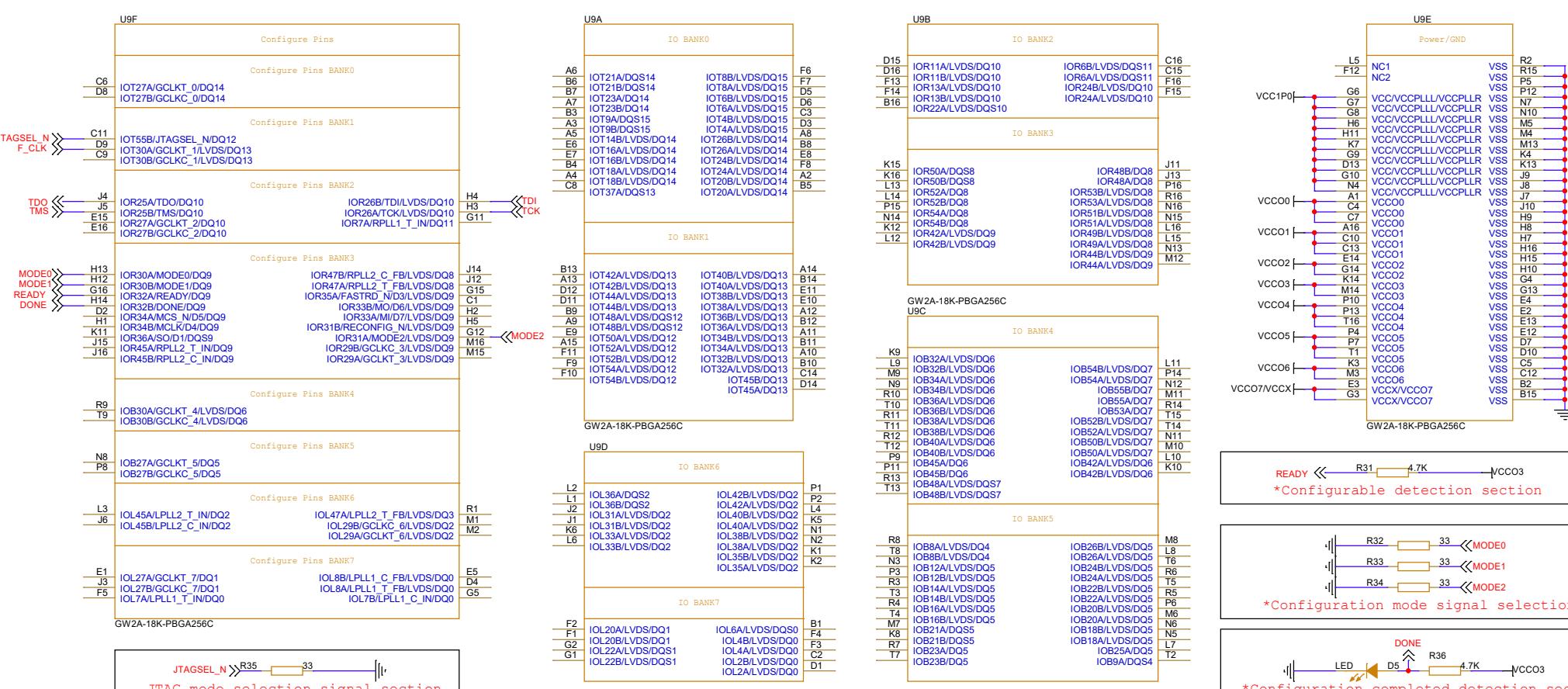
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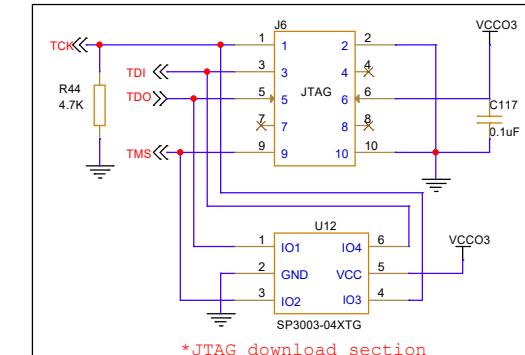
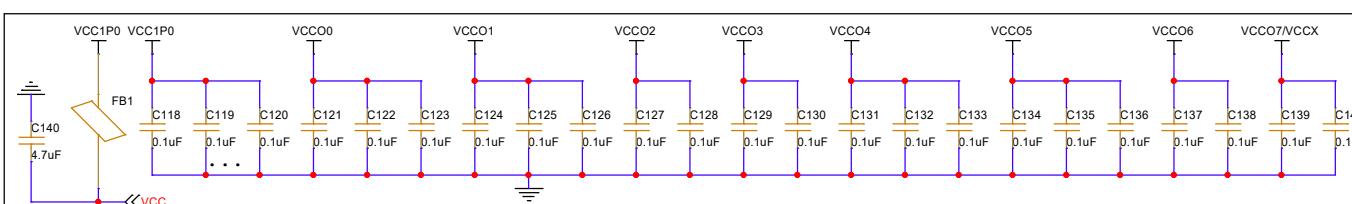
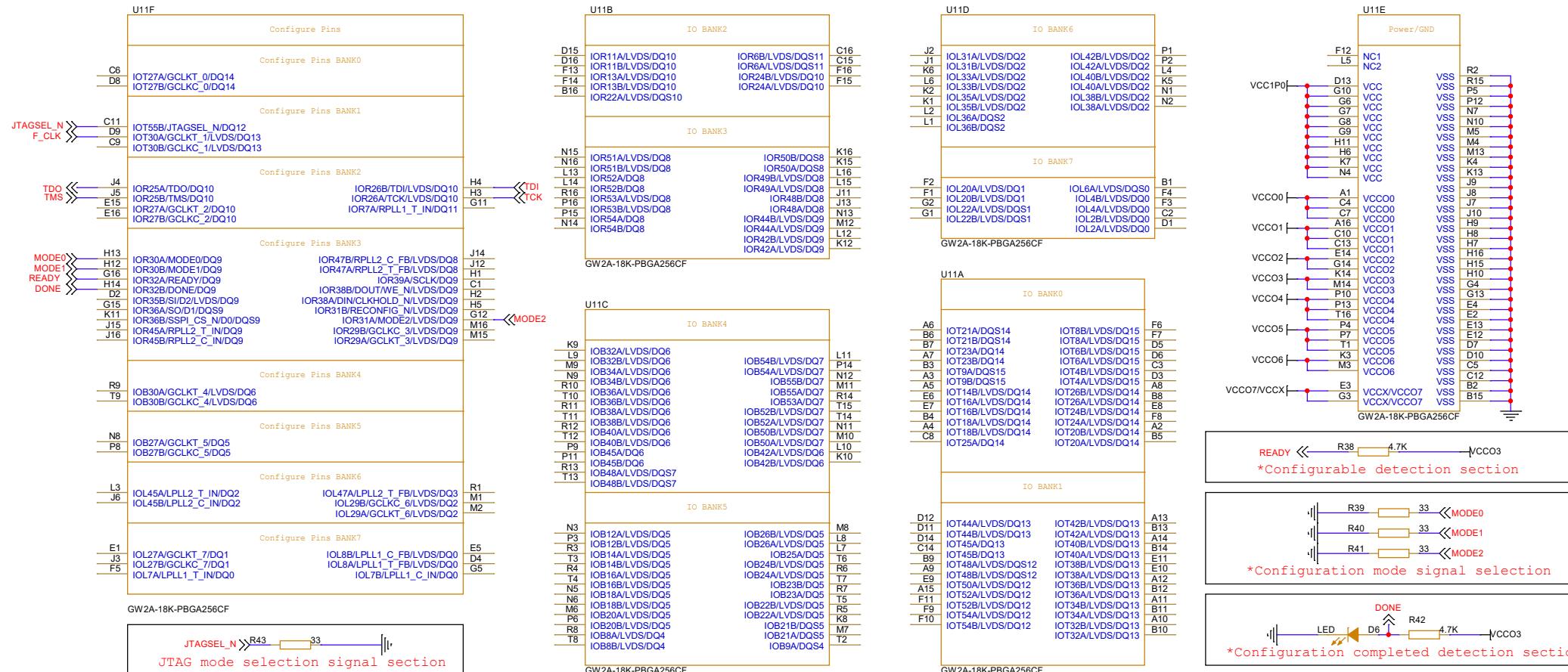
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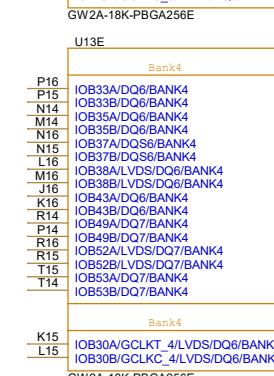
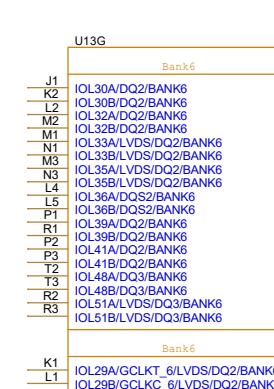
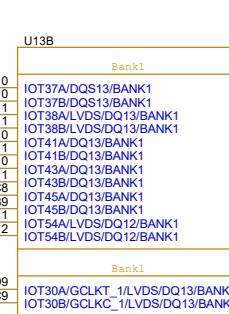
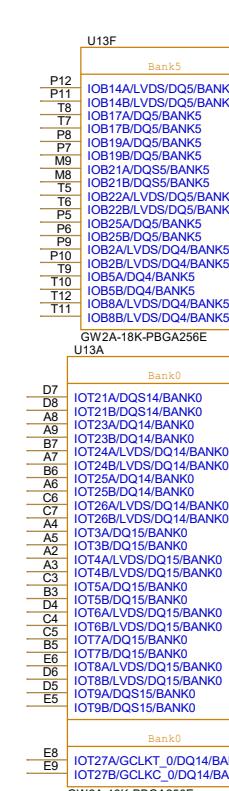
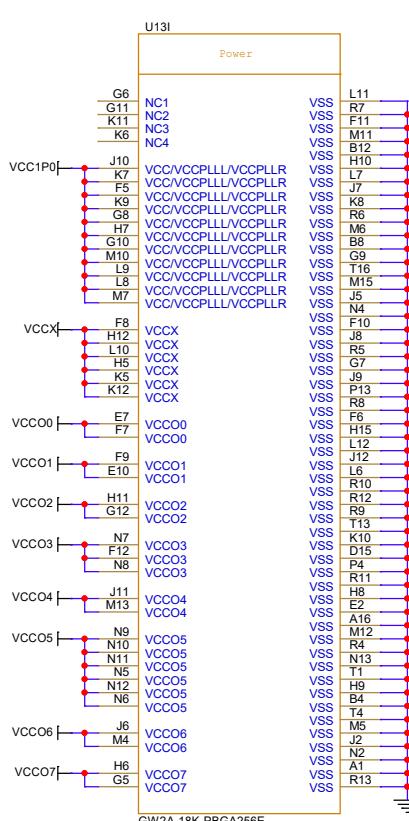
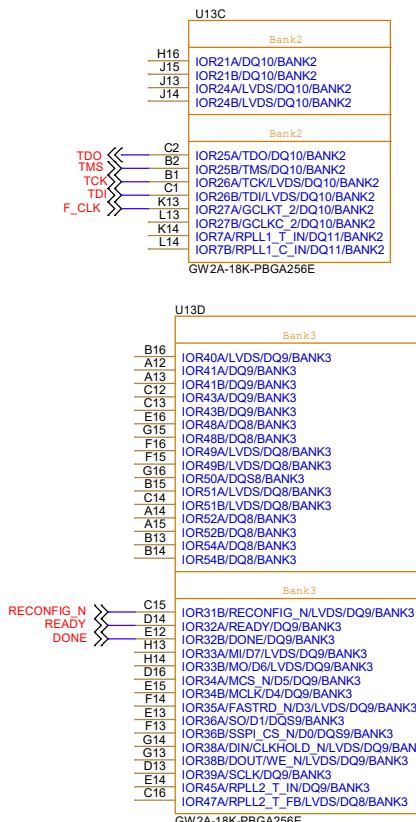


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**GW2A-LV18-PBGA256CF**

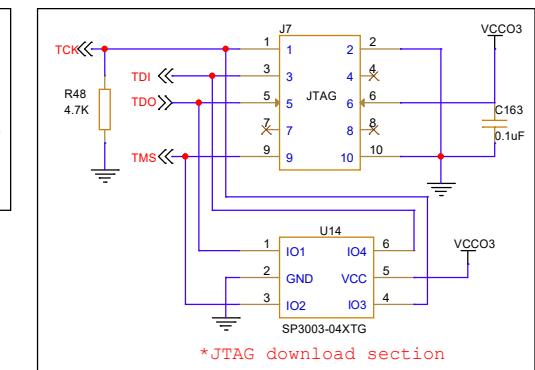
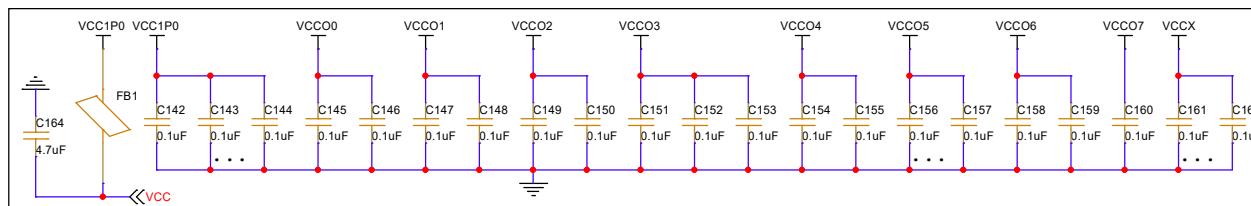
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**GW2A-LV18-PBGA256E**



**RECONFIG\_N** << R45 4.7K  
\*Configuration reset section

The circuit diagram shows a logic signal labeled "READY" entering a buffer stage. The buffer consists of a resistor R46 (blue) and a resistor 4.7K (orange) connected in series. The output of this buffer then connects to the "VCCO3" block.



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D

C

B

A

D

C

B

A

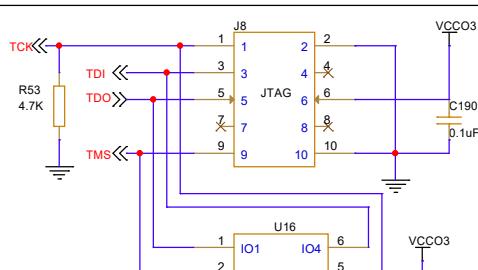
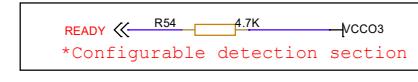
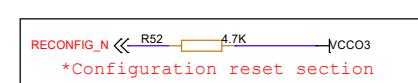
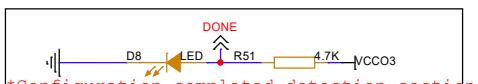
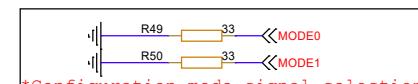
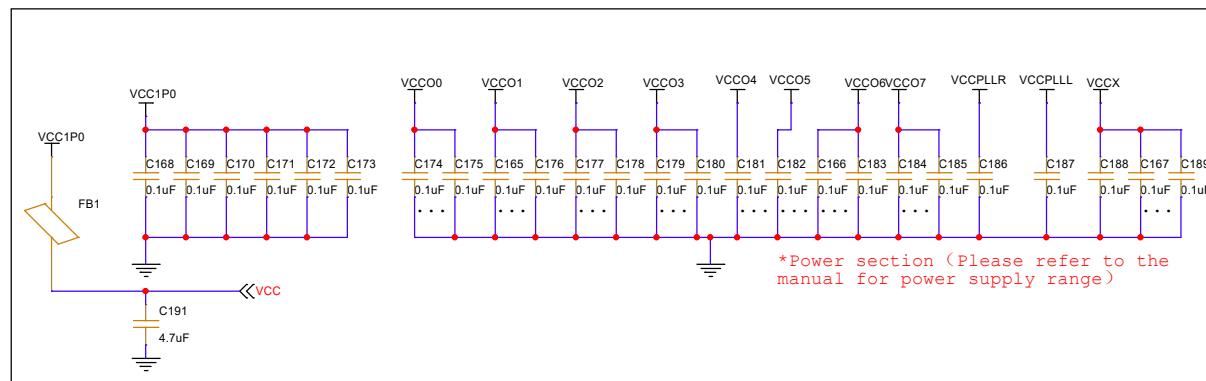
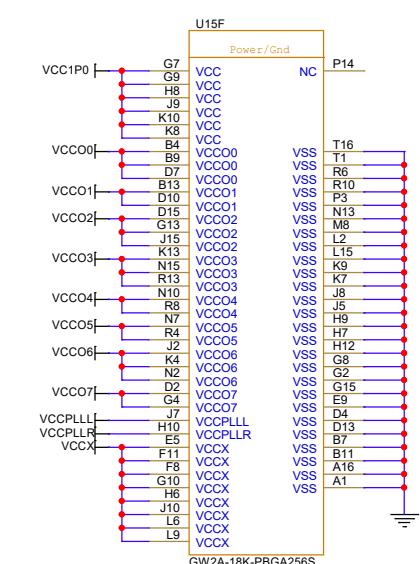
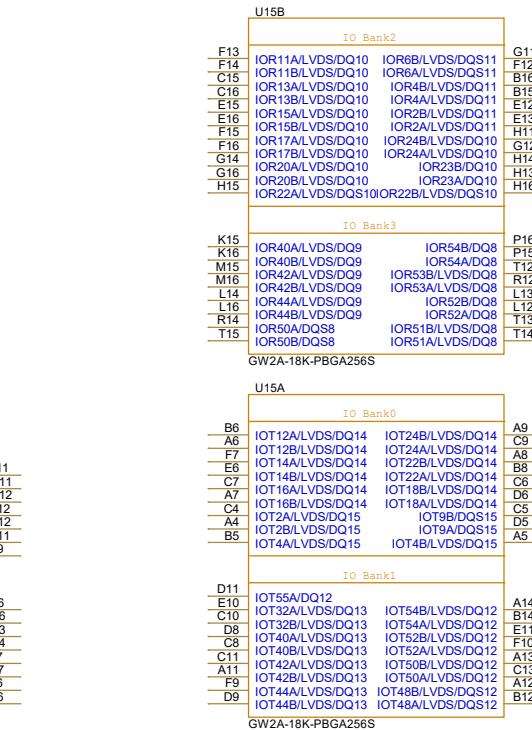
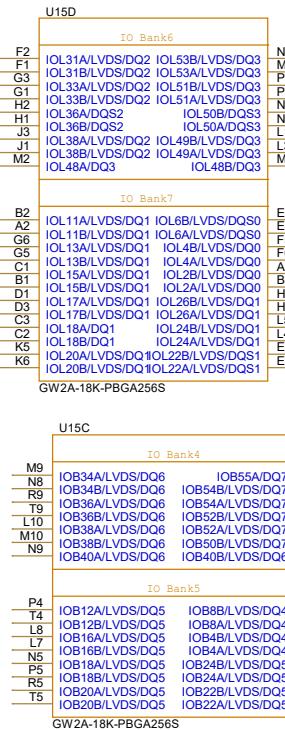
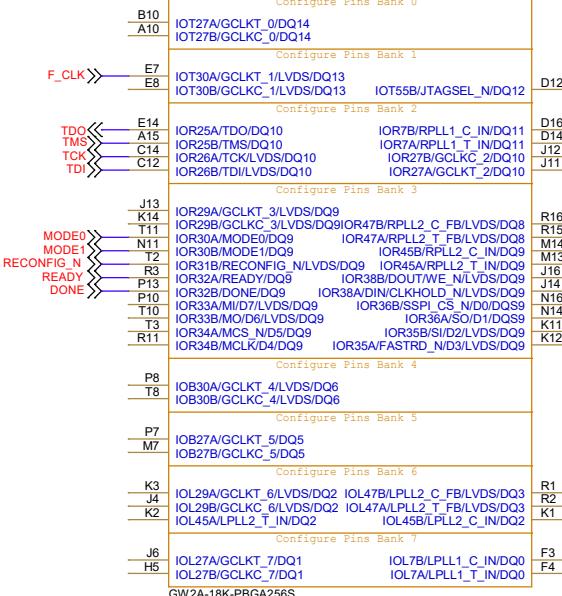
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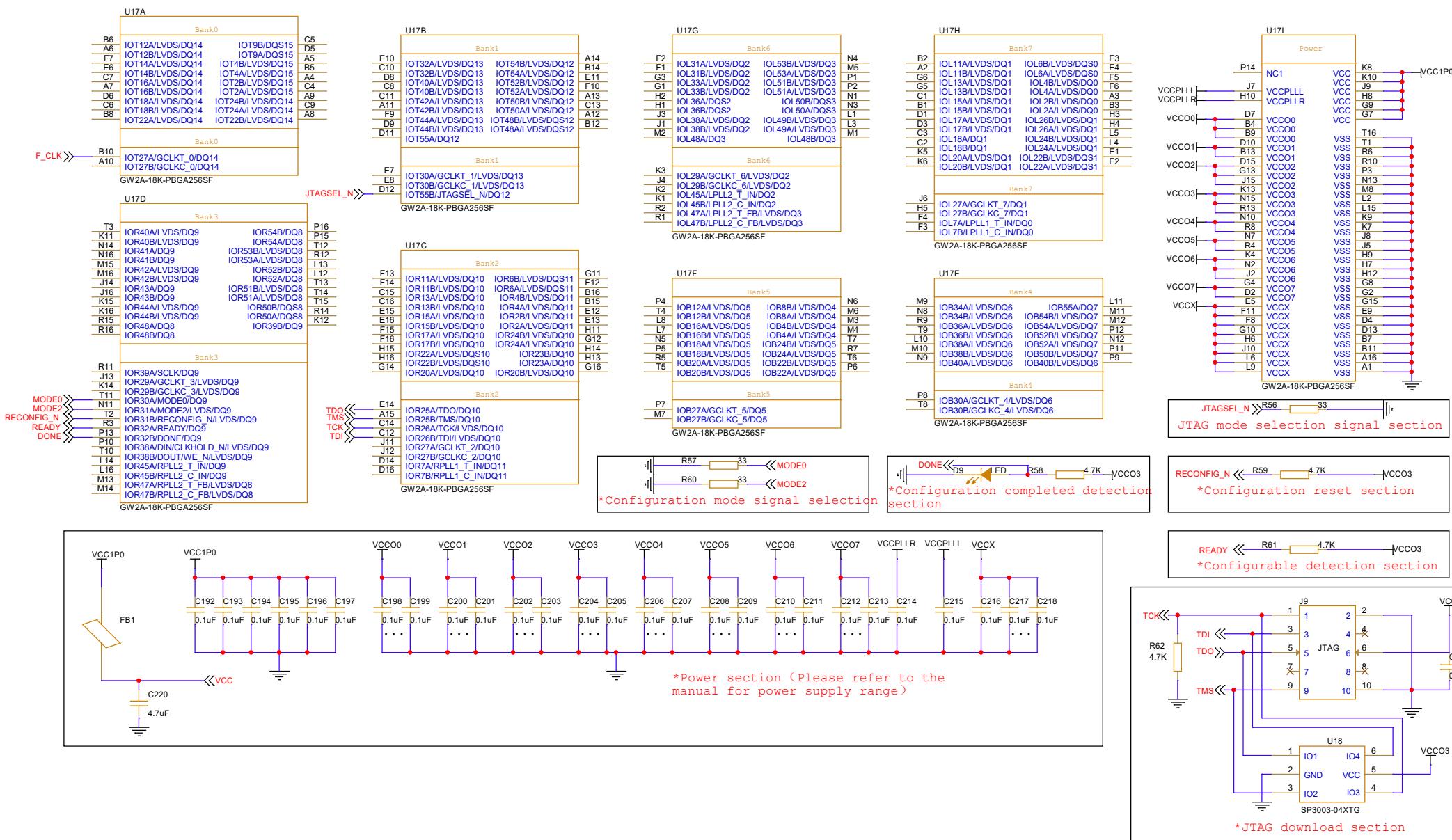
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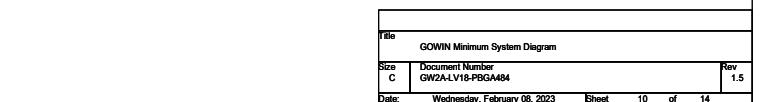
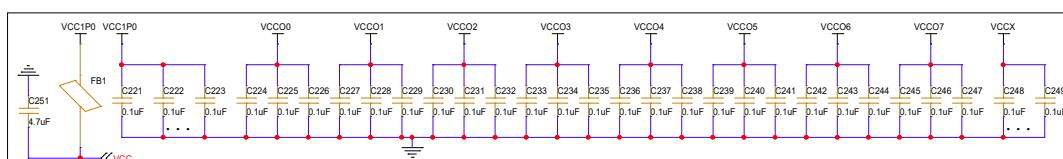
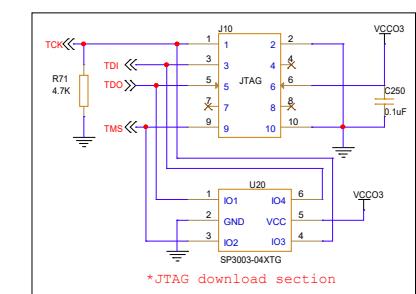
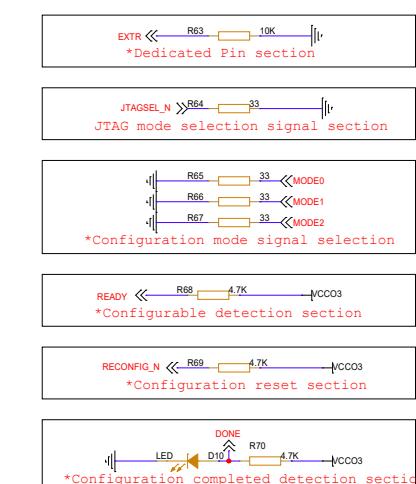
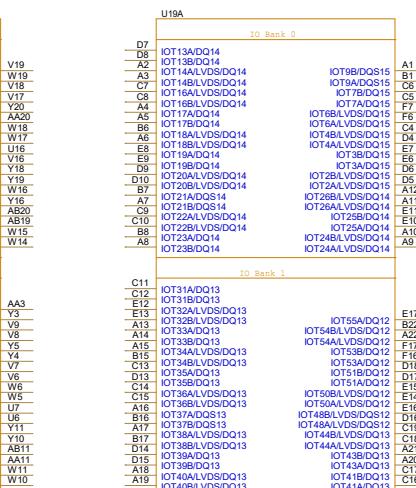
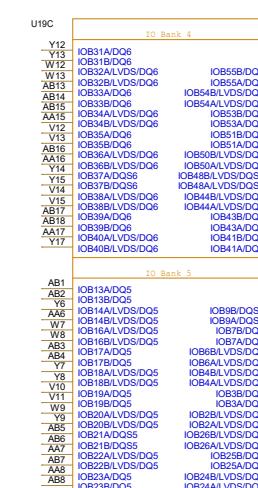
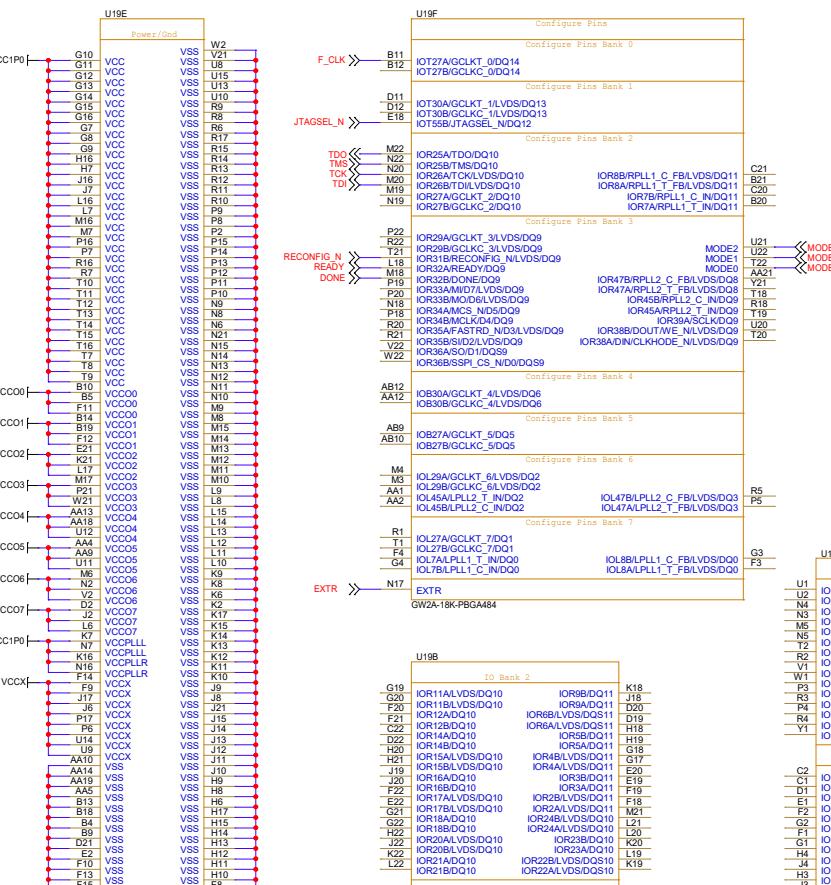
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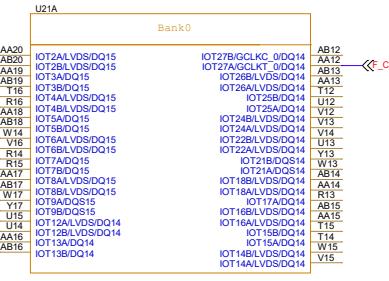
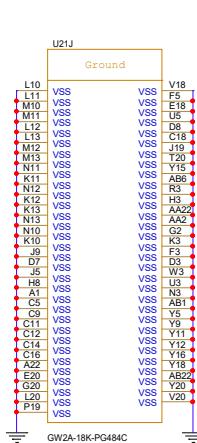
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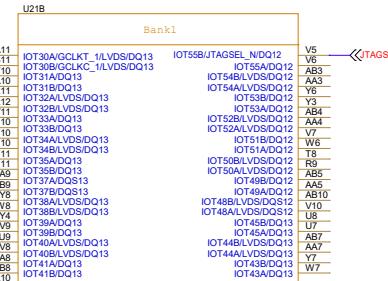




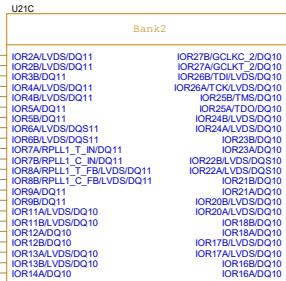




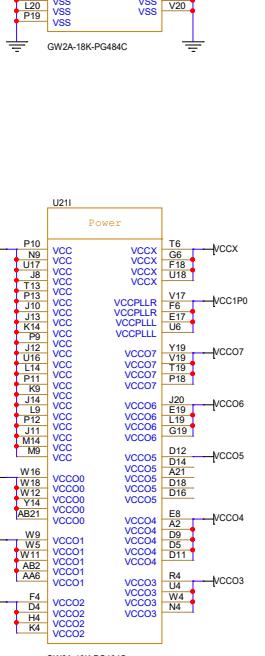
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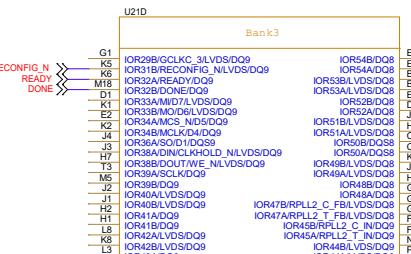
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IOT42B/LVDS/DQ13



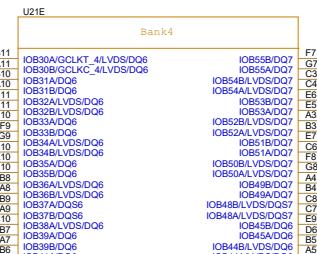
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IOR15A/LVDS/DQ10



GW2A-18K-PG484C



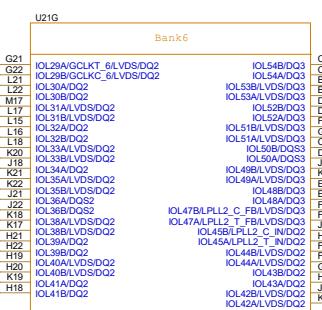
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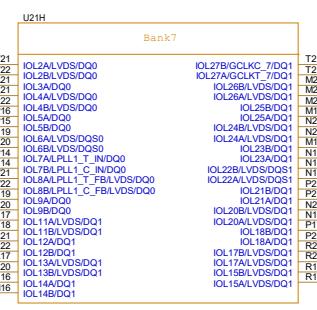
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**16** IOB13B/DQ5      **17** IOB14A/LVDS/DQ5      **18** IOB18A/LVDS/DQ5      **19** IOB17A/DQ5



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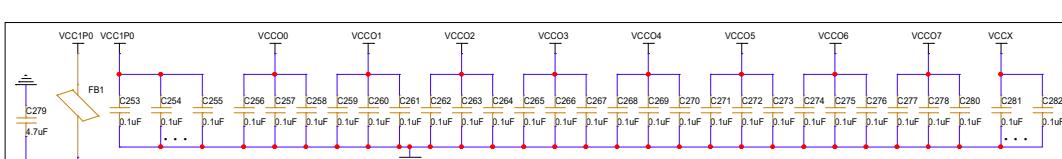
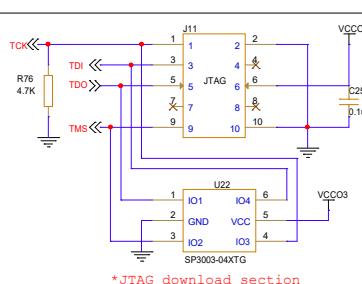
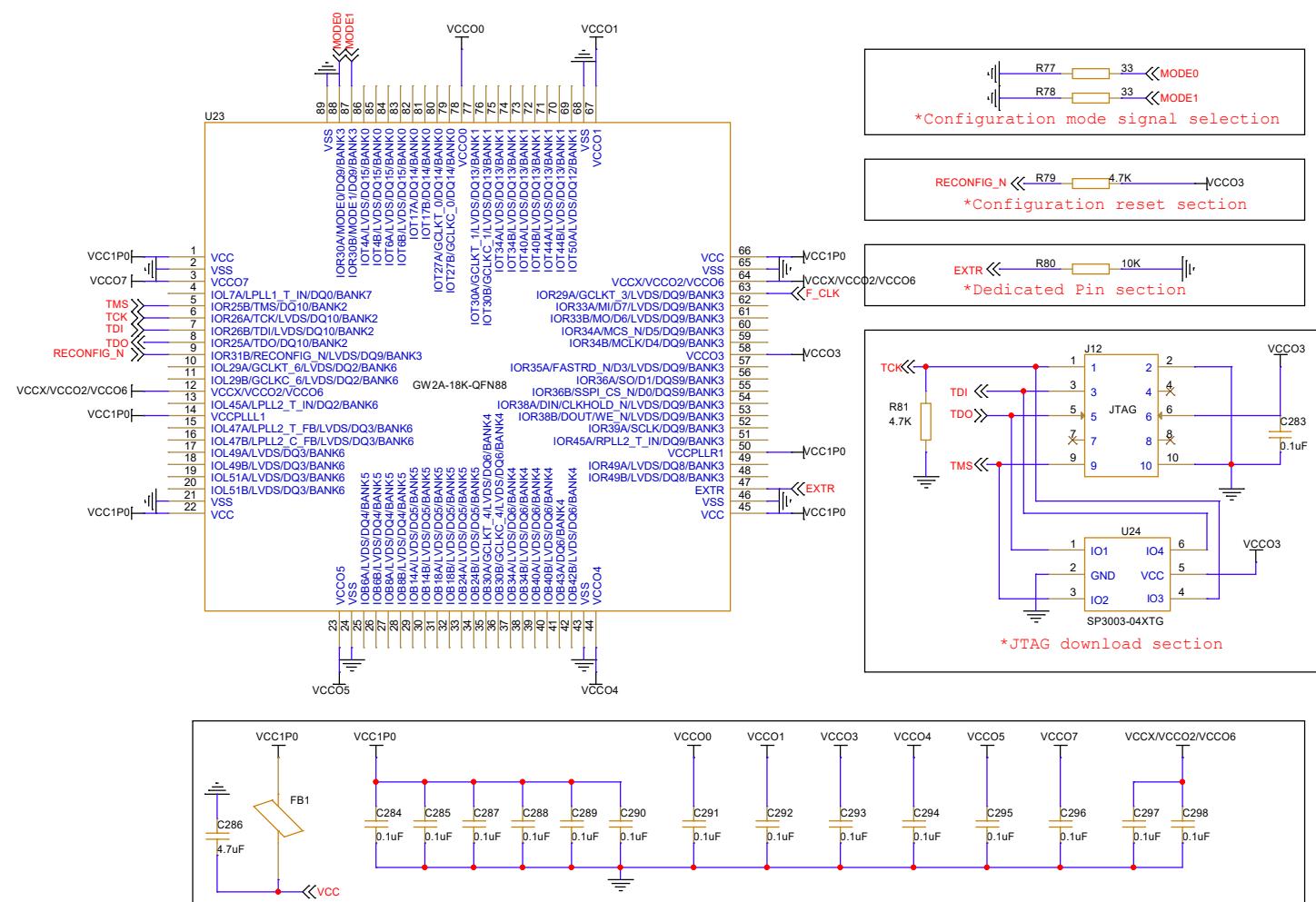


Figure 1.2.10. A logic symbol for a three-terminal voltage-controlled voltage source (VCCS). The output terminal is labeled V<sub>out</sub>, the input terminal is labeled V<sub>in</sub>, and the control terminal is labeled V<sub>CC</sub>.



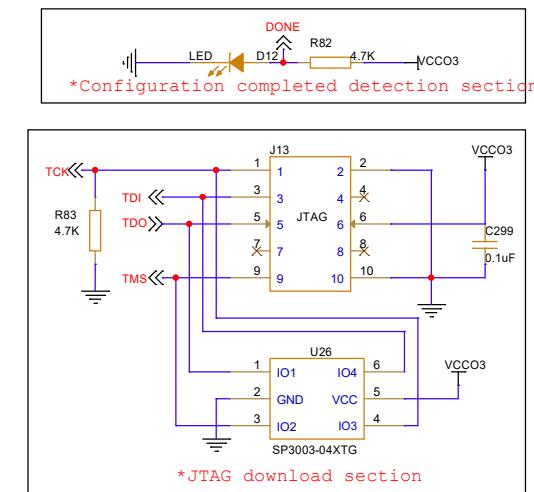
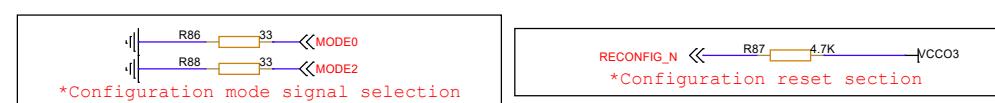
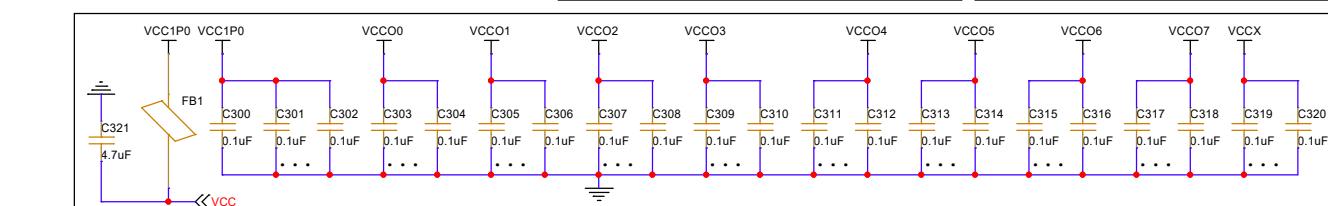
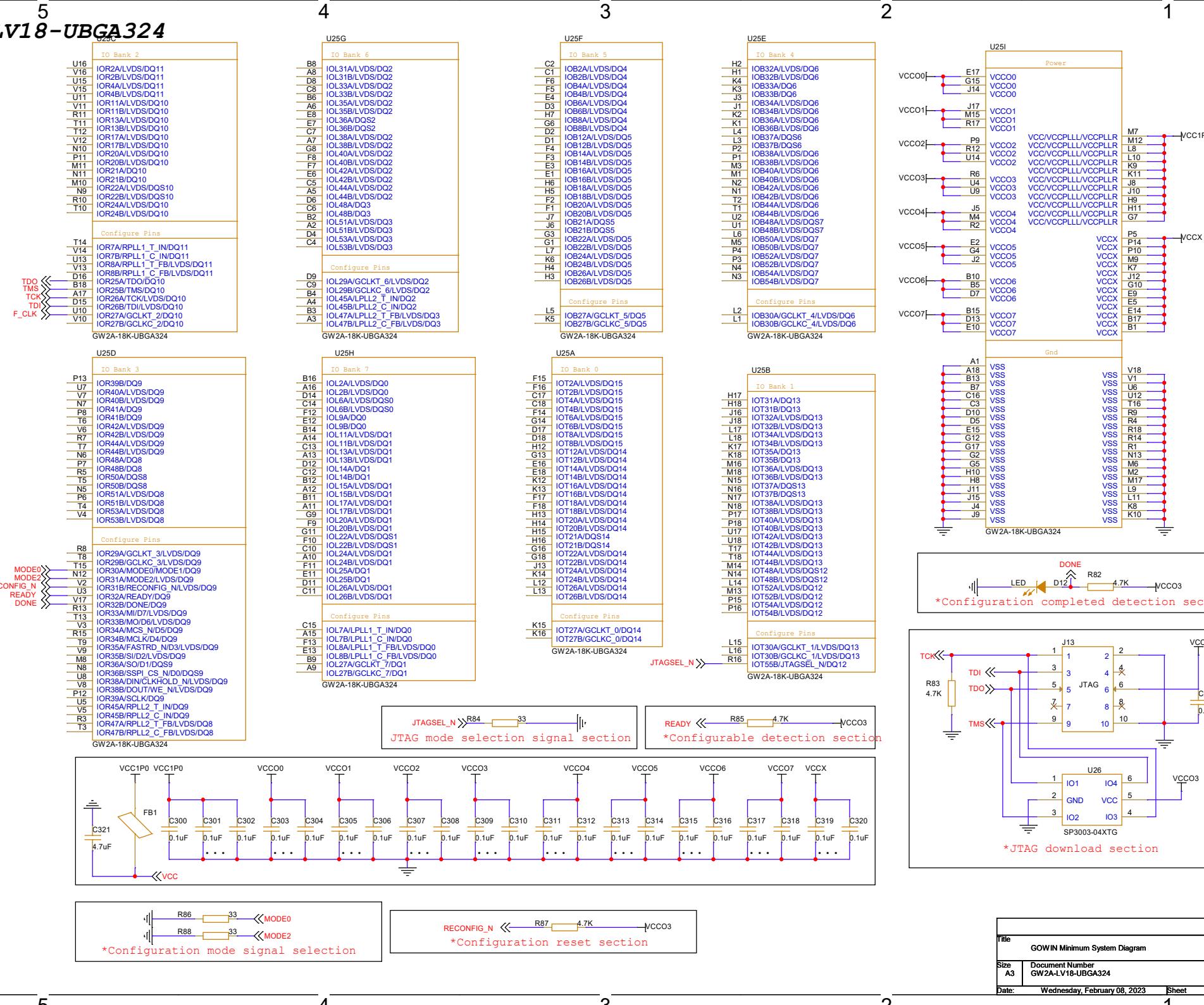
\*JTAG download section

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