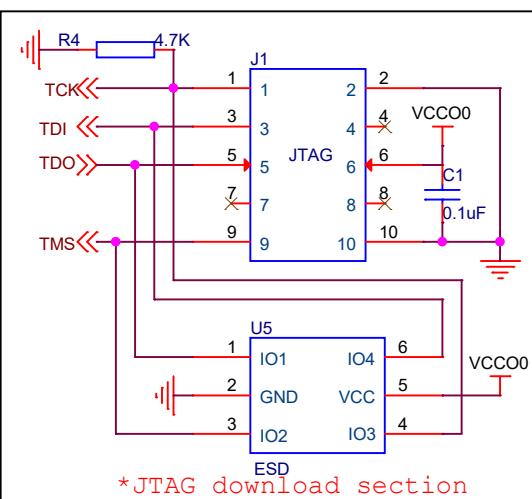


READY ⇢ R1 4.7K VCC00
*Configurable detection section

RECONFIG_N ⇢ R2 4.7K VCC00
*Configuration reset section

JTAGSEL_N ⇢ R3 1K |||
JTAG mode selection signal section



Notes:

1. F CLK signal is an external input clock signal.

It is recommended that F CLK signal be provided through an active oscillator crystal.

2. It is recommended that add an ESD protection chip to the JTAG download circuit.

Title	
GOWIN Minimum System Diagram	
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Rev 2.0	