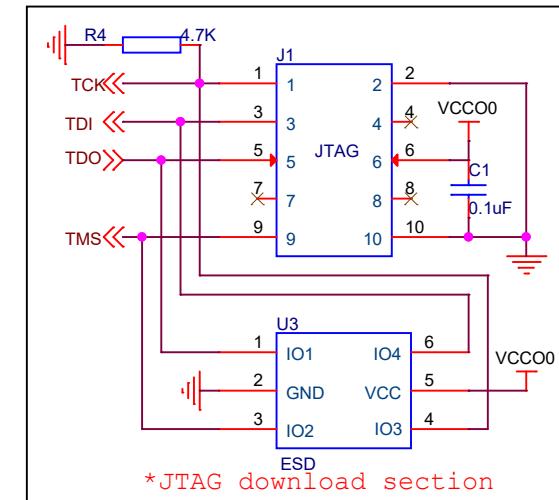


READY << R1 4.7K VCCO0  
\*Configurable detection section

RECONFIG\_N << R2 4.7K VCCO0  
\*Configuration reset section

JTAGSEL\_N >> R3 1K ||  
JTAG mode selection signal section



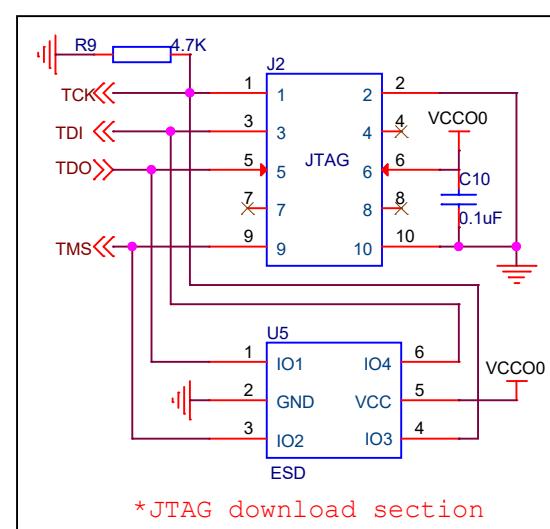
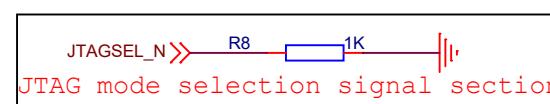
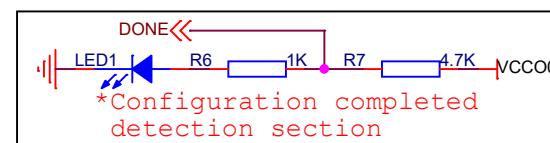
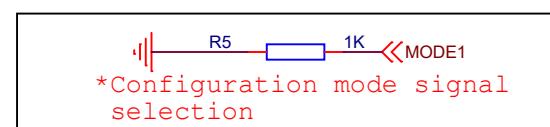
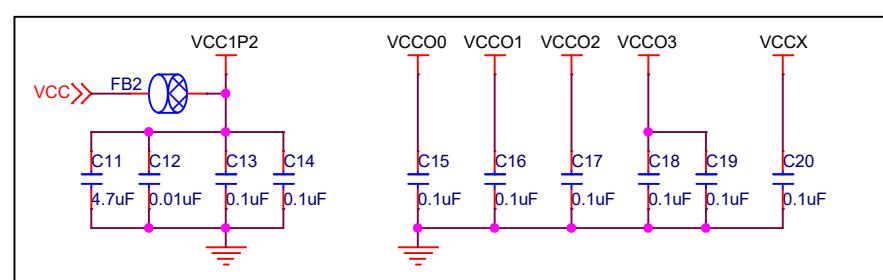
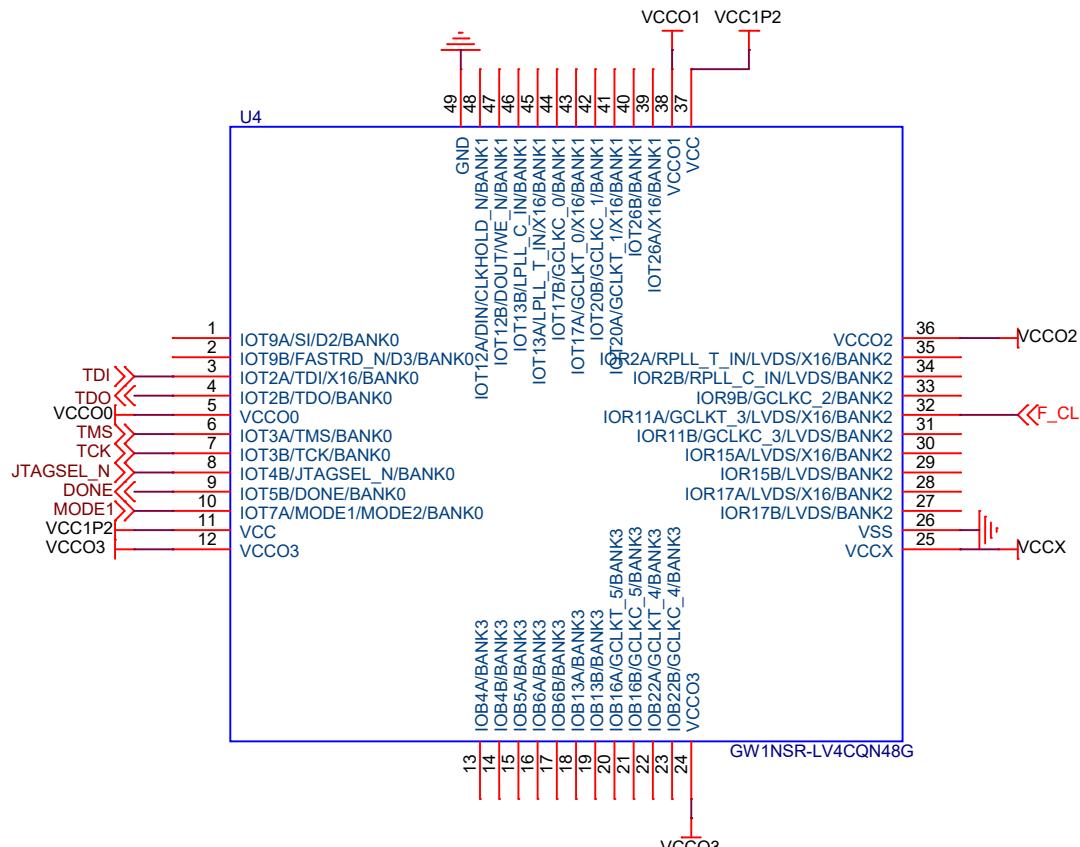
**Notes:**

1. F\_CLK signal is an external input clock signal.

It is recommended that F CLK signal be provided through an active oscillator crystal.

2. It is recommended that add an ESD protection chip to the JTAG download circuit.

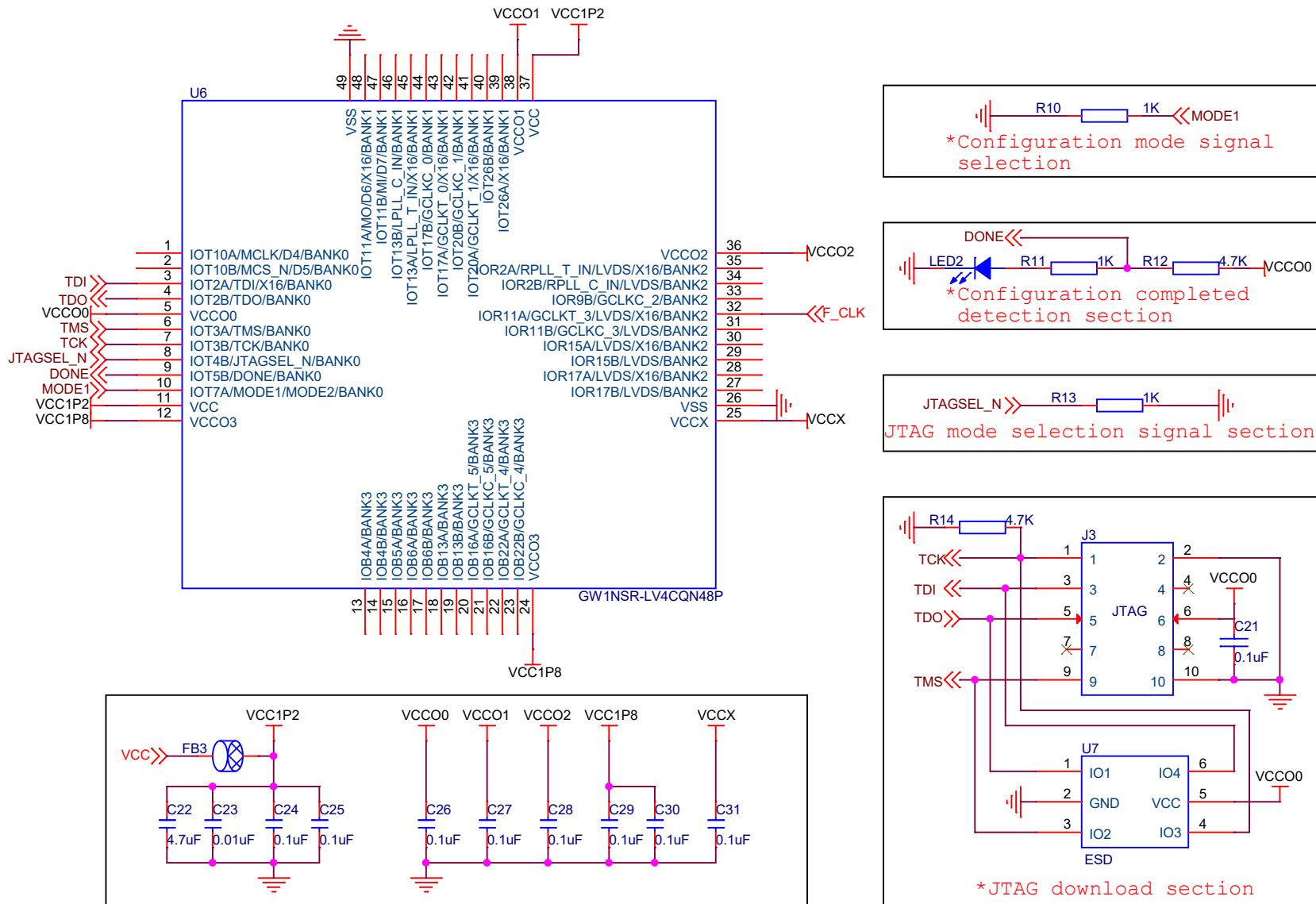
Title	
GOWIN Minimum System Diagram	
Size A4	Document Number GW1NSR-LV4CMG64P
Rev 2.0	



#### Notes:

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It is recommended that F\_CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.

# GW1NSR-LV4CQN48P



## Notes:

1. F\_CLK signal is an external input clock signal.  
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