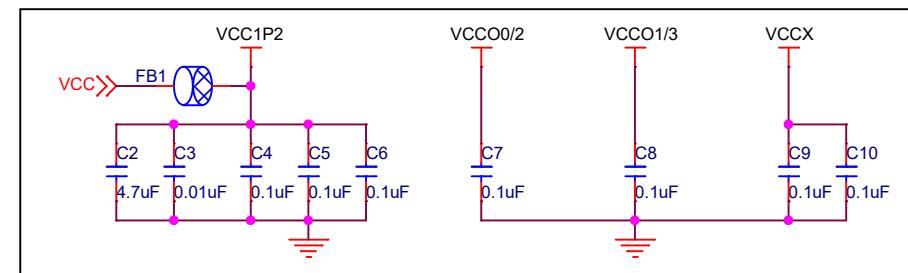
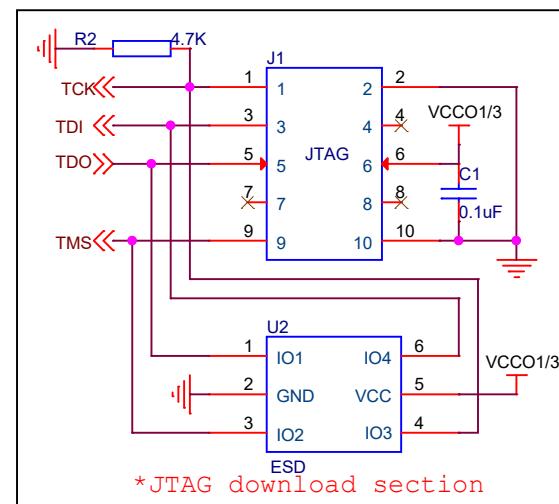
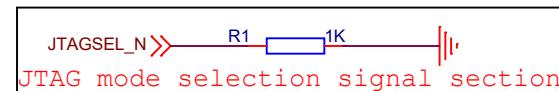
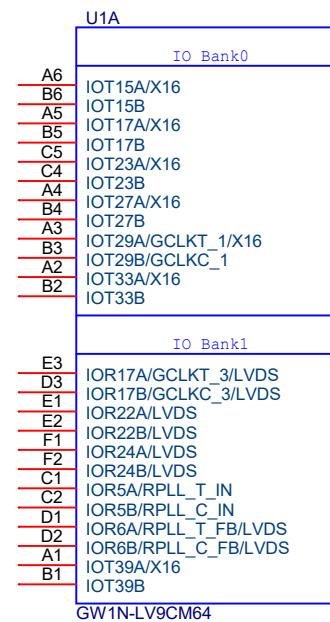
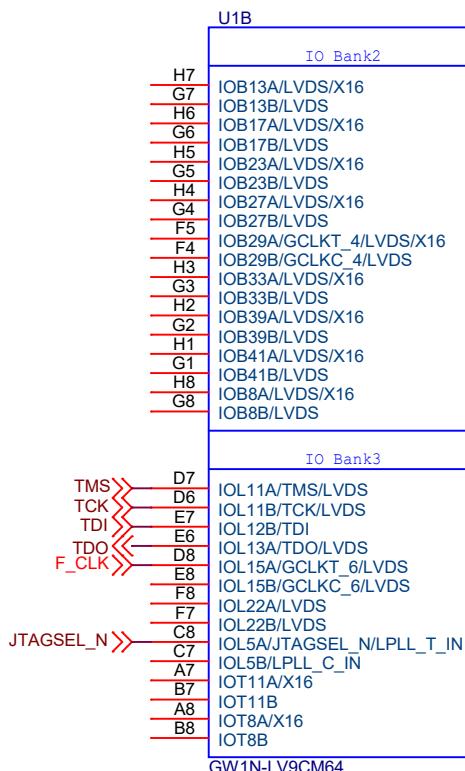


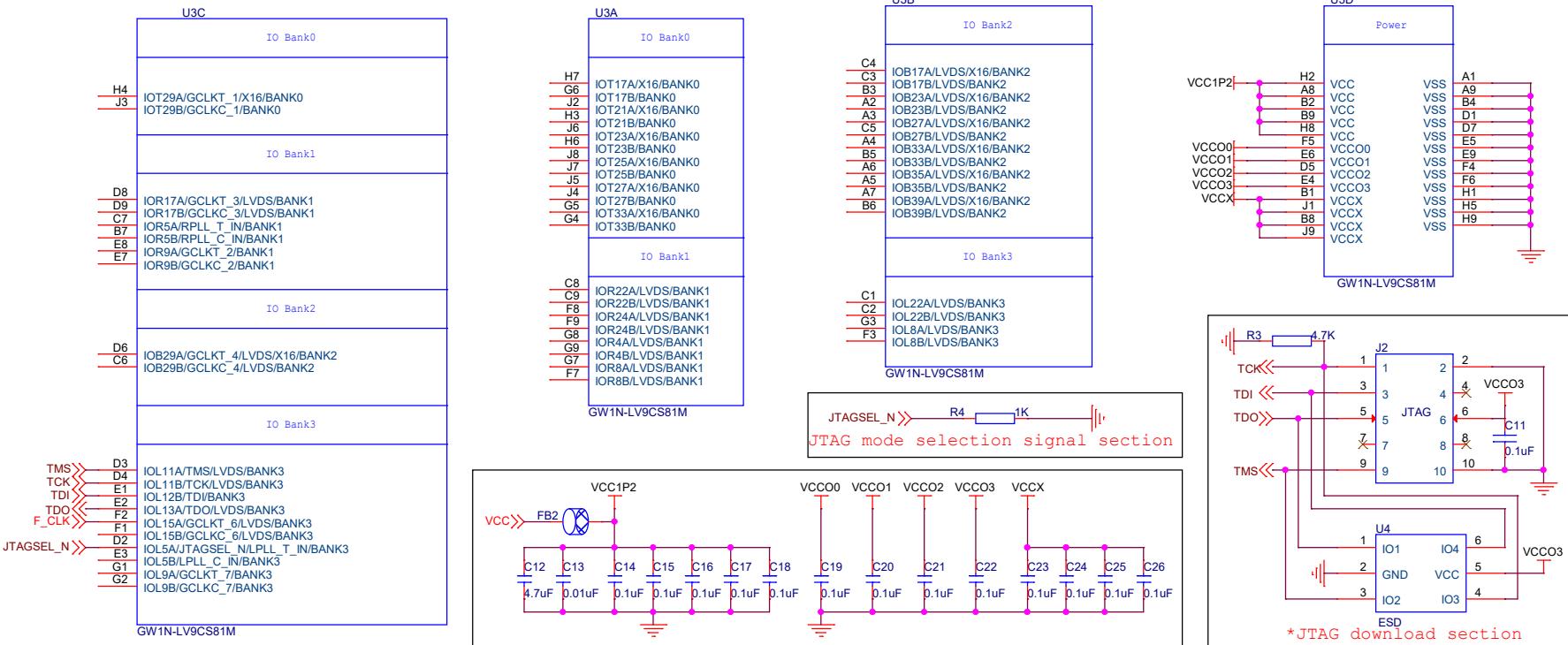
# GW1N-LV9CM64



## Notes:

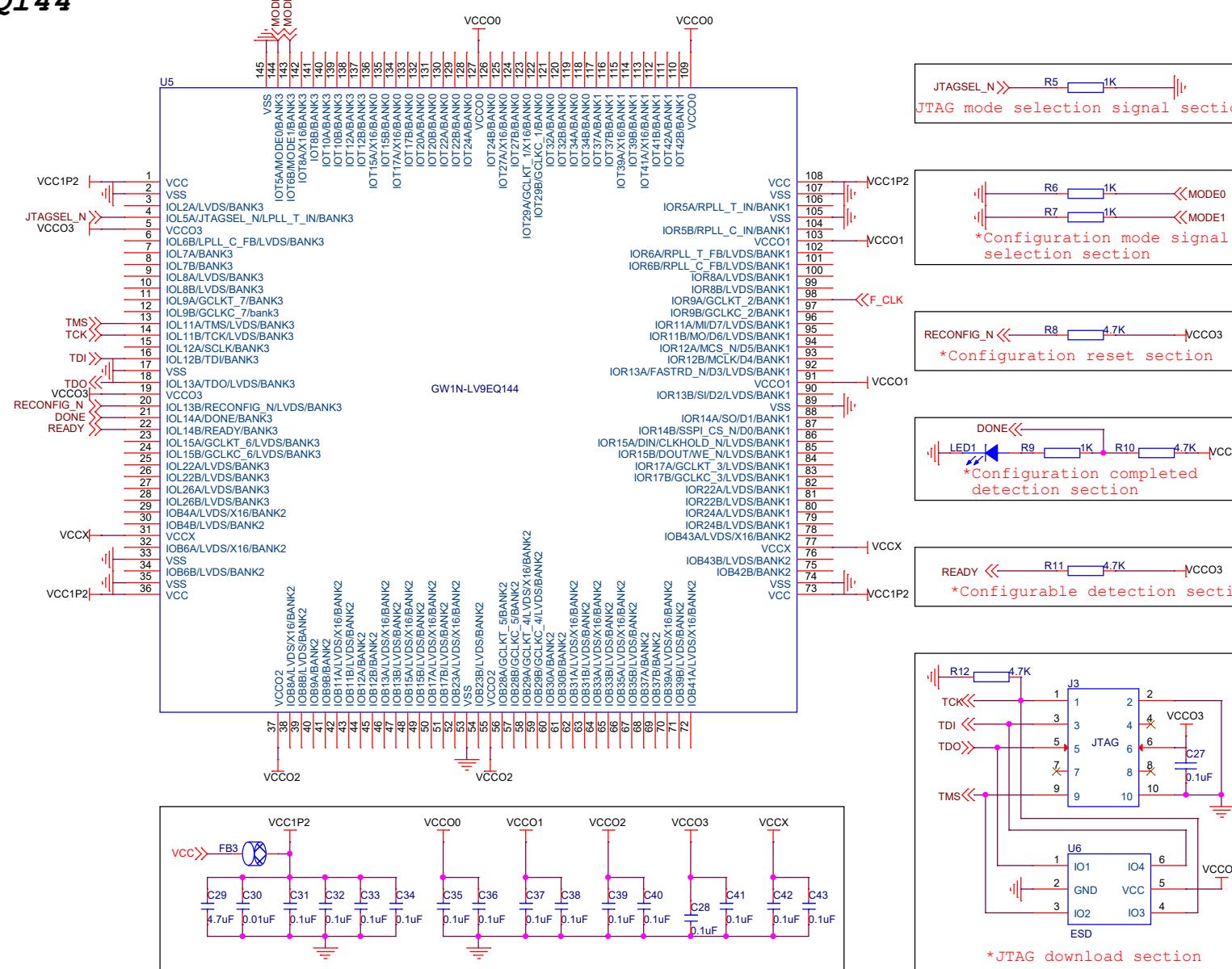
1. F\_CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.

Title	
GW1N Minimum System Diagram	
Size	Document Number
A4	GW1N-LV9CM64
Rev 2.0	
Date: Friday, April 21, 2023	Sheet 1 of 32

**GW1N-LV9CS81M****Notes:**

1. F\_CLK signal is an external input clock signal.
- It is recommended that F\_CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-LV9CS81M	2.0

**Notes:**

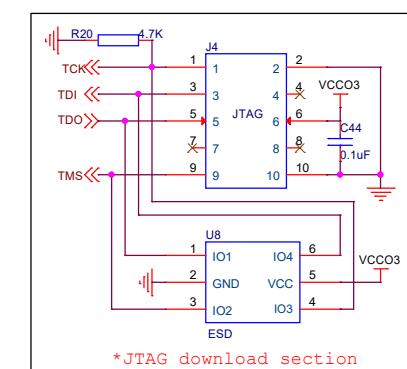
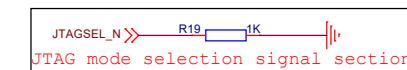
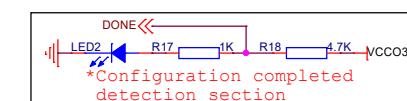
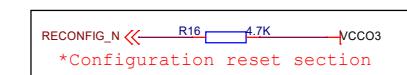
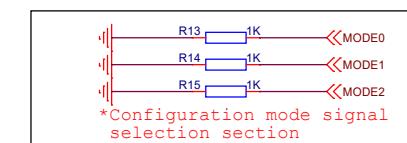
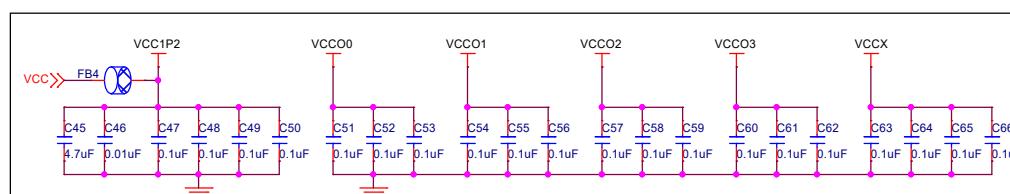
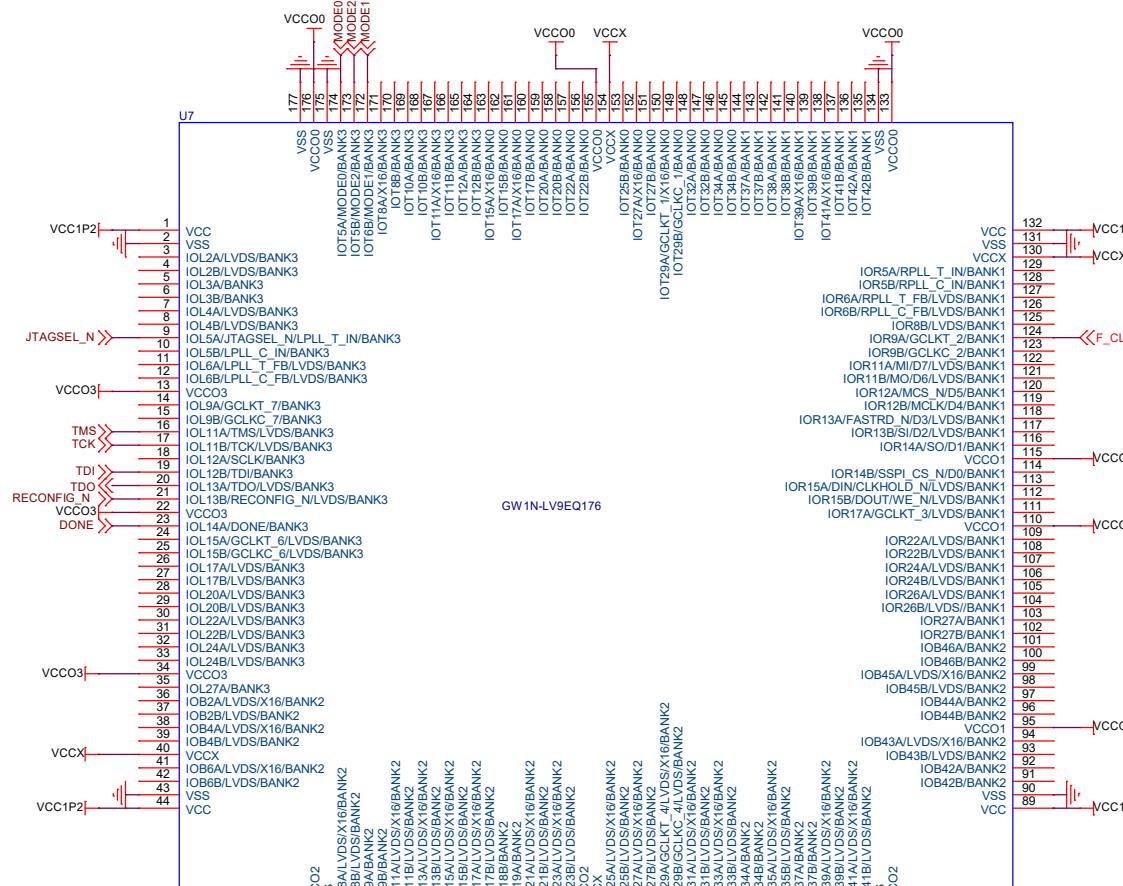
1. F\_CLK signal is an external input clock signal.

It is recommended that F\_CLK signal be provided through an active oscillator crystal.

2. It is recommended that add an ESD protection chip to the JTAG download circuit.

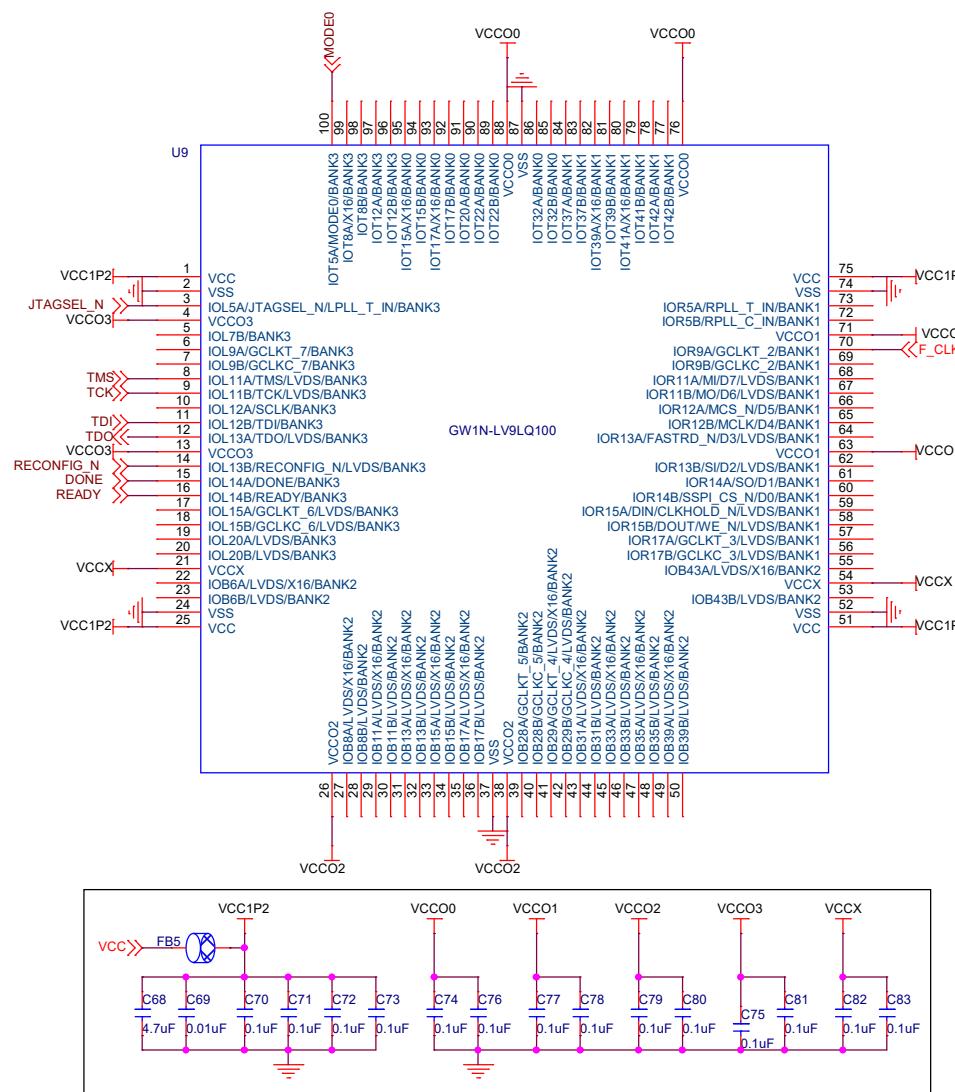
Title: GOWIN Minimum System Diagram  
Size: B Document Number: GW1N-LV9EQ144

Rev 2.0

**Notes:**

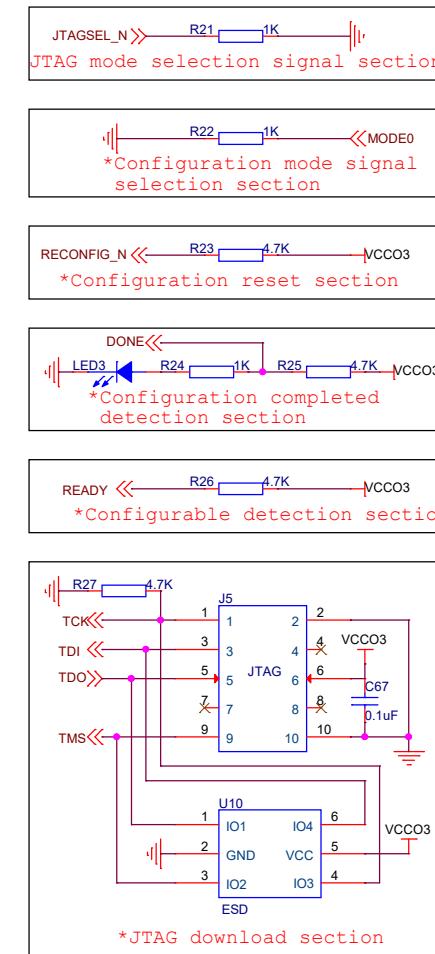
- F CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.
- It is recommended that add an ESD protection chip to the JTAG download circuit.

Title	
GW1N Minimum System Diagram	
Size	Document Number
A3	GW1N-LV9EQ176
Rev	2.0
Date:	Friday, April 21, 2023
Sheet	4 of 32

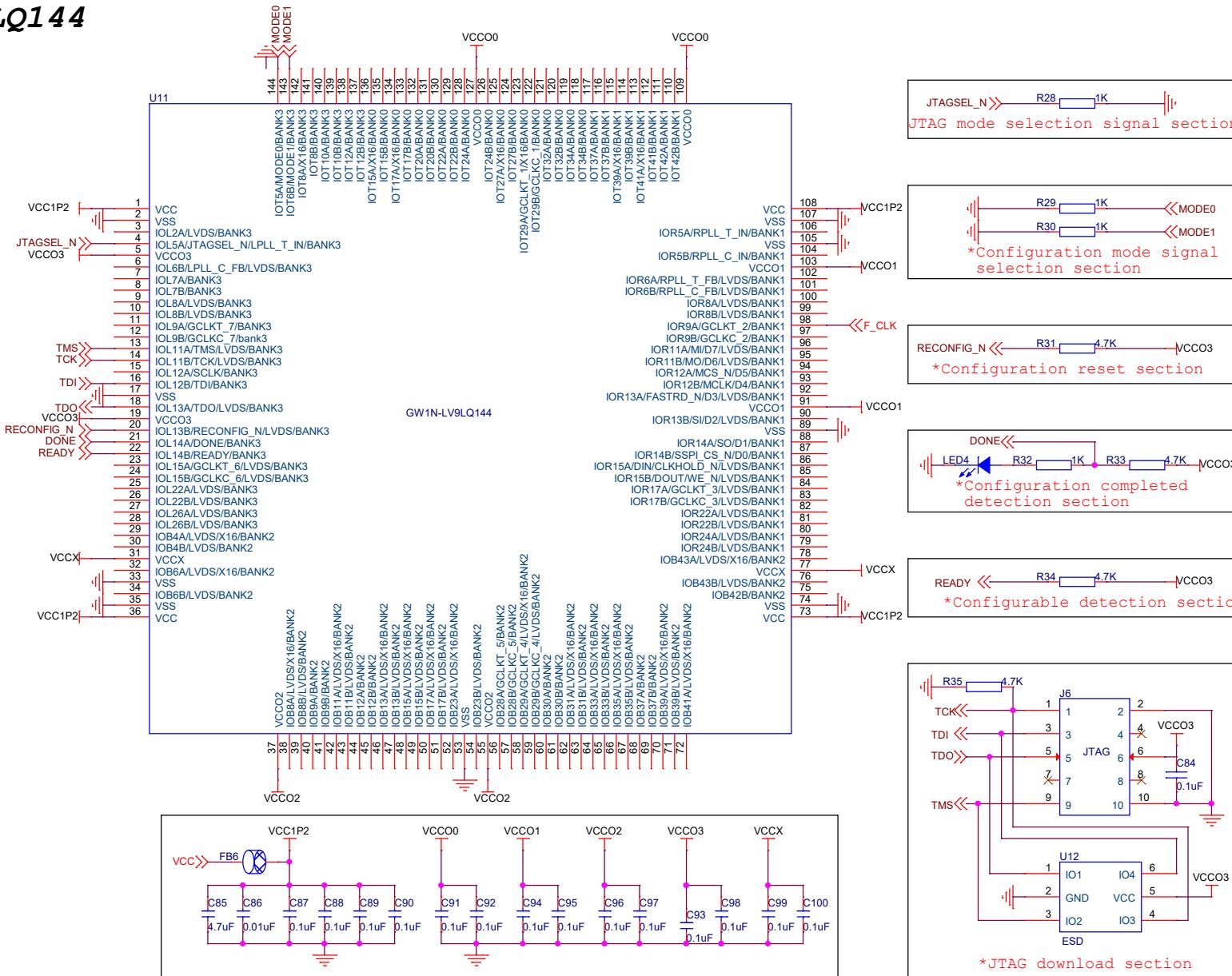


## Notes:

1. F\_CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.



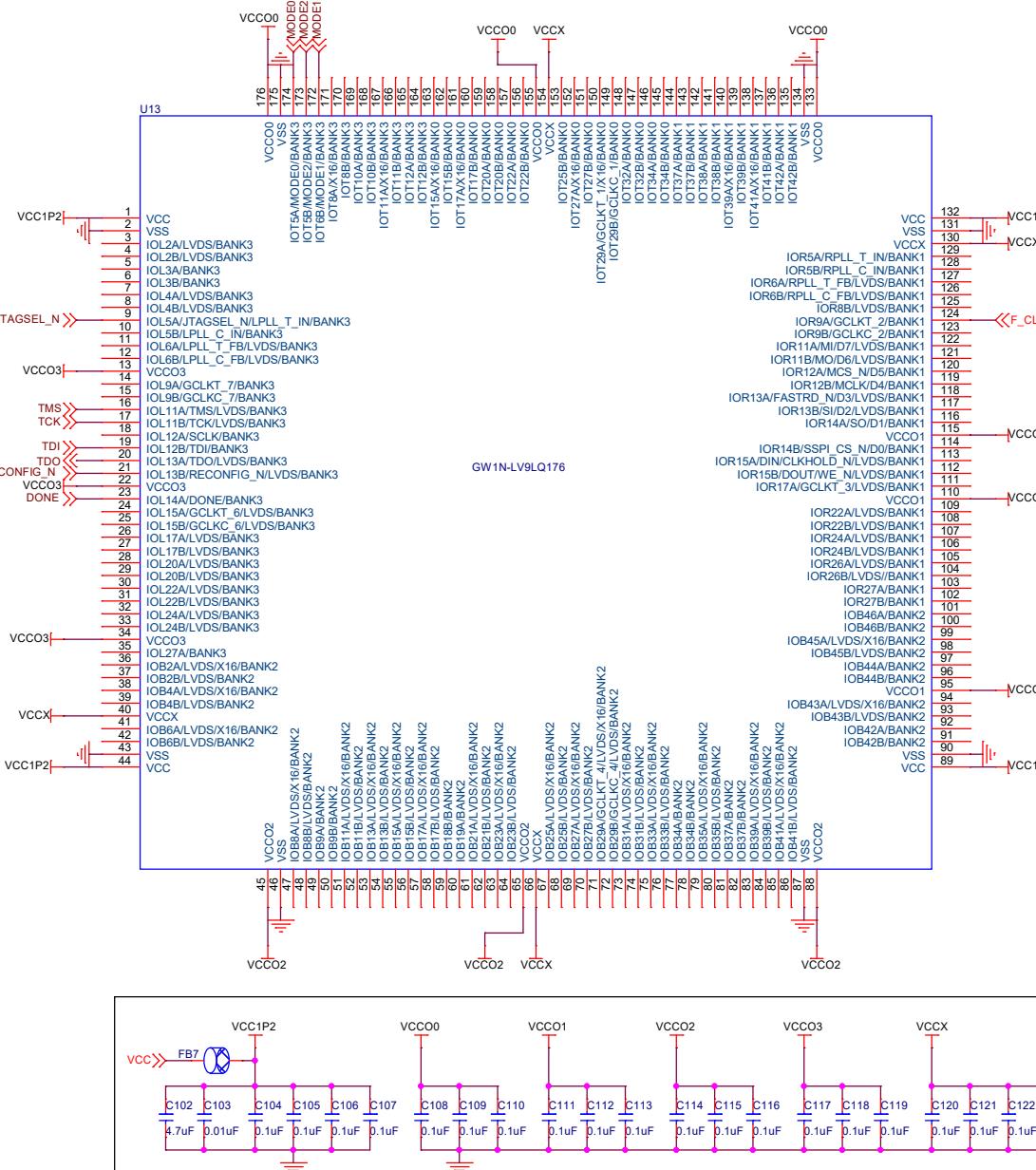
Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-LV9LQ100	2.0
Date:	Friday, April 21, 2023	Sheet 5 of 32

**Notes:**

1. F\_CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.

Title	
GOWIN Minimum System Diagram	
Size	Document Number GW1N-LV9LQ144
B	Rev 2.0

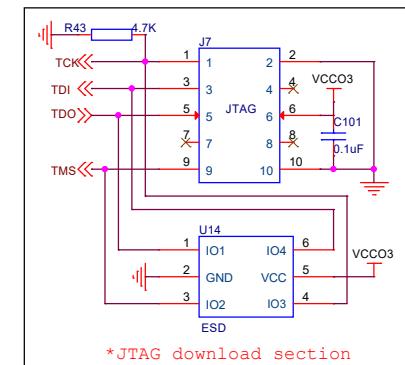
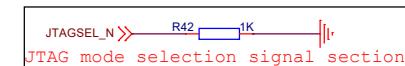
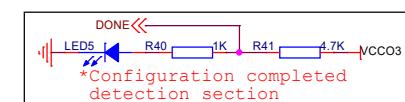
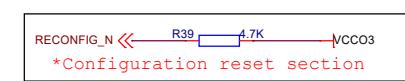
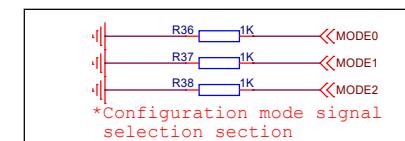
Date: Friday, April 21, 2023 Sheet 6 of 32

**Notes:**

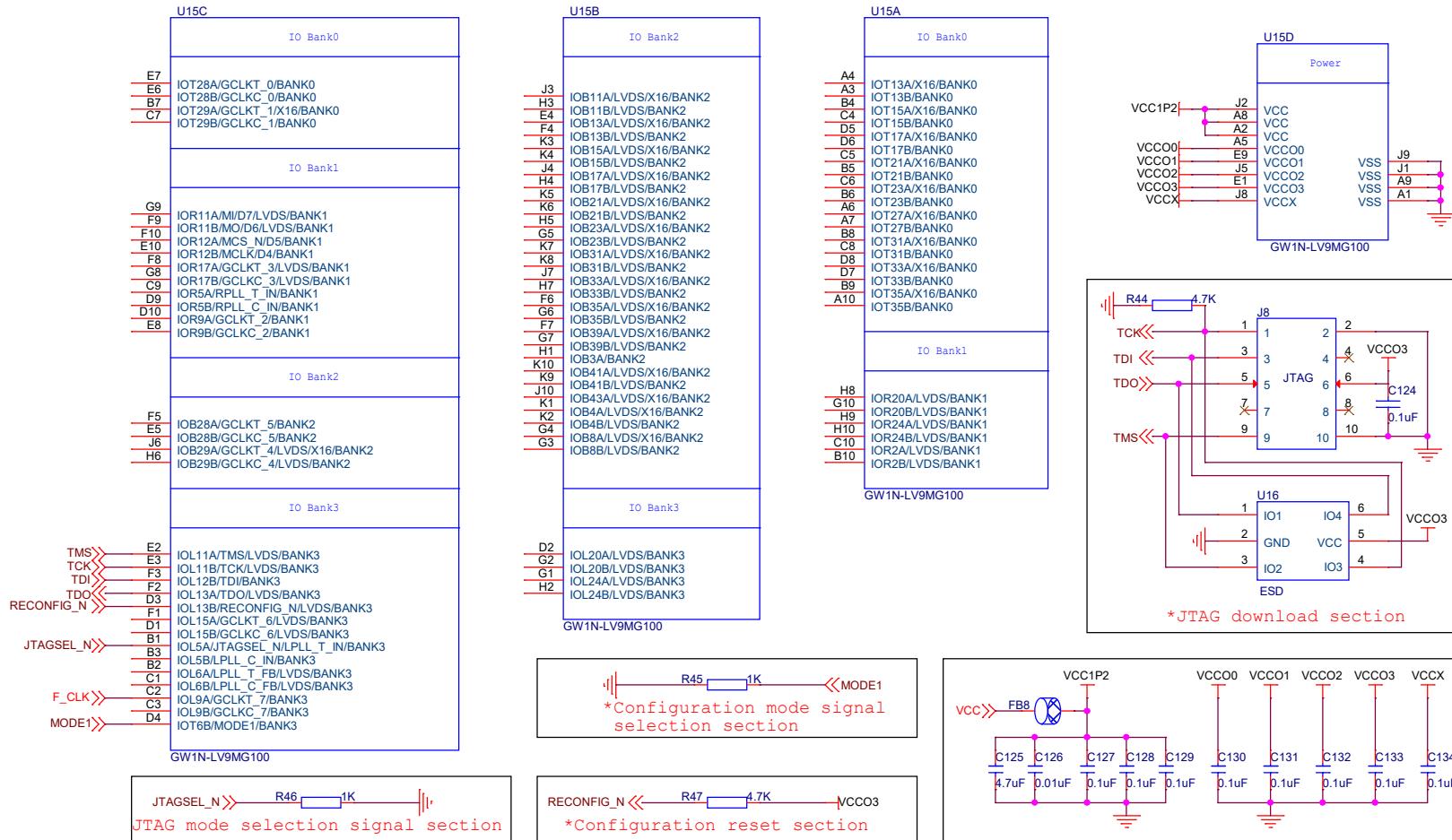
1. F\_CLK signal is an external input clock signal.

It is recommended that F\_CLK signal be provided through an active oscillator crystal.

2. It is recommended that add an ESD protection chip to the JTAG download circuit.

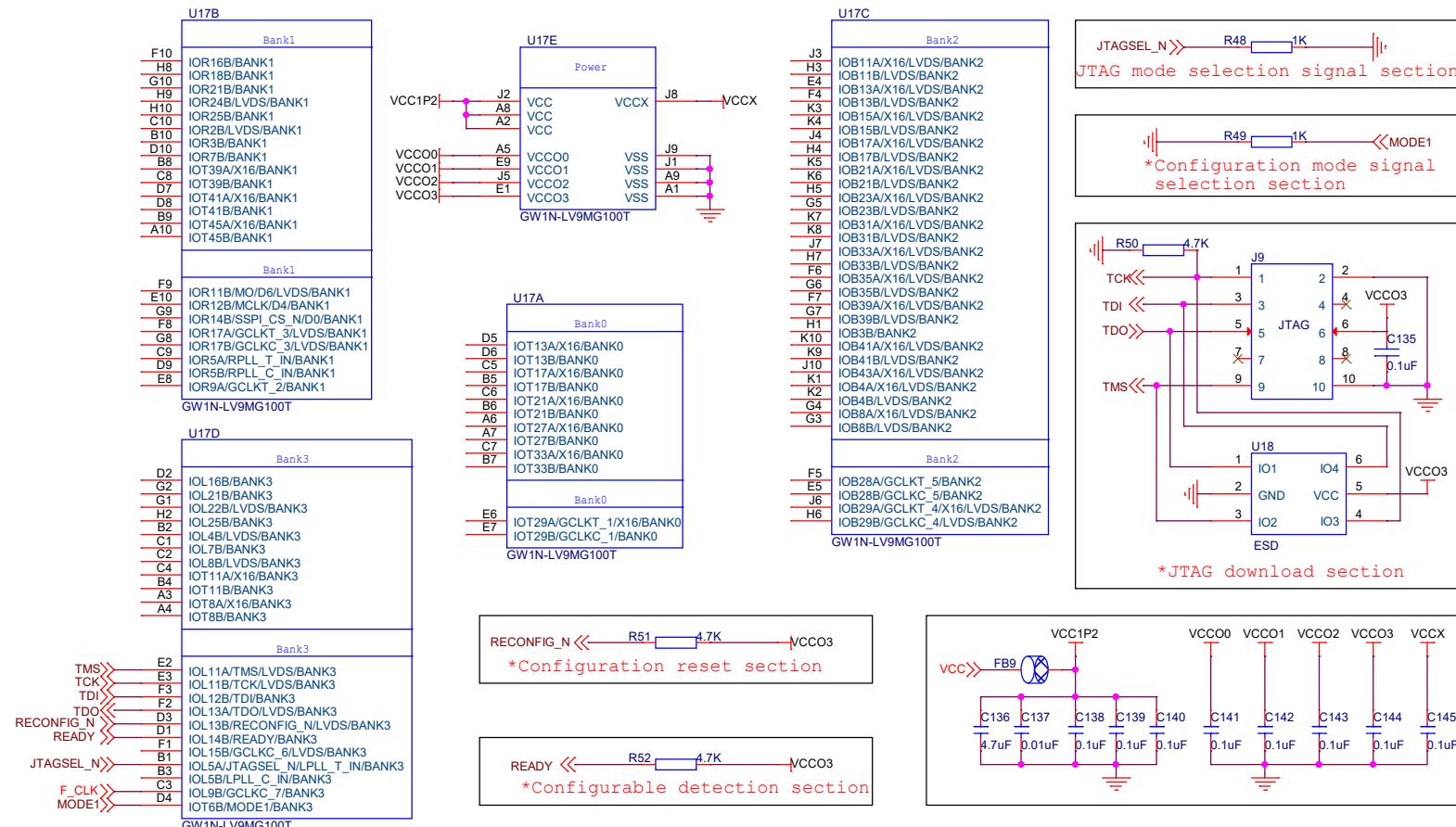


Title	
GOWIN Minimum System Diagram	
Size	Document Number
A3	GW1N-LV9LQ176
Date:	Friday, April 21, 2023
Rev	2.0

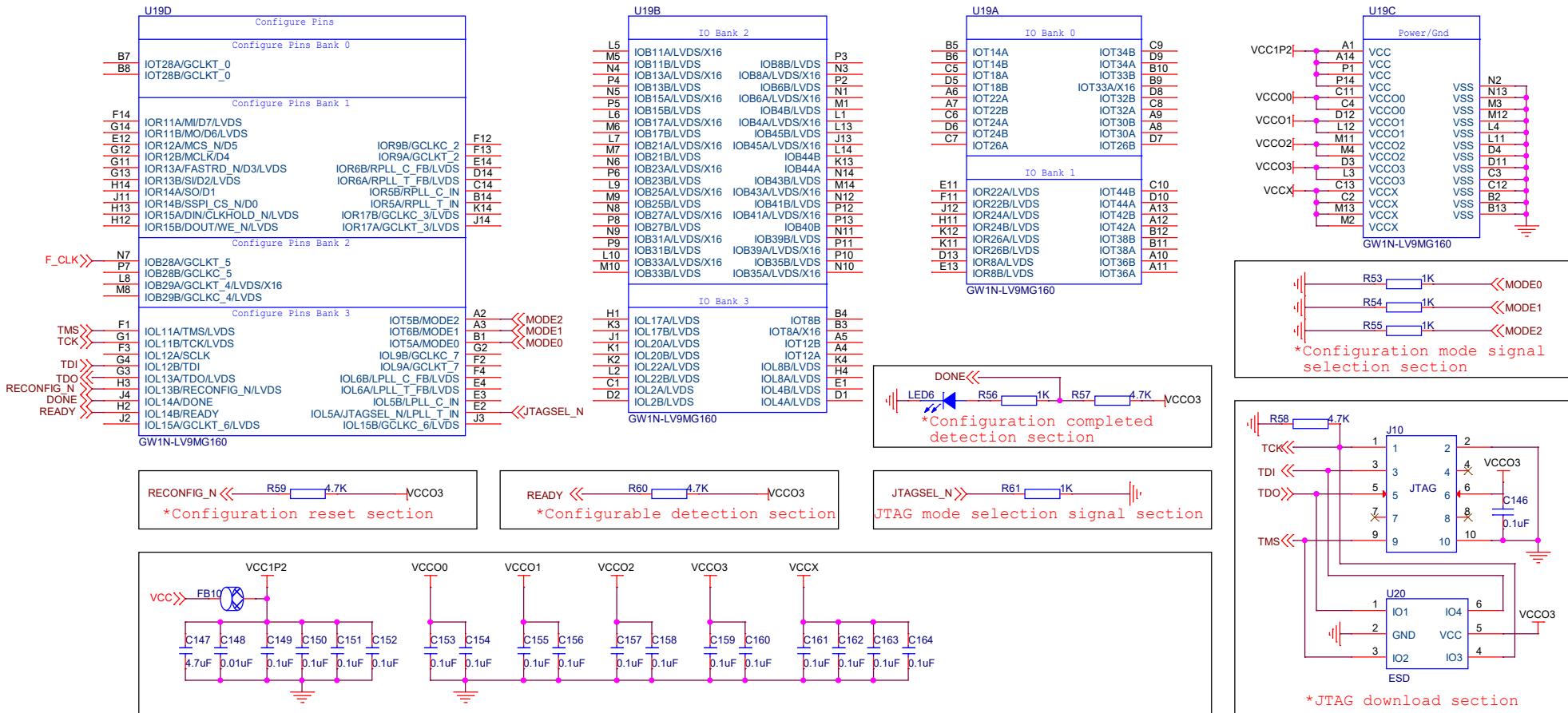
**Notes:**

1. F\_CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-LV9MG100	2.0
	Date: Friday, April 21, 2023	Sheet 8 of 32



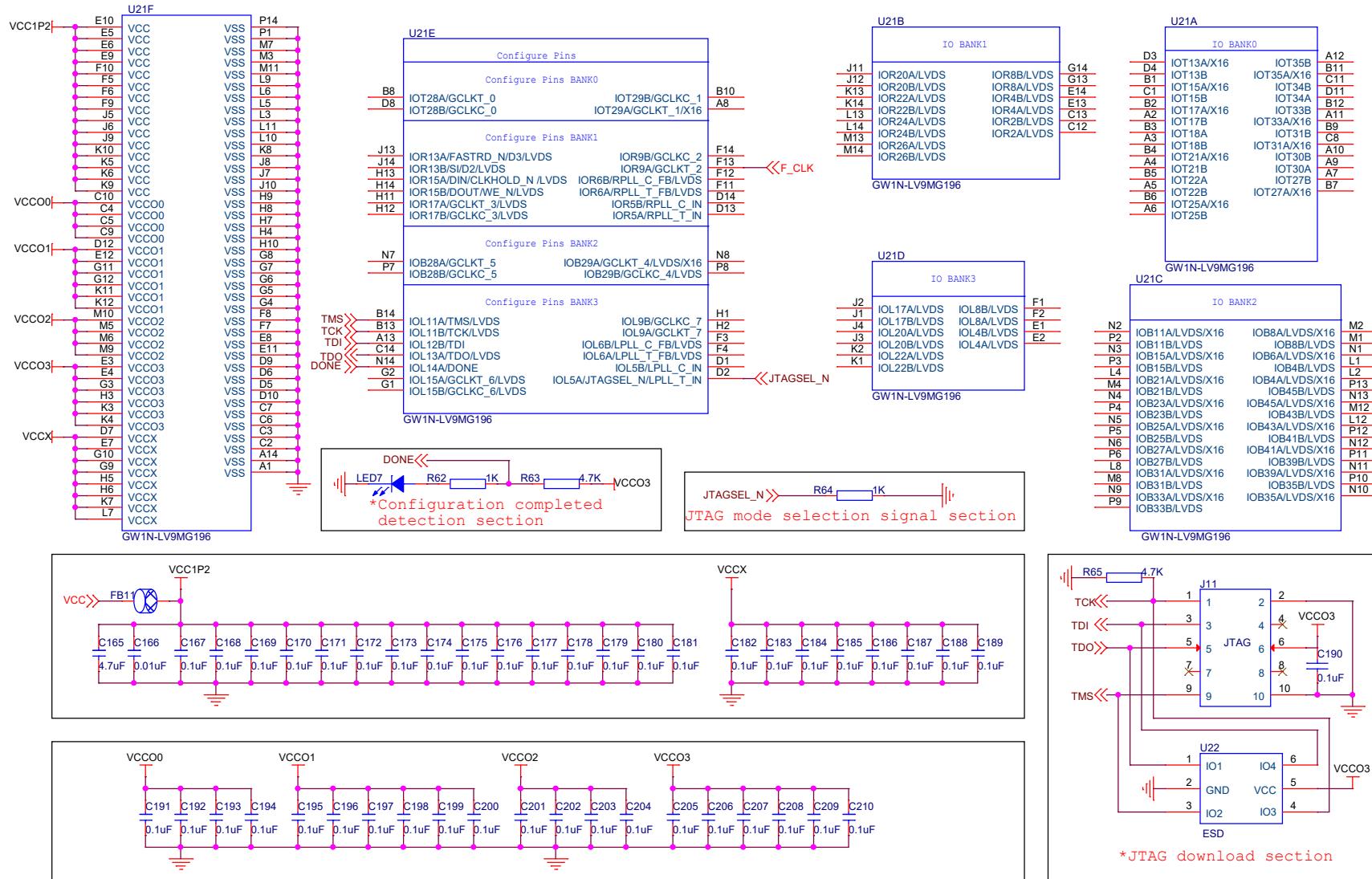
Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-LV9MG100T	2.0

**Notes:**

1. F CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-LV9MG160	2.0

Date: Friday, April 21, 2023 Sheet 10 of 32

**Notes:**

1. F\_CLK signal is an external input clock signal.

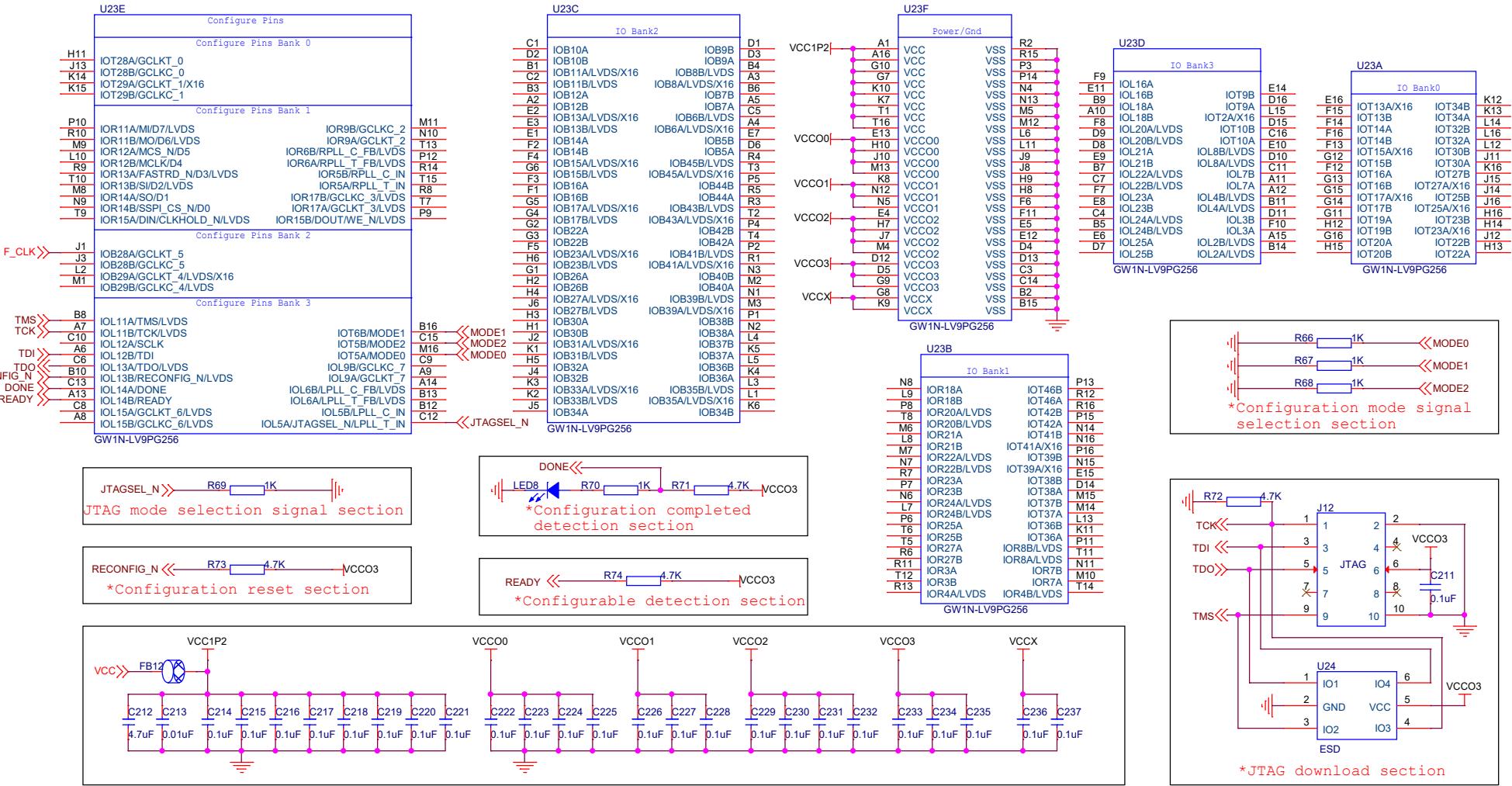
It is recommended that F\_CLK signal be provided through an active oscillator crystal.

2. It is recommended that add an ESD protection chip to the JTAG download circuit.

Title	
GOWIN Minimum System Diagram	

Size	Document Number	Rev
B	GW1N-LV9MG196	2.0

Date:	Friday, April 21, 2023	Sheet	11	of	32
-------	------------------------	-------	----	----	----

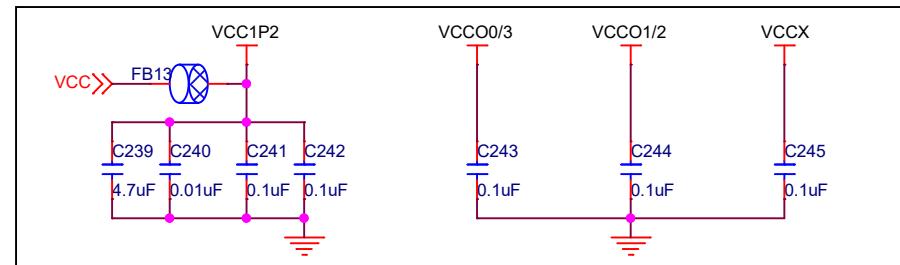
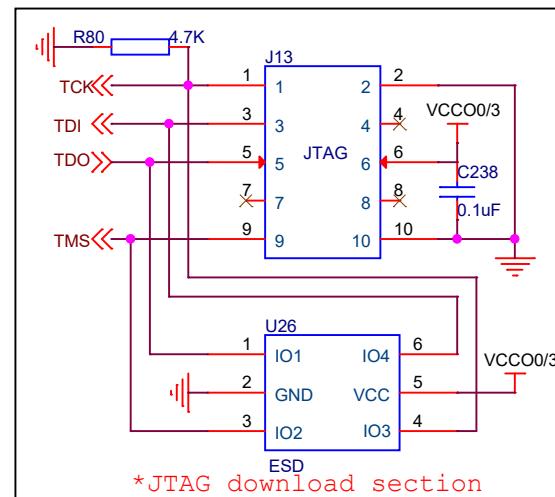
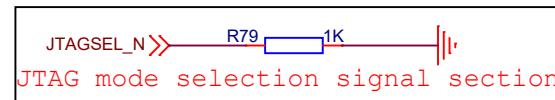
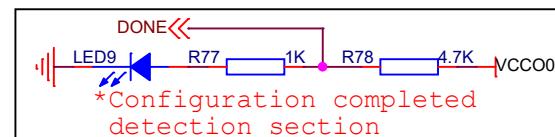
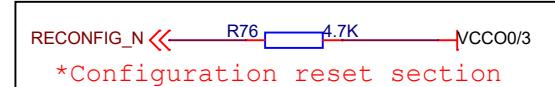
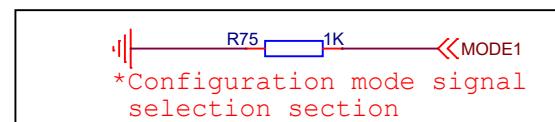
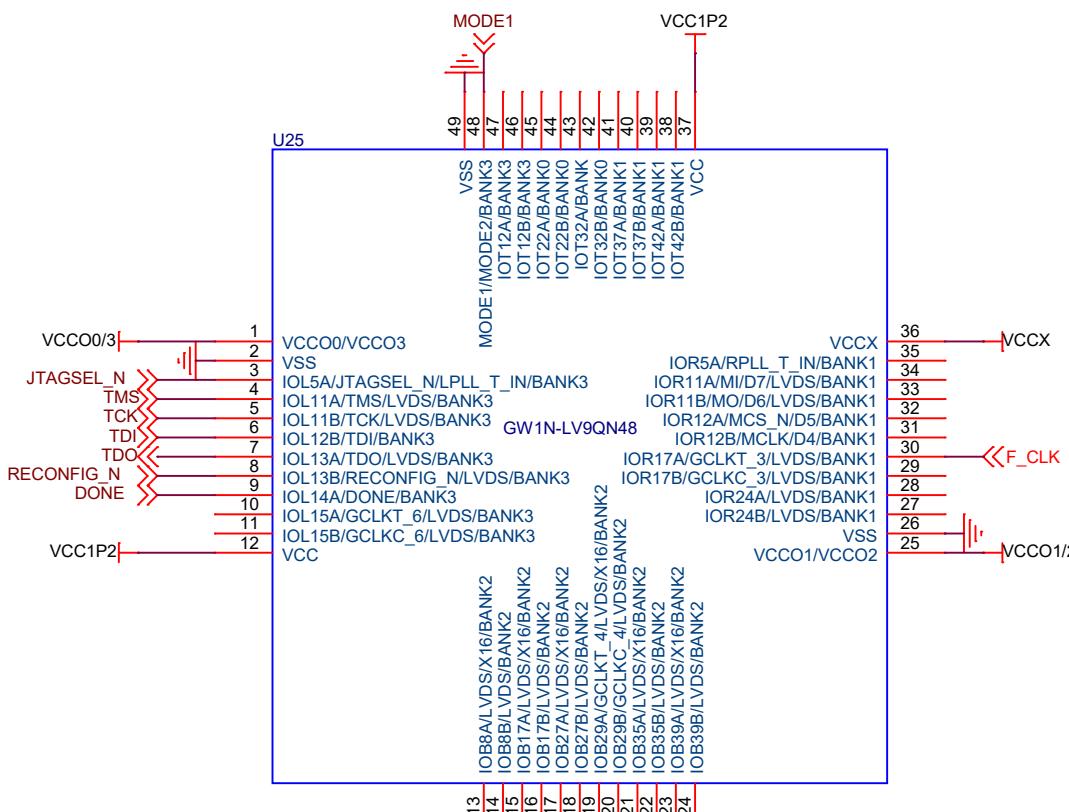


## Notes:

1. F CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		GOWIN Minimum System Diagram	
Size	Document Number	Rev	
B	GW1N-LV9PG256	2.0	
Date:	Friday, April 21, 2023	Sheet	12 of 32

# GW1N-LV9QN48



Title: GOWIN Minimum System Diagram

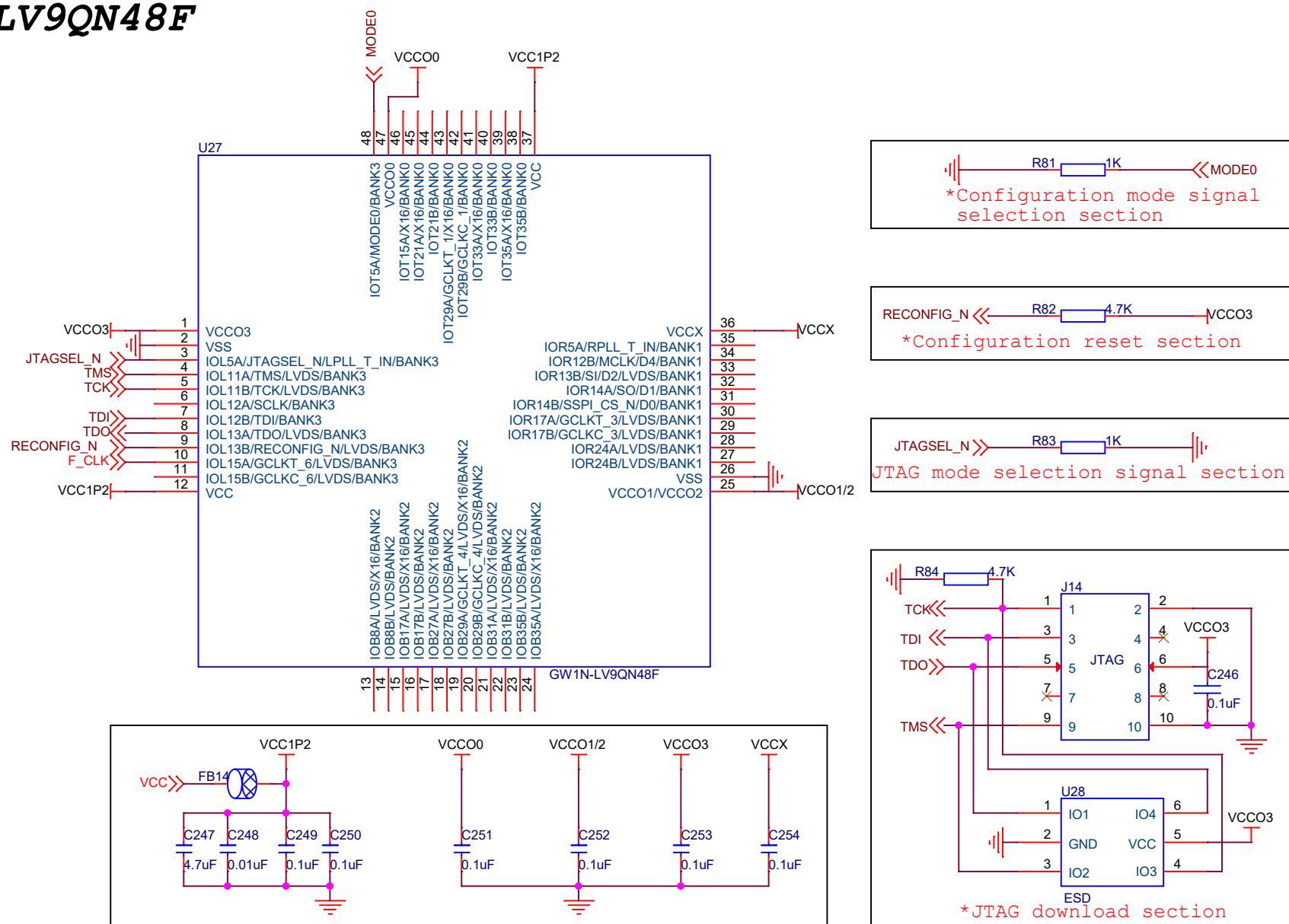
Size: A4 Document Number: GW1N-LV9QN48

Rev: 2.0

Date: Friday, April 21, 2023

Sheet 13 of 32

# GW1N-LV9QN48F



## Notes:

1. F\_CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.

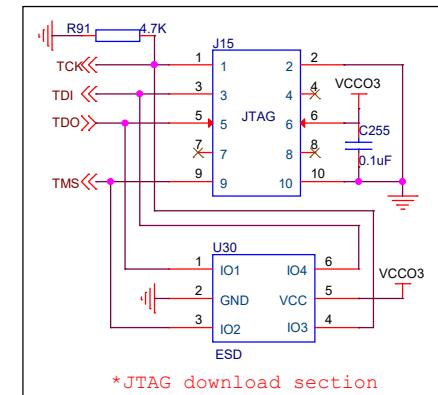
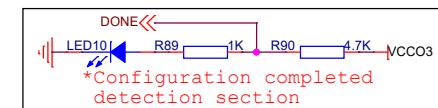
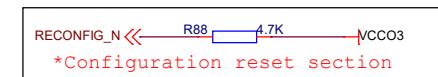
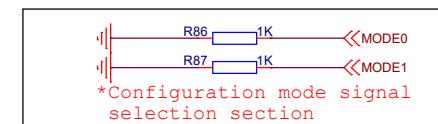
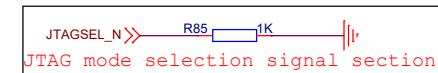
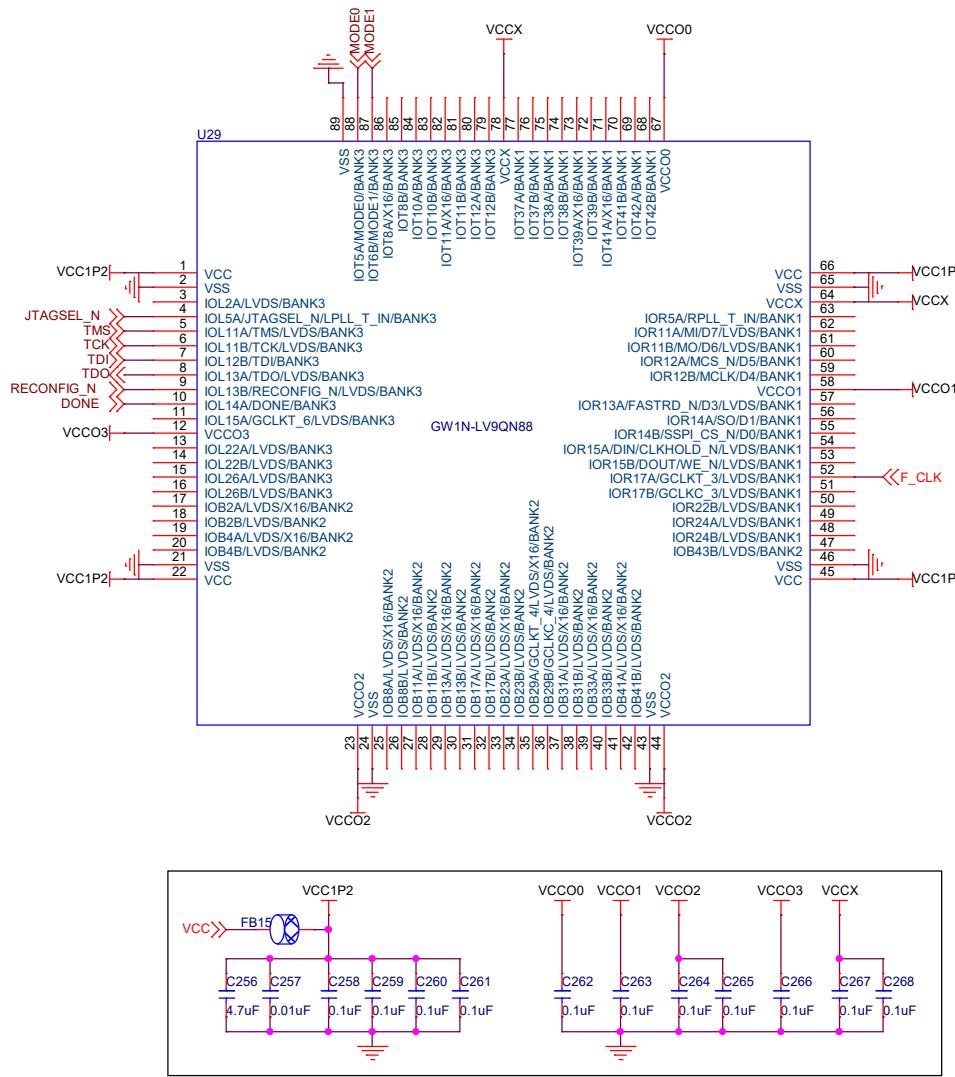
Title: GOWIN Minimum System Diagram

Size: A4 Document Number: GW1N-LV9QN48F

Rev: 2.0

Date: Friday, April 21, 2023

Sheet 14 of 32



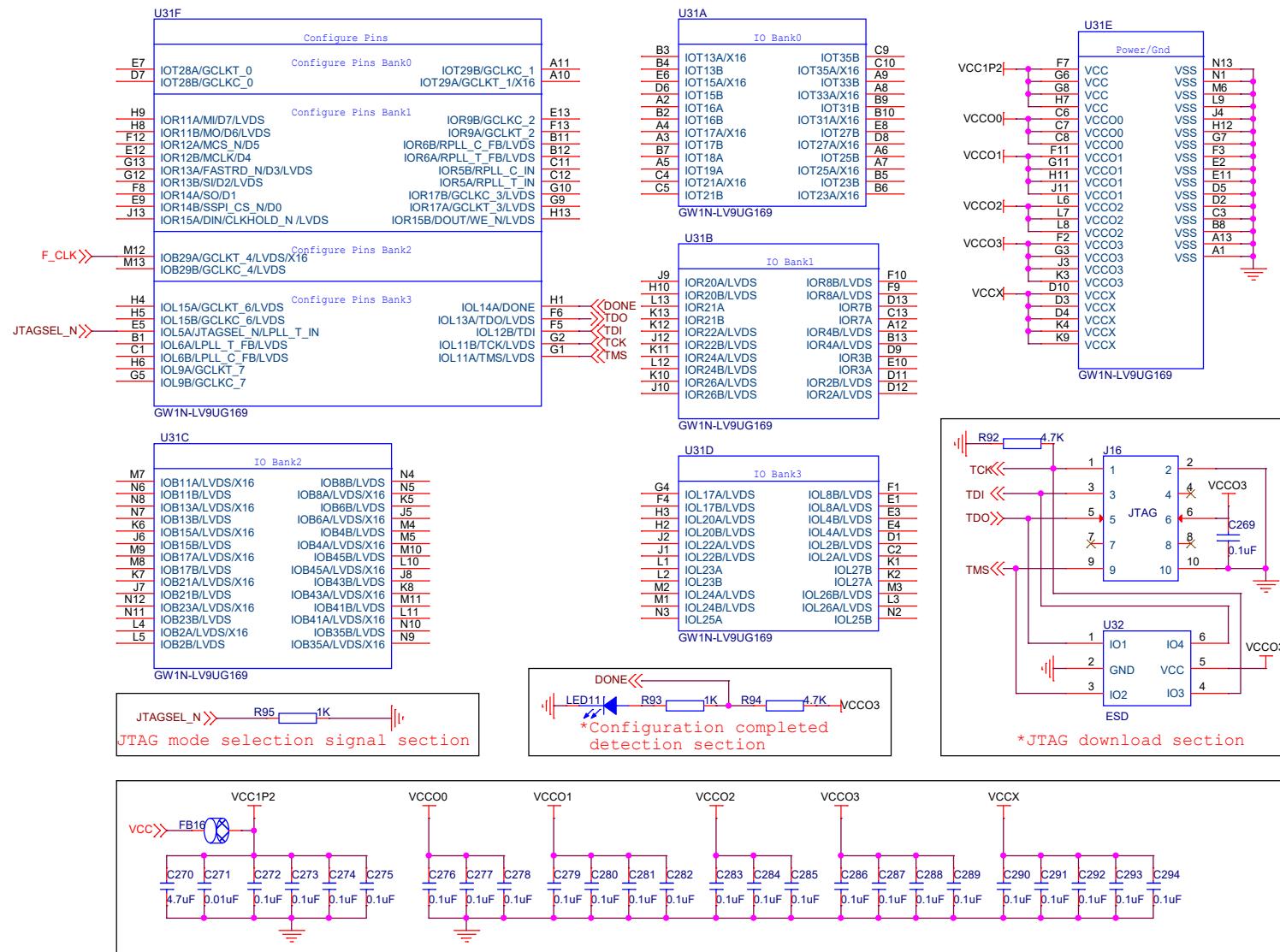
## Notes:

1. F\_CLK signal is an external input clock signal.

It is recommended that F\_CLK signal be provided through an active oscillator crystal.

2. It is recommended that add an ESD protection chip to the JTAG download circuit.

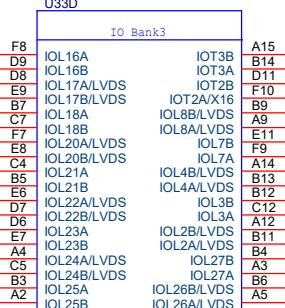
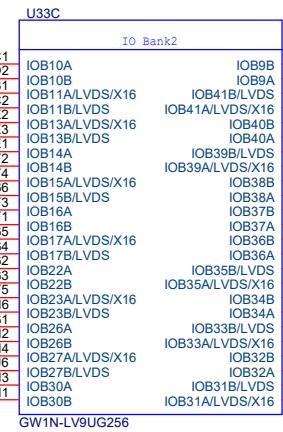
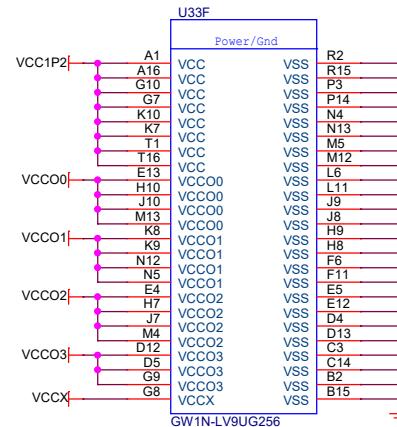
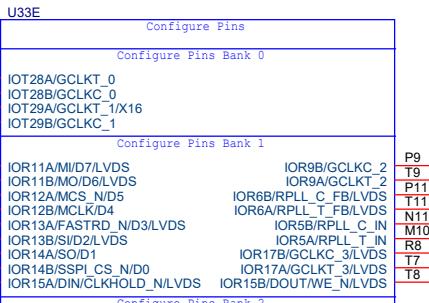
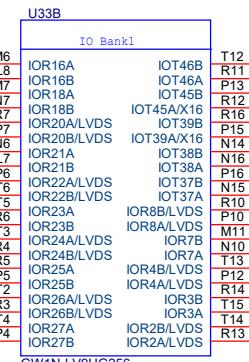
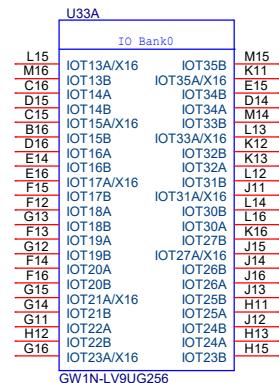
Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-LV9QN88	2.0
Date:	Friday, April 21, 2023	Sheet 15 of 32

**Notes:**

1. **F\_CLK** signal is an external input clock signal.  
It is recommended that **F\_CLK** signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.

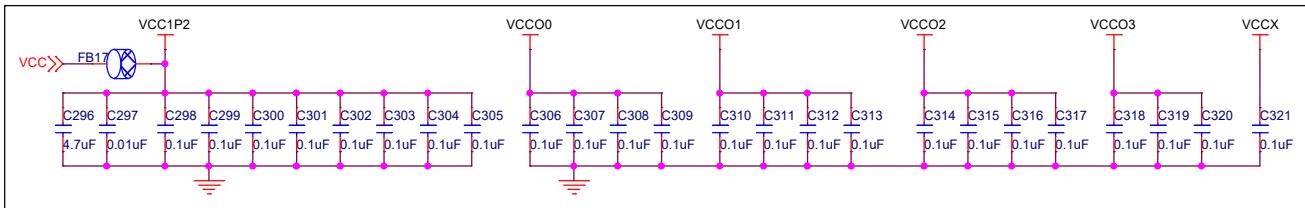
Title	
GOWIN Minimum System Diagram	
Size <b>B</b>	Document Number GW1N-LV9UG169
Rev 2.0	

Date: Friday, April 21, 2023 Sheet 16 of 32



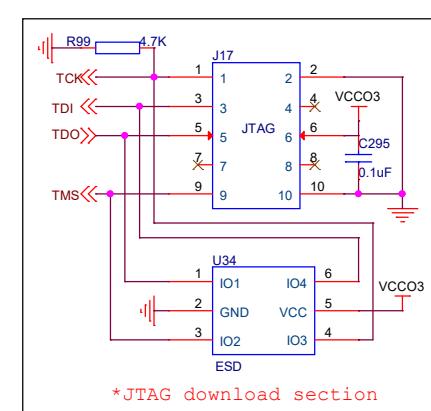
**RECONFIG\_N**  $\leftrightarrow$  R98  $4.7K$   $\rightarrow$  VCCO3  
*\*Configuration reset section*

**READY**  $\leftrightarrow$  R101  $4.7K$   $\rightarrow$  VCCO3  
*\*Configurable detection section*



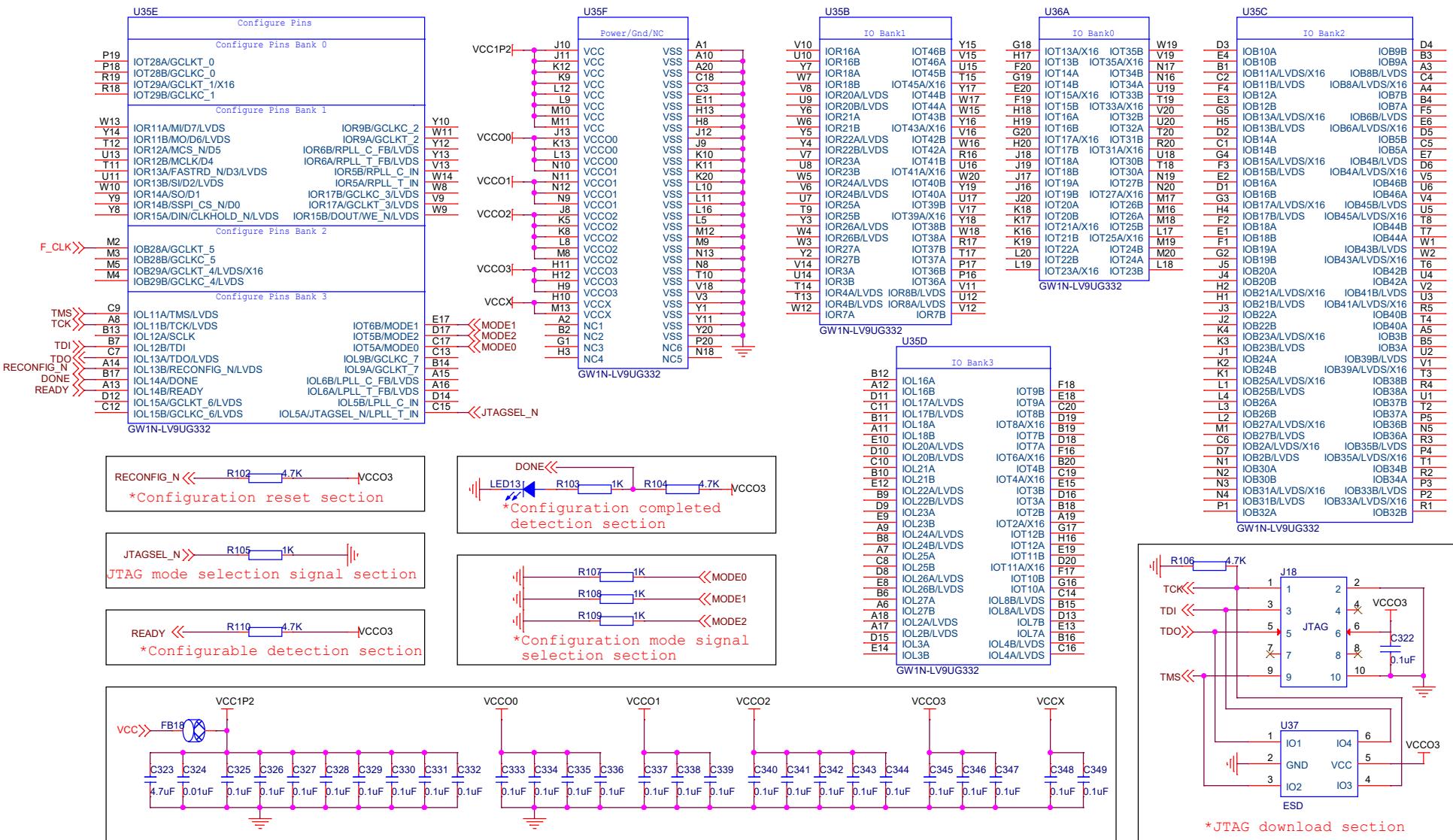
#### Notes:

1. F CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.



Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-LV9UG256	2.0

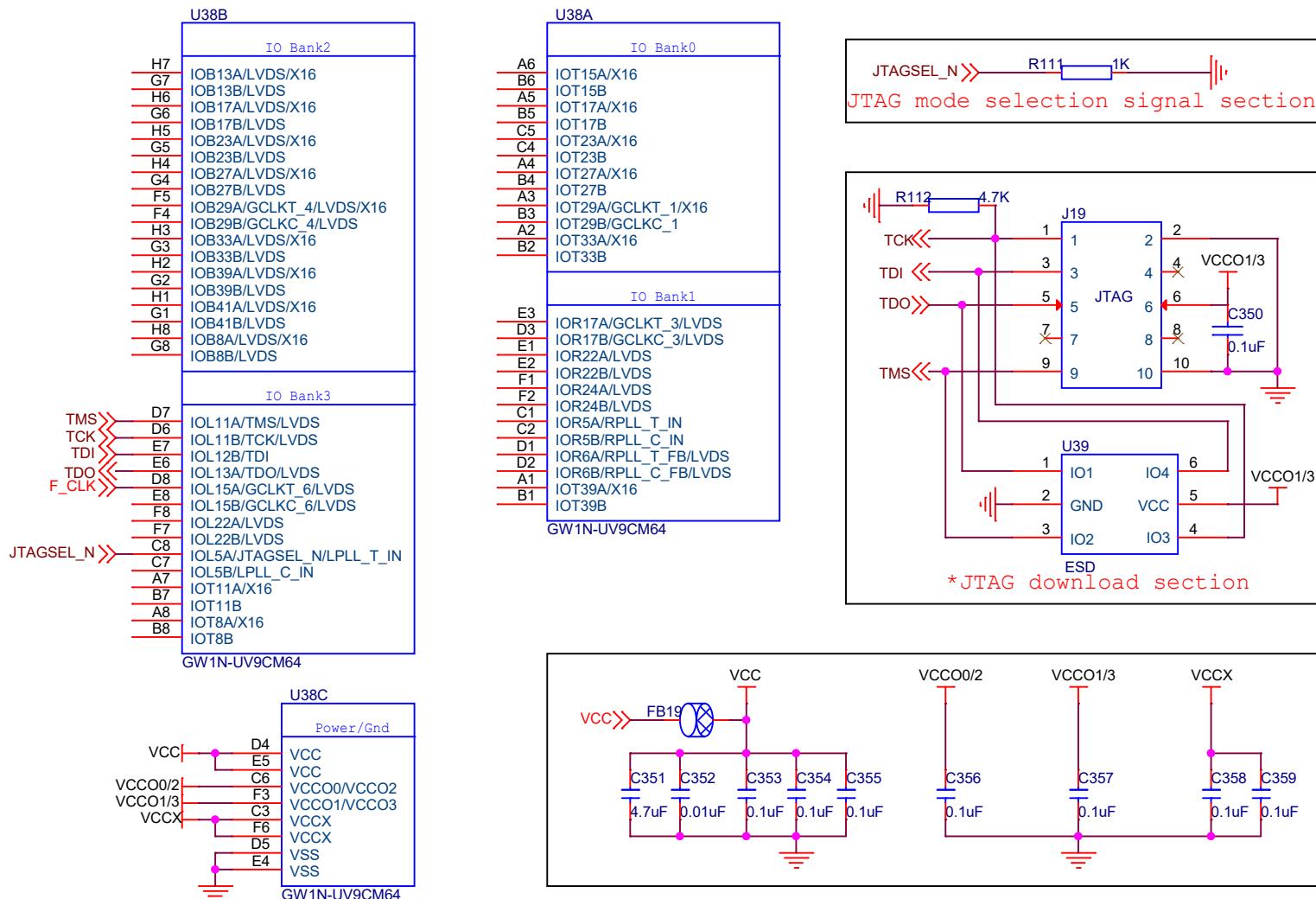
Date: Friday, April 21, 2023 Sheet 17 of 32

**Notes:**

1. F CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.

Title	
GOWIN Minimum System Diagram	
Size	Document Number
B	GW1N-LV9UG332
Rev	2.0
Date:	Friday, April 21, 2023
Sheet	18 of 32

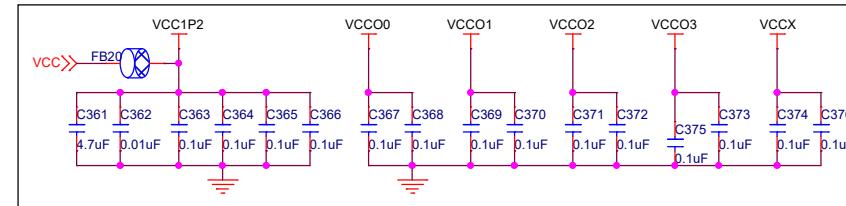
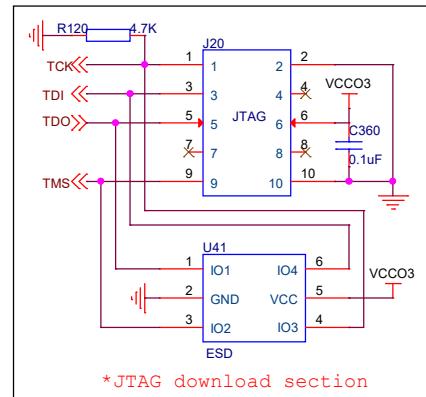
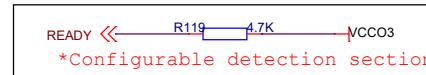
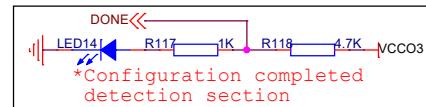
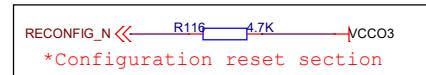
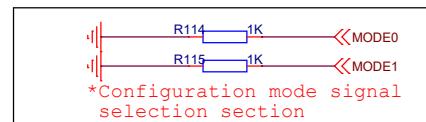
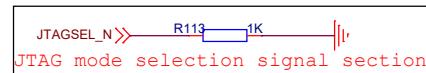
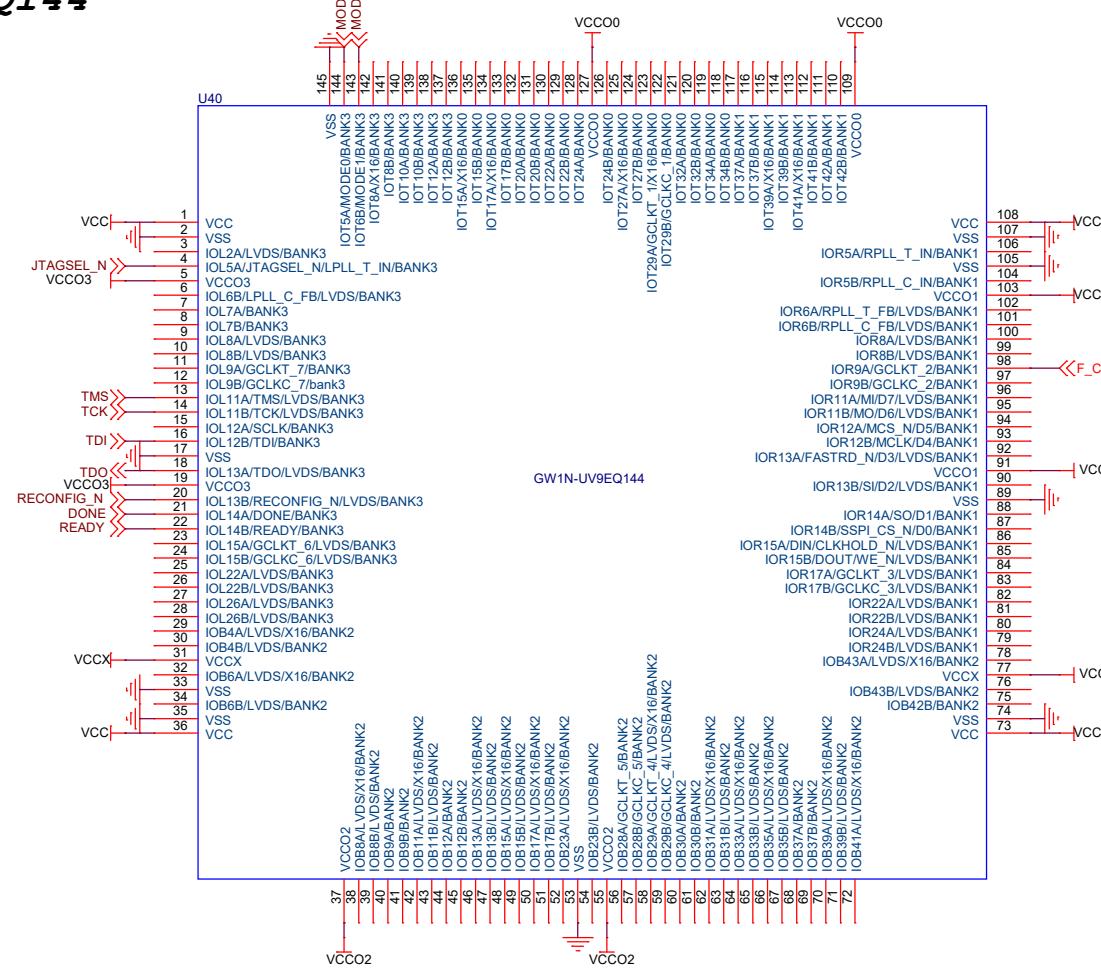
# GW1N-UV9CM64



## Notes:

1. F\_CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.

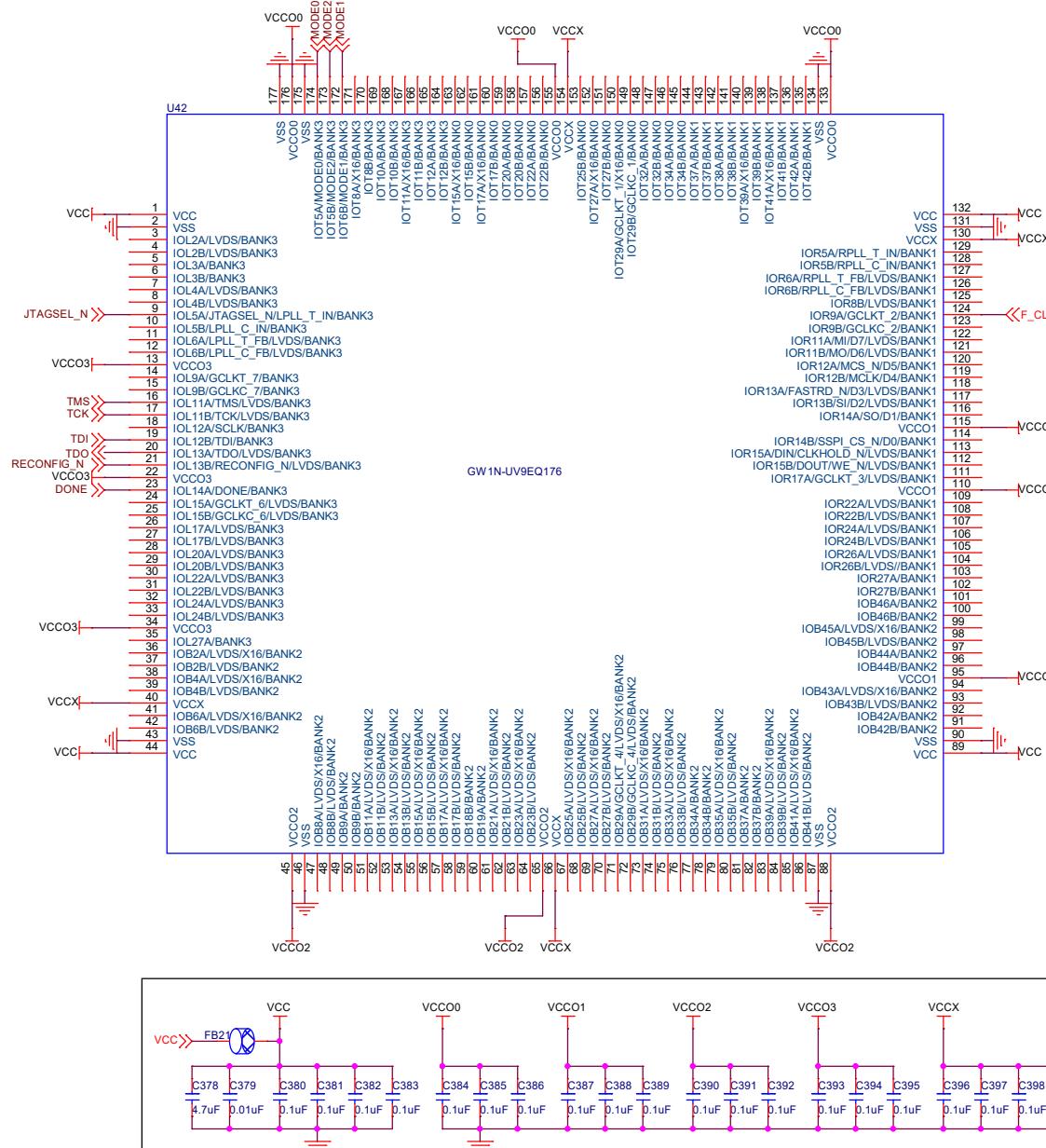
Title	
Size A4 Document Number GW1N-UV9CM64	
Date: Friday, April 21, 2023	Rev 2.0
Sheet 19 of 32	



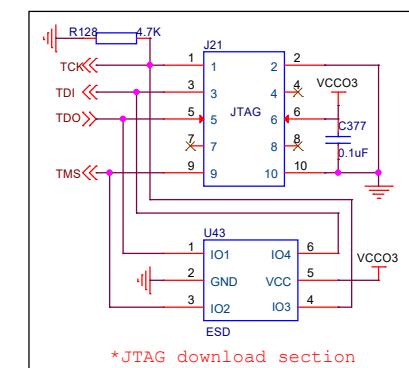
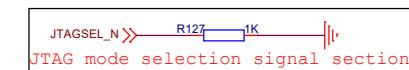
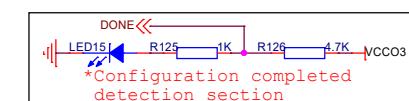
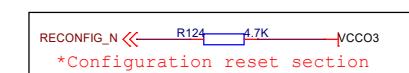
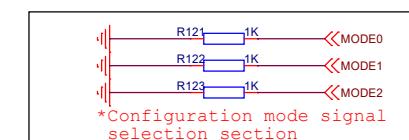
## Notes:

1. F\_CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.

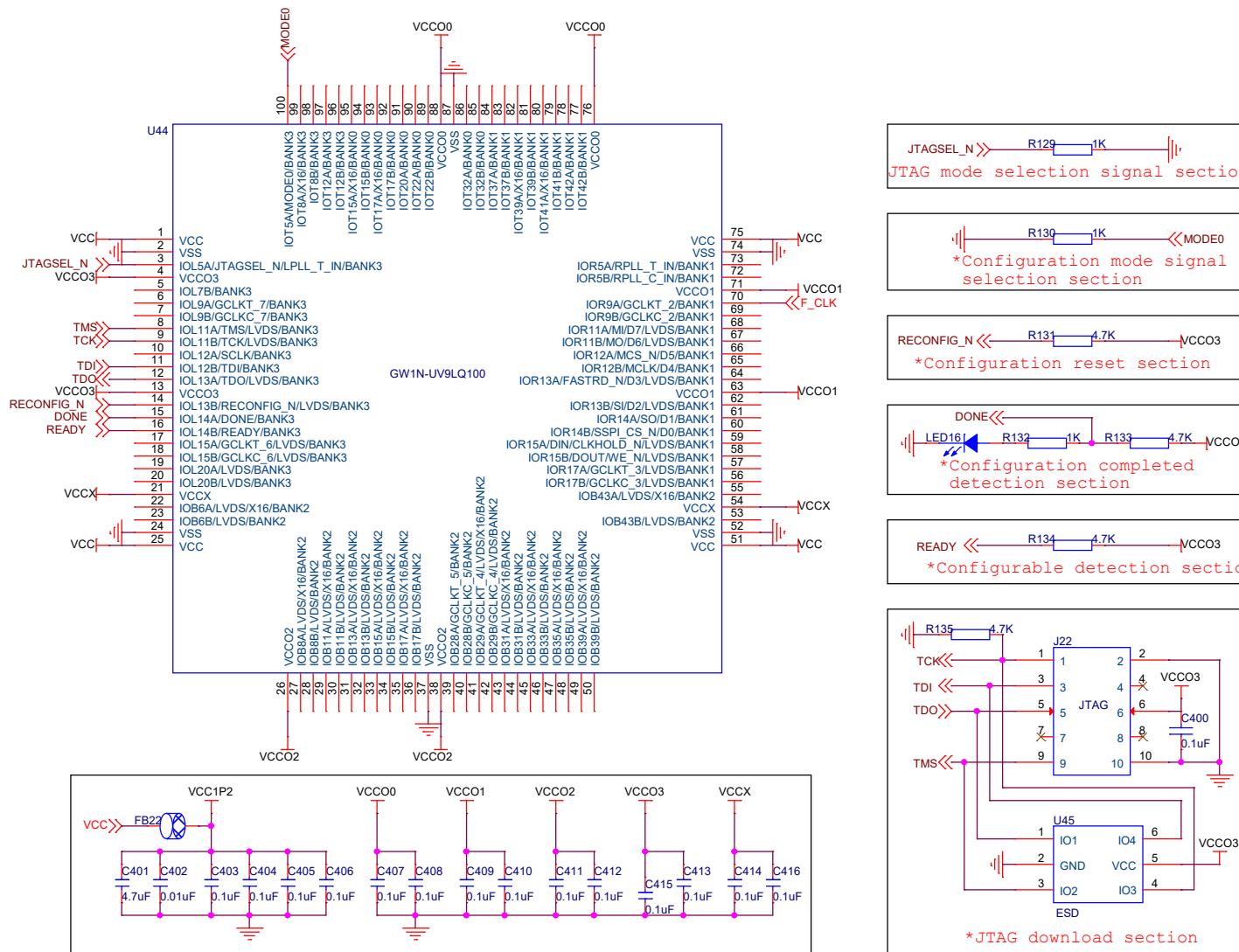
Title		GOWIN Minimum System Diagram
Size	Document Number	GW1N-UV9EQ144
B		Rev 2.0
Date: Friday, April 21, 2023	Sheet 20 of 32	

**Notes:**

- F CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.
- It is recommended that add an ESD protection chip to the JTAG download circuit.



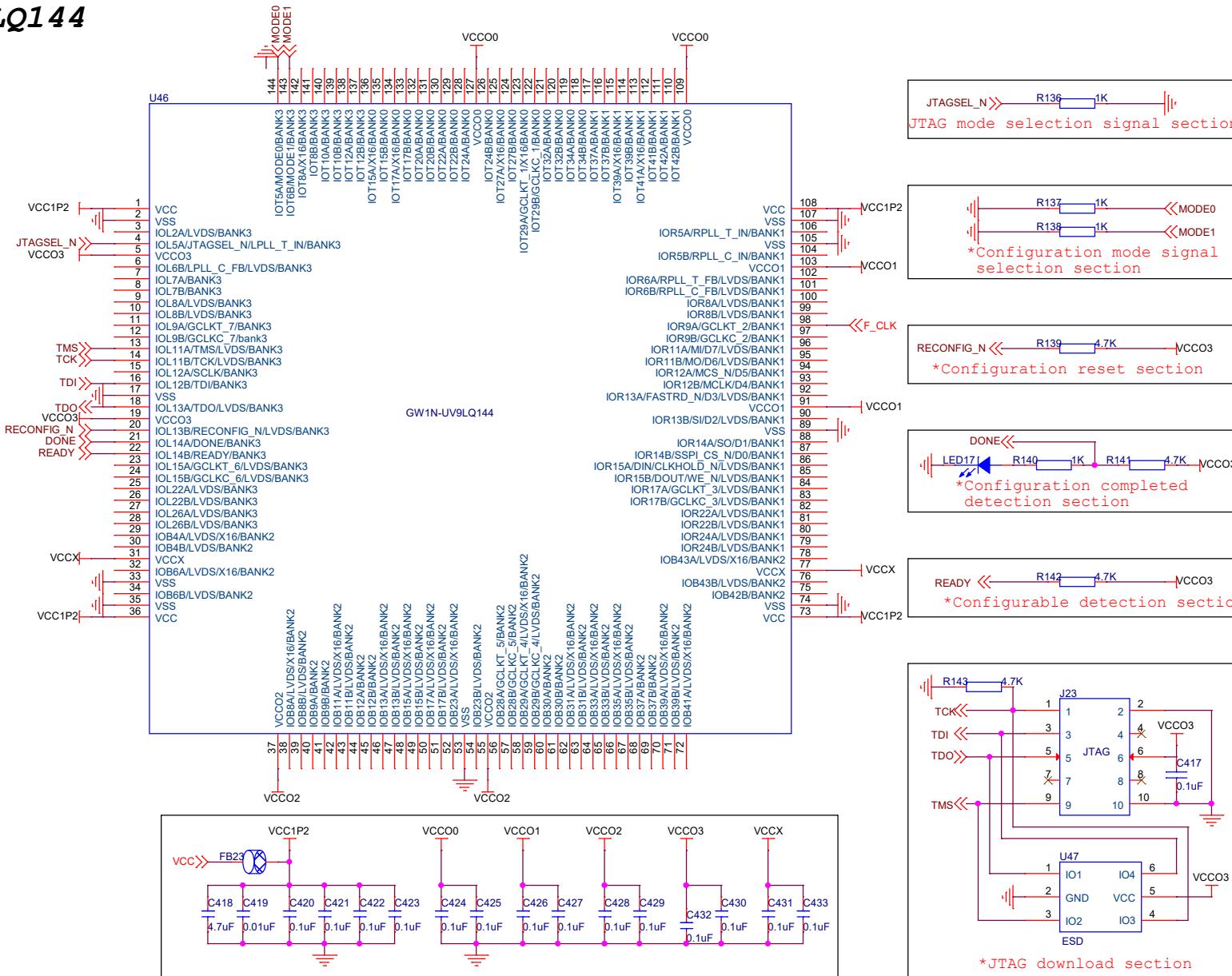
Title	
GOWIN Minimum System Diagram	
Size	Document Number
A3	GW1N-UV9EQ176
Date:	Friday, April 21, 2023
Rev	2.0



## Notes:

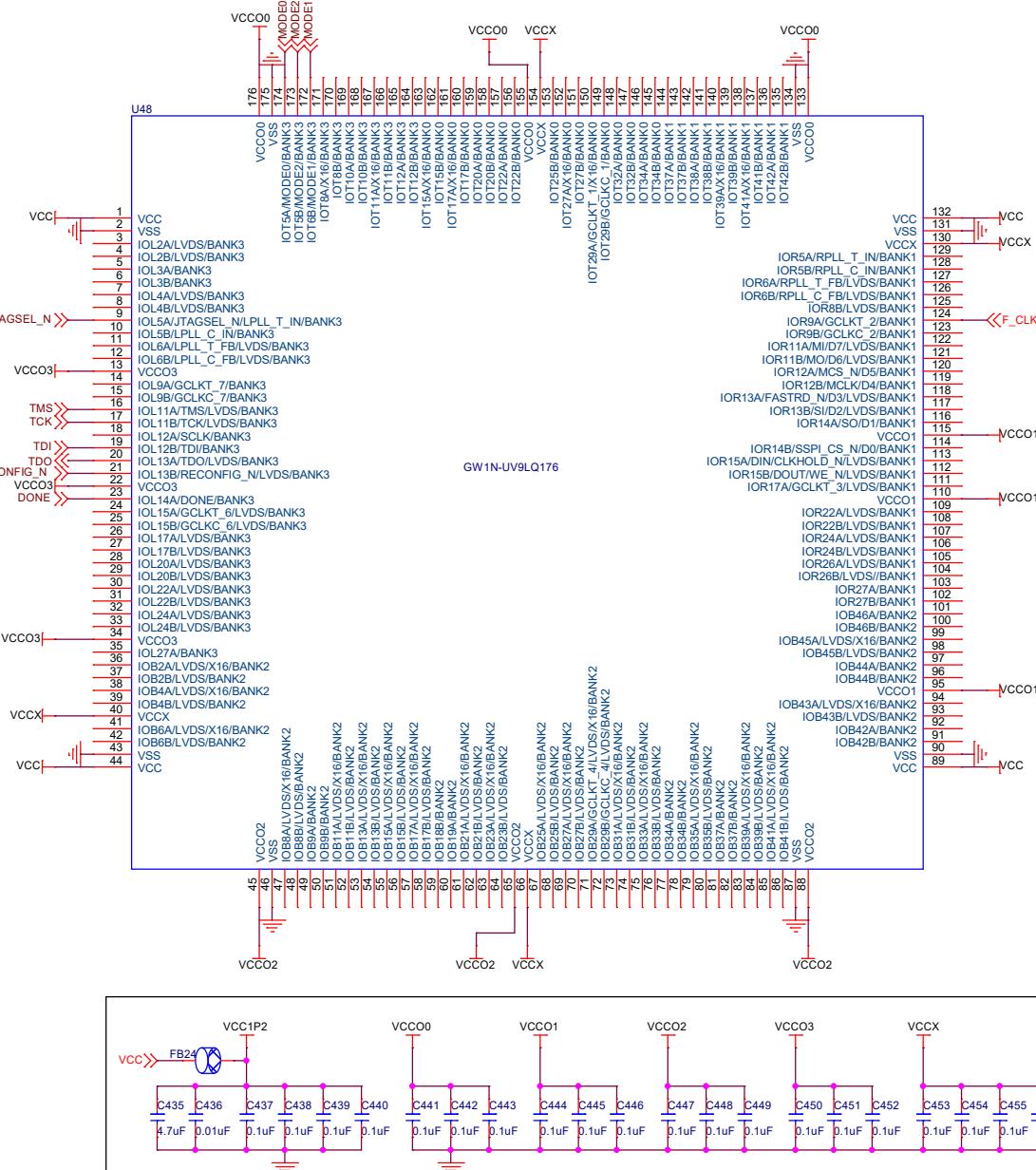
- F\_CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
- It is recommended that add an ESD protection chip to the JTAG download circuit.

Title	
GOWIN Minimum System Diagram	
Size B	Document Number GW1N-UV9LQ100
Rev 2.0	Date: Friday, April 21, 2023

**Notes:**

1. F\_CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		GOWIN Minimum System Diagram
Size		Document Number GW1N-UV9LQ144
Sheet	23	Rev 2.0
Date:	Friday, April 21, 2023	



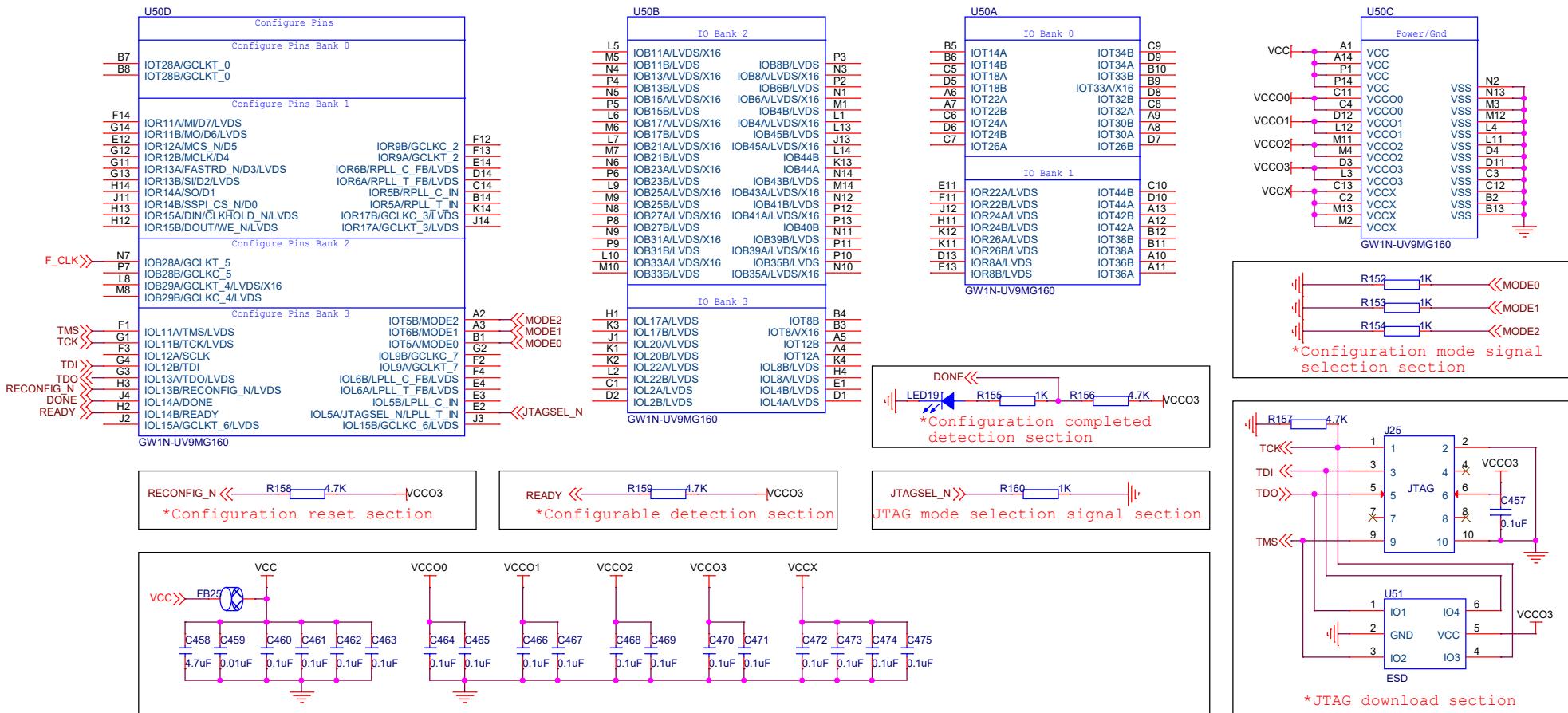
## Notes:

1. F\_CLK signal is an external input clock signal.

It is recommended that F\_CLK signal be provided through an active oscillator crystal.

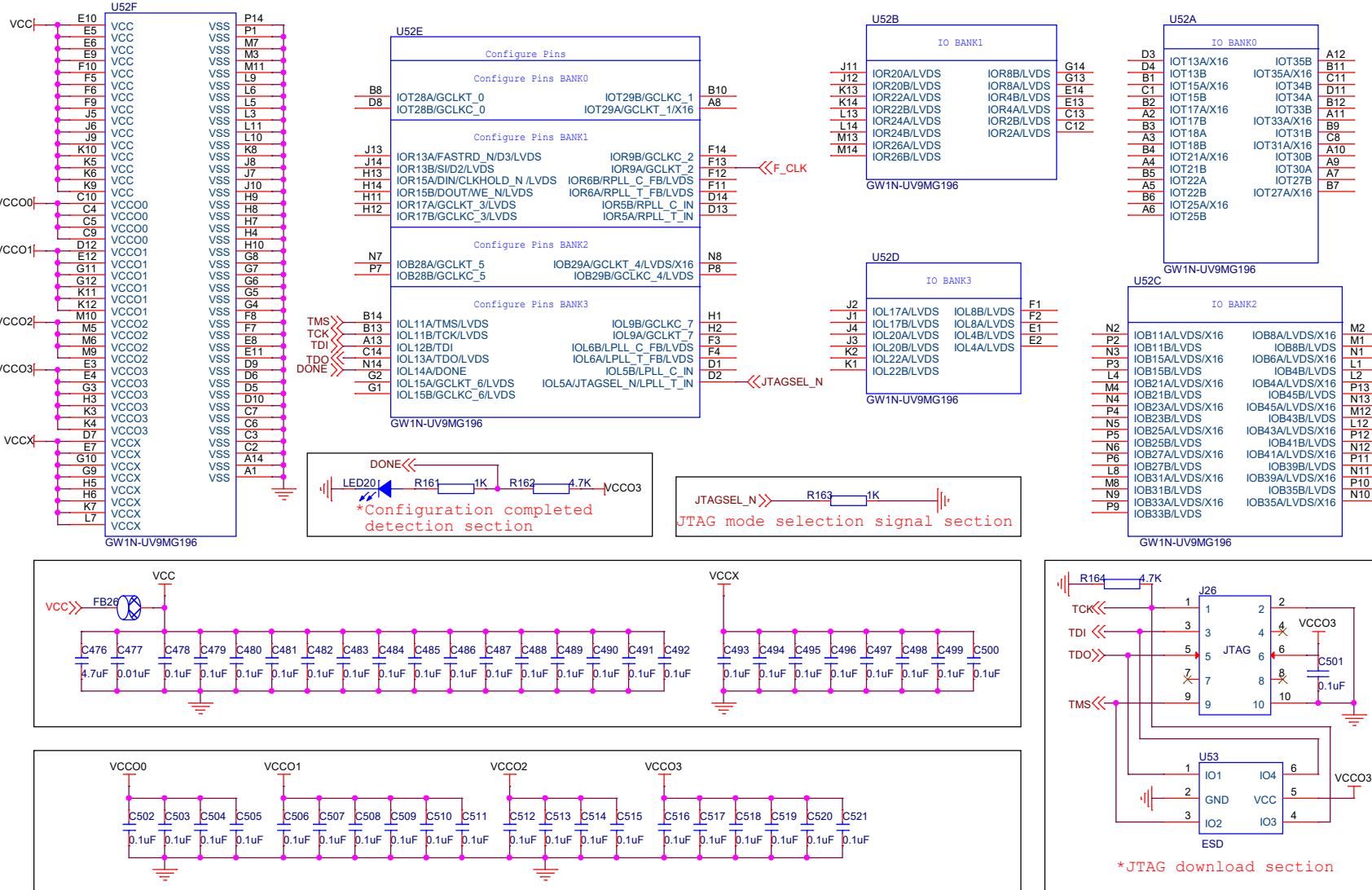
2. It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		GW1N Minimum System Diagram	
Size	Document Number		
		Date:	Rev
A3	GW1N-UV9LQ176	Friday, April 21, 2023	2.0

**Notes:**

1. F CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-UV9MG160	2.0
Date:	Friday, April 21, 2023	Sheet 25 of 32

**Notes:**

1. F\_CLK signal is an external input clock signal.

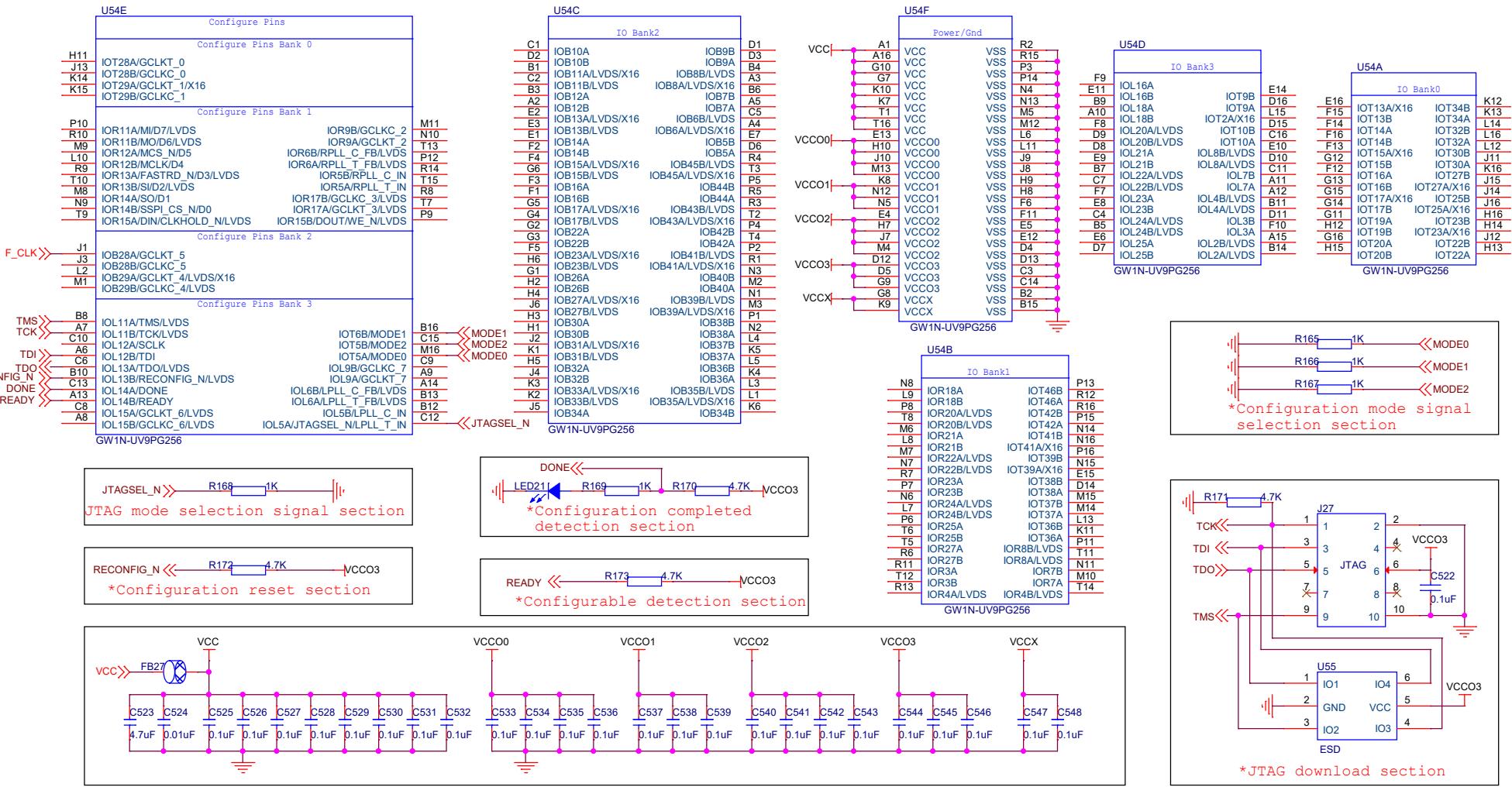
It is recommended that F\_CLK signal be provided through an active oscillator crystal.

2. It is recommended that add an ESD protection chip to the JTAG download circuit.

Title	
GOWIN Minimum System Diagram	

Size	Document Number	Rev
B	GW1N-UV9MG196	2.0

Date:	Friday, April 21, 2023	Sheet	26	of	32
-------	------------------------	-------	----	----	----

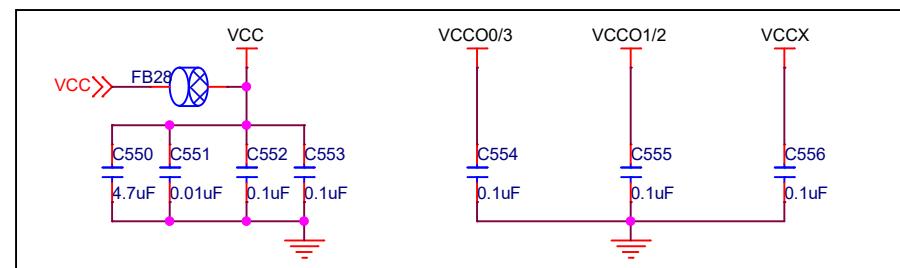
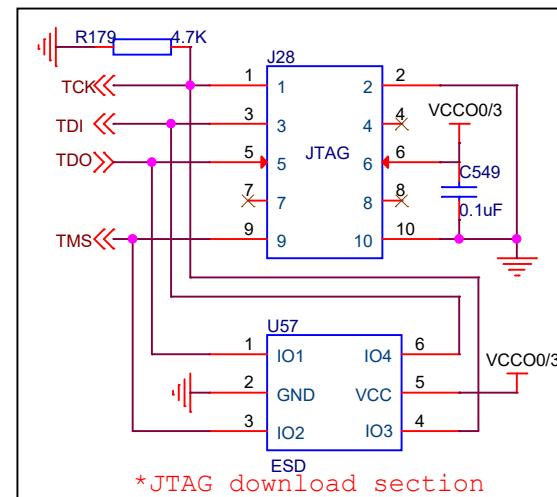
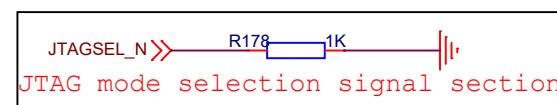
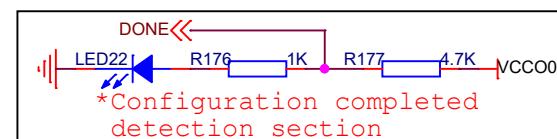
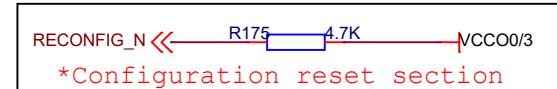
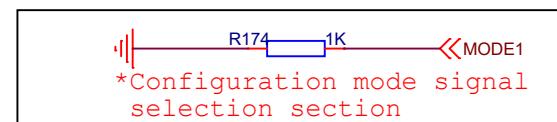
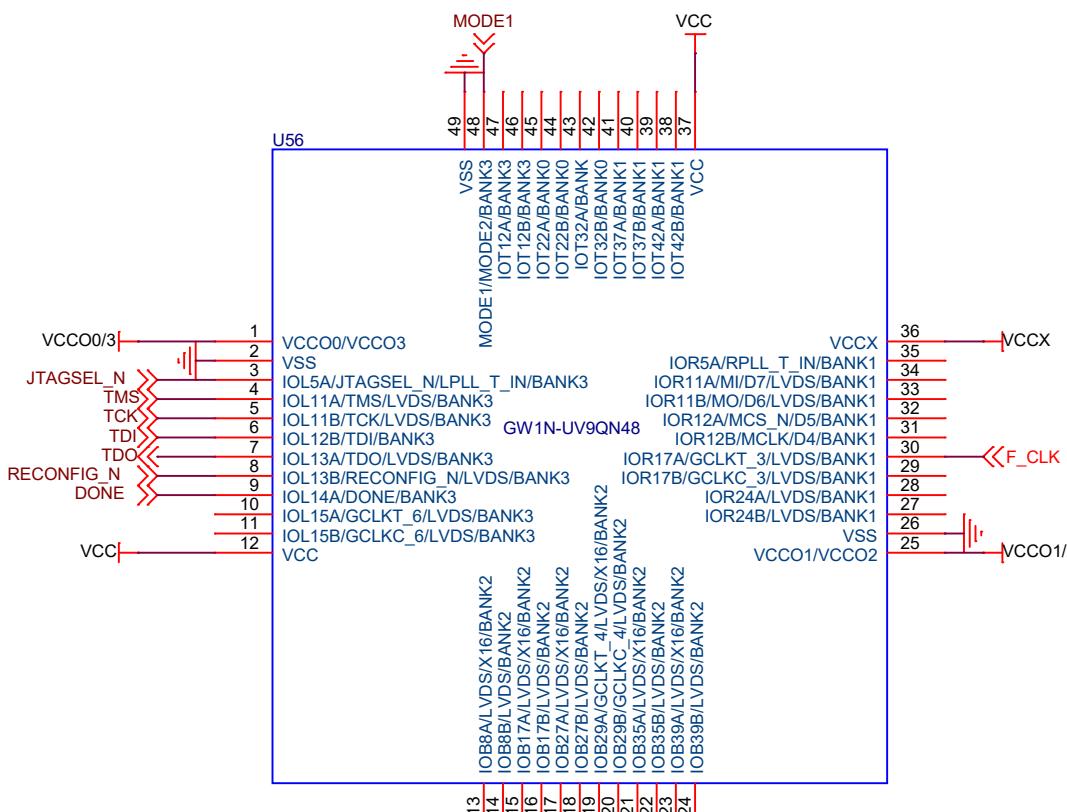


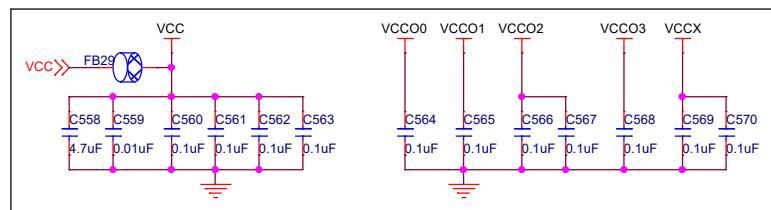
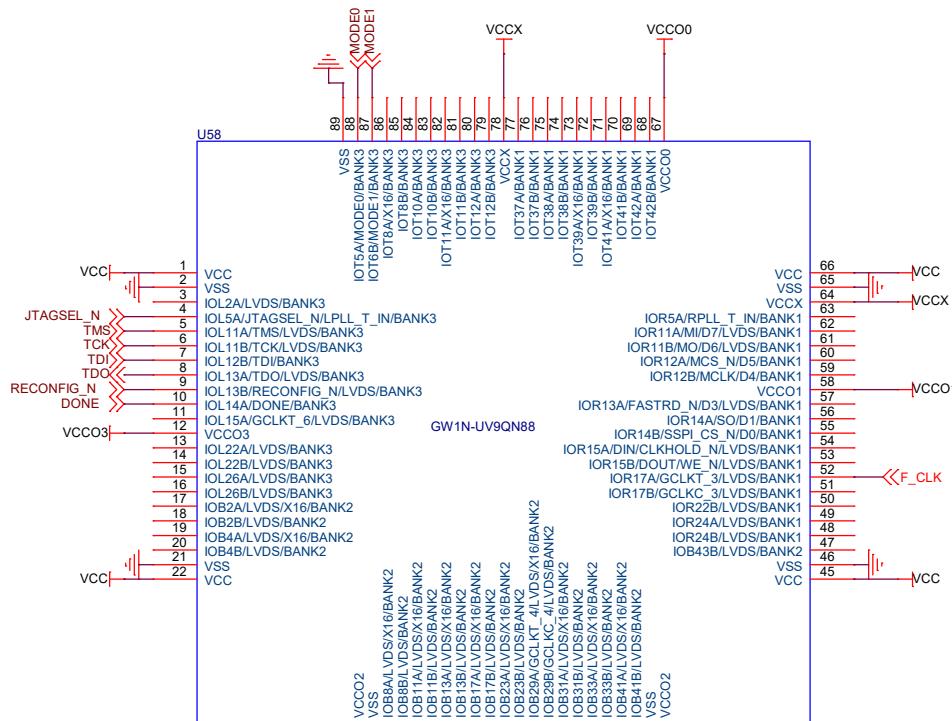
## Notes:

- F CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.
- It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-UV9PG256	2.0
Date:	Friday, April 21, 2023	Sheet 27 of 32

# GW1N-UV9QN48

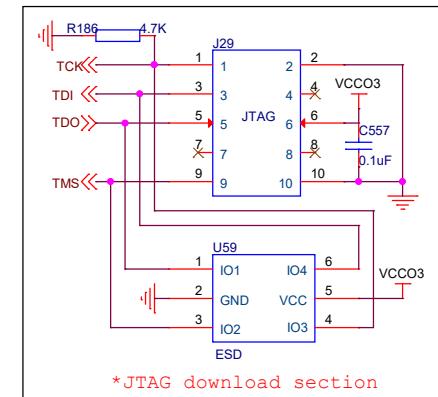
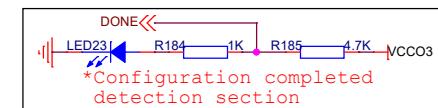
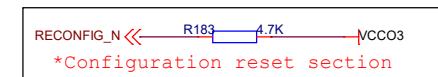
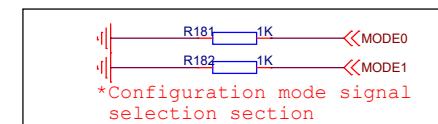
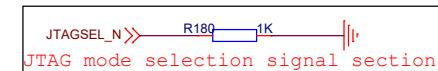


**Notes:**

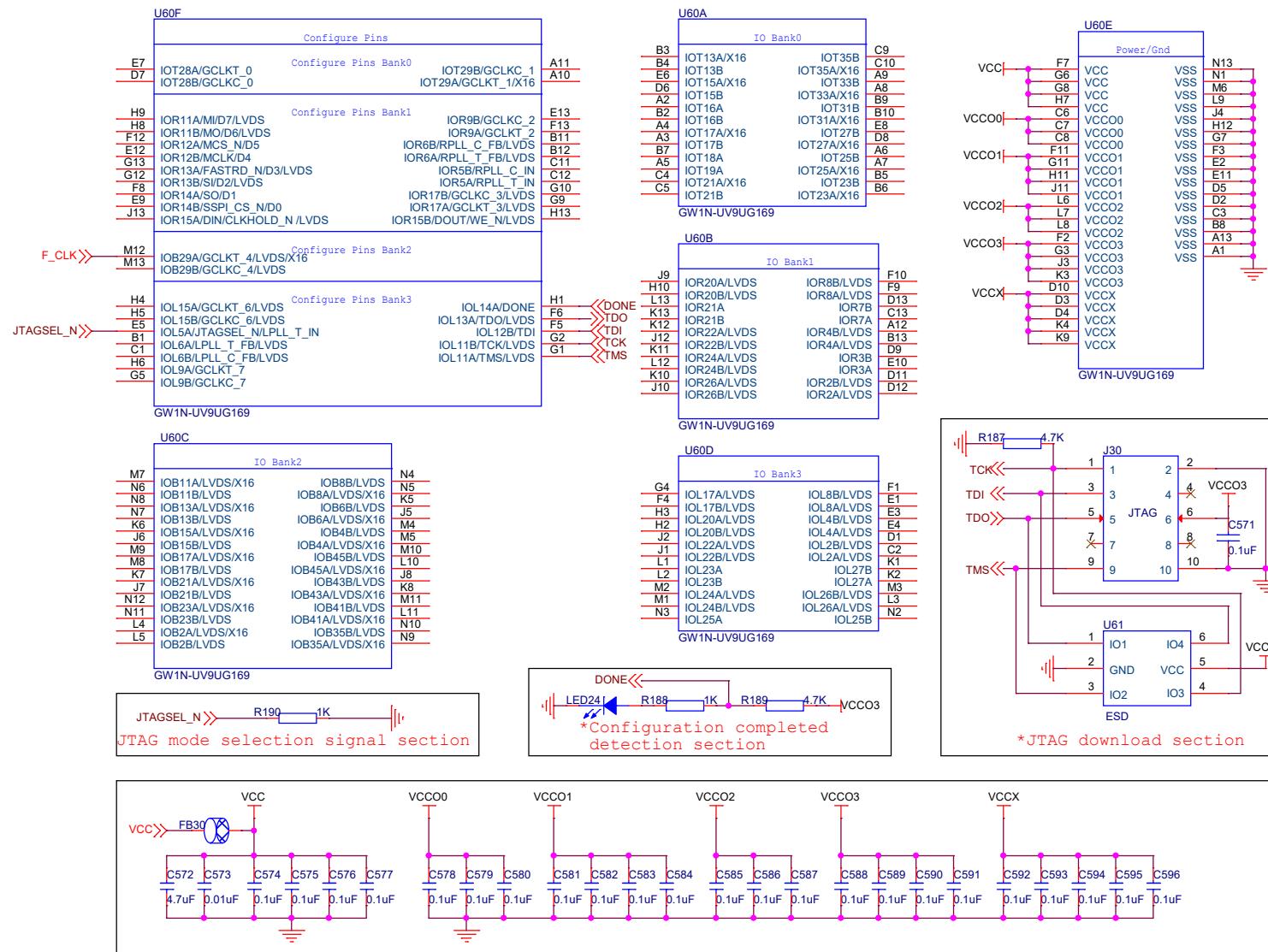
1. F\_CLK signal is an external input clock signal.

It is recommended that F\_CLK signal be provided through an active oscillator crystal.

2. It is recommended that add an ESD protection chip to the JTAG download circuit.



Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-UV9QN88	2.0
Date:	Friday, April 21, 2023	Sheet 29 of 32

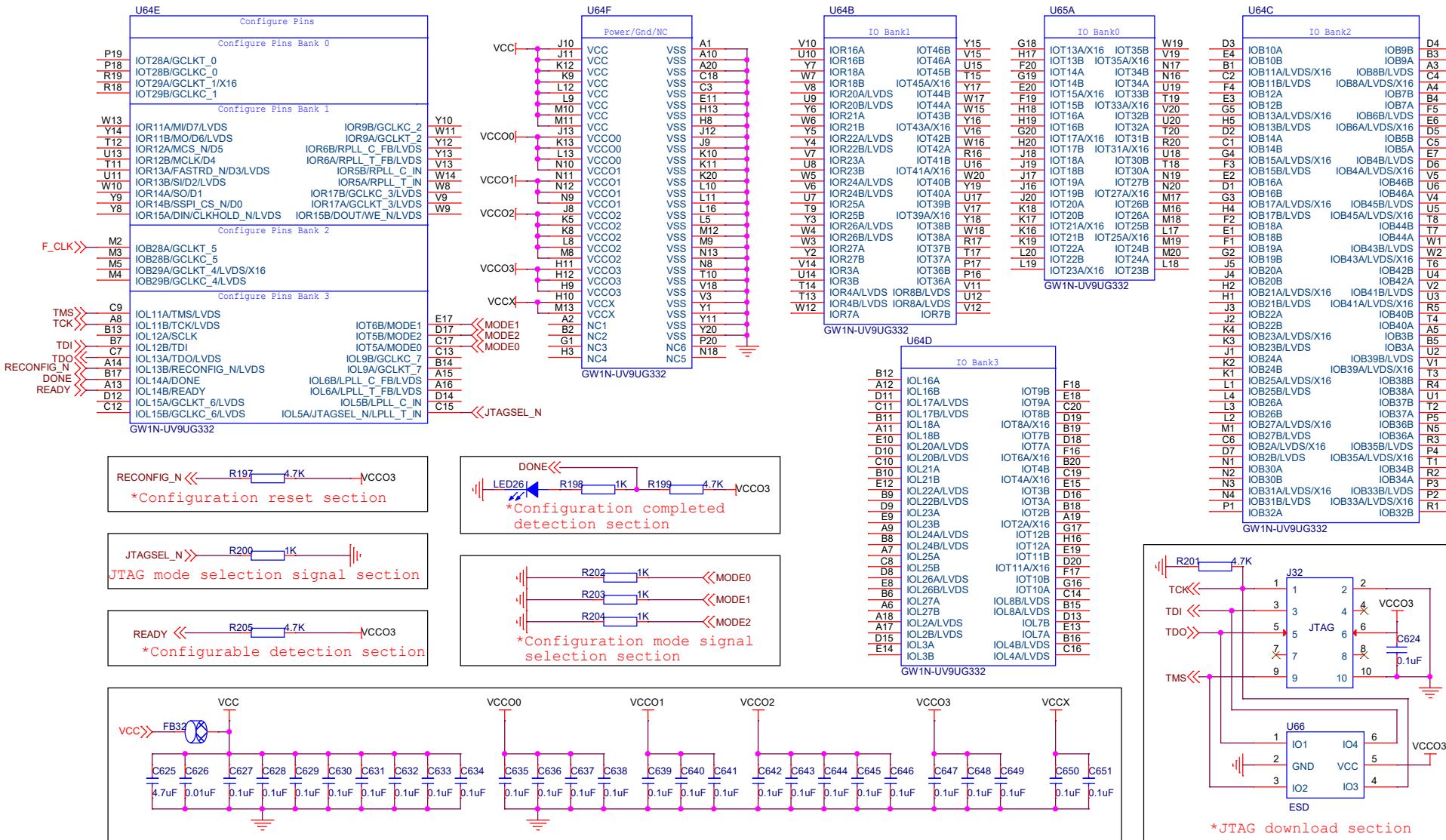
**Notes:**

1. F\_CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.

Title	
GOWIN Minimum System Diagram	
Size B	Document Number GW1N-UV9UG169
Rev 2.0	

Date: Friday, April 21, 2023 Sheet 30 of 32





## Notes:

1. F CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.

Title	
GOWIN Minimum System Diagram	
Size	Document Number GW1N-UV9UG332
B	Rev 2.0

Date: Friday, April 21, 2023 Sheet 32 of 32