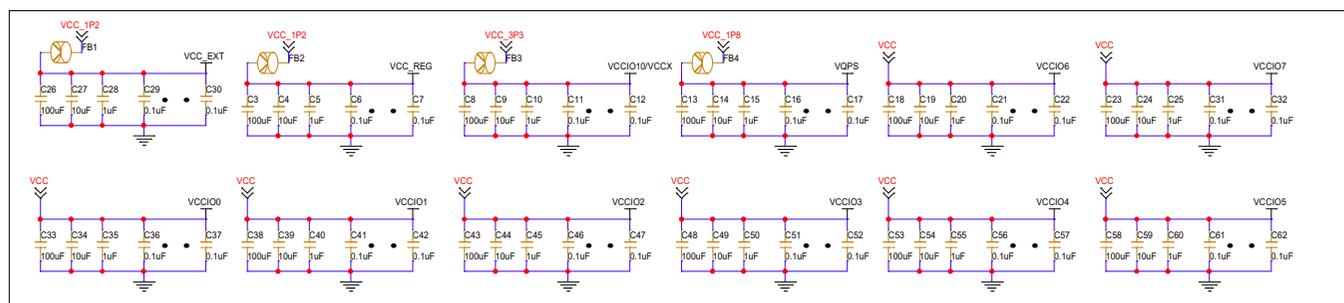
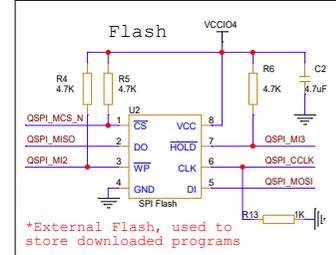
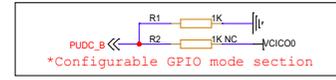
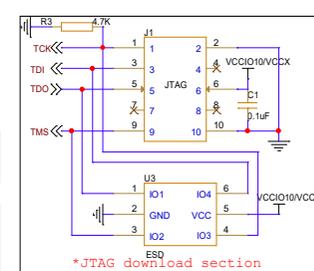
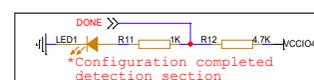
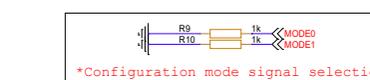
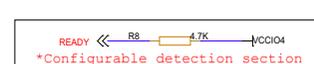
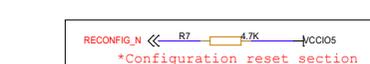
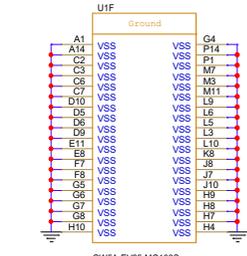
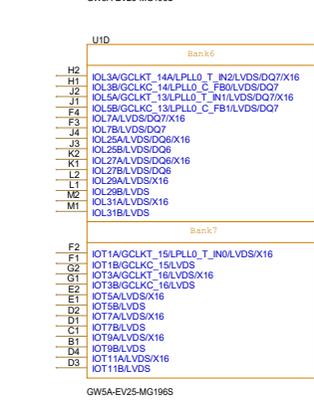
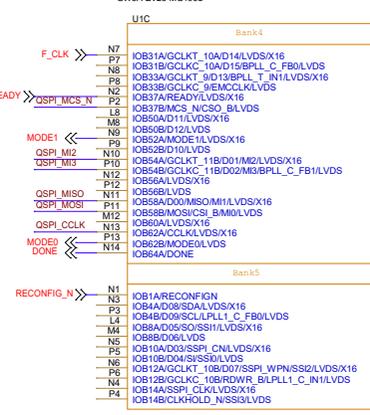
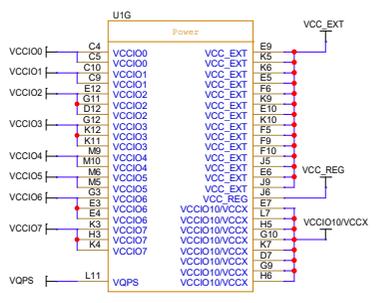
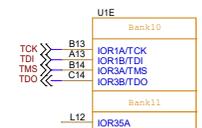
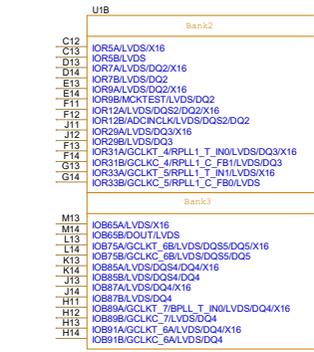
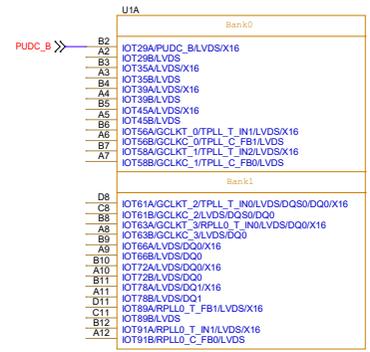
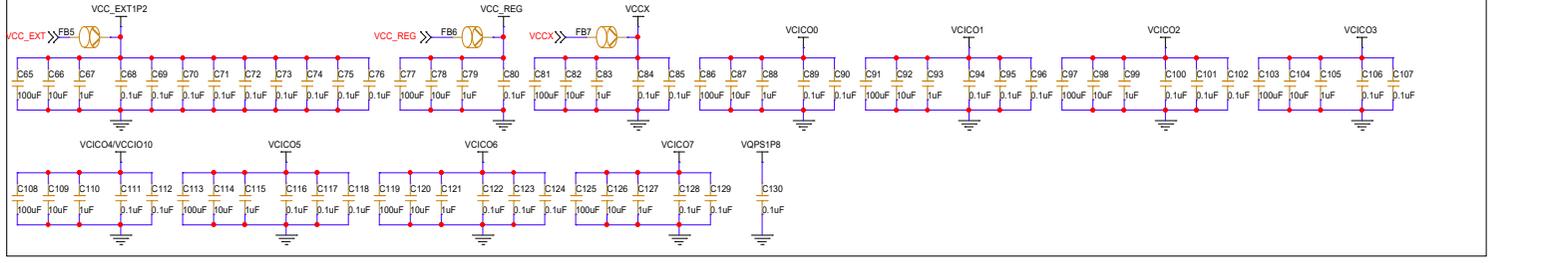
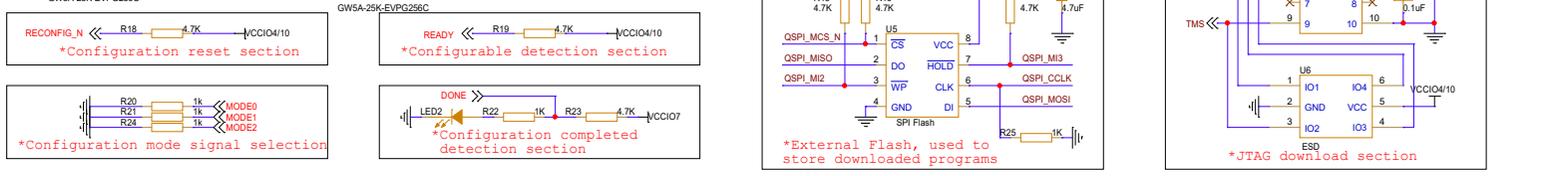
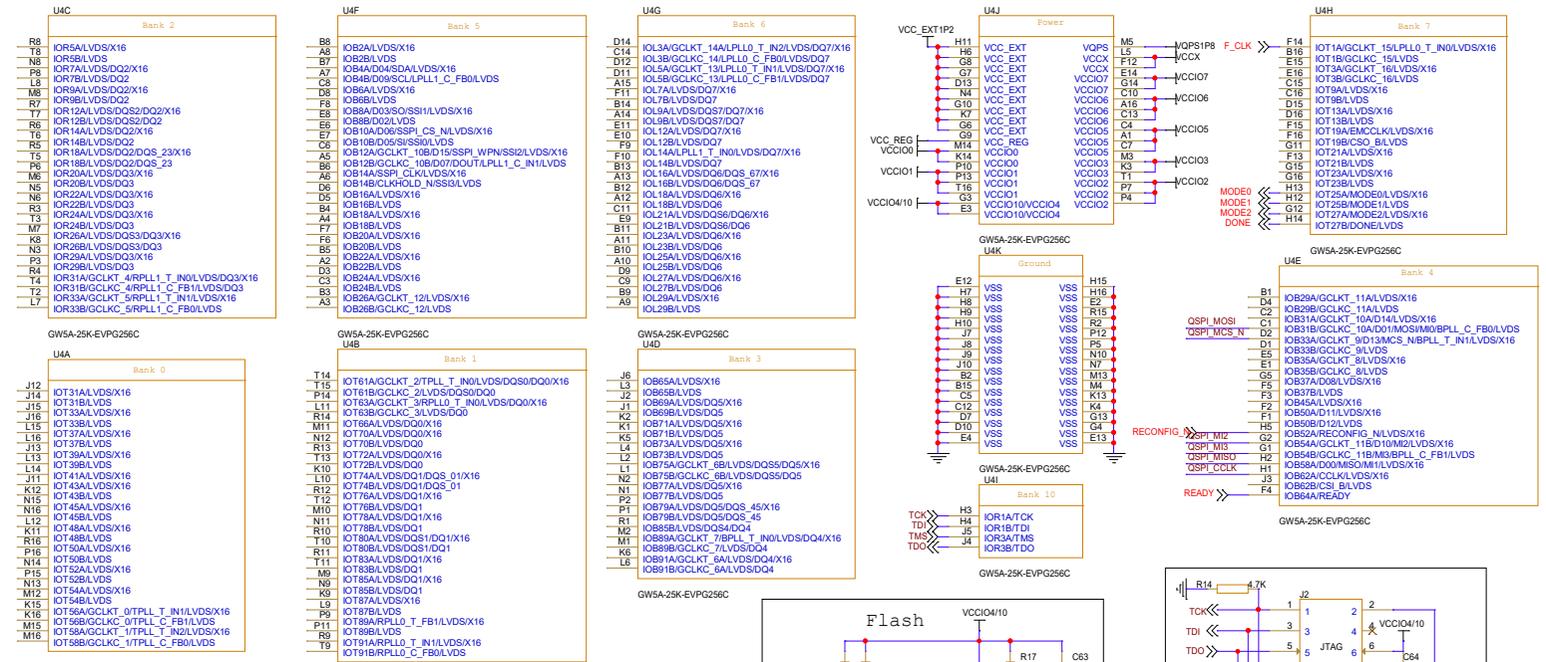


# GW5A-EV25MG196S

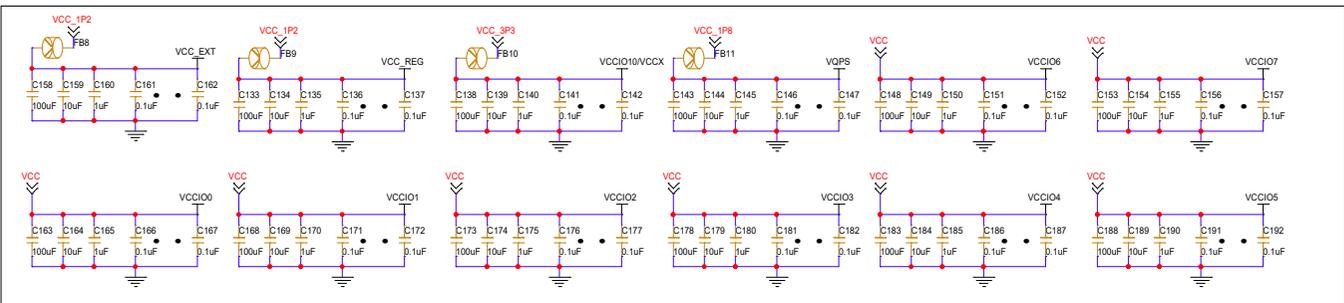
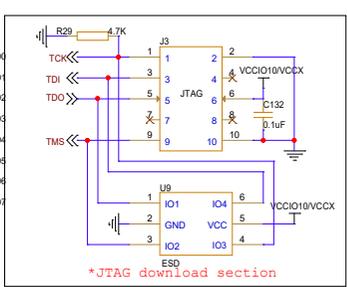
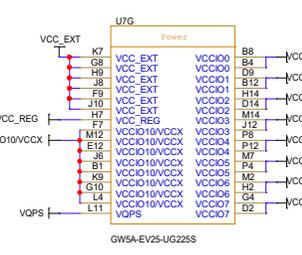
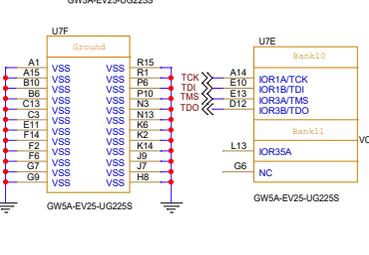
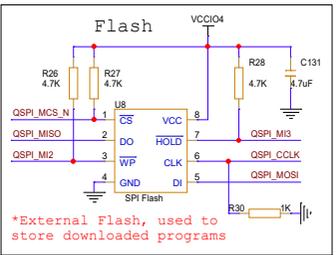
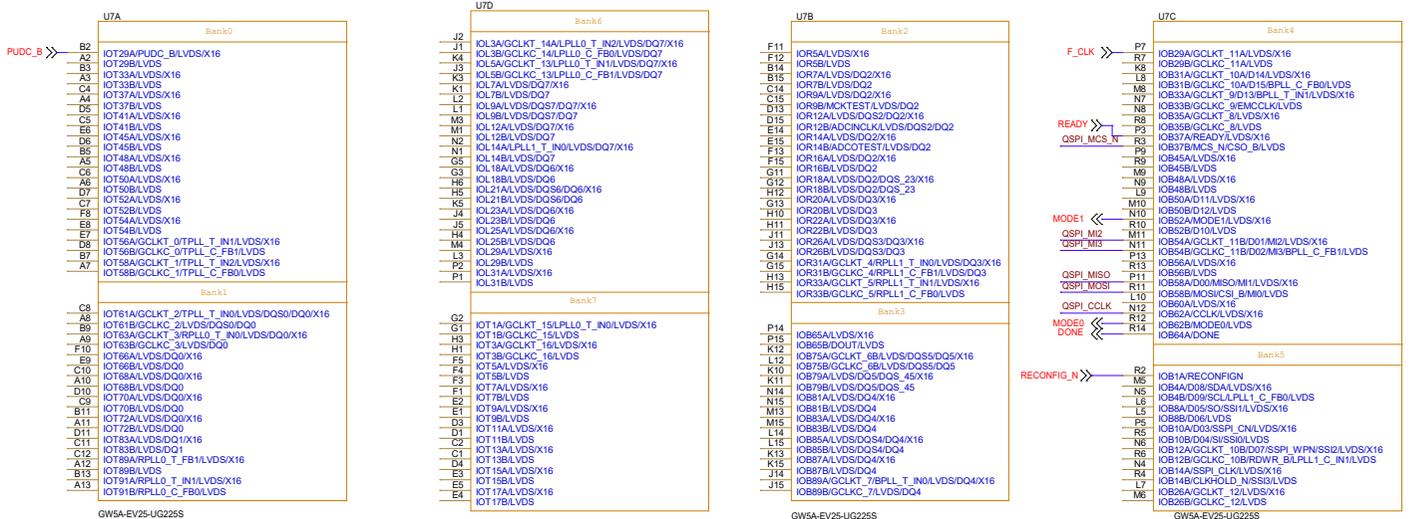


- Notes:
1. F\_CLK signal is an external input clock signal. It is recommended that F\_CLK signal be provided through an active oscillator crystal.
  2. External Flash memory is used to store downloaded programs. For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
  3. It is recommended that add an ESD protection chip to the JTAG download circuit.
  4. VCC core voltage requires a large current, so it is recommended to supply power separately.

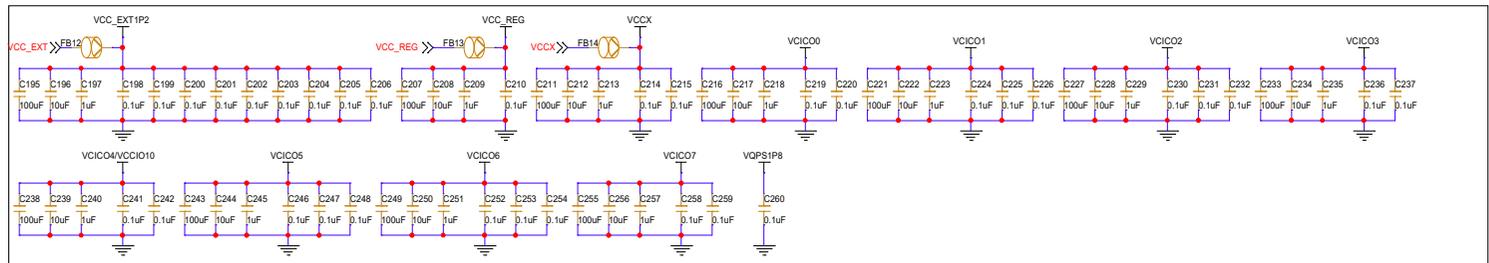
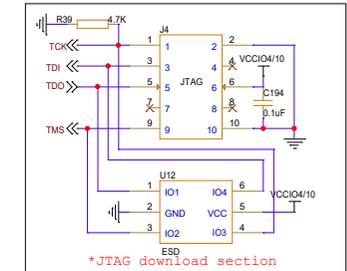
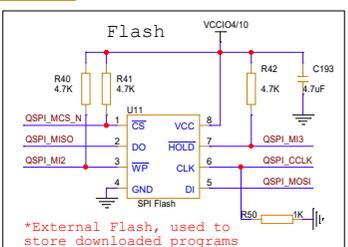
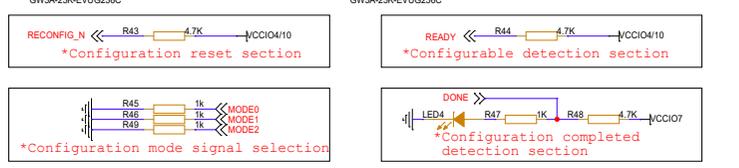
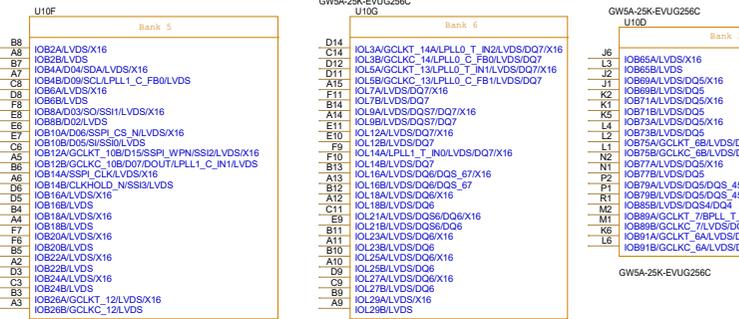
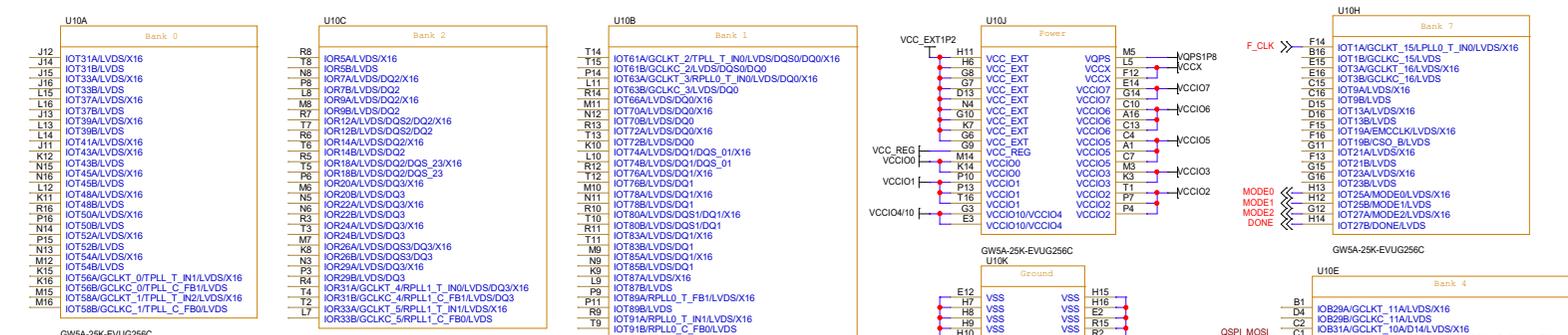
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Date	Thursday, May 25, 2023	Sheet	1 of 11



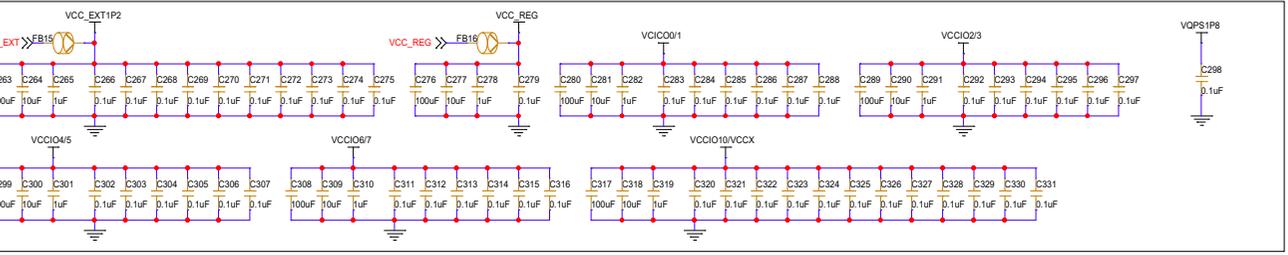
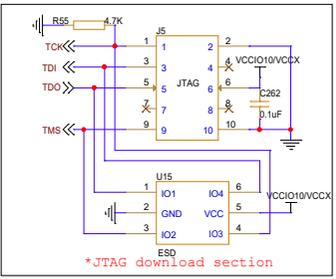
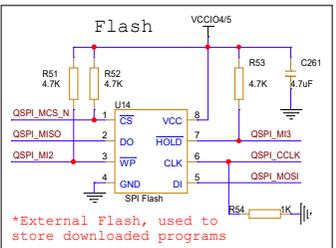
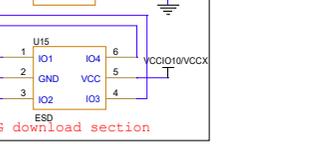
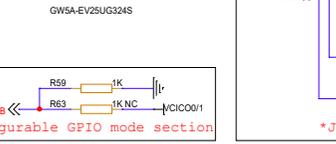
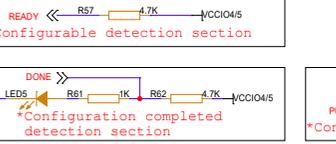
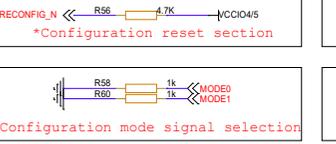
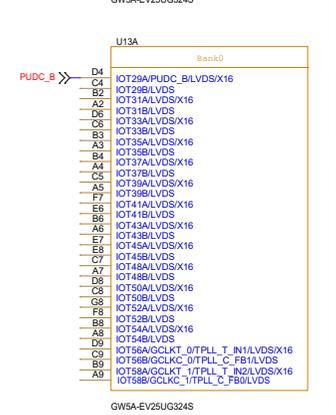
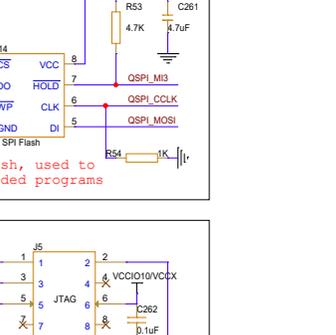
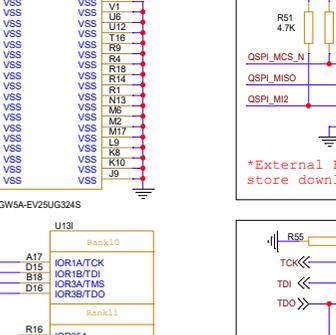
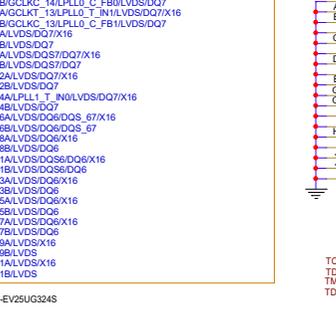
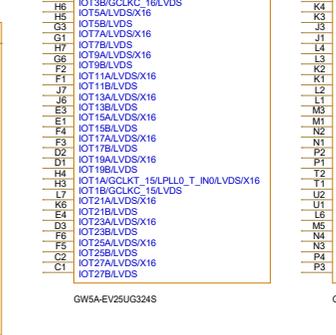
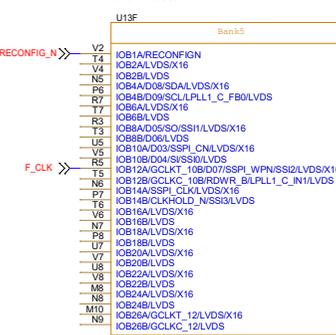
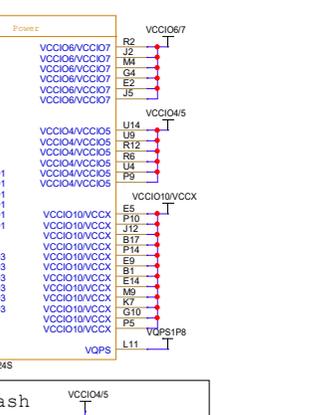
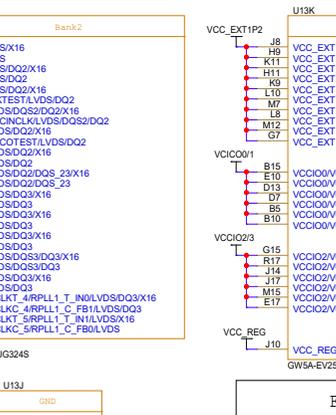
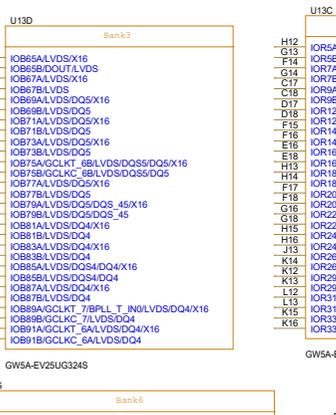
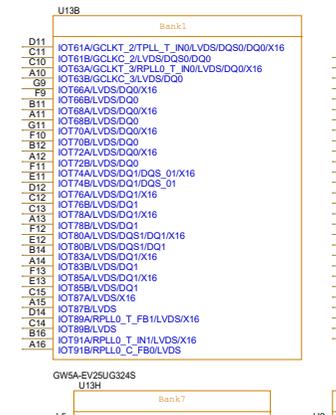
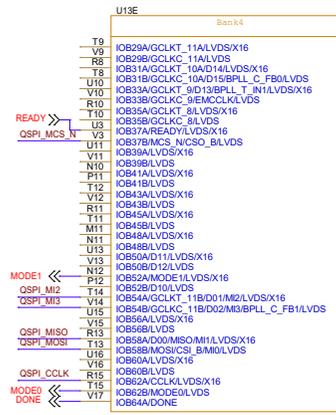
Notes:  
 1. F CLK signal is an external input clock signal.  
 It is recommended that F CLK signal be provided through an active oscillator crystal.  
 2. External Flash memory is used to store downloaded programs.  
 For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.  
 3. It is recommended that add an ESD protection chip to the JTAG download circuit.  
 4. VCC core voltage requires a large current, so it is recommended to supply power separately.



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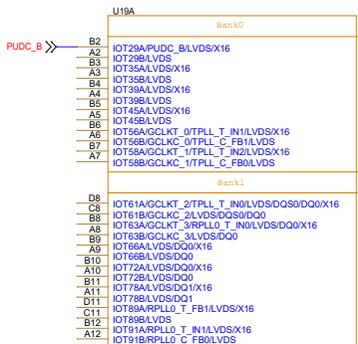


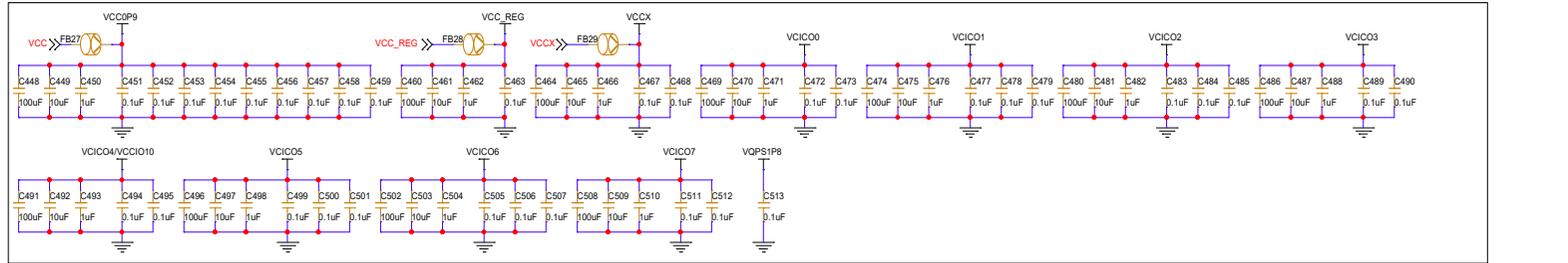
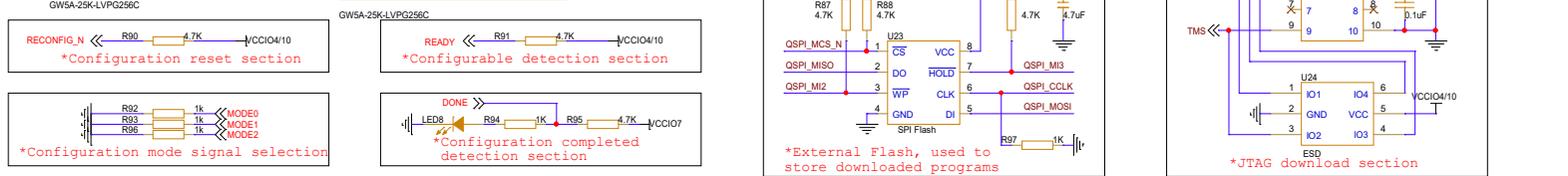
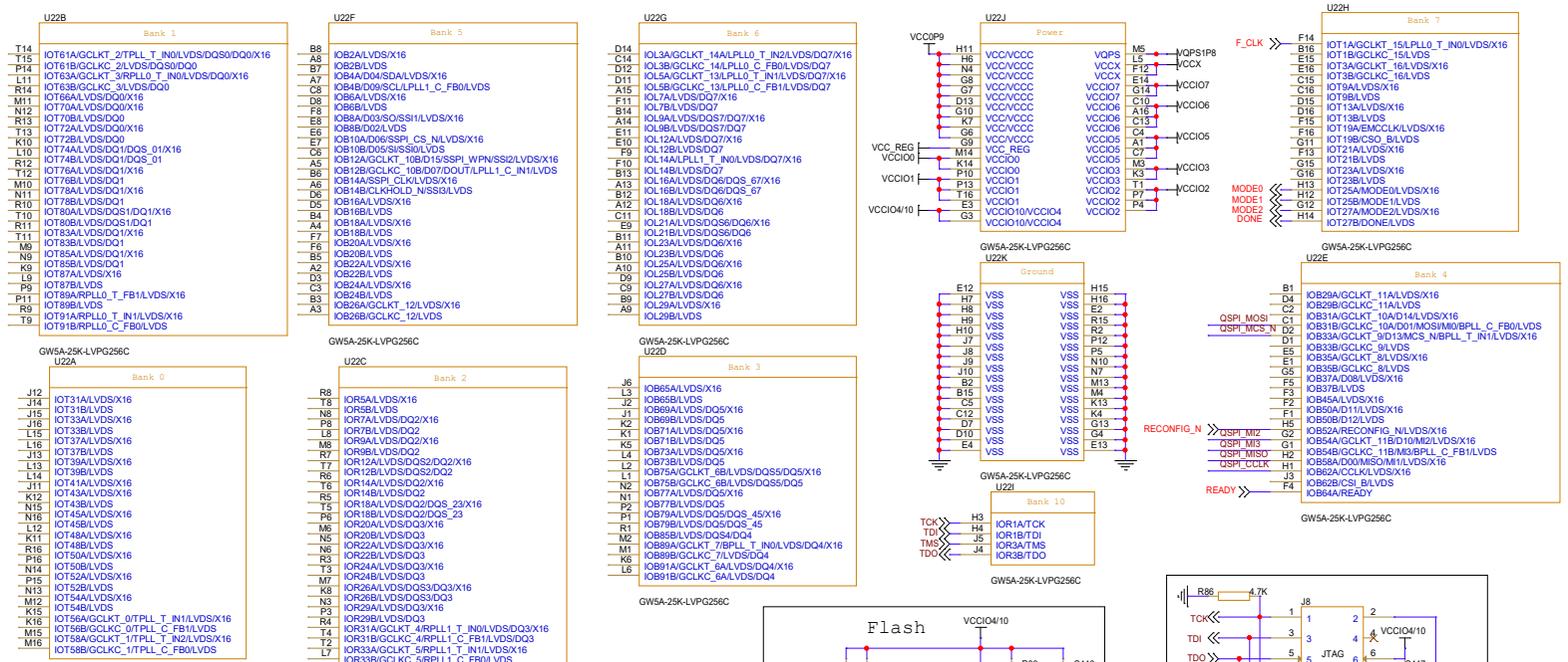
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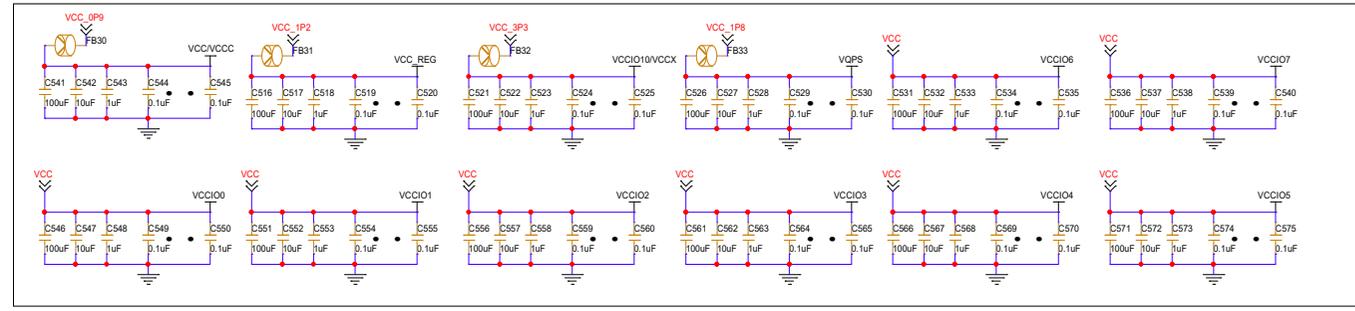
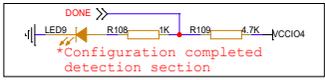
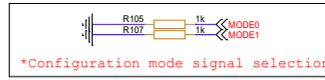
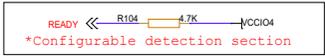
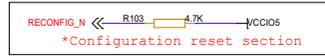
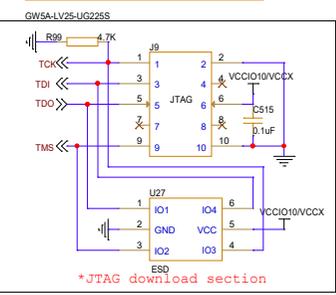
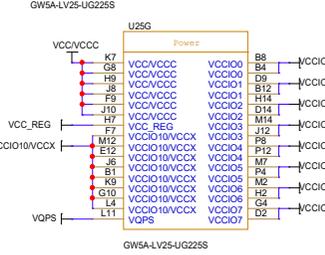
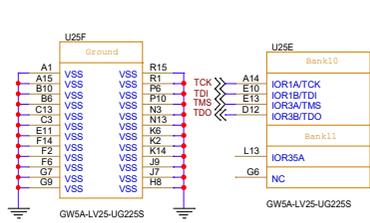
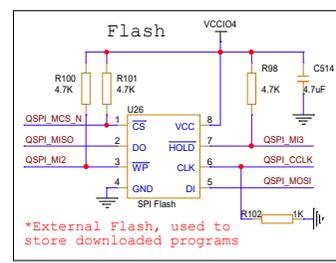
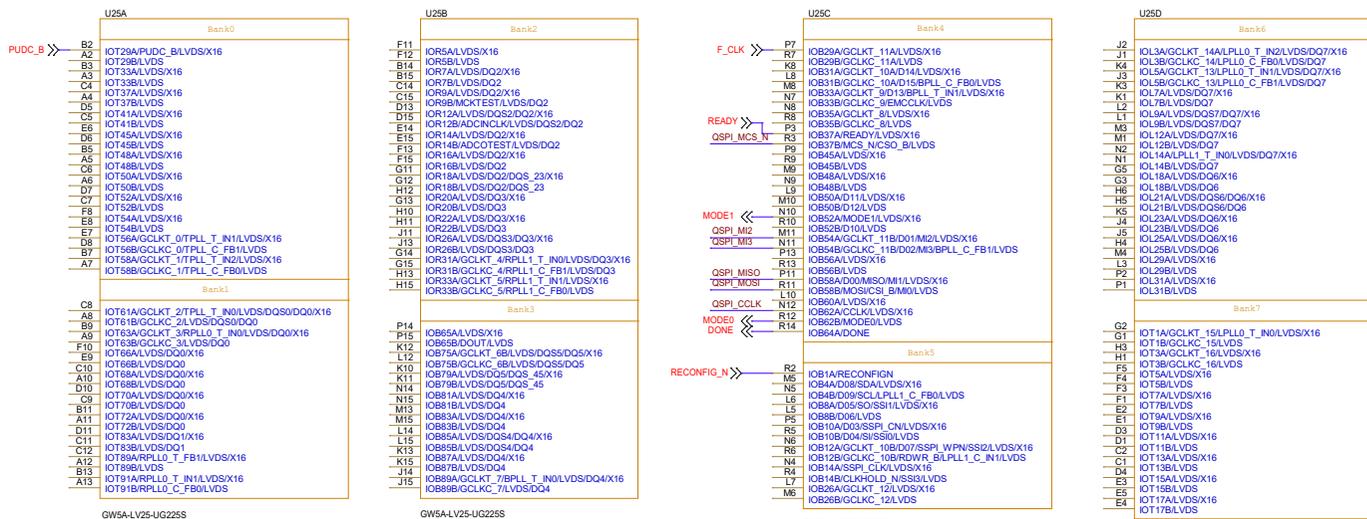






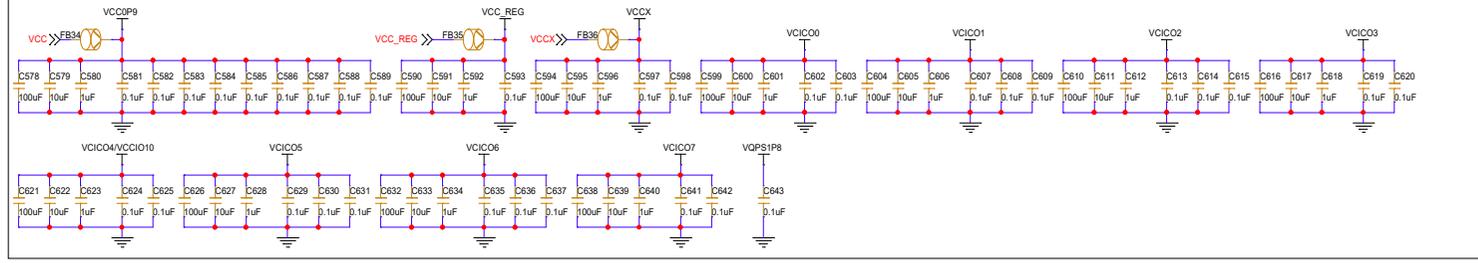
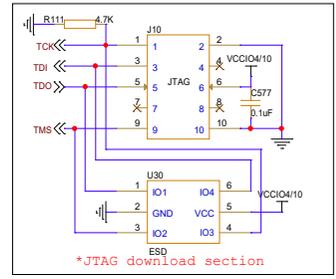
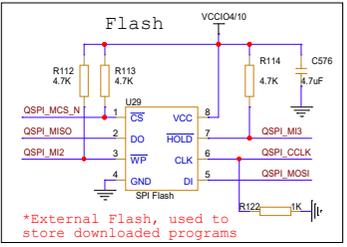
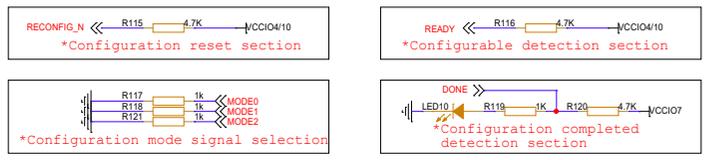
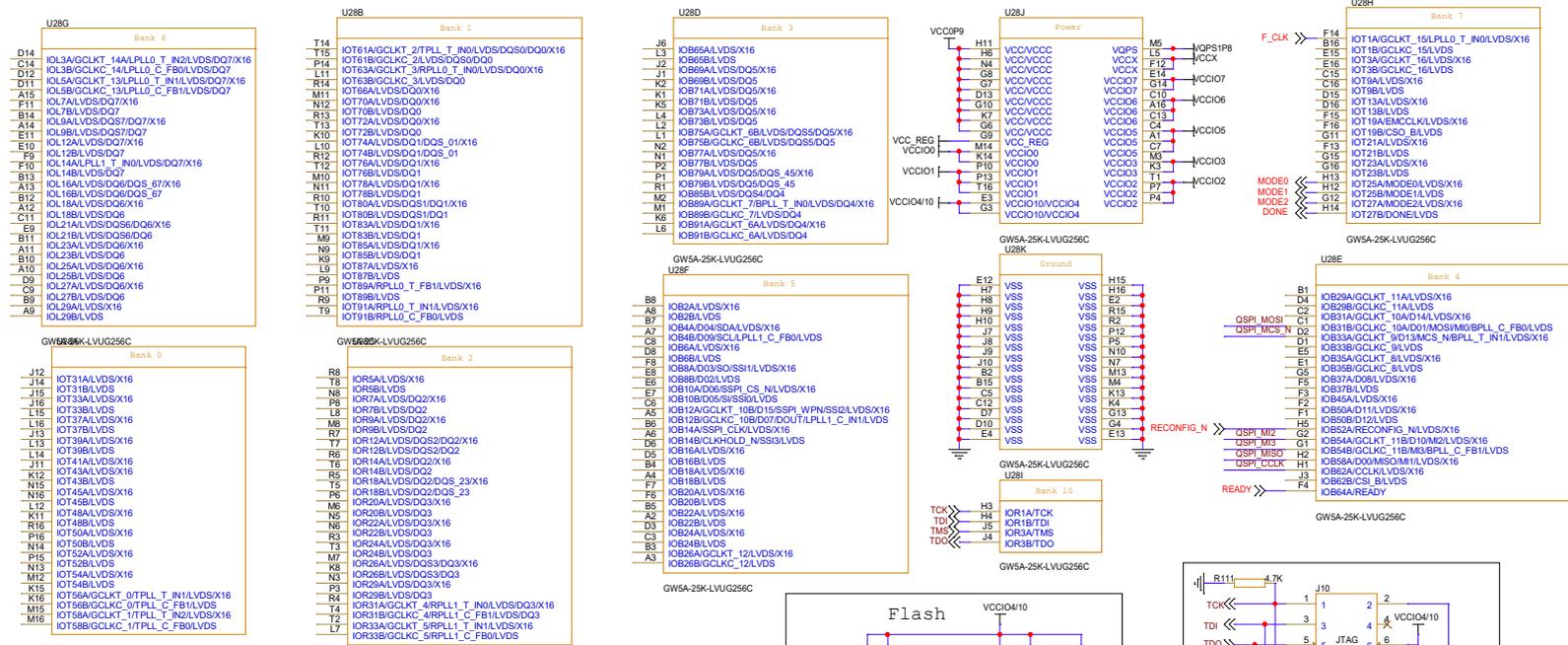
Notes:

1. F\_CLK signal is an external input clock signal. It is recommended that F\_CLK signal be provided through an active oscillator crystal.
2. External Flash memory is used to store downloaded programs. For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
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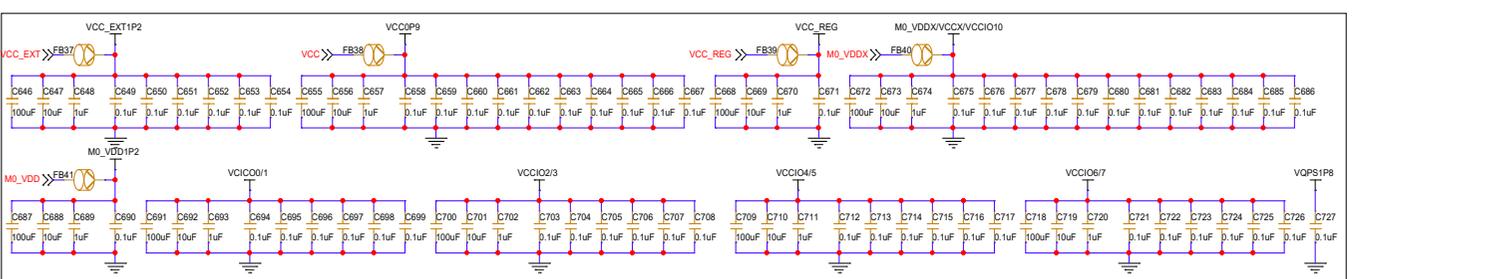
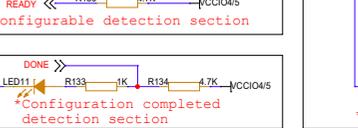
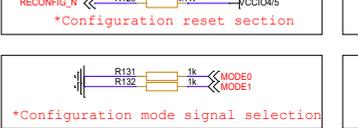
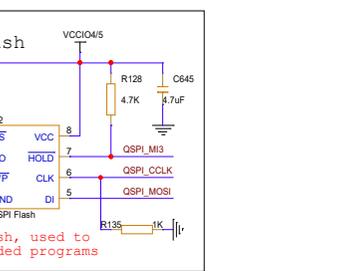
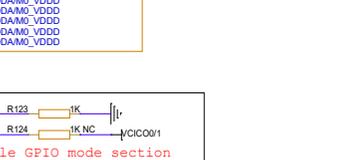
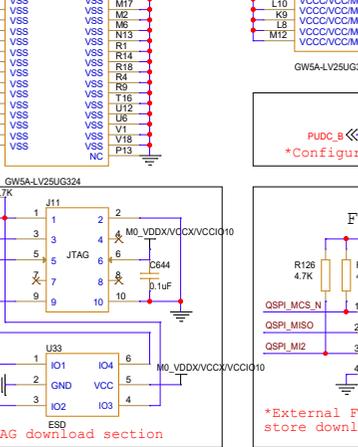
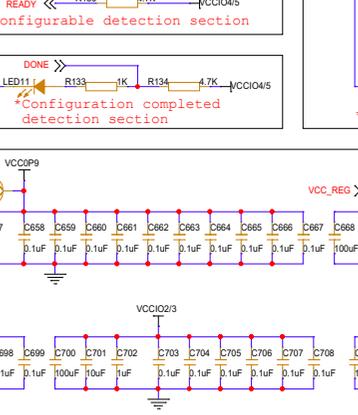
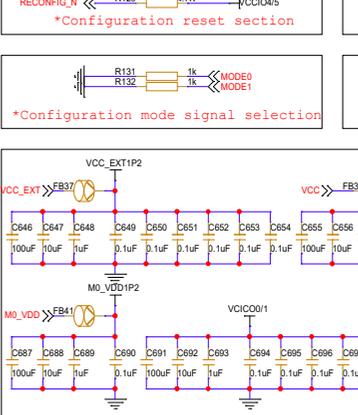
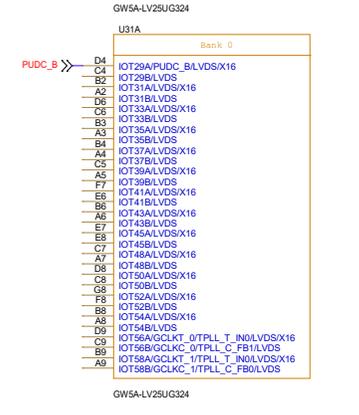
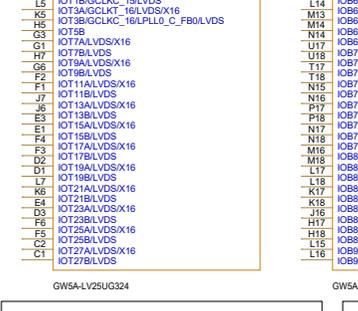
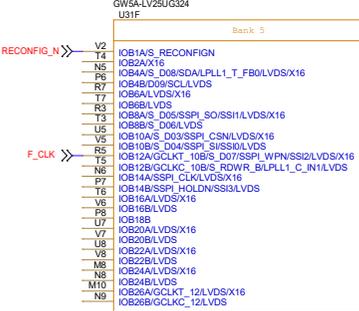
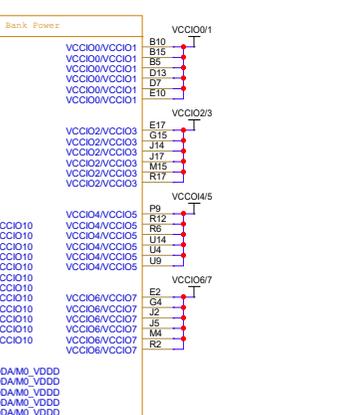
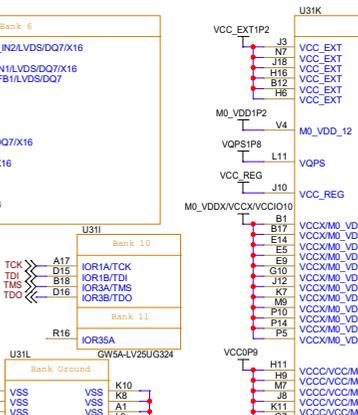
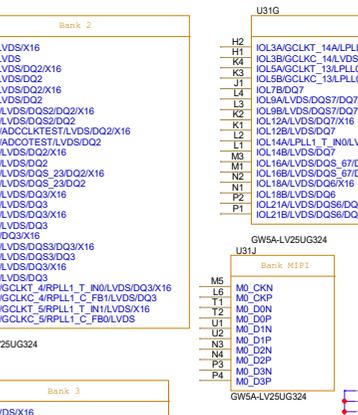
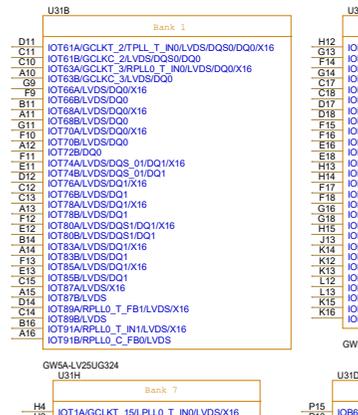
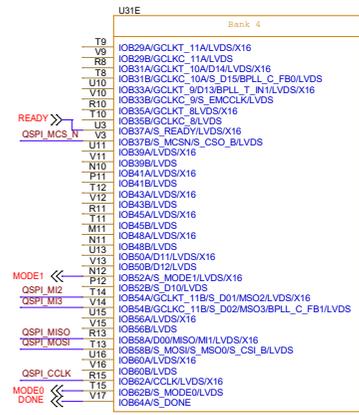


Notes:  
 1. F\_CLK signal is an external input clock signal.  
 It is recommended that F\_CLK signal be provided through an active oscillator crystal.  
 2. External Flash memory is used to store downloaded programs.  
 For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.  
 3. It is recommended that add an ESD protection chip to the JTAG download circuit.  
 4. VCC core voltage requires a large current, so it is recommended to supply power separately.

**GW5A-LV25UG256C**



- Notes:**
1. F CLK signal is an external input clock signal. It is recommended that F CLK signal be provided through an active oscillator crystal.
  2. External Flash memory is used to store downloaded programs. For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG250.
  3. It is recommended that add an ESD protection chip to the JTAG download circuit.
  4. VCC core voltage requires a large current, so it is recommended to supply power separately.



- Notes:
- 1.F CLK signal is an external input clock signal.
  - It is recommended that F CLK signal be provided through an active oscillator crystal.
  - External Flash memory is used to store downloaded programs.
  - For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
  - It is recommended that add an ESD protection chip to the JTAG download circuit.
  - VCC core voltage requires a large current, so it is recommended to supply power separately.