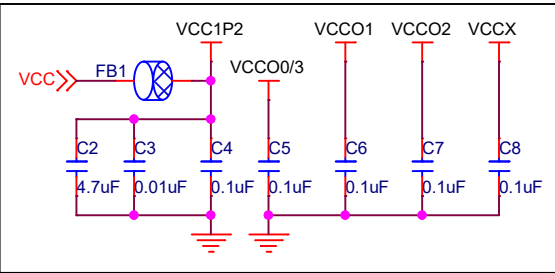
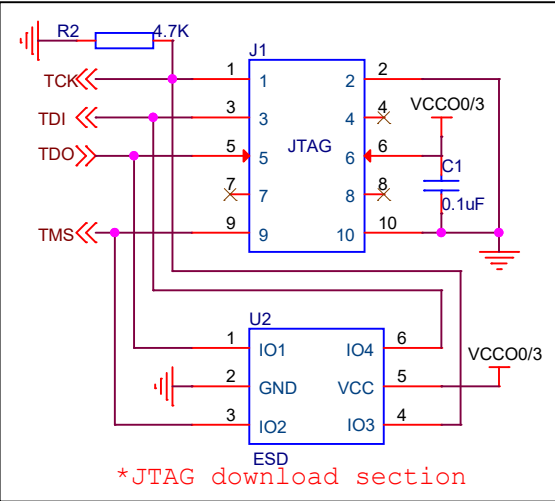
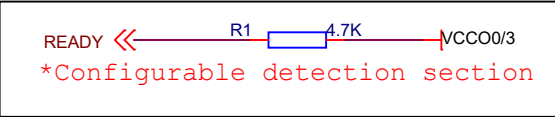
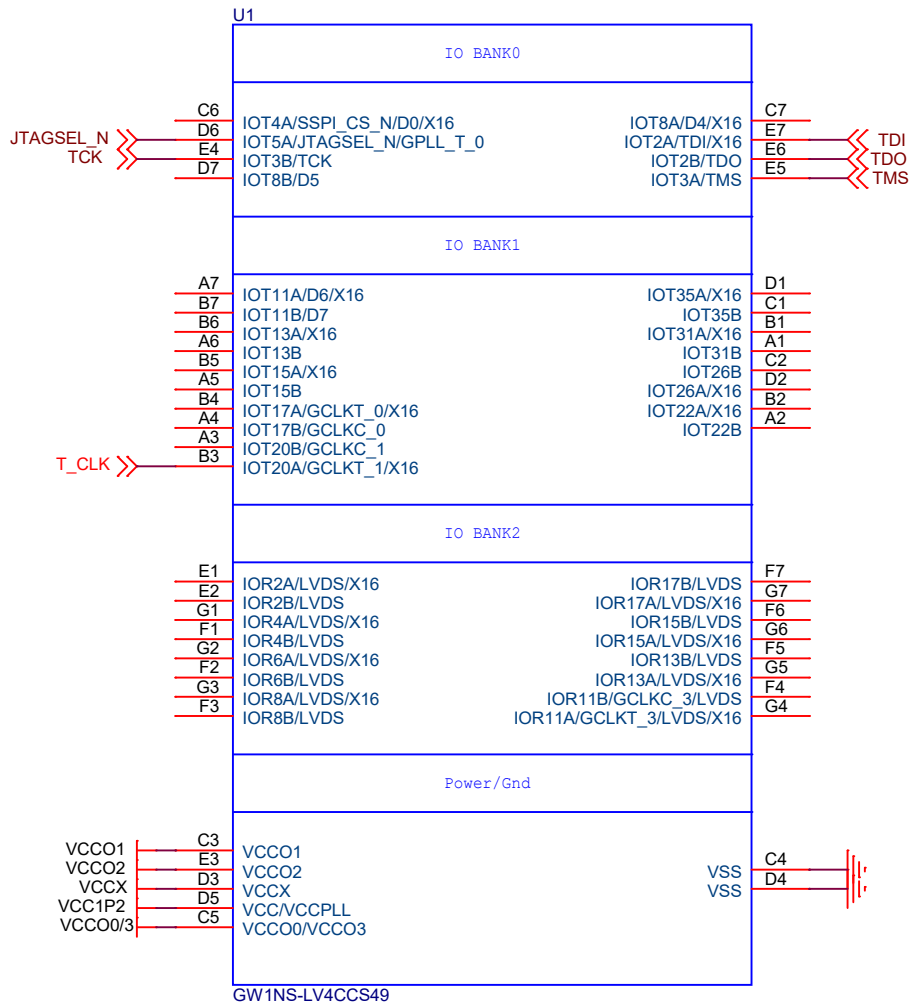


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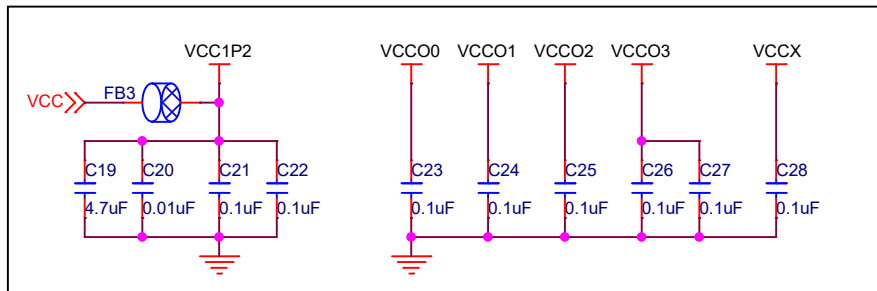
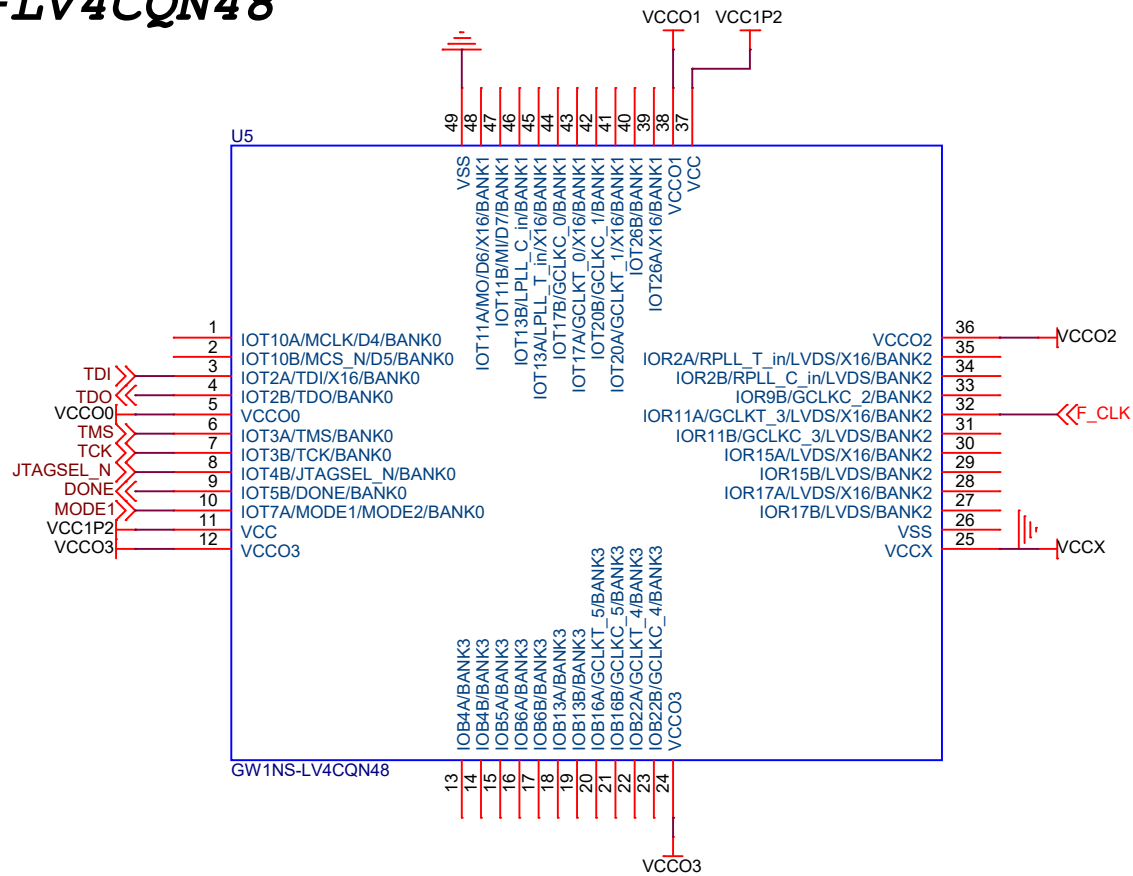
GW1NS-LV4CCS49



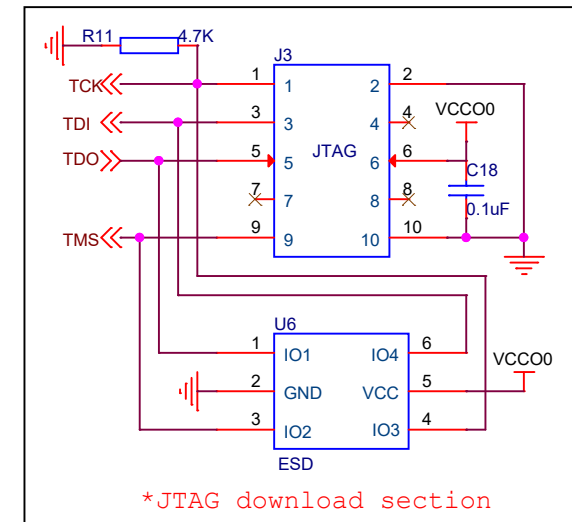
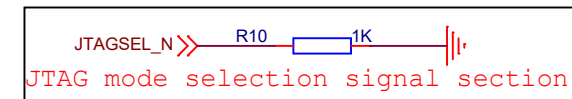
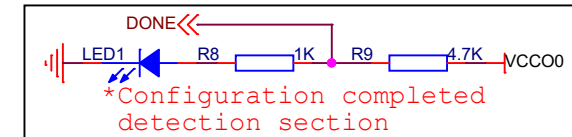
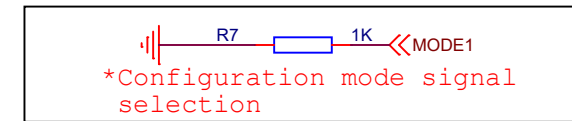
- Notes:
- 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
 - 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

A

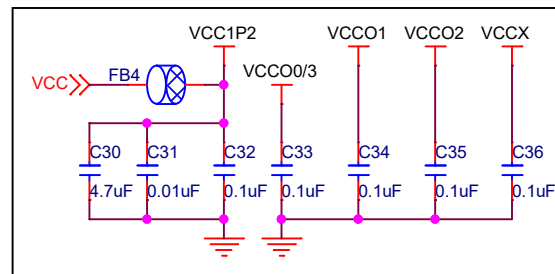
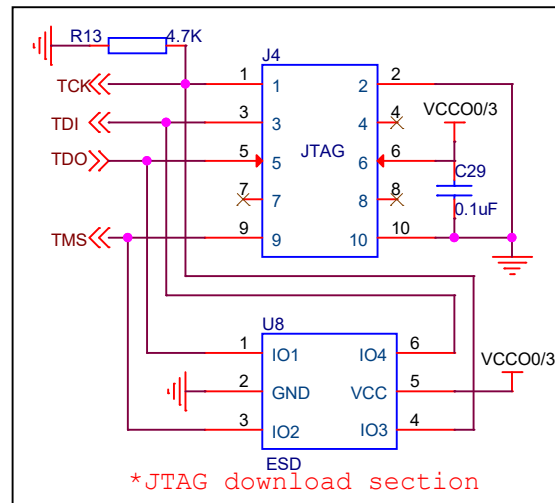
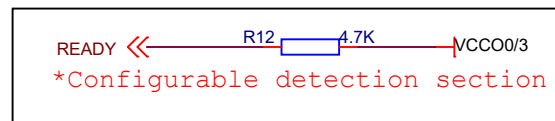
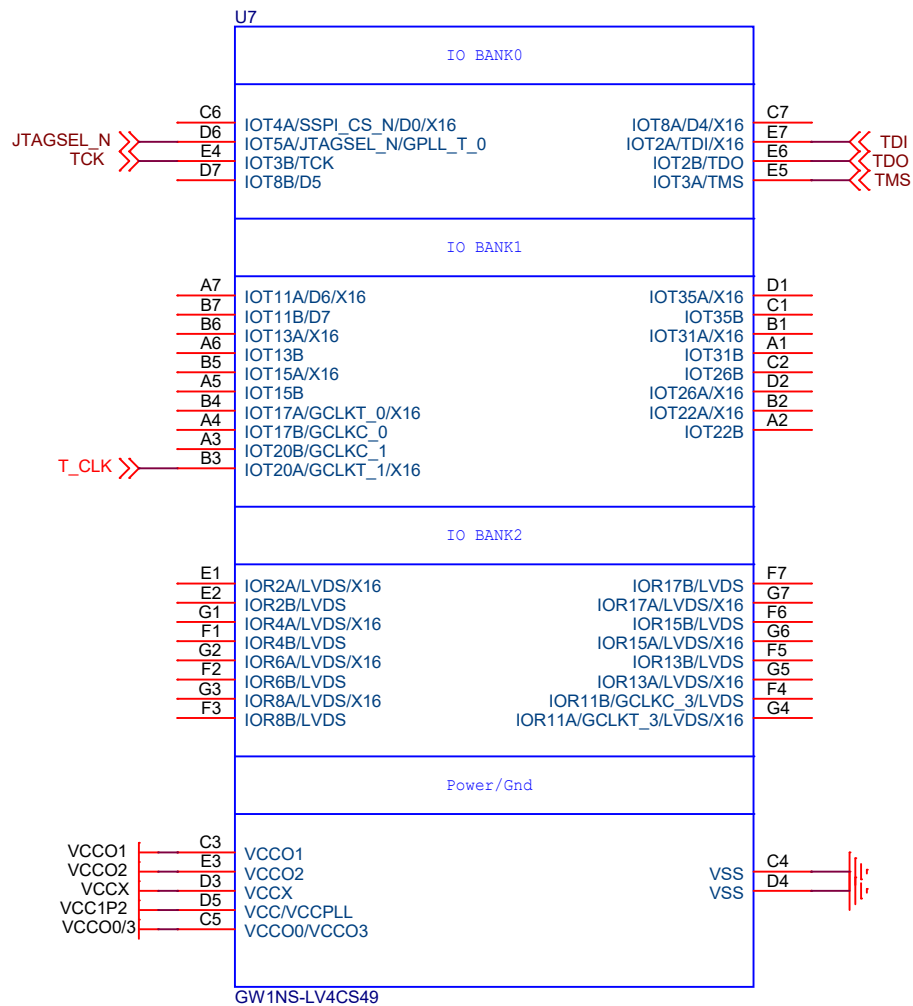
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GOWIN Minimum System Diagram			
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2.It is recommended that add an ESD protection chip to the JTAG download circuit.



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Notes:

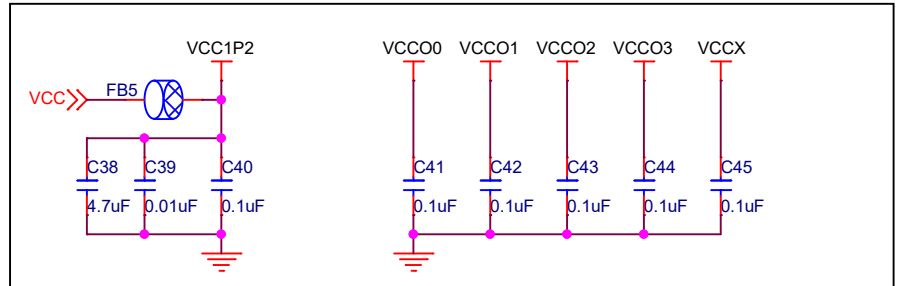
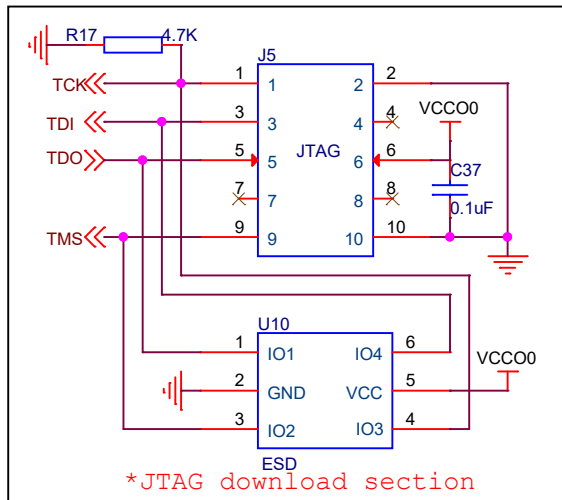
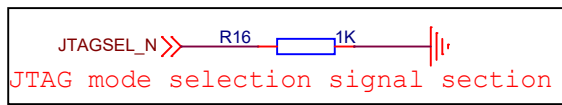
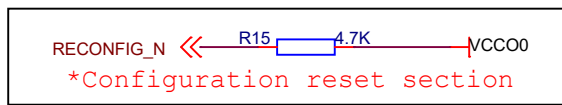
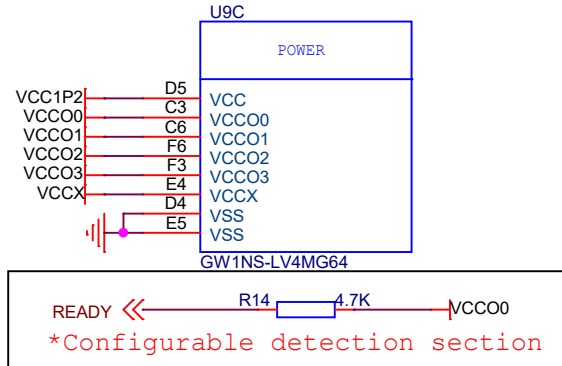
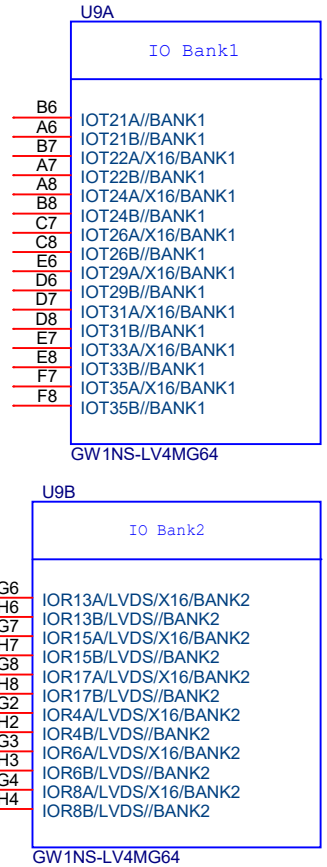
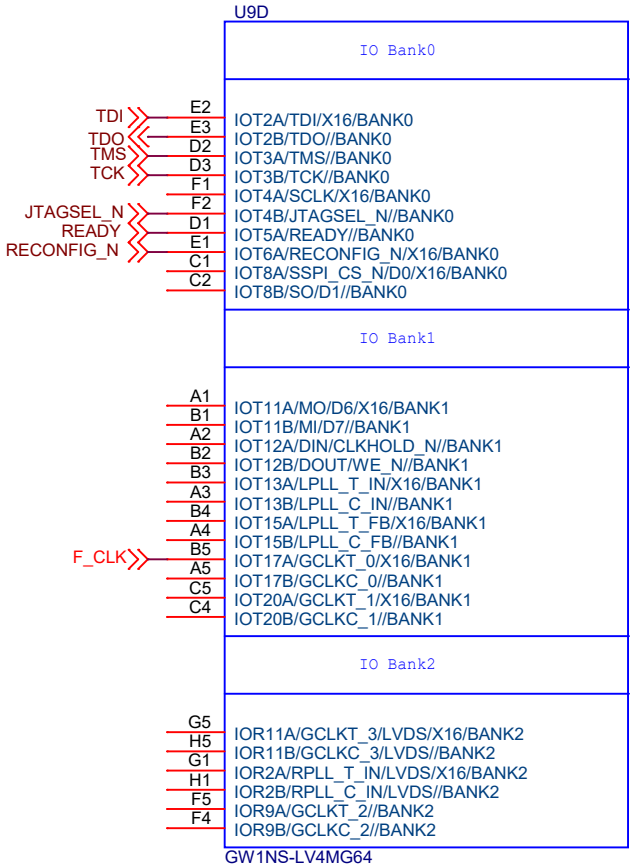
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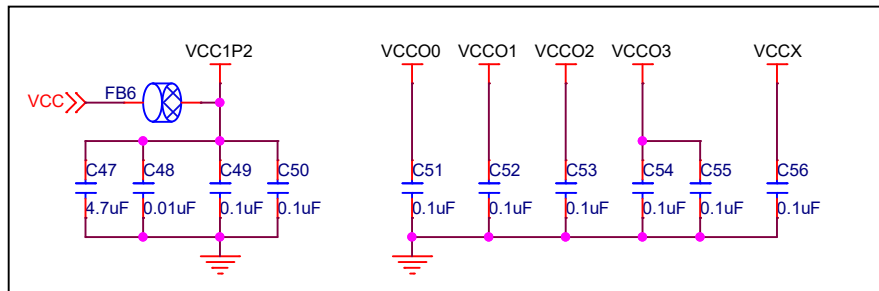
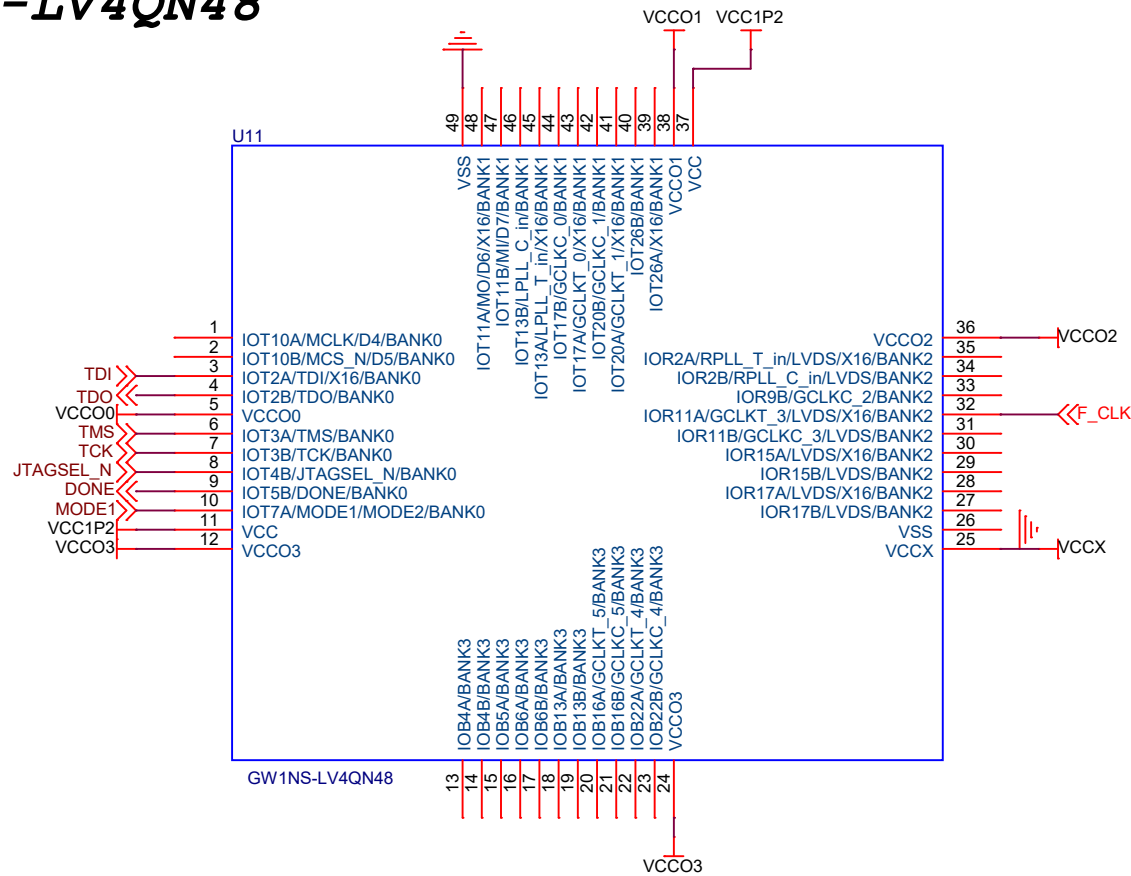
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