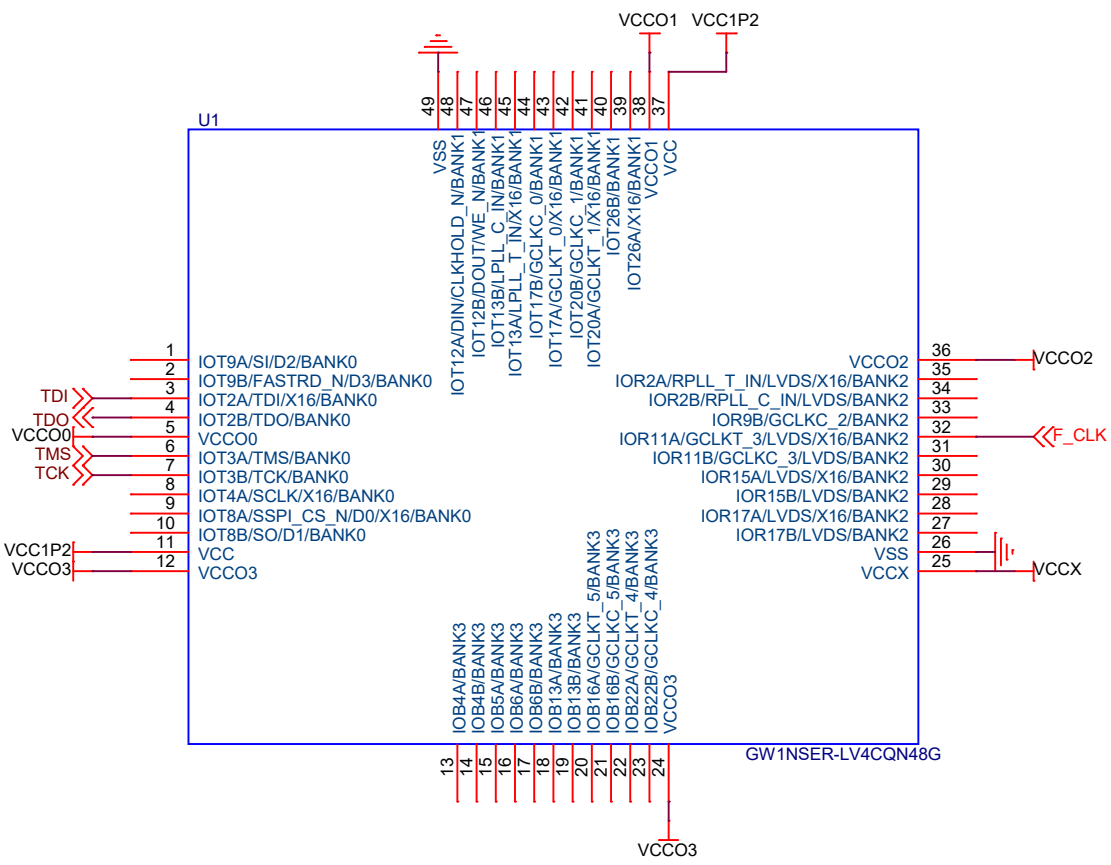
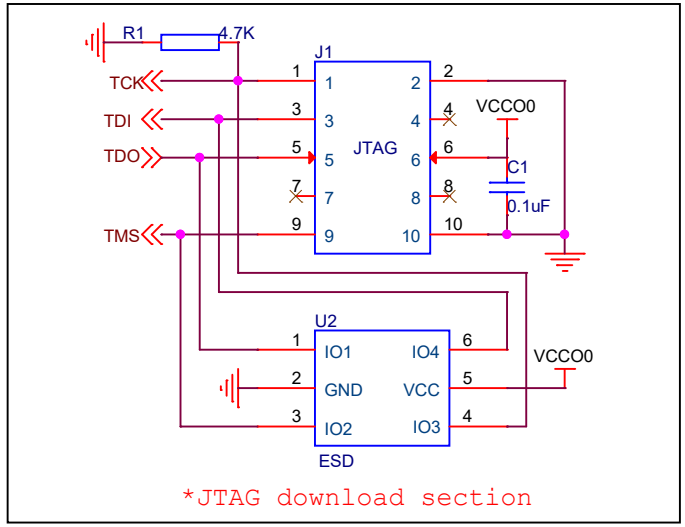
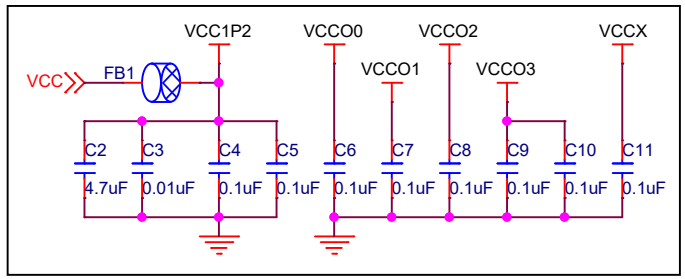
GW1NSER-LV4CQN48G



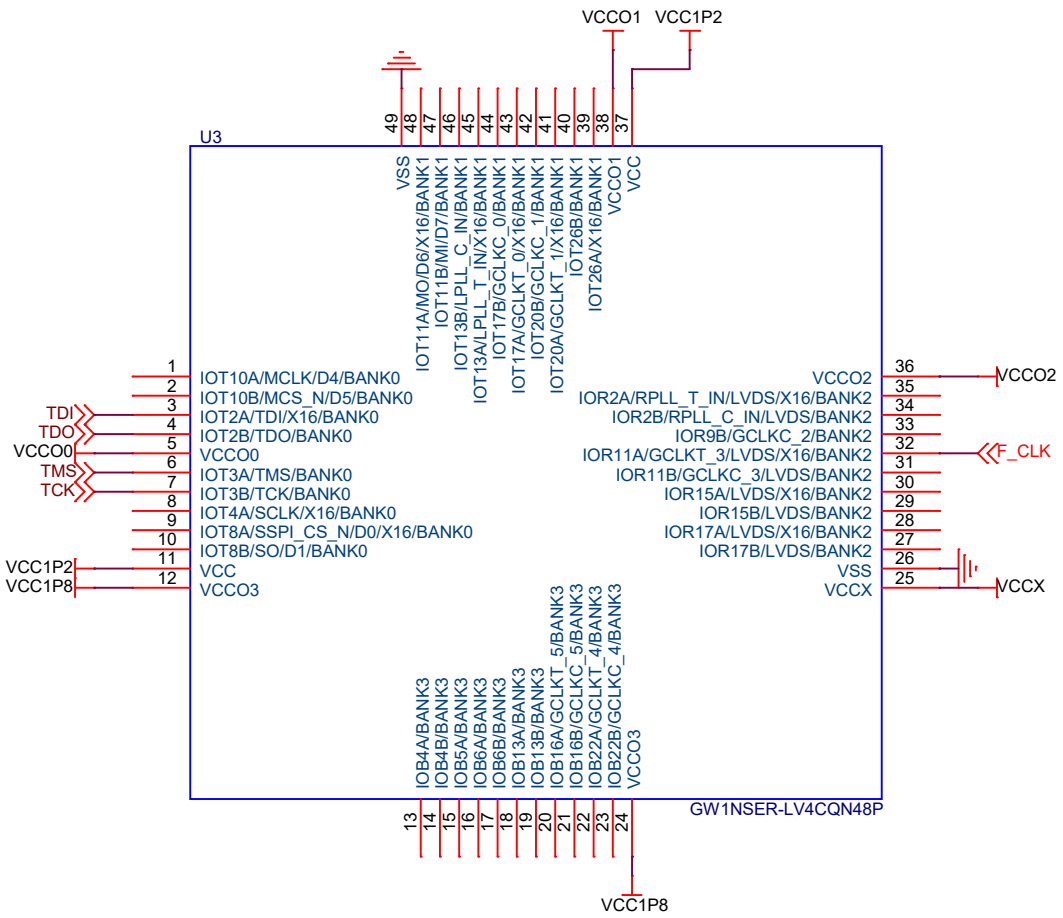


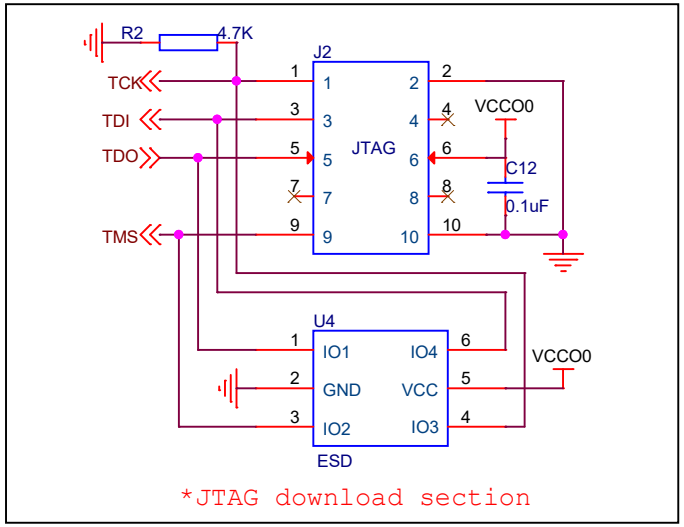


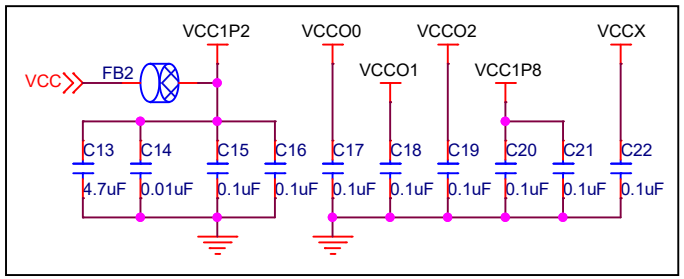
Notes:
1.F_CLK signal is an external input clock signal.
  It is recommended that F_CLK signal be provided through an active oscillator crystal.
2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title: GOWIN Minimum System Diagram		
Size: A4	Document Number: GW1NSER-LV4CQN48G	Rev: 2.0
Date: Tuesday, April 25, 2023	Sheet 1 of 2	

GW1NSER-LV4CQN48P







Notes:

1.F_CLK signal is an external input clock signal.
  It is recommended that F_CLK signal be provided through an active oscillator crystal.

2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title: GOWIN Minimum System Diagram		
Size: A4	Document Number: GW1NSER-LV4CQN48P	Rev: 2.0
Date: Tuesday, April 25, 2023	Sheet 2 of 2	