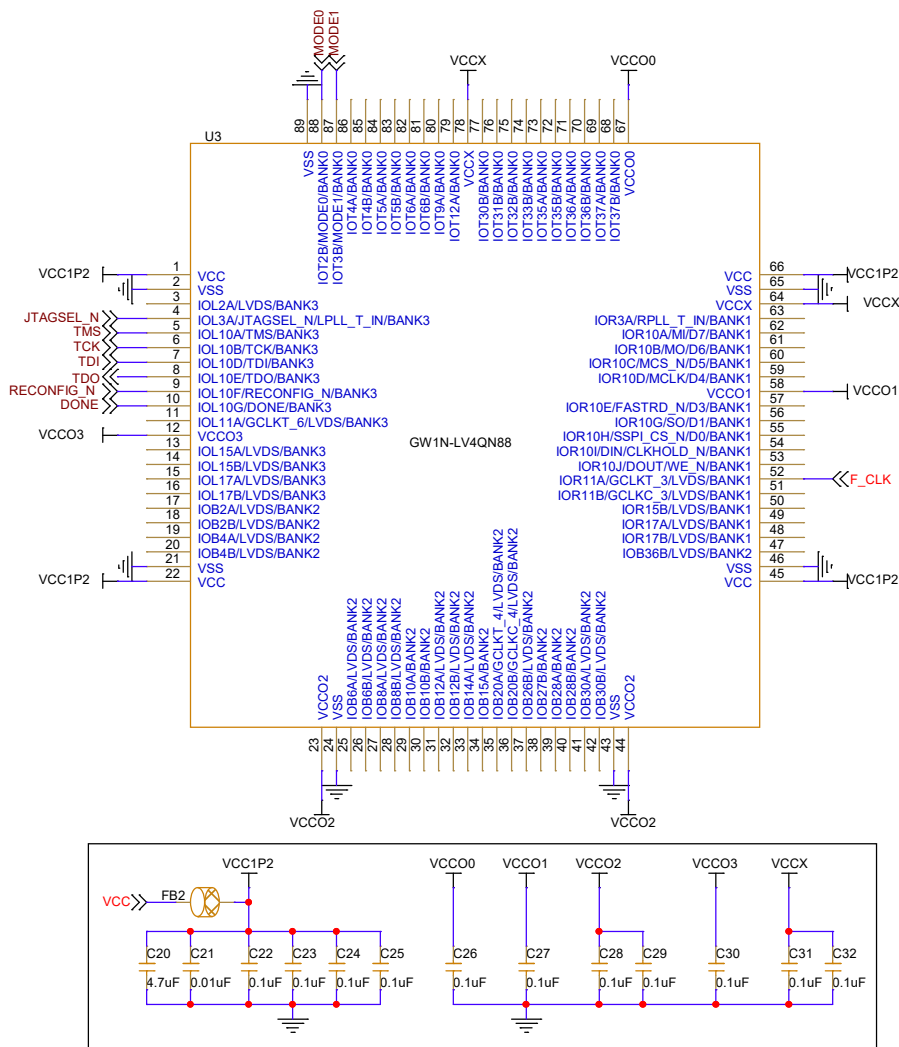
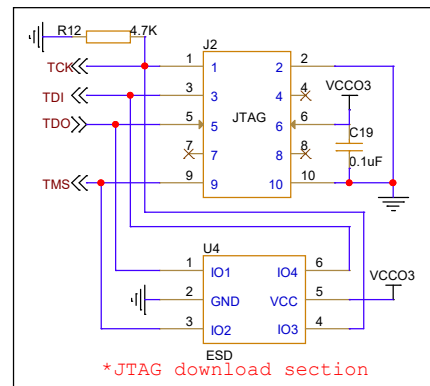
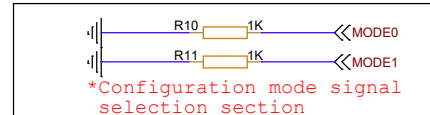
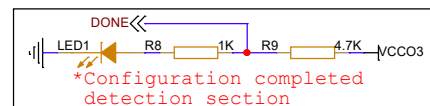
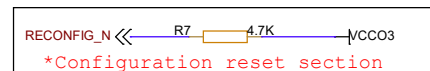
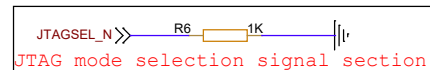


GW1N-LV4QN88



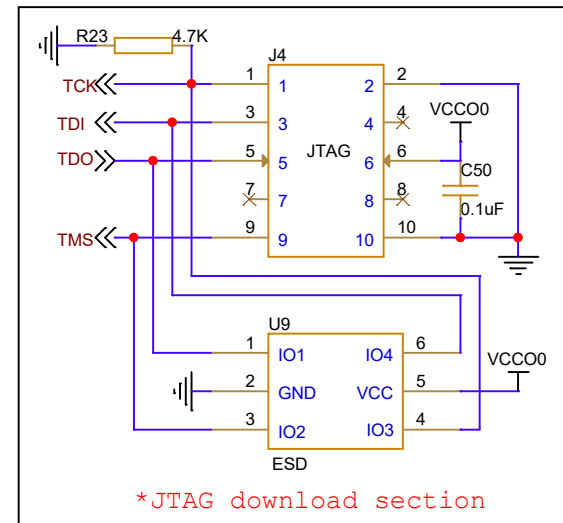
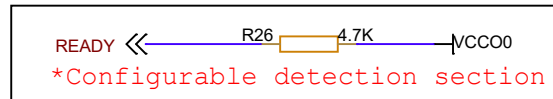
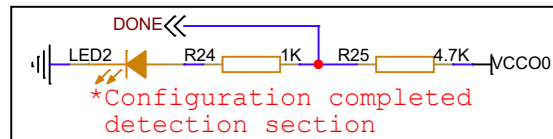
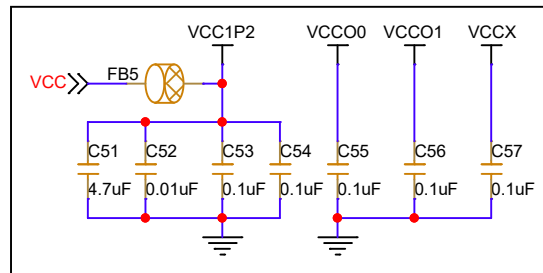
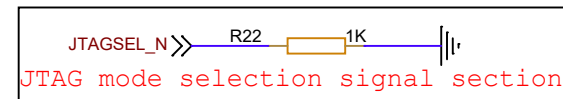
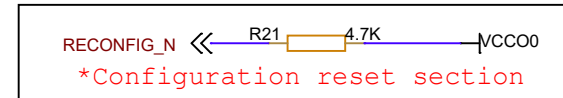
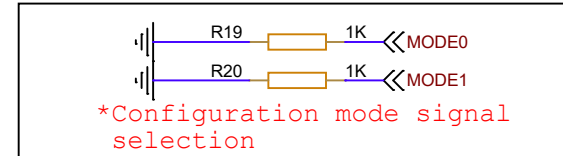
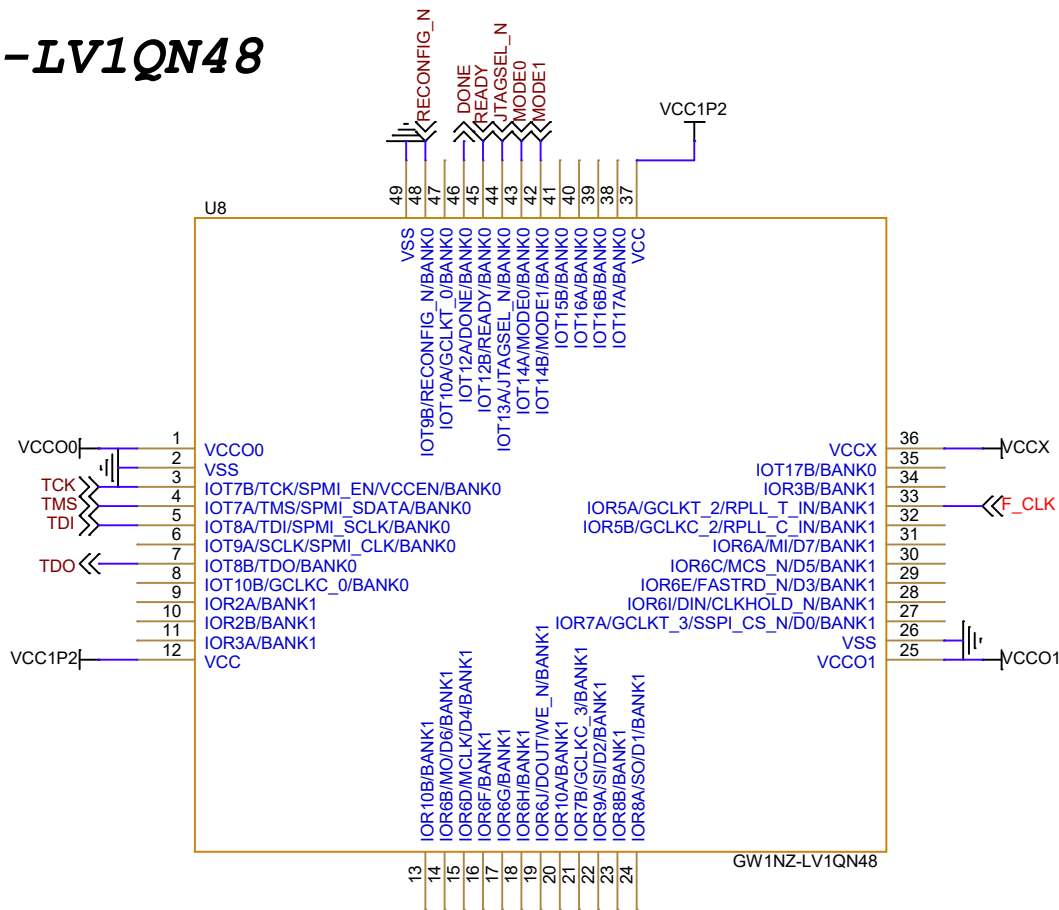
Notes:

- 1.F CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.



| | | |
|--|----------------------------|--------------|
| Title | | |
| Gowin FPGA-AOTOMOTIVE Minimum System Diagram | | |
| Size | Document Number | Rev |
| B | GW1N-LV4QN88 | 2.3 |
| Date: | Friday, September 08, 2023 | Sheet 2 of 8 |

GW1NZ-LV1QN48



Notes:

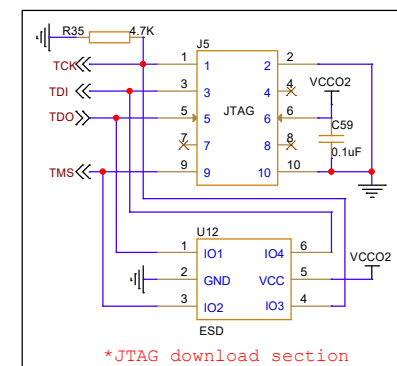
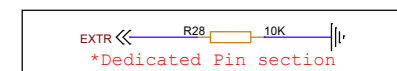
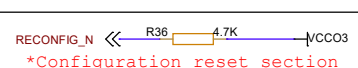
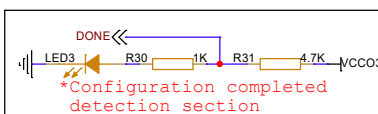
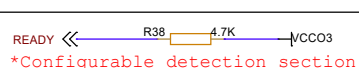
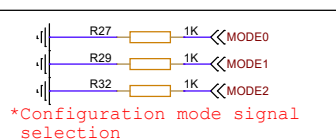
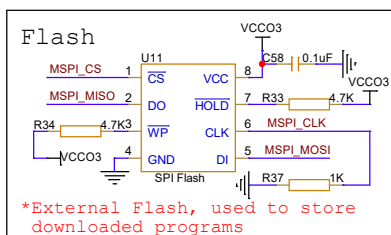
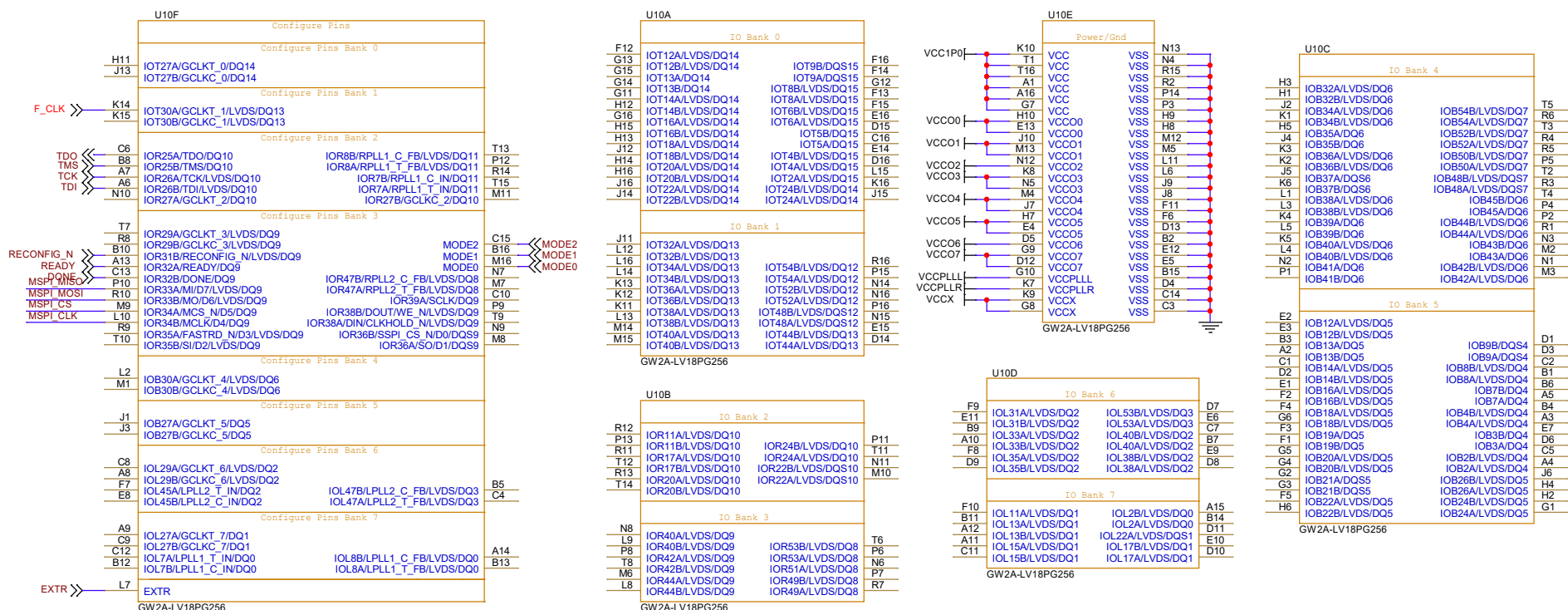
1.F_CLK signal is an external input clock signal.

It is recommended that F_CLK signal be provided through an active oscillator crystal.

2.It is recommended that add an ESD protection chip to the JTAG download circuit.

| | | |
|--|----------------------------|--------------|
| Title | | |
| Gowin FPGA-AOTOMOTIVE Minimum System Diagram | | |
| Size | Document Number | Rev |
| A4 | GW1NZ-LV1QN48 | 2.3 |
| Date: | Friday, September 08, 2023 | Sheet 4 of 8 |

GW2A-LV18PG256

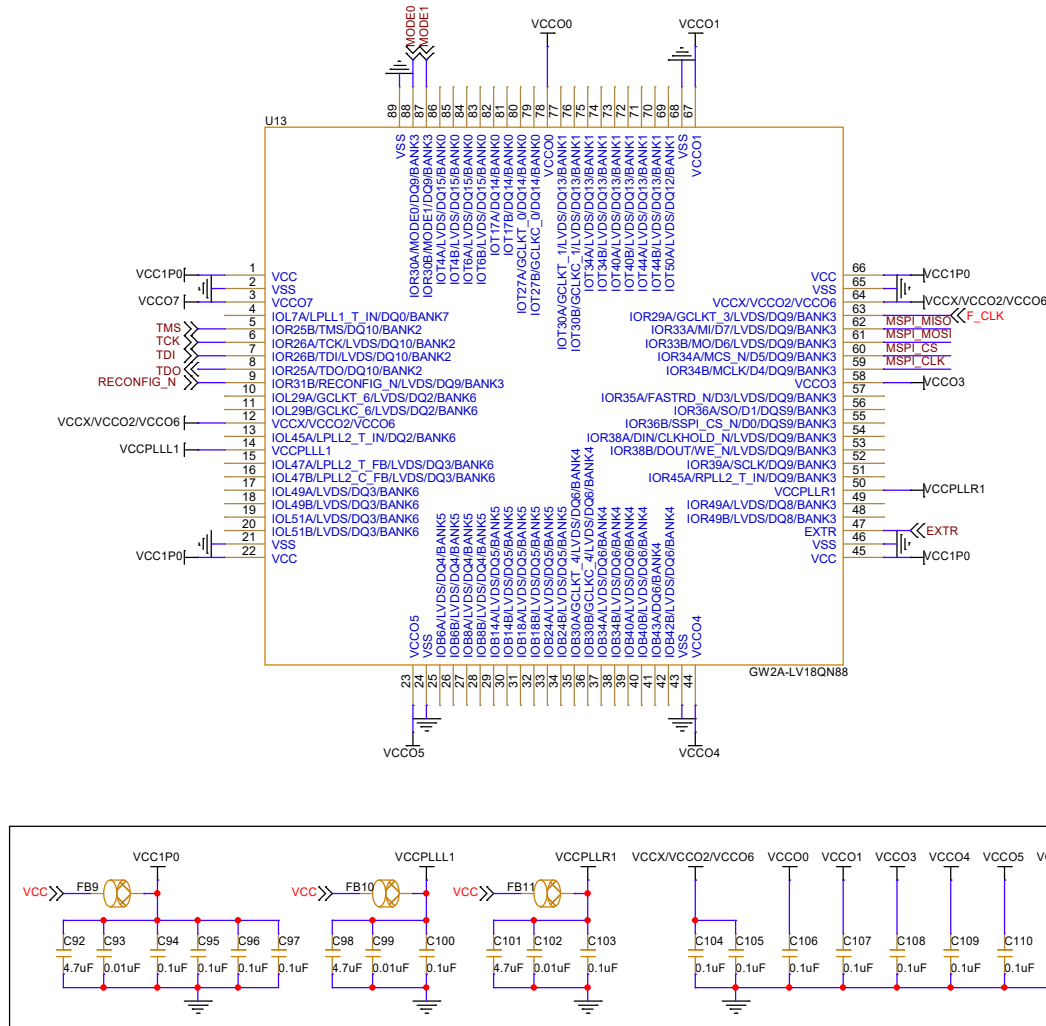


Notes:

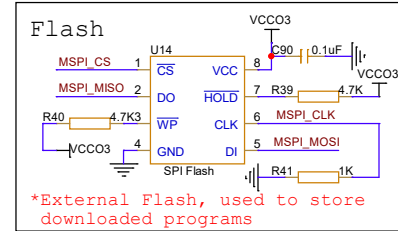
1. F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
3. It is recommended that add an ESD protection chip to the JTAG download circuit.

| | | | | |
|--|----------------------------|-------|---|------|
| Title | | | | |
| Gowin FPGA-AOTOMOTIVE Minimum System Diagram | | | | |
| Size | Document Number | Rev | | |
| A3 | GW2A-LV18PG256 | 2.3 | | |
| Date: | Friday, September 08, 2023 | Sheet | 5 | of 8 |

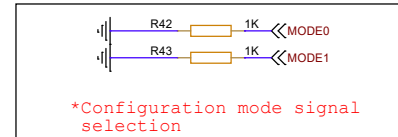
GW2A-LV18QN88



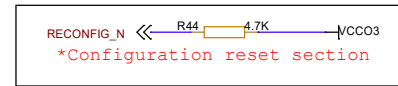
- Notes:
- 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
 - 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
 - 3.It is recommended that add an ESD protection chip to the JTAG download circuit.



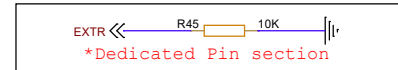
*External Flash, used to store downloaded programs



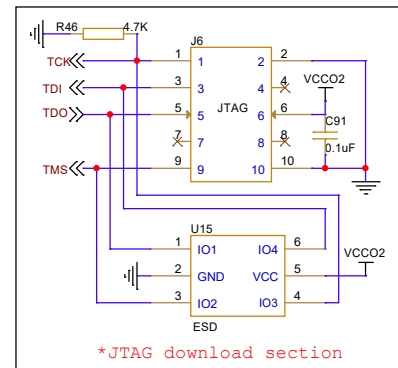
*Configuration mode signal selection



*Configuration reset section



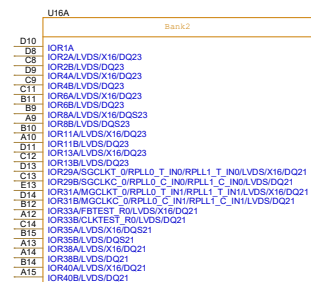
*Dedicated Pin section



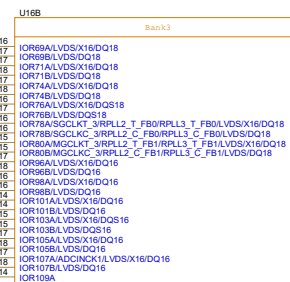
*JTAG download section

| | | |
|--|----------------------------|--------------|
| Title | | |
| Gowin FPGA-AOTOMOTIVE Minimum System Diagram | | |
| Size | Document Number | Rev |
| A3 | GW2A-LV18QN88 | 2.3 |
| Date: | Friday, September 08, 2023 | Sheet 6 of 8 |

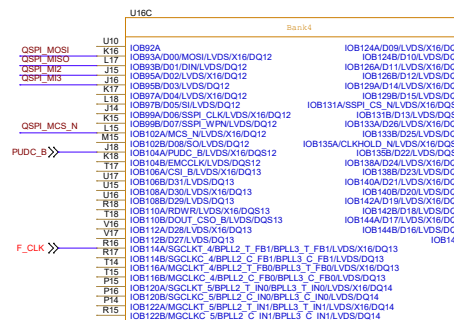
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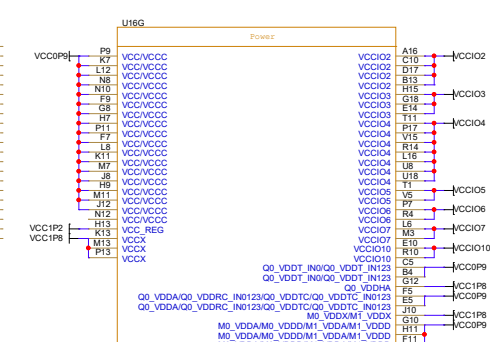
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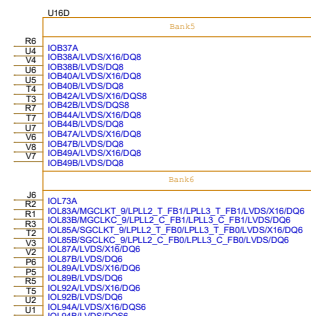
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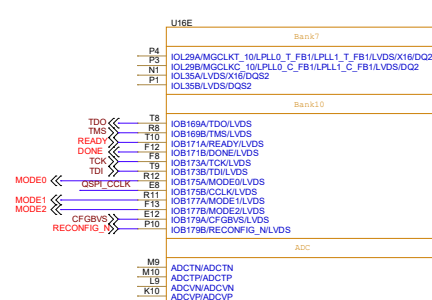
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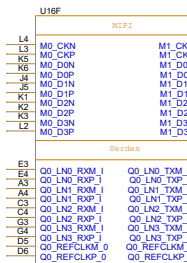
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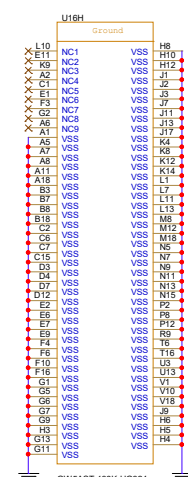
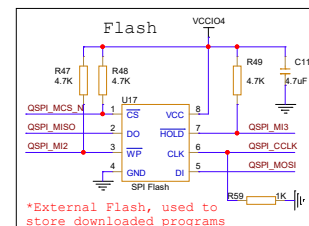
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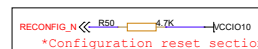
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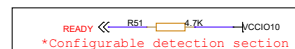
GW5AST-138K-UG32

 GW5AST-138K-UG324

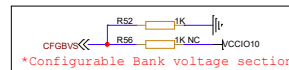
*External Flash, used to store downloaded programs



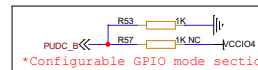
*Configuration reset section



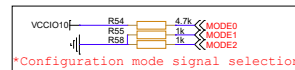
*Configurable detection section



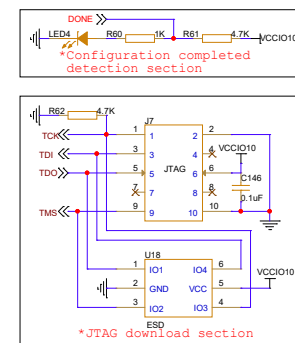
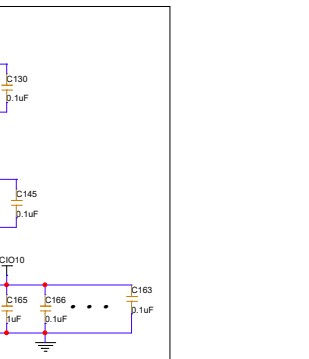
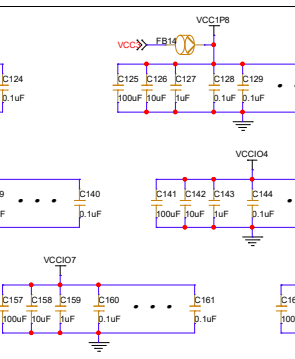
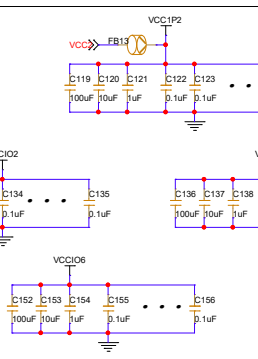
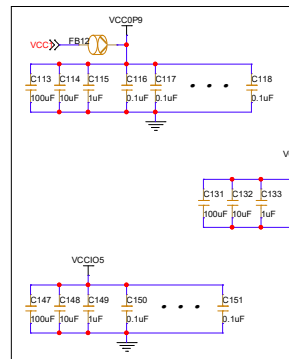
*Configurable Bank voltage section



*Configurable GPIO mode section



*Configuration mode signal selection

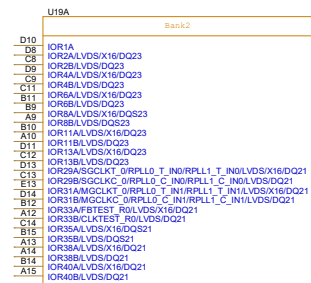


Timing diagram for U18 showing a pulse from 1 to 6.

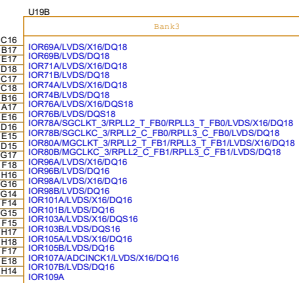
Notes:

- 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately

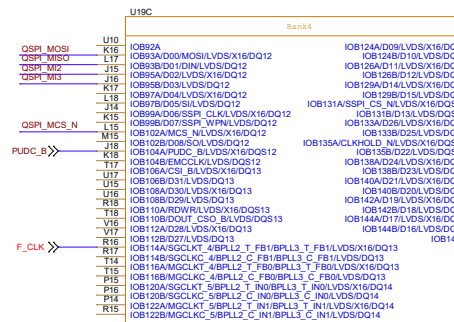
GW5AT-138K-UG324



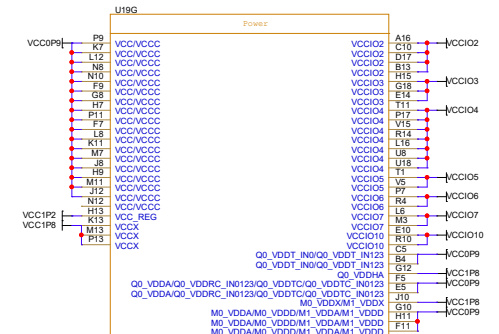
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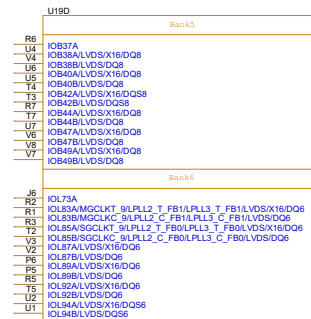
GW5AT-138K-UG324



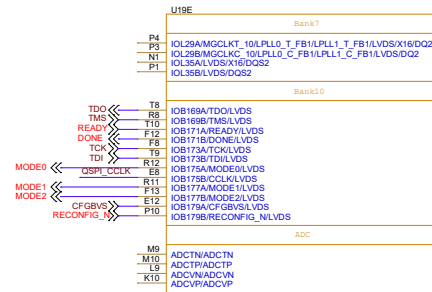
GW5AT-138K-UG32



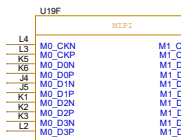
GW5AT-138K-UG32



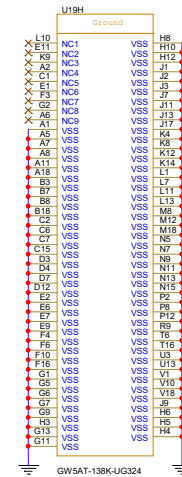
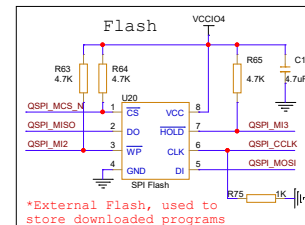
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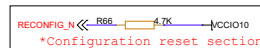
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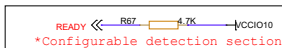
GW5AT-138K-UG32

 GW5AT-138K-UG324

*External Flash, used to store downloaded programs



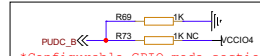
*Configuration reset section



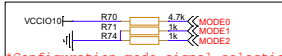
*Configurable detection section



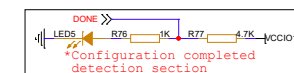
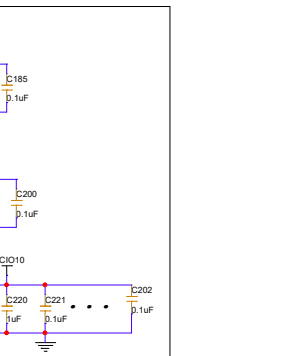
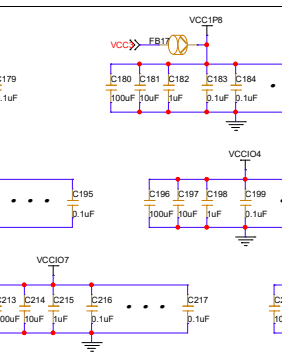
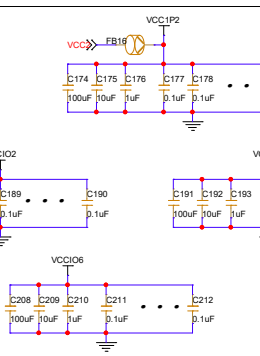
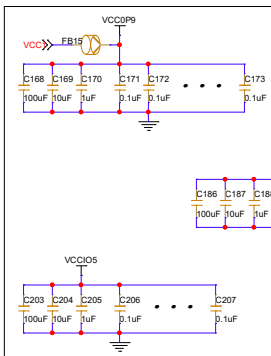
*Configurable Bank voltage section



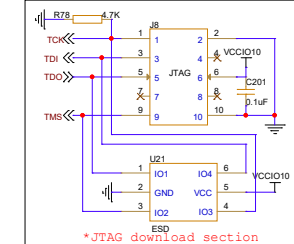
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*Configurable GPIO mode section
```



*Configuration mode signal selectio



```
*Configuration completed
detection section
```



*JTAG download section

Notes:

1.F CLK signal is an external input clock signal.

It is recommended that F CLK signal be provided through an active oscillator crystal.

2.External Flash memory is used to store downloaded programs.

For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.

3.It is recommended that add an ESD protection chip to the JTAG download circuit.

4.VCC core voltage requires a large current, so it is recommended to supply power separately