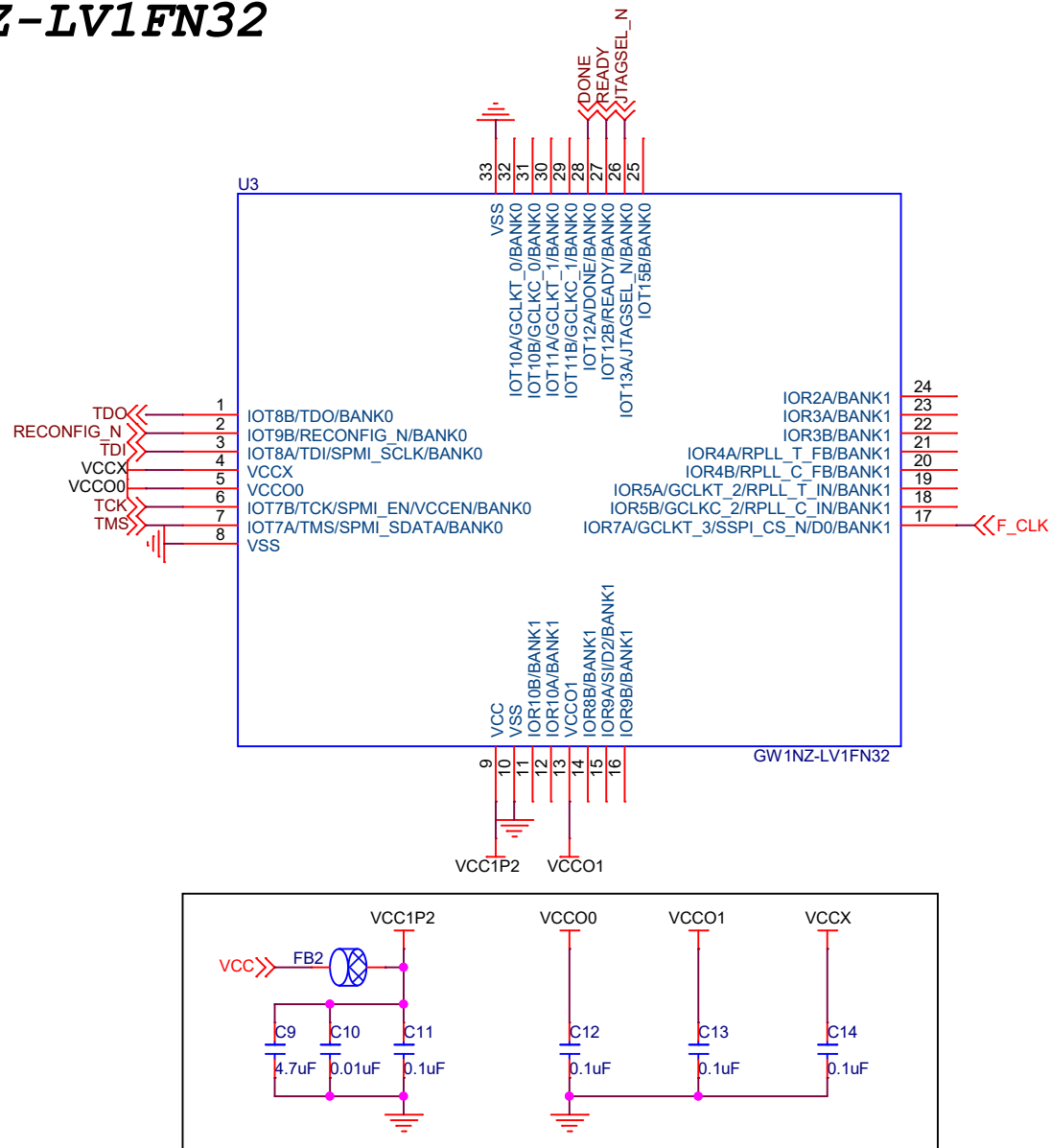
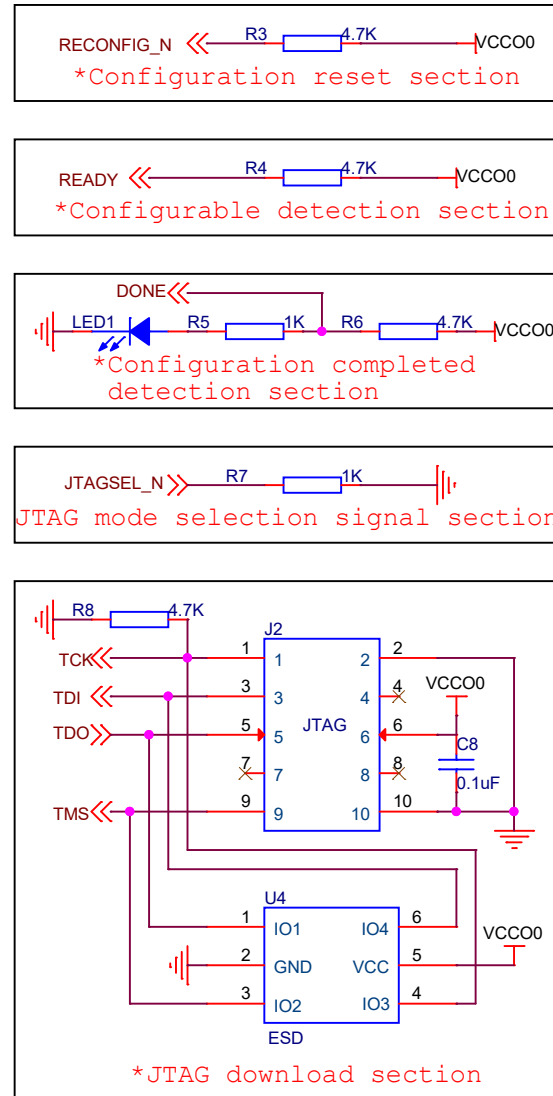


- Notes:
- 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
 - 2.It is recommended that add an ESD protection chip to the JTAG download circuit.



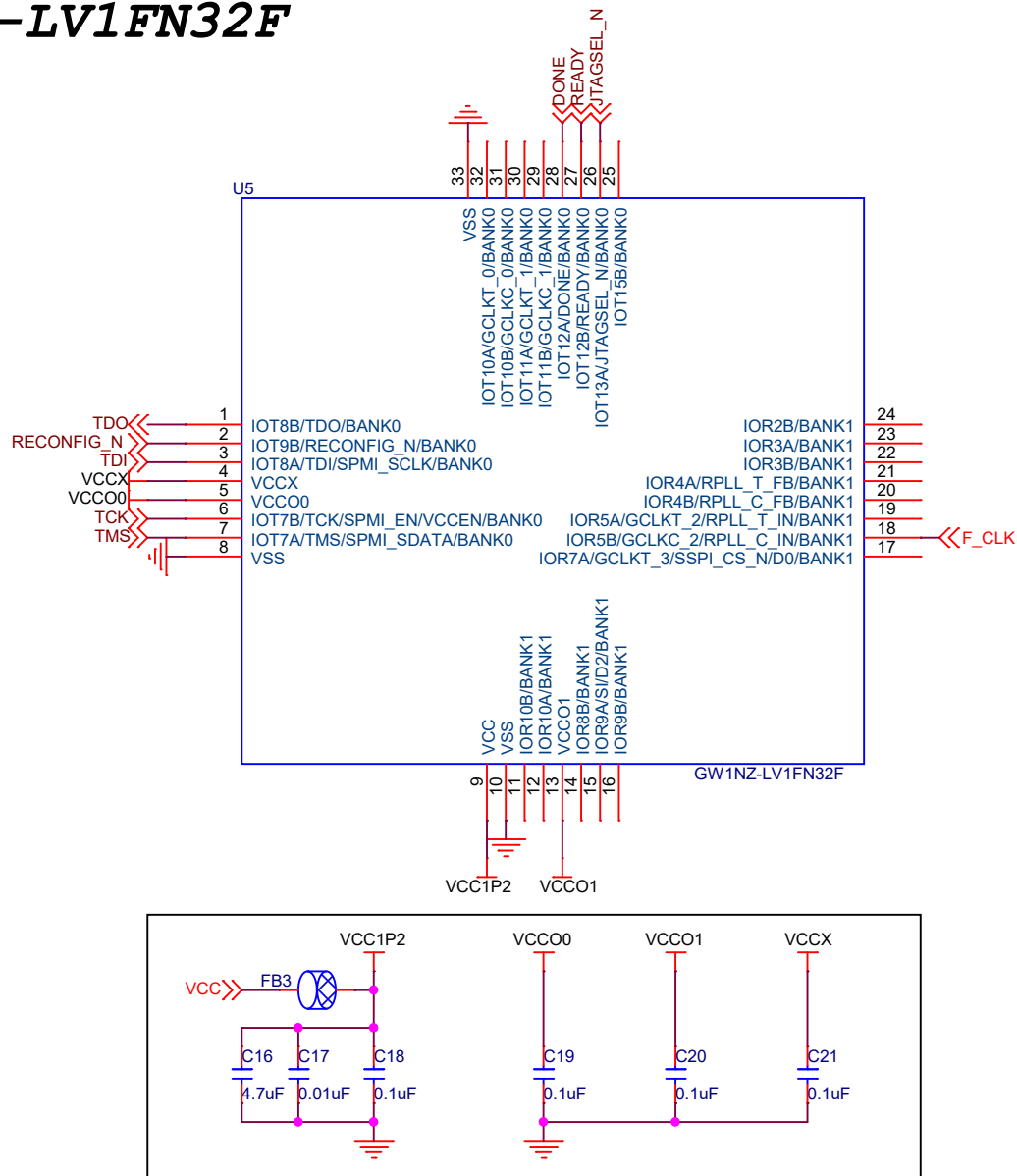
Notes:

- 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.



Title			
GOWIN Minimum System Diagram			
Size A4	Document Number GW1NZ-LV1FN32		Rev 2.0
Date:	Wednesday, April 26, 2023	Sheet	2 of 8

GW1NZ-LV1FN32F



Notes:

1.F_CLK signal is an external input clock signal.

It is recommended that F_CLK signal be provided through an active oscillator crystal.

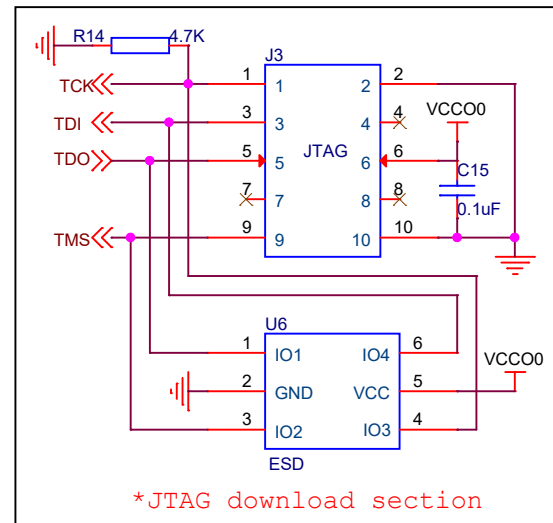
2.It is recommended that add an ESD protection chip to the JTAG download circuit.

RECONFIG_N << R9 4.7K VCCO0
*Configuration reset section

READY << R10 4.7K VCCO0
*Configurable detection section

DONE << LED2 R11 1K R12 4.7K VCCO0
*Configuration completed detection section

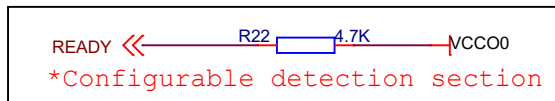
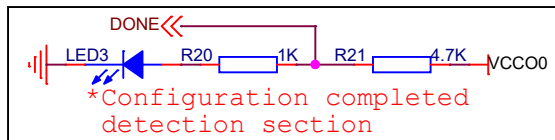
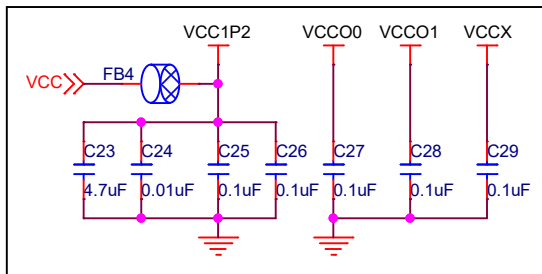
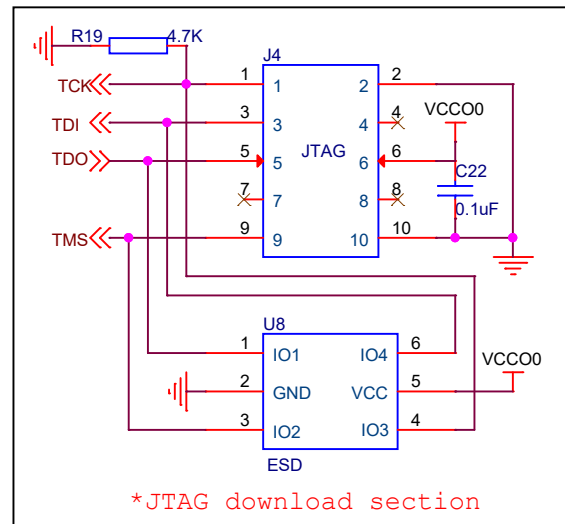
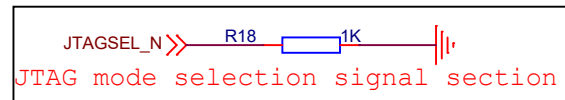
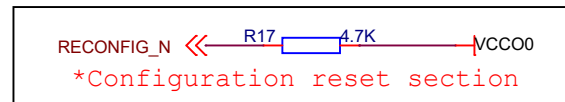
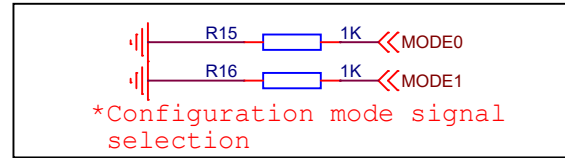
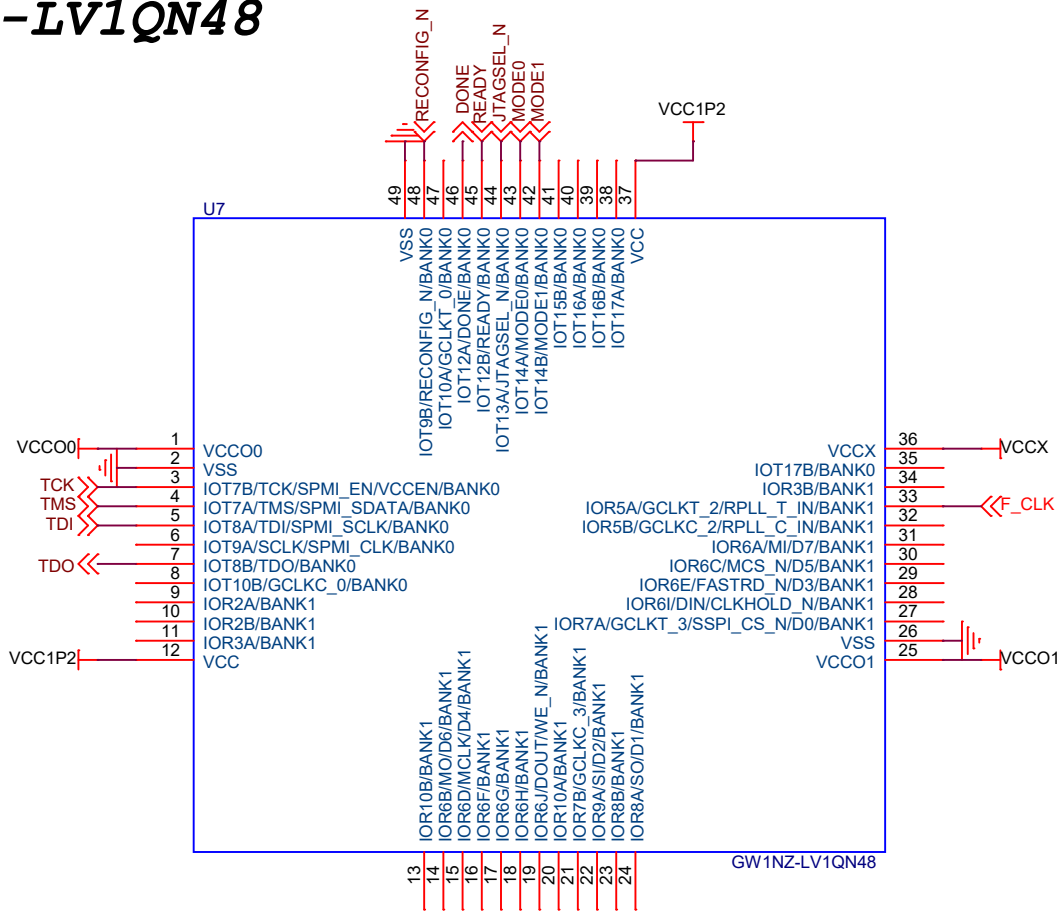
JTAGSEL_N >> R13 1K
JTAG mode selection signal section



*JTAG download section

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
A4	GW1NZ-LV1FN32F	2.0
Date:	Wednesday, April 26, 2023	Sheet 3 of 8

GW1NZ-LV1QN48



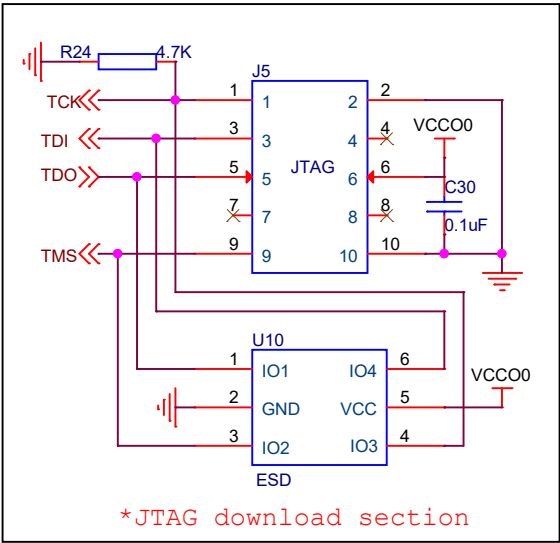
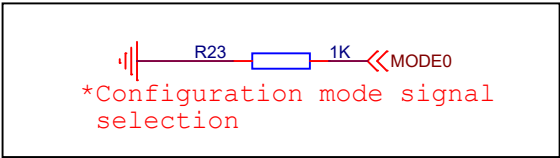
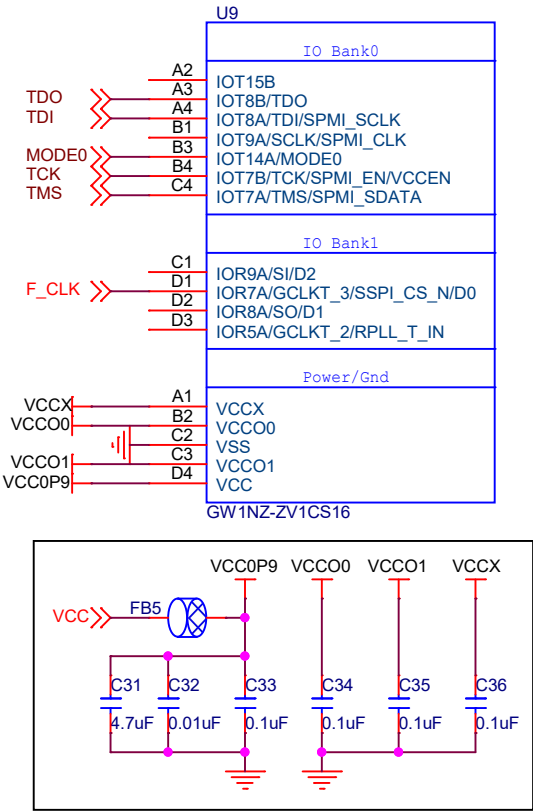
Notes:

1.F_CLK signal is an external input clock signal.

It is recommended that F_CLK signal be provided through an active oscillator crystal.

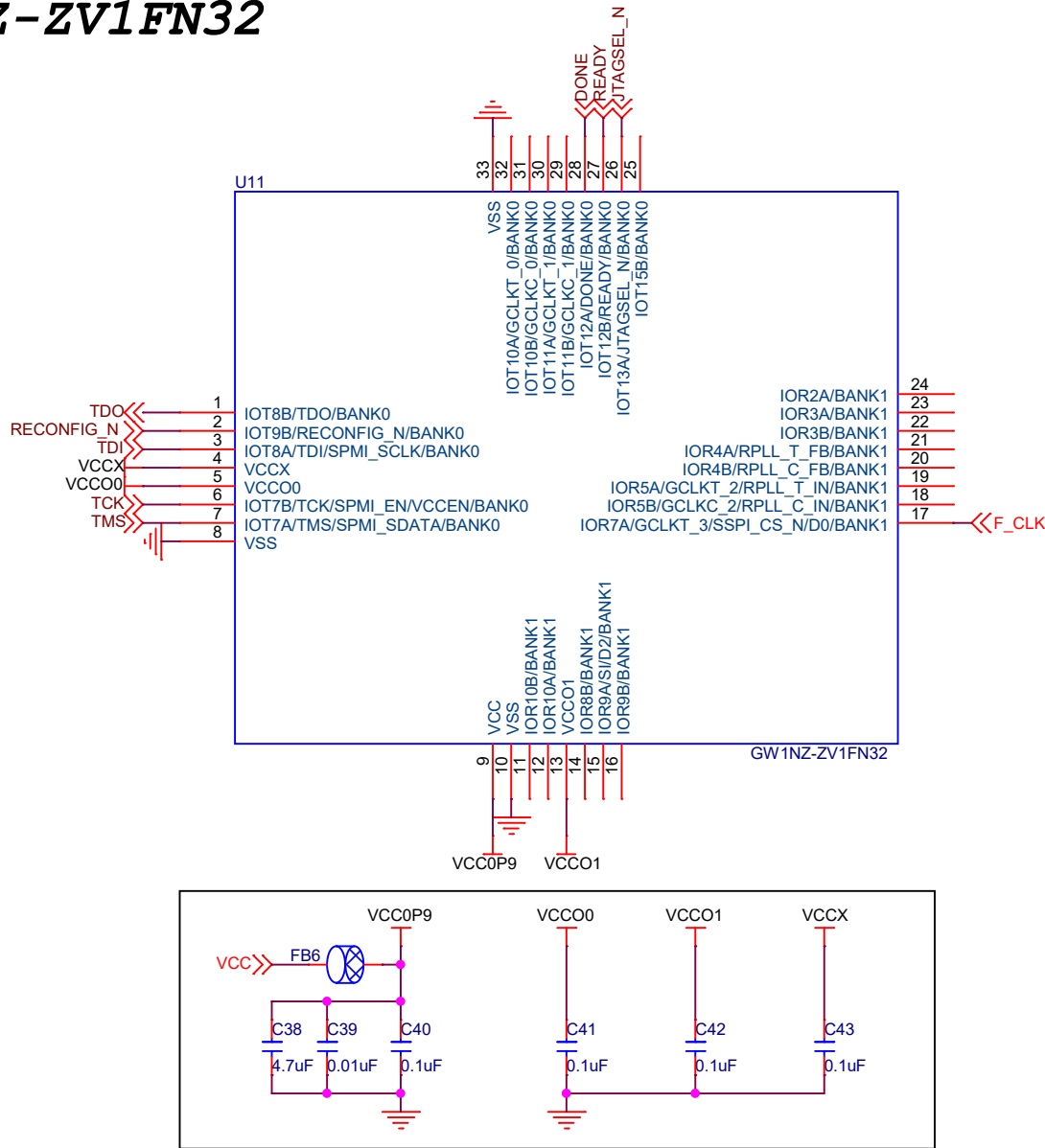
2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
A4	GW1NZ-LV1QN48	2.0
Date:	Wednesday, April 26, 2023	Sheet 4 of 8



- Notes:
- 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
 - 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

GW1NZ-ZV1FN32



Notes:

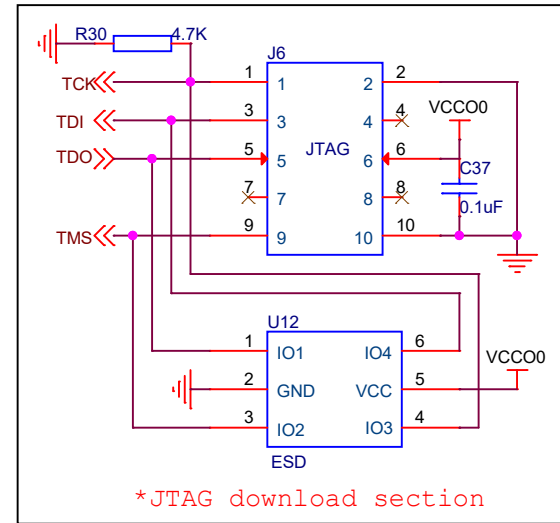
- 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

RECONFIG_N << R25 4.7K VCCO0
*Configuration reset section

READY << R26 4.7K VCCO0
*Configurable detection section

DONE << LED4 R27 1K R28 4.7K VCCO0
*Configuration completed detection section

JTAGSEL_N >> R29 1K
JTAG mode selection signal section



Title
GOWIN Minimum System Diagram

Size
A4

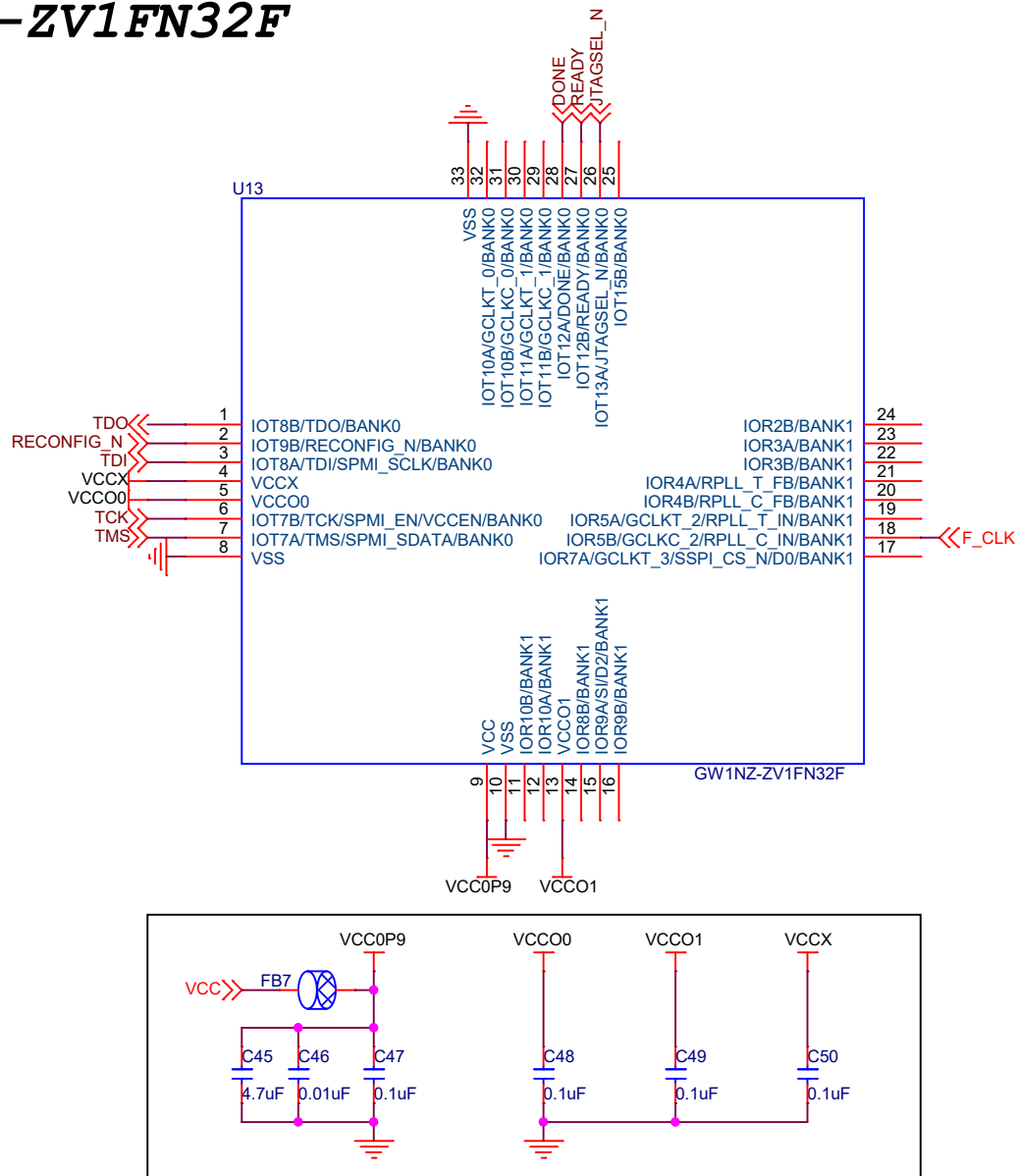
Document Number
GW1NZ-ZV1FN32

Rev
2.0

Date: Wednesday, April 26, 2023

Sheet 6 of 8

GW1NZ-ZV1FN32F



Notes:

1.F_CLK signal is an external input clock signal.

It is recommended that F_CLK signal be provided through an active oscillator crystal.

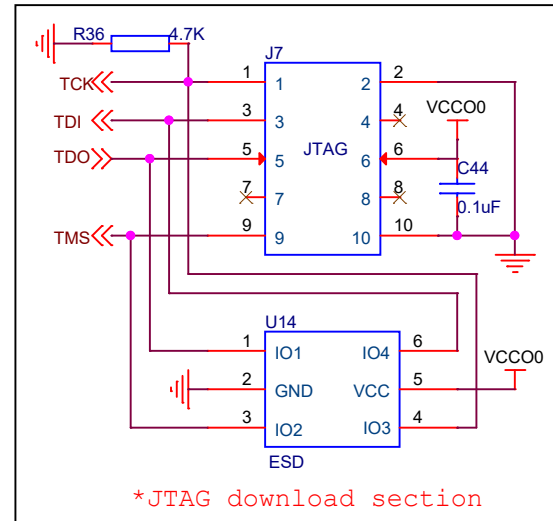
2.It is recommended that add an ESD protection chip to the JTAG download circuit.

RECONFIG_N << R31 4.7K VCCO0
*Configuration reset section

READY << R32 4.7K VCCO0
*Configurable detection section

DONE << LED5 R33 1K R34 4.7K VCCO0
*Configuration completed detection section

JTAGSEL_N >> R35 1K
JTAG mode selection signal section



Title
GOWIN Minimum System Diagram

Size
A4

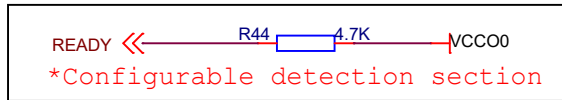
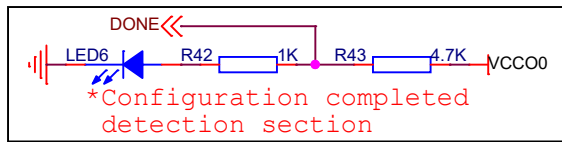
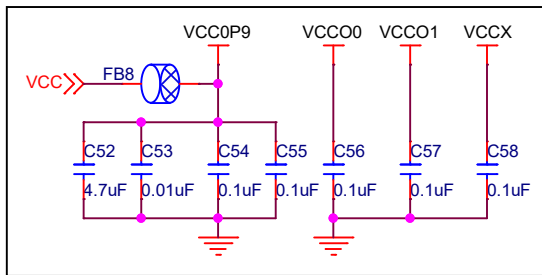
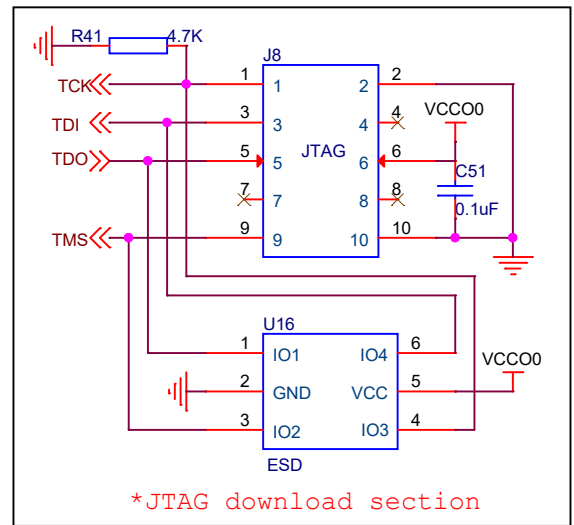
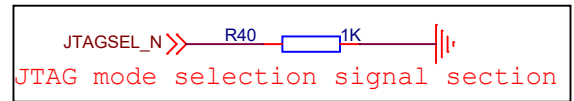
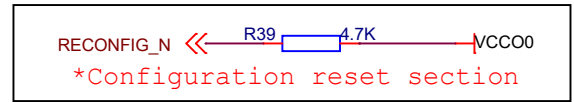
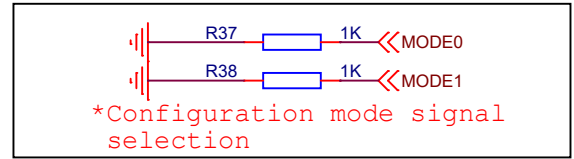
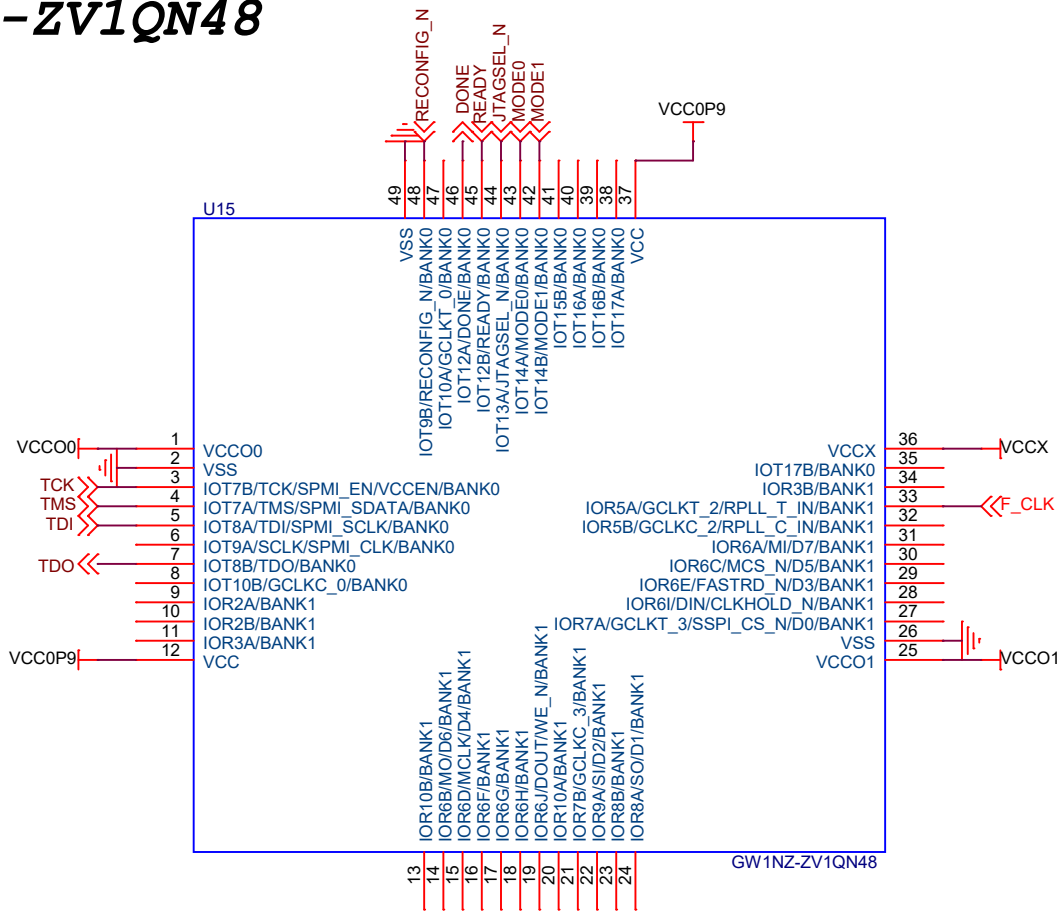
Document Number
GW1NZ-ZV1FN32F

Rev
2.0

Date: Wednesday, April 26, 2023

Sheet 7 of 8

GW1NZ-ZV1QN48



Notes:

1.F_CLK signal is an external input clock signal.

It is recommended that F_CLK signal be provided through an active oscillator crystal.

2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title
GOWIN Minimum System Diagram

Size
A4

Document Number
GW1NZ-ZV1QN48

Rev
2.0

Date: Wednesday, April 26, 2023

Sheet 8 of 8