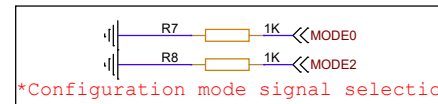
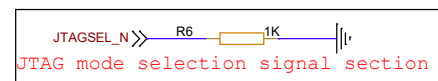
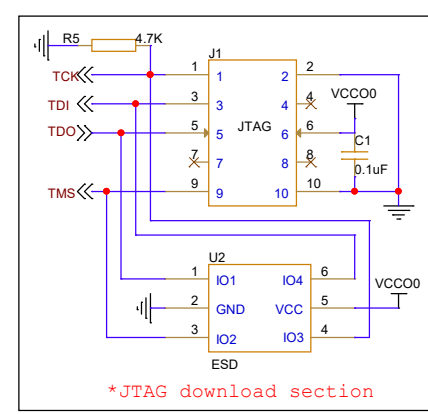
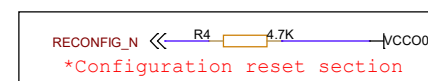
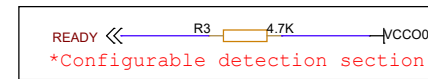
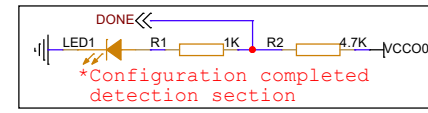
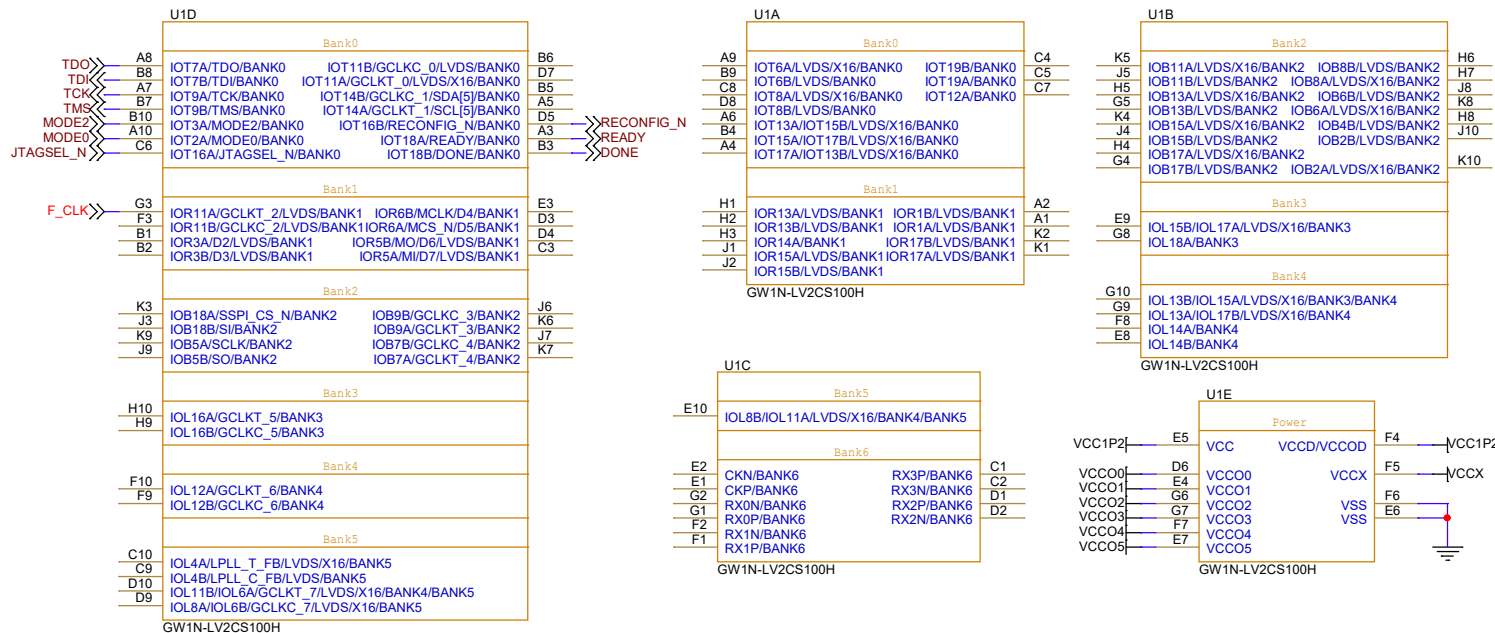


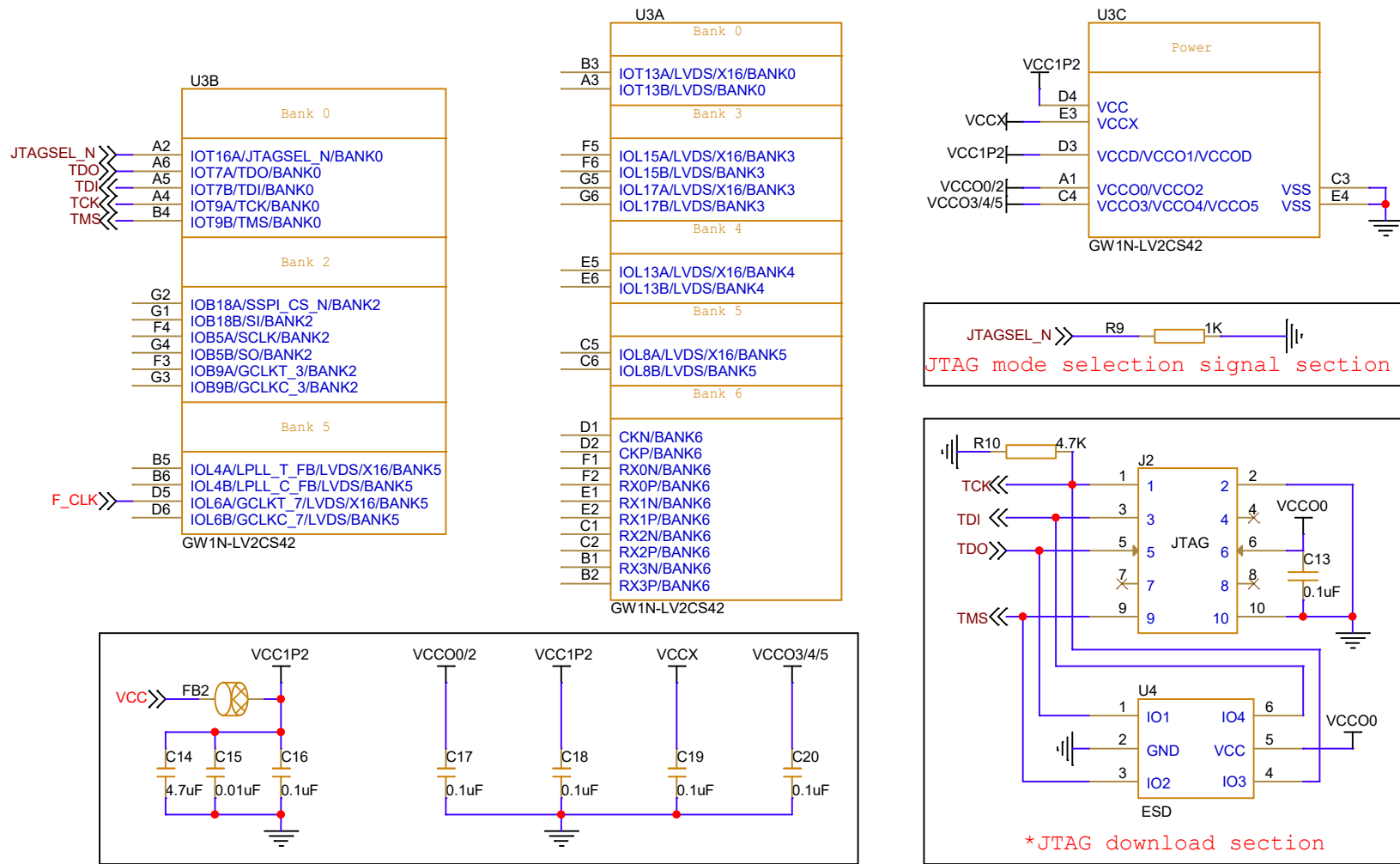
# GW1N-LV2CS100H



Notes:

- 1.F CLK signal is an external input clock signal.
- It is recommended that F CLK signal be provided through an active oscillator crystal.
- It is recommended that add an ESD protection chip to the JTAG download circuit.

# GW1N-LV2CS42

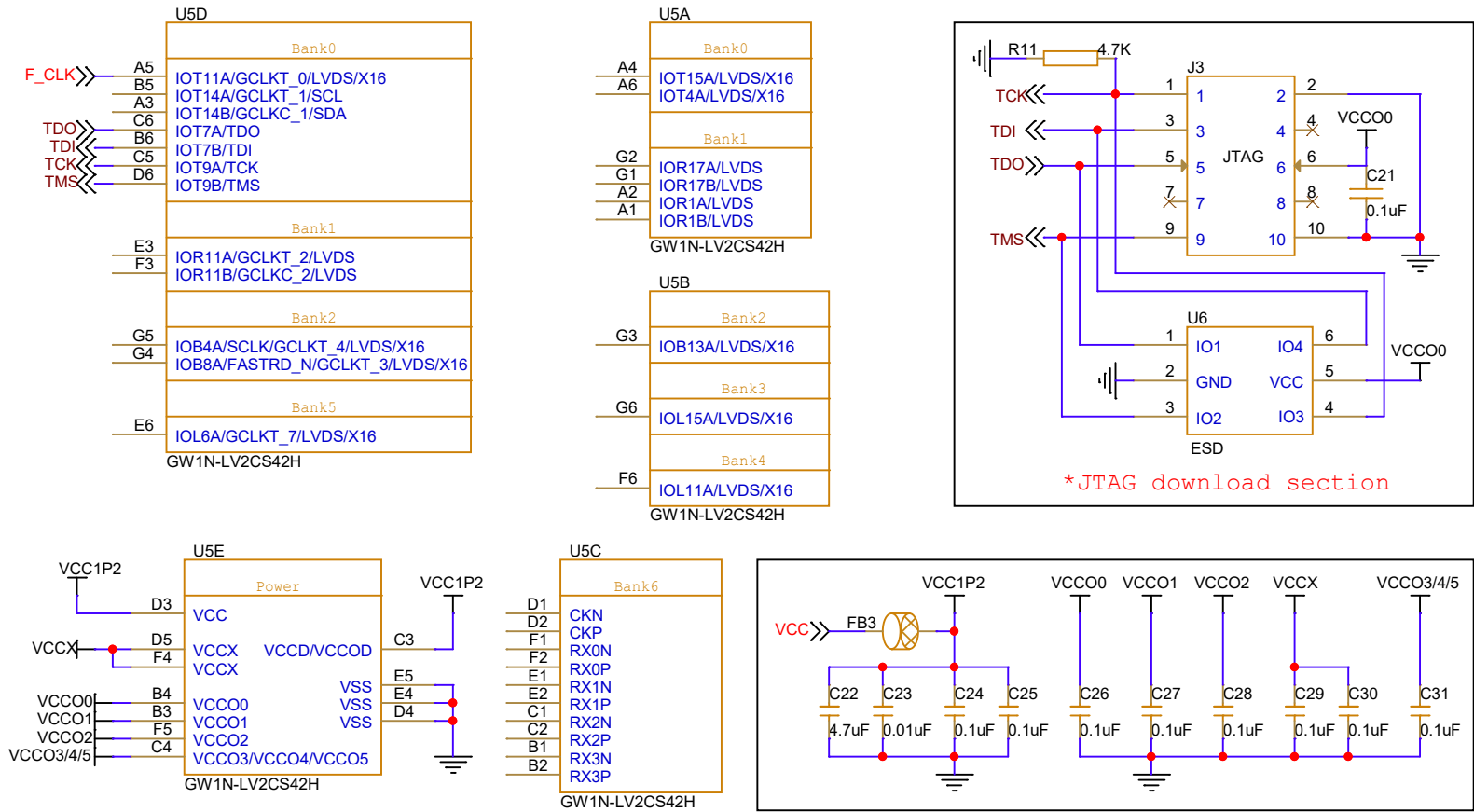


## Notes:

- 1.F\_CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

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GW1N-LV2CS42H



Notes:

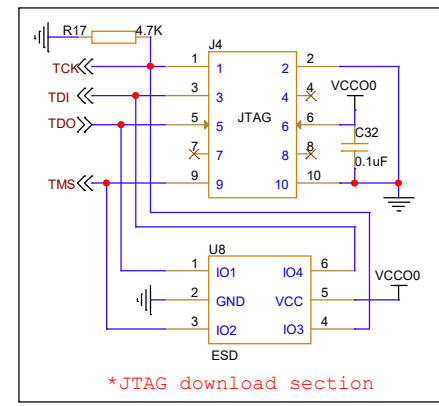
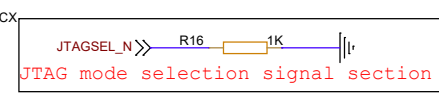
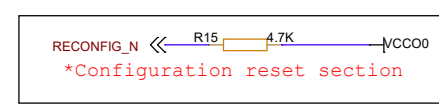
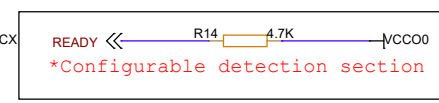
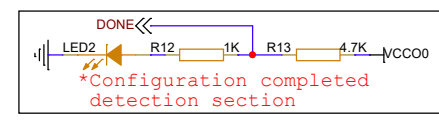
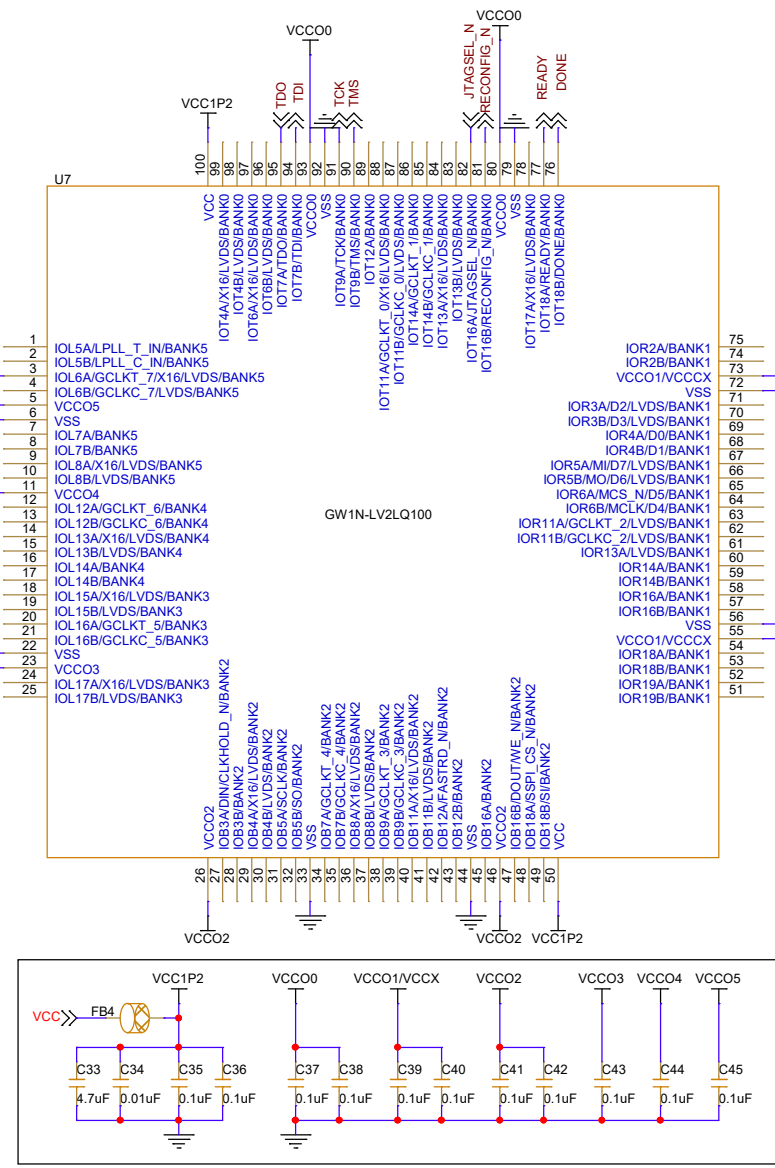
- 1.F\_CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

D

C

B

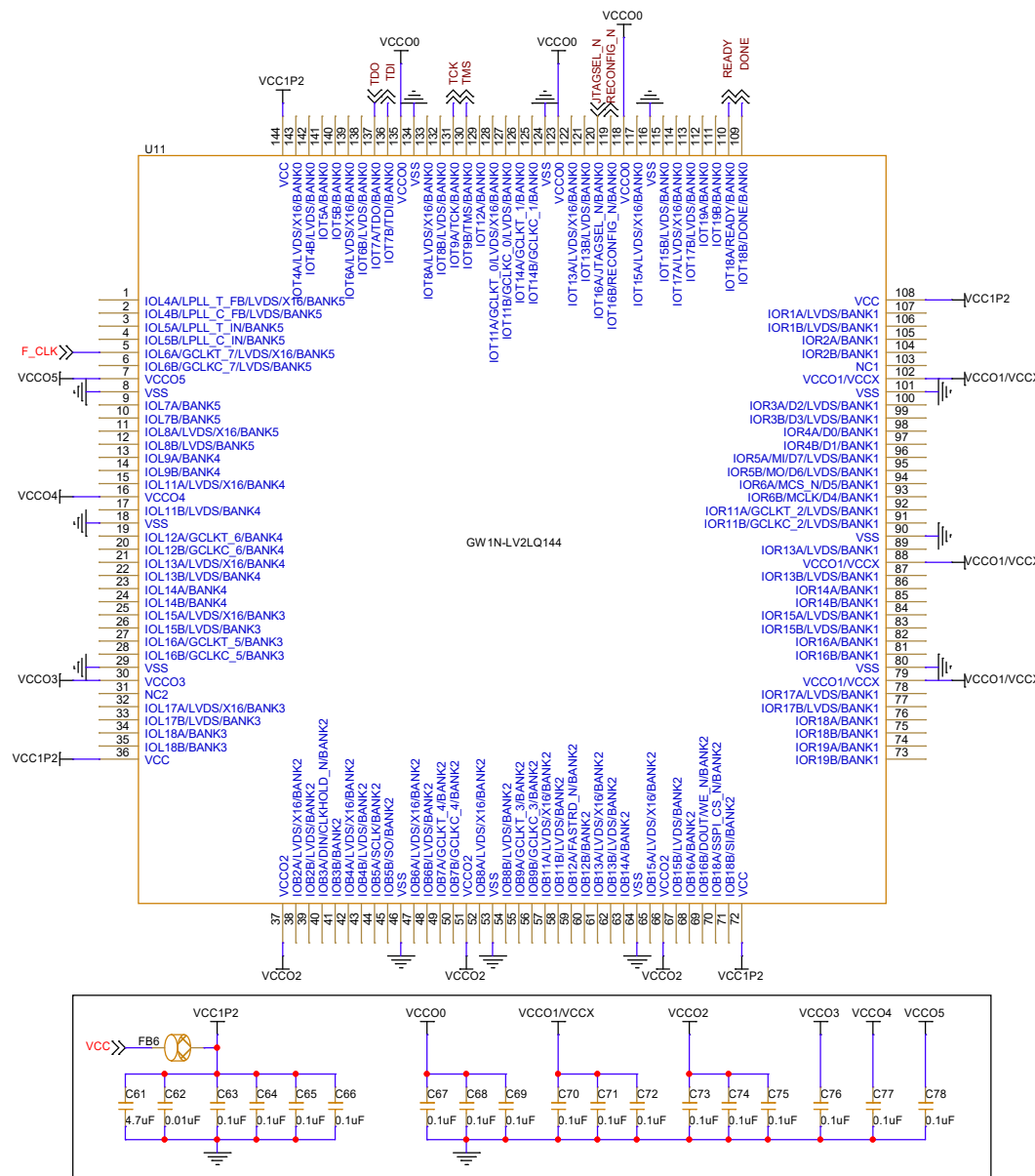
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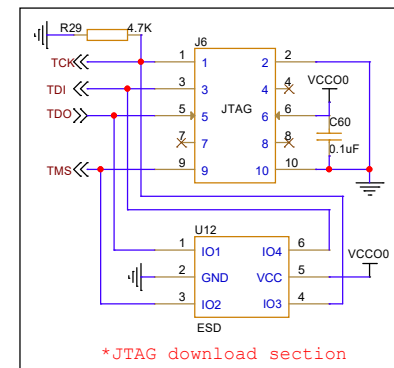
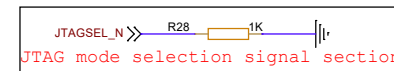
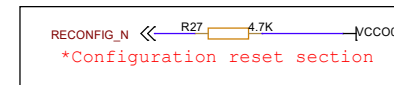
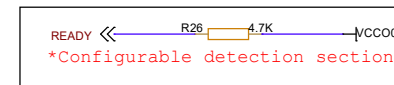
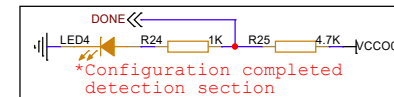
Notes:  
 1.F CLK signal is an external input clock signal.  
 It is recommended that F\_CLK signal be provided through an active oscillator crystal.  
 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

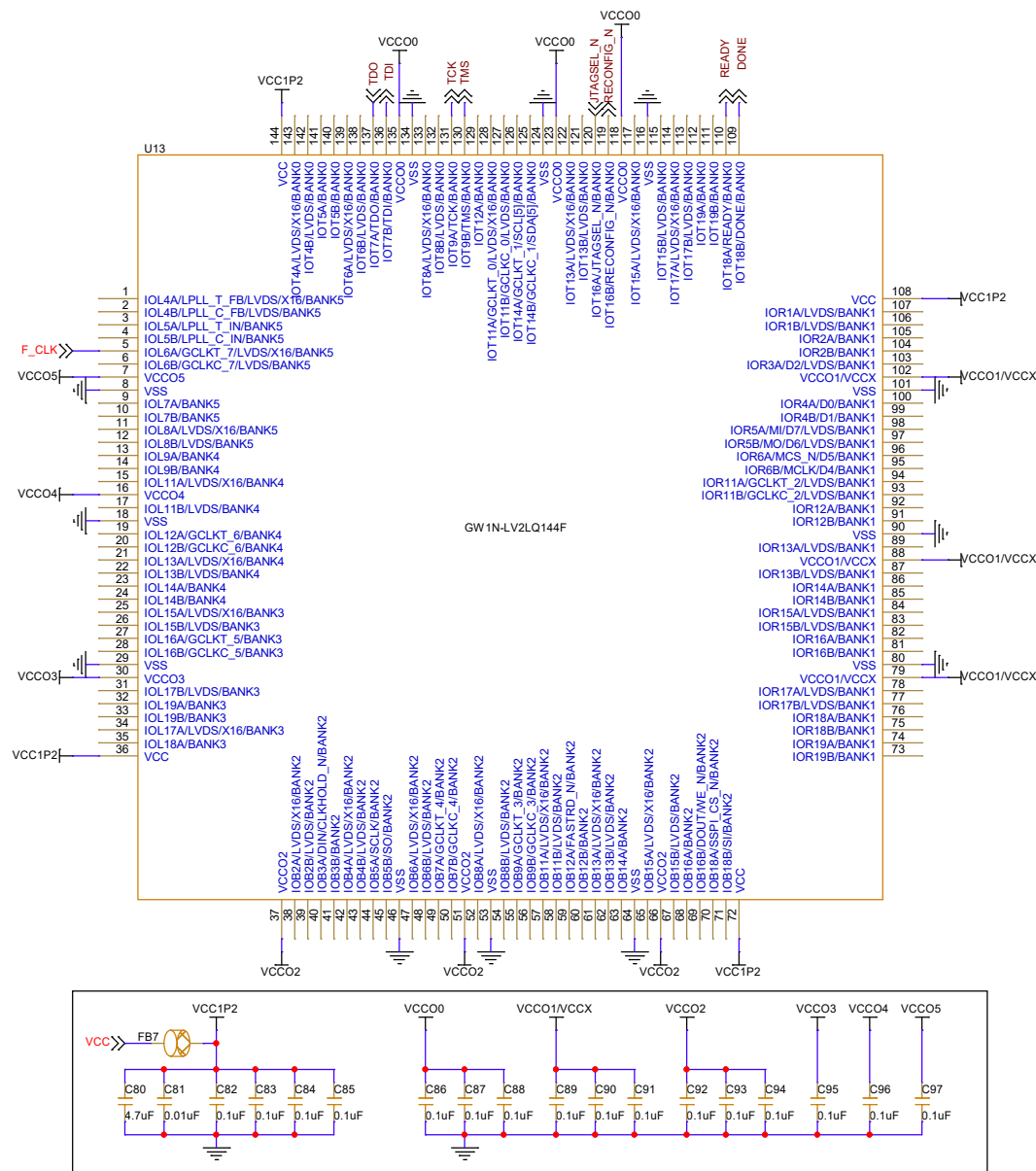
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GOWIN Minimum System Diagram		
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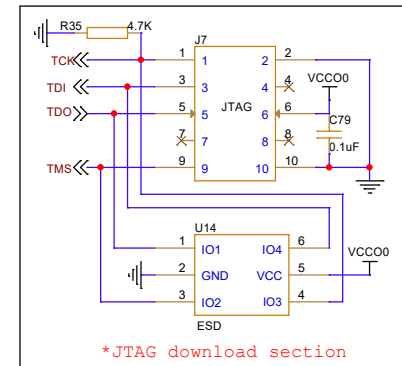
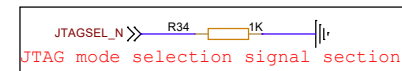
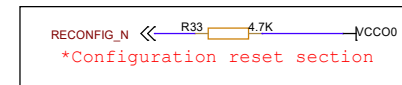
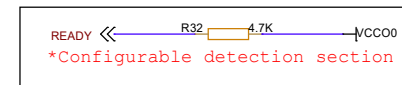
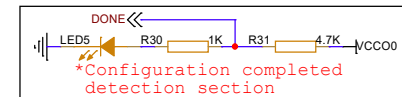


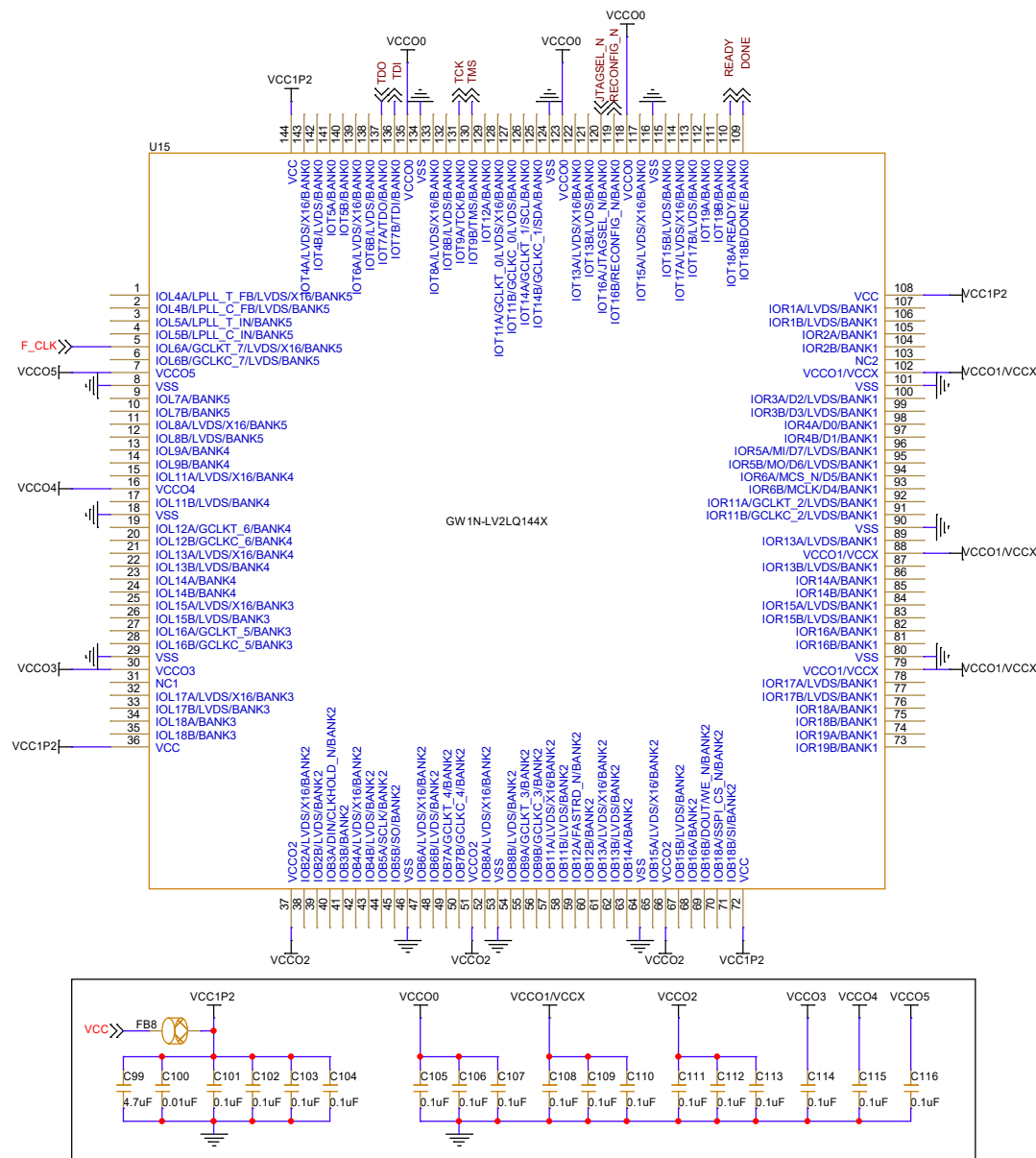
Notes:  
 1.F\_CLK signal is an external input clock signal.  
 It is recommended that F\_CLK signal be provided through an active oscillator crystal.  
 2.It is recommended that add an ESD protection chip to the JTAG download circuit.



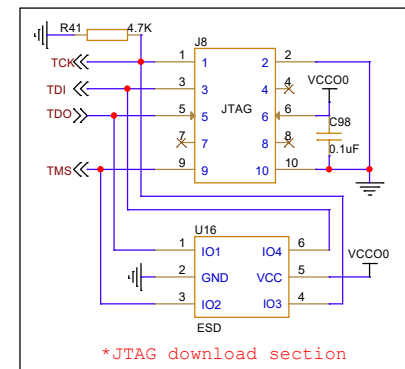
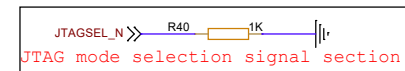
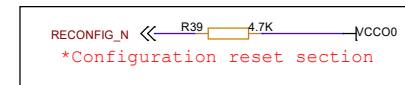
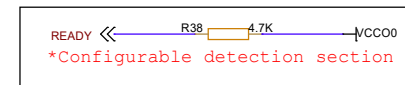
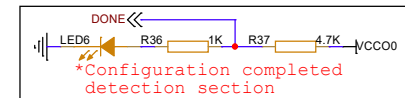


Notes:  
 1.F\_CLK signal is an external input clock signal.  
 It is recommended that F\_CLK signal be provided through an active oscillator crystal.  
 2.It is recommended that add an ESD protection chip to the JTAG download circuit.



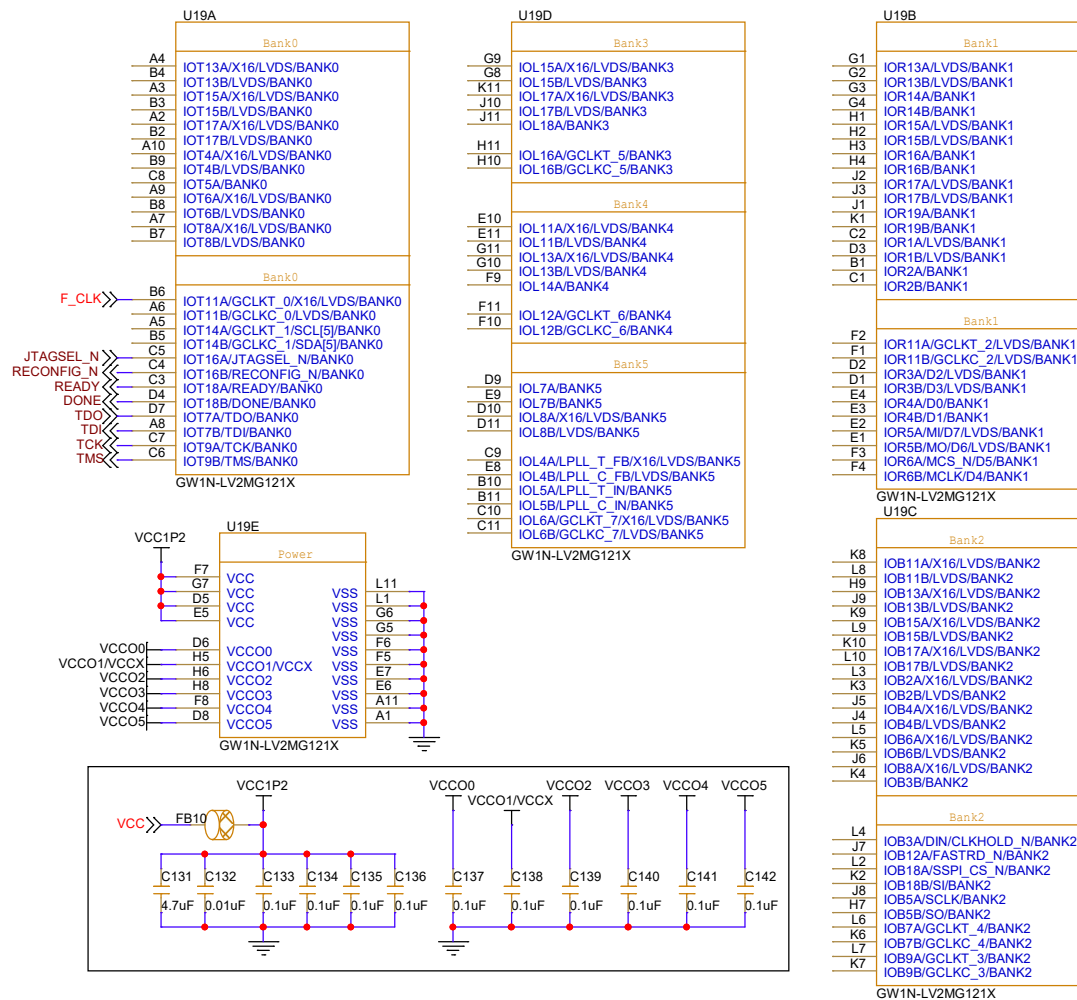


Notes:  
 1.F\_CLK signal is an external input clock signal.  
 It is recommended that F\_CLK signal be provided through an active oscillator crystal.  
 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

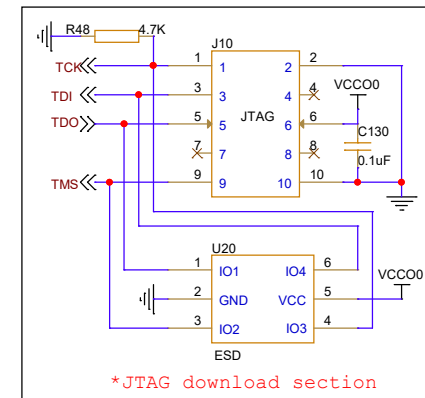


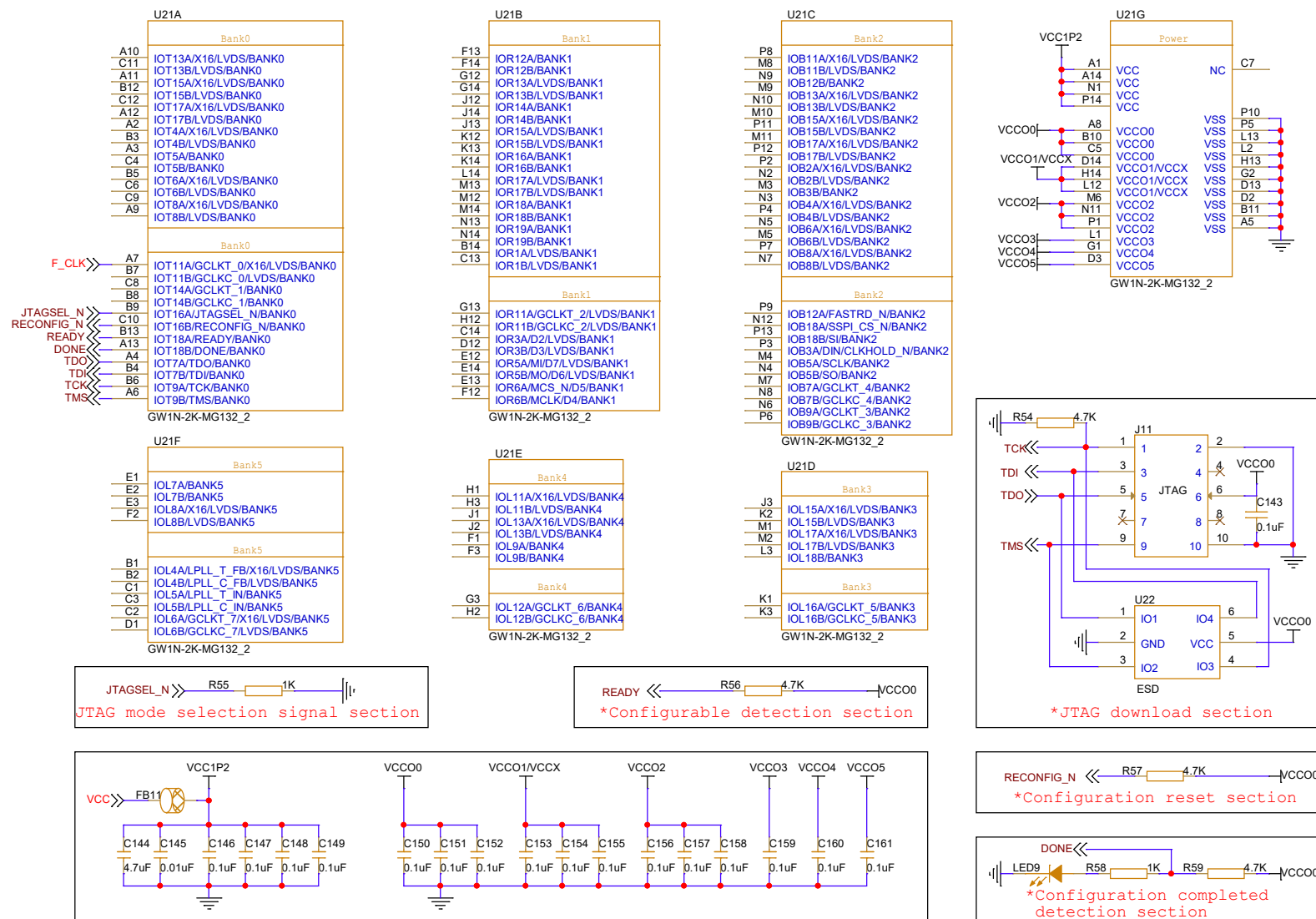




**Notes:**

- 1.F\_CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

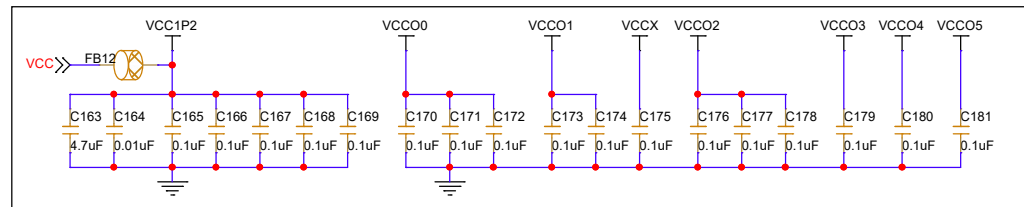
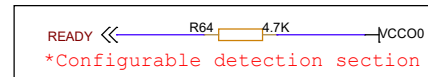
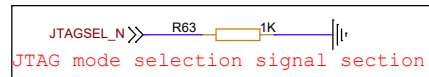
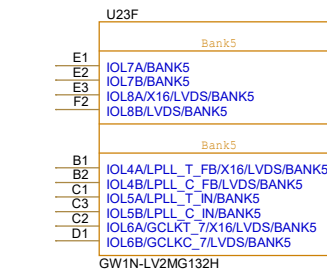
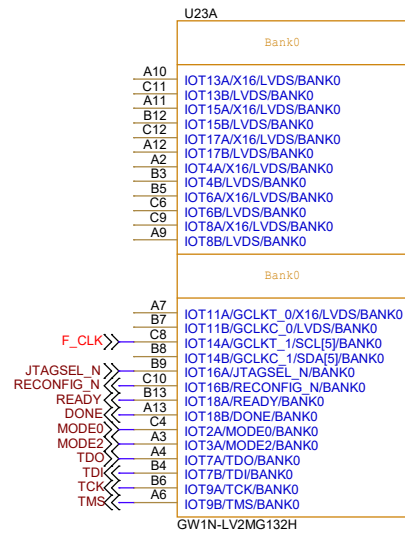




## Notes:

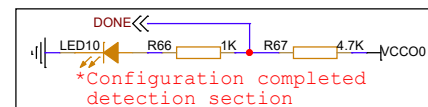
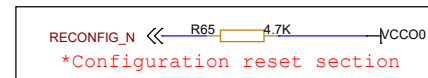
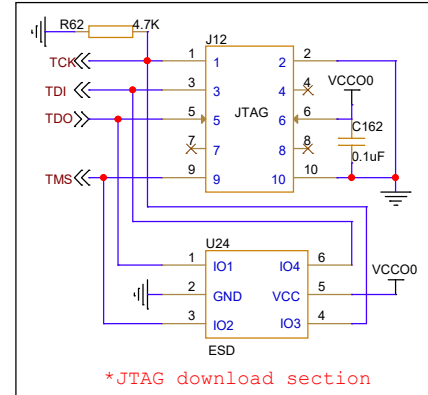
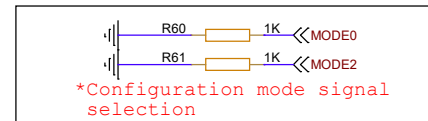
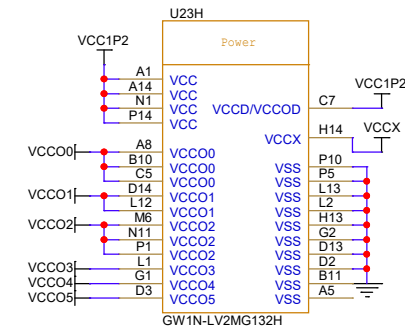
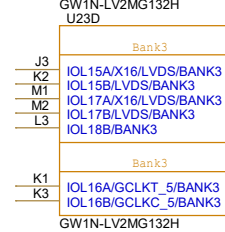
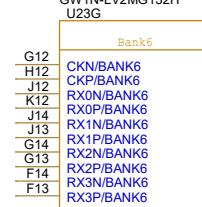
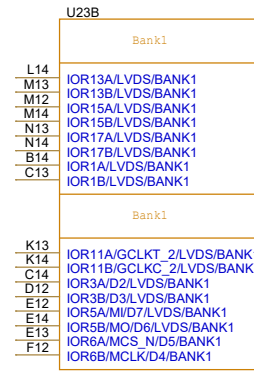
- 1.F CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
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B	GW1N-LV2MG132	2.0
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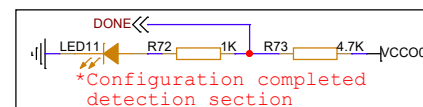
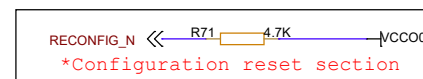
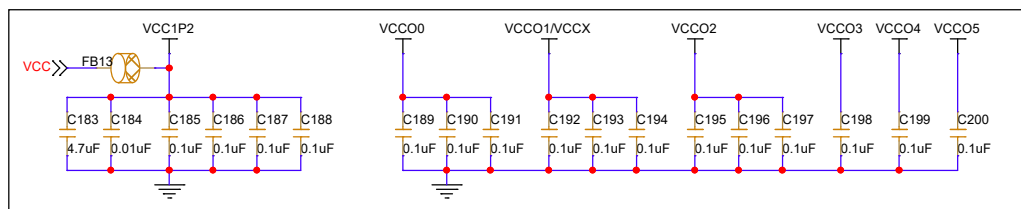
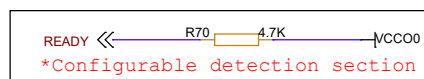
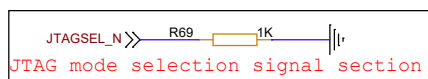
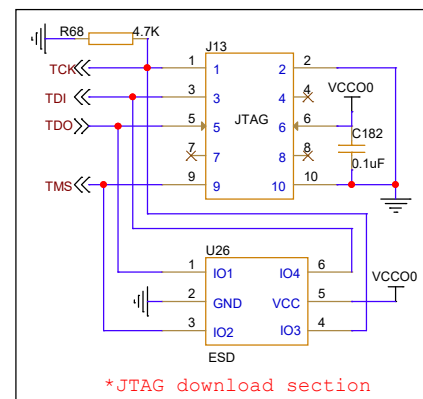
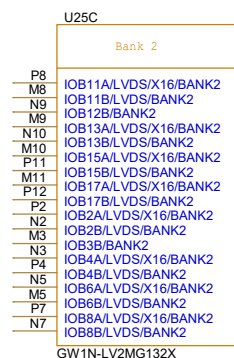
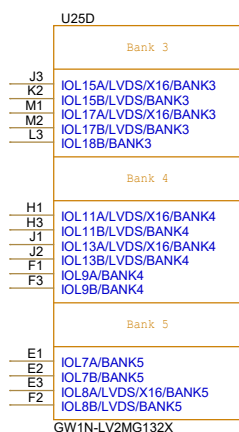
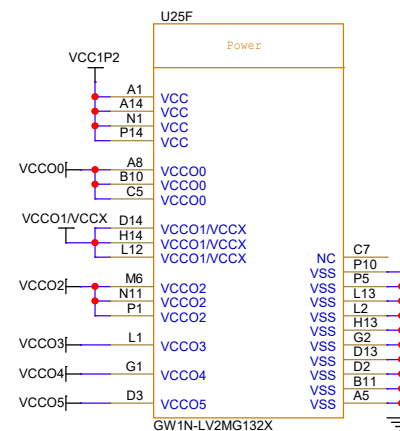
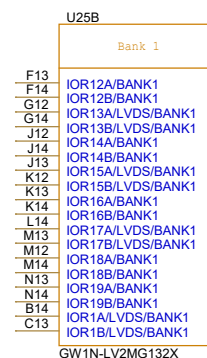
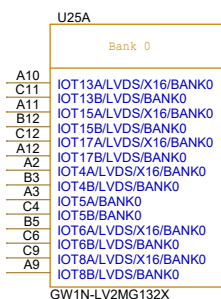
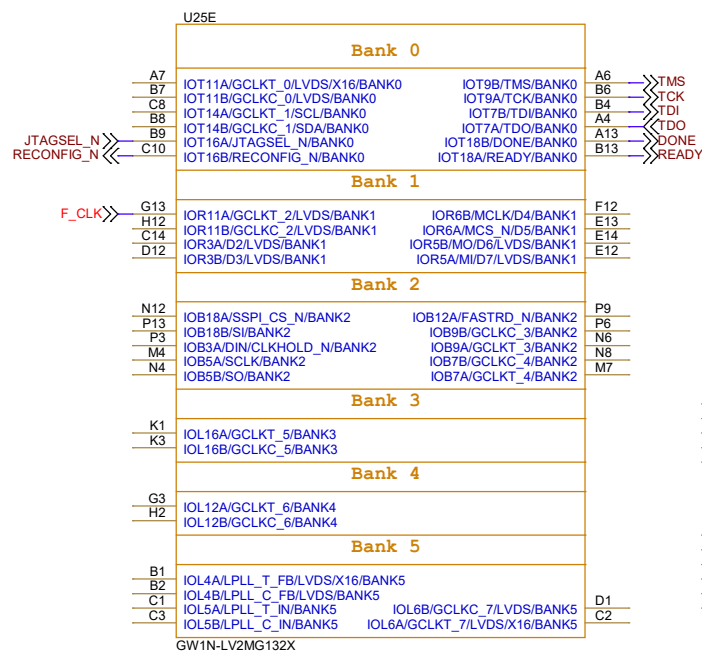


Notes:

- 1.F CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.



Title		
GOWIN Minimum System Diagram		
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B	GW1N-LV2MG132H	2.0
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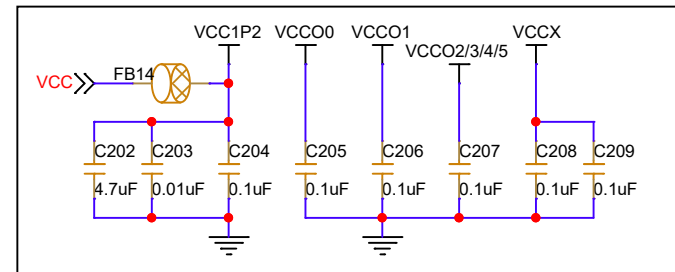
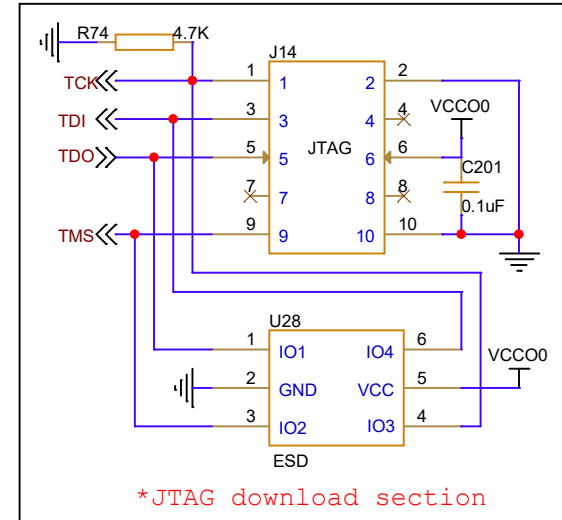
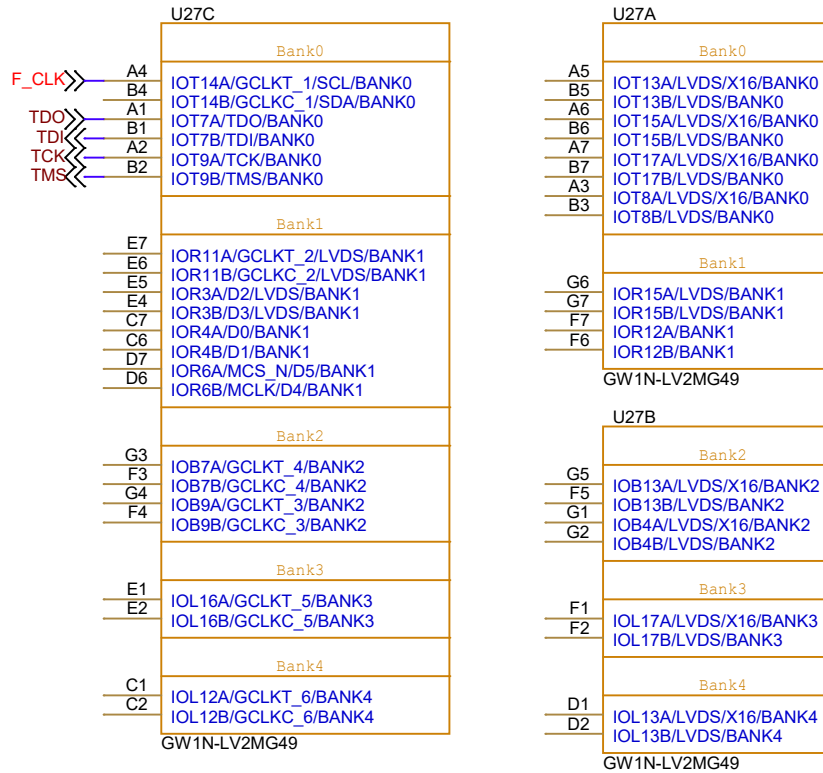


Notes:

1. F\_CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.

Title				
GOWIN Minimum System Diagram				
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# GW1N-LV2MG49



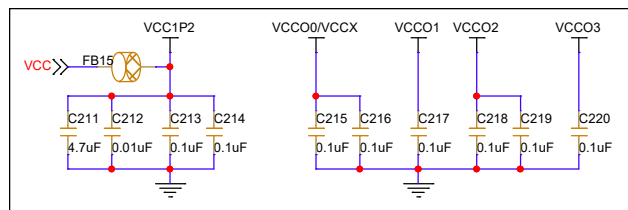
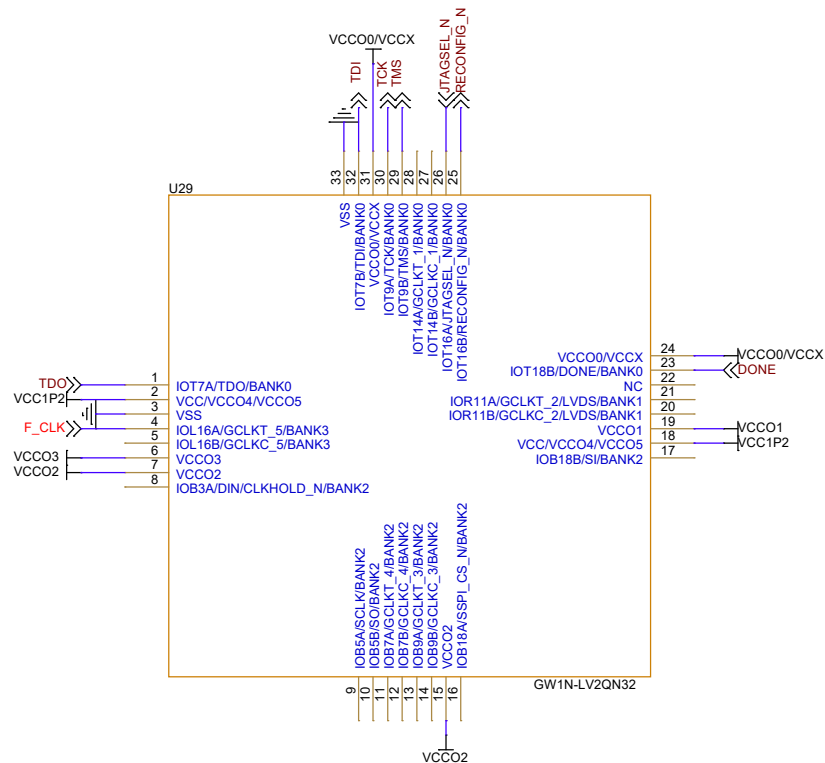
## Notes:

1.F\_CLK signal is an external input clock signal.

It is recommended that F\_CLK signal be provided through an active oscillator crystal.

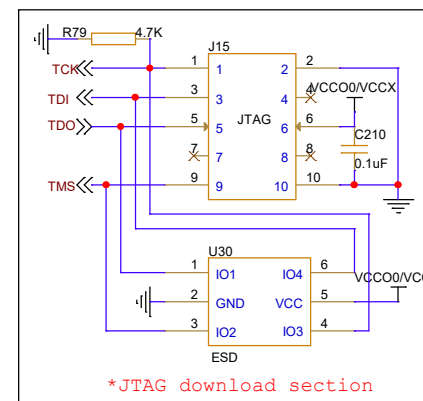
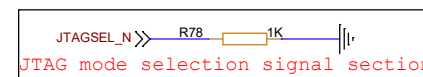
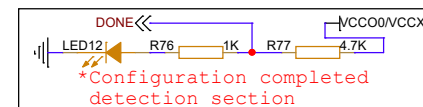
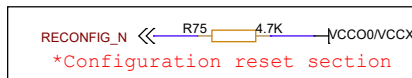
2.It is recommended that add an ESD protection chip to the JTAG download circuit.

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A4	GW1N-LV2MG49	2.0
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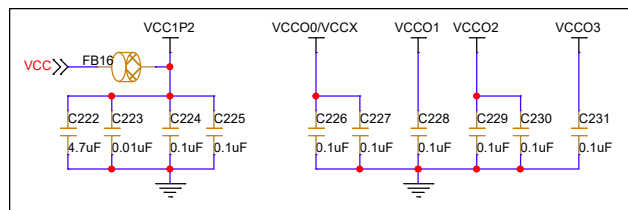
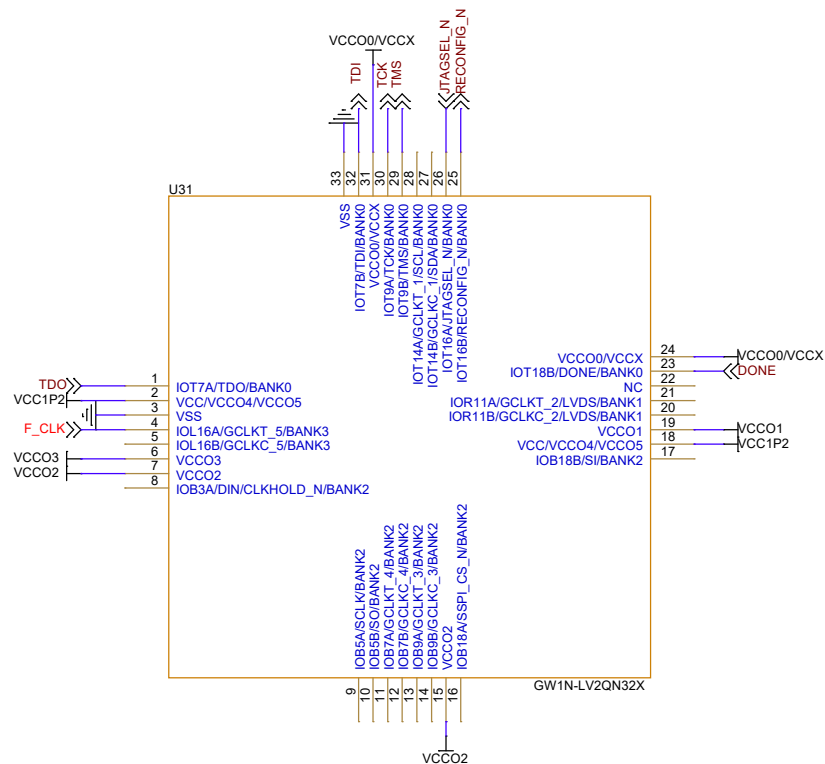
#### Notes:

- 1.F CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.



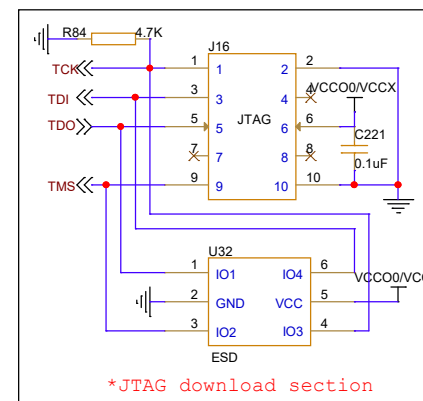
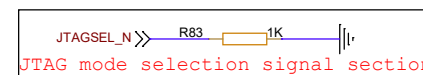
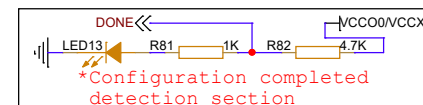
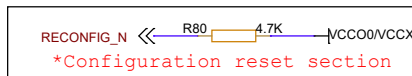
Title		
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Size	Document Number	Rev
B	GW1N-LV2QN32	2.0
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# GW1N-LV2QN32X



## Notes:

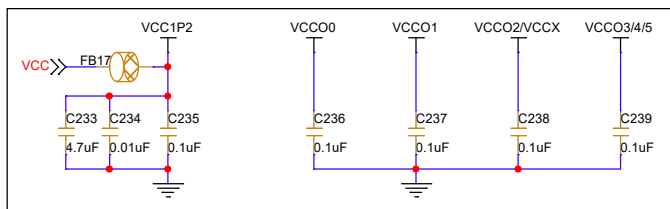
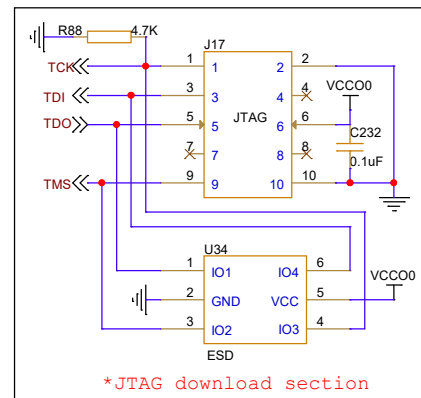
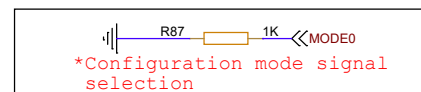
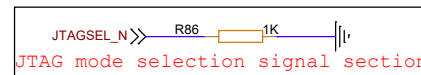
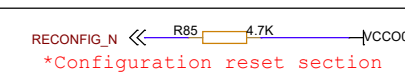
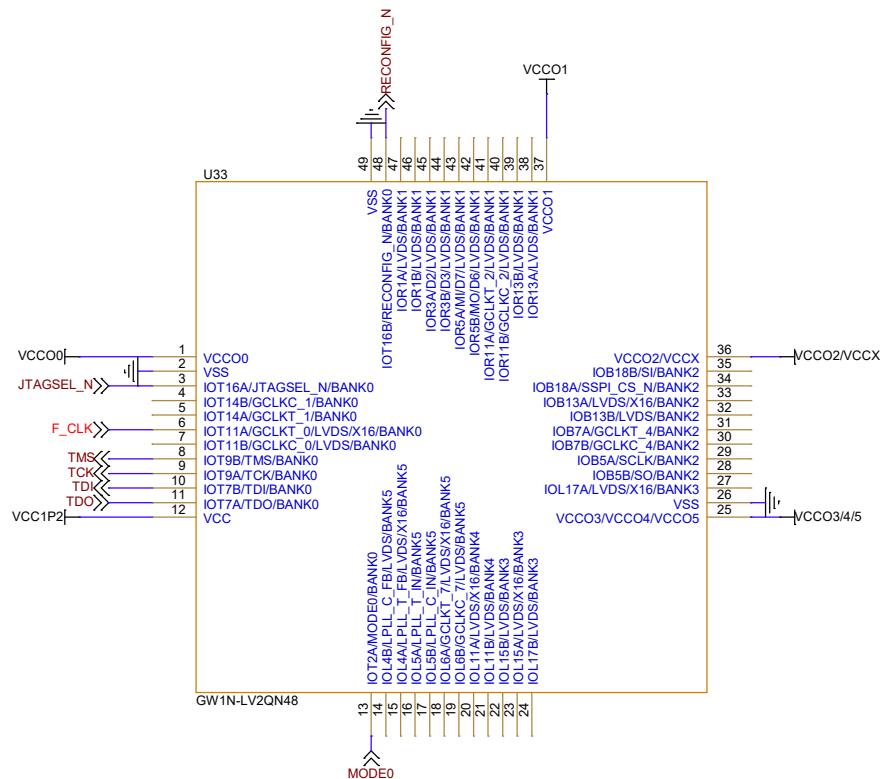
- 1.F CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection circuit to the JTAG download circuit.



Title		
GOWIN Minimum System Diagram		
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B	GW1N-LV2QN32X	2.0
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# GW1N-LV2QN48

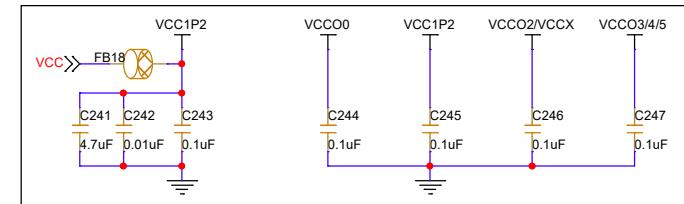
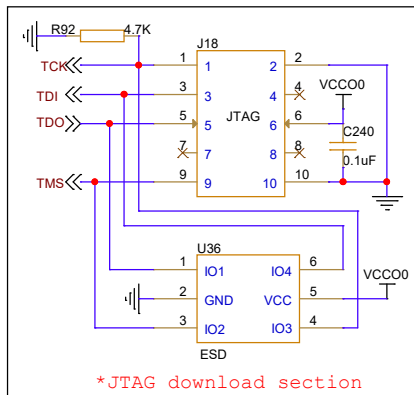
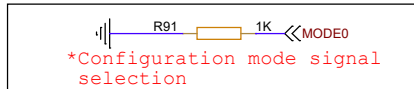
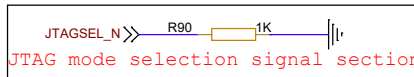
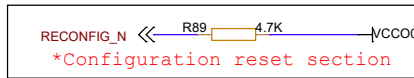
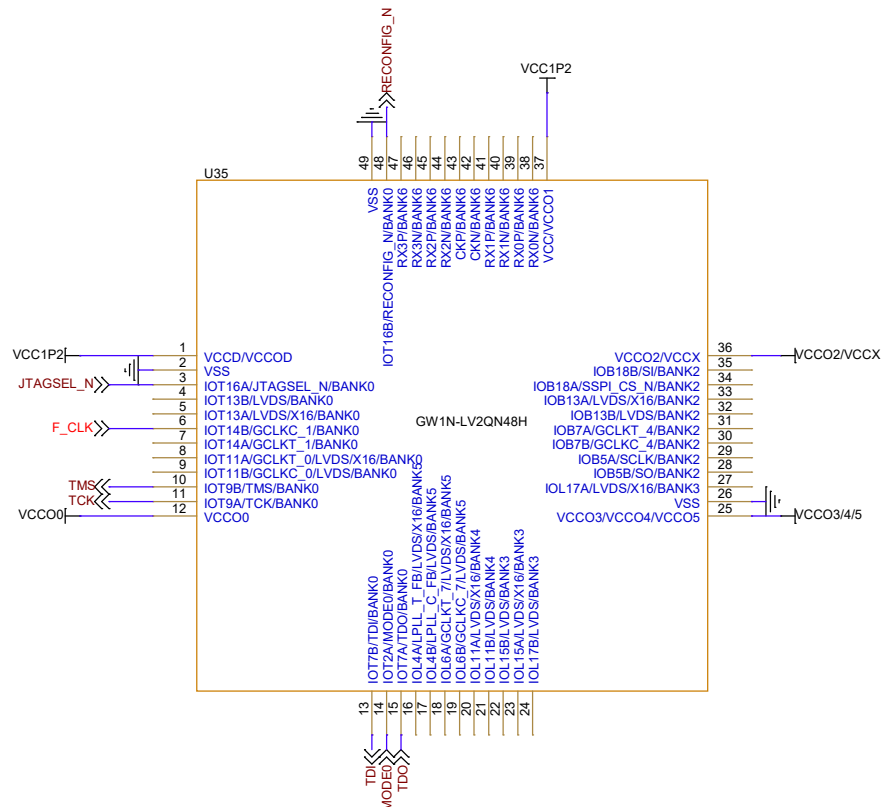


## Notes:

- 1.F CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

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GOWIN Minimum System Diagram		
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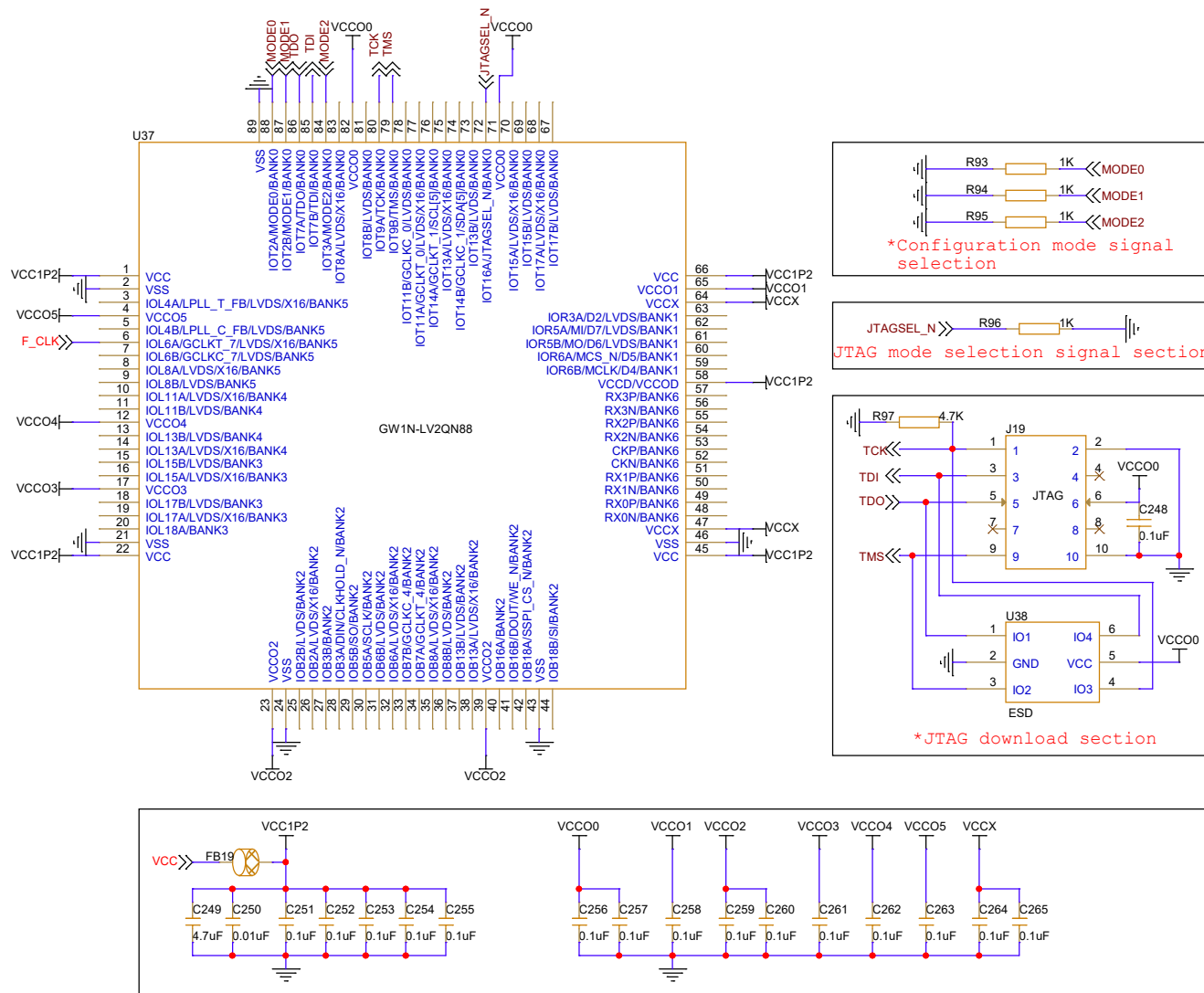
# GW1N-LV2QN48H



Notes:

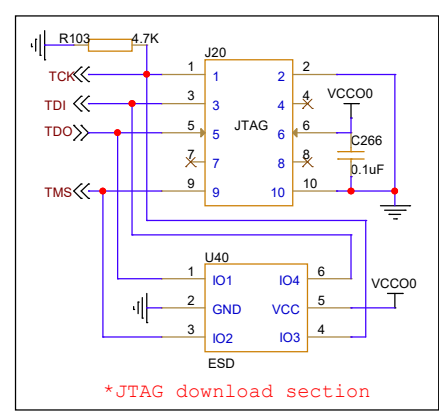
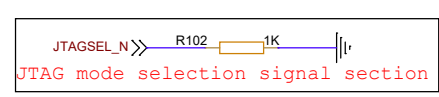
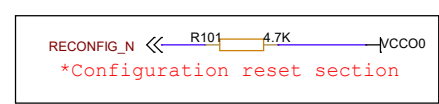
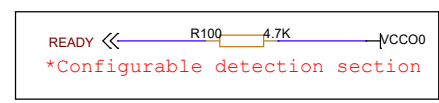
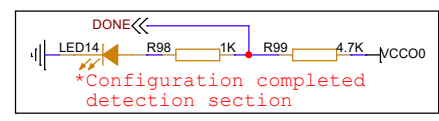
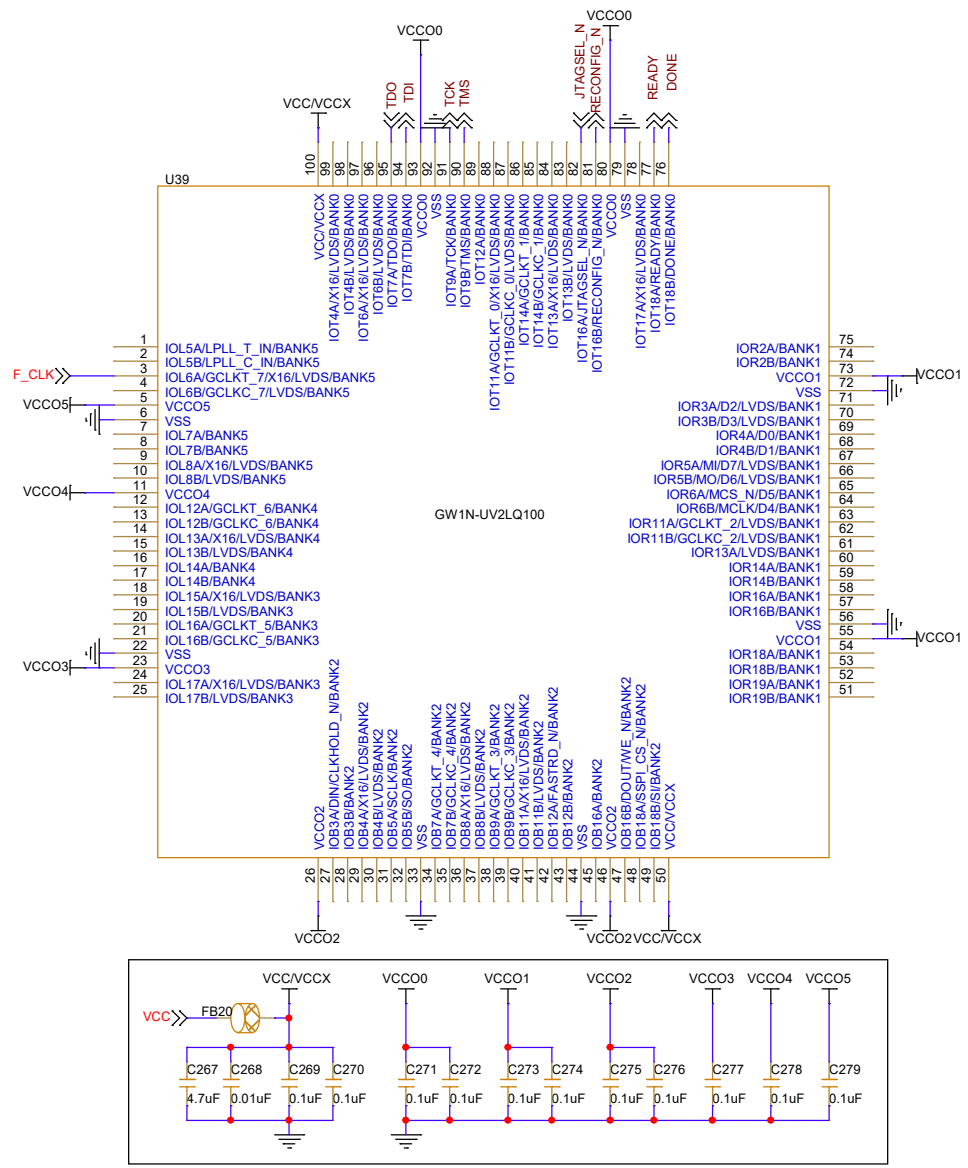
- 1.F CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

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GOWIN Minimum System Diagram		
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- Notes:
- 1.F CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
  - 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

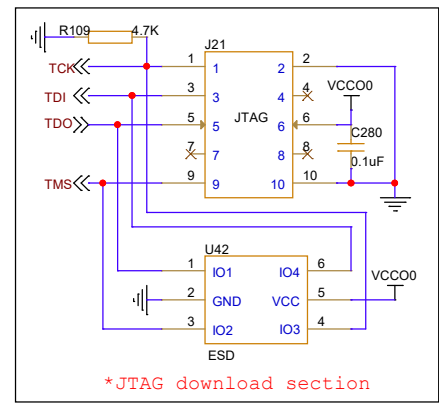
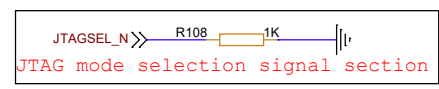
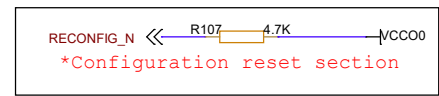
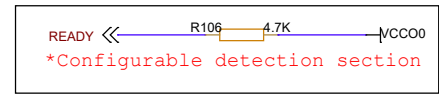
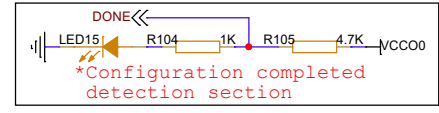
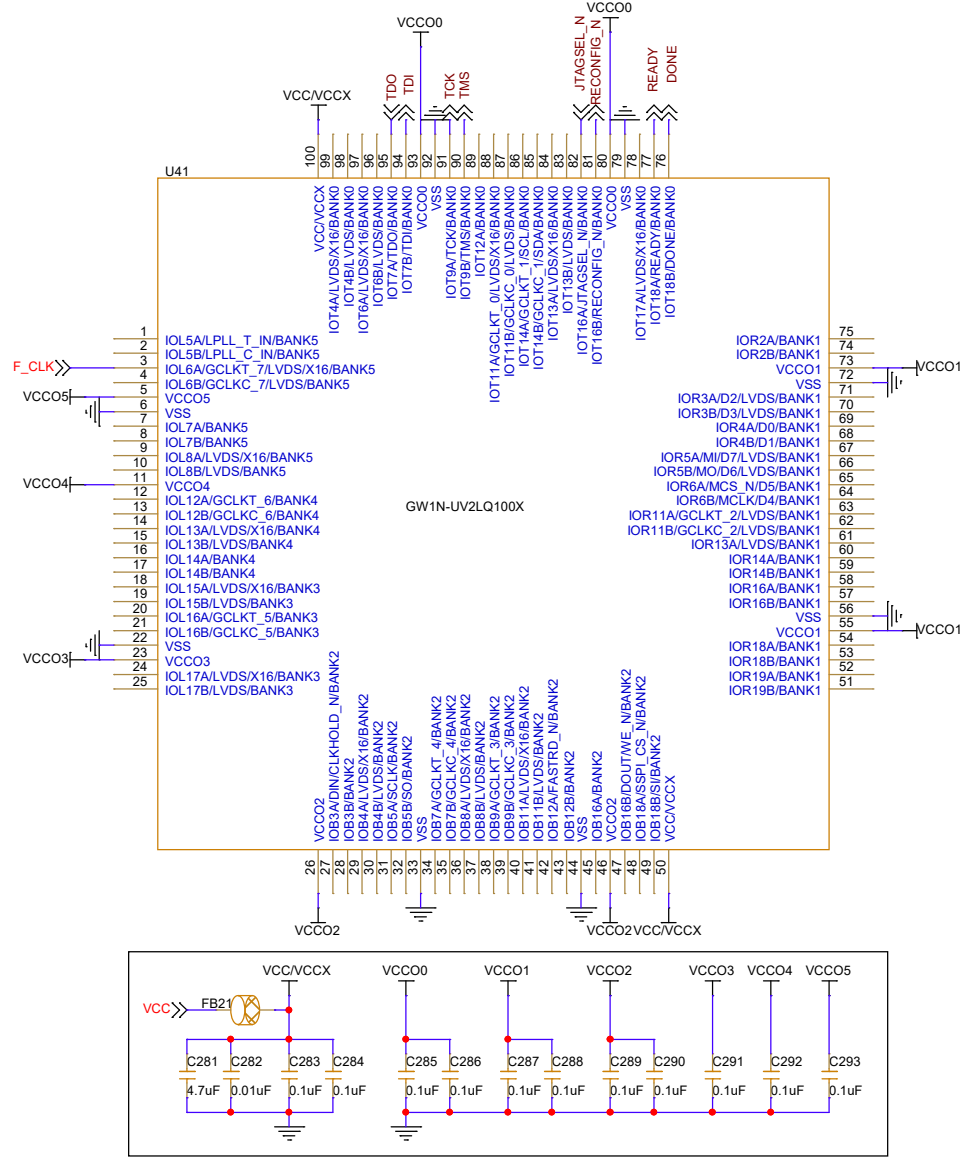
Title		
GOWIN Minimum System Diagram		
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Notes:

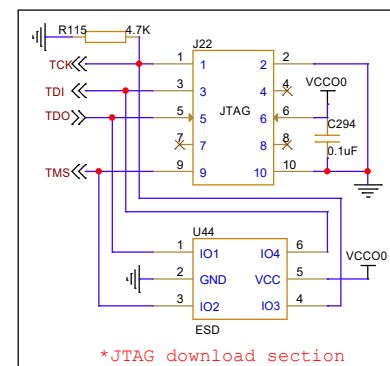
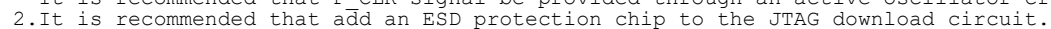
- 1.F CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

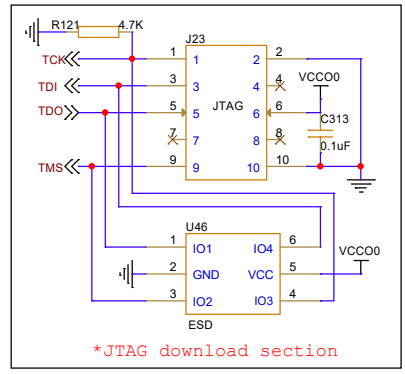
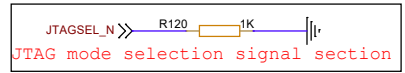
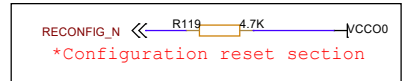
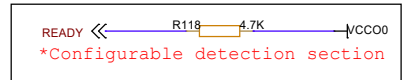
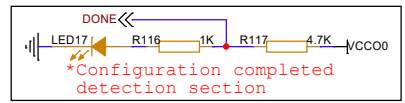
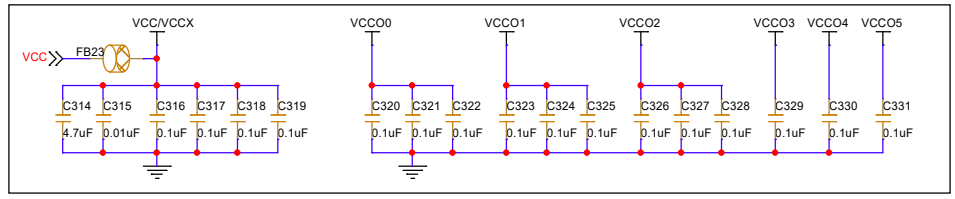
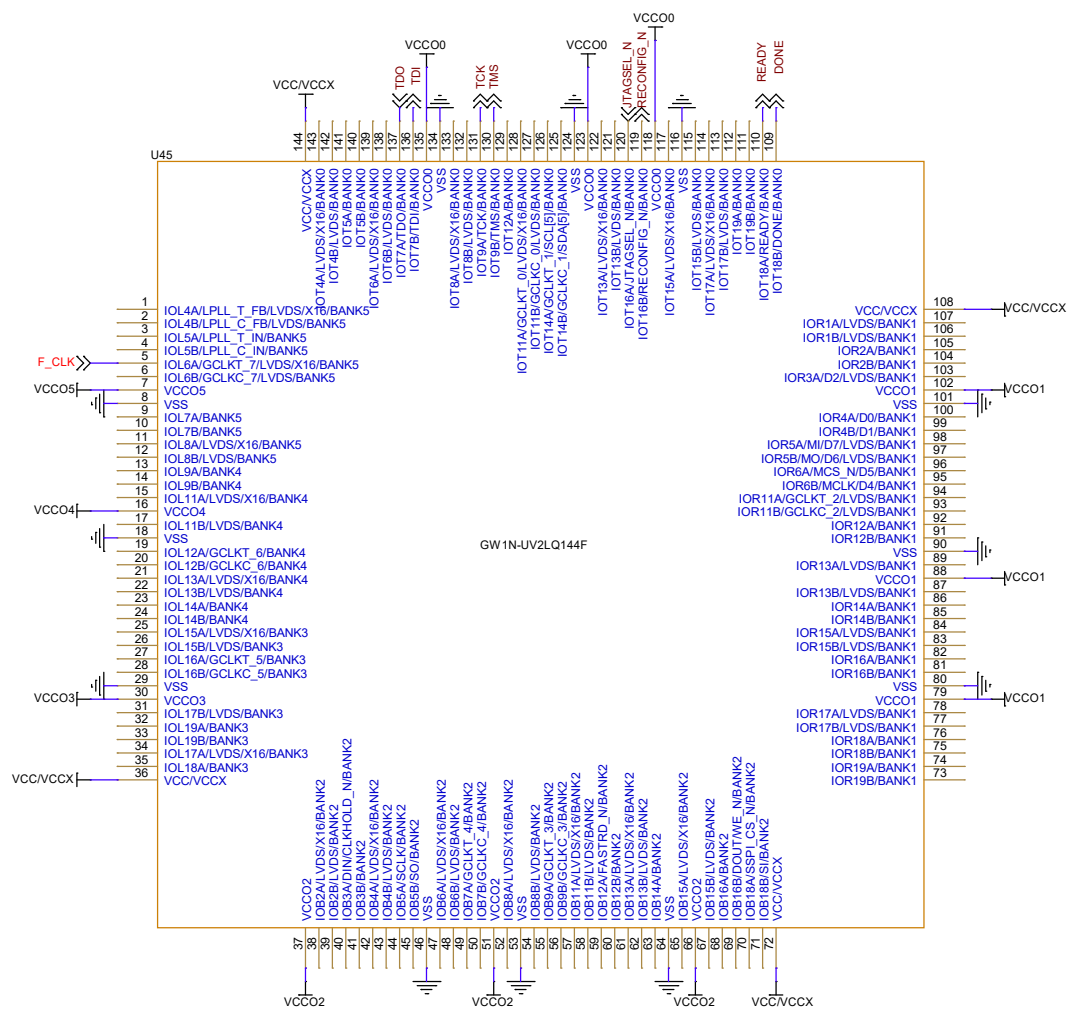
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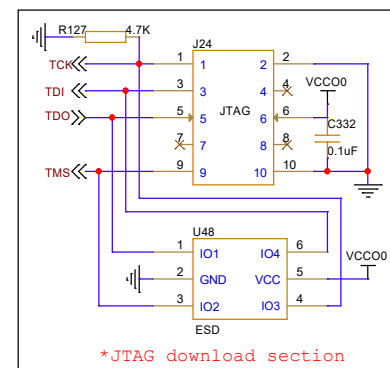
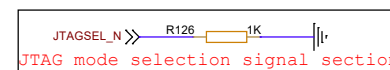
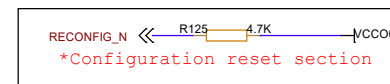
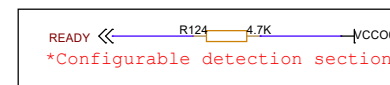
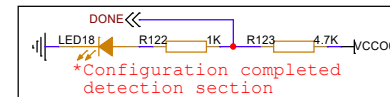
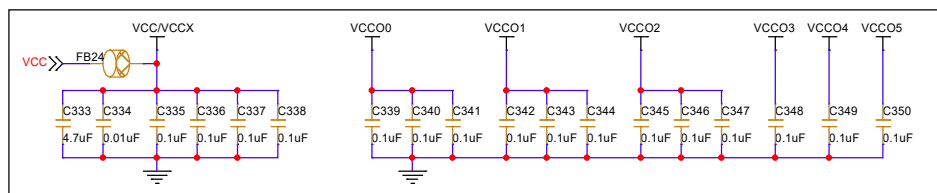
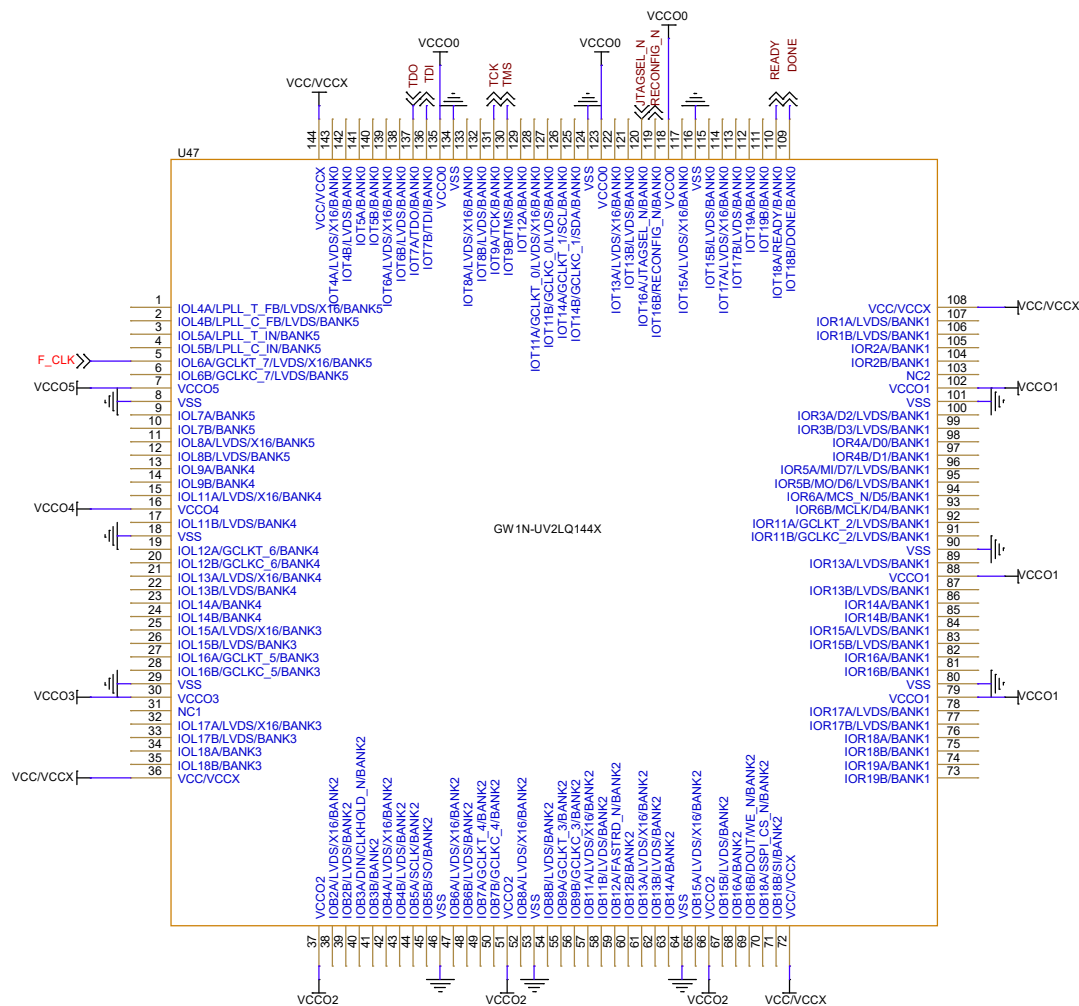
Notes:  
1.F CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.  
2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
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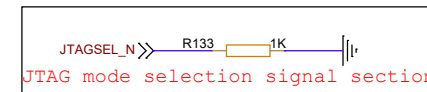
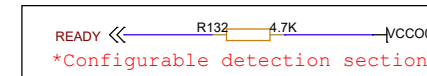
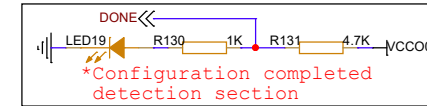
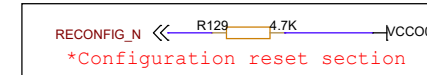
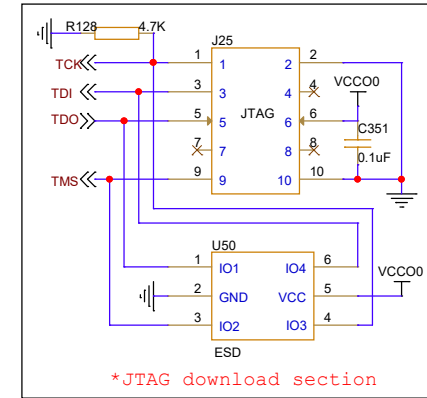
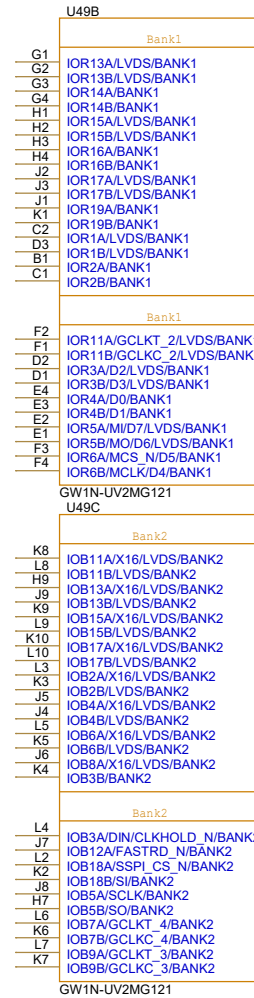
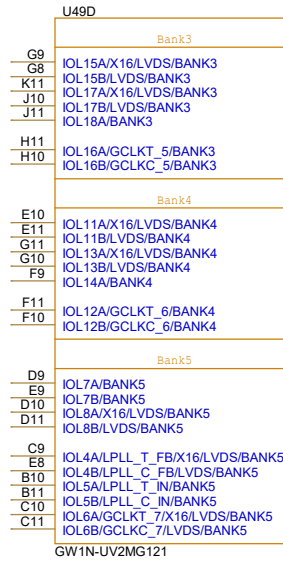
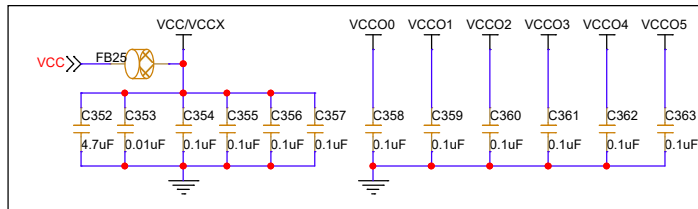
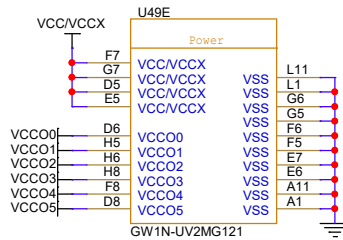
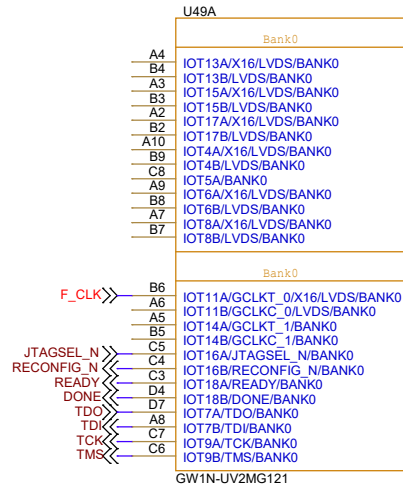


Notes:  
 1.F CLK signal is an external input clock signal.  
 It is recommended that F CLK signal be provided through an active oscillator crystal.  
 2.It is recommended that add an ESD protection chip to the JTAG download circuit.



- Notes:
- 1.F CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.
  - 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

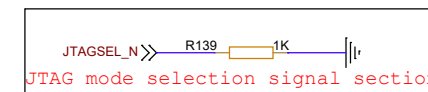
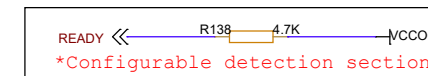
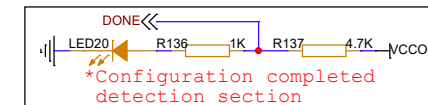
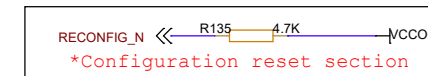
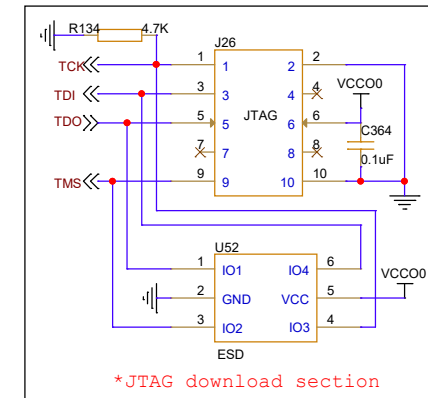
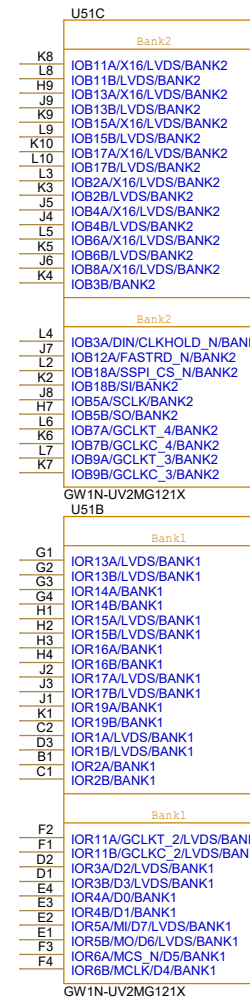
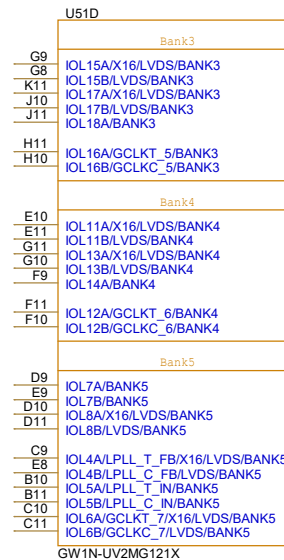
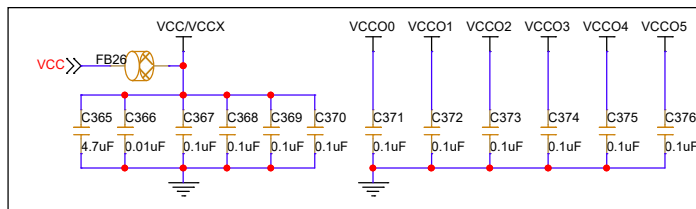
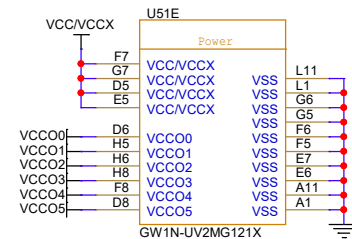
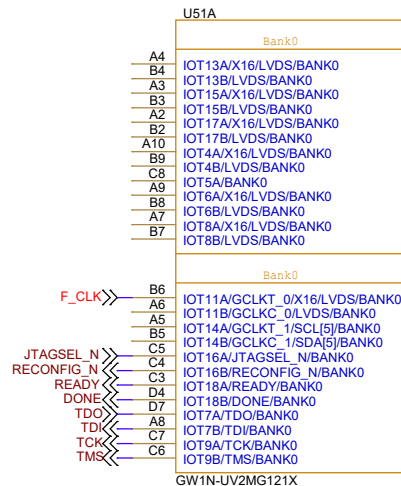




## Notes:

- 1.F\_CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
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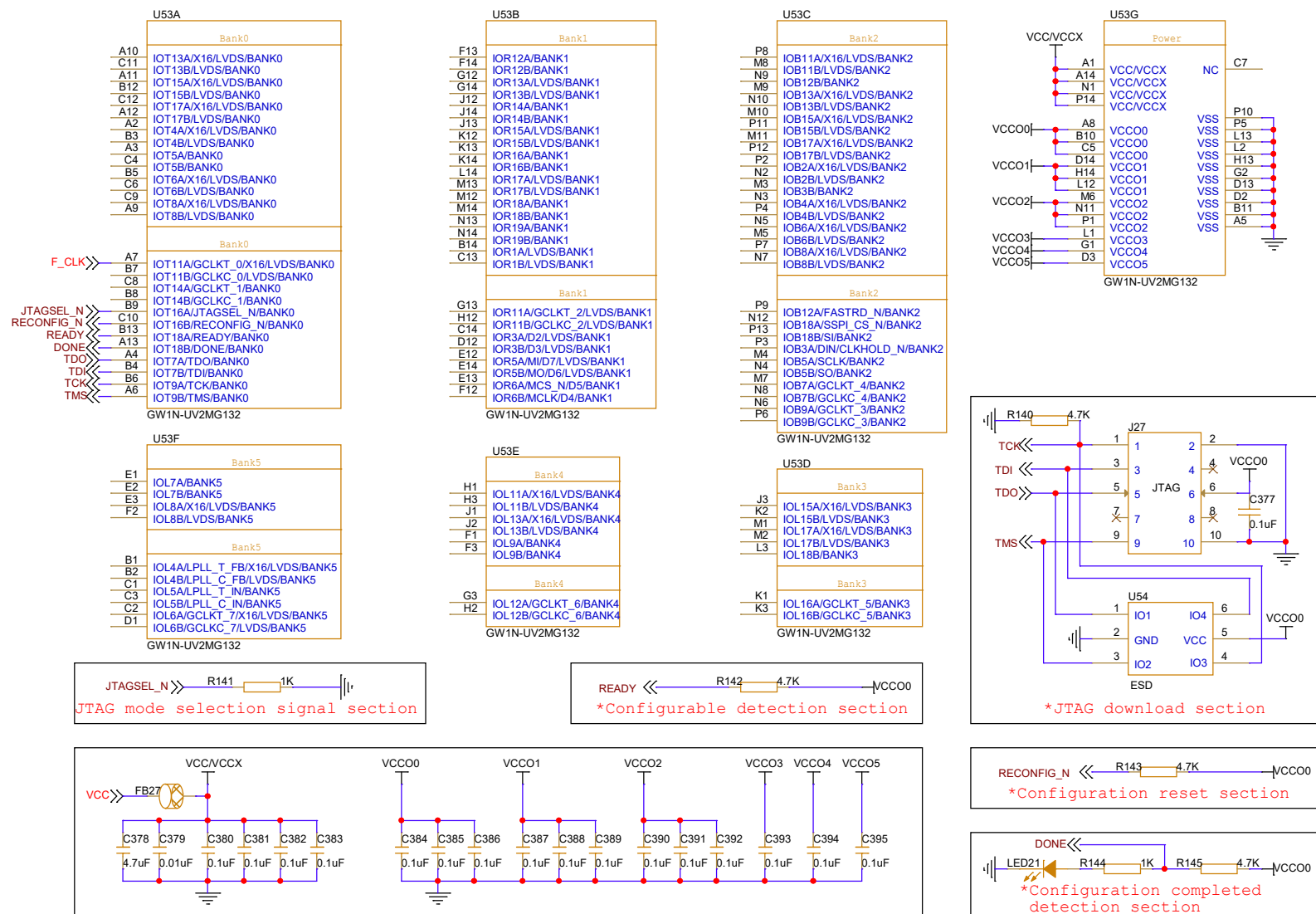
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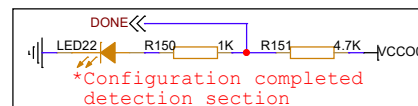
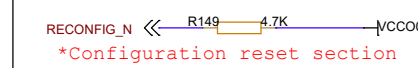
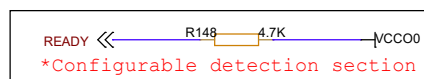
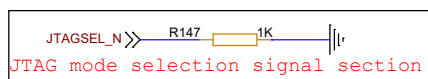
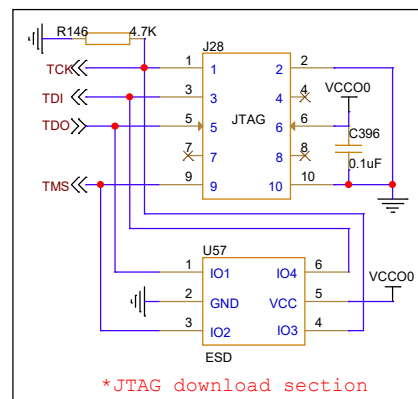
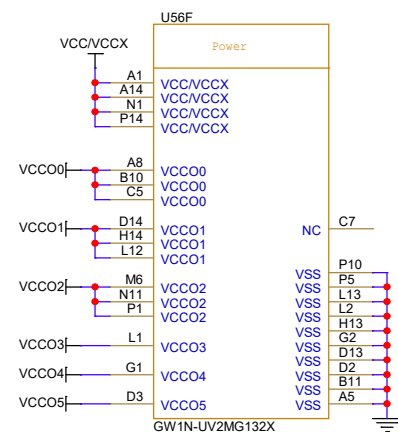
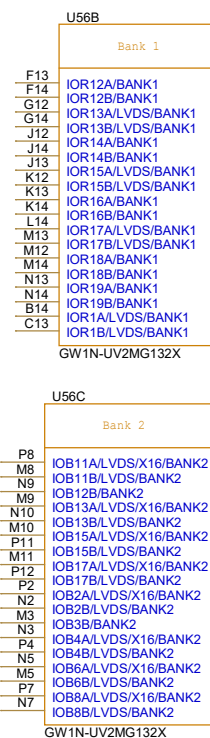
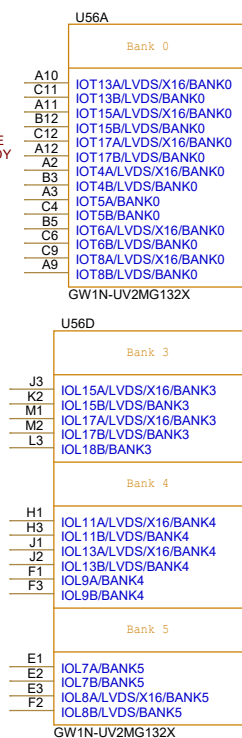
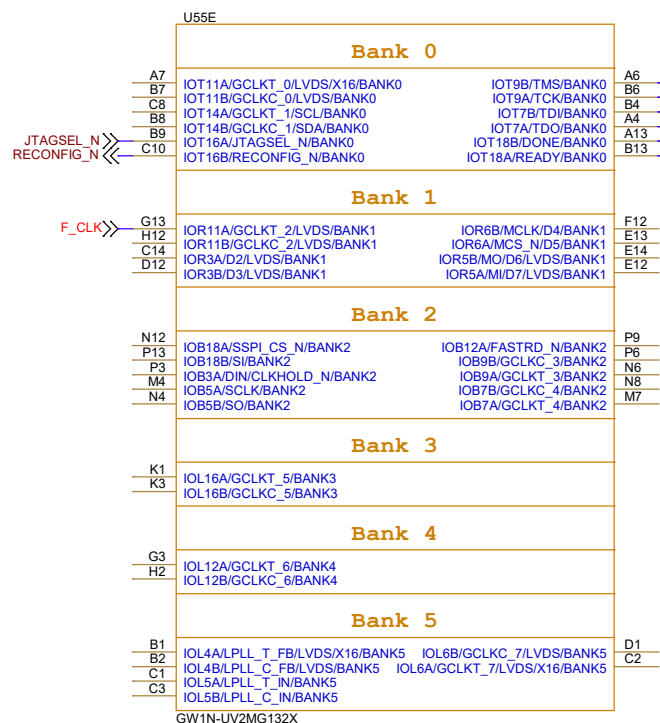
1.F\_CLK signal is an external input clock signal.

It is recommended that F\_CLK signal be provided through an active oscillator crystal.

2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
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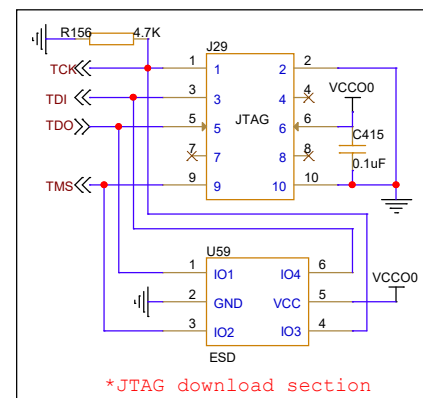
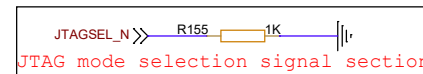
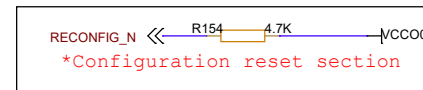
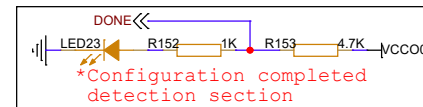
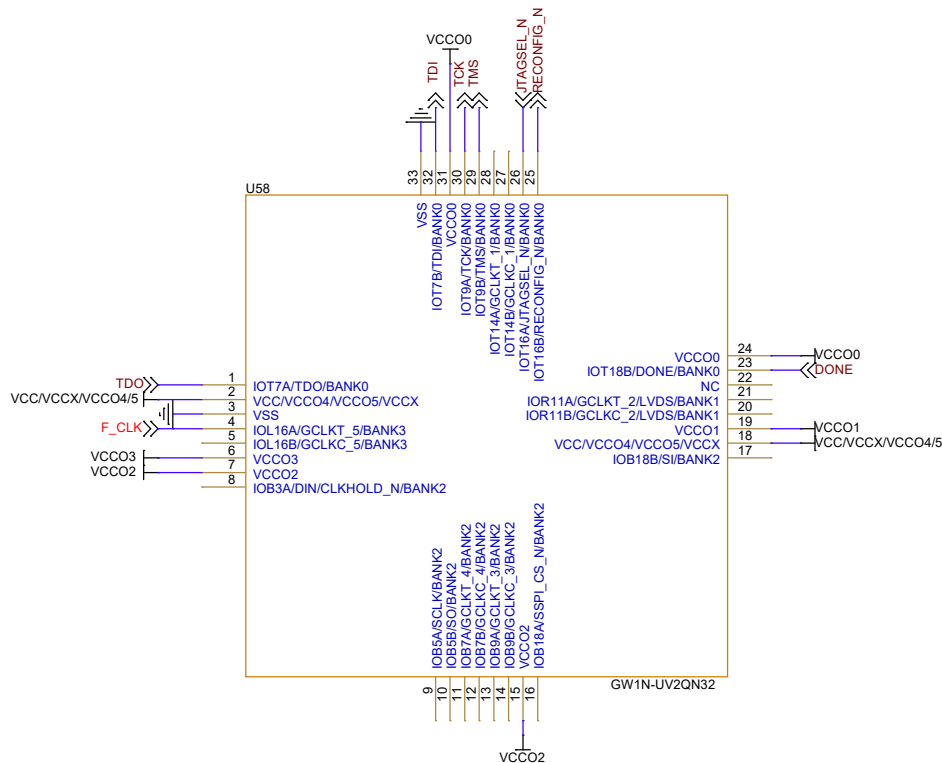




Notes:

- 1.F CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title				
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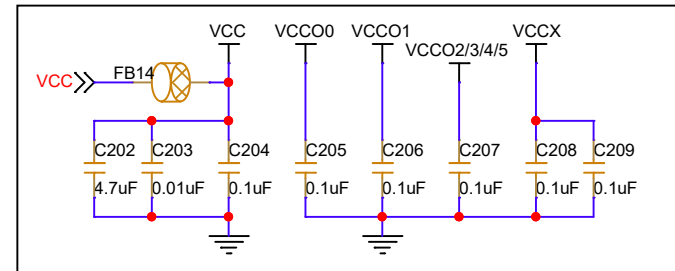
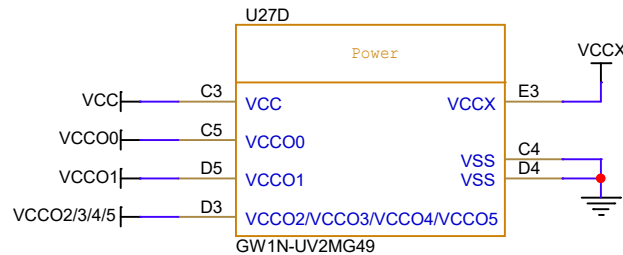
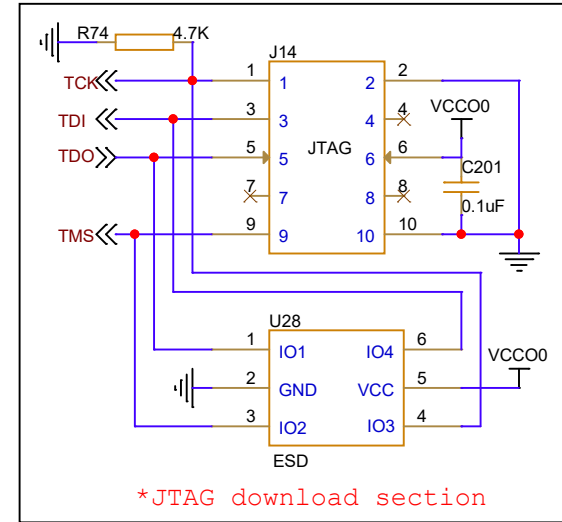
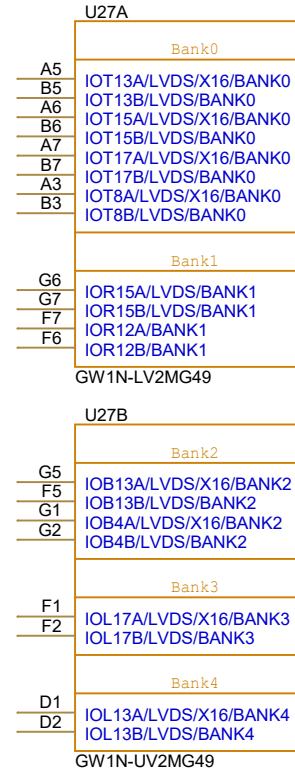
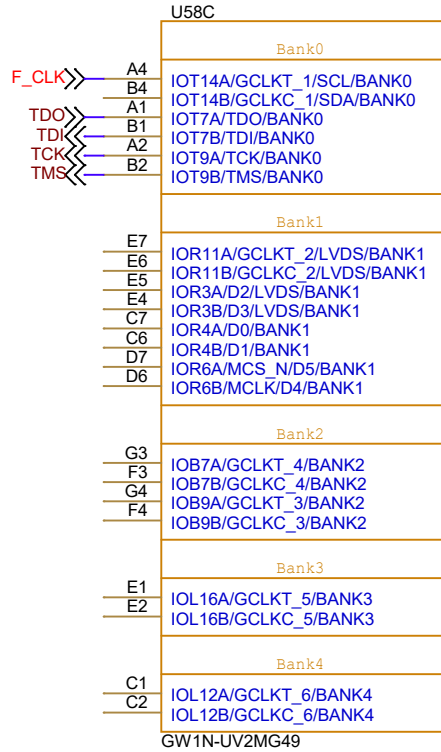


Notes:

- 1.F CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

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GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-UV2QN32	2.0
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# GW1N-UV2MG49



## Notes:

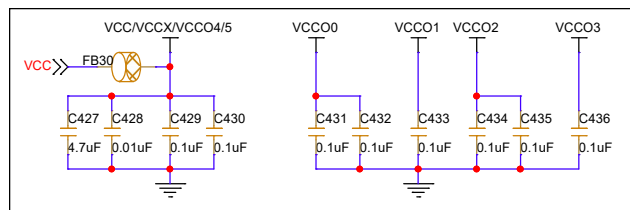
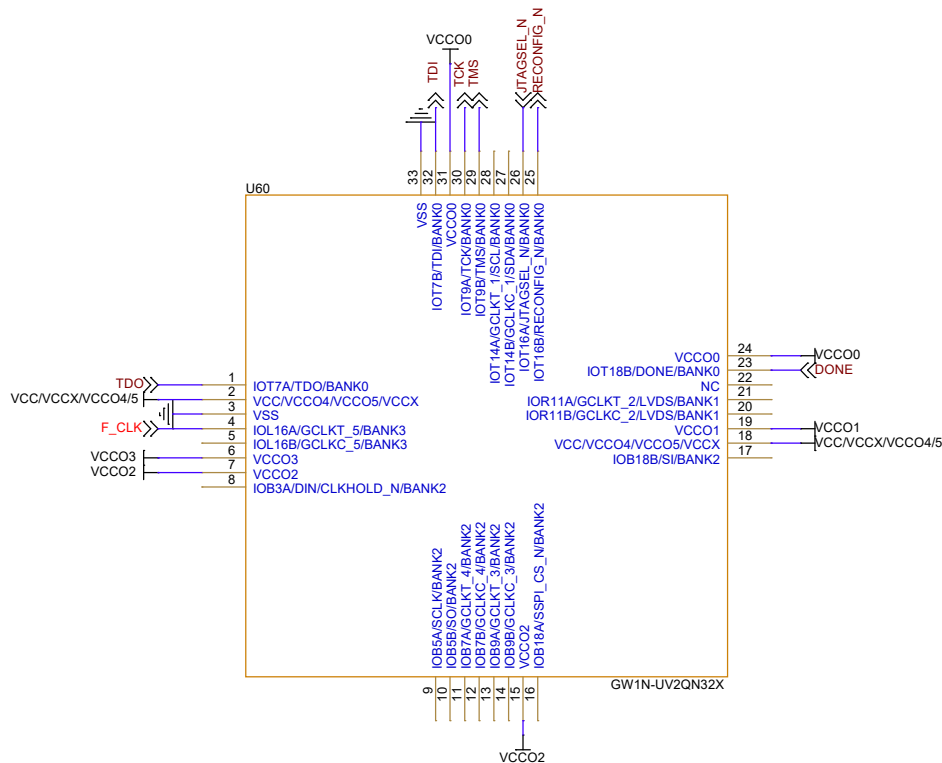
1.F\_CLK signal is an external input clock signal.

It is recommended that F\_CLK signal be provided through an active oscillator crystal.

2.It is recommended that add an ESD protection chip to the JTAG download circuit.

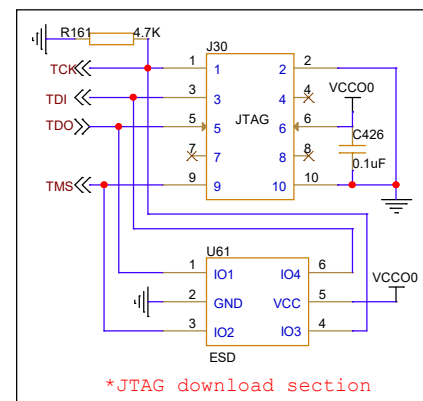
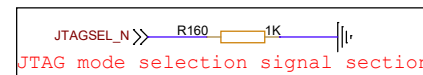
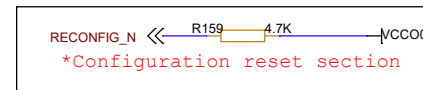
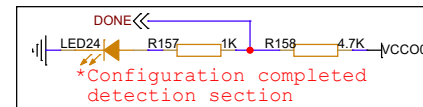
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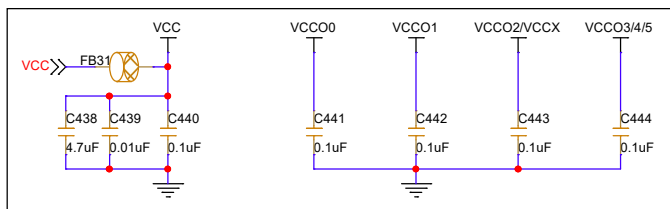
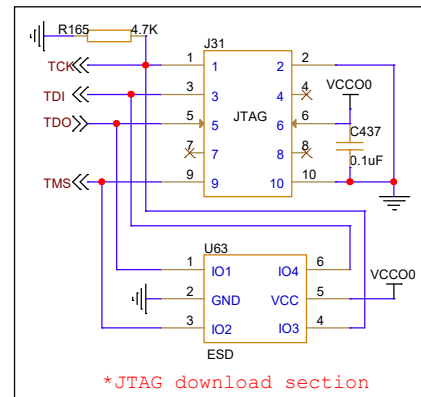
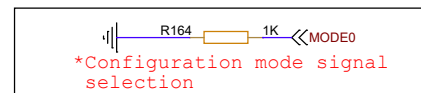
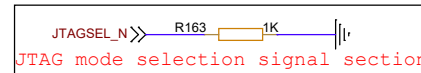
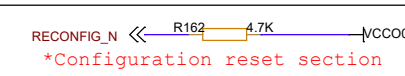
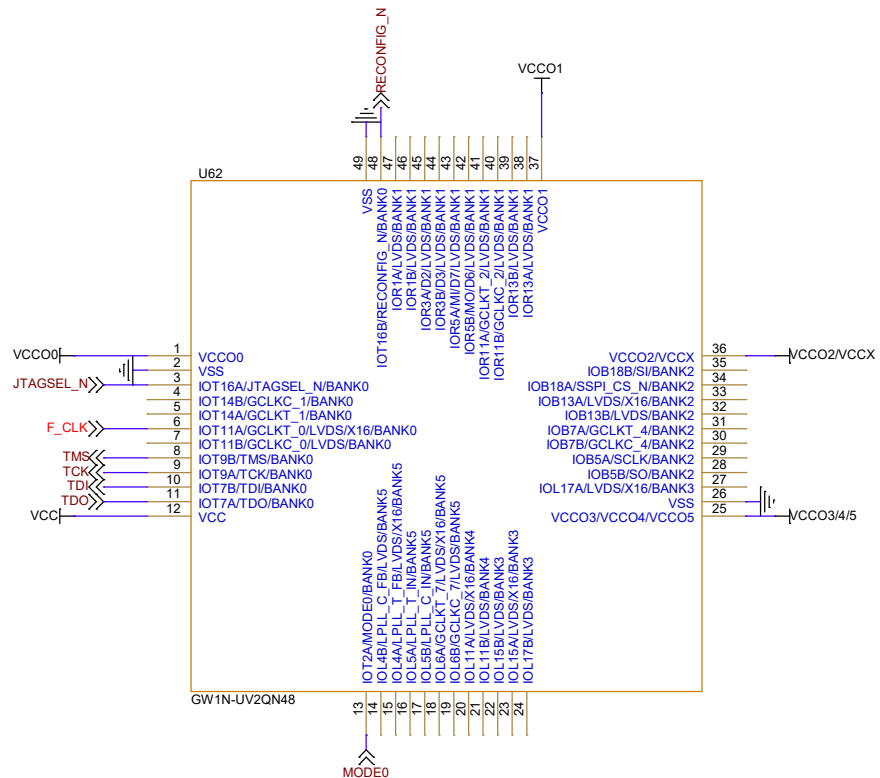


## Notes:

- 1.F CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.



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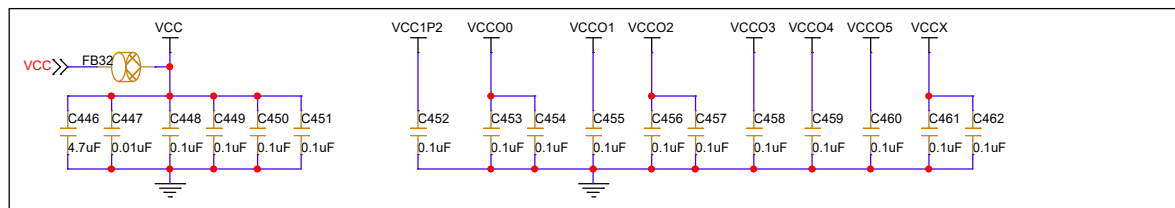
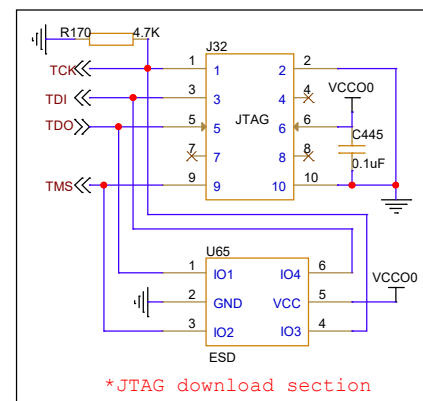
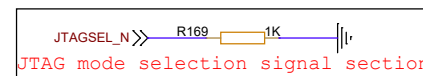
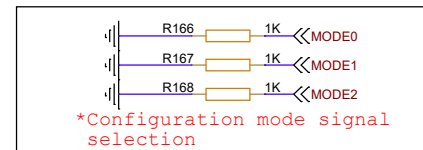
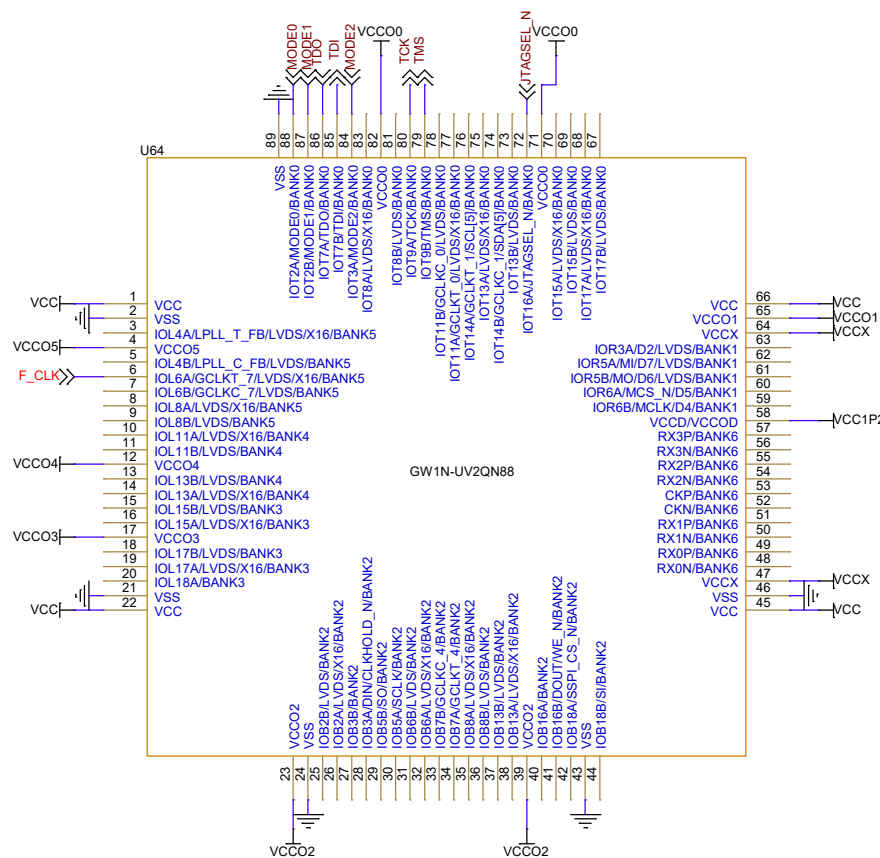


#### Notes:

- 1.F CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

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Notes:  
 1.F CLK signal is an external input clock signal.  
 It is recommended that F\_CLK signal be provided through an active oscillator crystal.  
 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

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GOWIN Minimum System Diagram		
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