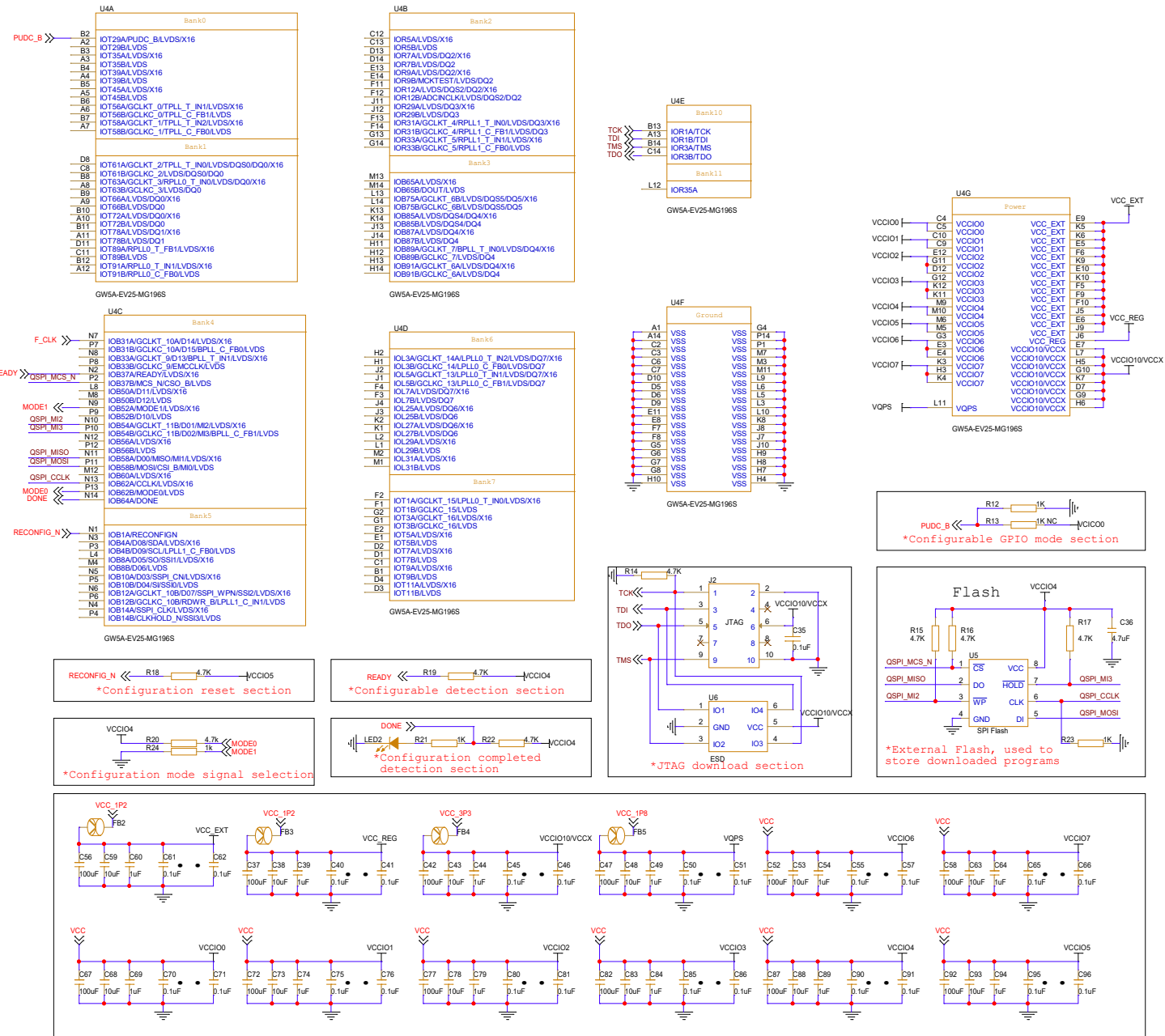


Notes:

- NOTES:
- 1.F CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal.
 - 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
 - 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
 - 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
 - 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG704, Arora V
FPGA Product Programming and Configuration Guide.

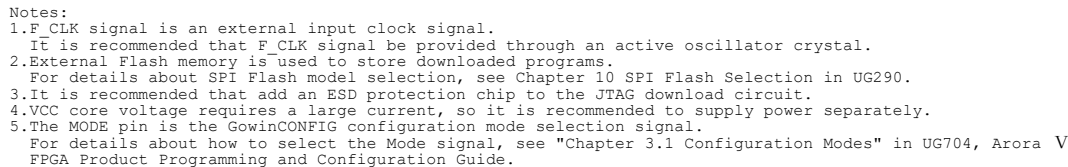
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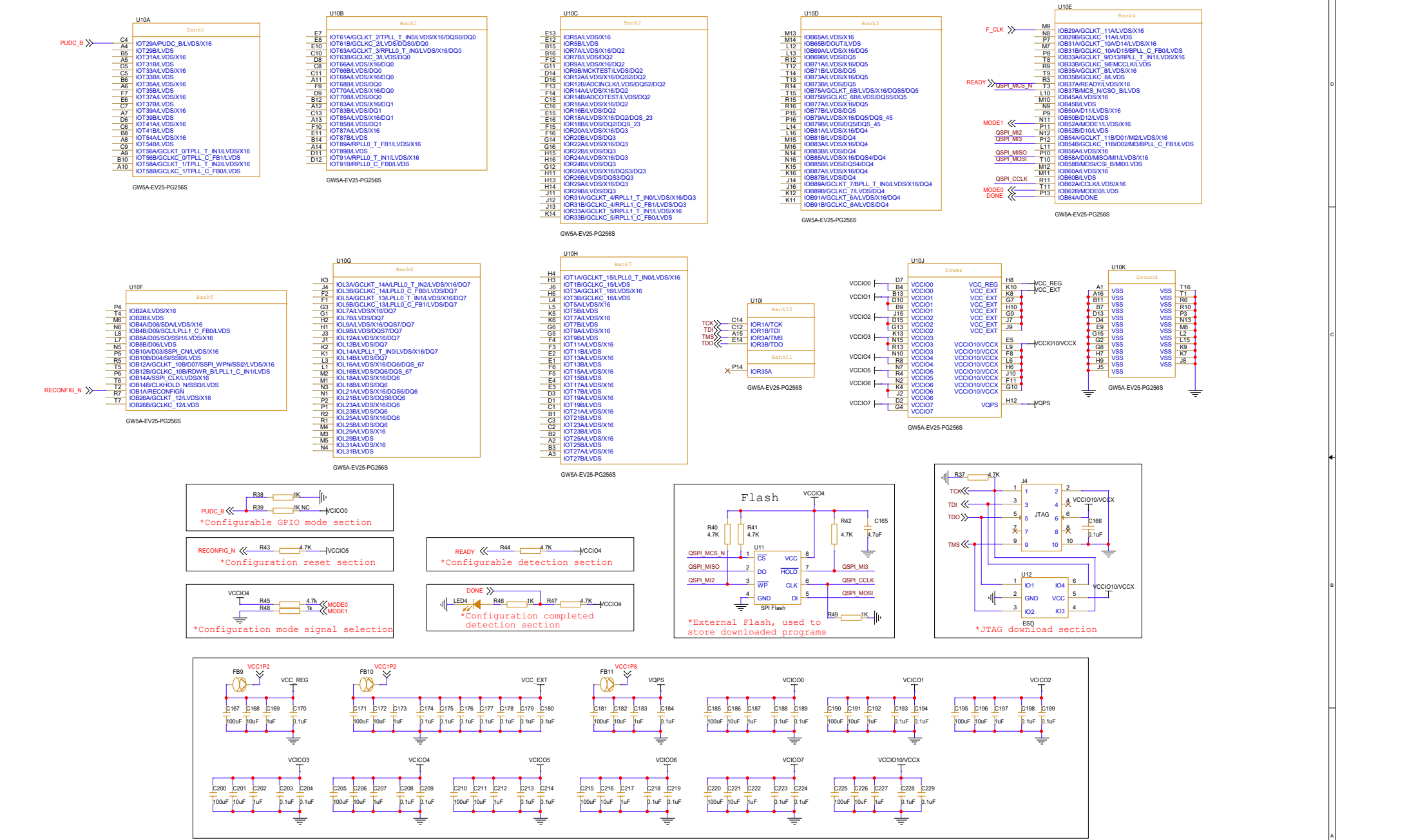
Notes:

- 1.F CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG704, Arora V
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File	<Title>		
Size	Document Number	Rev	
C	GW5A-EV25MG196S	2.1.1	
Date	Wednesday, October 11, 2023	Sheet	2 of 13



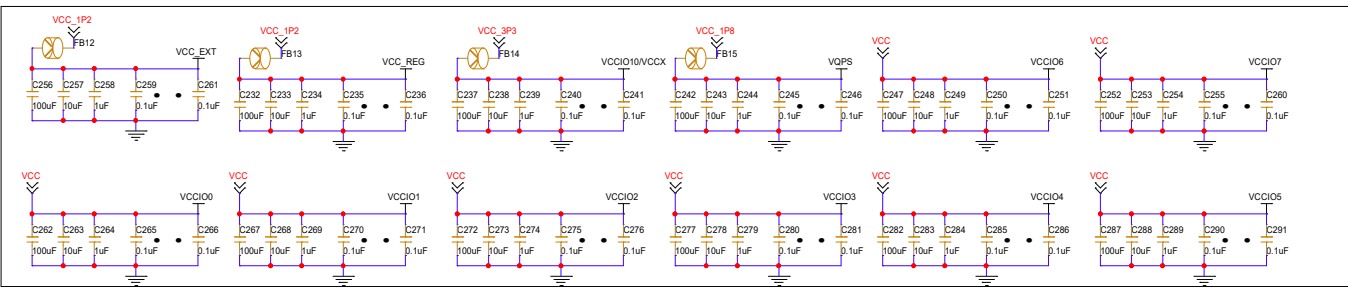
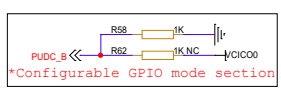
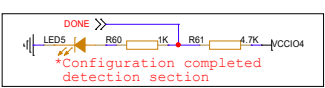
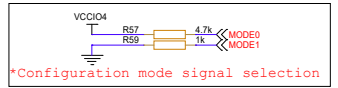
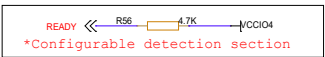
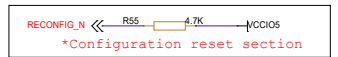
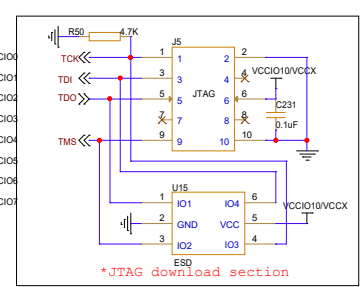
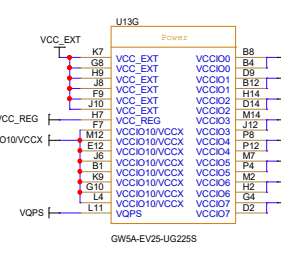
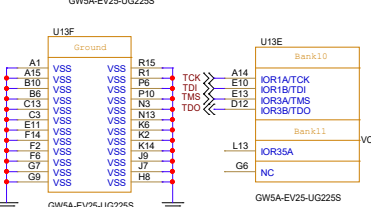
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Notes:

- 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG704, Arora V
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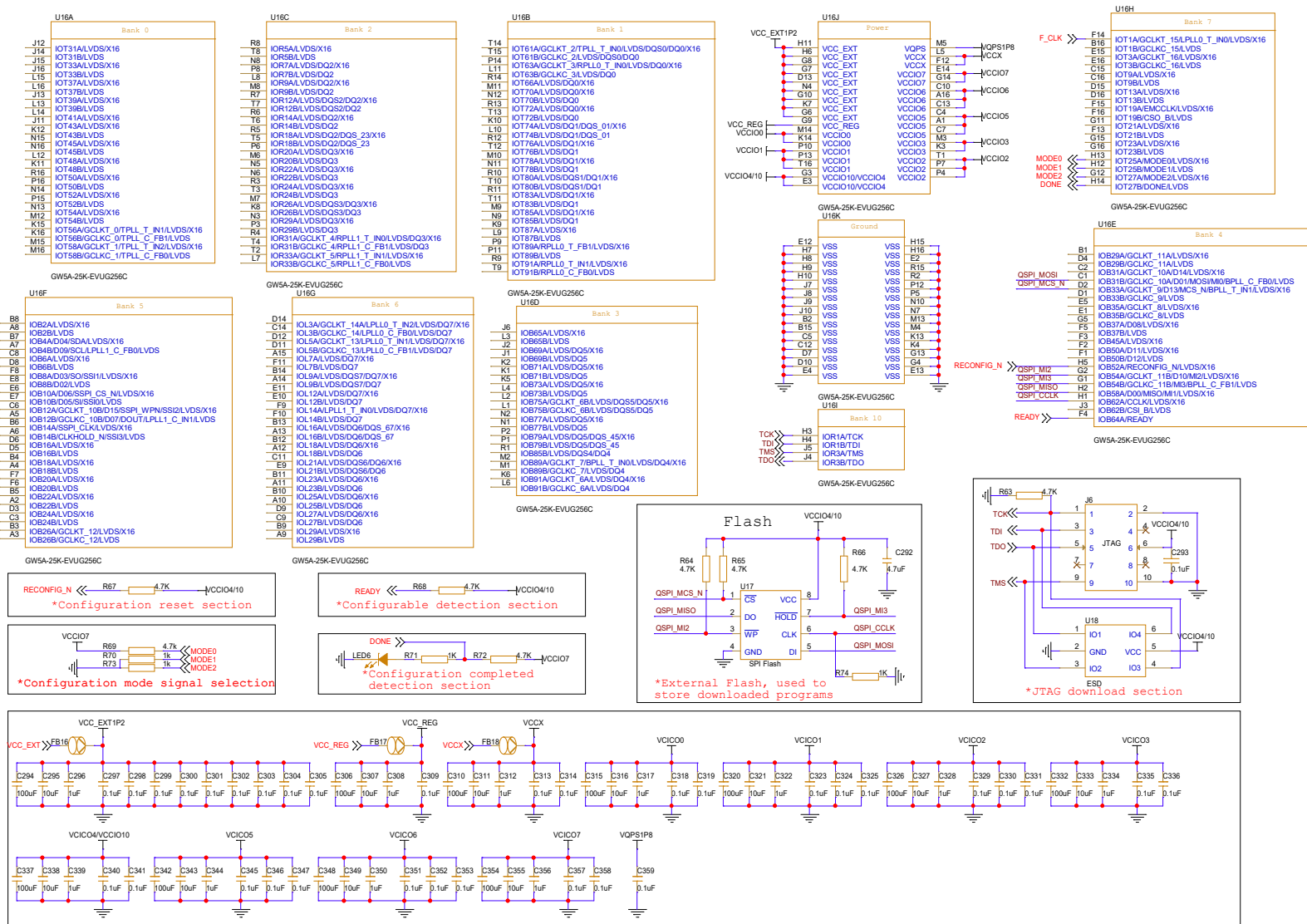
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Size	Document Number	Rev
	GW5A-EV25PG256S	
Date	Wednesday, October 11, 2023	Sheet 4 of 13



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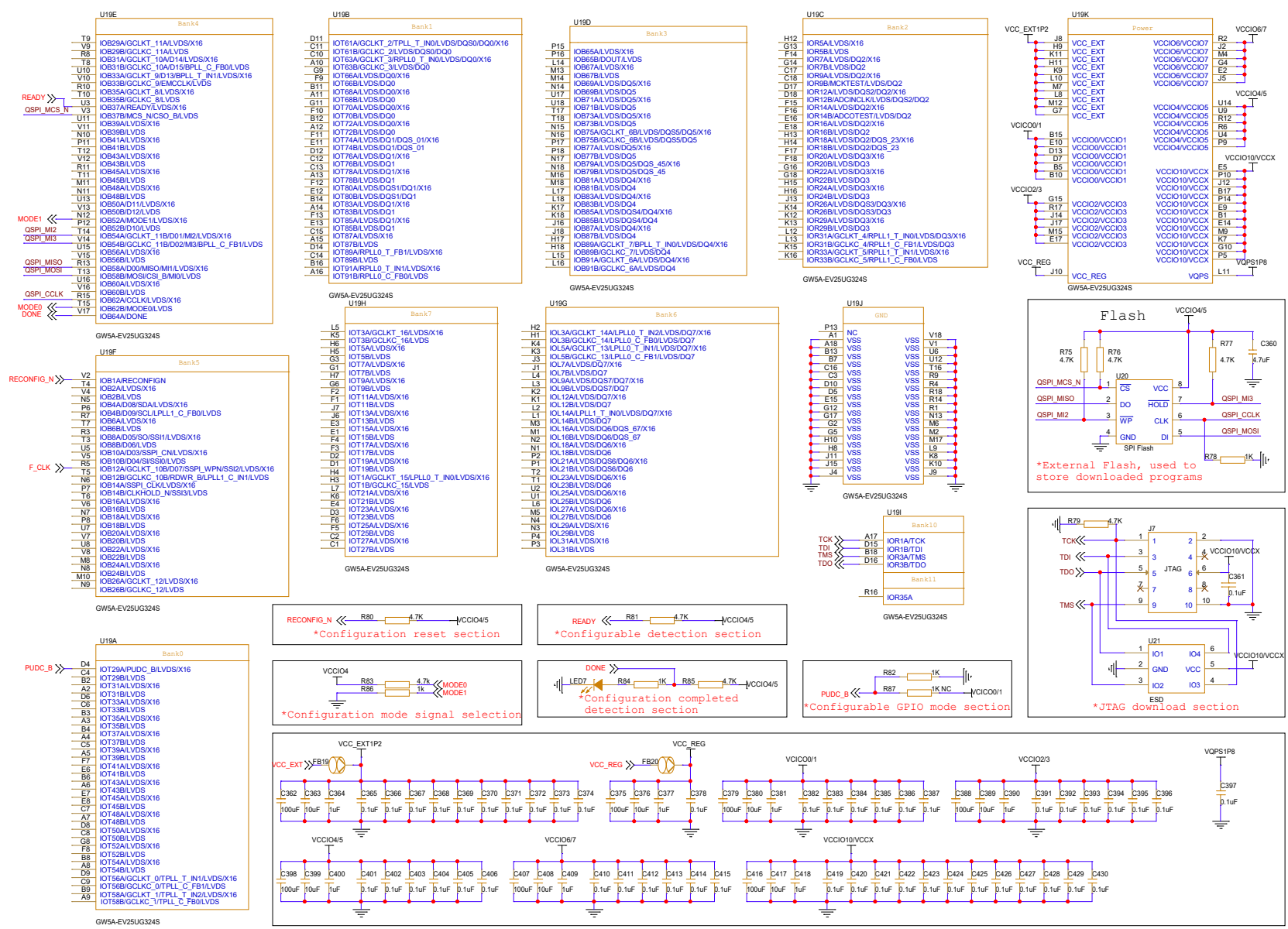
- 1.F CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG704, Arora V FPGA Product Programming and Configuration Guide.

GW5A-EV25UG256C



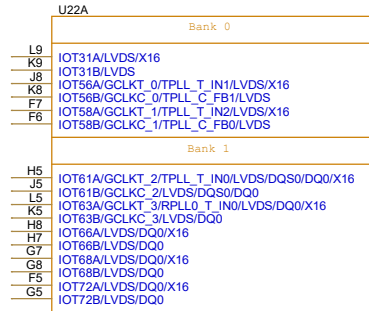
Notes:

- 1.F CLK signal is an external input clock signal.
- 2.It is recommended that F.CLK signal be provided through an active oscillator crystal.
- 3.External Flash memory is used to store downloaded programs.
- 4.For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
- 5.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 6.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 7.The MODE pin is the GowinCONFIG configuration mode selection signal.
- 8.For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG704, Arora V FPGA Product Programming and Configuration Guide.

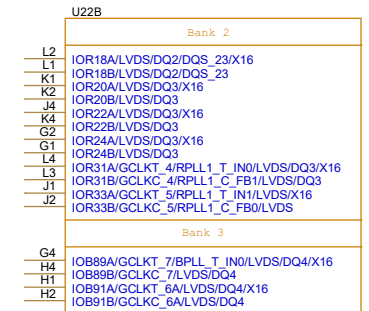


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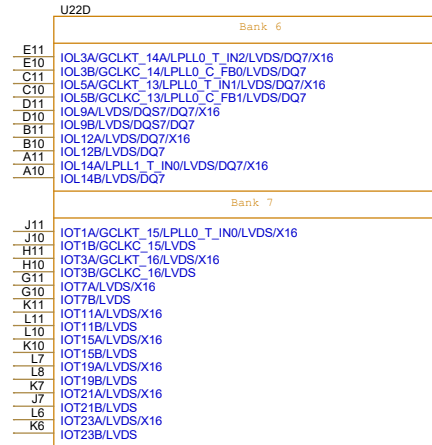
- 1.F CLK signal is an external input clock signal.
It is recommended that F.CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG704, Arora V
FPGA Product Programming and Configuration Guide.



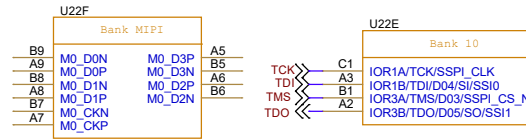
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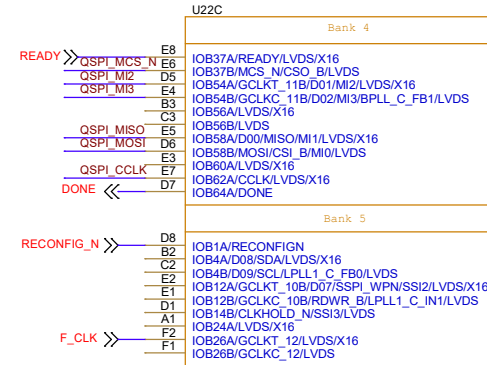
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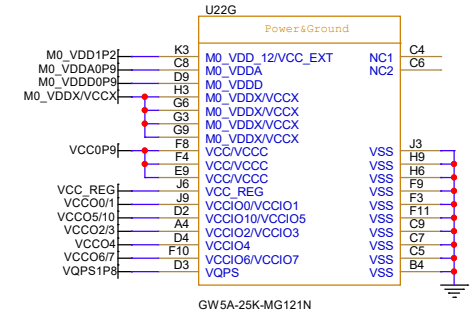
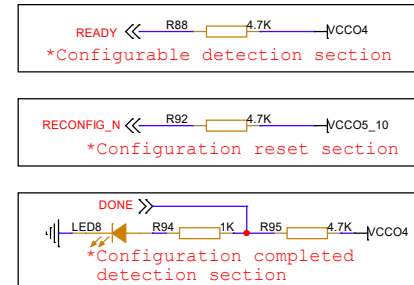
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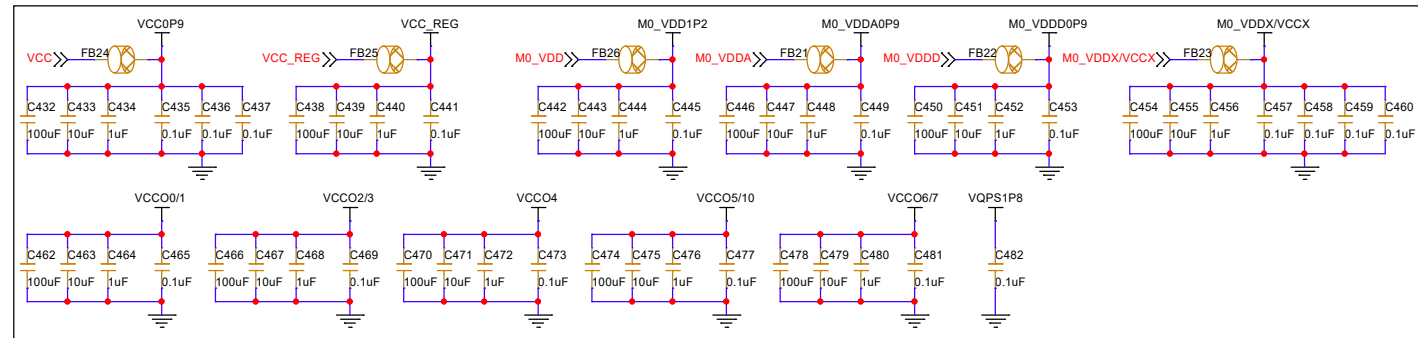
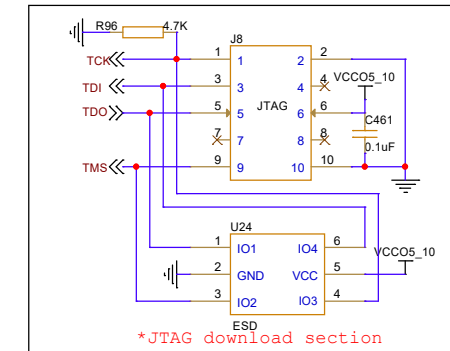
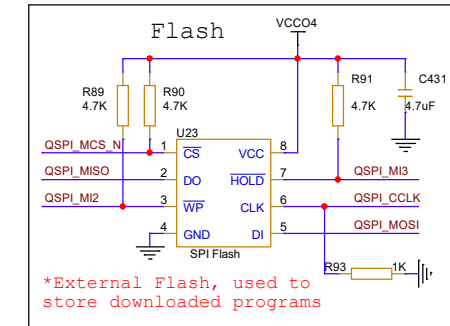
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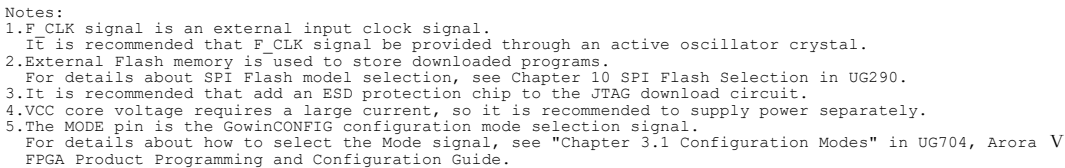


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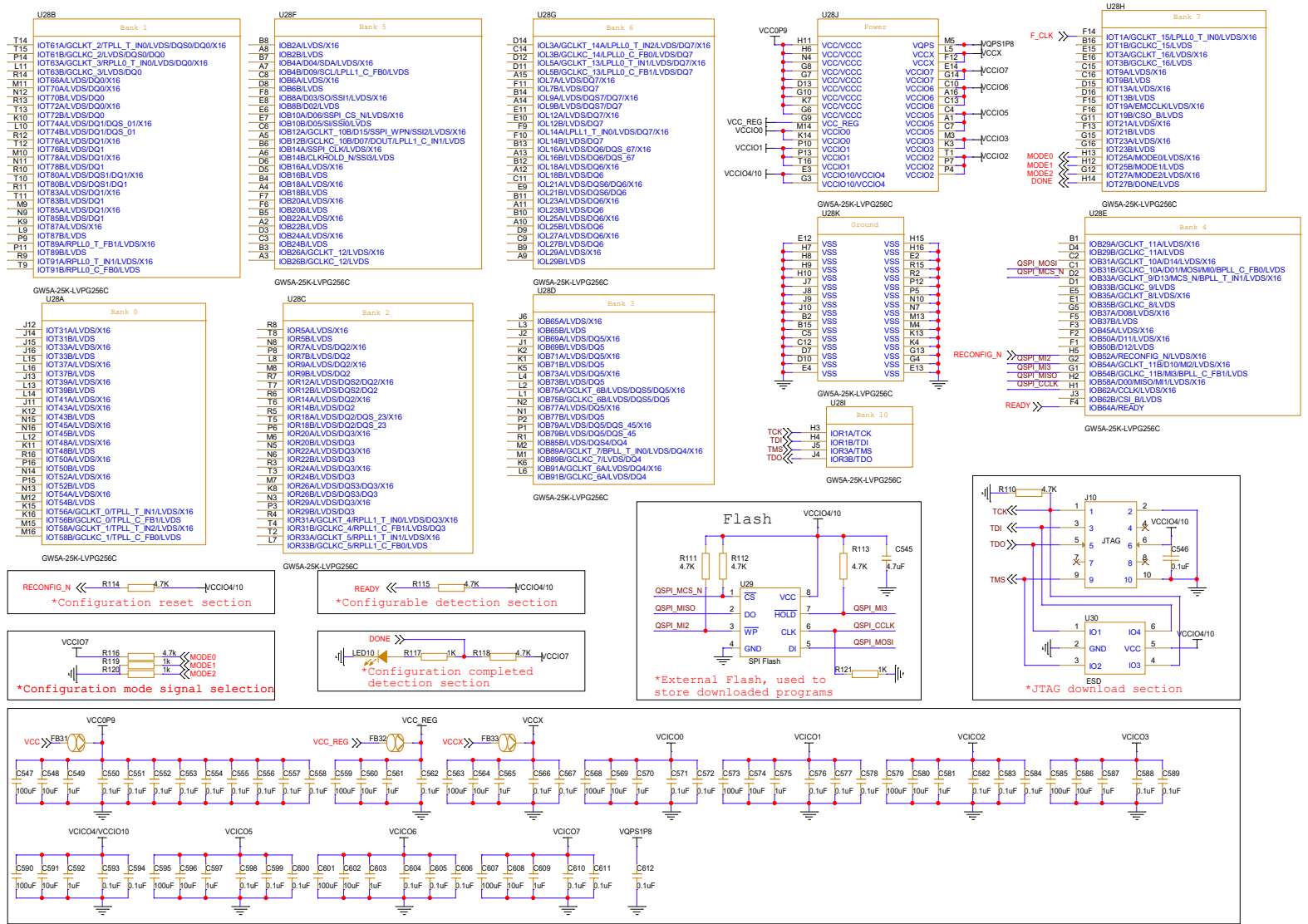


Notes:

- 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG704, Arora V FPGA Product Programming and Configuration Guide.



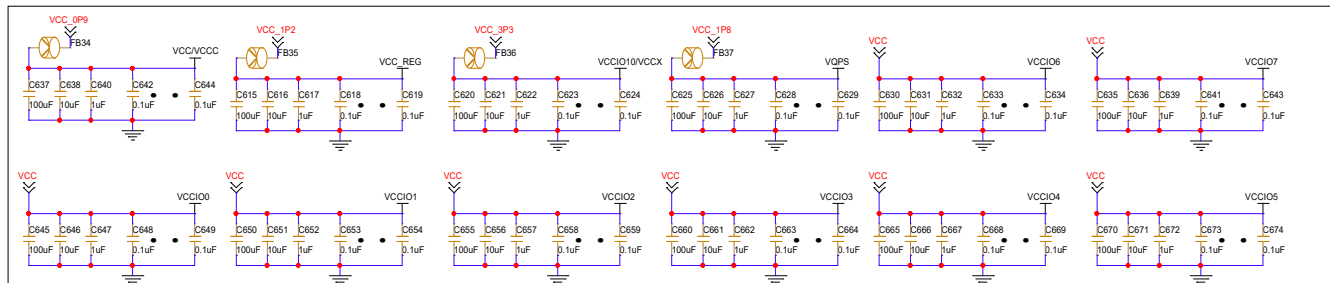
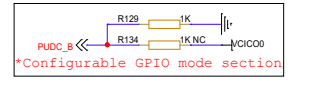
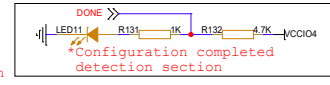
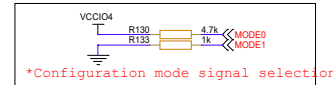
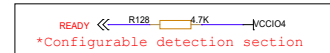
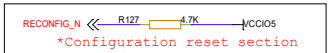
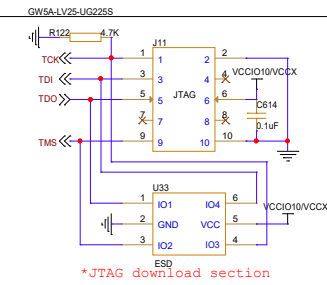
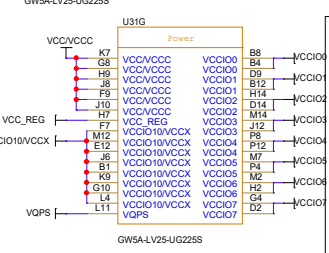
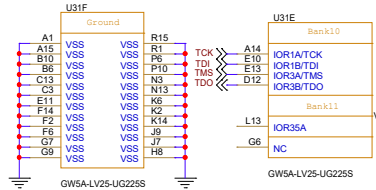
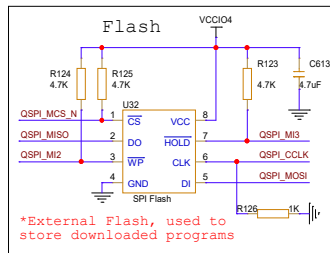
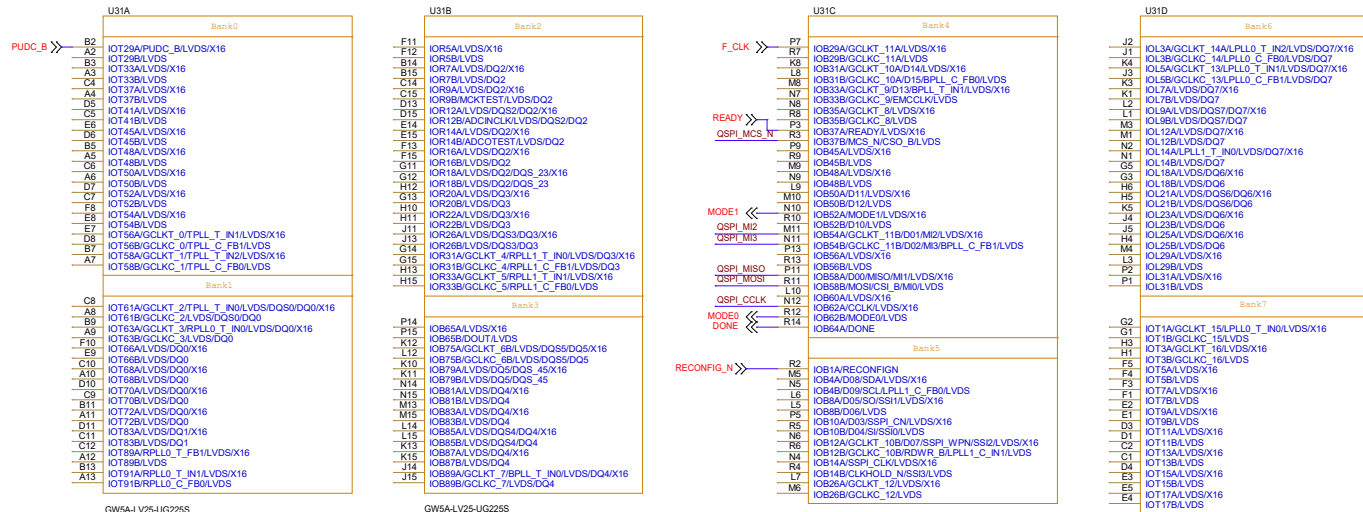
GW5A-LV25PG256C



Notes:

- 1.F CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG704, Arora V
FPGA Product Programming and Configuration Guide.

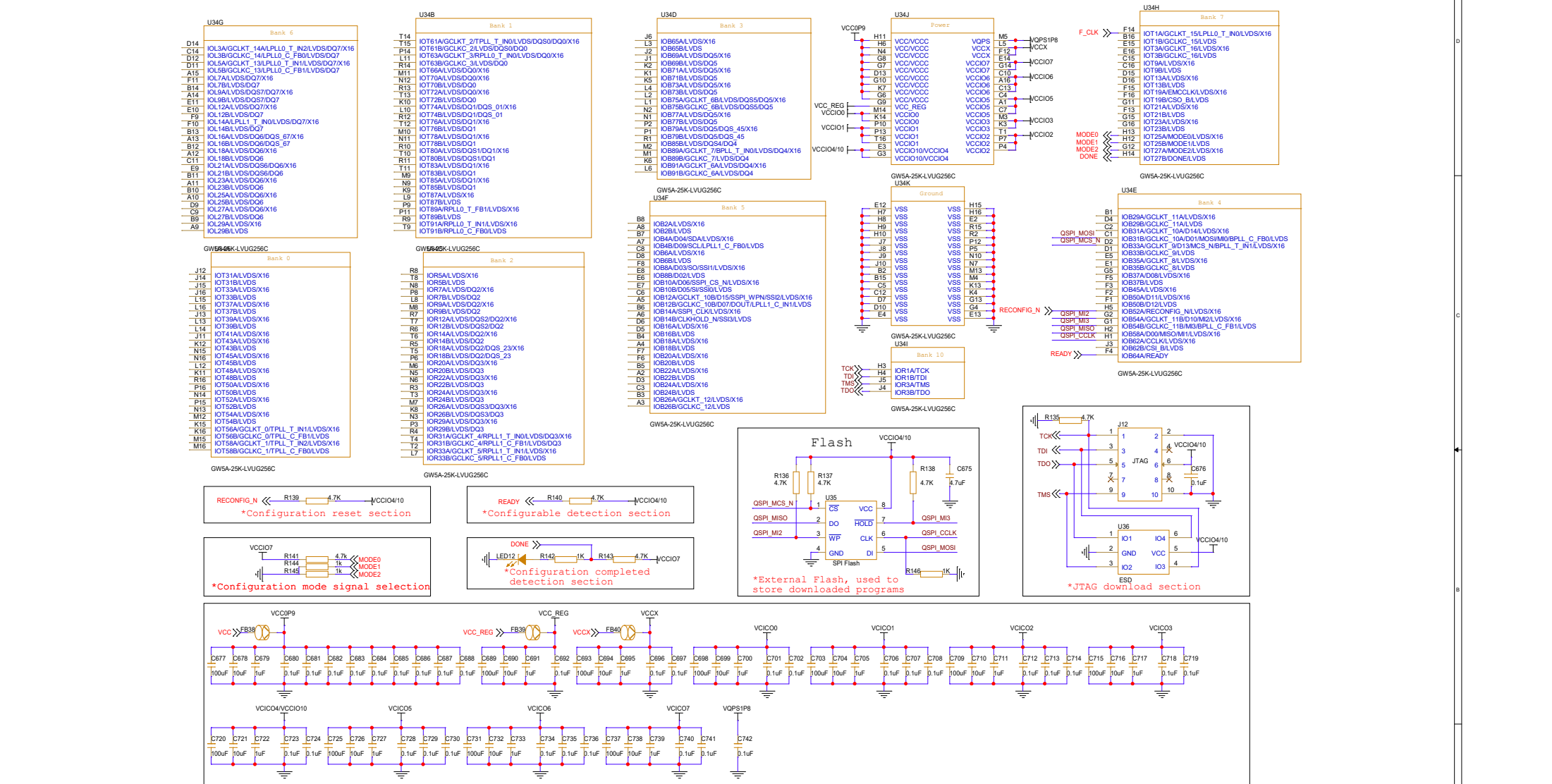
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Size	Document Number	Rev	
	GW5A-LV25PG256C	2.1.1	
Date	Wednesday, October 11, 2023	Sheet	10 of 13



- Notes:**
- 1.F_CLK signal is an external input clock signal.
 - 2.It is recommended that F_CLK signal be provided through an active oscillator crystal.
 - 3.External Flash memory is used to store downloaded programs.
 - 4.For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
 - 5.It is recommended that add an ESD protection chip to the JTAG download circuit.
 - 6.VCC core voltage requires a large current, so it is recommended to supply power separately.
 - 7.The MODE pin is the GowinCONFIG configuration mode selection signal.
 - 8.For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG704, Arora V FPGA Product Programming and Configuration Guide.

File	<Title>		
Size	Document Number		Rev
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Date	Wednesday, October 11, 2023	Sheet	11 of 13

GW5A-LV25UG256C

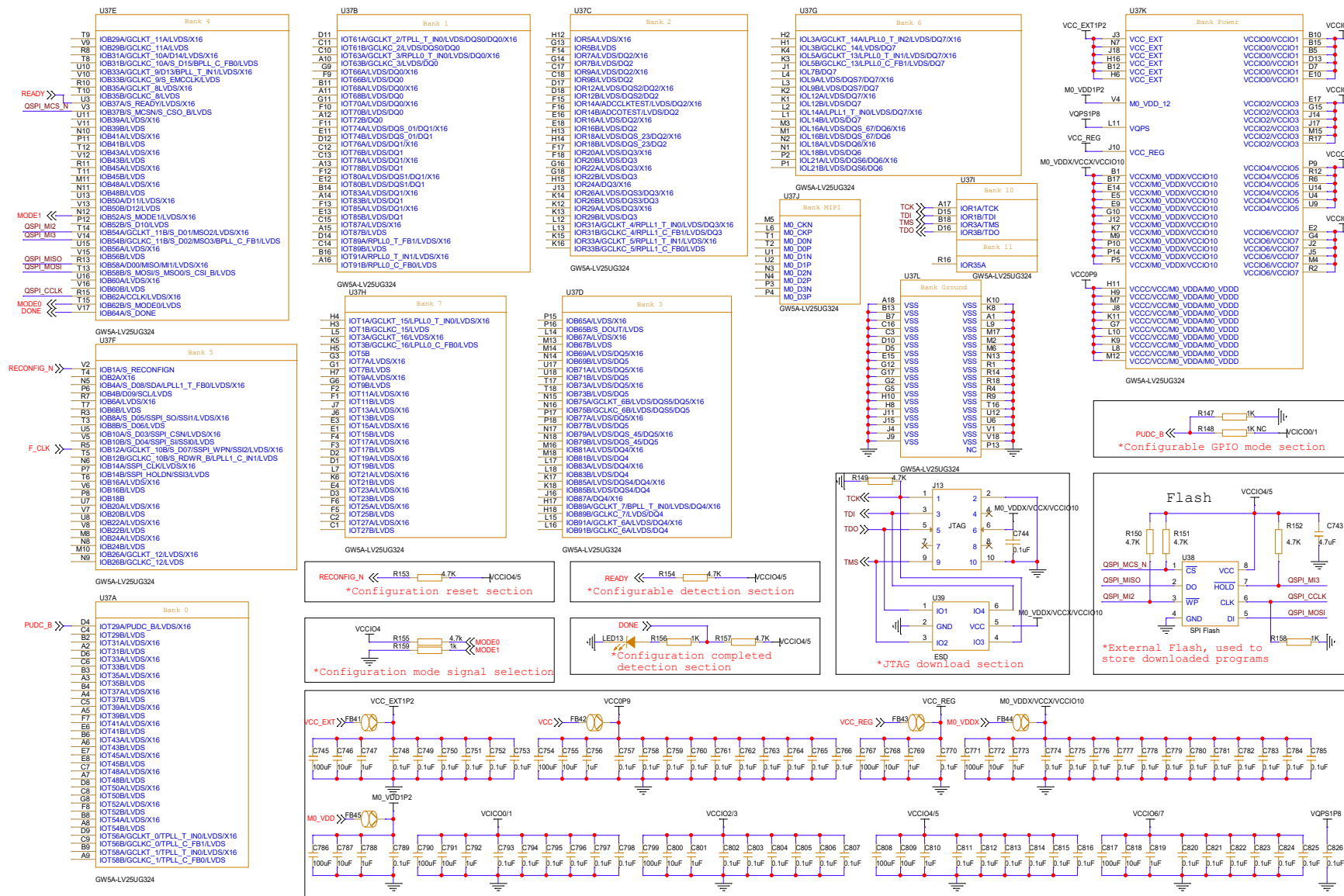


Notes:

- 1.F CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG704, Arora V
FPGA Product Programming and Configuration Guide.

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
C	GW5A-LV25UG256C	2.1.1
Date:	Wednesday, October 11, 2023	Sheet 12 of 13

GW5A-LV25UG324



Notes:

1. F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
3. It is recommended that add an ESD protection chip to the UTAG download circuit.
4. Voltage requirement: The voltage to it is recommended to supply power separately.
5. The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG704, Arora V
FPGA Product Programming and Configuration Guide.

Title				
GOWIN Minimum System Diagram				
Size C	Document Number GW5A-LV25G324			Rev 2.1.1
Date	Wednesday, October 11, 2023	Sheet	14	of 14