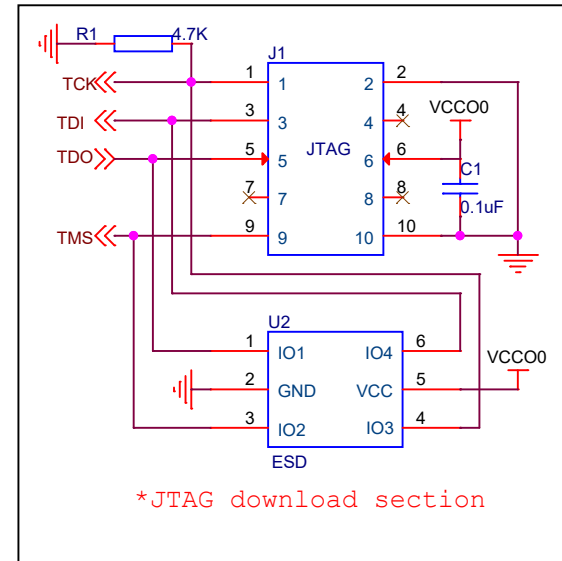
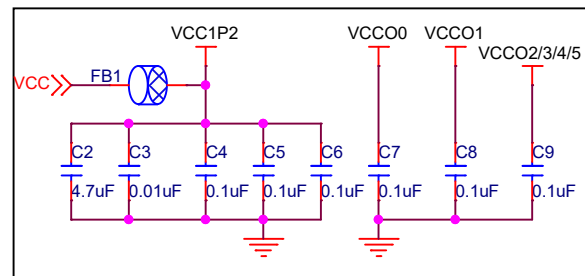
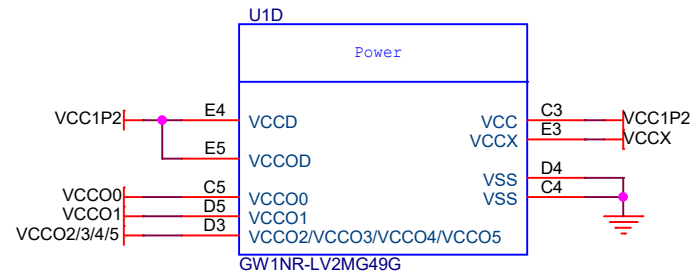
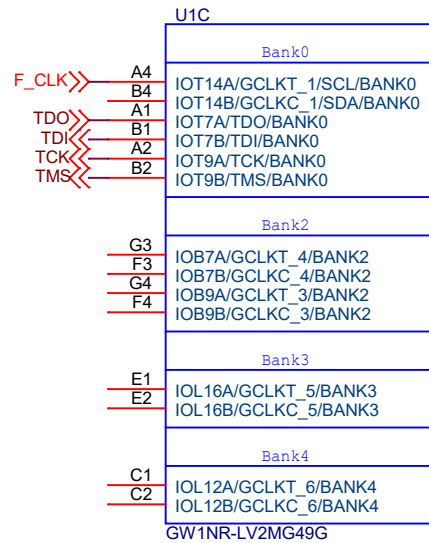
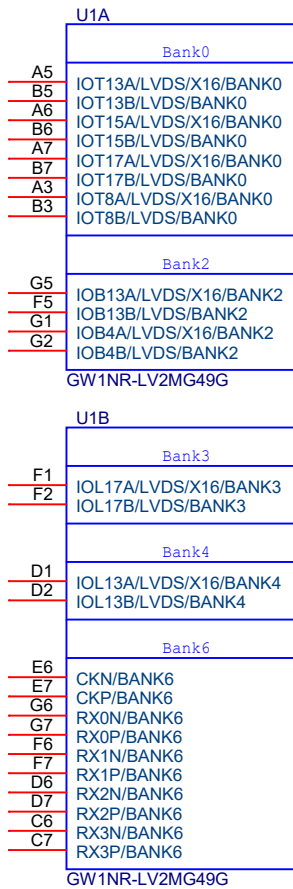


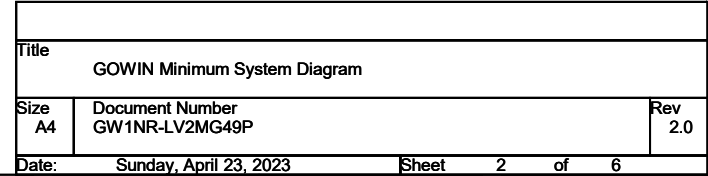
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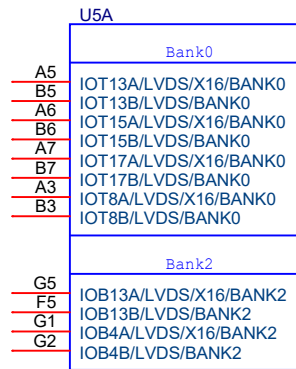
Notes:

- 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

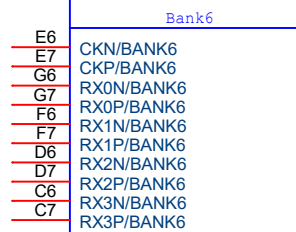
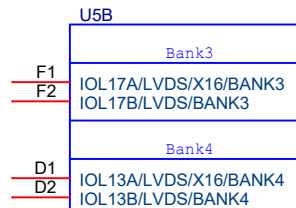
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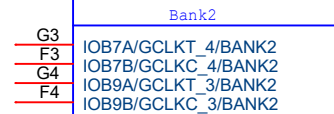
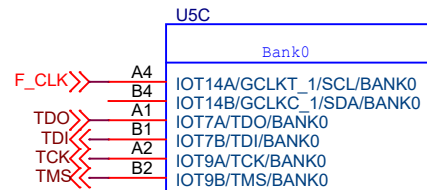
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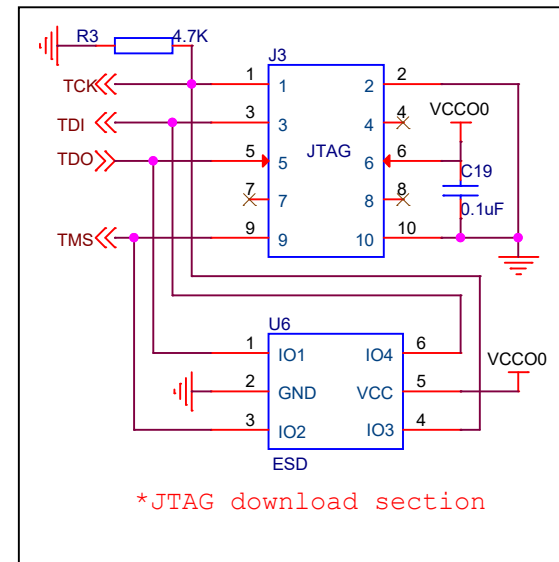
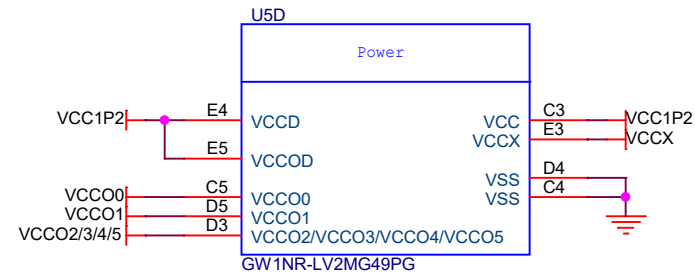
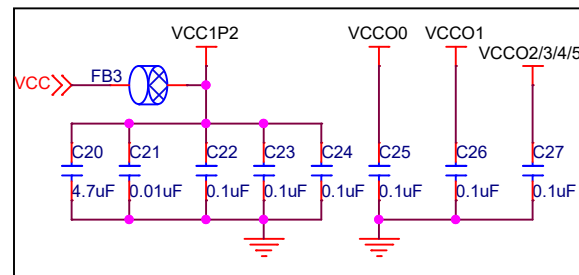
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GW1NR-LV2MG49PG



GW1NR-LV2MG49PG



Notes:

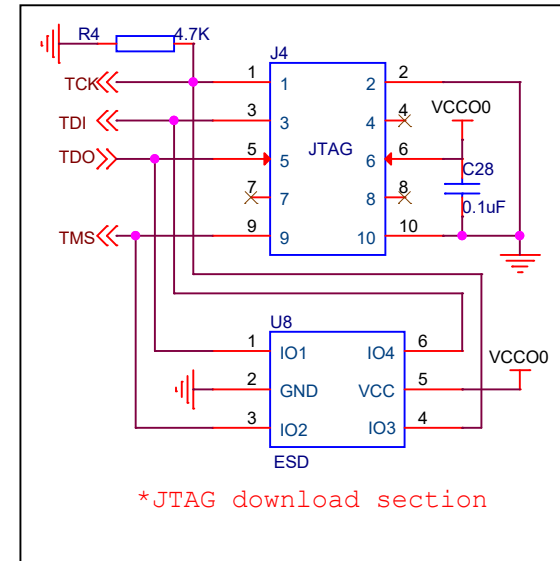
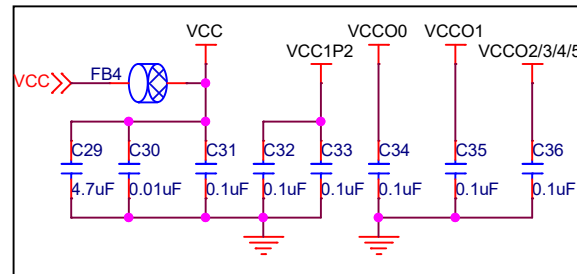
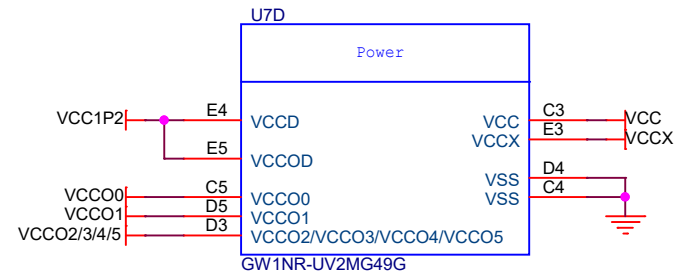
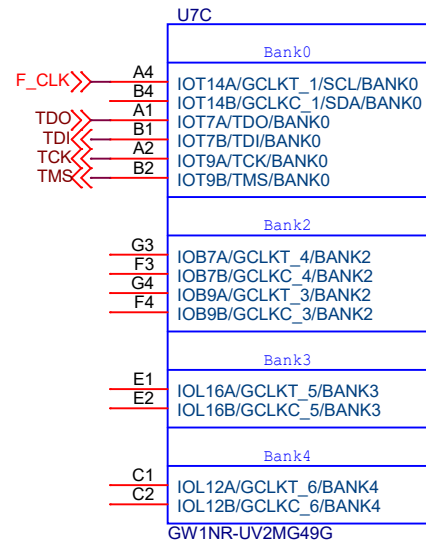
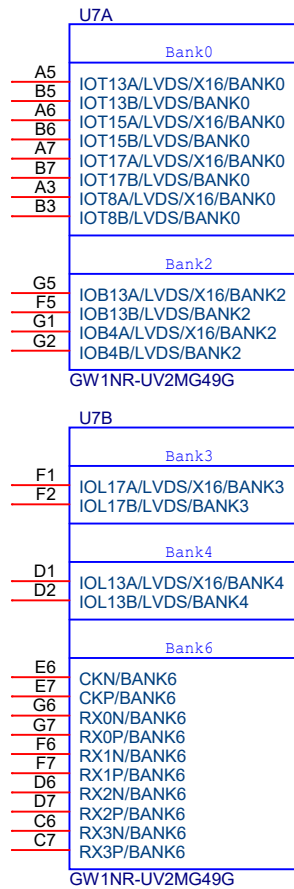
1.F_CLK signal is an external input clock signal.

It is recommended that F_CLK signal be provided through an active oscillator crystal.

2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
A4	GW1NR-LV2MG49PG	2.0
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GW1NR-UV2MG49G



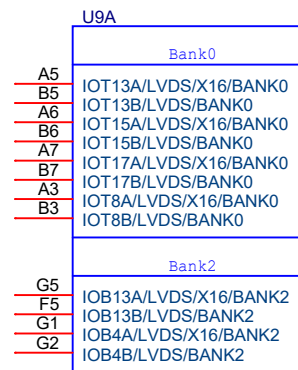
Notes:

1.F_CLK signal is an external input clock signal.

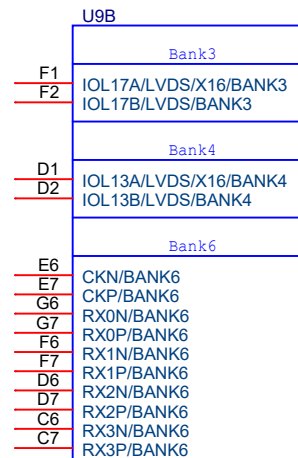
It is recommended that F_CLK signal be provided through an active oscillator crystal.

2.It is recommended that add an ESD protection chip to the JTAG download circuit.

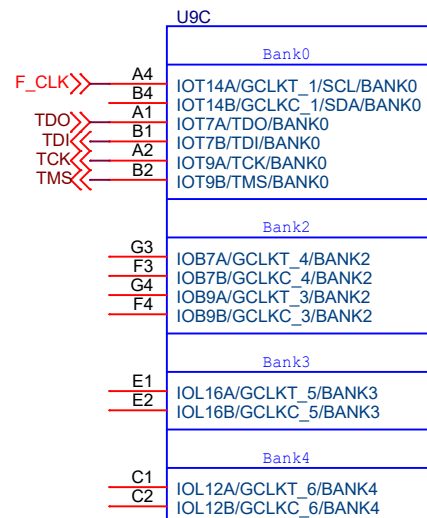
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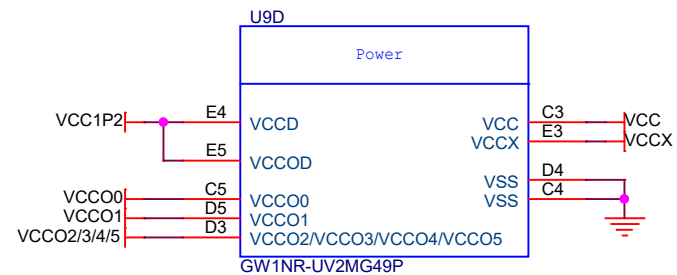
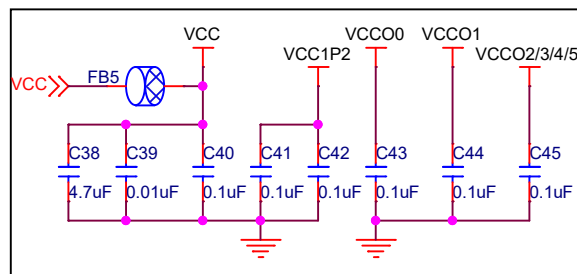
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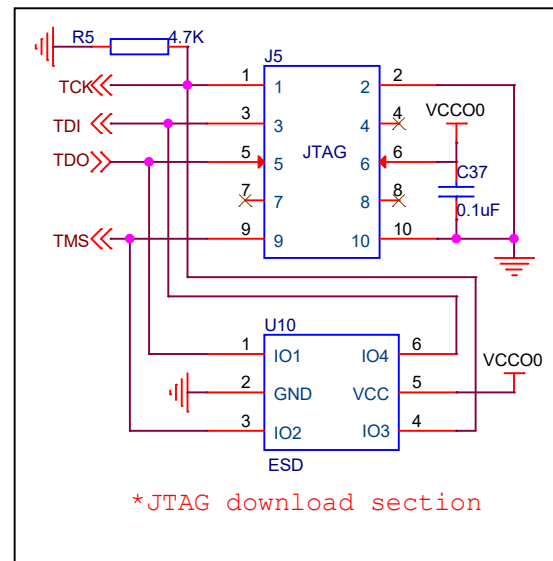
GW1NR-UV2MG49P



GW1NR-UV2MG49P



GW1NR-UV2MG49P



Notes:

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Title
GOWIN Minimum System Diagram

Size
A4

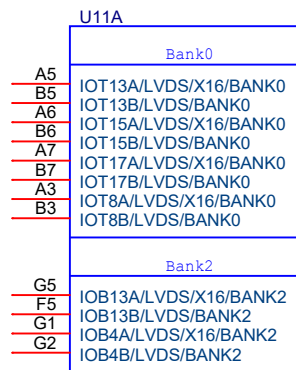
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GW1NR-UV2MG49P

Rev
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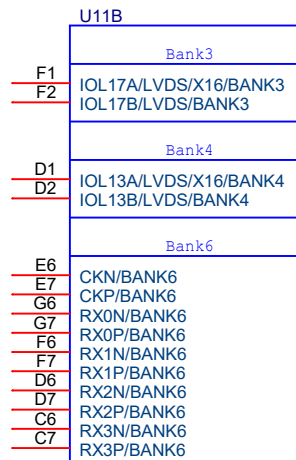
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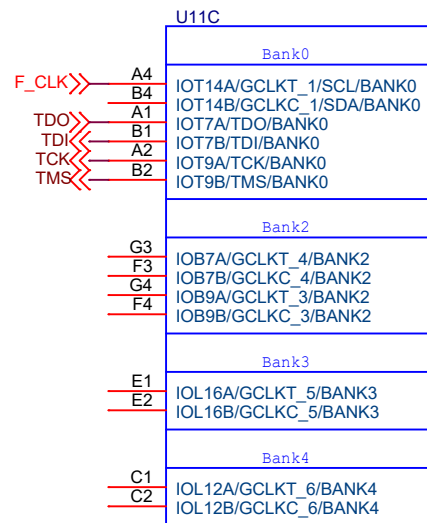
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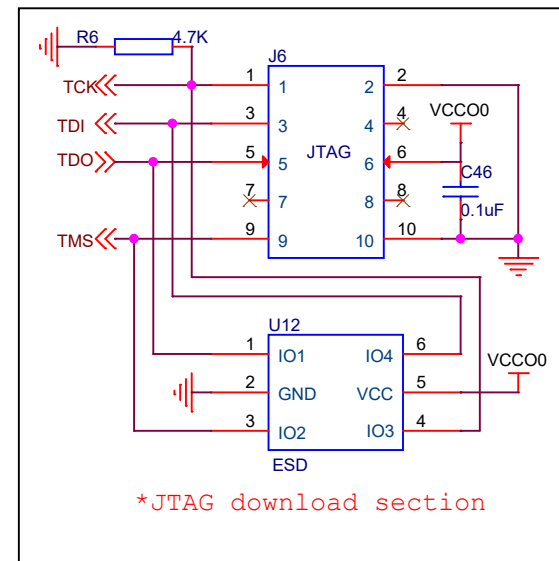
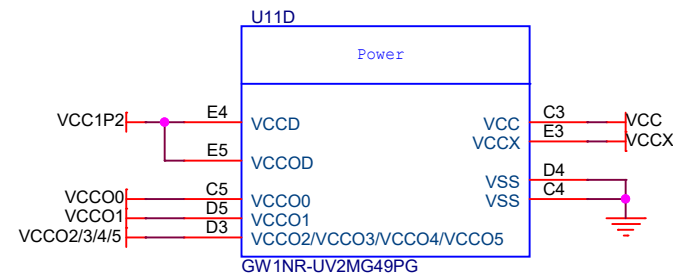
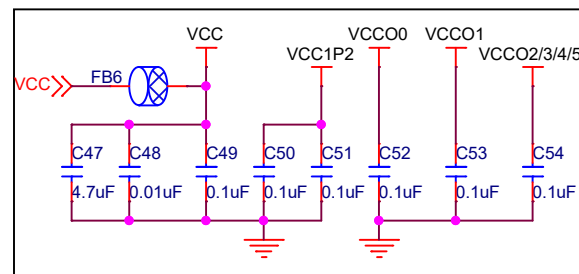
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GW1NR-UV2MG49PG



GW1NR-UV2MG49PG



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