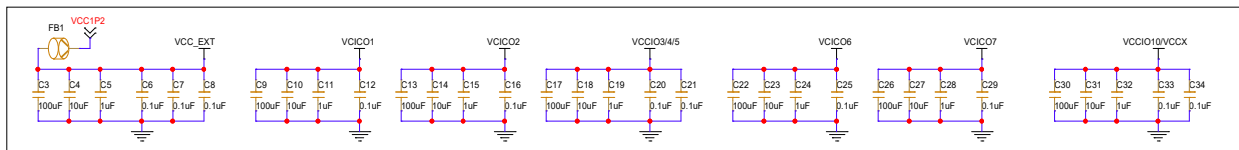
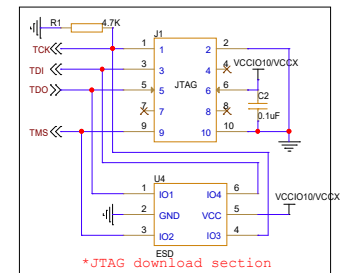
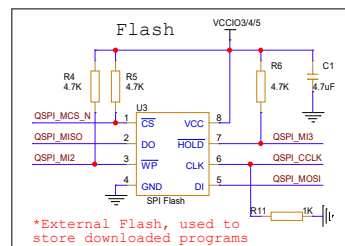
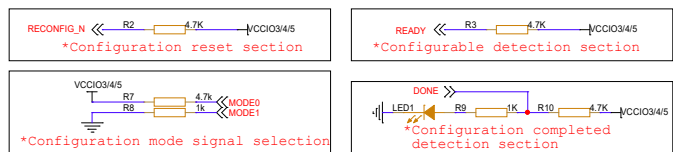
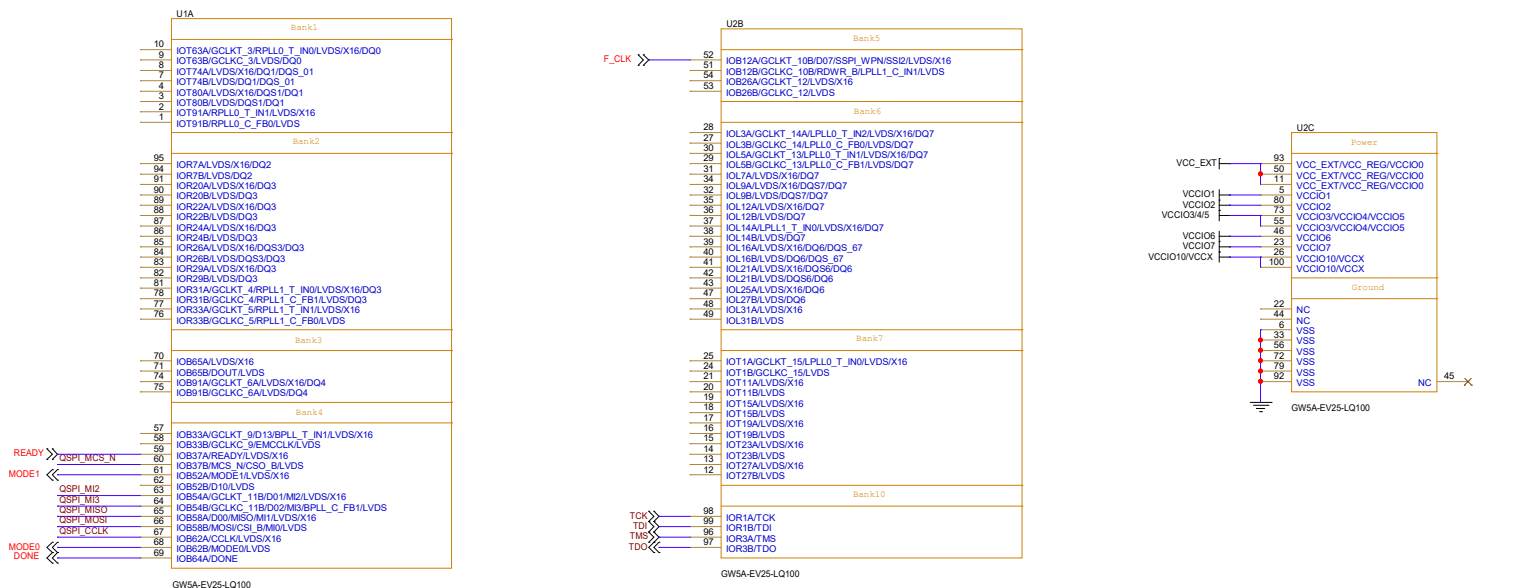


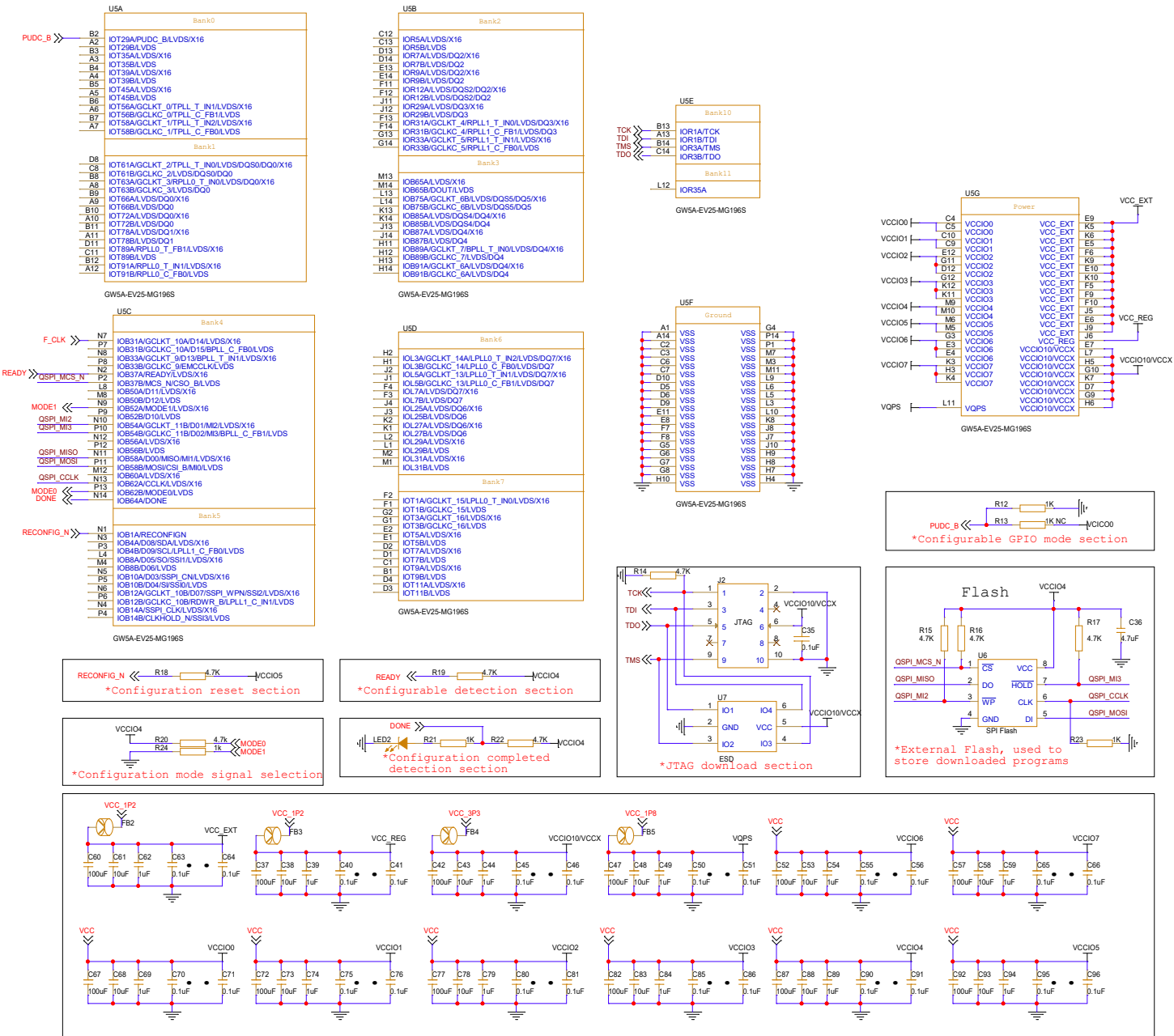
GW5A-EV25LQ100



Notes:

- 1.F CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG704, Arora V
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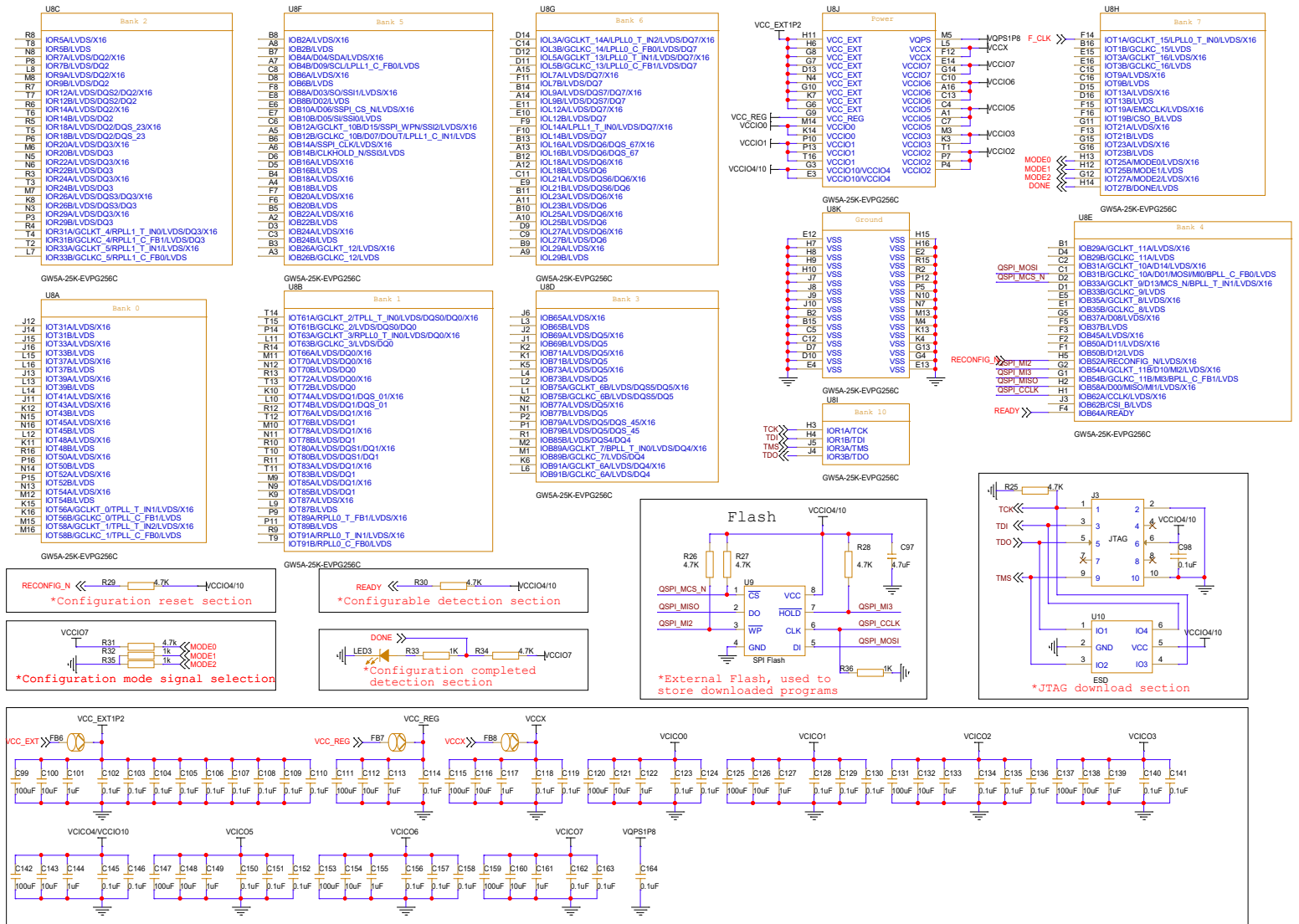
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Notes:

- 1.F CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash memory selection, see Chapter 10 SPI Flash Selection in UG290.
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For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG704, Arora V
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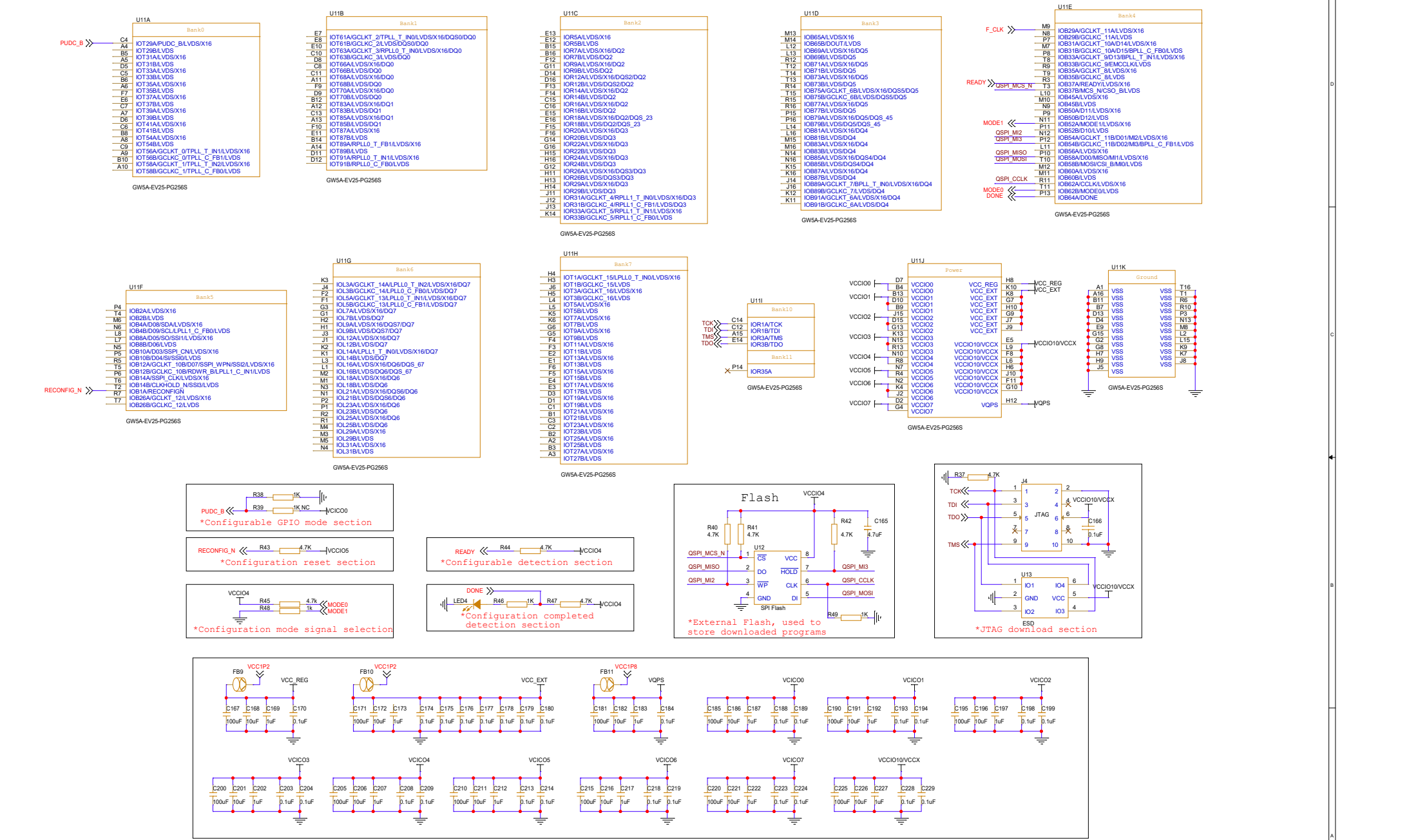
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Notes:

- F.CLK signal is an external input clock signal.
It is recommended that F.CLK signal be provided through an active oscillator crystal.
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For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
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- VCC core voltage requires a large current, so it is recommended to supply power separately.
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For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG704, Arora V FPGA Product Programming and Configuration Guide.

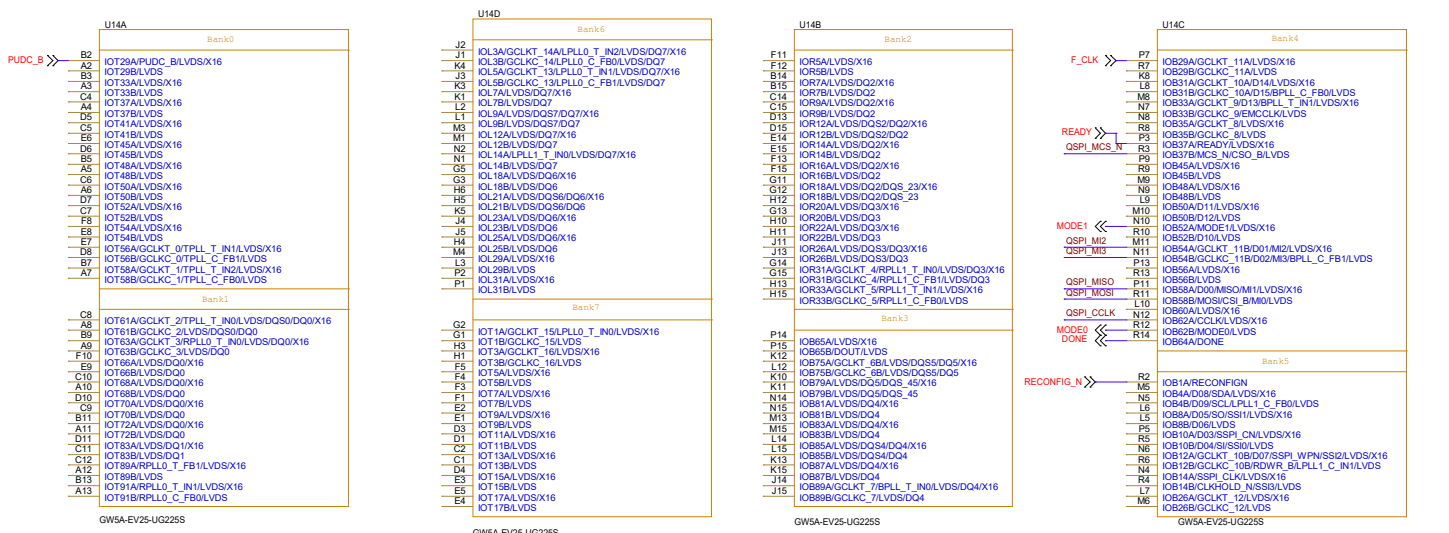
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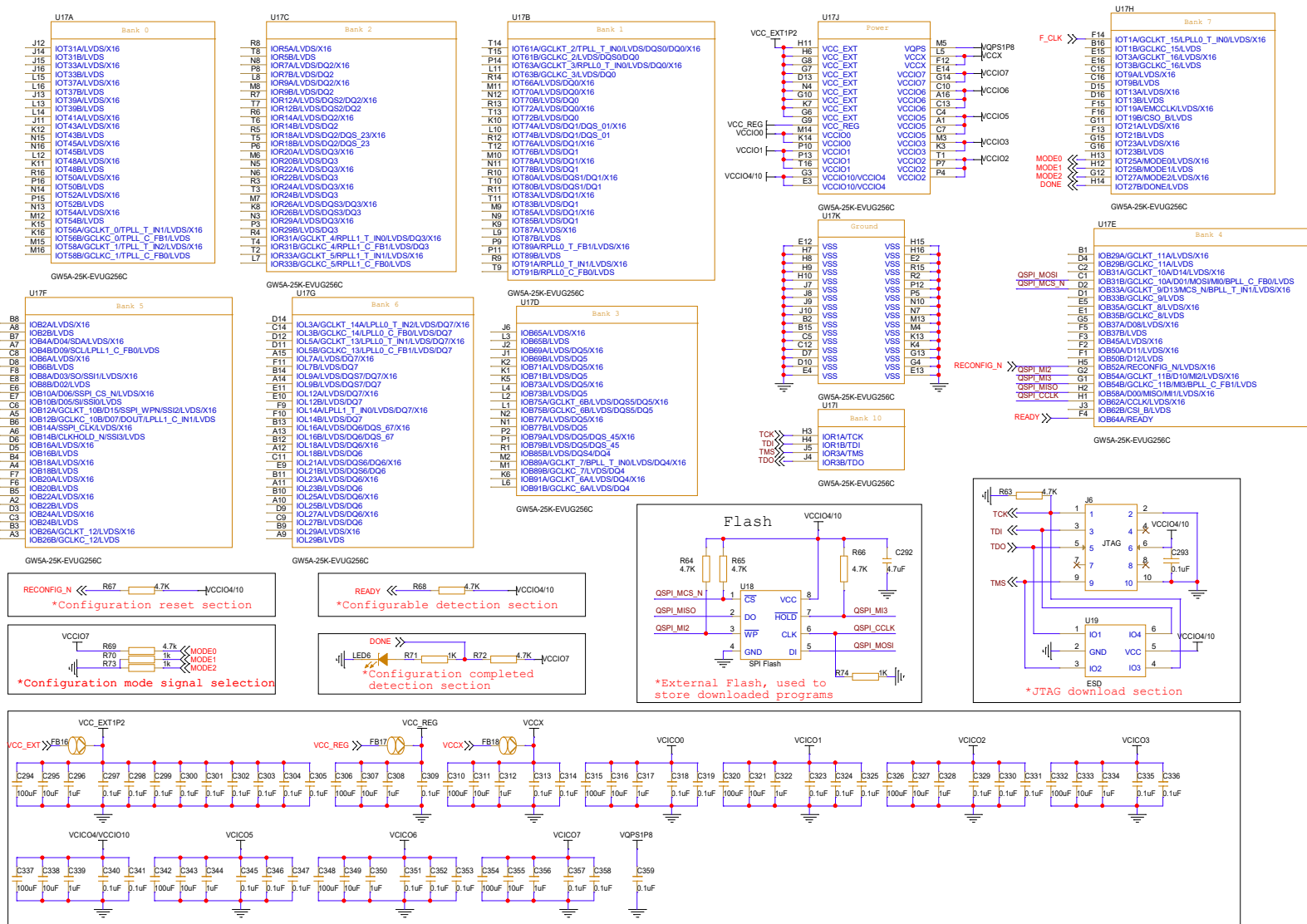
Notes:

- 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
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- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG704, Arora V
FPGA Product Programming and Configuration Guide.

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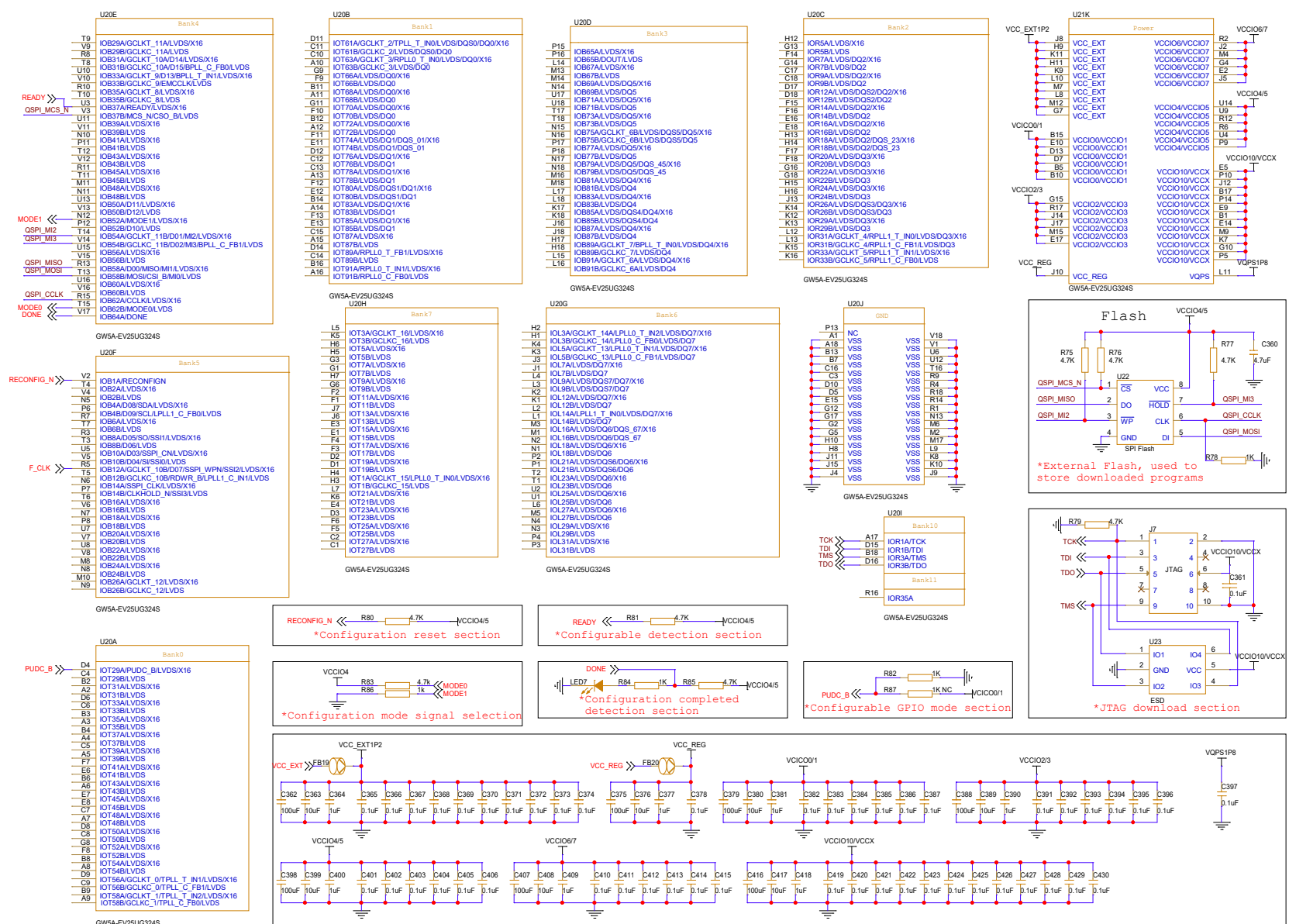


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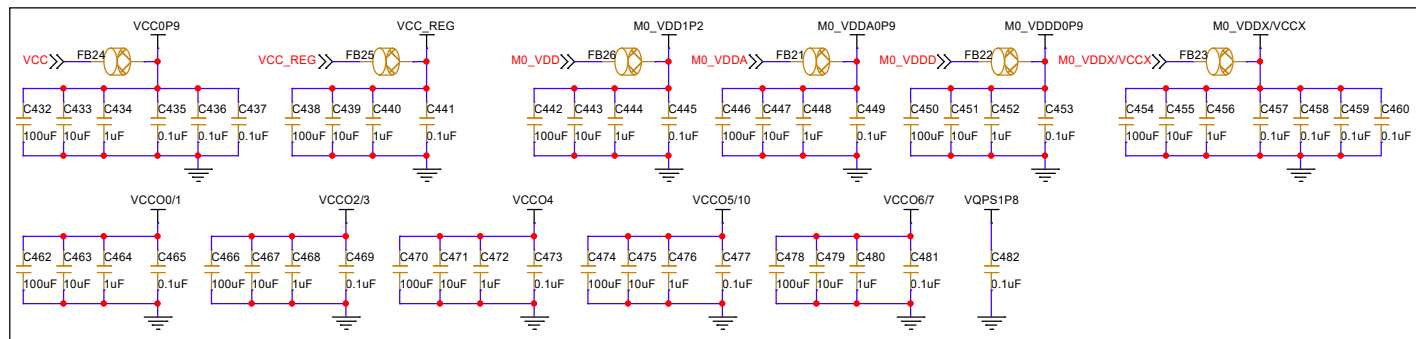
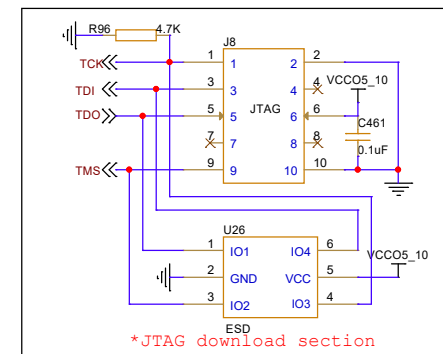
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Notes:

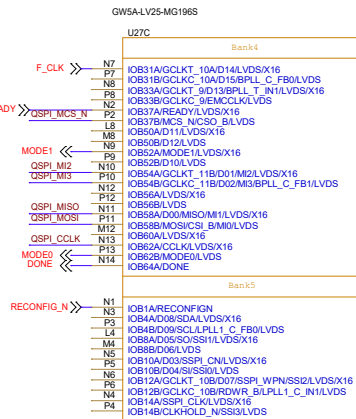
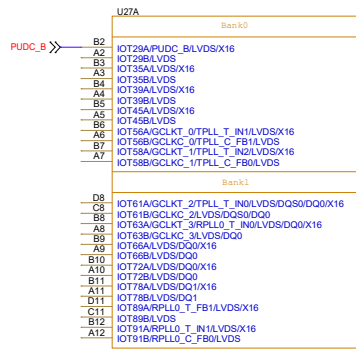
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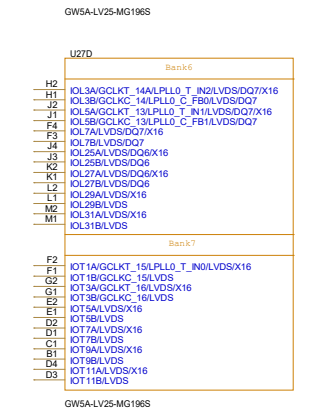
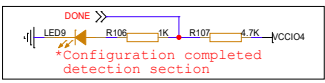
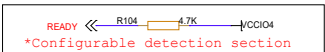
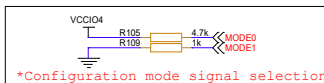
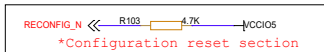


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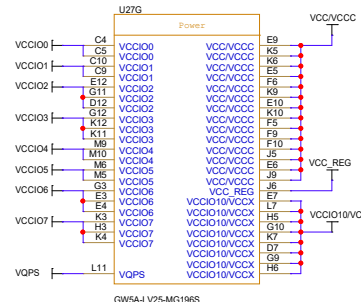
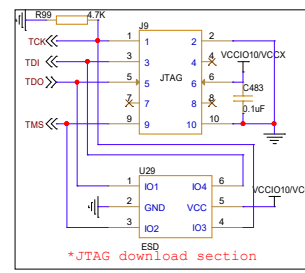
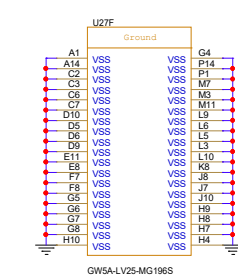
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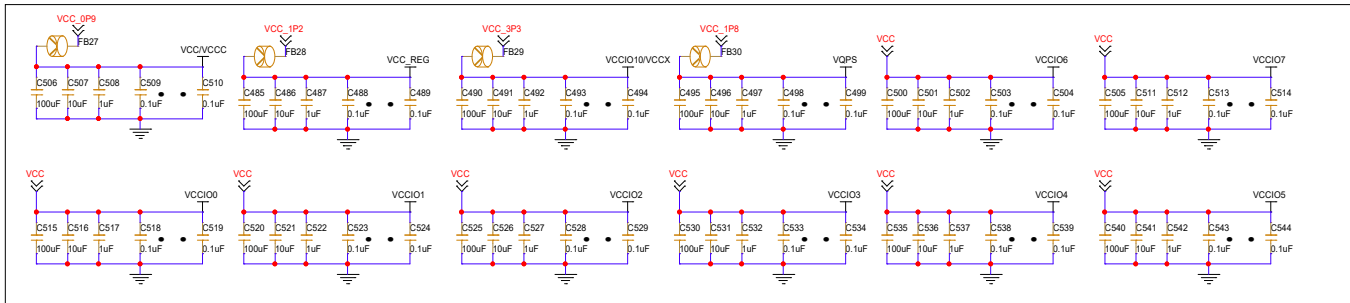
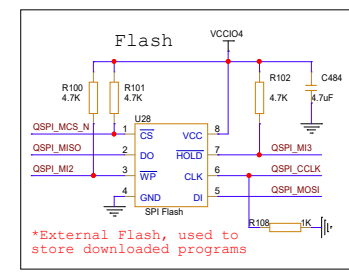
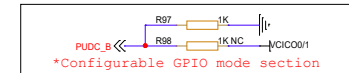
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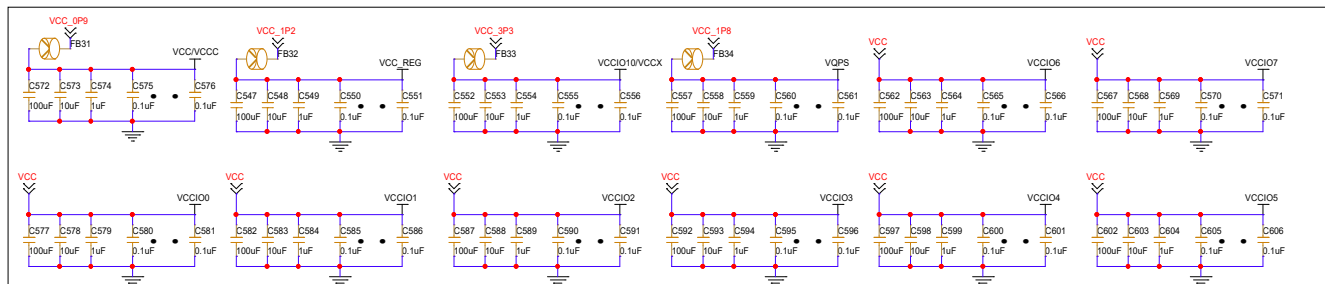
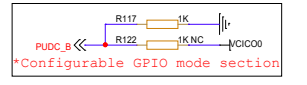
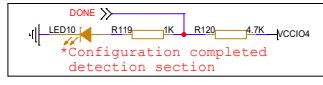
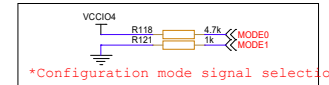
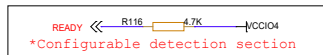
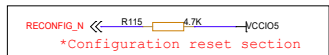
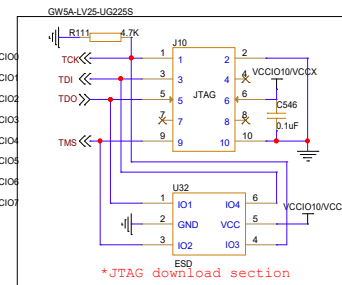
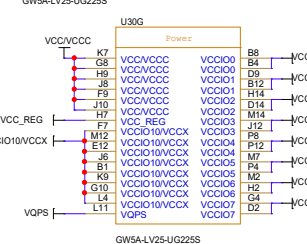
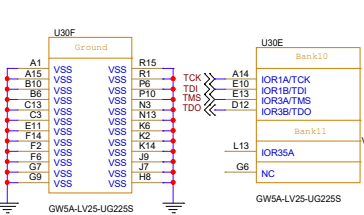
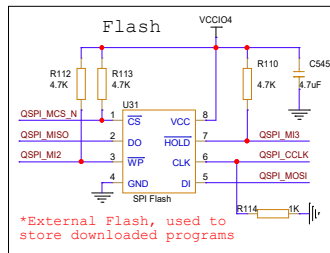
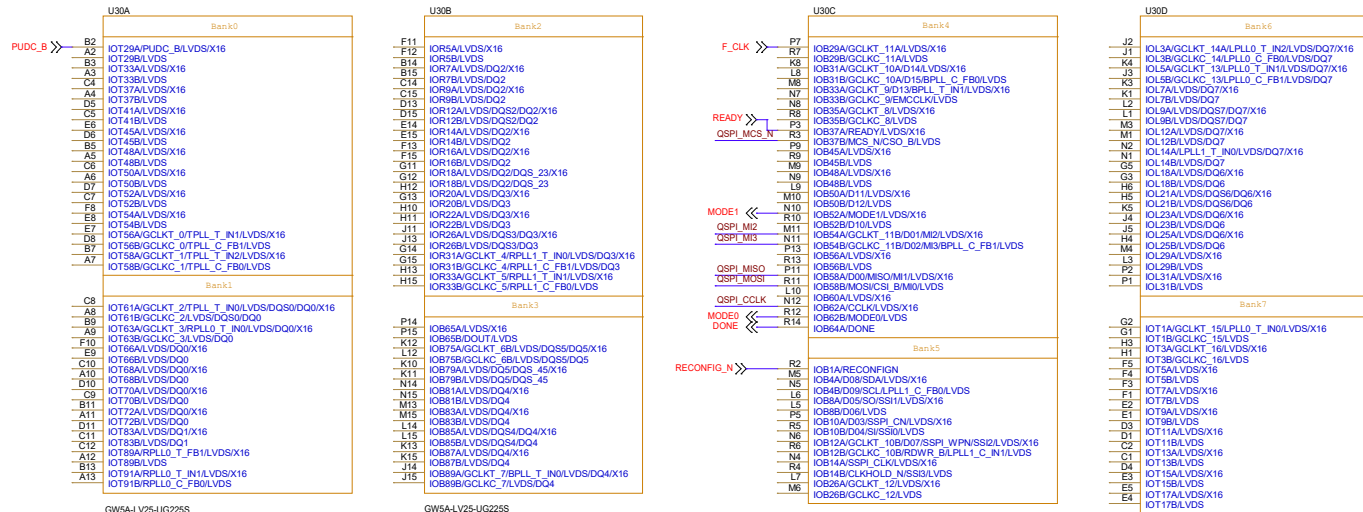


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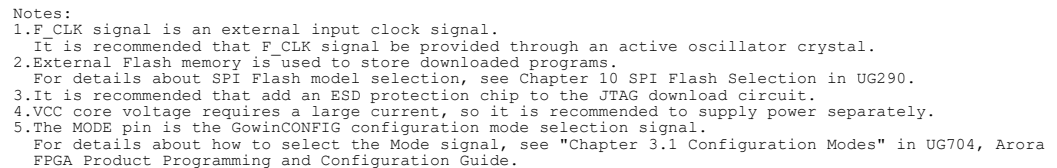
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 - 9.FPGA Product Programming and Configuration Guide.

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