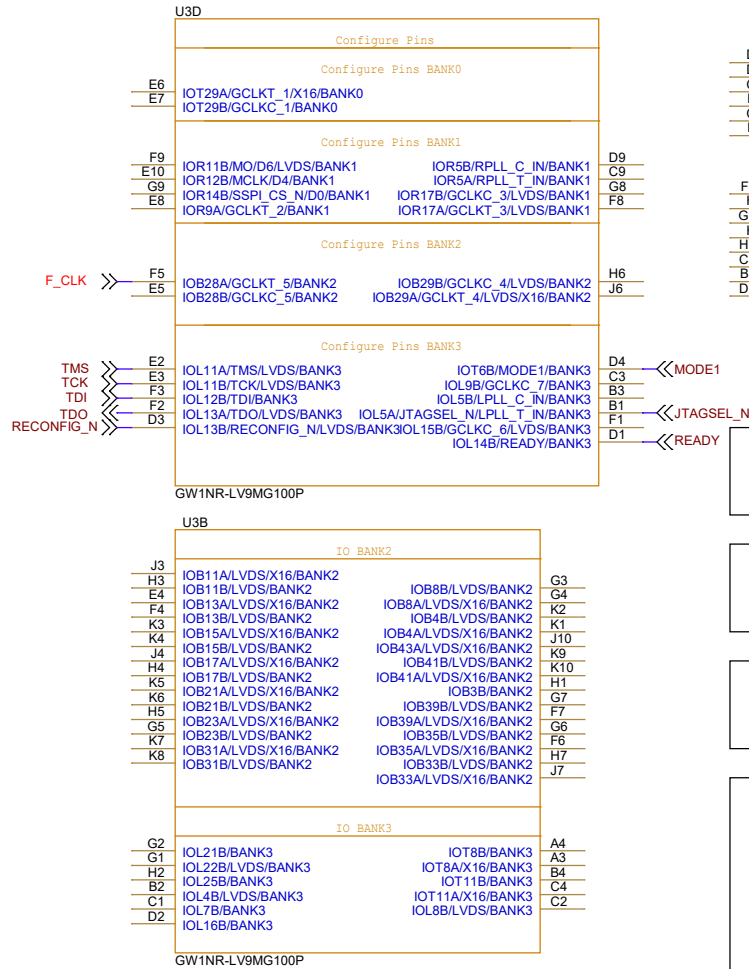


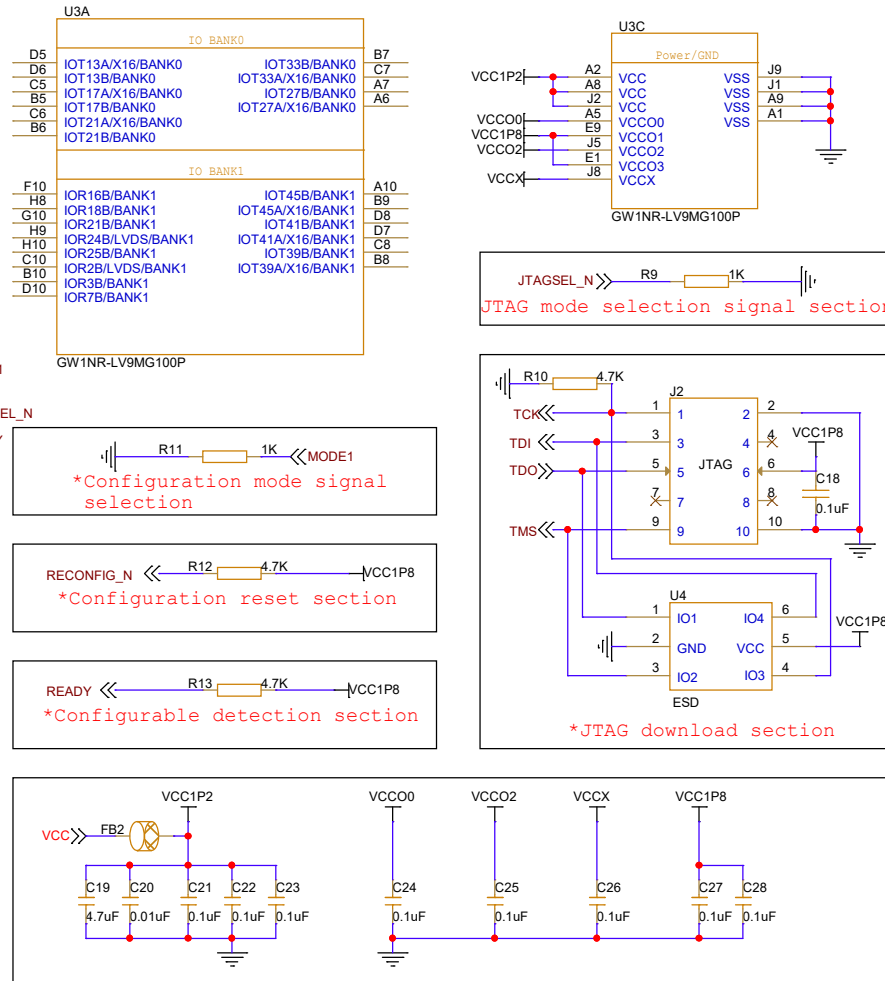
Notes:
1.F CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal.
2.It is recommended that add an ESD protection chip to the JTAG download circuit.

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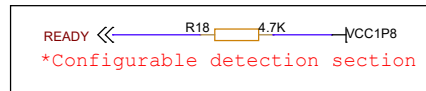
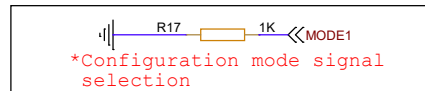


Notes:

- 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

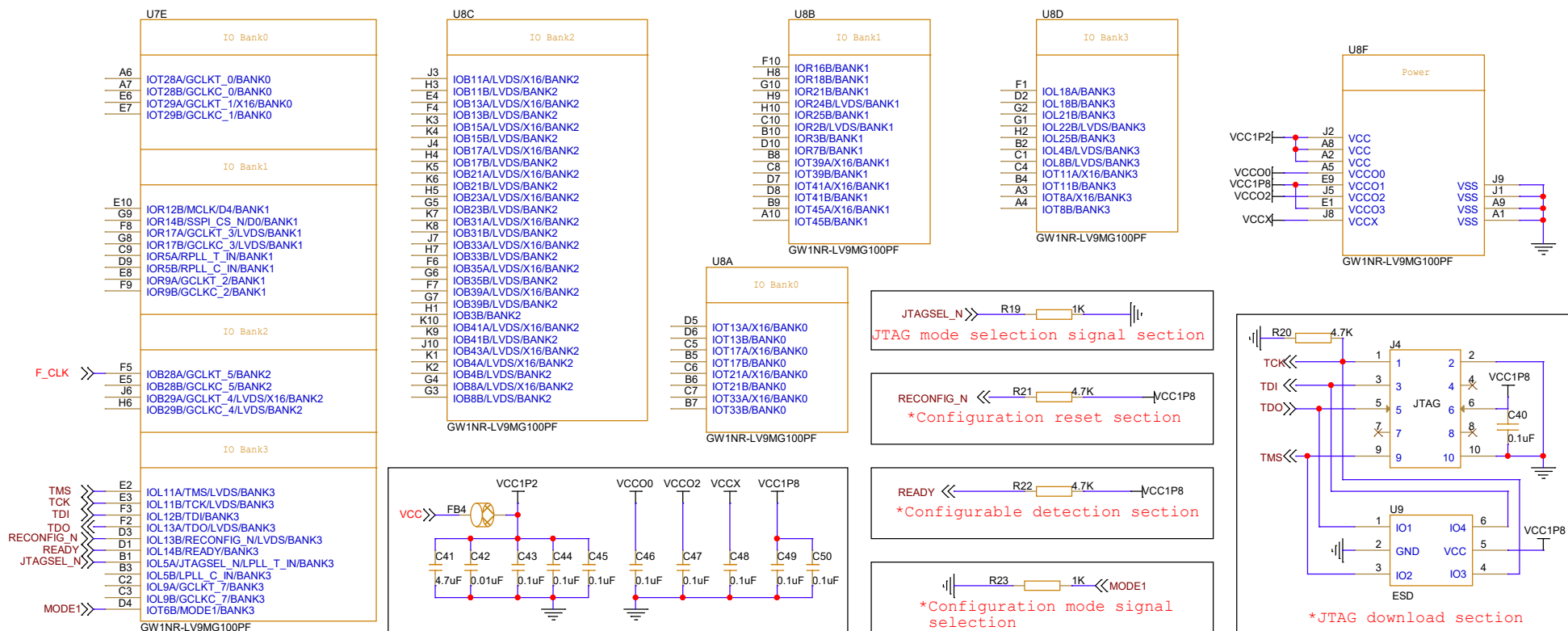


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| Title | | |
| GOWIN Minimum System Diagram | | |
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1.F CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.

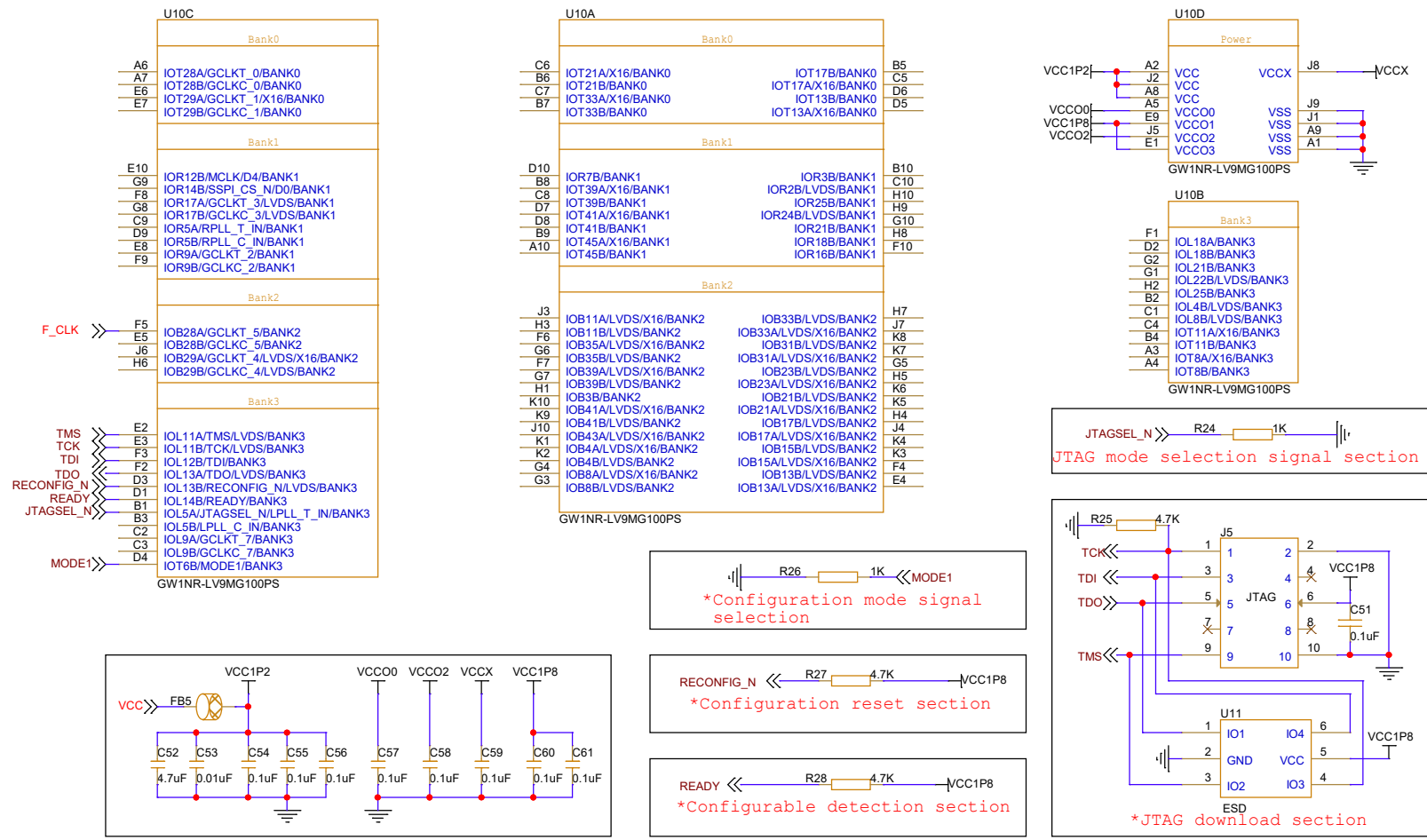
2.It is recommended that add an ESD protection chip to the JTAG download circuit.



Notes:

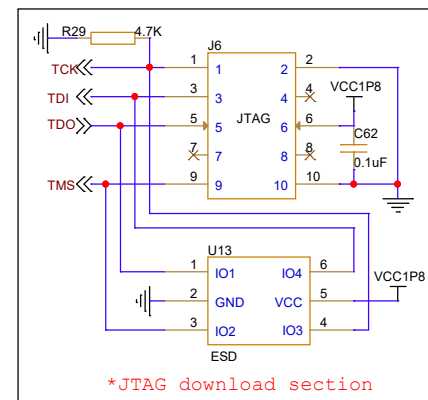
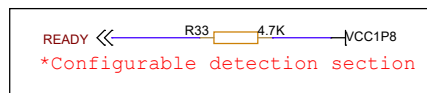
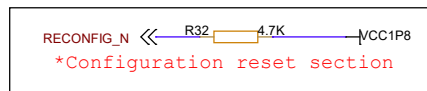
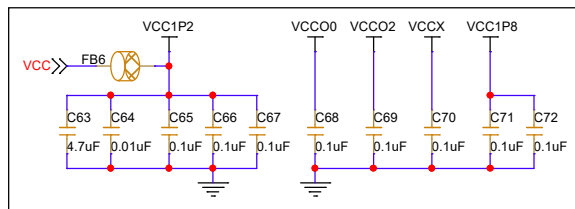
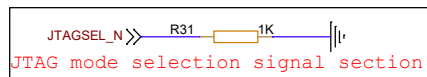
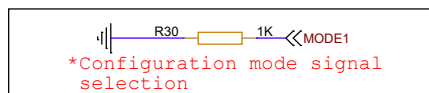
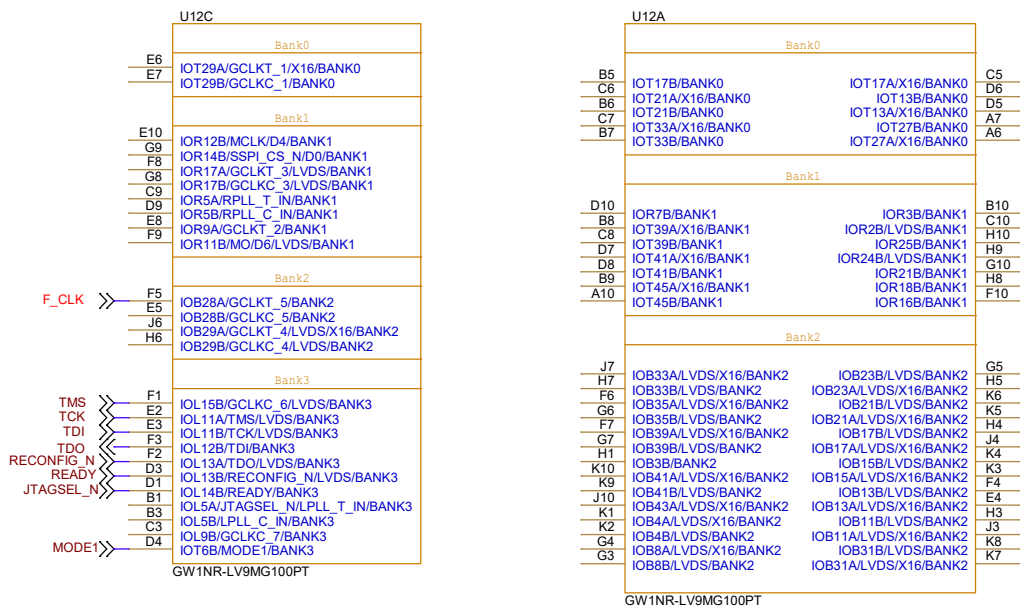
- 1.F CLK signal is an external input clock signal. It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

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| Title | | |
| GOWIN Minimum System Diagram | | |
| Size B | Document Number GW1NR-LV9MG100PF | Rev 2.1 |
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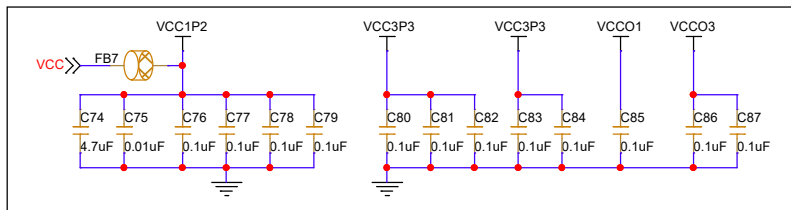
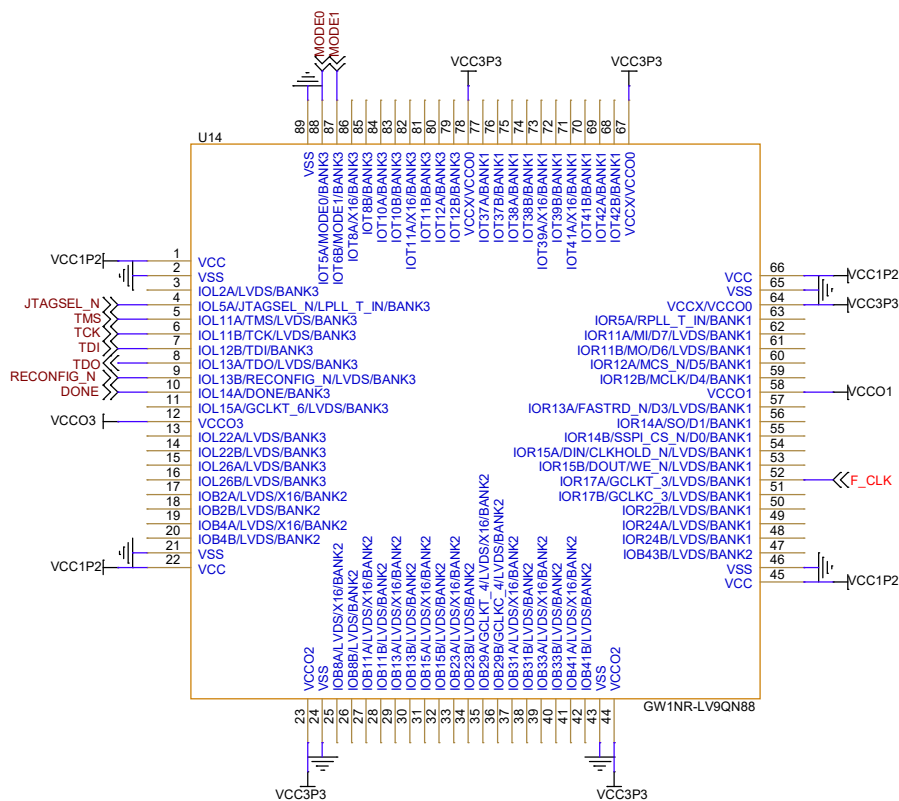
Notes:
1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2.It is recommended that add an ESD protection chip to the JTAG download circuit.

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| GOWIN Minimum System Diagram | | |
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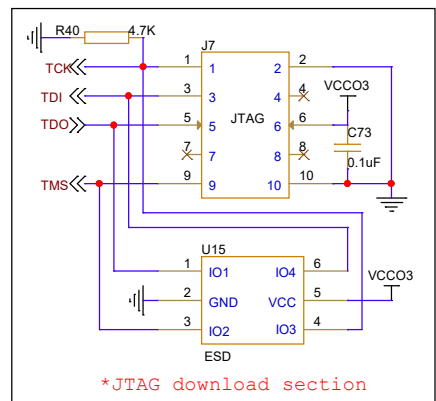
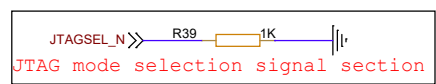
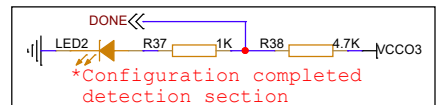
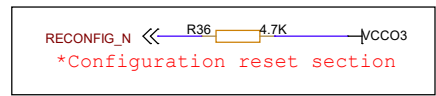
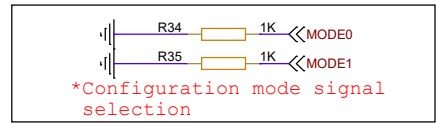


- Notes:
- 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
 - 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

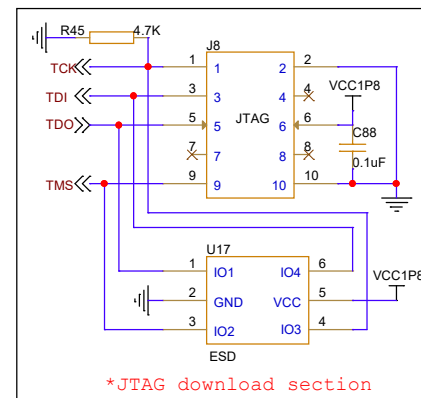
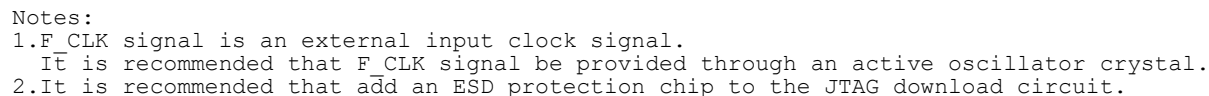
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| Title | | |
| GOWIN Minimum System Diagram | | |
| Size | Document Number | Rev |
| B | GW1NR-LV9MG100PT | 2.1 |
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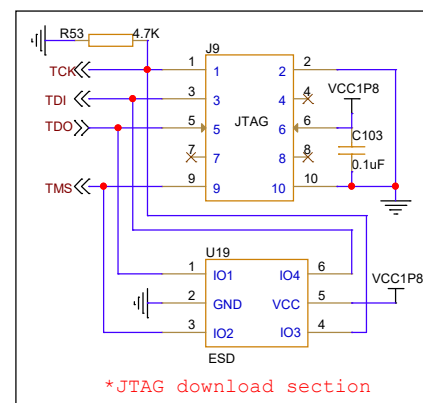
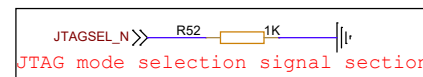
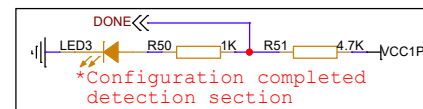
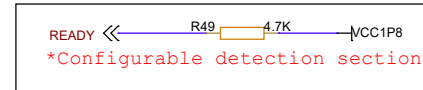
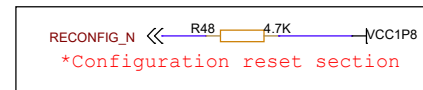
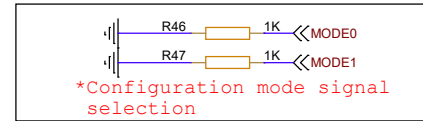
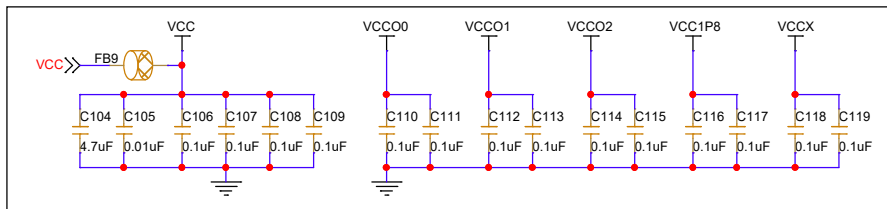
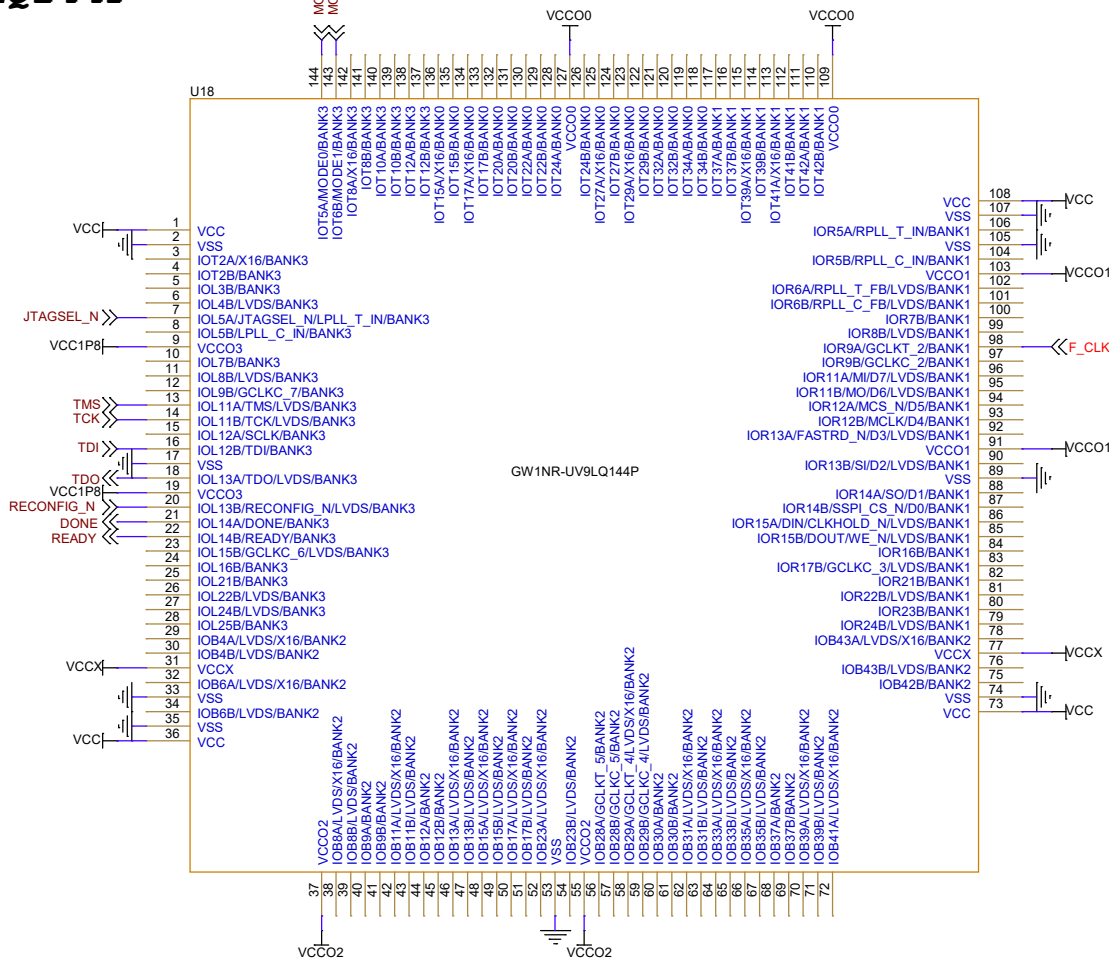
Notes:
 1. F CLK signal is an external input clock signal.
 It is recommended that F CLK signal be provided through an active oscillator crystal.
 2. It is recommended that add an ESD protection chip to the JTAG download circuit.



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| Title | | | |
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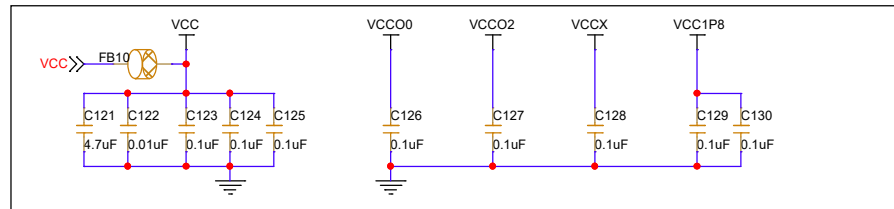
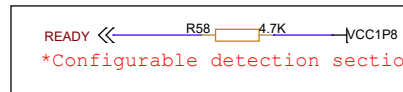
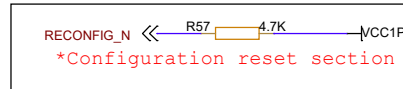
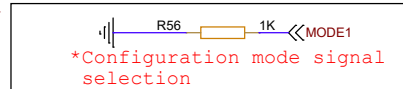
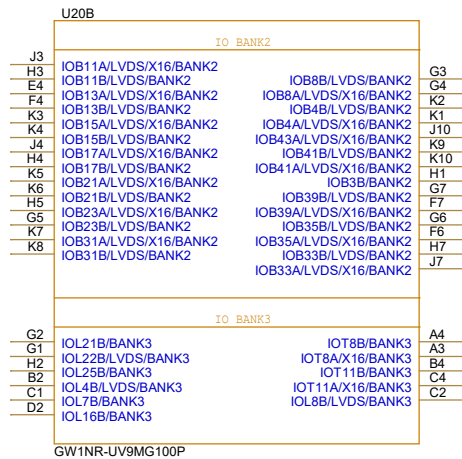
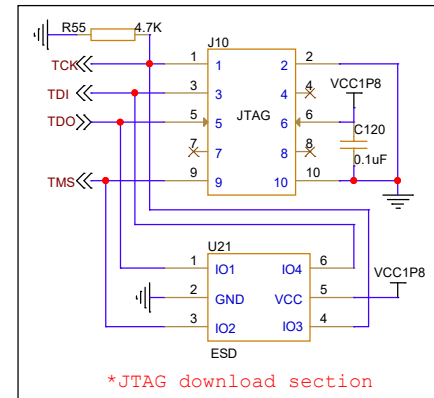
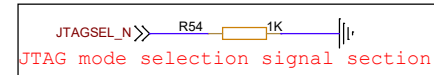
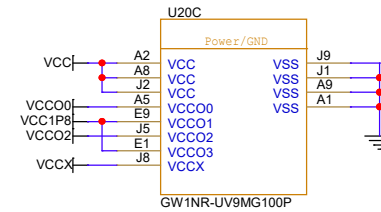
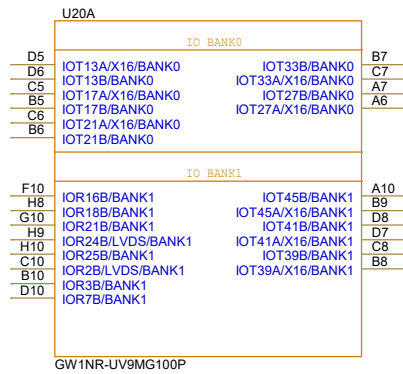
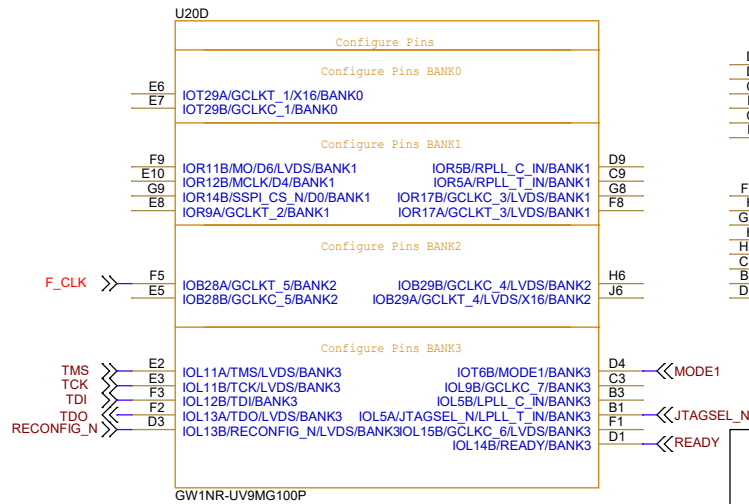


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| Title | | | |
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Notes:
1.F CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal.
2.It is recommended that add an ESD protection chip to the JTAG download circuit.

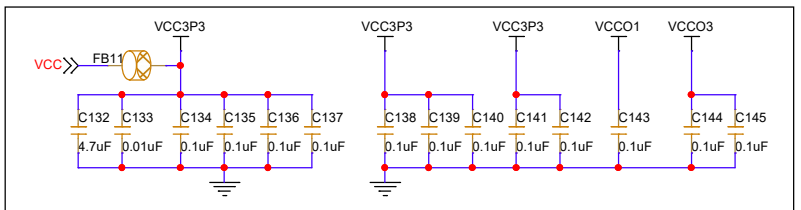
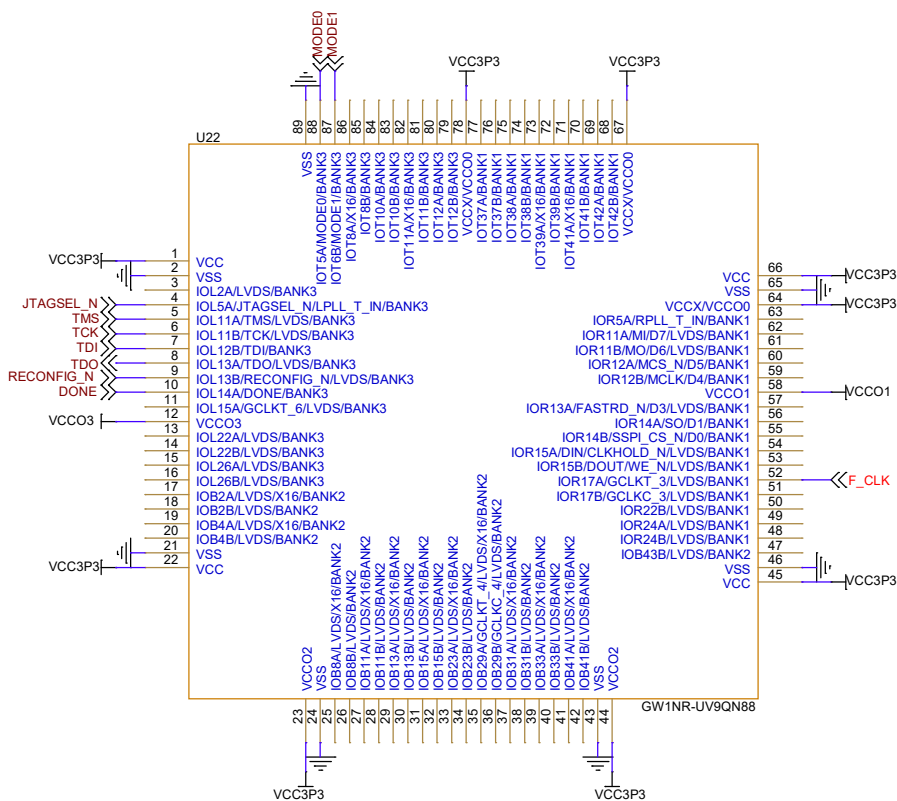
| | | |
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| Title | | |
| GOWIN Minimum System Diagram | | |
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Notes:

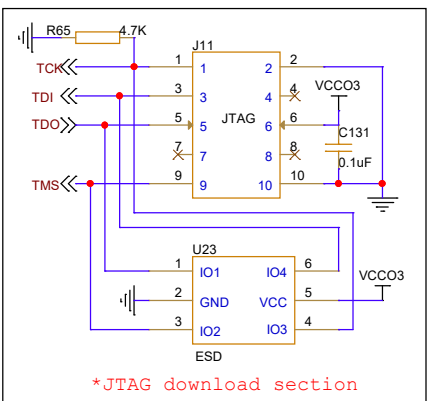
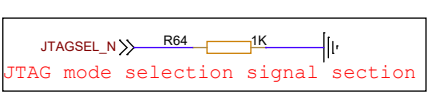
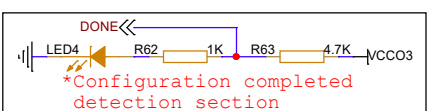
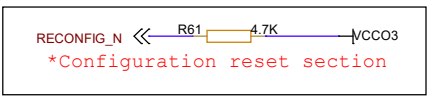
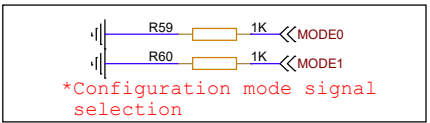
- 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

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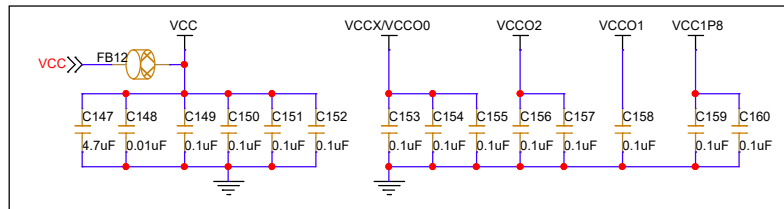
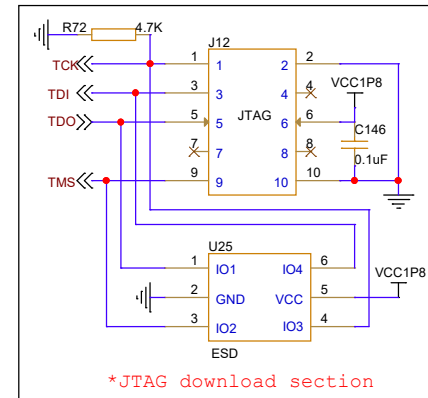
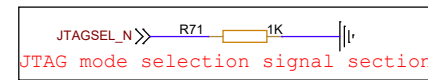
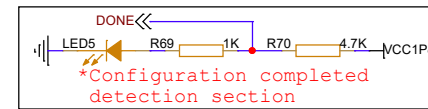
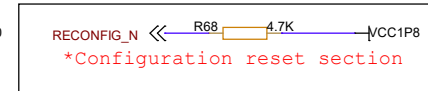
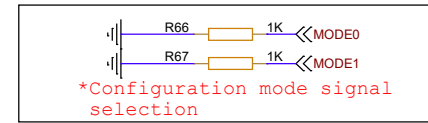
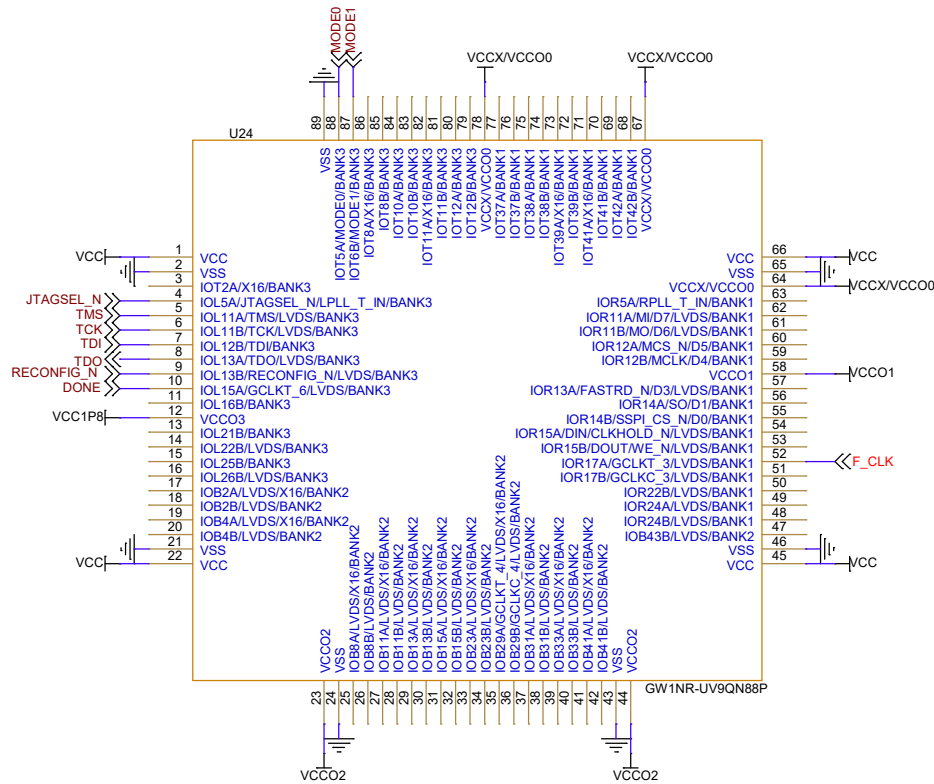


Notes:

- 1.F CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.



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Notes:

- 1.F CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

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| Title | | |
| GOWIN Minimum System Diagram | | |
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