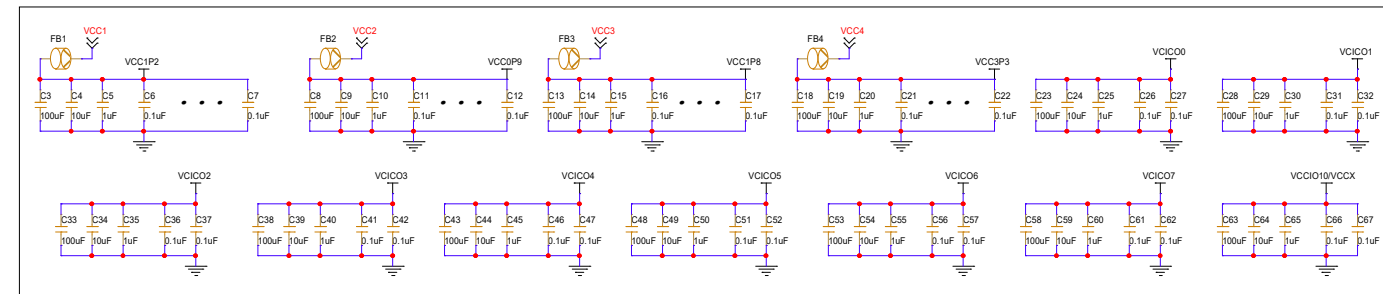
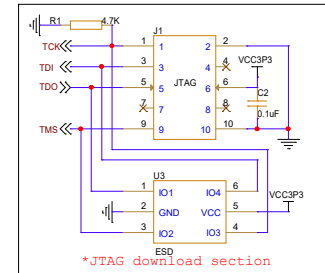
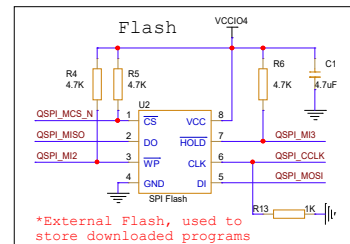
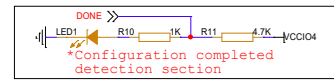
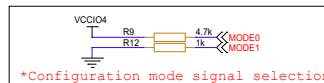
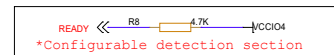
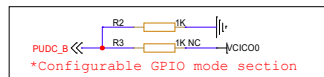
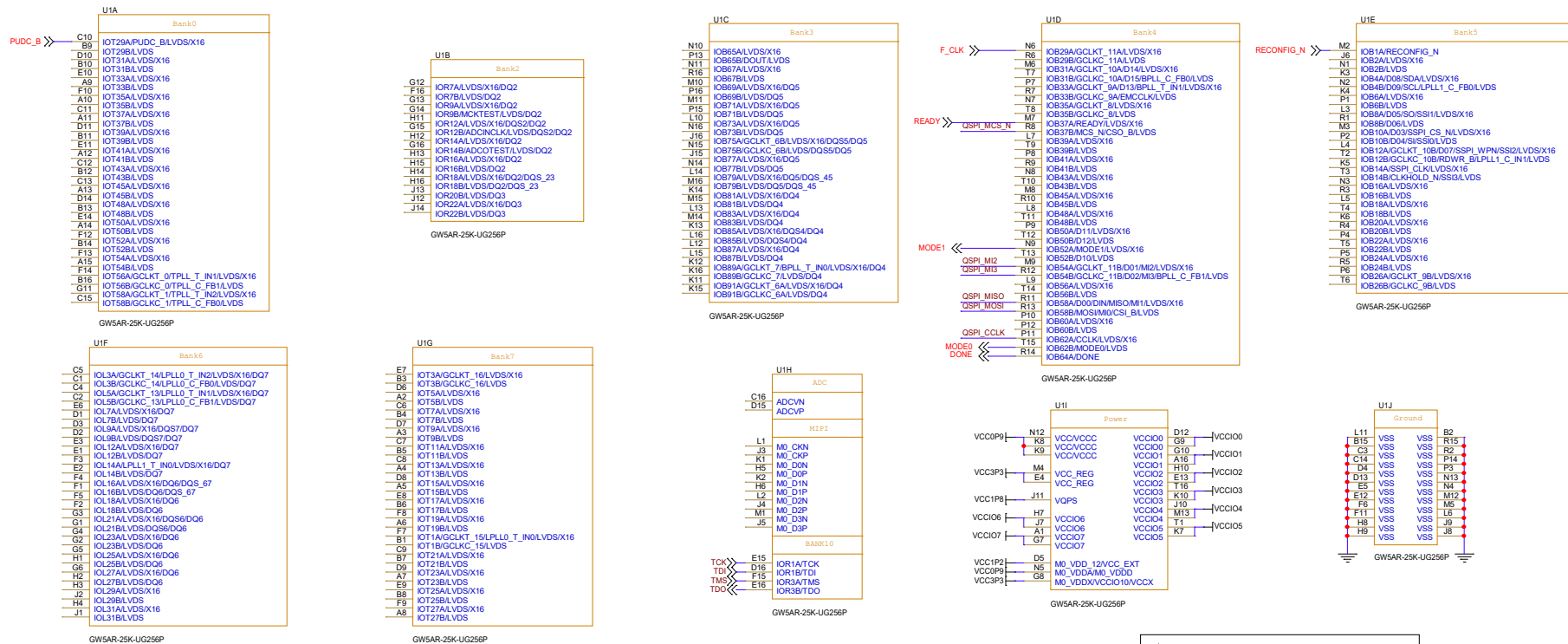


5	4	3	2	1
---	---	---	---	---



Notes:

1. F.CLK signal is an external input clock signal.  
It is recommended that F.CLK signal be provided through an active oscillator crystal.
2. External Flash memory is used to store downloaded programs.  
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
3. It is recommended that add an ESD protection chip to the JTAG download circuit.
4. Core voltage requires a large current, so it is recommended to supply power separately.
5. The MODE pin is the GowinCONF1 configuration mode selection signal.  
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG704, Arora V  
FPGA Product Programming and Configuration Guide.

Title			
GOWIN Minimum System Diagram			
Size	Document Number		Rev
C	GWSAR-25K-UG256P		2.0
Date:	Tuesday, September 05, 2023	Sheet	1 of 1