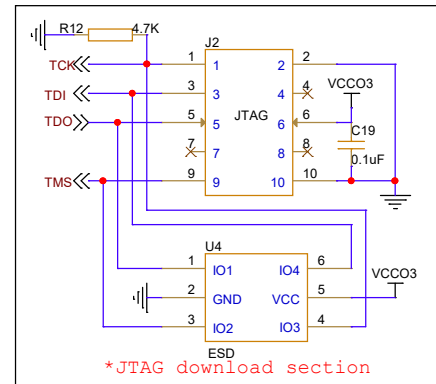
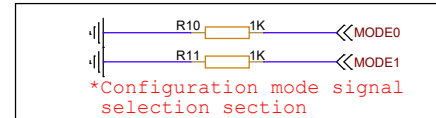
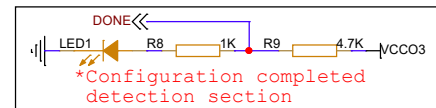
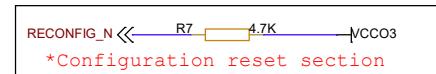
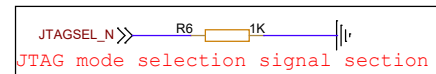
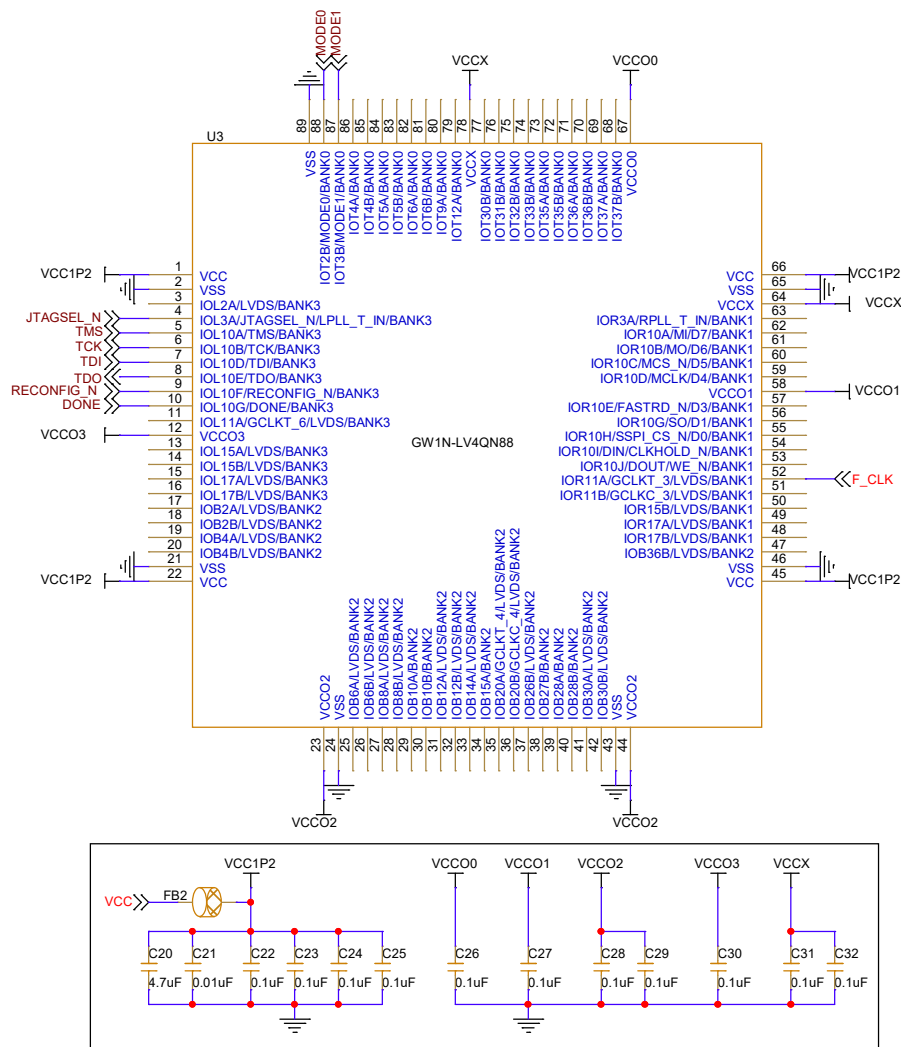


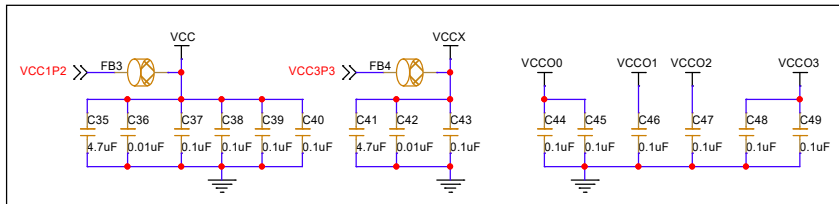
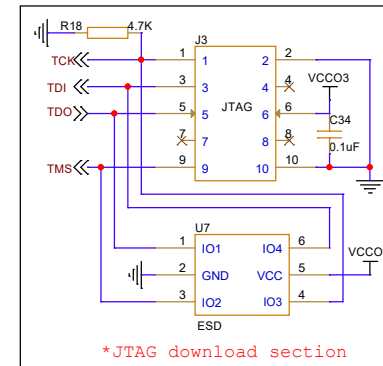
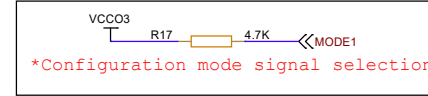
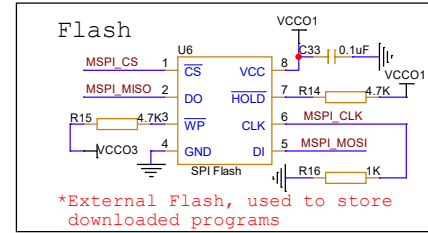
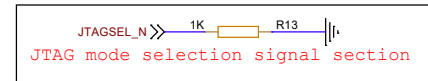
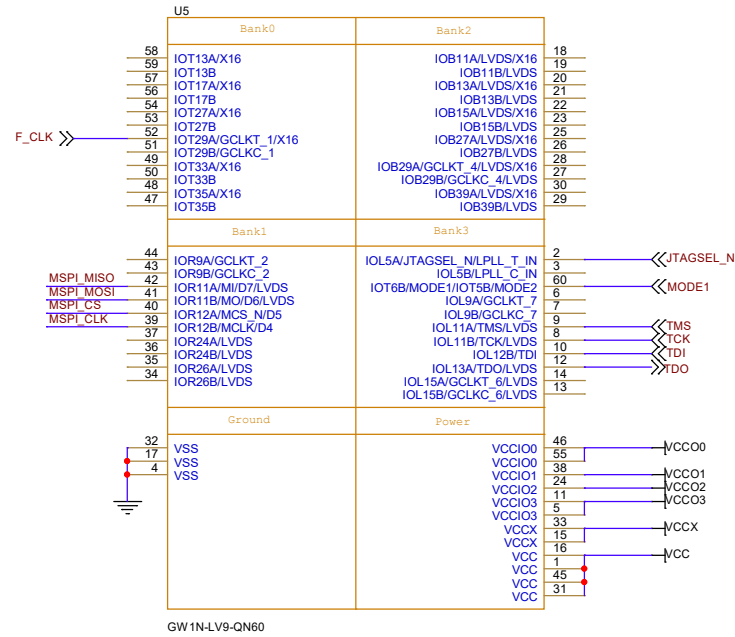
GW1N-LV4QN88



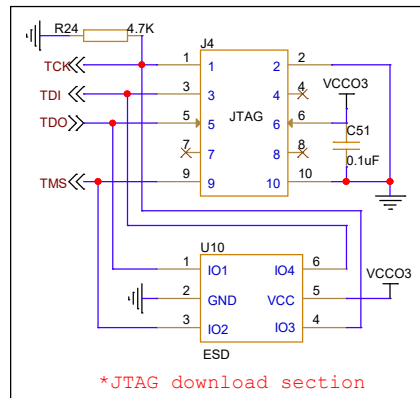
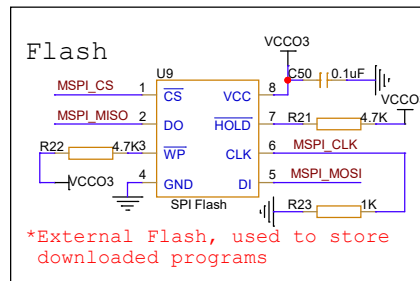
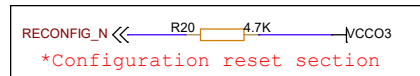
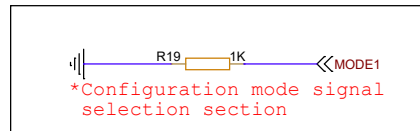
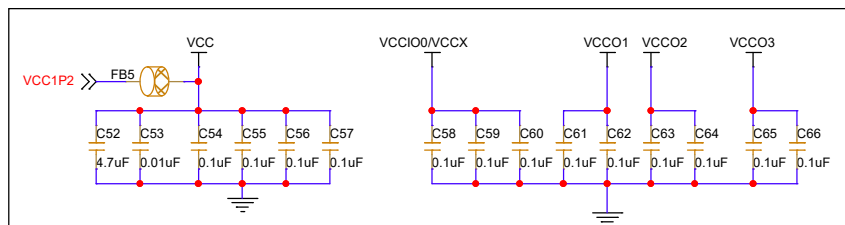
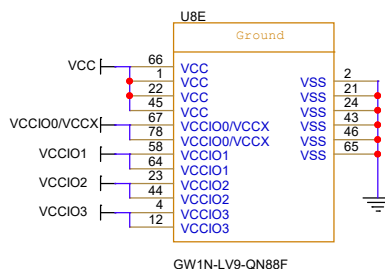
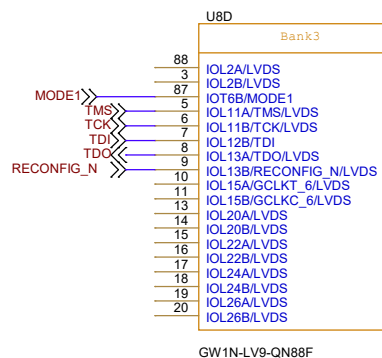
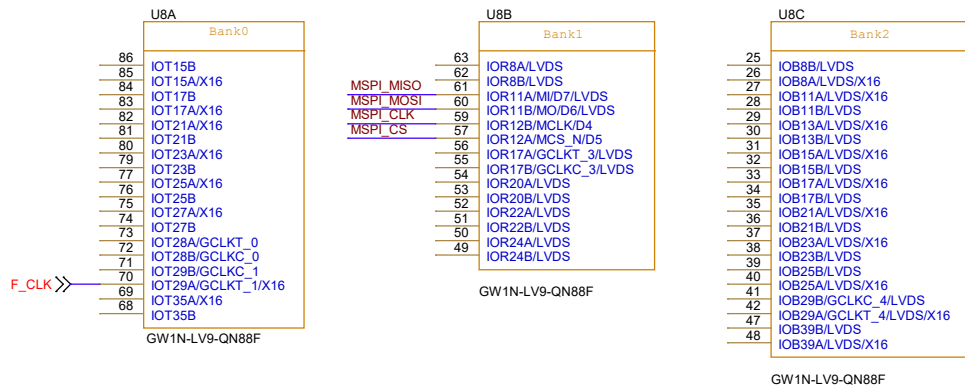
Notes:

- 1.F CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
Gowin FPGA-AOTOMOTIVE Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-LV4QN88	2.5
Date:	Tuesday, October 31, 2023	Sheet 2 of 10



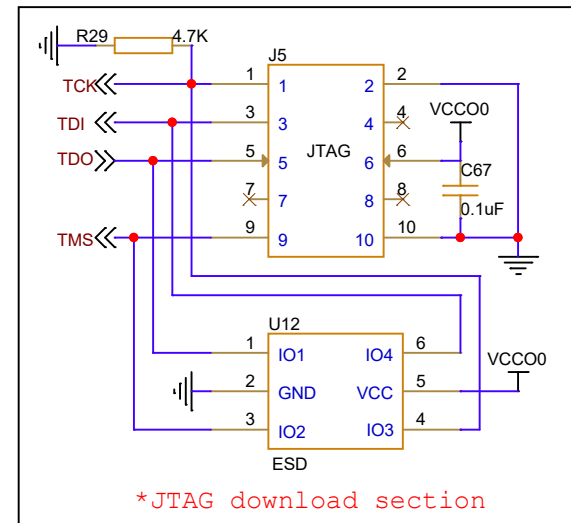
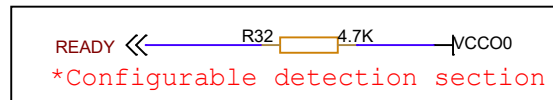
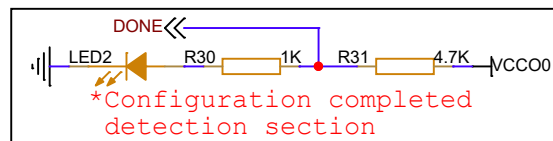
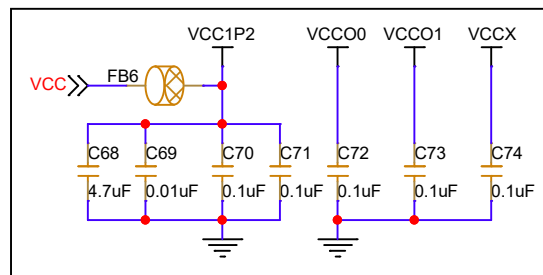
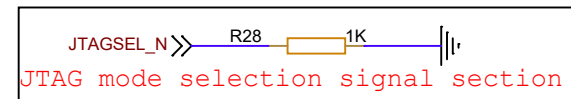
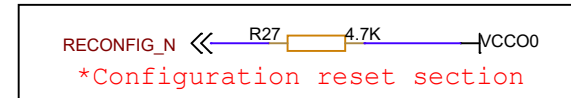
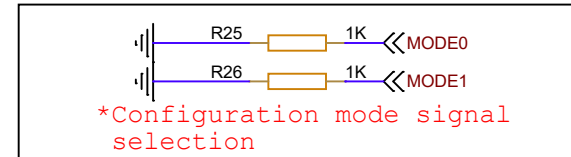
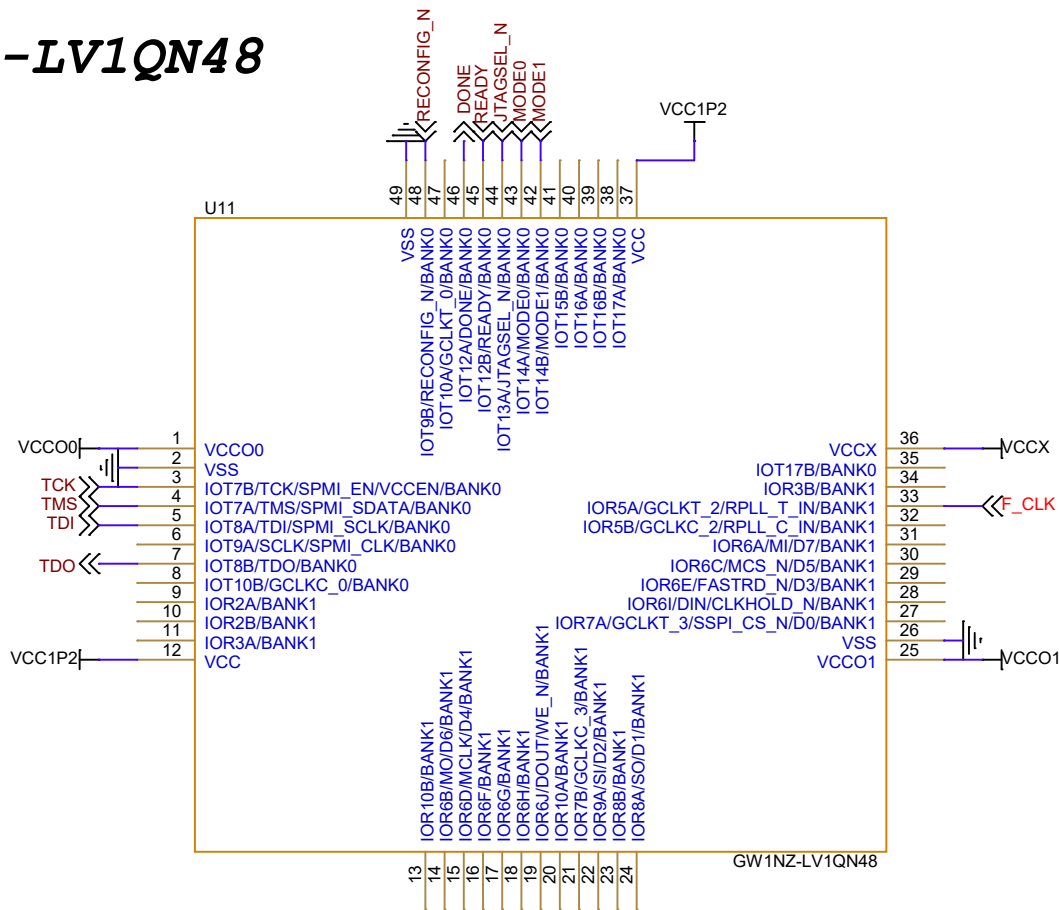
- Notes:
- 1.F CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
 - 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
 - 3.It is recommended that add an ESD protection chip to the JTAG download circuit.



- Notes:
- 1.F CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
 - 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size B	Document Number GW1N-LV9QN88F	Rev 2.5
Date:	Tuesday, October 31, 2023	Sheet 4 of 10

GW1NZ-LV1QN48



Notes:

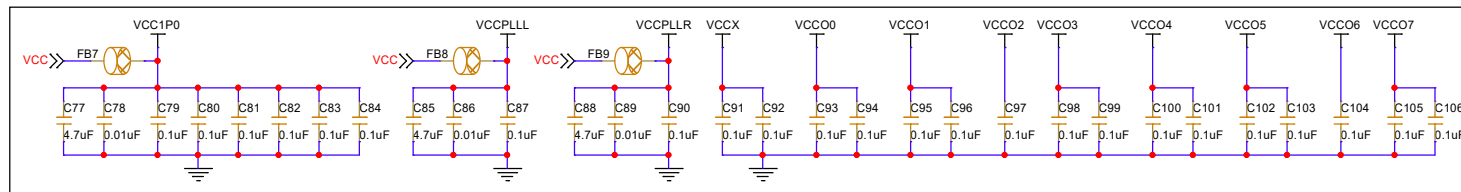
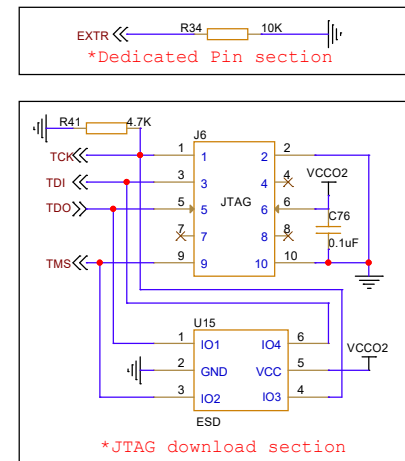
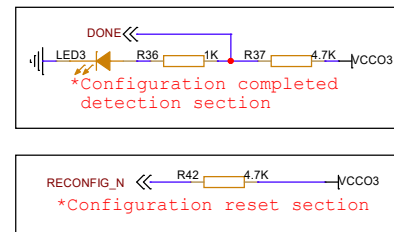
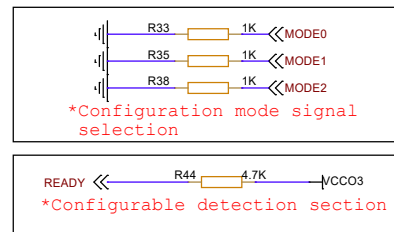
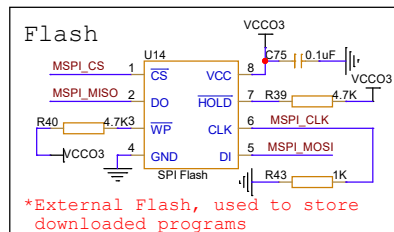
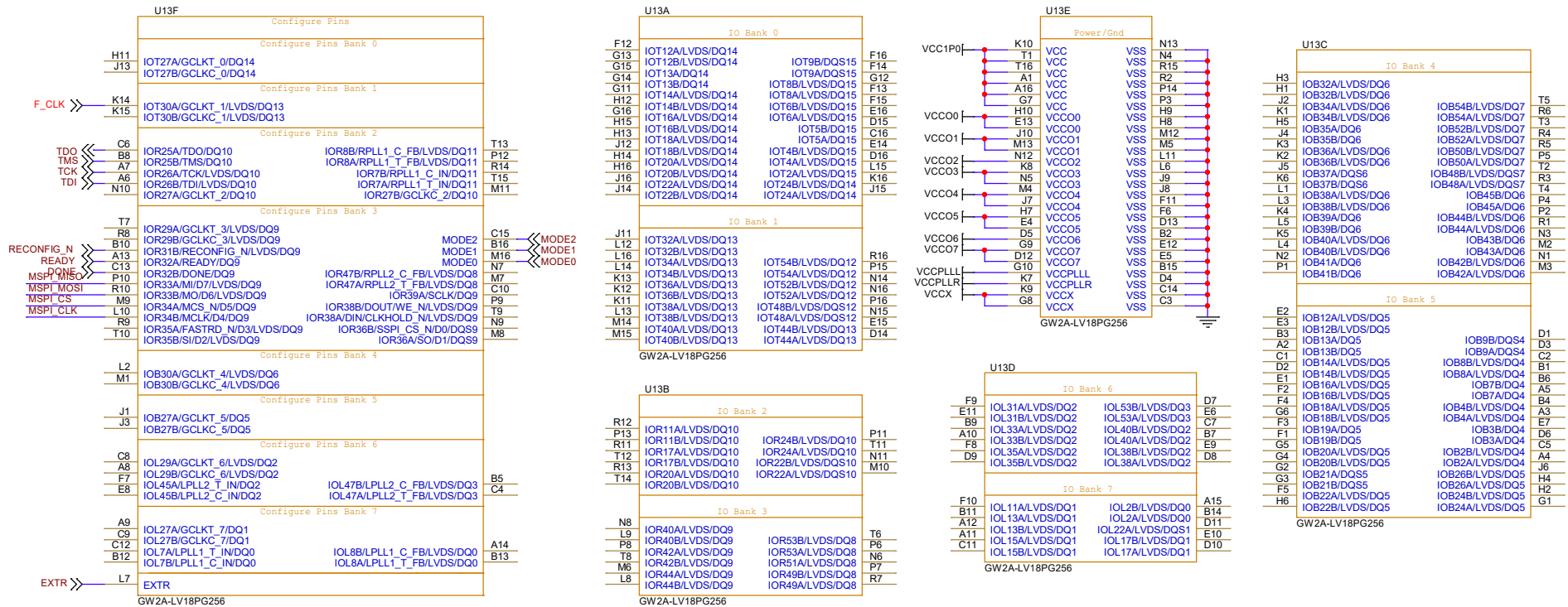
1.F_CLK signal is an external input clock signal.

It is recommended that F_CLK signal be provided through an active oscillator crystal.

2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
Gowin FPGA-AOTOMOTIVE Minimum System Diagram		
Size	Document Number	Rev
A4	GW1NZ-LV1QN48	2.4
Date:	Tuesday, October 31, 2023	Sheet 5 of 10

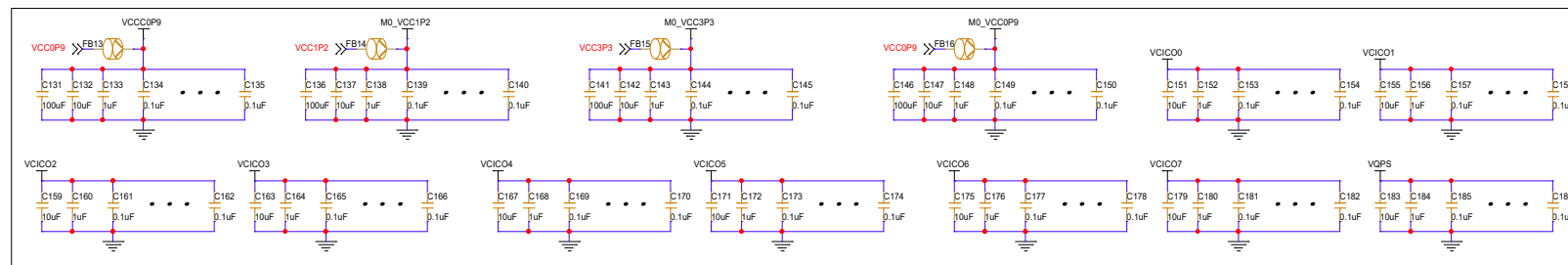
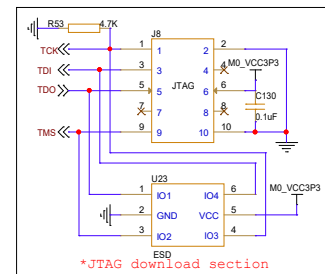
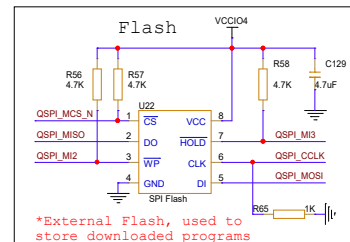
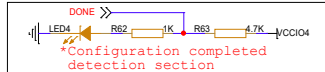
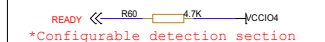
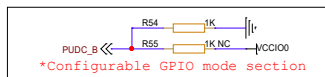
GW2A-LV18PG256



Notes:

1. F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
3. It is recommended that add an ESD protection chip to the JTAG download circuit.

GW5A-LV25PG256

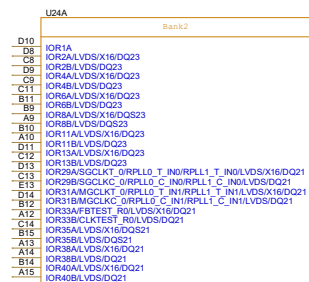


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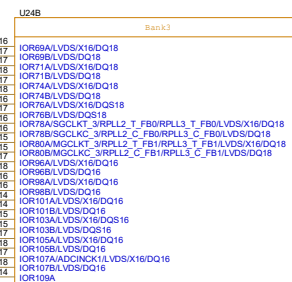
- NOTES:
- 1.F CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
 - 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
 - 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
 - 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
 - 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG704, Arora V
FPGA Product Programming and Configuration Guide.

Title				
GOWIN Minimum System Diagram				
Size C	Document Number GW5A-LV2SPG256			Rev 2
Date:	Tuesday, October 31, 2023	Sheet	8	of 10

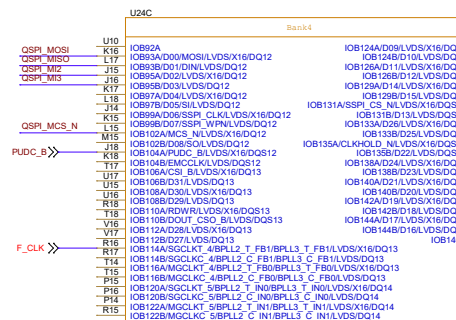
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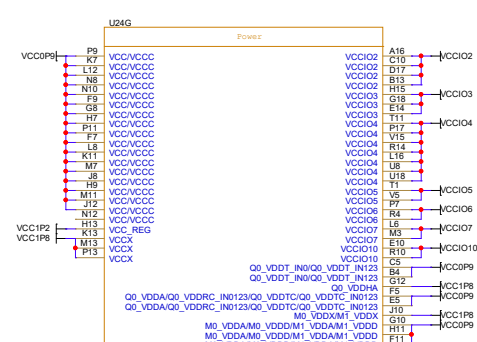
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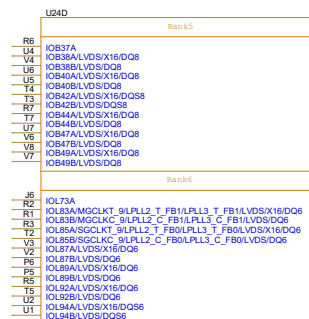
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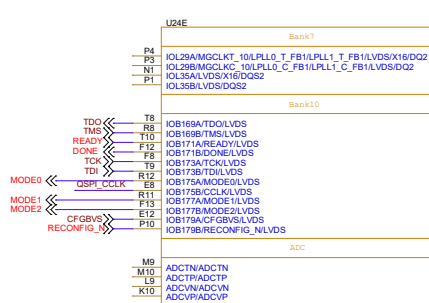
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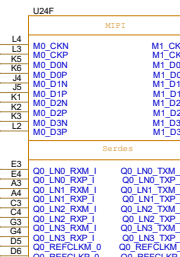
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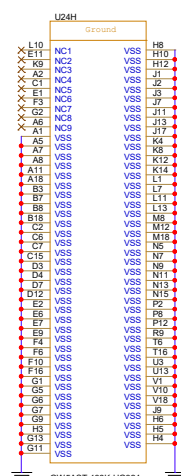
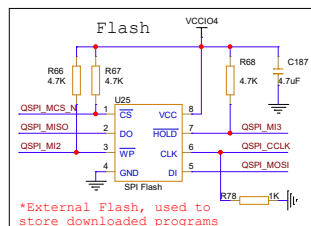
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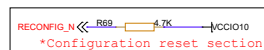
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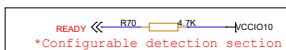
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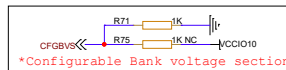
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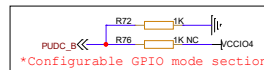
*Configuration reset section



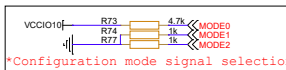
*Configurable detection section



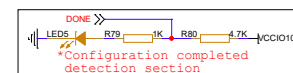
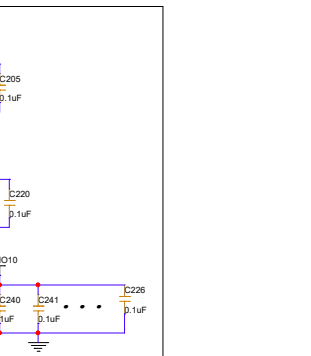
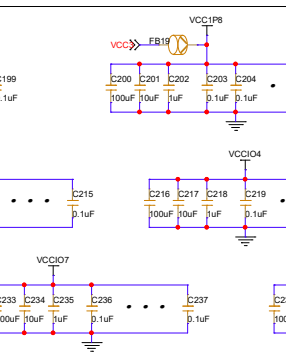
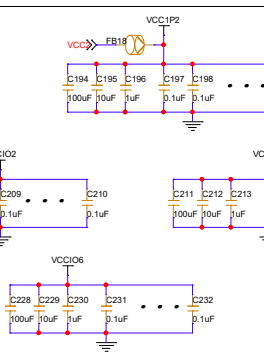
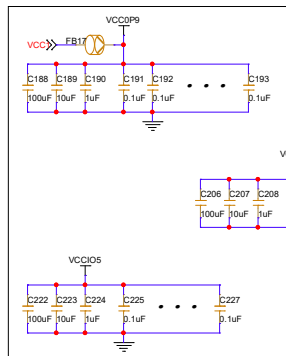
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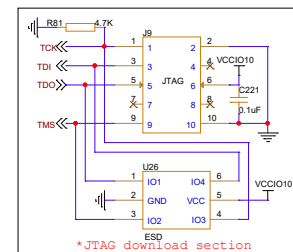
*Configurable GPIO mode section



*Configuration mode signal selectio



*Configuration completed
detection section

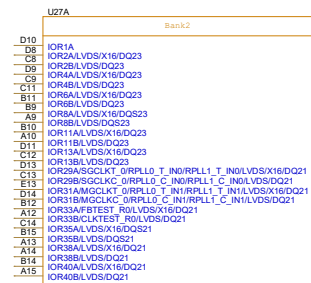


ESD
*ITAG download section

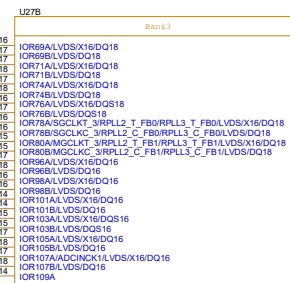
Notes:

- NOTES:
- 1.F CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal.
 - 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
 - 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
 - 4.VCC core voltage requires a large current, so it is recommended to supply power separately.

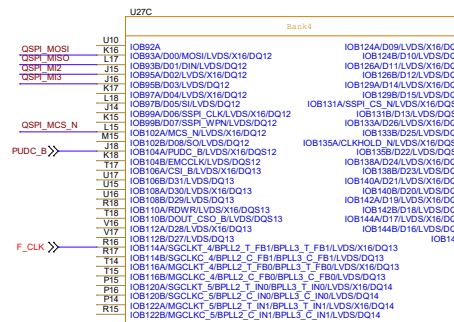
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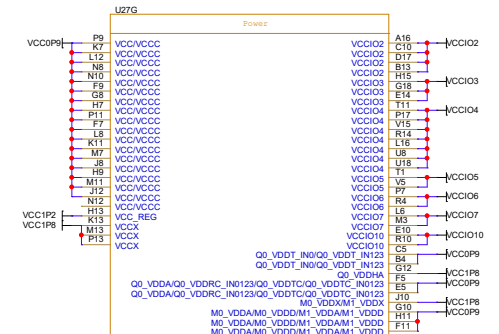
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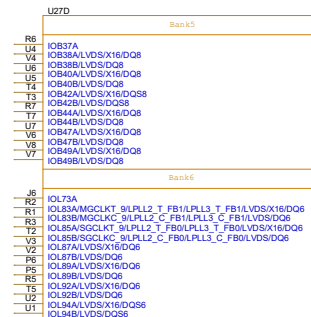
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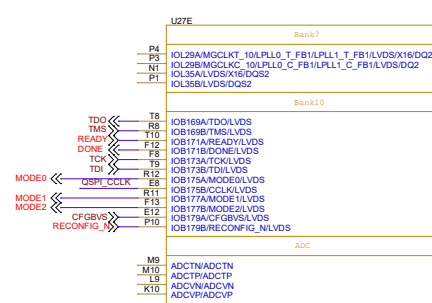
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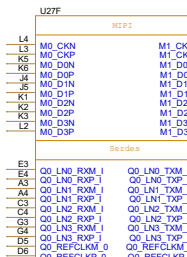
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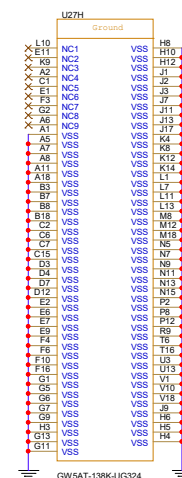
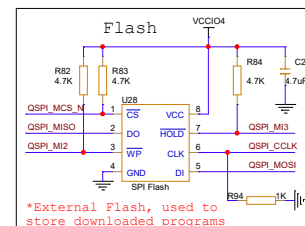
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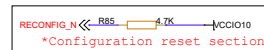
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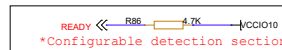
GW5AT-138K-UG3

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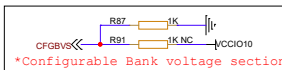
*External Flash, used to store downloaded programs



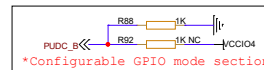
*Configuration reset section



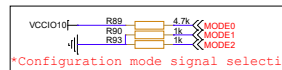
*Configurable detection section



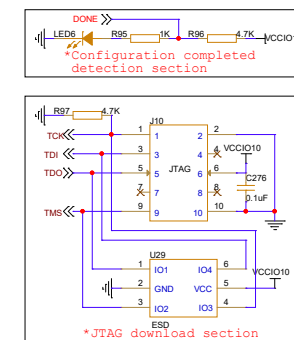
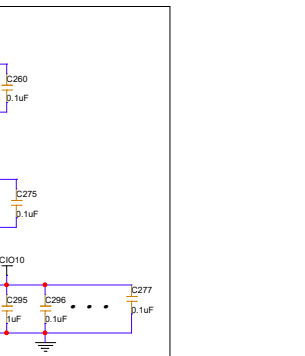
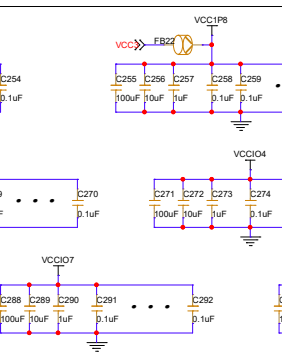
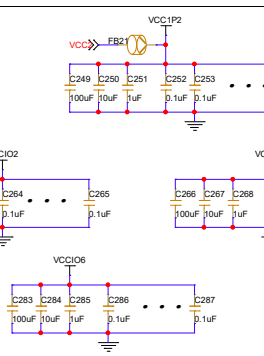
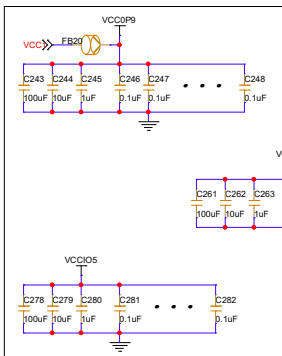
*Configurable Bank voltage section



*Configurable GPIO mode section



*Configuration mode signal selecti



ESD
*.JTAG download section

Notes:

- NOTES:
- 1.F CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal.
 - 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
 - 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
 - 4.VCC core voltage requires a large current, so it is recommended to supply power separately.