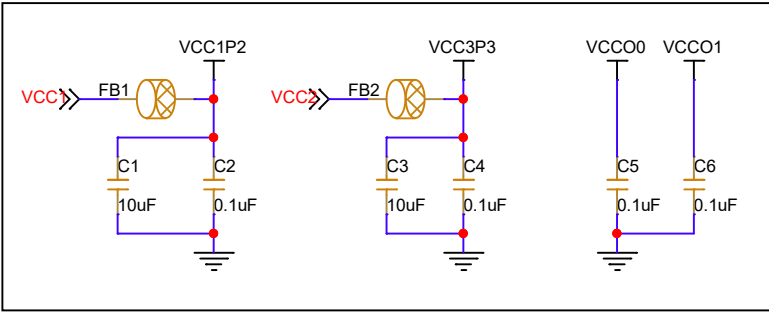
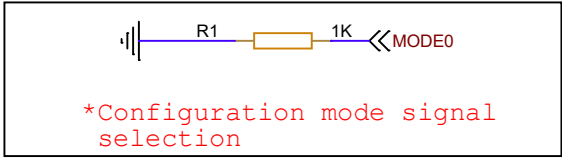
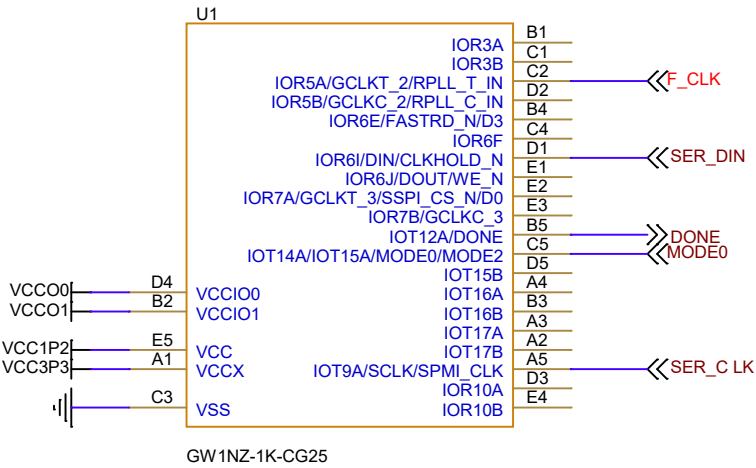


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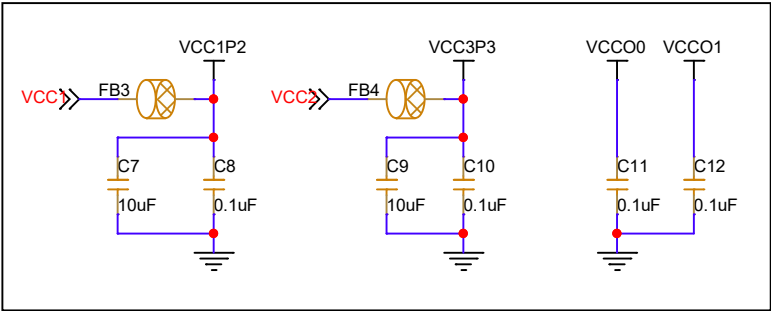
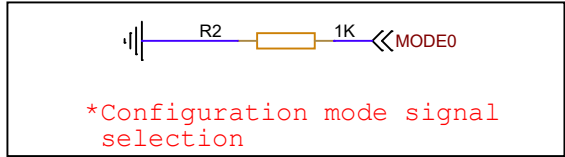
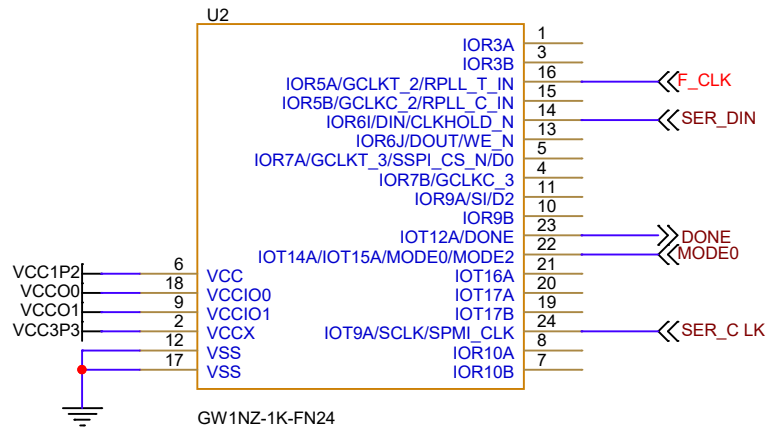
GW1NZ-1K-CG25



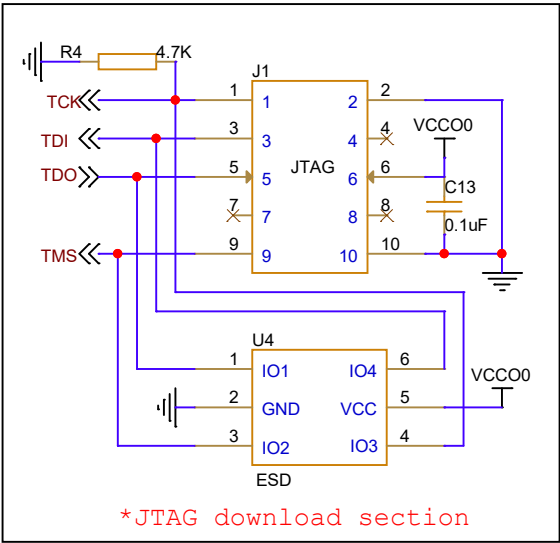
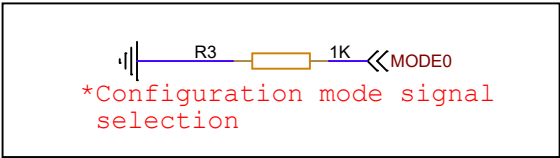
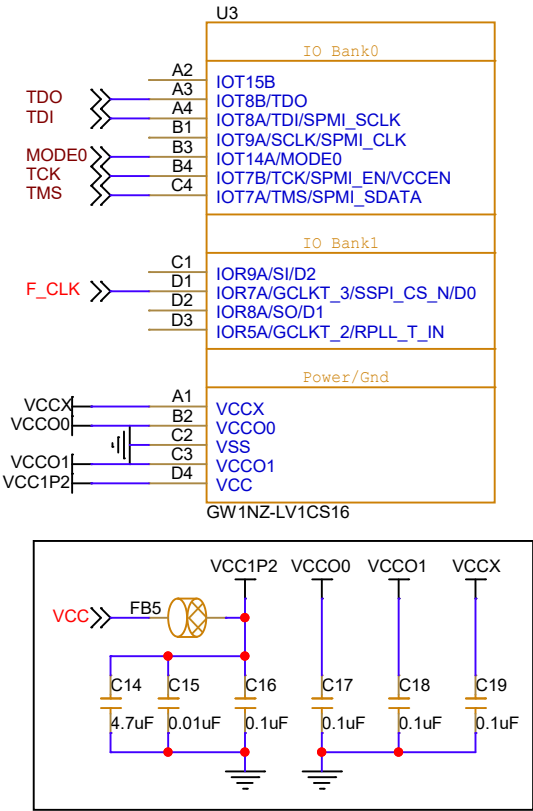
Notes:

1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.

GW1NZ-1K-FN24



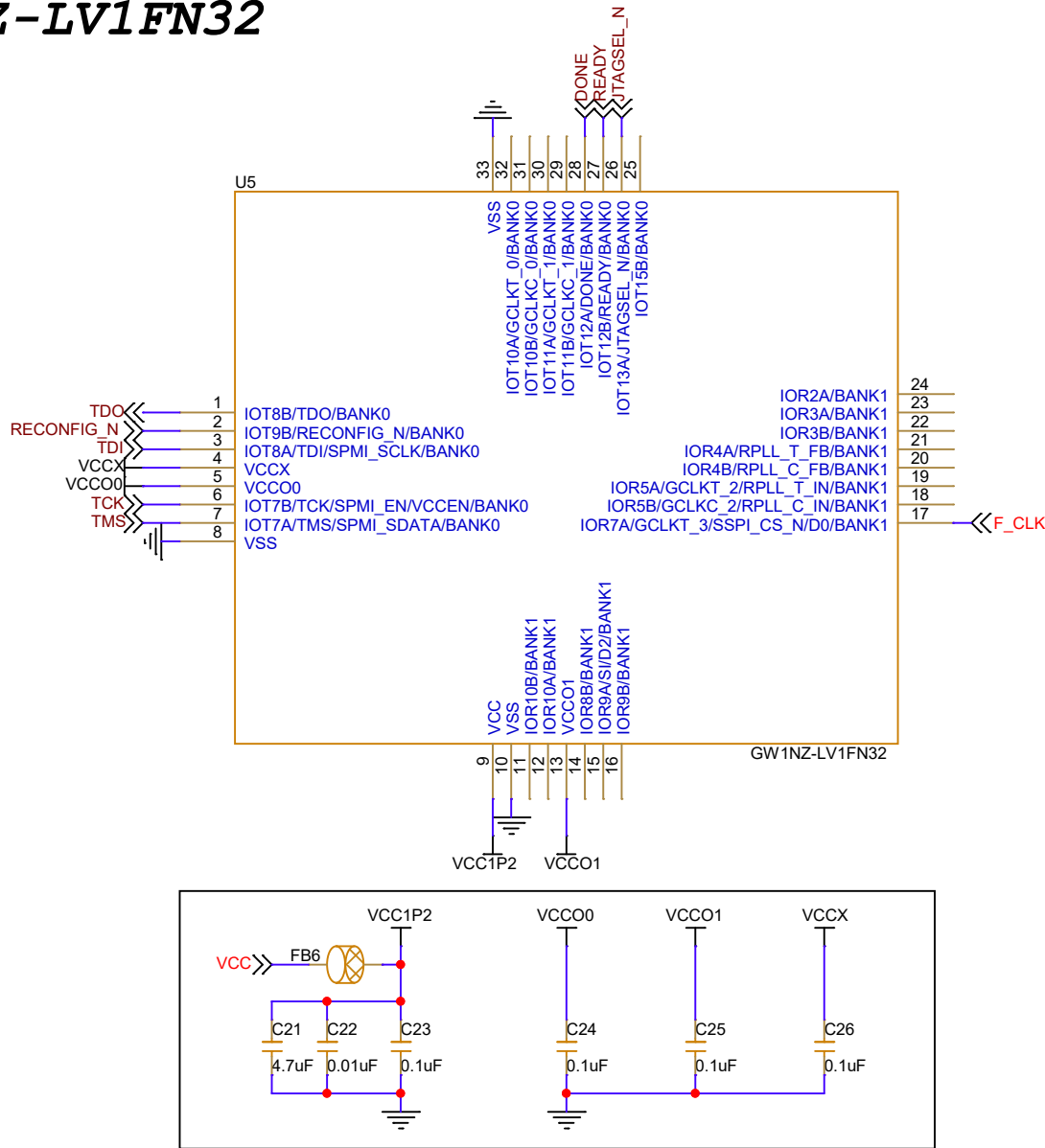
Notes:
1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.



Notes:

- 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

GW1NZ-LV1FN32



Notes:

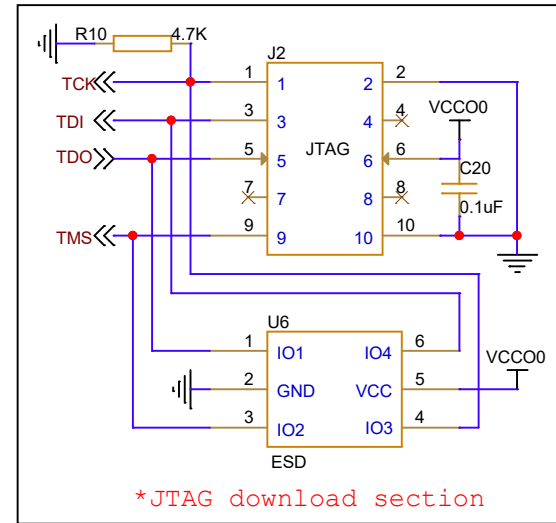
- 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- It is recommended that add an ESD protection chip to the JTAG download circuit.

RECONFIG_N << R5 4.7K VCCO0
*Configuration reset section

READY << R6 4.7K VCCO0
*Configurable detection section

DONE << LED1 R7 1K R8 4.7K VCCO0
*Configuration completed detection section

JTAGSEL_N >> R9 1K
JTAG mode selection signal section



*JTAG download section

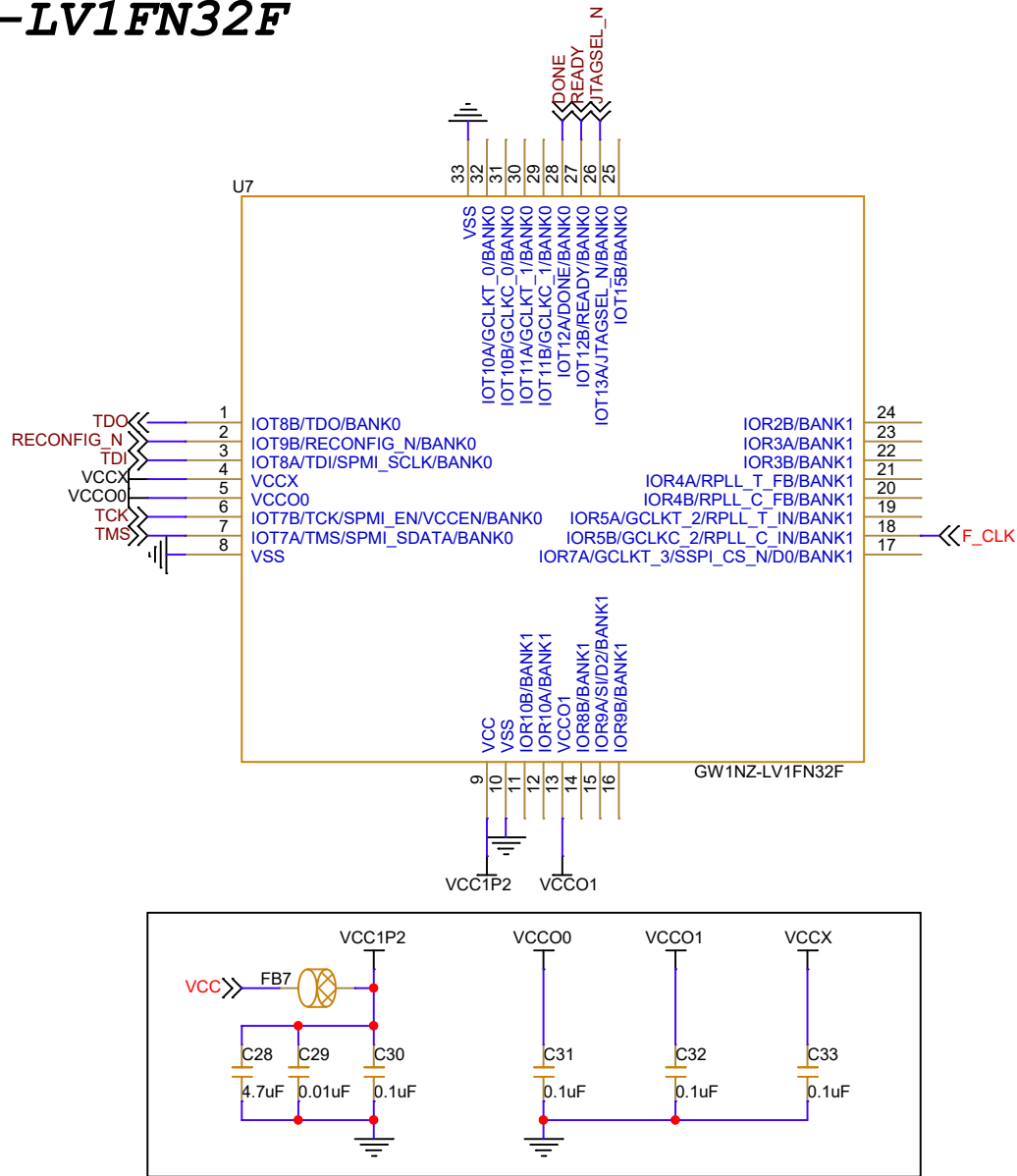
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Notes:

1.F_CLK signal is an external input clock signal.

It is recommended that F_CLK signal be provided through an active oscillator crystal.

2.It is recommended that add an ESD protection chip to the JTAG download circuit.

RECONFIG_N << R11 4.7K VCCO0
*Configuration reset section

READY << R12 4.7K VCCO0
*Configurable detection section

DONE << LED2 R13 1K R14 4.7K VCCO0
*Configuration completed detection section

JTAGSEL_N >> R15 1K
JTAG mode selection signal section

JTAG download section

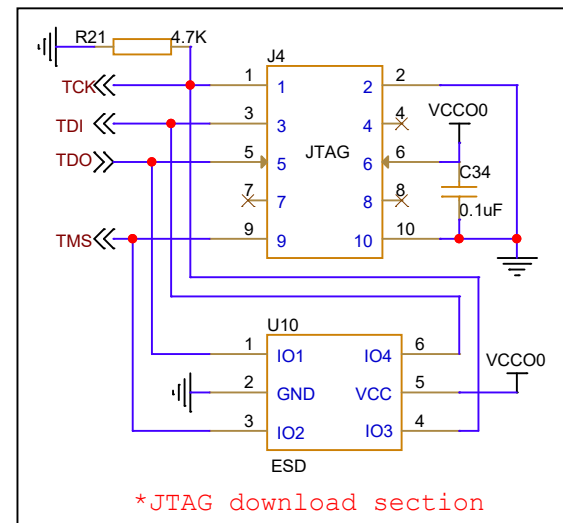
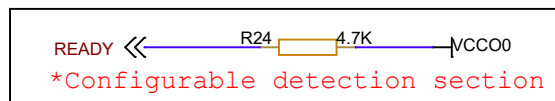
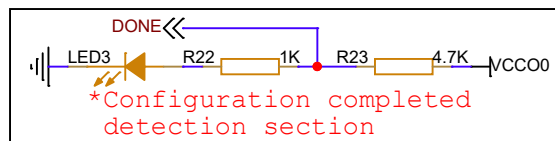
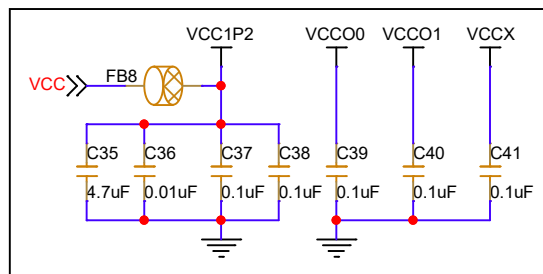
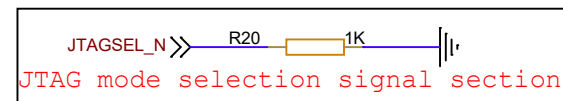
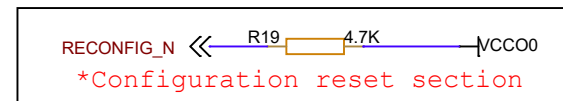
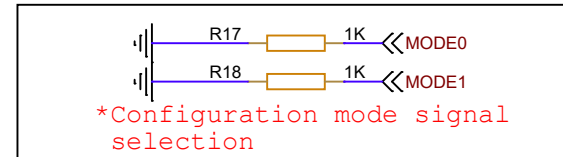
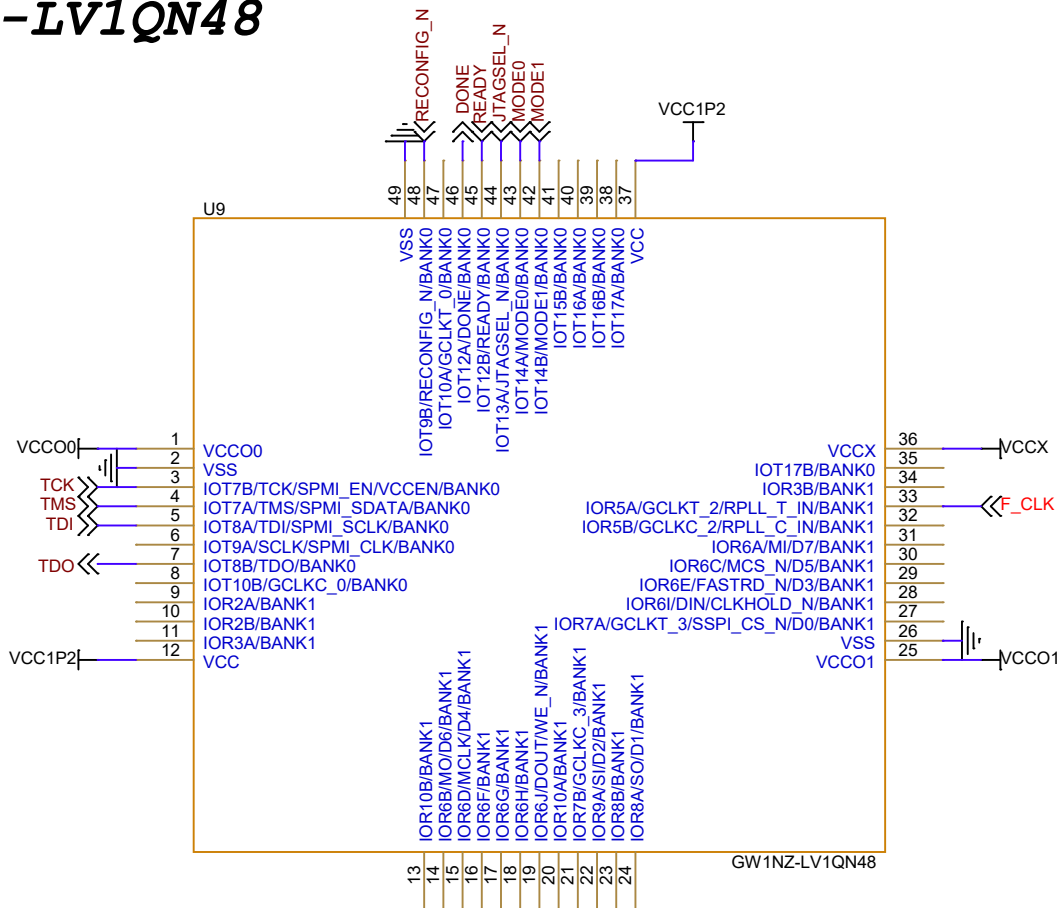
Title
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GW1NZ-LV1QN48



Notes:

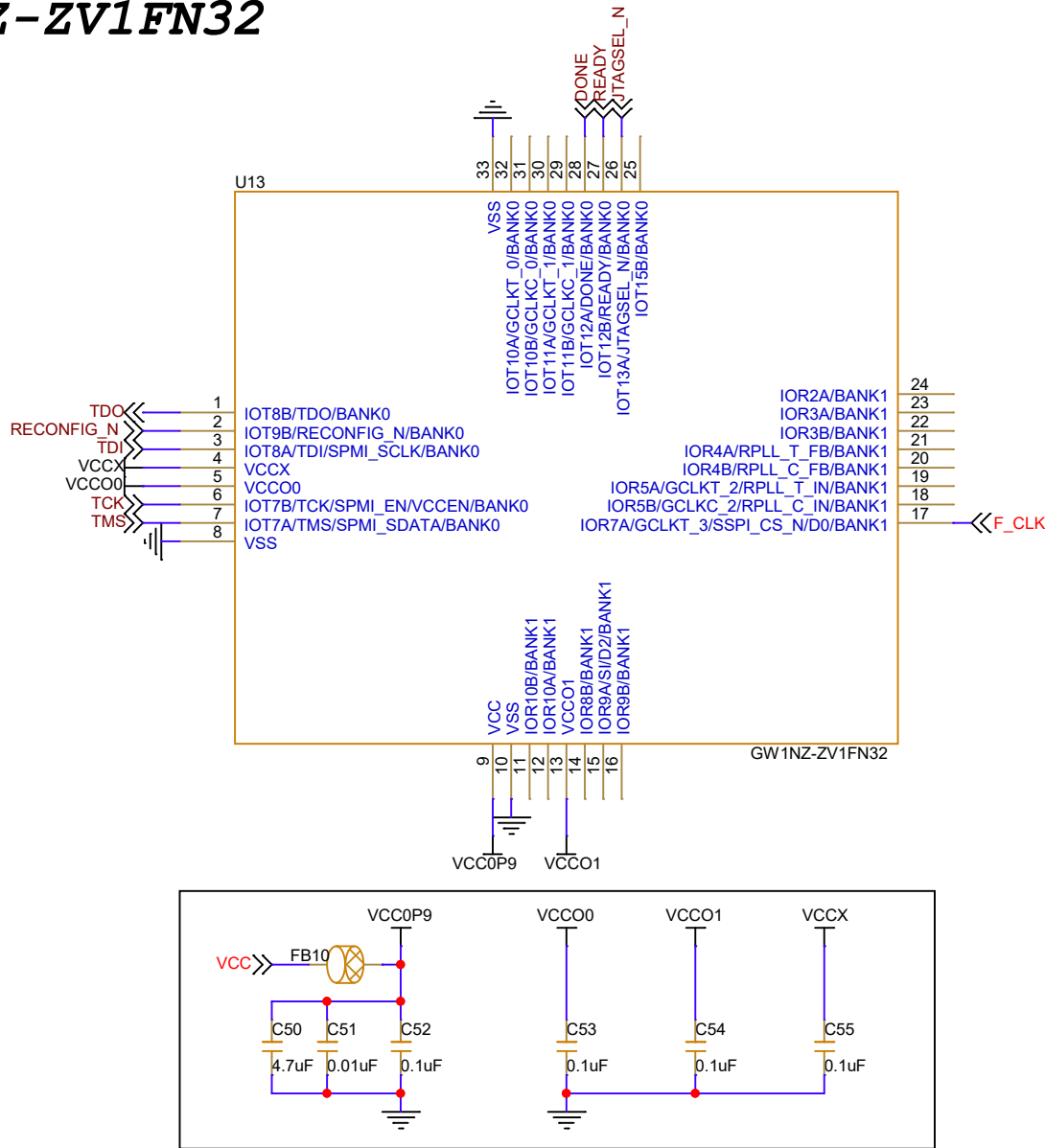
1.F CLK signal is an external input clock signal.

It is recommended that F_CLK signal be provided through an active oscillator crystal.

2.It is recommended that add an ESD protection chip to the JTAG download circuit.

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Notes:

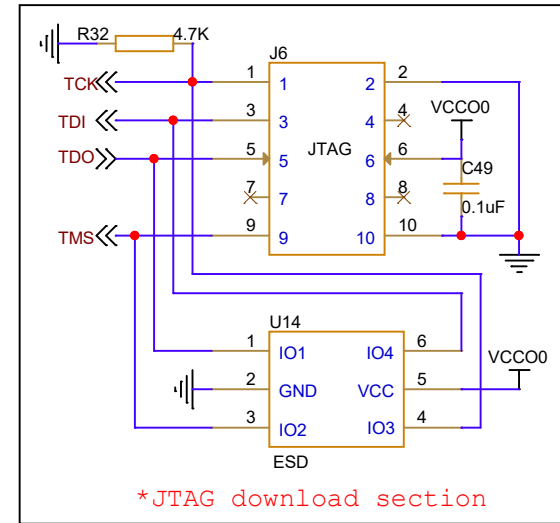
1. F_CLK signal is an external input clock signal. It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.

RECONFIG_N << R27 4.7K VCCO0
*Configuration reset section

READY << R28 4.7K VCCO0
*Configurable detection section

DONE << LED4 R29 1K R30 4.7K VCCO0
*Configuration completed detection section

JTAGSEL_N >> R31 1K
JTAG mode selection signal section



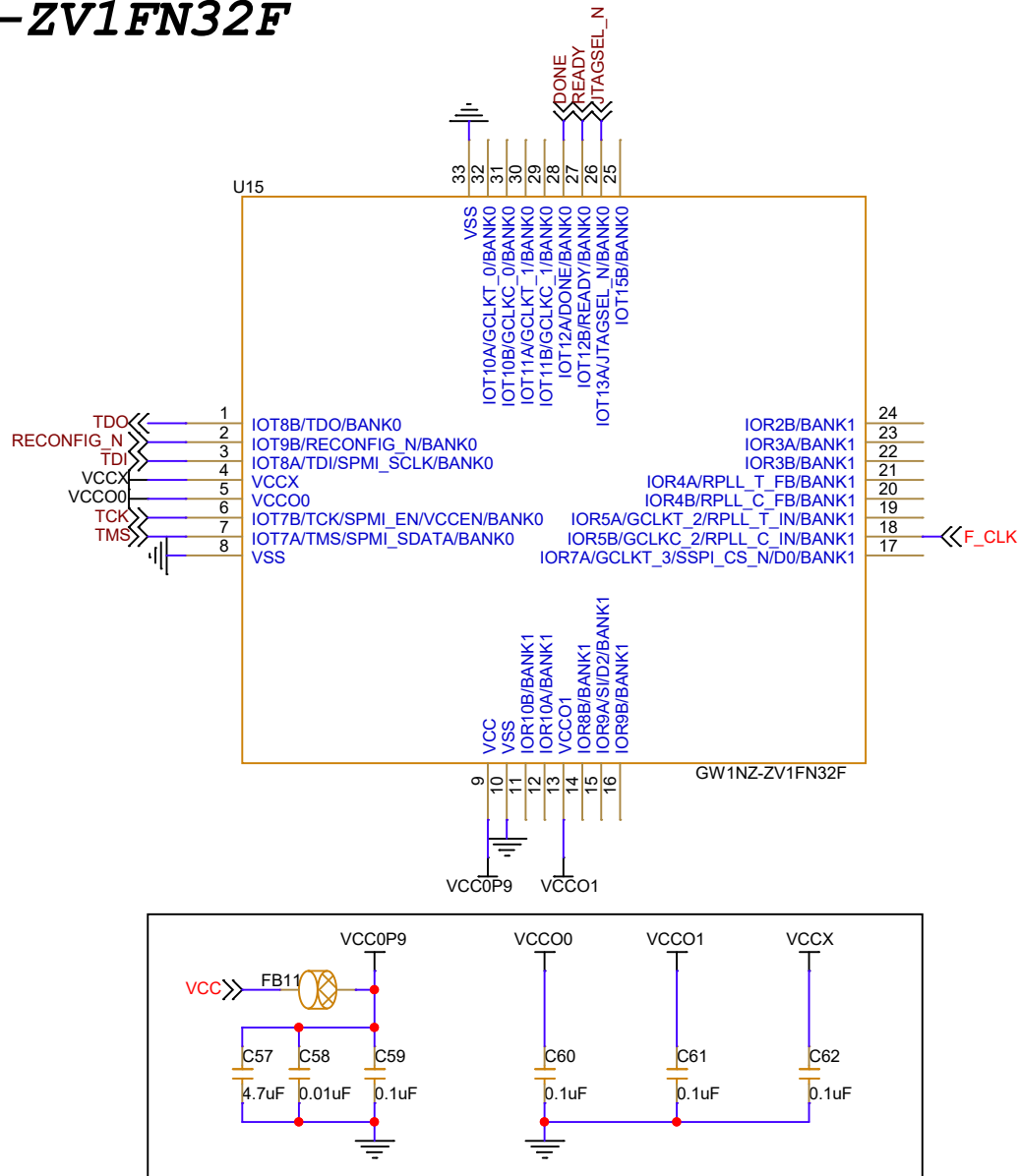
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Notes:

1.F_CLK signal is an external input clock signal.

It is recommended that F_CLK signal be provided through an active oscillator crystal.

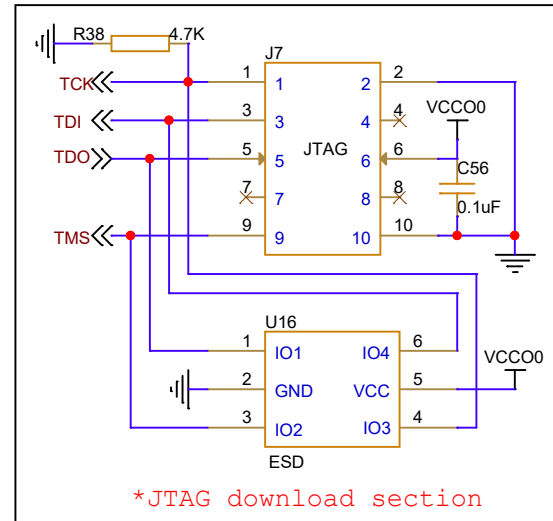
2.It is recommended that add an ESD protection chip to the JTAG download circuit.

RECONFIG_N << R33 4.7K VCCO0
*Configuration reset section

READY << R34 4.7K VCCO0
*Configurable detection section

DONE << LED5 R35 1K R36 4.7K VCCO0
*Configuration completed detection section

JTAGSEL_N >> R37 1K
JTAG mode selection signal section



Title
GOWIN Minimum System Diagram

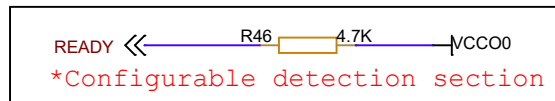
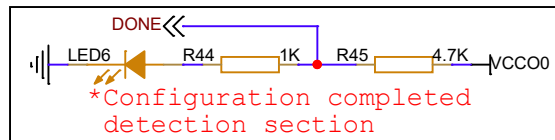
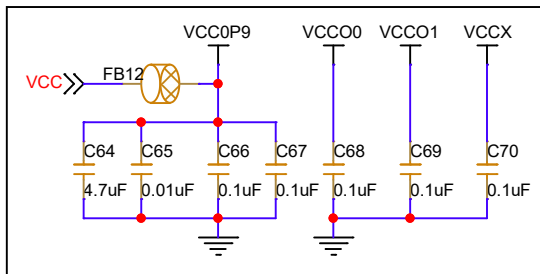
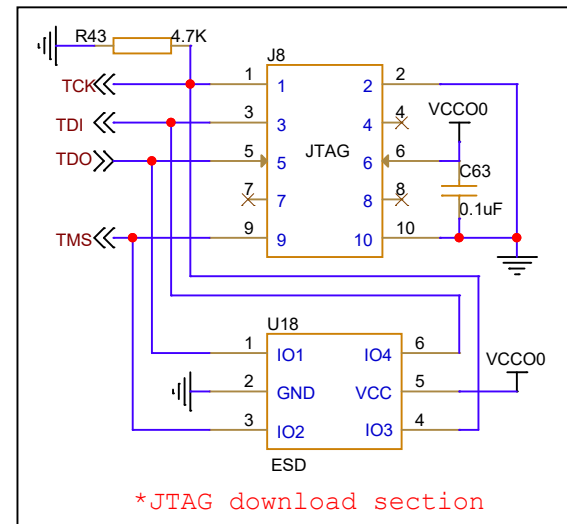
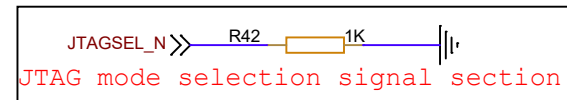
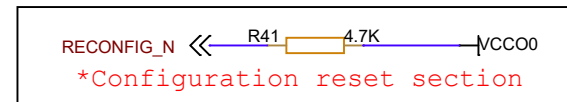
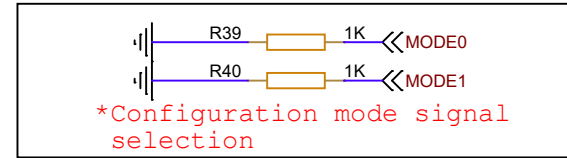
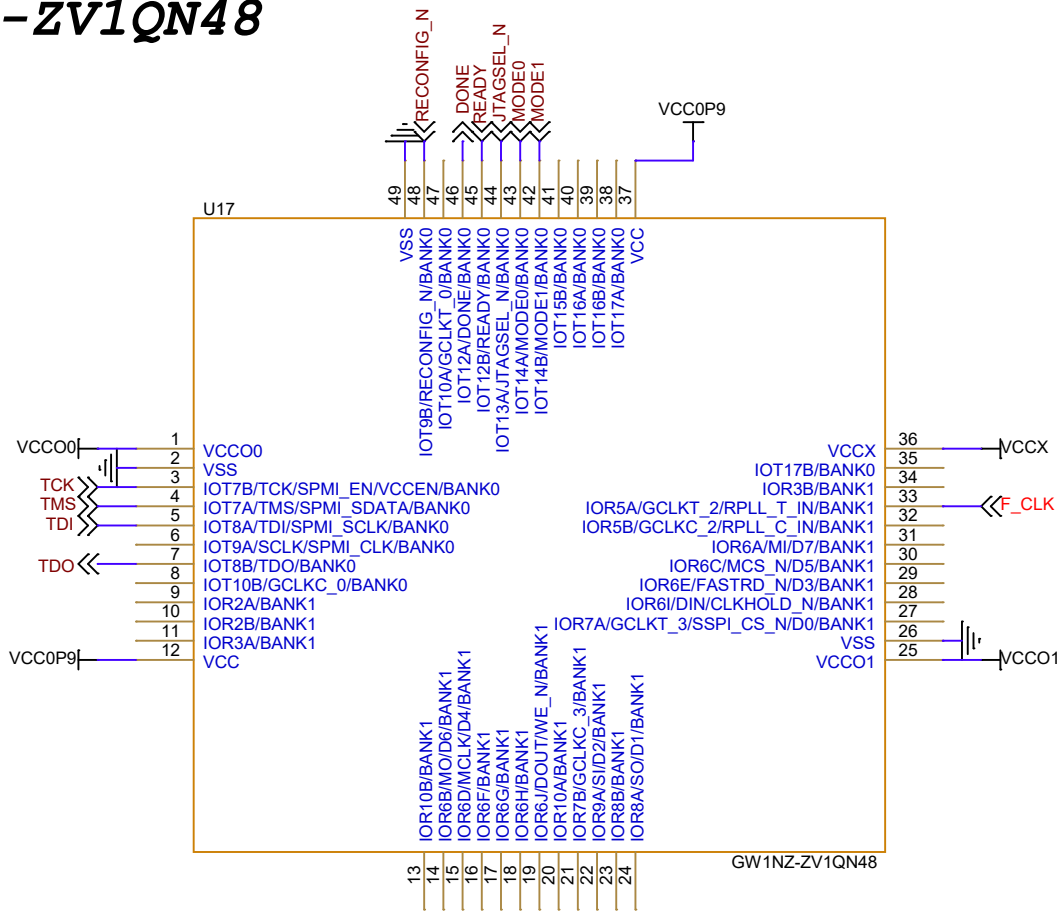
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Notes:

1.F_CLK signal is an external input clock signal.

It is recommended that F_CLK signal be provided through an active oscillator crystal.

2.It is recommended that add an ESD protection chip to the JTAG download circuit.

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