

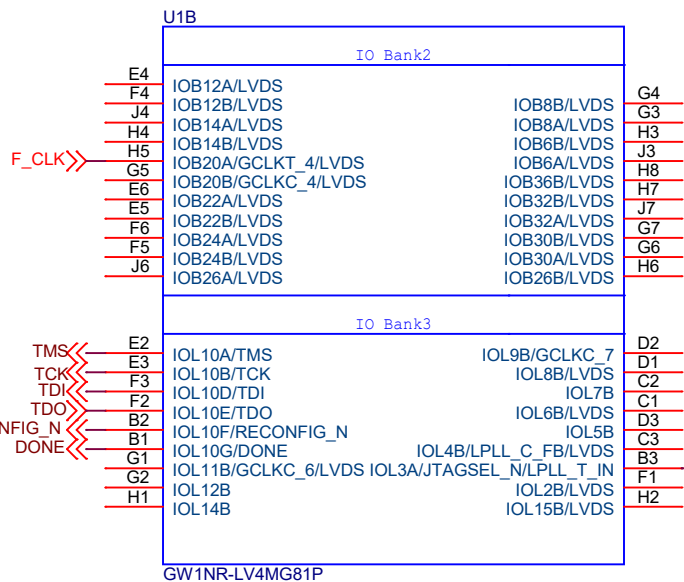
# GW1NR-LV4MG81P

D

C

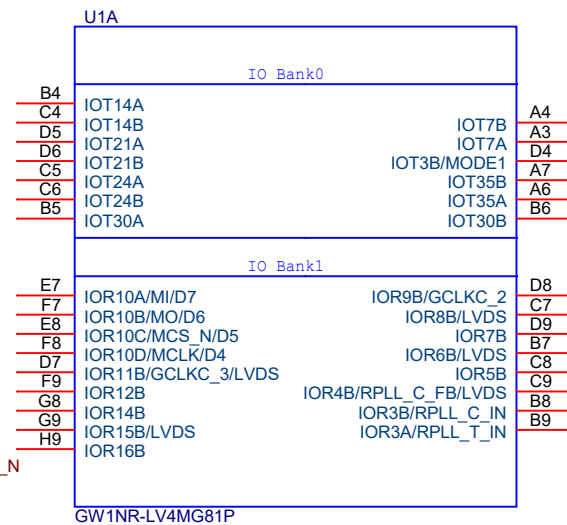
B

A



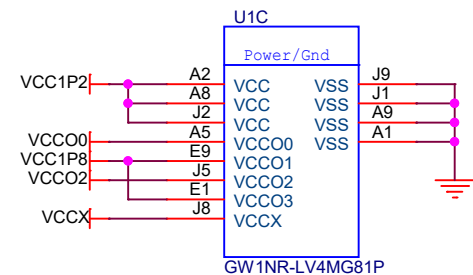
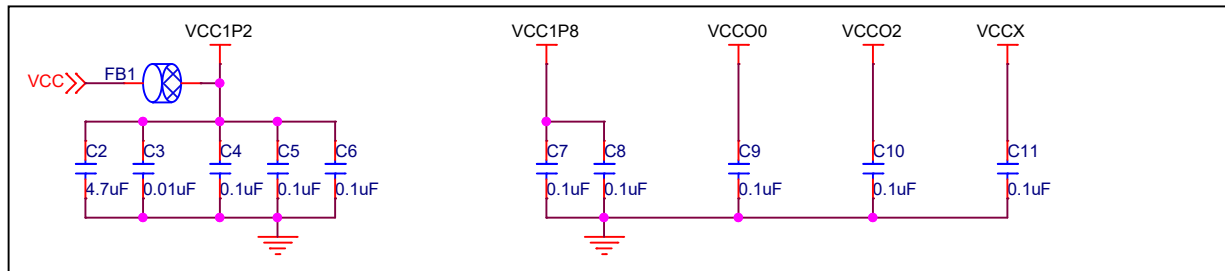
RECONFIG\_N << R3 4.7K VCCO3

\*Configuration reset section



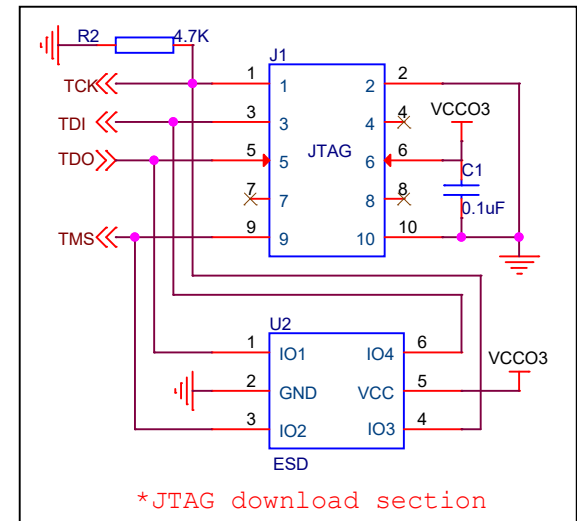
DONE << LED1 R4 1K R5 4.7K VCCO3

\*Configuration completed detection section



JTAGSEL\_N >> R1 1K

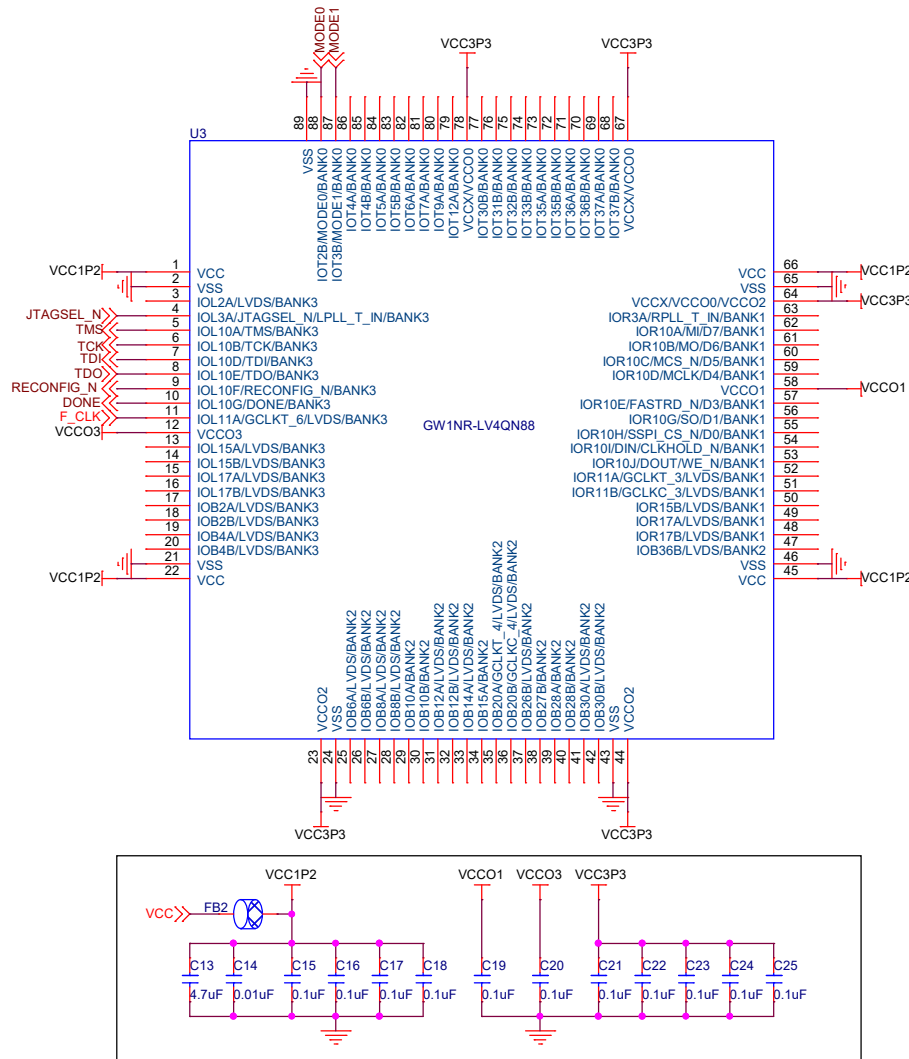
JTAG mode selection signal section



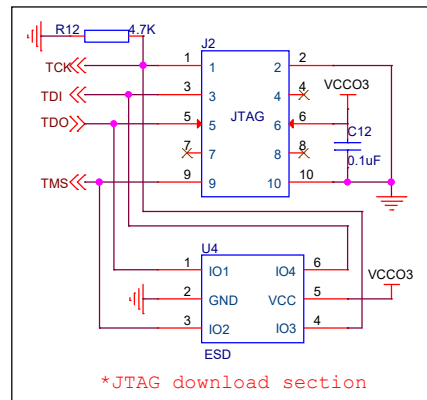
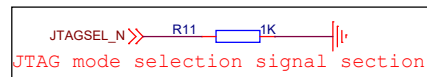
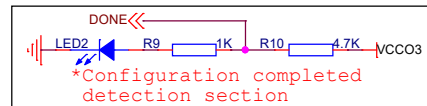
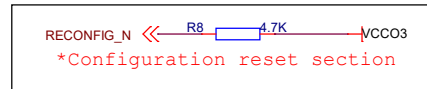
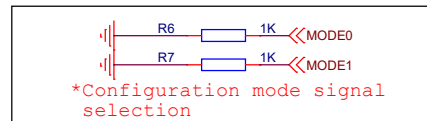
## Notes:

- 1.F\_CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

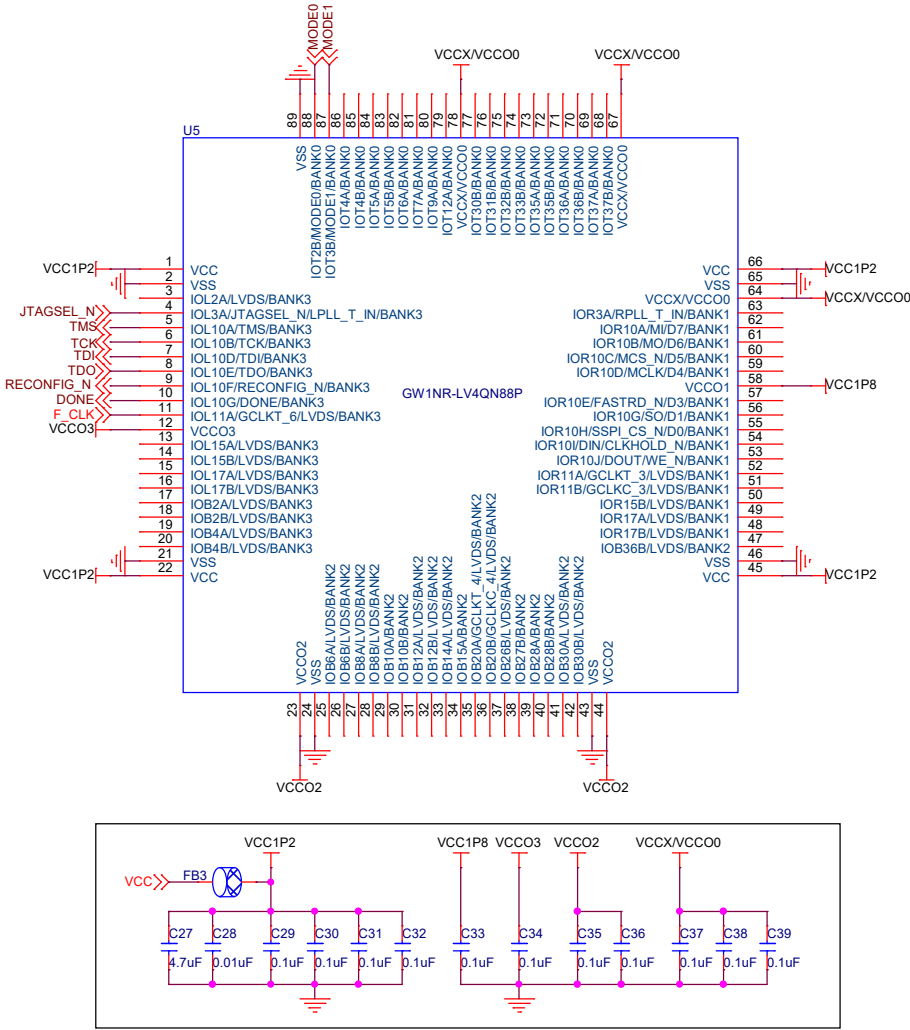
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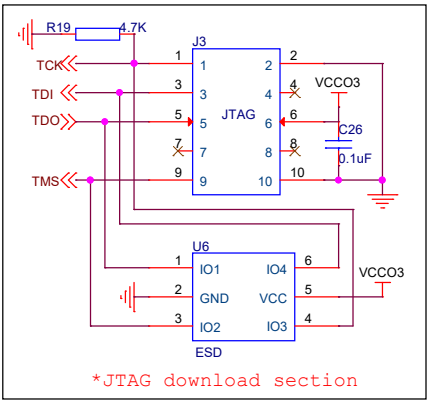
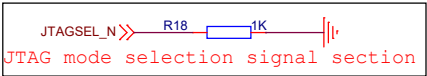
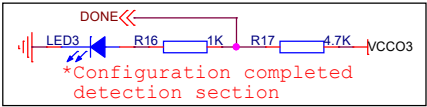
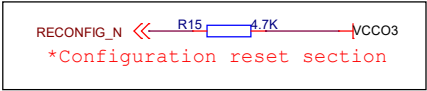
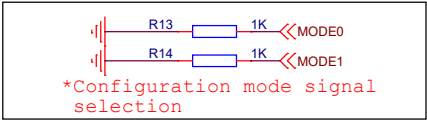
- Notes:
- 1.F CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
  - 2.It is recommended that add an ESD protection chip to the JTAG download circuit.



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- Notes:
- 1.F CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
  - 2.It is recommended that add an ESD protection chip to the JTAG download circuit.



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GOWIN Minimum System Diagram			
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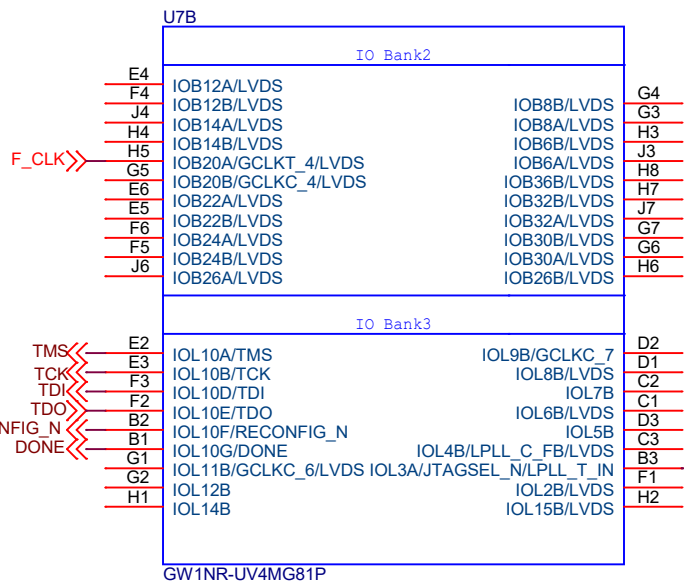
# GW1NR-UV4MG81P

D

C

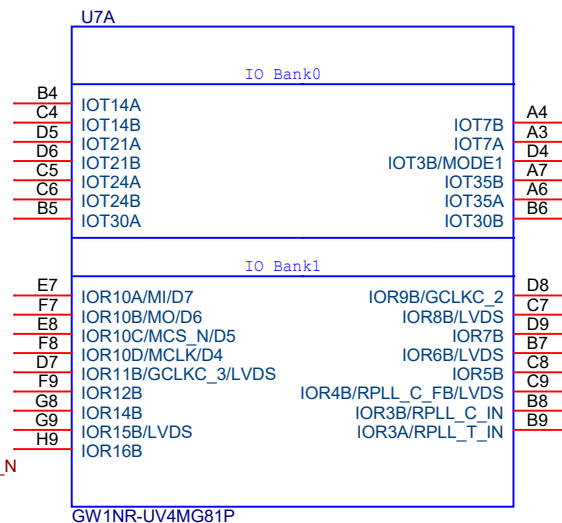
B

A



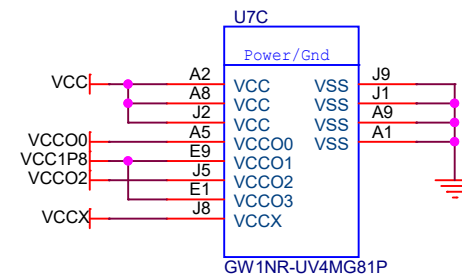
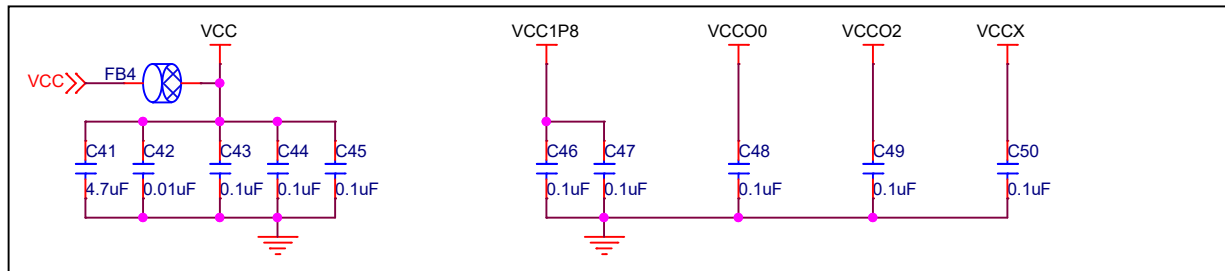
RECONFIG\_N << R22 4.7K VCCO3

\*Configuration reset section



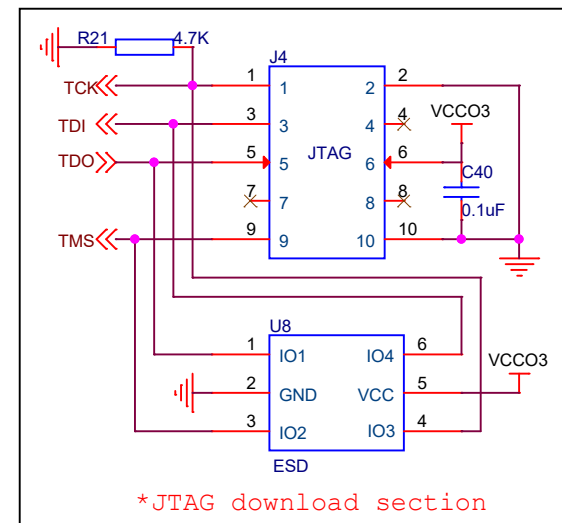
DONE << LED4 R23 1K R24 4.7K VCCO3

\*Configuration completed detection section



JTAGSEL\_N >> R20 1K

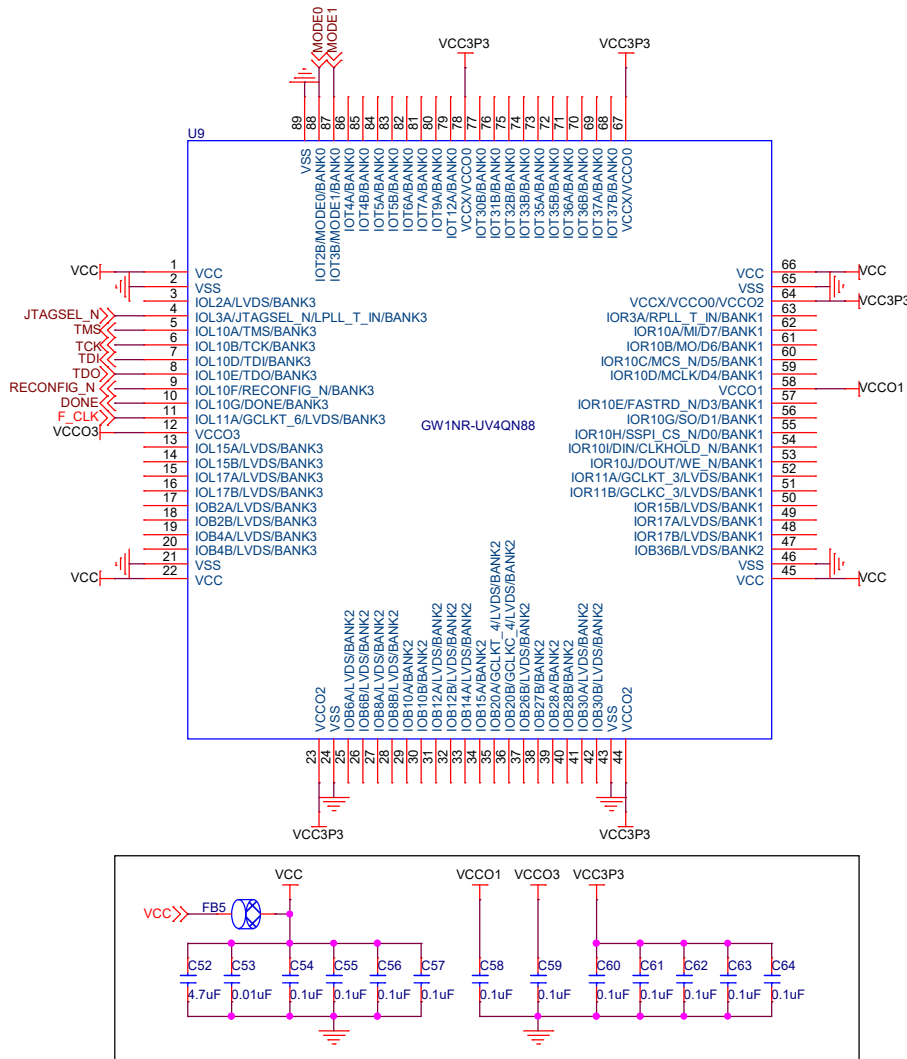
JTAG mode selection signal section



## Notes:

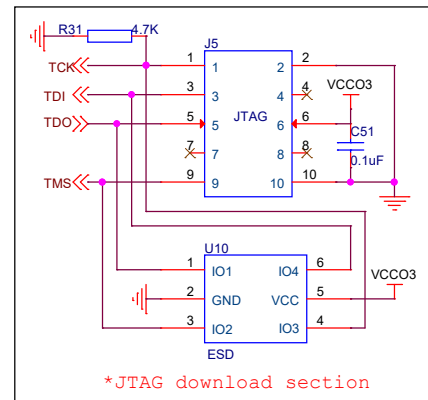
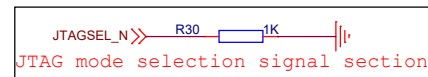
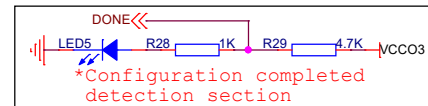
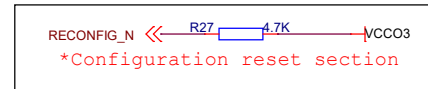
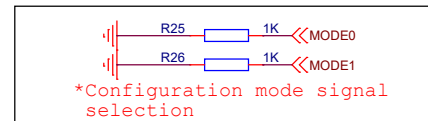
- 1.F\_CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

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GOWIN Minimum System Diagram		
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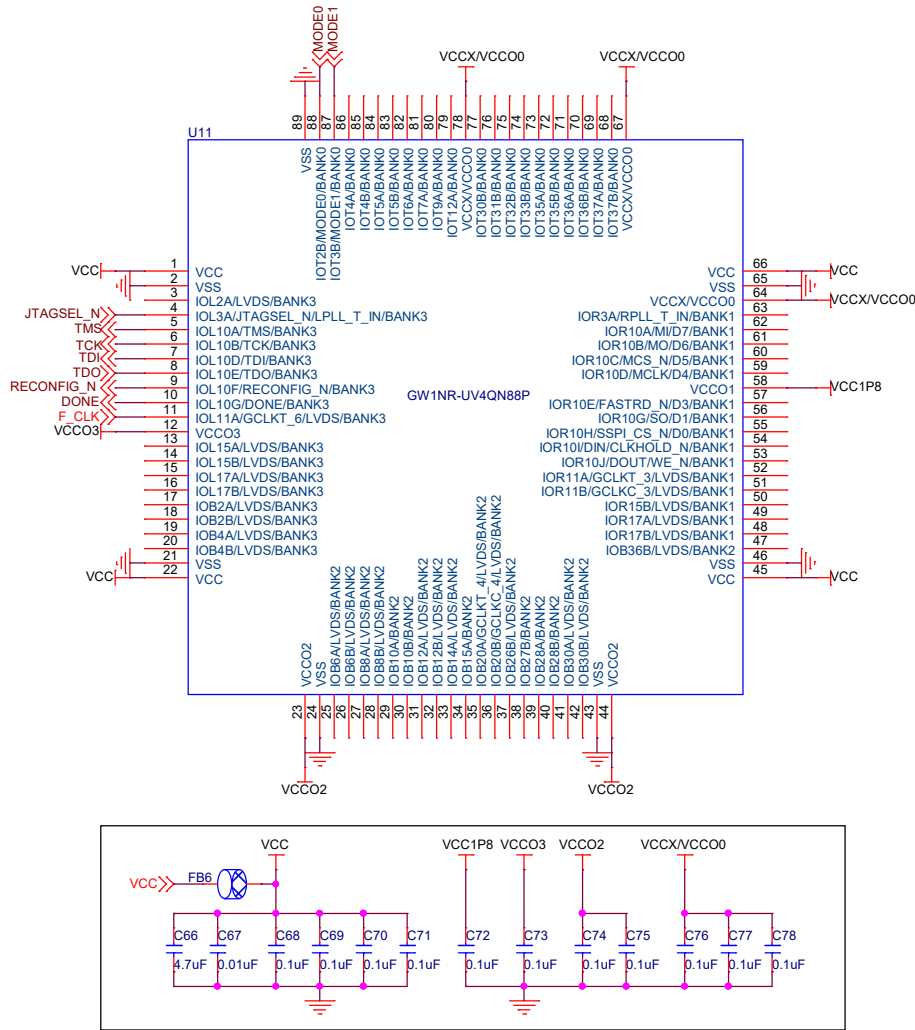


Notes:

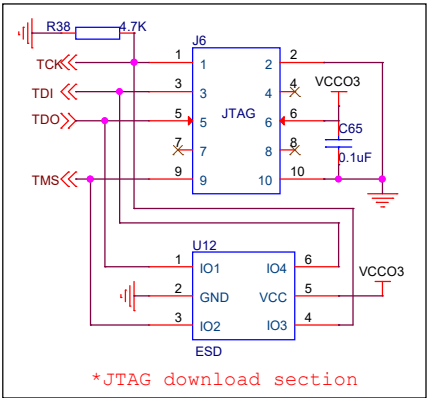
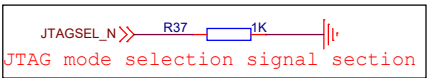
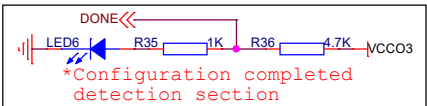
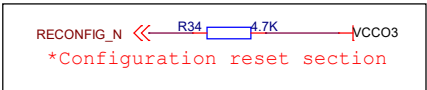
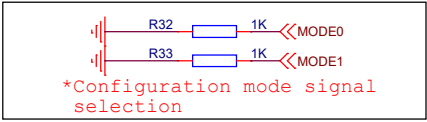
- 1.F CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.



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Notes:  
1.F CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.  
2.It is recommended that add an ESD protection chip to the JTAG download circuit.



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GOWIN Minimum System Diagram			
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