Gowin_EMPU_M1 Hardware Design

Reference Manual

IPUG531-2.4E, 01/17/2025

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Revision History

Date	Version	Description
02/19/2019	1.0E	Initial version published.
07/18/2019	1.1E	MCU hardware design supports extended peripherals: CAN, Ethernet, SPI-Flash, RTC, DualTimer, TRNG, I²C, SPI, SD-Card.
08/18/2019	1.2E	● MCU hardware design and software programming design support extended peripheral: DD3 Memory. ● Fixed known issues of ITCM, DTCM Size and IDE.
09/27/2019	1.3E	● MCU hardware design and software programming design support read, write and erasure of SPI-Flash. ● MCU software programming design supports a continuous multi-byte read and write of I²C. ● Fixed known issues of address mapping of AHB2 and APB2 extended interface in MCU software programming design. ● Fixed known issues of continuous read and write of DDR3 Memory in MCU software programming design.
12/06/2019	1.4E	● MCU hardware design and software programming design supports PSRAM. ● Updated MCU compiling software GMD V1.0. ● RTOS reference design updated. ● Hardware and software reference design of AHB2 and APB2 extension bus interface added.
03/03/2020	1.5E	● MCU hardware design supports read and write of SPI-Card. ● Fixed known issues of data read and write of DDR when "synplify Pro" synthesizes. ● The FPGA devices of GW2A-18C/GW2AR-18C/GW2A-55C supported.
06/12/2020	1.6E	● MCU supports External instruction memory. ● MCU supports External data memory. ● 6 AHB bus interfaces extended. ● 16 APB bus interfaces extended. ● GPIO supports multiple interface types. ● I²C supports multiple interface types.
01/25/2021	1.7E	● Fixed known issues of SPI-Flash initialization. ● The reference design of GW1N-9C, GW2A-18C, GW2A-55C (Version C) updated. ● The reference design of version Gowin Software updated. ● The reference supports of external interrupt signal added.
07/21/2021	1.8E	● GW1N-9C/GW1NR-9C supports embedded UserFlash as instruction memory. ● Known issues of read and write for SPI full-duplex fixed. ● The reference design of SynplifyPro deleted. ● The reference design and the version of Gowin Software updated.
10/12/2021	1.9E	● ITCM and DTCM size of GW2AN-9X/GW2AN-18X modified. ● GW2AN-9X/GW2AN-18X does not support external DDR3. ● DK-START-GW2AR18 V1.1 development board reference design updated.

Date	Version	Description
		● Non-BlockRAM ITCM/DTCM solution added.
05/11/2023	2.0E	● Extended external interrupt inputs supported. ● Arora V FPGA products supported. ● Hardware reference design updated. ● External instruction memory and data memory solutions added. ● Extended external interrupt input solutions added. ● Arora V external instruction memory solutions added.
07/21/2023	2.1E	● GW5AT-138 and GW5A-25 system performance statistics added. ● Hardware target GW5A-25 added. ● GW5A-25 reference design added. ● Tested software version updated. ● Arora V integrated and Arora V solution removed.
03/07/2024	2.2E	● Ethernet, DDR3 Memory, and PSRAM Memory peripheral modules updated. ● GW5A/S/R/T-138 Version B/75 Version B/25 Version A devices support DDR3 Memory and Ethernet peripherals. ● GW5AT-60 Version A devices supported.
06/28/2024	2.3E	● GW5ART-15 Version A devices supported. ● Hardware reference design updated.
01/17/2025	2.4E	● Functions of CAN, Ethernet, DDR3, and PSRAM peripherals updated. ● GW5A/T-60 and GW5AT/RT-15 devices support DDR3 peripheral. ● Hardware reference design updated.

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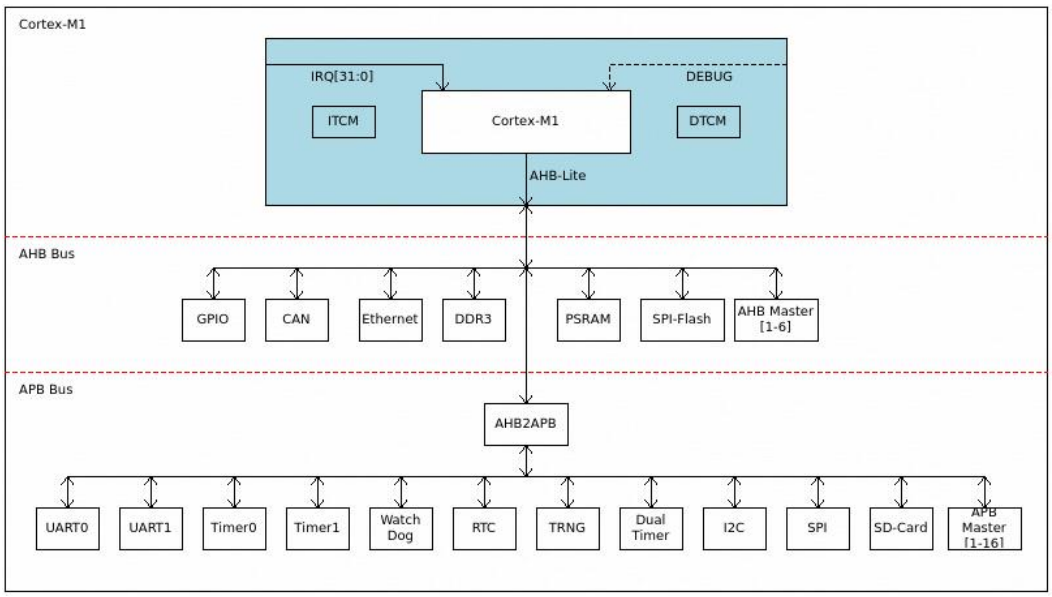
1 Hardware Architecture

1.1 System Architecture

Gowin_EMPU_M1 architecture consists of three levels, as shown in Figure 1-1.

Figure 1-1 System Architecture



First level: Cortex-M1 core, ITCM, and DTCM

Second level: AHB bus, GPIO, CAN, Ethernet, DDR3 Memory, PSRAM Memory, SPI-Flash Memory, and AHB Master [1-6].

Third level: APB bus, UART0, UART1, Timer0, Timer1, Watch Dog, RTC, TRNG, DualTimer, I^2C Master, SPI Master, SD-Card and APB Master [1-16].

1.2 System Feature

Gowin_EMPU_M1 includes two sub-systems:

- Cortex-M1 core system
- Bus peripheral system

1.2.1 Cortex-M1 Core System

Processor Core

- ARM architecture v6-M Thumb, the instruction set architecture, supports 16-bit Thumb and 32-bit Thumb2 instruction set
- Configurable extension operation system
- System exception handling
- Interrupt exception handling and normal thread model
- One stack pointer for normal operation system and two stack pointers for extension operation system
- Big/Little-endian format
  - Configurable Big/Little-endian format
  - Little-endian format for instructions and system control register
  - Little-endian format for debugging system

NVIC

- External interrupts can be configured: 1, 8, 16, 32
- Four priority levels
- Extends 4 external interrupt inputs for users to extend peripherals
- Saves processor status automatically during interrupts handling and recovers automatically at the end of interrupt handling

Debug System

Control the debugging system through configuration options.

- If you turn off the debugging system, Cortex-M1 core will not support it.
- If you turn on the debugging system, Cortex-M1 core will support it.
  - Full mode and reduced mode can be configured
    a) Full mode: Four BreakPoint Units and two Data Watchpoints;
    b) Reduced mode: Two BreakPoint Units and one Data Watchpoints;
  - Configurable DAP ports
    a) JTAG/Serial Wire
    b) JTAG
    c) Serial Wire

Memory

- ITCM: instruction memory
  - You can select internal instruction memory or external instruction memory
  - You can configure the Size of internal instruction memory as 1/2/4/8/16/32/64/128/256/512KB

  - You can configure the initial value of internal instruction memory
- DTCM: data memory
  - You can select internal data memory or external data memory
  - You can configure the Size of internal data memory as 1/2/4/8/16/32/64/128/256/512KB

32 Bits Hardware Multiplier

- Normal mode
- Small mode

1.2.2 Bus Peripheral System

- AHB bus, GPIO, CAN, Ethernet, DDR3 Memory, PSRAM Memory, SPI-Flash Memory, and AHB Master [1-6].
- APB bus, UART0, UART1, Timer0, Timer1, Watch Dog, RTC, TRNG, DualTimer, I^2C Master, SPI Master, SD-Card and APB Master [1-16].

1.3 System Ports

The definition of Gowin_EMPU_M1 Ports is as shown in Table 1-1.

Table 1-1 System Ports Definition

Name	I/O	Data Width	Description	Module
HCLK	in	1	System Clock	–
hwRstn	in	1	System Reset	–
LOCKUP	out	1	Core Lockup State	–
HALTED	out	1	Core Halt Debug State	Debug
JTAG_3	inout	1	TRST	Debug JTAG and Serial Wire
JTAG_4	inout	1	GND	
JTAG_5	inout	1	TDI	
JTAG_6	inout	1	GND	
JTAG_7	inout	1	TMS/SWDIO	
JTAG_8	inout	1	GND	
JTAG_9	inout	1	TCK/SWDCLK	
JTAG_10	inout	1	GND	
JTAG_11	inout	1	RTCK	
JTAG_12	inout	1	GND	
JTAG_13	inout	1	TDO/SWO	
JTAG_14	inout	1	GND	
JTAG_15	inout	1	RESET	
JTAG_16	inout	1	GND	
JTAG_17	inout	1	NC	
JTAG_18	inout	1	GND	
EXTINT	in	[3:0]	Extended external interrupt	NVIC

Name	I/O	Data Width	Description	Module
			input	
GPIO	inout	[15:0]	GPIO I/O	GPIO I/O
GPIOIN	in	[15:0]	GPIO input	GPIO non-I/O
GPIOOUT	out	[15:0]	GPIO output	
GPIOOUTEN	out	[15:0]	GPIO output enable	
UART0RXD	in	1	UART0 receive	UART0
UART0TXD	out	1	UART0 transmit	
UART1RXD	in	1	UART1 receive	UART1
UART1TXD	out	1	UART1 transmit	
TIMER0EXTIN	in	1	Timer0 external interrupt	Timer0
TIMER1EXTIN	in	1	Timer1 external interrupt	Timer1
RTCSRCCLK	in	1	RTC clock source: 32.768KHz	RTC
SCL	inout	1	Serial Clock	I^2C I/O
SDA	inout	1	Serial data	
SCLIN	in	1	Serial clock input	I^2C non-I/O
SCLOUT	out	1	Serial clock output	
SCLOUTEN	out	1	Serial clock output enable	
SDAIN	in	1	Serial clock input	
SDAOUT	out	1	Serial clock output	
SDAOUTEN	out	1	Serial clock output enable	
MOSI	out	1	Master output/Slave input	SPI
MISO	in	1	Master input/Slave output	
SCLK	out	1	Clock signal	
NSS	out	1	Slave select signal	
SD_SPICLK	in	1	SPI clock signal	SD-Card
SD_CLK	out	1	SD clock signal	
SD_CS	out	1	Chip select signal	
SD_DATAIN	in	1	Data input	
SD_DATAOUT	out	1	Data output	
SD_CARD_INIT	out	1	Initialization "0"	
SD_CHECKIN	in	1	Input check	
SD_CHECKOUT	out	1	Output check	
CAN_RX	in	1	Data input	CAN
CAN_TX	out	1	Data output	
RGMII_TXC	out	1	RGMII transmitting clock	Ethernet RGMII Interface
RGMII_TX_CTL	out	1	RGMII transmitting control	
RGMII_TXD	out	[3:0]	RGMII transmitting data	
RGMII_TXD	in	1	RGMII receiving clock	

Name	I/O	Data Width	Description	Module
RGMII_RX_CTL	in	10	RGMII receiving control	
RGMII_RXD	in	[3:0]	RGMII/MII receiving data	
GTX_CLK	in	1	RGMII 125MHz clock input	
GMII_RX_CLK	in	1	GMII receiving clock	
GMII_RX_DV	in	1	GMII receiving enable	
GMII_RXD	in	[7:0]	GMII receiving data	
GMII_RX_ER	in	1	GMII receiving error	Ethernet GMII Interface
GTX_CLK	in	1	GMII 125MHz clock input	
GMII_GTX_CLK	out	1	GMII receiving clock	
GMII_TXD	out	[7:0]	GMII transmitting data	
GMII_TX_EN	out	1	GMII transmitting enable	
GMII_TX_ER	out	1	GMII transmitting error	
MII_RX_CLK	in	1	MII receiving clock	
MII_RXD	in	[3:0]	MII receiving data	
MII_RX_DV	in	1	MII receiving enable	
MII_RX_ER	in	1	MII receiving error	
MII_TX_CLK	in	1	MII transmitting clock	Ethernet MII Interface
MII_TXD	out	[3:0]	MII transmitting data	
MII_TX_EN	out	1	MII transmitting enable	
MII_TX_ER	out	1	MII transmitting error	
MII_COL	in	1	MII conflicting signal	
MII_CRS	in	1	MII carrier signal	
MDC	out	1	Manage channel clock	Ethernet
MDIO	inout	1	Manage channel data	
DDR_CLK_I	in	1	Reference clock, 50MHz recommended	
DDR_STOP_O	out	1	Control signal for GW5A devices, used to control the switching of DDR_MEM_CLK_I, active-low	
DDR_MEM_CLK_I	in	1	Memory interface frequency input by user; when using GW2A devices, this clock can be the PLL output clock or another clock. When using GW5A devices, this clock must be output from PLL's clkout2	DDR3 Memory
DDR_LOCK_I	in	1	If DDR_MEM_CLK_I is input by multiplying PLL, this port is connected to the PLL's pll_lock pin. If the user is not using PLL, this port is connected to high level	

Name	I/O	Data Width	Description	Module
DDR_RSTN_I	in	1	Reset signal	
DDR_INIT_COMPLETE_O	out	1	Initialization completed signal	
DDR_ADDR_O	out	[13:0]	Row address, Column address	
DDR_BA_O	out	[2:0]	Bank address	
DDR_CS_N_O	out	1	Chip select signal	
DDR_RAS_N_O	out	1	Row address strobe signal	
DDR_CAS_N_O	out	1	Column address strobe signal	
DDR_WE_N_O	out	1	Row write enable	
DDR_CLK_O	out	1	A clock signal provided to DDR3 SDRAM	
DDR_CLK_N_O	out	1	Compose a differential signal with DDR_CLK_O	
DDR_CKE_O	out	1	DDR3 SDRAM clock enable signal	
DDR_ODT_O	out	1	Terminating resistor control of memory signal	
DDR_RESET_N_O	out	1	DDR3 SDRAM reset signal	
DDR_DQM_O	out	[1:0]	DDR3 SDRAM data masking signal	
DDR_DQ_IO	inout	[15:0]	DDR3 SDRAM data	
DDR_DQS_IO	inout	[1:0]	DDR3 SDRAM data strobe signal	
DDR_DQS_N_IO	inout	[1:0]	Compose a differential signal with DDR_DQS_IO	
O_psram_ck	out	[1:0]	A clock signal provided to PSRAM	PSRAM Memory
O_psram_ck_n	out	[1:0]	Compose the difference signal with the O_psram_ck	
IO_psram_rwds	inout	[1:0]	PSRAM data selection signal and mask signal	
IO_psram_dq	inout	[15:0]	PSRAM data	
O_psram_reset_n	out	[1:0]	PSRAM reset signal	
O_psram_cs_n	out	[1:0]	Chip selected, active-low.	
init_calib	out	1	Initialization completed signal	
psram_ref_clk	in	1	Reference input clock, it is usually on-board crystal oscillator clock.	
psram_memory_clk	in	1	You can input chip working clock, which is generally a high clock of PLL frequency multiplication, or not use PLL.	
FLASH_SPI_HOLDN	inout	1	NC	SPI-Flash Memory
FLASH_SPI_CSN	inout	1	Slave select signal	

Name	I/O	Data Width	Description	Module
FLASH_SPI_MISO	inout	1	Master input/Slave output	
FLASH_SPI_MOSI	inout	1	Master output/Slave input	
FLASH_SPI_WPN	inout	1	NC	
FLASH_SPI_CLK	inout	1	Clock signal	
APB1PSTRB	out	[3:0]	APB1 PSTRB	APB1 Master [1]
APB1PPROT	out	[2:0]	APB1 PPROT	
APB1PSEL	out	1	APB1 PSEL	
APB1PENABLE	out	1	APB1 PENABLE	
APB1PADDR	out	[31:0]	APB1 PADDR	
APB1PWRITE	out	1	APB1 PWRITE	
APB1PWDATA	out	[31:0]	APB1 PWDATA	
APB1PRDATA	in	[31:0]	APB1 PRDATA	
APB1PREADY	in	1	APB1 PREADY	
APB1PSLVERR	in	1	APB1 PSLVERR	
APB1PCLK	out	1	APB1 PCLK	
APB1PRESET	out	1	APB1 RESET	
APB2PSTRB	out	[3:0]	APB2 PSTRB	APB Master [2]
APB2PPROT	out	[2:0]	APB2 PPROT	
APB2PSEL	out	1	APB2 PSEL	
APB2PENABLE	out	1	APB2 PENABLE	
APB2PADDR	out	[31:0]	APB2 PADDR	
APB2PWRITE	out	1	APB2 PWRITE	
APB2PWDATA	out	[31:0]	APB2 PWDATA	
APB2PRDATA	in	[31:0]	APB2 PRDATA	
APB2PREADY	in	1	APB2 PREADY	
APB2PSLVERR	in	1	APB2 PSLVERR	
APB2PCLK	out	1	APB2 PCLK	
APB2PRESET	out	1	APB2 RESET	
APB3PSTRB	out	[3:0]	APB3 PSTRB	APB Master [3]
APB3PPROT	out	[2:0]	APB3 PPROT	
APB3PSEL	out	1	APB3 PSEL	
APB3PENABLE	out	1	APB3 PENABLE	
APB3PADDR	out	[31:0]	APB3 PADDR	
APB3PWRITE	out	1	APB3 PWRITE	
APB3PWDATA	out	[31:0]	APB3 PWDATA	
APB3PRDATA	in	[31:0]	APB3 PRDATA	
APB3PREADY	in	1	APB3 PREADY	

Name	I/O	Data Width	Description	Module
APB3PSLVERR	in	1	APB3 PSLVERR	
APB3PCLK	out	1	APB3 PCLK	
APB3PRESET	out	1	APB3 RESET	
APB4PSTRB	out	[3:0]	APB4 PSTRB	
APB4PPROT	out	[2:0]	APB4 PPROT	
APB4PSEL	out	1	APB4 PSEL	
APB4PENABLE	out	1	APB4 PENABLE	
APB4PADDR	out	[31:0]	APB4 PADDR	
APB4PWRITE	out	1	APB4 PWRITE	
APB4PWDATA	out	[31:0]	APB4 PWDATA	APB Master [4]
APB4PRDATA	in	[31:0]	APB4 PRDATA	
APB4PREADY	in	1	APB4 PREADY	
APB4PSLVERR	in	1	APB4 PSLVERR	
APB4PCLK	out	1	APB4 PCLK	
APB4PRESET	out	1	APB4 RESET	
APB5PSTRB	out	[3:0]	APB5 PSTRB	
APB5PPROT	out	[2:0]	APB5 PPROT	
APB5PSEL	out	1	APB5 PSEL	
APB5PENABLE	out	1	APB5 PENABLE	
APB5PADDR	out	[31:0]	APB5 PADDR	
APB5PWRITE	out	1	APB5 PWRITE	
APB5PWDATA	out	[31:0]	APB5 PWDATA	APB Master [5]
APB5PRDATA	in	[31:0]	APB5 PRDATA	
APB5PREADY	in	1	APB5 PREADY	
APB5PSLVERR	in	1	APB5 PSLVERR	
APB5PCLK	out	1	APB5 PCLK	
APB5PRESET	out	1	APB5 RESET	
APB6PSTRB	out	[3:0]	APB6 PSTRB	
APB6PPROT	out	[2:0]	APB6 PPROT	
APB6PSEL	out	1	APB6 PSEL	
APB6PENABLE	out	1	APB6 PENABLE	
APB6PADDR	out	[31:0]	APB6 PADDR	
APB6PWRITE	out	1	APB6 PWRITE	
APB6PWDATA	out	[31:0]	APB6 PWDATA	APB Master [6]
APB6PRDATA	in	[31:0]	APB6 PRDATA	
APB6PREADY	in	1	APB6 PREADY	
APB6PSLVERR	in	1	APB6 PSLVERR	
APB6PCLK	out	1	APB6 PCLK	

Name	I/O	Data Width	Description	Module
APB6PRESET	out	1	APB6 RESET	
APB7PSTRB	out	[3:0]	APB7 PSTRB	APB Master [7]
APB7PPROT	out	[2:0]	APB7 PPROT	
APB7PSEL	out	1	APB7 PSEL	
APB7PENABLE	out	1	APB7 PENABLE	
APB7PADDR	out	[31:0]	APB7 PADDR	
APB7PWRITE	out	1	APB7 PWRITE	
APB7PWDATA	out	[31:0]	APB7 PWDATA	
APB7PRDATA	in	[31:0]	APB7 PRDATA	
APB7PREADY	in	1	APB7 PREADY	
APB7PSLVERR	in	1	APB7 PSLVERR	
APB7PCLK	out	1	APB7 PCLK	
APB7PRESET	out	1	APB7 RESET	
APB8PSTRB	out	[3:0]	APB8 PSTRB	APB Master [8]
APB8PPROT	out	[2:0]	APB8 PPROT	
APB8PSEL	out	1	APB8 PSEL	
APB8PENABLE	out	1	APB8 PENABLE	
APB8PADDR	out	[31:0]	APB8 PADDR	
APB8PWRITE	out	1	APB8 PWRITE	
APB8PWDATA	out	[31:0]	APB8 PWDATA	
APB8PRDATA	in	[31:0]	APB8 PRDATA	
APB8PREADY	in	1	APB8 PREADY	
APB8PSLVERR	in	1	APB8 PSLVERR	
APB8PCLK	out	1	APB8 PCLK	
APB8PRESET	out	1	APB8 RESET	
APB9PSTRB	out	[3:0]	APB9 PSTRB	APB Master [9]
APB9PPROT	out	[2:0]	APB9 PPROT	
APB9PSEL	out	1	APB9 PSEL	
APB9PENABLE	out	1	APB9 PENABLE	
APB9PADDR	out	[31:0]	APB9 PADDR	
APB9PWRITE	out	1	APB9 PWRITE	
APB9PWDATA	out	[31:0]	APB9 PWDATA	
APB9PRDATA	in	[31:0]	APB9 PRDATA	
APB9PREADY	in	1	APB9 PREADY	
APB9PSLVERR	in	1	APB9 PSLVERR	
APB9PCLK	out	1	APB9 PCLK	
APB9PRESET	out	1	APB9 RESET	
APB10PSTRB	out	[3:0]	APB10 PSTRB	APB

Name	I/O	Data Width	Description	Module
APB10PPROT	out	[2:0]	APB10 PPROT	Master [10]
APB10PSEL	out	1	APB10 PSEL	
APB10PENABLE	out	1	APB10 PENABLE	
APB10PADDR	out	[31:0]	APB10 PADDR	
APB10PWRITE	out	1	APB10 PWRITE	
APB10PWDATA	out	[31:0]	APB10 PWDATA	
APB10PRDATA	in	[31:0]	APB10 PRDATA	
APB10PREADY	in	1	APB10 PREADY	
APB10PSLVERR	in	1	APB10 PSLVERR	
APB10PCLK	out	1	APB10 PCLK	
APB10PRESET	out	1	APB10 RESET	
APB11PSTRB	out	[3:0]	APB11 PSTRB	APB Master [11]
APB11PPROT	out	[2:0]	APB11 PPROT	
APB11PSEL	out	1	APB11 PSEL	
APB11PENABLE	out	1	APB11 PENABLE	
APB11PADDR	out	[31:0]	APB11 PADDR	
APB11PWRITE	out	1	APB11 PWRITE	
APB11PWDATA	out	[31:0]	APB11 PWDATA	
APB11PRDATA	in	[31:0]	APB11 PRDATA	
APB11PREADY	in	1	APB11 PREADY	
APB11PSLVERR	in	1	APB11 PSLVERR	
APB11PCLK	out	1	APB11 PCLK	
APB11PRESET	out	1	APB11 RESET	
APB12PSTRB	out	[3:0]	APB12 PSTRB	APB Master [12]
APB12PPROT	out	[2:0]	APB12 PPROT	
APB12PSEL	out	1	APB12 PSEL	
APB12PENABLE	out	1	APB12 PENABLE	
APB12PADDR	out	[31:0]	APB12 PADDR	
APB12PWRITE	out	1	APB12 PWRITE	
APB12PWDATA	out	[31:0]	APB12 PWDATA	
APB12PRDATA	in	[31:0]	APB12 PRDATA	
APB12PREADY	in	1	APB12 PREADY	
APB12PSLVERR	in	1	APB12 PSLVERR	
APB12PCLK	out	1	APB12 PCLK	
APB12PRESET	out	1	APB12 RESET	
APB13PSTRB	out	[3:0]	APB13 PSTRB	APB Master [13]
APB13PPROT	out	[2:0]	APB13 PPROT	
APB13PSEL	out	1	APB13 PSEL	

Name	I/O	Data Width	Description	Module
APB13PENABLE	out	1	APB13 PENABLE	
APB13PADDR	out	[31:0]	APB13 PADDR	
APB13PWRITE	out	1	APB13 PWRITE	
APB13PWDATA	out	[31:0]	APB13 PWDATA	
APB13PRDATA	in	[31:0]	APB13 PRDATA	
APB13PREADY	in	1	APB13 PREADY	
APB13PSLVERR	in	1	APB13 PSLVERR	
APB13PCLK	out	1	APB13 PCLK	
APB13PRESET	out	1	APB13 RESET	
APB14PSTRB	out	[3:0]	APB14 PSTRB	
APB14PPROT	out	[2:0]	APB14 PPROT	
APB14PSEL	out	1	APB14 PSEL	
APB14PENABLE	out	1	APB14 PENABLE	
APB14PADDR	out	[31:0]	APB14 PADDR	
APB14PWRITE	out	1	APB14 PWRITE	APB Master [14]
APB14PWDATA	out	[31:0]	APB14 PWDATA	
APB14PRDATA	in	[31:0]	APB14 PRDATA	
APB14PREADY	in	1	APB14 PREADY	
APB14PSLVERR	in	1	APB14 PSLVERR	
APB14PCLK	out	1	APB14 PCLK	
APB14PRESET	out	1	APB14 RESET	
APB15PSTRB	out	[3:0]	APB15 PSTRB	
APB15PPROT	out	[2:0]	APB15 PPROT	
APB15PSEL	out	1	APB15 PSEL	
APB15PENABLE	out	1	APB15 PENABLE	
APB15PADDR	out	[31:0]	APB15 PADDR	
APB15PWRITE	out	1	APB15 PWRITE	APB Master [15]
APB15PWDATA	out	[31:0]	APB15 PWDATA	
APB15PRDATA	in	[31:0]	APB15 PRDATA	
APB15PREADY	in	1	APB15 PREADY	
APB15PSLVERR	in	1	APB15 PSLVERR	
APB15PCLK	out	1	APB15 PCLK	
APB15PRESET	out	1	APB15 RESET	
APB16PSTRB	out	[3:0]	APB16 PSTRB	
APB16PPROT	out	[2:0]	APB16 PPROT	
APB16PSEL	out	1	APB16 PSEL	APB Master [16]
APB16PENABLE	out	1	APB16 PENABLE	
APB16PADDR	out	[31:0]	APB16 PADDR	

Name	I/O	Data Width	Description	Module
APB16PWRITE	out	1	APB16 PWRITE	
APB16PWDATA	out	[31:0]	APB16 PWDATA	
APB16PRDATA	in	[31:0]	APB16 PRDATA	
APB16PREADY	in	1	APB16 PREADY	
APB16PSLVERR	in	1	APB16 PSLVERR	
APB16PCLK	out	1	APB16 PCLK	
APB16PRESET	out	1	APB16 RESET	
EXTFLASH0HSEL	out	1	External Flash HSEL	External Instruction Memory
EXTFLASH0HADDR	out	[31:0]	External Flash HADDR	
EXTFLASH0HTRANS	out	[1:0]	External Flash HTRANS	
EXTFLASH0HWRITE	out	1	External Flash HWRITE	
EXTFLASH0HSIZE	out	[2:0]	External Flash HSIZE	
EXTFLASH0HBURST	out	[2:0]	External Flash HBURST	
EXTFLASH0HPROT	out	[3:0]	External Flash HPROT	
EXTFLASH0HWDATA	out	[31:0]	External Flash HWDATA	
EXTFLASH0HMASTLOCK	out	1	External Flash HMASTLOCK	
EXTFLASH0HREADYMUX	out	1	External Flash HREADYMUX	
EXTFLASH0HRDATA	in	[31:0]	External Flash HRDATA	
EXTFLASH0HREADYOUT	in	1	External Flash HREDAYOUT	
EXTFLASH0HRESP	in	[1:0]	External Flash HRESP	
EXTFLASH0HMASTER	out	[3:0]	External Flash MASTER	
EXTFLASH0HCLK	out	1	External Flash HCLK	
EXTFLASH0HRESET	out	1	External Flash RESET	
EXTSRAM0HSEL	out	1	External SRAM HSEL	External Data Memory
EXTSRAM0HADDR	out	[31:0]	External SRAM HADDR	
EXTSRAM0HTRANS	out	[1:0]	External SRAM HTRANS	
EXTSRAM0HWRITE	out	1	External SRAM HWRITE	
EXTSRAM0HSIZE	out	[2:0]	External SRAM HSIZE	
EXTSRAM0HBURST	out	[2:0]	External SRAM HBURST	

Name	I/O	Data Width	Description	Module
EXTSRAM0HPROT	out	[3:0]	External SRAM HPROT	
EXTSRAM0HWDATA	out	[31:0]	External SRAM HWDATA	
EXTSRAM0HMASTLOCK	out	1	External SRAM HMASTLOCK	
EXTSRAM0HREADYMUX	out	1	External SRAM HREADYMUX	
EXTSRAM0HRDATA	in	[31:0]	External SRAM HRDATA	
EXTSRAM0HREADYOUT	in	1	External SRAM HREDAYOUT	
EXTSRAM0HRESP	in	[1:0]	External SRAM HRESP	
EXTSRAM0HMASTER	out	[3:0]	External SRAM MASTER	
EXTSRAM0HCLK	out	1	External SRAM HCLK	
EXTSRAM0HRESET	out	1	External SRAM RESET	
AHB1HSEL	out	1	AHB1 HSEL	AHB Master [1]
AHB1HADDR	out	[31:0]	AHB1 HADDR	
AHB1HTRANS	out	[1:0]	AHB1 HTRANS	
AHB1HWRITE	out	1	AHB1 HWRITE	
AHB1HSIZE	out	[2:0]	AHB1 HSIZE	
AHB1HBURST	out	[2:0]	AHB1 HBURST	
AHB1HPROT	out	[3:0]	AHB1 HPROT	
AHB1HWDATA	out	[31:0]	AHB1 HWDATA	
AHB1HMASTLOCK	out	1	AHB1 HMASTLOCK	
AHB1HREADYMUX	out	1	AHB1 HREADYMUX	
AHB1HRDATA	in	[31:0]	AHB1 HRDATA	
AHB1HREADYOUT	in	1	AHB1 HREDAYOUT	
AHB1HRESP	in	[1:0]	AHB1 HRESP	
AHB1HMASTER	out	[3:0]	AHB1 MASTER	
AHB1HCLK	out	1	AHB1 HCLK	
AHB1HRESET	out	1	AHB1 RESET	
AHB2HSEL	out	1	AHB2 HSEL	AHB Master [2]
AHB2HADDR	out	[31:0]	AHB2 HADDR	
AHB2HTRANS	out	[1:0]	AHB2 HTRANS	
AHB2HWRITE	out	1	AHB2 HWRITE	
AHB2HSIZE	out	[2:0]	AHB2 HSIZE	
AHB2HBURST	out	[2:0]	AHB2 HBURST	
AHB2HPROT	out	[3:0]	AHB2 HPROT	

Name	I/O	Data Width	Description	Module
AHB2HWDATA	out	[31:0]	AHB2 HWDATA	
AHB2HMASTLOCK	out	1	AHB2 HMASTLOCK	
AHB2HREADYMUX	out	1	AHB2 HREADYMUX	
AHB2HRDATA	in	[31:0]	AHB2 HRDATA	
AHB2HREADYOUT	in	1	AHB2 HREDAYOUT	
AHB2HRESP	in	[1:0]	AHB2 HRESP	
AHB2HMASTER	out	[3:0]	AHB2 MASTER	
AHB2HCLK	out	1	AHB2 HCLK	
AHB2HRESET	out	1	AHB2 RESET	
AHB3HSEL	out	1	AHB3 HSEL	AHB Master [3]
AHB3HADDR	out	[31:0]	AHB3 HADDR	
AHB3HTRANS	out	[1:0]	AHB3 HTRANS	
AHB3HWRITE	out	1	AHB3 HWRITE	
AHB3HSIZE	out	[2:0]	AHB3 HSIZE	
AHB3HBURST	out	[2:0]	AHB3 HBURST	
AHB3HPROT	out	[3:0]	AHB3 HPROT	
AHB3HWDATA	out	[31:0]	AHB3 HWDATA	
AHB3HMASTLOCK	out	1	AHB3 HMASTLOCK	
AHB3HREADYMUX	out	1	AHB3 HREADYMUX	
AHB3HRDATA	in	[31:0]	AHB3 HRDATA	
AHB3HREADYOUT	in	1	AHB3 HREDAYOUT	
AHB3HRESP	in	[1:0]	AHB3 HRESP	
AHB3HMASTER	out	[3:0]	AHB3 MASTER	
AHB3HCLK	out	1	AHB3 HCLK	
AHB3HRESET	out	1	AHB3 RESET	
AHB4HSEL	out	1	AHB4 HSEL	AHB Master [4]
AHB4HADDR	out	[31:0]	AHB4 HADDR	
AHB4HTRANS	out	[1:0]	AHB4 HTRANS	
AHB4HWRITE	out	1	AHB4 HWRITE	
AHB4HSIZE	out	[2:0]	AHB4 HSIZE	
AHB4HBURST	out	[2:0]	AHB4 HBURST	
AHB4HPROT	out	[3:0]	AHB4 HPROT	
AHB4HWDATA	out	[31:0]	AHB4 HWDATA	
AHB4HMASTLOCK	out	1	AHB4 HMASTLOCK	
AHB4HREADYMUX	out	1	AHB4 HREADYMUX	

Name	I/O	Data Width	Description	Module
AHB4HRDATA	in	[31:0]	AHB4 HRDATA	
AHB4HREADYOUT	in	1	AHB4 HREDAYOUT	
AHB4HRESP	in	[1:0]	AHB4 HRESP	
AHB4HMASTER	out	[3:0]	AHB4 MASTER	
AHB4HCLK	out	1	AHB4 HCLK	
AHB4HRESET	out	1	AHB4 RESET	
AHB5HSEL	out	1	AHB5 HSEL	AHB Master [5]
AHB5HADDR	out	[31:0]	AHB5 HADDR	
AHB5HTRANS	out	[1:0]	AHB5 HTRANS	
AHB5HWRITE	out	1	AHB5 HWRITE	
AHB5HSIZE	out	[2:0]	AHB5 HSIZE	
AHB5HBURST	out	[2:0]	AHB5 HBURST	
AHB5HPROT	out	[3:0]	AHB5 HPROT	
AHB5HWDATA	out	[31:0]	AHB5 HWDATA	
AHB5HMASTLOCK	out	1	AHB5 HMASTLOCK	
AHB5HREADYMUX	out	1	AHB5 HREADYMUX	
AHB5HRDATA	in	[31:0]	AHB5 HRDATA	
AHB5HREADYOUT	in	1	AHB5 HREDAYOUT	
AHB5HRESP	in	[1:0]	AHB5 HRESP	
AHB5HMASTER	out	[3:0]	AHB5 MASTER	
AHB5HCLK	out	1	AHB5 HCLK	
AHB5HRESET	out	1	AHB5 RESET	
AHB6HSEL	out	1	AHB6 HSEL	AHB Master [6]
AHB6HADDR	out	[31:0]	AHB6 HADDR	
AHB6HTRANS	out	[1:0]	AHB6 HTRANS	
AHB6HWRITE	out	1	AHB6 HWRITE	
AHB6HSIZE	out	[2:0]	AHB6 HSIZE	
AHB6HBURST	out	[2:0]	AHB6 HBURST	
AHB6HPROT	out	[3:0]	AHB6 HPROT	
AHB6HWDATA	out	[31:0]	AHB6 HWDATA	
AHB6HMASTLOCK	out	1	AHB6 HMASTLOCK	
AHB6HREADYMUX	out	1	AHB6 HREADYMUX	
AHB6HRDATA	in	[31:0]	AHB6 HRDATA	
AHB6HREADYOUT	in	1	AHB6 HREDAYOUT	
AHB6HRESP	in	[1:0]	AHB6 HRESP	

Name	I/O	Data Width	Description	Module
AHB6HMASTER	out	[3:0]	AHB6 MASTER	
AHB6HCLK	out	1	AHB6 HCLK	
AHB6HRESET	out	1	AHB6 RESET	

1.4 System Resource Statistics

Using GW5A-25 Version A as an example, the system resource statistics of Gowin_EMPU_M1 is as shown in Table 1-2.

Table 1-2 System Resource Statistics

Configuration \ Resources	LUTs	Registers	BSRAMs	DSP Macros
Cortex-M1 core system (Debug Version)	5496	2551	32 (DPB)	2 (MULT27X36)
Cortex-M1 core system (No Debug Version)	3080	1175	32 (SP)	2 (MULT27X36)
Cortex-M1 core system+ GPIO, SPI-Flash, 2x UART, 2x Timer, I2C, SPI, TRNG, WDT, DualTimer, AHB Master [1], APB Master [1]	10957	5299	32 (DPB)	2 (MULT27X36)

1.5 System Performance Statistics

The system performance statistics of Gowin_EMPU_M1 for different devices is as shown in Table 1-3.

Table 1-3 System Performance Statistics

Device	GW1N-9 Version C	GW2A-18 Version C	GW2A-55 Version C	GW5AST-138 Version B	GW5A-25 Version A	GW5AT-60 Version B
Frequency	60MHz	100MHz	100MHz	125MHz	130MHz	130MHz
Configuration	No debug	Debug	Debug	Debug	Debug	Debug
ITCM	8KB	32KB	32KB	32KB	32KB	32KB
DTCM	8KB	32KB	32KB	32KB	32KB	32KB
Peripheral	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO

2 Hardware Design Flow

2.1 Hardware Target

- DK_START_GW2A18 V2.0
  GW2A-LV18PG256C8/I7
  GW2A-18 (Version C)
- DK_START_GW1N-LV9LQ144C6I5 V2.1
  GW1N-LV9LQ144C6/I5
  GW1N-9 (Version C)
- DK_START_GW2A-LV55PG484C8I7 V1.3
  GW2A-LV55PG484C8/I7
  GW2A-55 (Version C)
- DK_START_GW2AR-LV18EQ144C8I7 V1.1
  GW2AR-LV18EQ144PC8/I7
  GW2AR-18 (Version C)
- DK_START_GW5AST-LV138FPG676A V1.0
  GW5AST-LV138FPG676AES
  GW5AST-138 (Version B)
- TANG_MEGA-138K_Pro_Dock
  GW5AST-LV138FPG676AES
  GW5AST-138 (Version B)
- DK_START_GW5A-LV25UG324 V2.0
  GW5A-LV25UG324C2/I1
  GW5A-25 (Version A)
- DK_START_DDR2-GW5A_EV25UG324S V1.0
  GW5A-EV25UG324SES
  GW5A-25 (Version A)

- DK_DP_GW5AT-LV60UG225 V1.0
  GW5AT-LV60UG225C2/I1
  GW5AT-60 (Version B)

2.2 Software Version

Tested software version: Gowin_V1.9.11 (64-bit)

2.3 IP Core Generator Tool

Configure and generate Gowin_EMPU_M1 hardware design using IP Core Generator tool of Gowin Software.

2.4 Download Tool

Download the bitstream file of the hardware design using Gowin Programmer.

For the using of Gowin Programmer, see SUG502, *Gowin Programmer User Guide*.

2.5 Design Flow

Gowin_EMPU_M1 hardware design flow is as follows:

1. Use IP Core Generator to configure Cortex-M1, APB Bus Peripherals and AHB Bus Peripherals. Then generate Gowin_EMPU_M1 hardware design. Import to project.
2. Instantiate Gowin_EMPU_M1 Top Module, import user designs, and connect user designs with Gowin_EMPU_M1 Top Module.
3. Add physical and timing Constraints.
4. Use GowinSynthesis as the synthesis tool to synthesize.
5. Run Place & Route tool to generate the bitstream files of the hardware design.
6. Download the bitstream file to chips using Gowin Programmer.

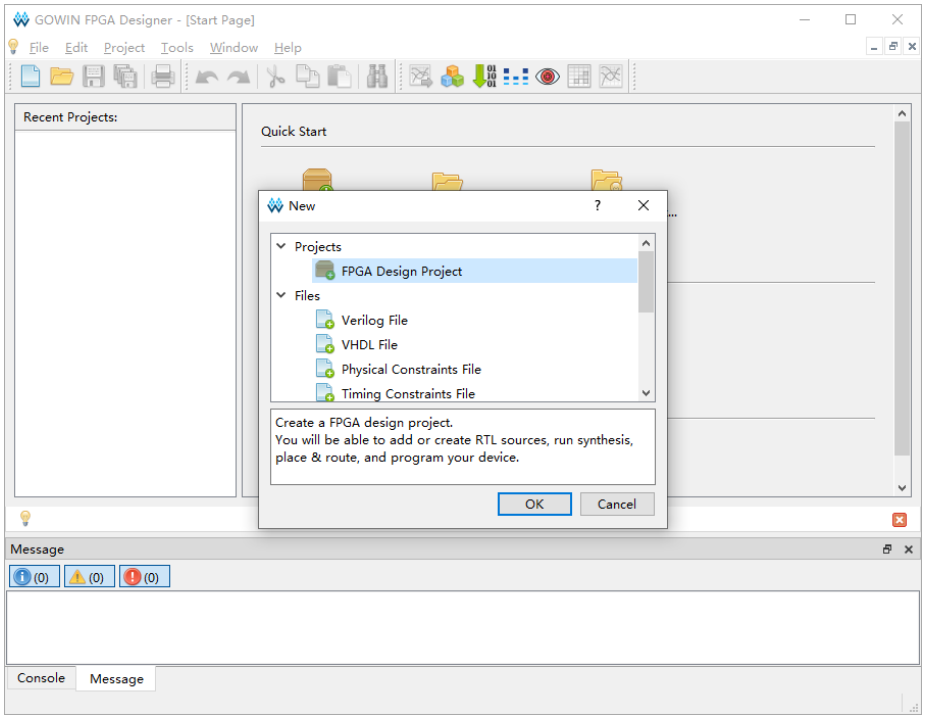
3 Project Template

3.1 Project Creation

3.1.1 Create a New Project

Run Gowin software. Click "File > New… > FPGA Design Project" on the menu bar, or click "" on the tool bar, or click "New Project…" under "Quick Start" to create FPGA Design project, as shown in Figure 3-1.

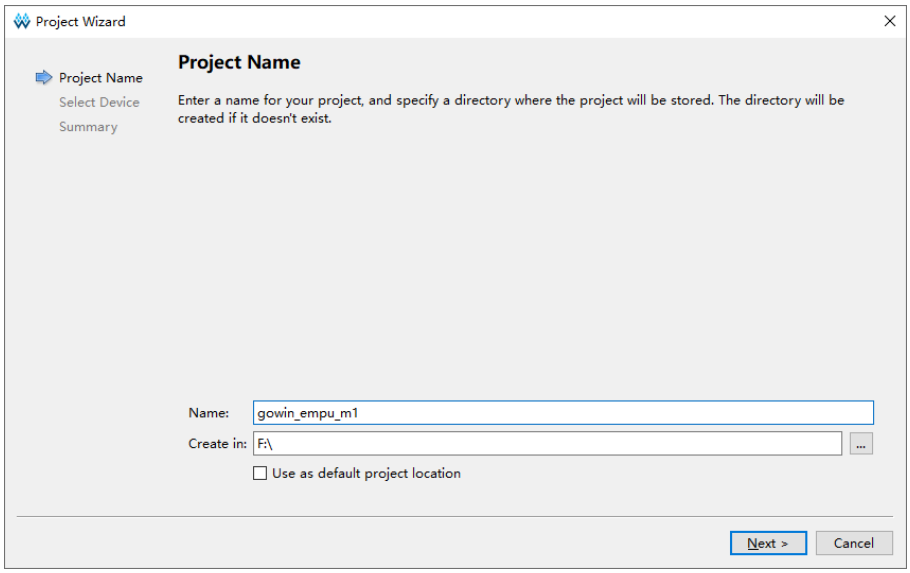
Figure 3-1 Create a FPGA Design Project



3.1.2 Set Project Name and Path

Enter the project name and select the project path, as shown in Figure 3-2.

Figure 3-2 Set Project Name and Path



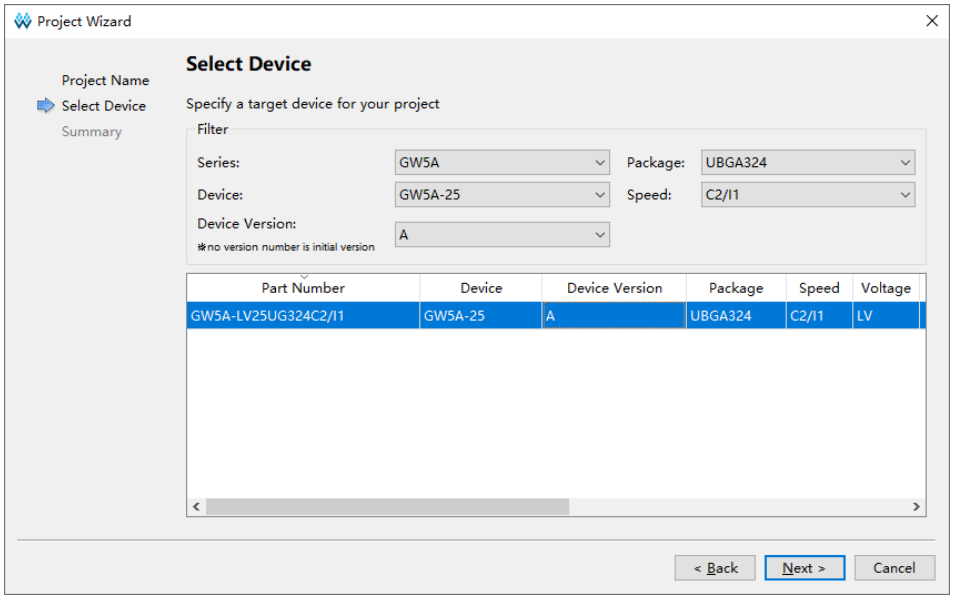
3.1.3 Select Device

Select Series, Device, Device Version, Package, Speed, and Part Number, as shown in Figure 3-3.

Use DK_START_GW5A-LV25UG324 V2.0 reference design for an instance.

- Series: GW5A
- Device: GW5A-25
- Device Version: A
- Package: UBGA324
- Speed: C2/I1
- Part Number: GW5A-LV25UG324C2/I1

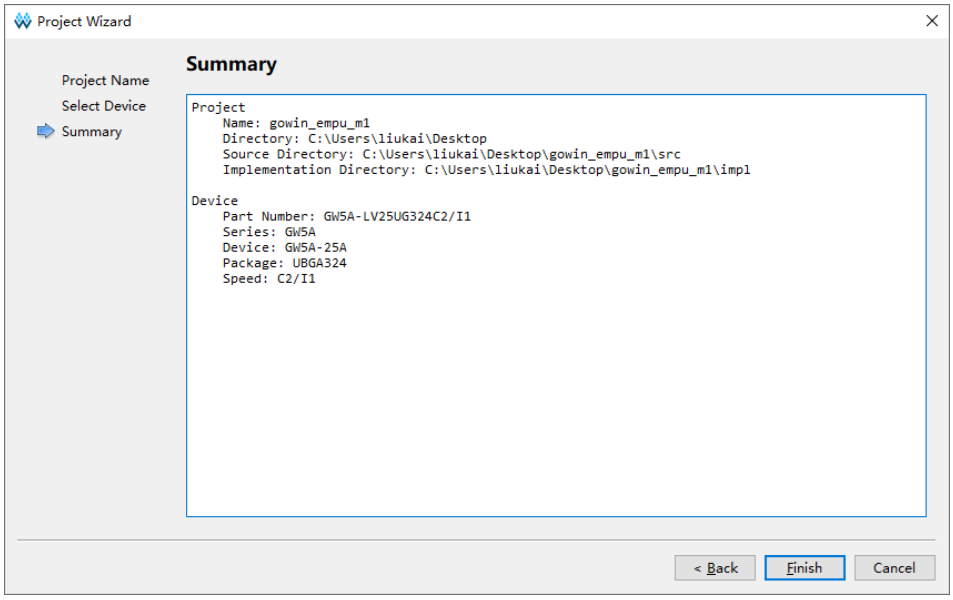
Figure 3-3 Select Device



3.1.4 Project Creation Completed

As shown in Figure 3-4, the new project is completed.

Figure 3-4 Summary



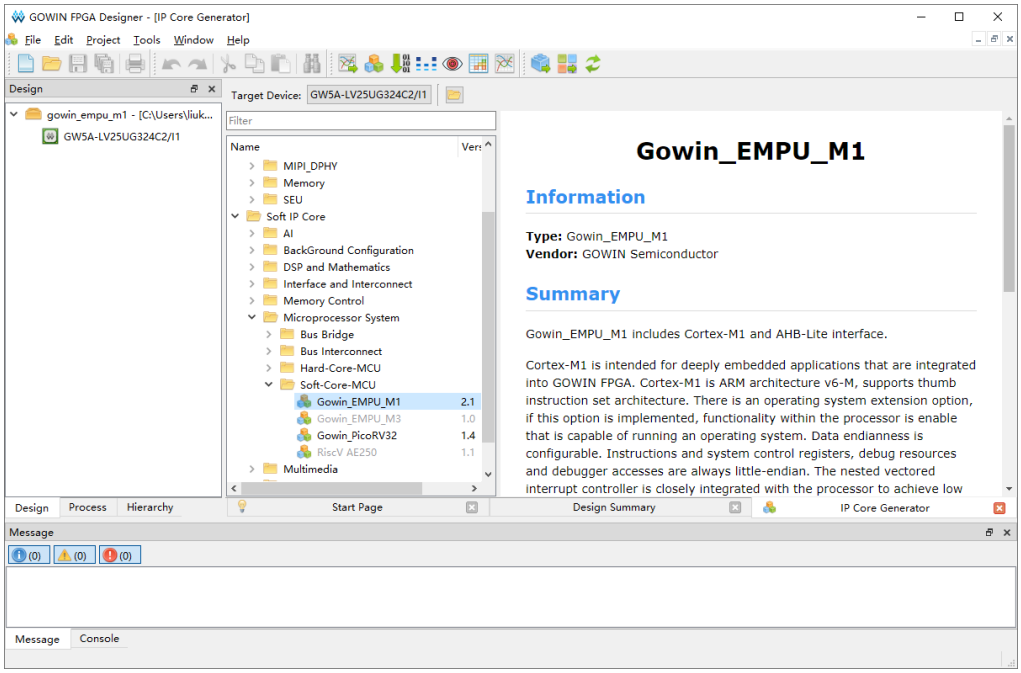
3.2 Hardware Design

Use IP Core Generator to generate Gowin_EMPU_M1 hardware designs.

Select "Tools > IP Core Generator" in the menu bar or "  " to open the IP Core Generator.

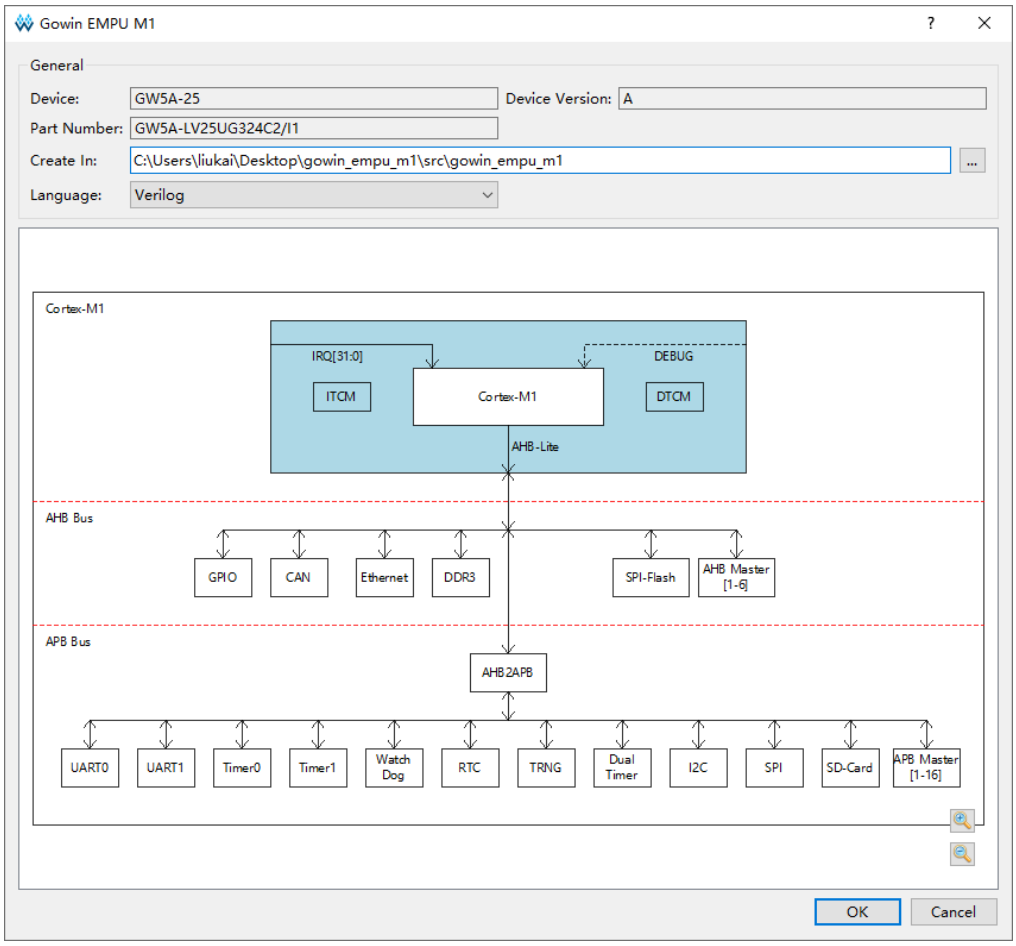
Select "Soft IP Core > Microprocessor System > Soft-Core-MCU > Gowin_EMPU_M1 2.1" as shown in Figure 3-5.

Figure 3-5 Select Gowin_EMPU_M1



Open Gowin_EMPU_M1. Gowin_EMPU_M1 system configuration options are as shown in Figure 3-6, including Cortex-M1, APB Bus Peripherals and AHB Bus Peripherals.

Figure 3-6 System Configuration



3.2.1 Cortex-M1 Core System Configuration

Cortex-M1 core system configuration is as shown in Table 3-1.

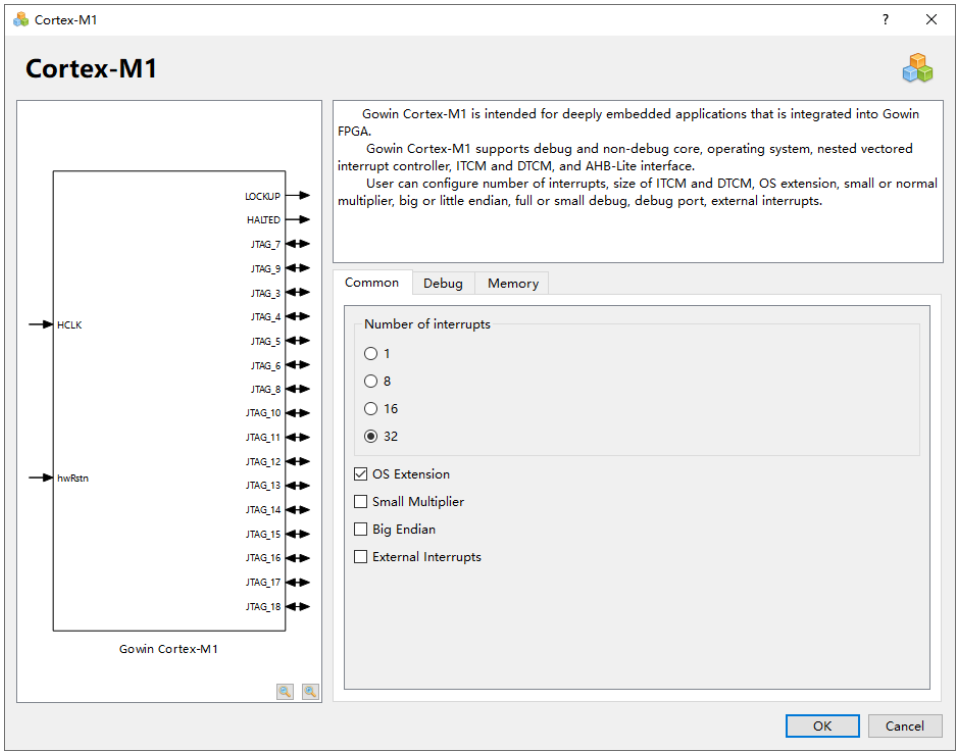
Table 3-1 Cortex-M1 Core System Configuration

Options	Description
Number of interrupts	Configure external interrupts number of Cortex-M1; you can select 1, 8, 16, or 32, and the default value is 32.
OS Extension	Cortex-M1 supports operation system or not, and the default is support.
Small Multiplier	Configure Cortex-M1 hardware multiplier in small mode, and the default is normal mode.
Big Endian	Configure Cortex-M1 data in big endian format, and the default is little endian.
External Interrupts	Configure four extended external interrupt inputs
Enable Debug	Enable Cortex-M1 Debug, and the default is Enable Debug.
Debug Port Select	Configure debugger interface, which can be selected as JTAG, Serial Wire, or JTAG and Serial Wire, and the default is JTAG and Serial Wire.
Small Debug	Configure debugger in Small mode, and the default is Full mode.
ITCM Select	Select internal or external instruction memory, and the default is internal instruction memory.
ITCM Size	Configure the Size of internal instruction memory as 1/2/4/8/16/32/64/128/256/512KB. ● For GW1N/R-9, the maximum size is 32KB, and the default is 16KB. ● For GW2AN-9X/18X, the maximum size is 32KB, and the default is 16KB. ● For GW2A/R/NR-18, the maximum size is 64KB, and the default is 32KB. ● For GW2A/N-55, the maximum size is 256KB, and the default is 64KB. ● For GW5A/T/ST/S-138, the maximum size is 512KB, and the default is 128KB. ● For GW5AT-75, the maximum size is 256KB, and the default is 128KB. ● For GW5A/R/S-25, the maximum size is 64KB, and the default is 32KB. ● For GW5A/T-60, the maximum size is 128KB, and the default is 64KB. ● For GW5AT/RT-15, the maximum size is 64KB, and the default is 32KB.
Initialize ITCM	Enable ITCM Initialization, and the default is disabled.
ITCM Initialization Path	ITCM Initial value file path
DTCM Select	Select internal or external data memory, and the default is internal data memory
DTCM Size	Configure the Size of internal data memory as 1/2/4/8/16/32/64/128/256/512KB. ● For GW1N/R-9, the maximum size is 32KB, and the default is 16KB. ● For GW2AN-9X/18X, the maximum size is 32KB, and the default is 16KB. ● For GW2A/R/NR-18, the maximum size is 64KB, and the default is 32KB. ● For GW2A/N-55, the maximum size is 256KB, and the default is 64KB. ● For GW5A/T/ST/S-138, the maximum size is 512KB, and the default is 128KB. ● For GW5AT-75, the maximum size is 256KB, and the default is 128KB.

Options	Description
	● For GW5A/R/S-25, the maximum size is 64KB, and the default is 32KB. ● For GW5A/T-60, the maximum size is 128KB, and the default is 64KB. ● For GW5AT/RT-15, the maximum size is 64KB, and the default is 32KB.

Double click Cortex-M1 to open the Cortex-M1 system configuration options including "Common", "Debug", and "Memory", as shown in Figure 3-7.

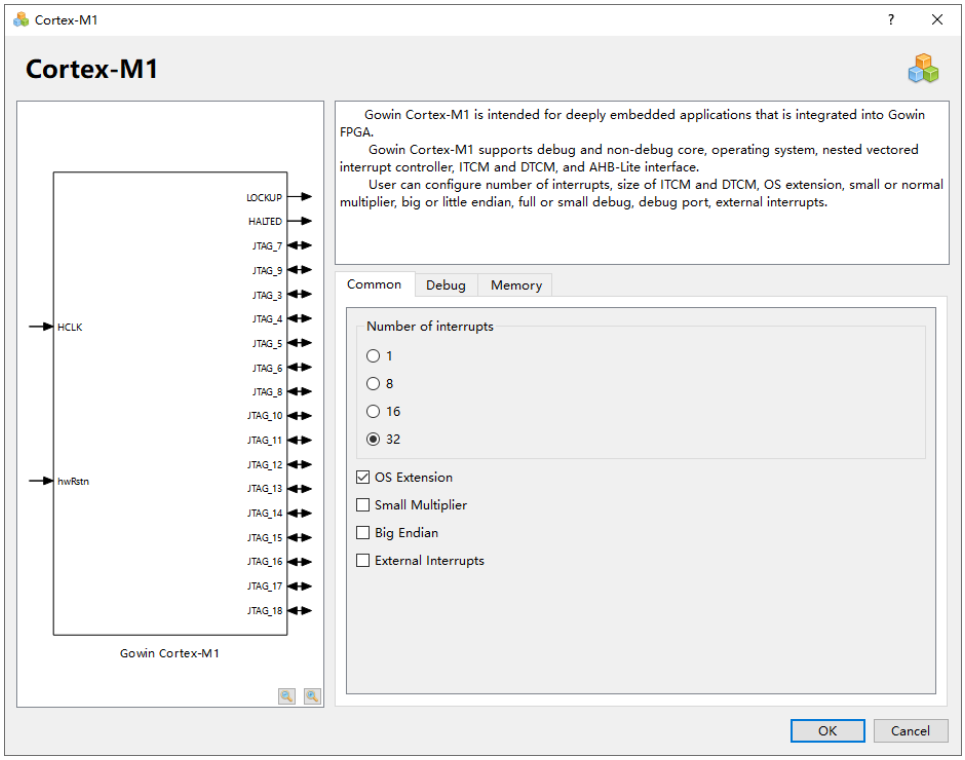
Figure 3-7 Cortex-M1 Core System Configuration Option



Common

Select "Common", you can configure "Number of interrupts", "OS Extension", "Small Multiplier", "Big Endian", and "External Interrupts", as shown in Figure 3-8.

Figure 3-8 Cortex-M1 Common Configuration

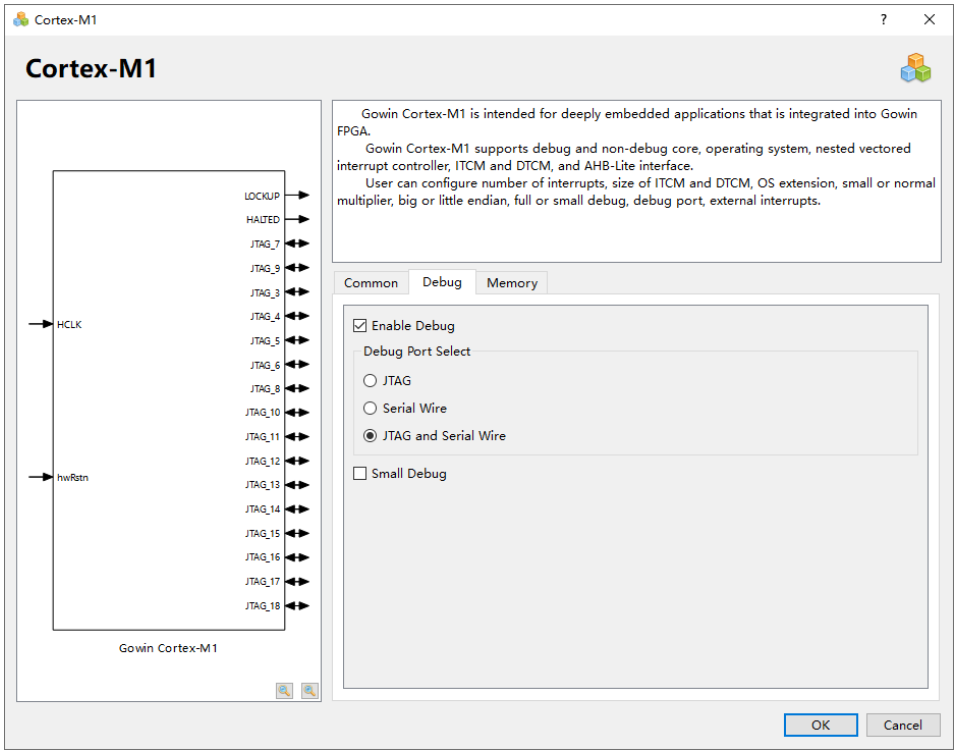


- Number of Interrupts
  You can configure 1,8,16 or 32 external interrupts. The default is 32.
- OS Extension
  If OS Extension is selected, Cortex-M1 will support operation system extension. The default is support.
- Small Multiplier
  If Multiplier Mode is selected, Cortex-M1 supports Small multiplier; if not, it supports Normal multiplier. The default is Normal multiplier.
- Big Endian
  If Big Endian is selected, Cortex-M1 supports big endian; if not, it supports little endian. The default is little endian.
- External Interrupts
  If External Interrupt is selected, Cortes-M1 supports four external interrupt inputs; if not, it does not support external interrupt. The default is not supported.

Debug

Select Debugging Configuration, you can enable debug, debug interface and select debugger mode, as shown in Figure 3-9.

Figure 3-9 Cortex-M1 Debug Configuration

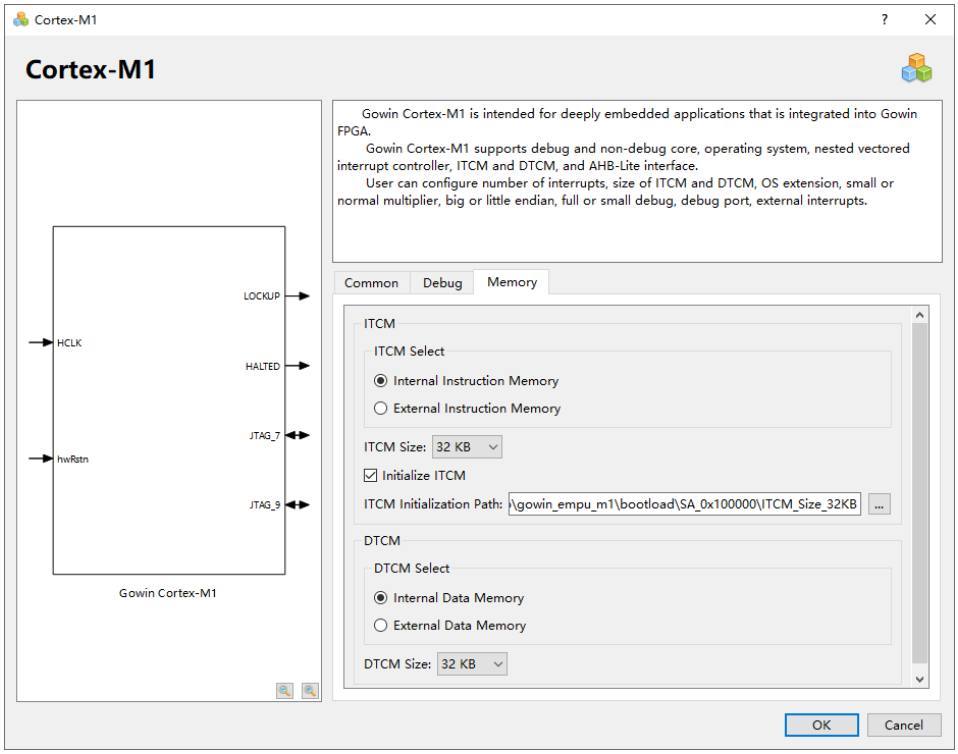


- Enable Debug
  If Enable Debug is selected, Cortex-M1 supports debugging; if not, it does not support debugging. The default is Enable Debug.
- Debug Interface
  You can select JTAG, Serial Wire, or JTAG and Serial Wire. The default is JTAG and Serial Wire.
- Debugger Mode
  If "Small Debug" is selected, Cortex-M1 supports debugger in small mode; if not, it supports debugger in Full mode. The default is debugger in Full mode.

Memory

Select Memory, you can configure ITCM and DTCM, as shown in Figure 3-10.

Figure 3-10 Cortex-M1 Memory Configuration



- ITCM Select
  - You can select "Internal Instruction Memory" or "External Instruction Memory", and the default is "Internal Instruction Memory".
  - Internal Instruction Memory: On-chip Block RAM hardware storage resource; start address 0x00000000.
  - External Instruction Memory: SPI-Flash Memory; start address 0x00000000.
- ITCM Size
  - Prerequisite: Internal Instruction Memory has been selected.
  - You can select 1KB, 2KB, 4KB, 8KB, 16KB, 32KB, 64KB, 128KB, 256KB, or 512KB.
  - For GW1N/R-9, the maximum size is 32KB, and the default is 16KB.
  - For GW2AN-9X/18X, the maximum size is 32KB, and the default is 16KB.
  - For GW2A/R/NR-18, the maximum size is 64KB, and the default is 32KB.
  - For GW2A/N-55, the maximum size is 256KB, and the default is 64KB.
  - For GW5A/T/ST/S-138, the maximum size is 512KB, and the default is 128KB.

  - For GW5AT-75, the maximum size is 256KB, and the default is 128KB.
  - For GW5A/R/S-25, the maximum size is 64KB, and the default is 32KB.
  - For GW5A/T-60, the maximum size is 128KB, and the default is 64KB.
  - For GW5AT/RT-15, the maximum size is 64KB, and the default is 32KB.

- ITCM Initialization
  - Prerequisite: Internal Instruction Memory has been selected;
  - If Initialize ITCM is selected, ITCM initialization is supported. You can import ITCM initial value file path.
  - If off-chip SPI-Flash Memory is selected to download and start-up, ITCM initial value imports the different bootload file paths according to different ITCM Size.

  Note!

  The ITCM Initialization Path cannot contain numbers or escape characters such as "\r" and "\n".

- DTCM Select
  - You can select Internal Data Memory or External Data Memory，and the default is Internal Data Memory.
  - Internal Data Memory: On-chip Block RAM hardware storage resource; start address 0x00000000.
  - External Data Memory: DDR Memory; start address 0x00000000.
- DTCM Size
  - Prerequisite: Internal Data Memory has been selected;
  - You can select 1KB, 2KB, 4KB, 8KB, 16KB, 32KB, 64KB, 128KB, 256KB or 512KB.
  - For GW1N/R-9, the maximum size is 32KB, and the default is 16KB.
  - For GW2AN-9X/18X, the maximum size is 32KB, and the default is 16KB.
  - For GW2A/R/NR-18, the maximum size is 64KB, and the default is 32KB.
  - For GW2A/N-55, the maximum size is 256KB, and the default is 64KB.
  - For GW5A/T/ST/S-138, the maximum size is 512KB, and the default is 128KB.
  - For GW5AT-75, the maximum size is 256KB, and the default is 128KB.

- For GW5A/R/S-25, the maximum size is 64KB, and the default is 32KB.
- For GW5A/T-60, the maximum size is 128KB, and the default is 64KB.
- For GW5AT/RT-15, the maximum size is 64KB, and the default is 32KB.

- ITCM and DTCM Configuration Limits
  - Prerequisite: Internal Instruction Memory and Internal Data Memory has been selected.
  - For GW1N/R-9, ITCM or DTCM can be configured up to 32KB. If ITCM or DTCM has been configured to 32KB, the other can only be configured up to 16KB.
  - For GW2AN-9X/18X, ITCM or DTCM can be configured up to 32KB. If ITCM or DTCM has been configured to 32KB, the other can only be configured up to 16KB.
  - For GW2A/R/NR-18, ITCM or DTCM can be configured up to 64KB. If ITCM or DTCM has been configured to 64KB, the other can only be configured up to 16KB.
  - For GW2A/N-55, ITCM or DTCM can be configured up to 256KB. If ITCM or DTCM has been configured to 32KB, the other can only be configured up to 16KB.
  - For GW5A/T/ST/S-138, ITCM or DTCM can be configured up to 512KB. If ITCM or DTCM has been configured to 512KB, the other can only be configured up to 128KB.
  - For GW5AT-75, ITCM or DTCM can be configured up to 256KB. If ITCM or DTCM has been configured to 256KB, the other can only be configured up to 256KB.
  - For GW5A/R/S-25, ITCM or DTCM can be configured up to 64KB. If ITCM or DTCM has been configured to 64KB, the other can only be configured up to 32KB.
  - For GW5AT/RT-15, ITCM or DTCM can be configured up to 64KB. If ITCM or DTCM has been configured to 64KB, the other can only be configured up to 8KB.
  - For GW5A/T-60, ITCM or DTCM can be configured up to 128KB. If ITCM or DTCM has been configured to 128KB, the other can only be configured up to 64KB.
- External Instruction/Data Memory Solution
  - For GW1N/R-9, you can choose embedded UserFlash as External Instruction Memory. You can see…\solution\Embedded_Memory in the reference design for details; and the instruction memory start address is 0x00000000.
  - Use SPI-Flash Memory as External Instruction Memory and use BSRAM Memory as External Data Memory. You can see …

\solution\External_Memory in the reference design for details; the instruction memory start address is 0x00000000, and the data memory start address is 0x20100000.

3.2.2 Bus Peripheral System Configuration

Bus peripheral system configuration options are described in Table 3-2.

Table 3-2 Bus Peripheral System Configuration Options

Options	Description
Enable GPIO	Enable GPIO, disabled by default.
Enable GPIO I/O	Enable GPIO inout, disabled by default.
Enable CAN	Enable CAN, disabled by default.
Buffer Depth	CAN selects Buffer Depth. The default Value is 256.
Enable Ethernet	Enable Ethernet, disabled by default.
Interface	Ethernet selects Interface (RGMII/GMII/MII). The default is RGMII.
RGMII Input Delay	RGMII input delay. The default Value is 100.
MIIM Clock Divider	MIIM clock divider. The default Value is 20.
Enable DDR3	Enable DDR3 Memory, disabled by default.
Enable PSRAM	Enable PSRAM Memory, disabled by default.
Enable SPI-Flash	Enable SPI-Flash Memory functions including download and read, write and erasure of Memory, disabled by default.
Enable AHB Master [1]	Enable AHB Master[1], disabled by default.
Enable AHB Master [2]	Enable AHB Master[2], disabled by default.
Enable AHB Master [3]	Enable AHB Master[3], disabled by default.
Enable AHB Master [4]	Enable AHB Master[4], disabled by default.
Enable AHB Master [5]	Enable AHB Master[5], disabled by default.
Enable AHB Master [6]	Enable AHB Master[6], disabled by default.
Enable UART0	Enable Serial Port0, disabled by default.
Enable UART1	Enable Serial Port1, disabled by default.
Enable Timer0	Enable Timer0, disabled by default.
Enable Timer1	Enable Timer1, disabled by default.
Enable WatchDog	Enable Watchdog, disabled by default.
Enable RTC	Enable RTC, disabled by default.
Enable TRNG	Enable TRNG, disabled by default.
Enable DualTimer	Enable DualTimer, disabled by default.
Enable I^2C	Enable I^2C master, disabled by default.
Enable I^2C I/O	Enable I^2C master inout, enabled by default.
Enable SPI	Enable SPI master, disabled by default.
Enable SD-Card	Enable SPI-Card, disabled by default
Enable APB Master [1]	Enable APB Master[1], disabled by default.
Enable APB Master [2]	Enable APB Master[2], disabled by default.

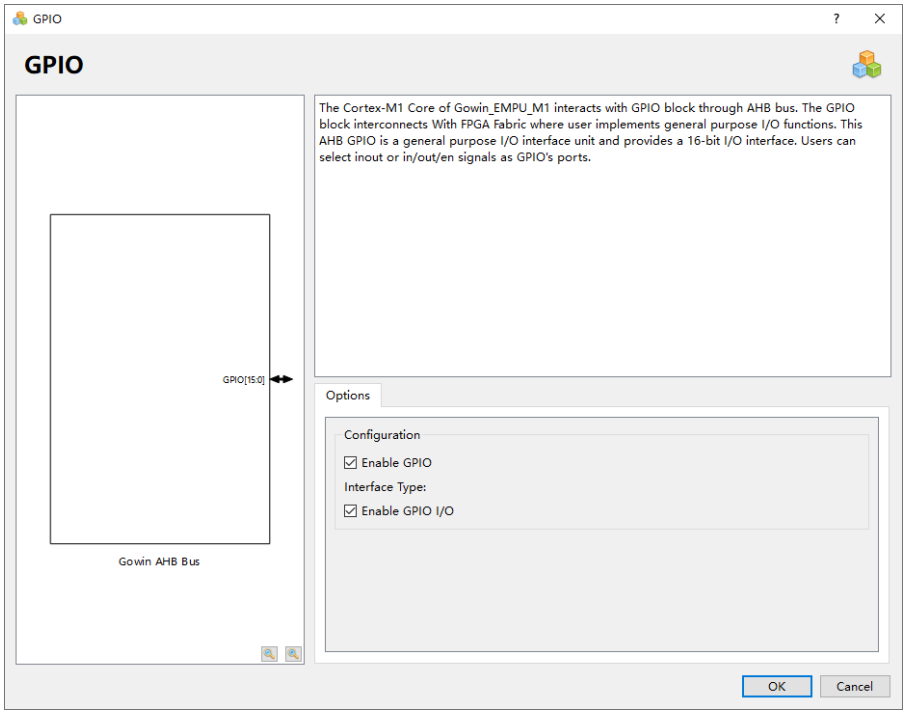
Options	Description
Enable APB Master [3]	Enable APB Master[3], disabled by default.
Enable APB Master [4]	Enable APB Master[4], disabled by default.
Enable APB Master [5]	Enable APB Master[5], disabled by default.
Enable APB Master [6]	Enable APB Master[6], disabled by default.
Enable APB Master [7]	Enable APB Master[7], disabled by default.
Enable APB Master [8]	Enable APB Master[8], disabled by default.
Enable APB Master [9]	Enable APB Master[9], disabled by default.
Enable APB Master [10]	Enable APB Master[10], disabled by default.
Enable APB Master [11]	Enable APB Master[11], disabled by default.
Enable APB Master [12]	Enable APB Master[12], disabled by default.
Enable APB Master [13]	Enable APB Master[13], disabled by default.
Enable APB Master [14]	Enable APB Master[14], disabled by default.
Enable APB Master [15]	Enable APB Master[15], disabled by default.
Enable APB Master [16]	Enable APB Master[16], disabled by default.

GPIO

Double click to configure GPIO, as shown in Figure 3-11.

- If "Enable GPIO" is selected, Gowin_EMPU_M1 supports GPIO, disabled by default.
- If "Enable GPIO" is selected, GPIO port type can be configured.
- If "Enable GPIO I/O" is selected, GPIO supports INOUT port, or supports IN, OUT, EN, and the default is INOUT.

Figure 3-11 GPIO Configuration

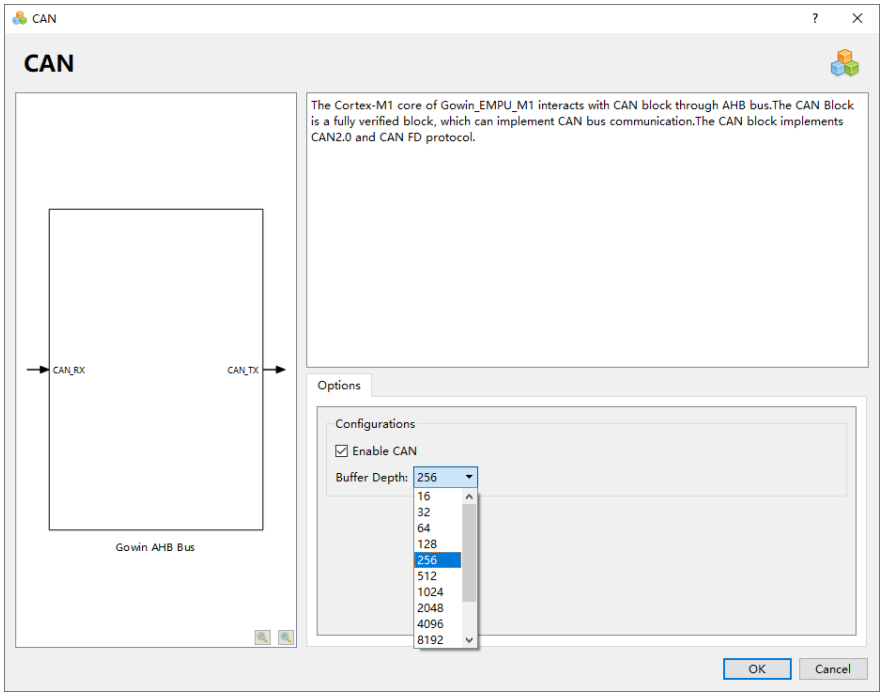


CAN

Double click to open CAN, as shown in Figure 3-12.

- If "Enable CAN" is selected, Gowin_EMPU_M1 supports CAN, disabled by default.
- If "Enable CAN" is selected, Buffer Depth can be configured.
- Select and configure "Buffer Depth". The default value is 256.

Figure 3-12 CAN Configuration



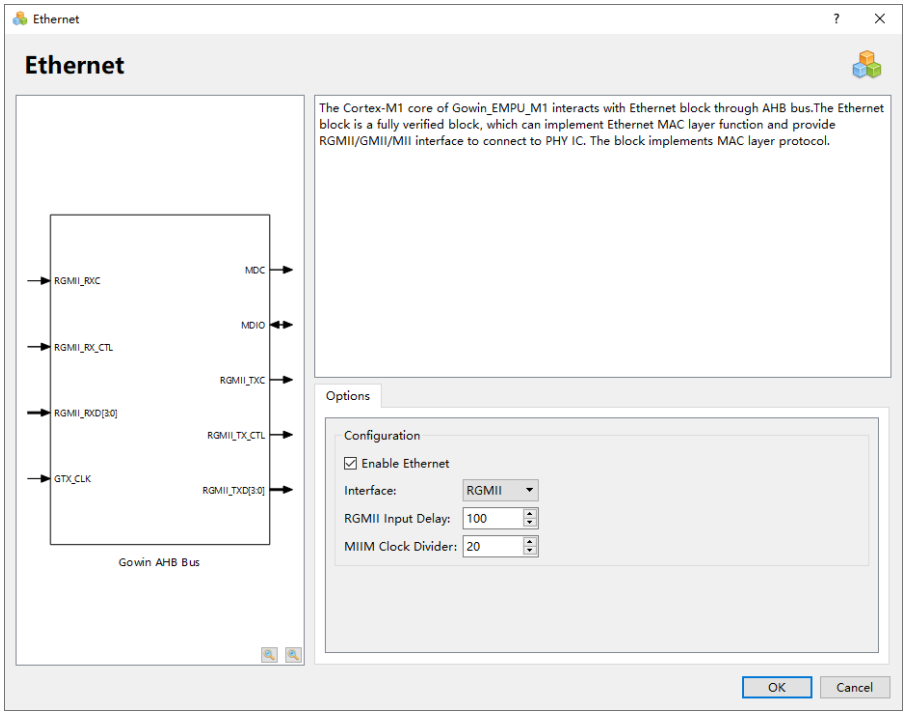
Ethernet

Double click to open Ethernet, as shown in Figure 3-13.

- If "Enable Ethernet" is selected, Gowin_EMPU_M1 supports Ethernet, disabled by default.
- If "Enable Ethernet" is selected, you can configure Interface, RGMII Input Delay, and MIIM Clock Divider.
  - Select "Interface", and you can configure RGMII, GMII, MII, or GMII/MII. The default is RGMII.
  - If "RGMII" is selected, you can configure RGMII Input Delay. The default value is 100.
  - If "MIIM Clock Divider" is selected, you can configure MIIM Clock Divider. The default value is 20.
- If "RGMII" or "GMII" is selected, 125MHz clock input must be provided to GTX_CLK.
- Gowin_EMPU_M1 Ethernet supports "lwIP" and "uIP" TCP/IP software stacks,
  see …\ref_design\MCU_RefDesign\MDK_RefDesign\cm1_tcpip for

reference.

Figure 3-13 Ethernet Configuration

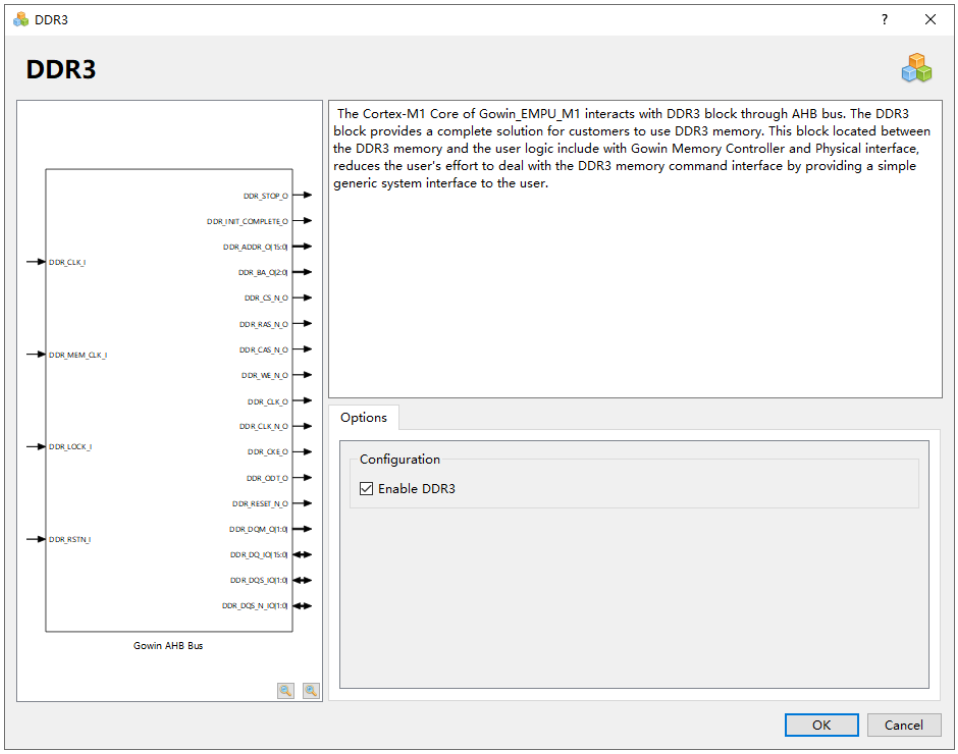


DDR3 Memory

Double click to configure DDR3 Memory, as shown in Figure 3-14.

- If "Enable DDR3" is selected, Gowin_EMPU_M1 supports DDR3 Memory, disabled by default.
- DDR_MEM_CLK_I: User-input memory interface frequency, and it is recommended to connect a 200MHz clock input.
- DDR_CLK_I: Reference clock input, 50MHz recommended.

Figure 3-14 DDR3 Memory Configuration



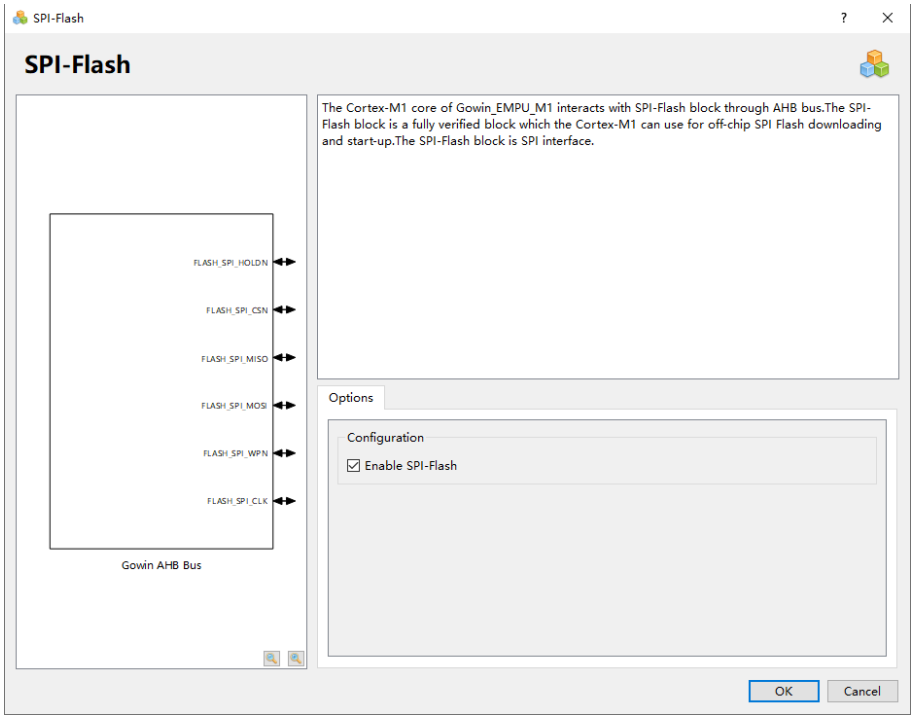
SPI-Flash Memory

SPI-Flash Memory supports the functions including download, and the read, write and erasure of Memory.

Double click to configure SPI-Flash Memory, as shown in Figure 3-15.

- If "Enable SPI-Flash" is selected, Gowin_EMPU_M1 supports SPI-Flash Memory, disabled by default.
- If Gowin_EMPU_M1 uses off-chip SPI-Flash Memory to download and start-up, "Enable SPI-Flash" must be selected.

Figure 3-15 SPI-Flash Memory Configuration

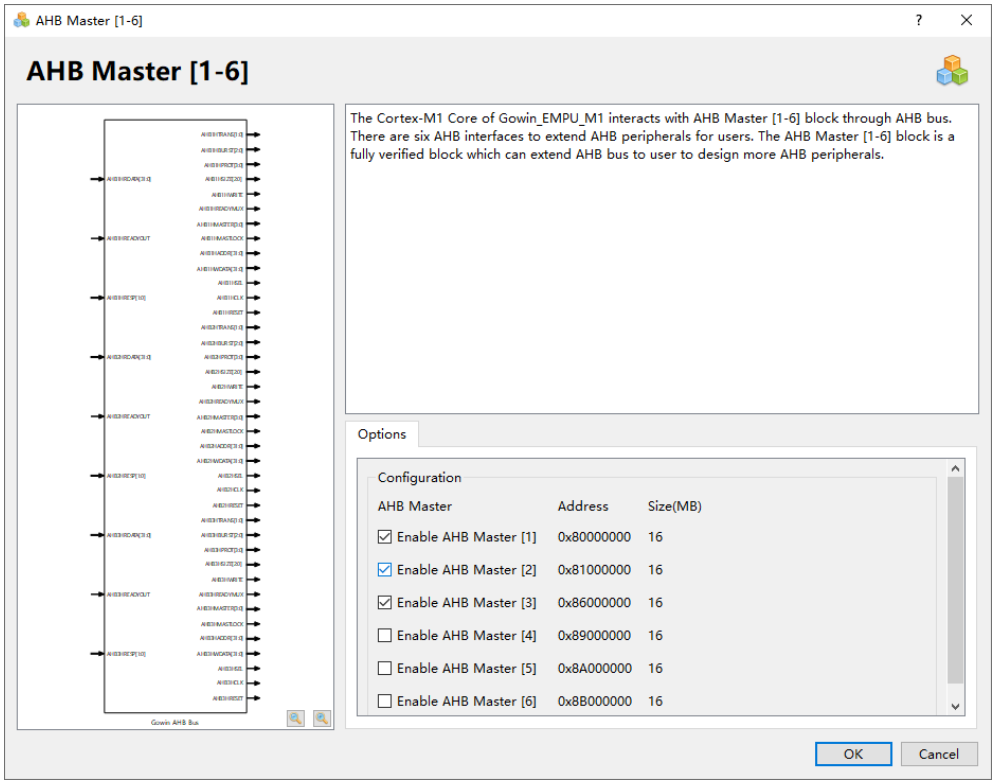


AHB Master [1-6]

Double click to open AHB Master[1-6], you can configure AHB Master [1-6] user AHB bus extension interface, as shown in Figure 3-16 ;

- If "Enable AHB Master [1]" is selected, Gowin_EMPU_M1 will support AHB Master [1] user AHB bus extension interface. You can extend AHB peripherals, disable by default.
- If "Enable AHB Master [2]" is selected, Gowin_EMPU_M1 will support AHB Master [2] user AHB bus extension interface. You can extend AHB peripherals, disable by default.
- If "Enable AHB Master [3]" is selected, Gowin_EMPU_M1 will support AHB Master [3] user AHB bus extension interface. You can extende AHB peripherals, disable by default.
- If "Enable AHB Master [4]" is selected, Gowin_EMPU_M1 will support AHB Master [4] user AHB bus extension interface. You can extend AHB peripherals, disable by default.
- If "Enable AHB Master [5]" is selected, Gowin_EMPU_M1 will support AHB Master [5] user AHB bus extension interface. You can extend AHB peripherals, disable by default.
- If "Enable AHB Master [6]" is selected, Gowin_EMPU_M1 will support AHB Master [6] user AHB bus extension interface. You can extend AHB peripherals, disable by default.

Figure 3-16 AHB Master [1-6]



The start address and the address space definition of AHB Master [1-6] user AHB bus extension interface are shown in Table 3-3.

Table 3-3 AHB Master [1-6] Address Definition

AHB interface	Start Address	Size (MB)
AHB Master [1]	0x80000000	16
AHB Master [2]	0x81000000	16
AHB Master [3]	0x86000000	16
AHB Master [4]	0x89000000	16
AHB Master [5]	0x8A000000	16
AHB Master [6]	0x8B000000	16

If you need to support external interrupt signal for the AHB external device extended on this AHB extension interface, please refer to the following two ways:

- Enable External Interrupts: Enable four external interrupt signals, connected to the interrupt signals of the extended peripherals.
- If the above 4 external interrupt signals are still not enough, enable GPIO to use GPIO[15:0] as the external interrupt signals.

UART

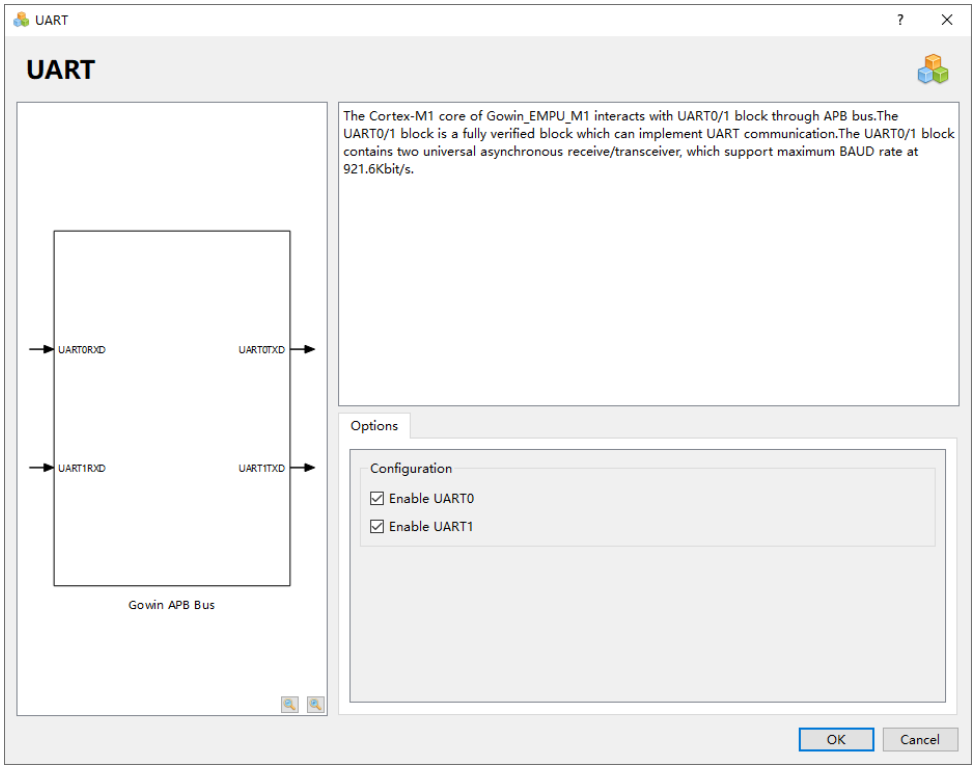
Double click UART0 or UART1, as shown in Figure 3-17.

- If "Enable UART0" is selected, Gowin_EMPU_M1 supports UART0,

disabled by default;

- If "Enable UART1" is selected, Gowin_EMPU_M1 supports UART1, disabled by default.

Figure 3-17 UART Configuration

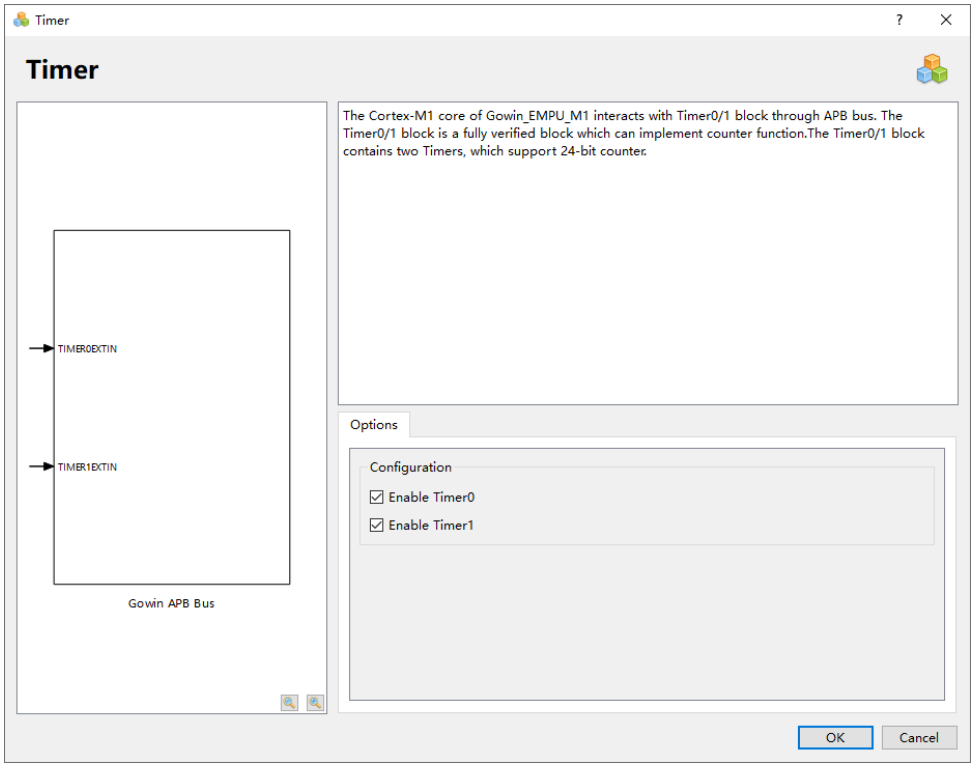


Timer

Double click to configure Timer0 or Timer1, as shown in Figure 3-18.

- If "Enable Timer0" is selected, Gowin_EMPU_M1 supports UART0, disabled by default.
- If "Enable Timer1" is selected, Gowin_EMPU_M1 supports Timer1, disabled by default.

Figure 3-18 Timer Configuration

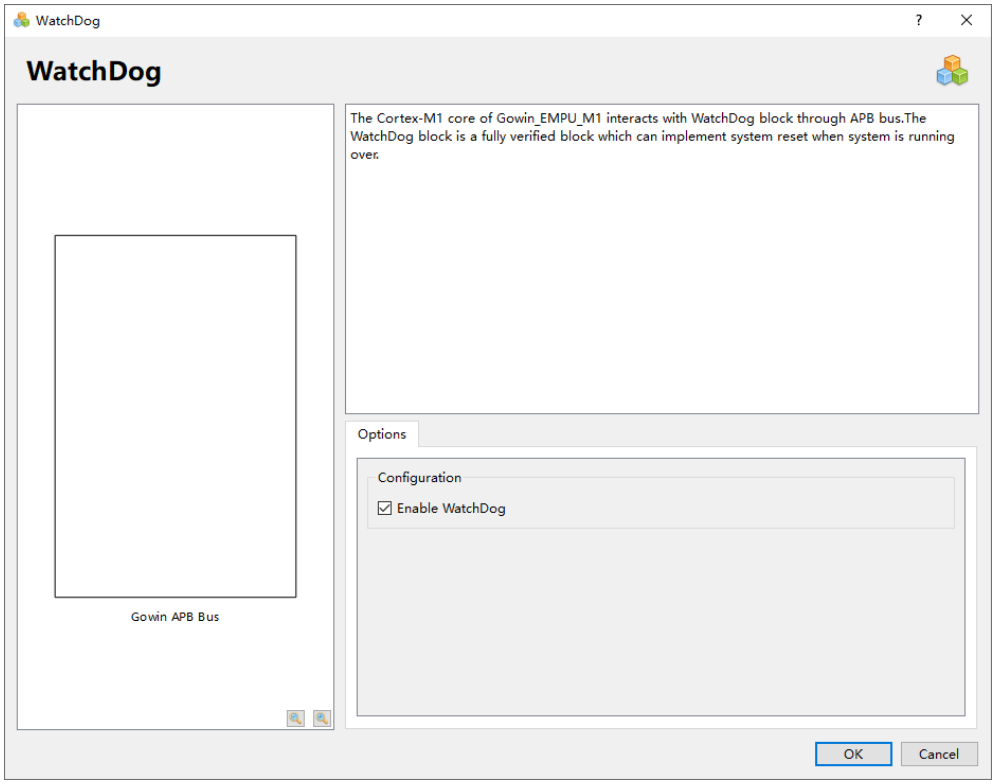


WatchDog

Double click to configure WatchDog, as shown in Figure 3-19.

If "Enable WatchDog" is selected, Gowin_EMPU_M1 supports WatchDog, disabled by default.

Figure 3-19 WatchDog Configuration



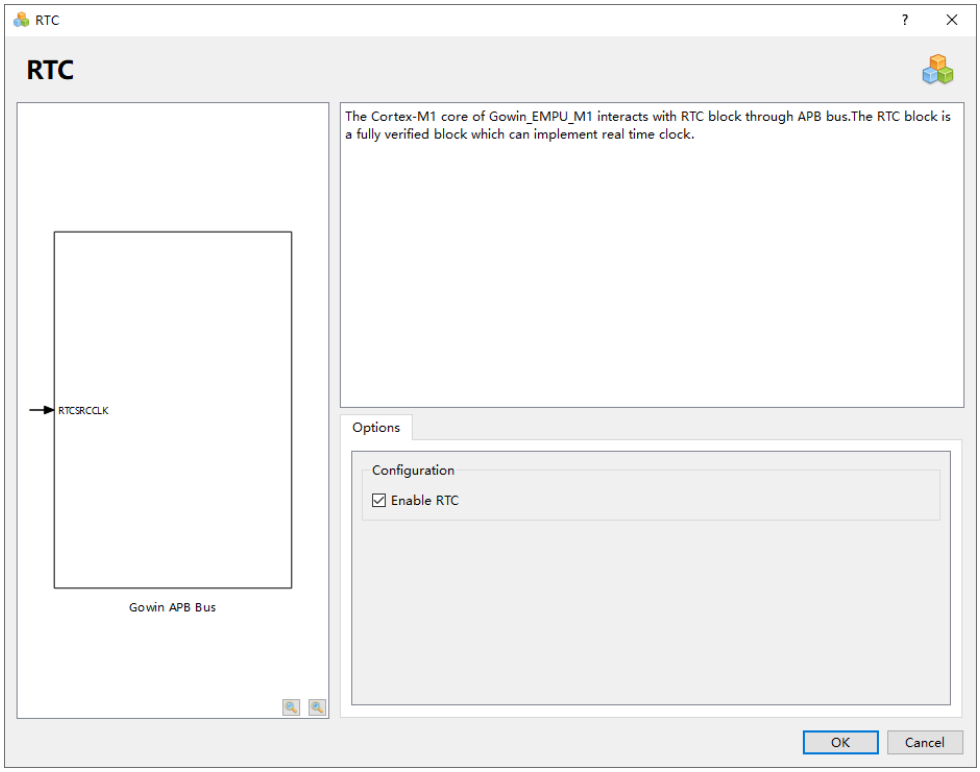
RTC

Double click to configure RTC, as shown in Figure 3-20.

If "Enable RTC" is selected, Gowin_EMPU_M1 supports RTC, disabled by default.

3.072MHz clock input must be provided to RTCSRCCL. The division in RTC is 1Hz.

Figure 3-20 RTC Configuration

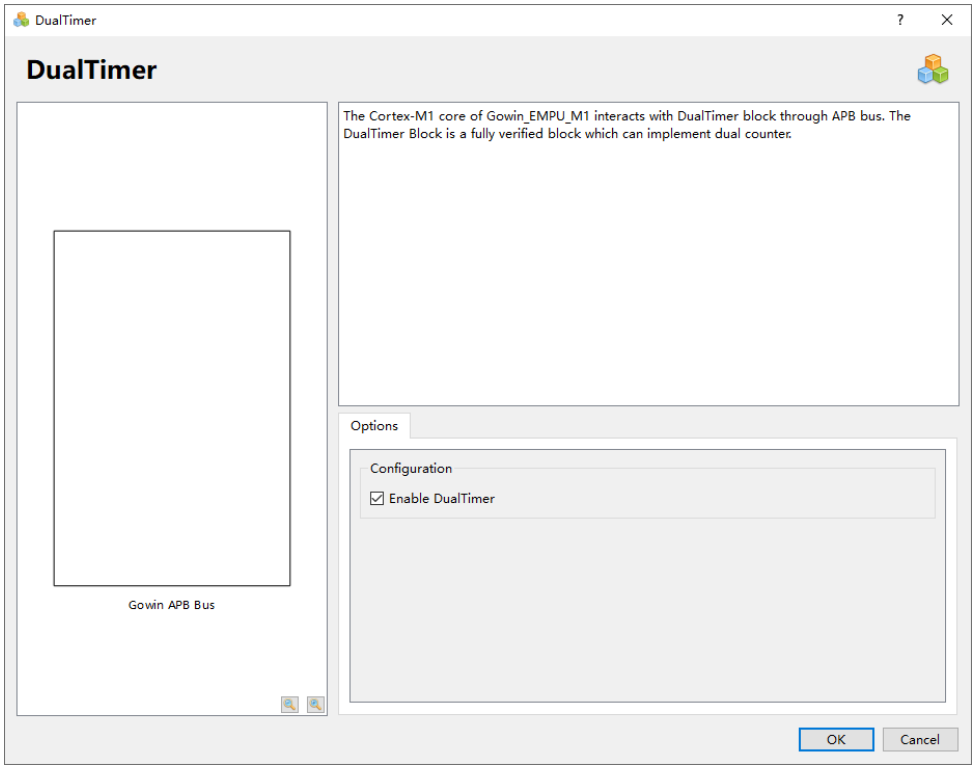


DualTimer

Double click to open DualTimer, as shown in Figure 3-21.

If "Enable DualTimer" is selected, Gowin_EMPU_M1 supports DualTimer, disabled by default.

Figure 3-21 DualTimer Configuration

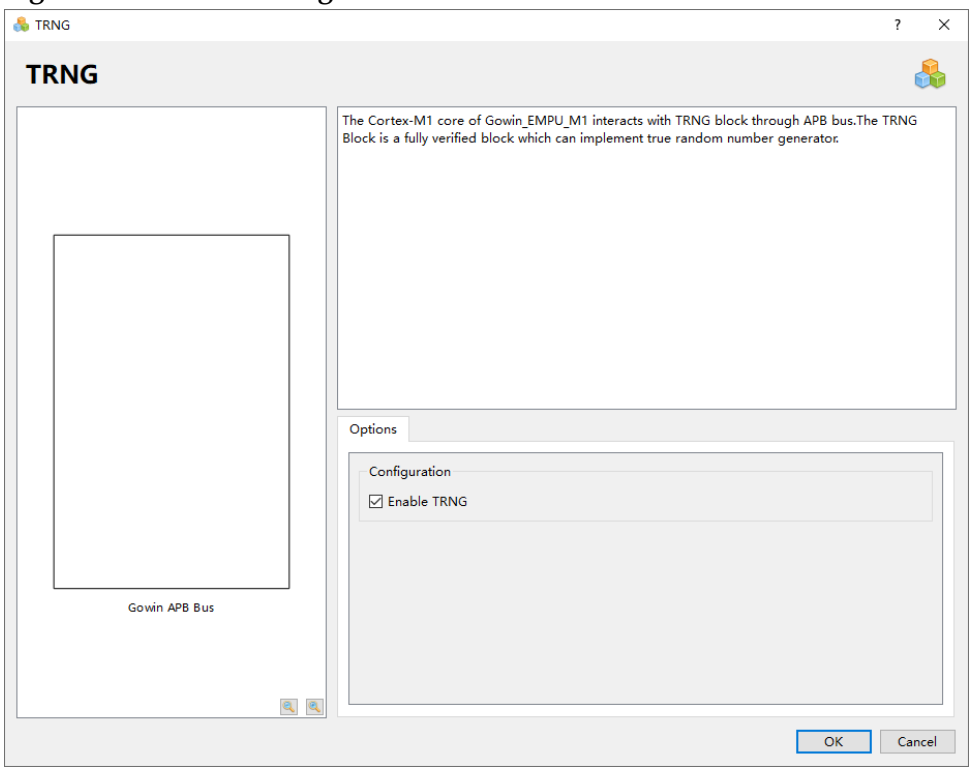


TRNG

Double click to open TRNG, as shown in Figure 3-22.

If "Enable TRNG" is selected, Gowin_EMPU_M1 supports TRNG, disabled by default.

Figure 3-22 TRNG Configuration

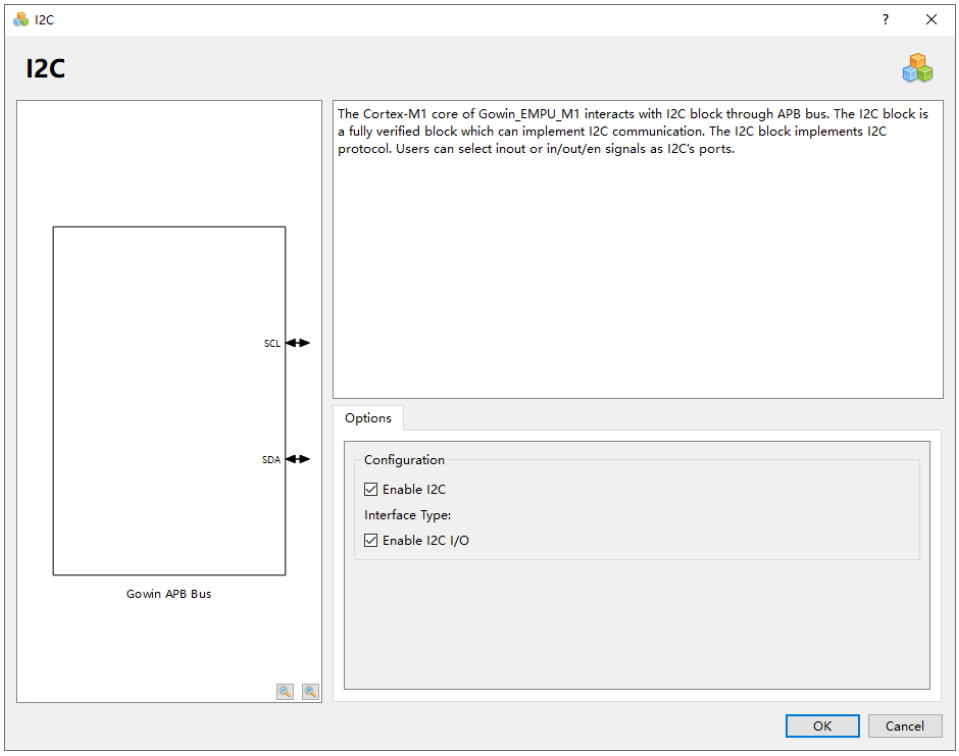


I2C

Double click to open I2C, and configure I2C Master, as shown in Figure 3-23.

- If "Enable I2C" is selected, Gowin_EMPU_M1 supports I2C Master, disabled by default.
- If "Enable I2C" is selected, I2C Master port type can be configured.
- If "Enable I2C I/O" is selected, I2C Master supports INOUT port type, or supports IN, OUT, EN, and supports INOUT by default.

Figure 3-23 I2C Configuration

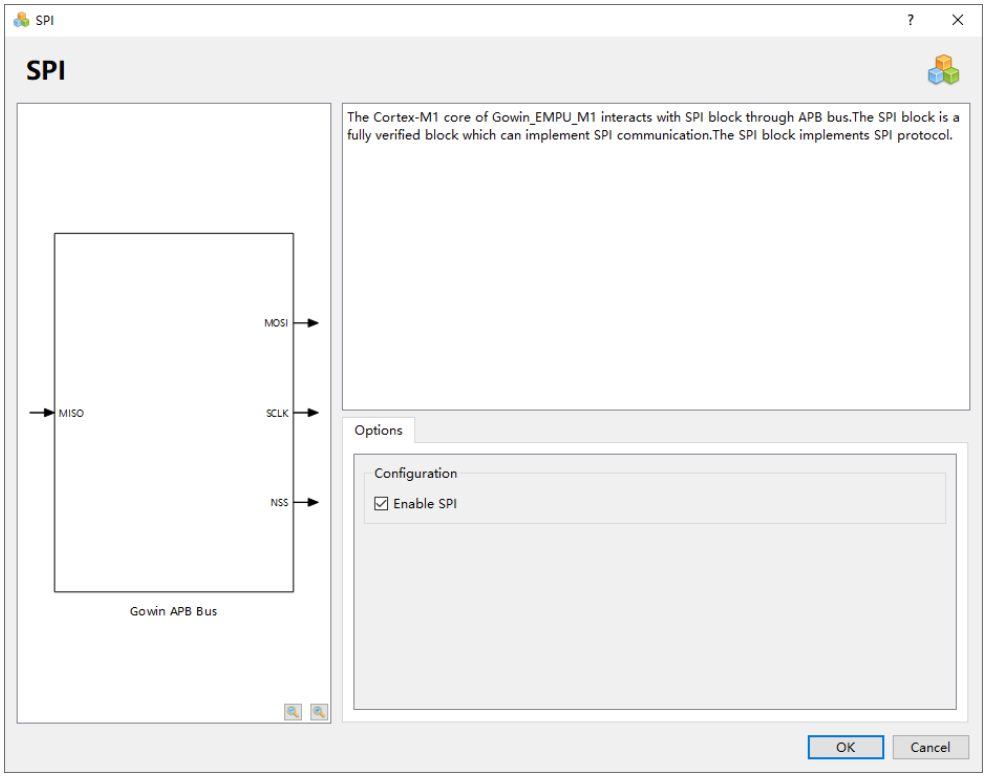


SPI

Double click to configure SPI Master, as shown in Figure 3-24.

If "Enable SPI" is selected, Gowin_EMPU_M1 supports SPI Master, disabled by default.

Figure 3-24 SPI Configuration

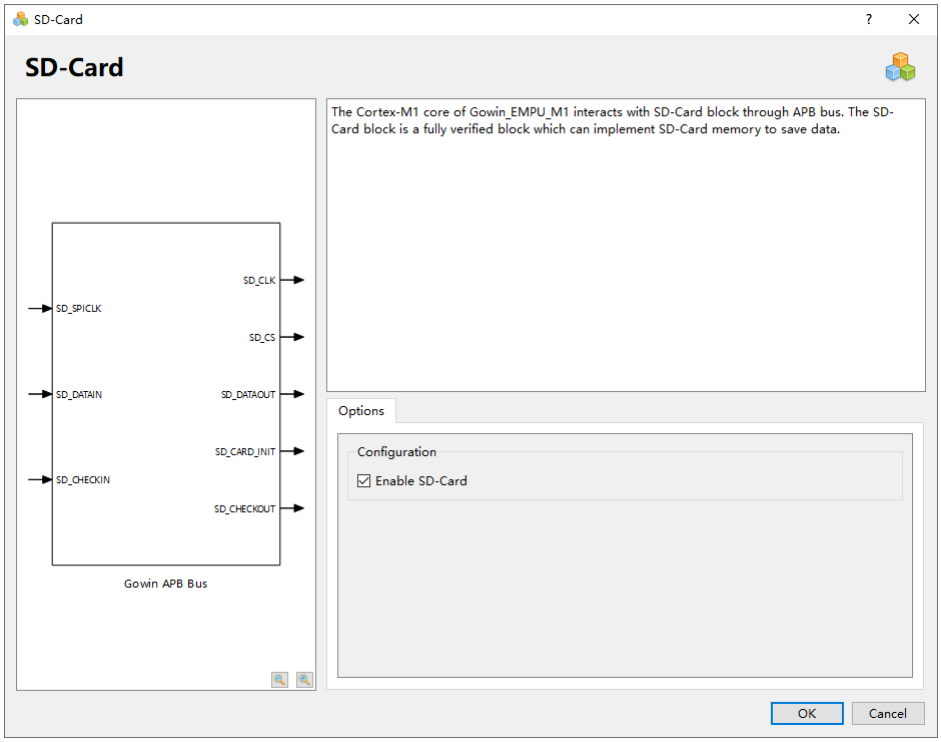


SD-Card Configuration

Double click to configure SD-Card, as shown in Figure 3-25.

- If "Enable SD-Card" is selected, Gowin_EMPU_M1 supports SD-Card, disabled by default.
- 30MHz clock input must be provided to SD_SPICLK.
- The supported SD-Card peripheral only supports FAT16 and SD-Cards up to 4GB.

Figure 3-25 SD-Card Configuration



APB Master [1-16]

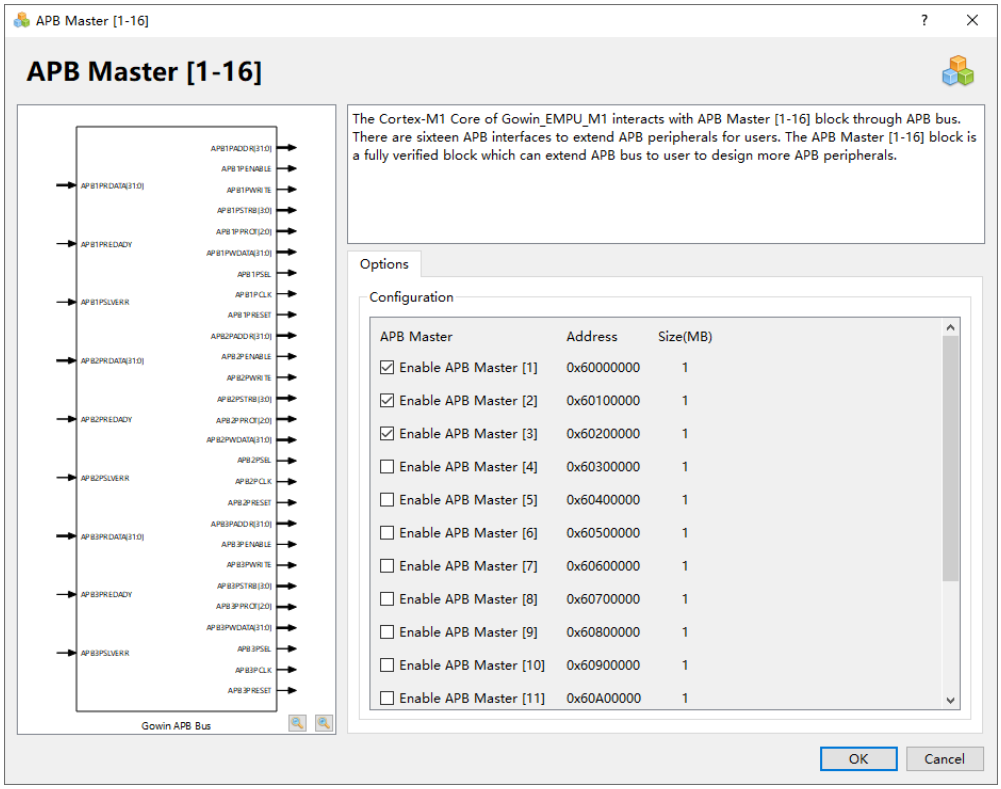
Double click to open APB Master [1-16], and configure APB Master [1-16], as shown in Figure 3-26.

- If "Enable APB Master [1]" is selected, Gowin_EMPU_M1 supports APB Master [1] user APB bus extension interface. You can extend APB peripherals, disabled by default.
- If "Enable APB Master [2]" is selected, Gowin_EMPU_M1 supports APB Master [2] user APB bus extension interface. You can extend APB peripherals, disabled by default.
- If "Enable APB Master [3]" is selected, Gowin_EMPU_M1 supports APB Master [3] user APB bus extension interface. You can extend APB peripherals, disabled by default.
- If "Enable APB Master [4]" is selected, Gowin_EMPU_M1 supports APB Master [4] user APB bus extension interface. You can extend APB peripherals, disabled by default.
- If "Enable APB Master [5]" is selected, Gowin_EMPU_M1 supports

APB Master [5] user APB bus extension interface. You can extend APB peripherals, disabled by default.

- If "Enable APB Master [6]" is selected, Gowin_EMPU_M1 supports APB Master [6] user APB bus extension interface. You can extend APB peripherals, disabled by default.
- If "Enable APB Master [7]" is selected, Gowin_EMPU_M1 supports APB Master [7] user APB bus extension interface. You can extend APB peripherals, disabled by default.
- If "Enable APB Master [8]" is selected, Gowin_EMPU_M1 supports APB Master [8] user APB bus extension interface. You can extend APB peripherals, disabled by default.
- If "Enable APB Master [9]" is selected, Gowin_EMPU_M1 supports APB Master [9] user APB bus extension interface. You can extend APB peripherals, disabled by default.
- If "Enable APB Master [10]" is selected, Gowin_EMPU_M1 supports APB Master [10] user APB bus extension interface. You can extend APB peripherals, disabled by default.
- If "Enable APB Master [11]" is selected, Gowin_EMPU_M1 supports APB Master [11] user APB bus extension interface. You can extend APB peripherals, disabled by default.
- If "Enable APB Master [12]" is selected, Gowin_EMPU_M1 supports APB Master [12] user APB bus extension interface. You can extend APB peripherals, disabled by default.
- If "Enable APB Master [13]" is selected, Gowin_EMPU_M1 supports APB Master [13] user APB bus extension interface. You can extend APB peripherals, disabled by default.
- If "Enable APB Master [14]" is selected, Gowin_EMPU_M1 supports APB Master [14] user APB bus extension interface. You can extend APB peripherals, disabled by default.
- If "Enable APB Master [15]" is selected, Gowin_EMPU_M1 supports APB Master [15] user APB bus extension interface. You can extend APB peripherals, disabled by default.
- If "Enable APB Master [16]" is selected, Gowin_EMPU_M1 supports APB Master [16] user APB bus extension interface. You can extend APB peripherals, disabled by default.

Figure 3-26 APB Master [1-16] Configuration



The start address and the address space definition of APB Master [1-16] user APB bus extension interface are shown in Table 3-4.

Table 3-4 APB Master [1-16] Address Definition

APB bus interface	Start Address	Size (MB)
APB Master [1]	0x60000000	1
APB Master [2]	0x60100000	1
APB Master [3]	0x60200000	1
APB Master [4]	0x60300000	1
APB Master [5]	0x60400000	1
APB Master [6]	0x60500000	1
APB Master [7]	0x60600000	1
APB Master [8]	0x60700000	1
APB Master [9]	0x60800000	1
APB Master [10]	0x60900000	1
APB Master [11]	0x60A00000	1
APB Master [12]	0x60B00000	1
APB Master [13]	0x60C00000	1
APB Master [14]	0x60D00000	1
APB Master [15]	0x60E00000	1
APB Master [16]	0x60F00000	1

If you need to support external interrupt signal for the APB external device extended on this APB extension interface, please refer to the following two ways:

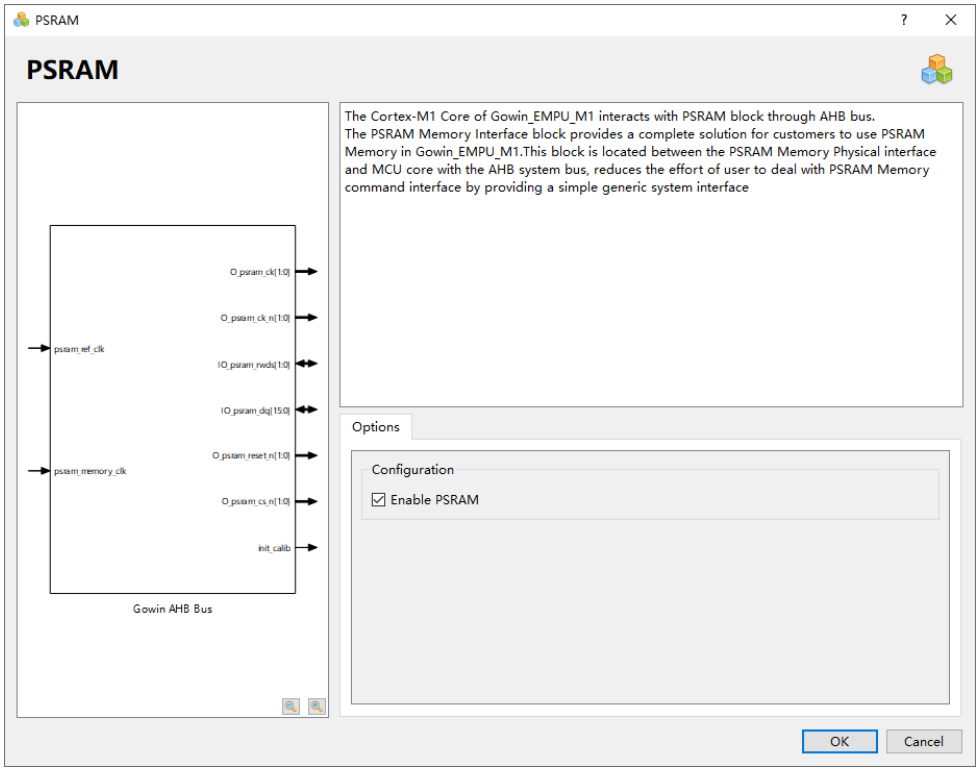
- Enable External Interrupts: Enable four external interrupt signals, connected to the interrupt signals of the extended peripherals.
- If the above 4 external interrupt signals are still not enough, enable GPIO to use GPIO[15:0] as the external interrupt signals.

PSRAM Configuration

Double click to open PSRAM, and configure PSRAM, as shown in Figure 3-27.

- If "Enable PSRAM" is selected, Gowin_EMPU_M1 supports PSRAM, disabled by default.
- Only the following devices support Gowin_EMPU_M1 PSRAM:
  - GW2AR-18 version C QFN88P
  - GW2AR-18 version C QFN88PF
  - GW2AR-18 version C eLQFP144P
  - GW2AR-18 version C eLQFP144PF
  - GW2ANR-18 version C QFN88

Figure 3-27 PSRAM Configuration



3.3 User Design

- After Gowin_EMPU_M1 configuration, you can generate Gowin_EMPU_M1 hardware design.
- Instantiate Gowin_EMPU_M1 Top Module.
- Import user designs and connect it with Gowin_EMPU_M1 to form a complete RTL design.

3.4 Constraint

After the user RTL design is completed, physical constraints can be generated according to the used development board and the IO.

Timing constraints file can be generated according to timing requirements.

How to generate physical constraints, please refer to *SUG935, Gowin Design Physical Constraints User Guide*, *SUG1018, Arora V Design Physical Constraints User Guide*.

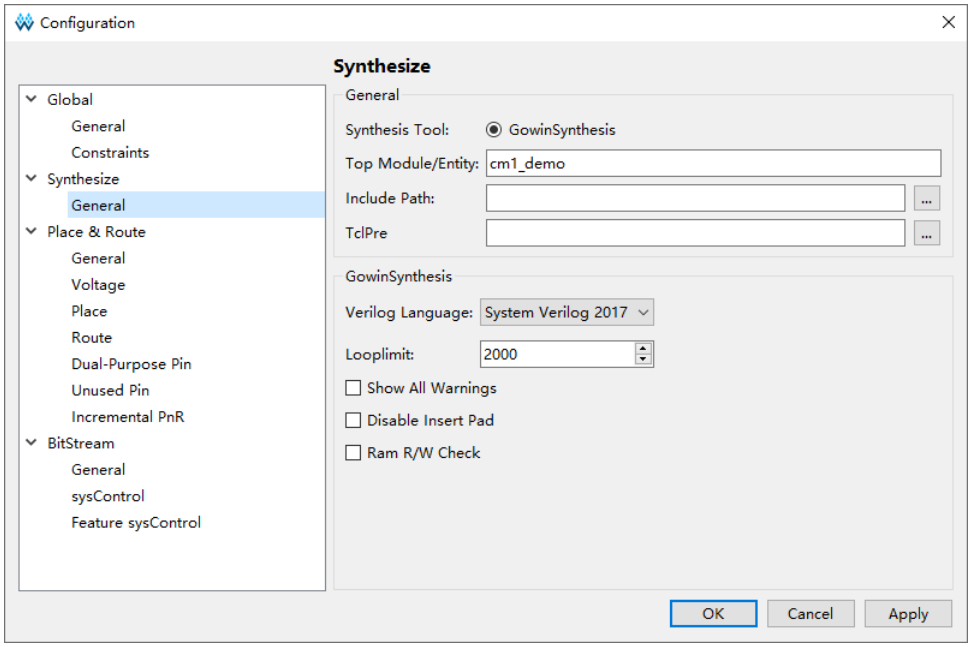
3.5 Configuration

3.5.1 Synthesis Configuration

The "Synthesize > General" configuration is as shown in Figure 3-28.

- Configure "Top Module/Entity" according to the top module name in the design.
- Configure "Include Path" according to the actual file path in the design.
- Configure "Verilog Language" according to System Verilog 2017.

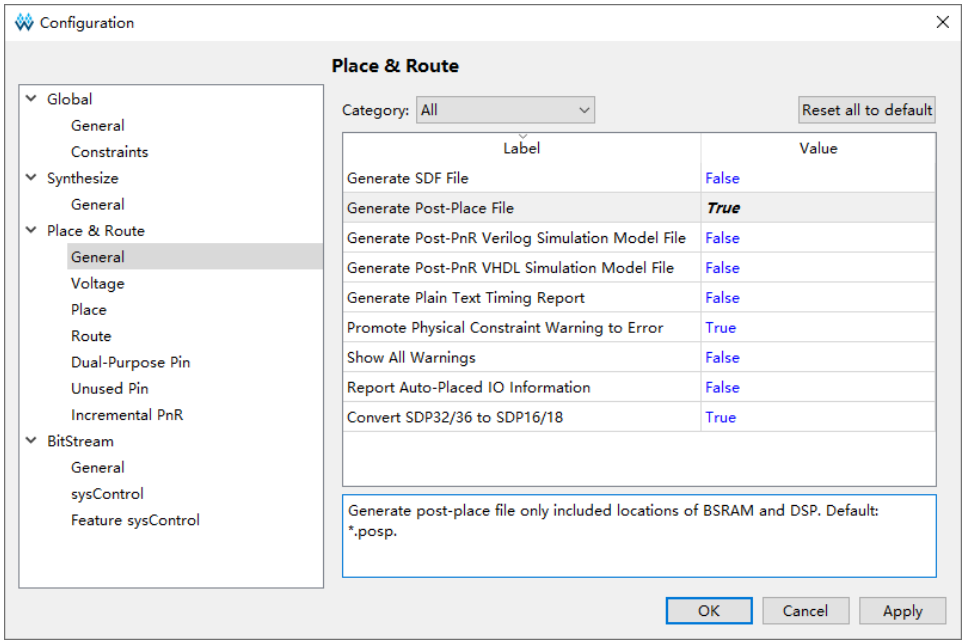
Figure 3-28 Synthesis Configuration



3.5.2 Post-Place File Configuration

If you use the download method of automatically merging Gowin_EMPU_M1 software programming design and hardware design, you need to configure "Place & Route > General > Generate Post-Place File" to generate a Post-Place File, as shown in Figure 3-29.

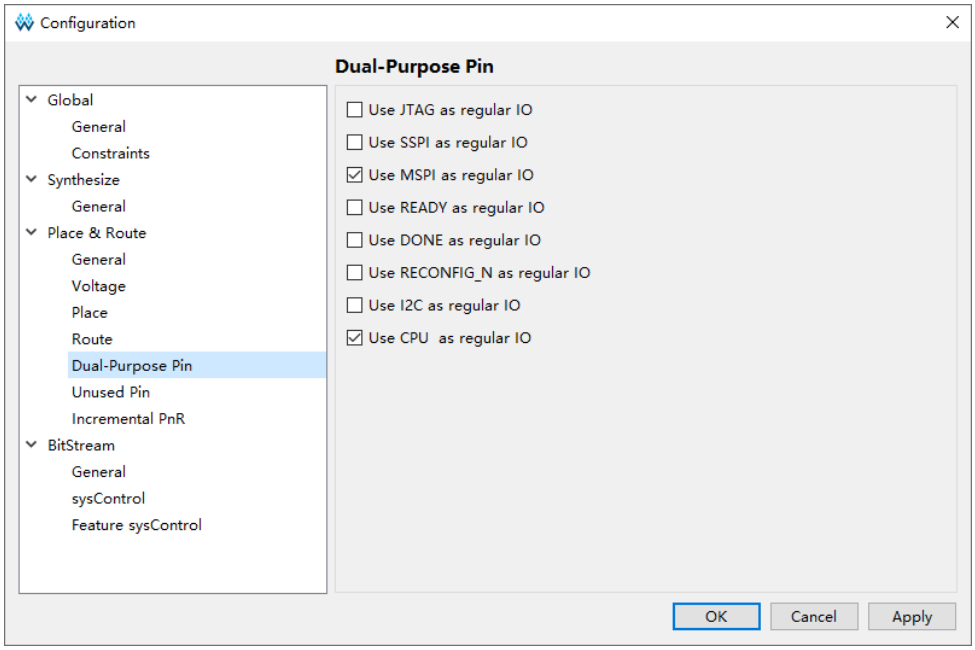
Figure 3-29 Post-Place File Configuration



3.5.3 Dual-Purpose Pin Configuration

If Gowin_EMPU_M1 uses off-chip SPI-Flash Memory to download and start-up, you need to configure "Place & Route > Dual-Purpose Pin" to use MSPI and CPU IO as regular IO; otherwise, there is no need to configure dual-purpose, as shown in Figure 3-30

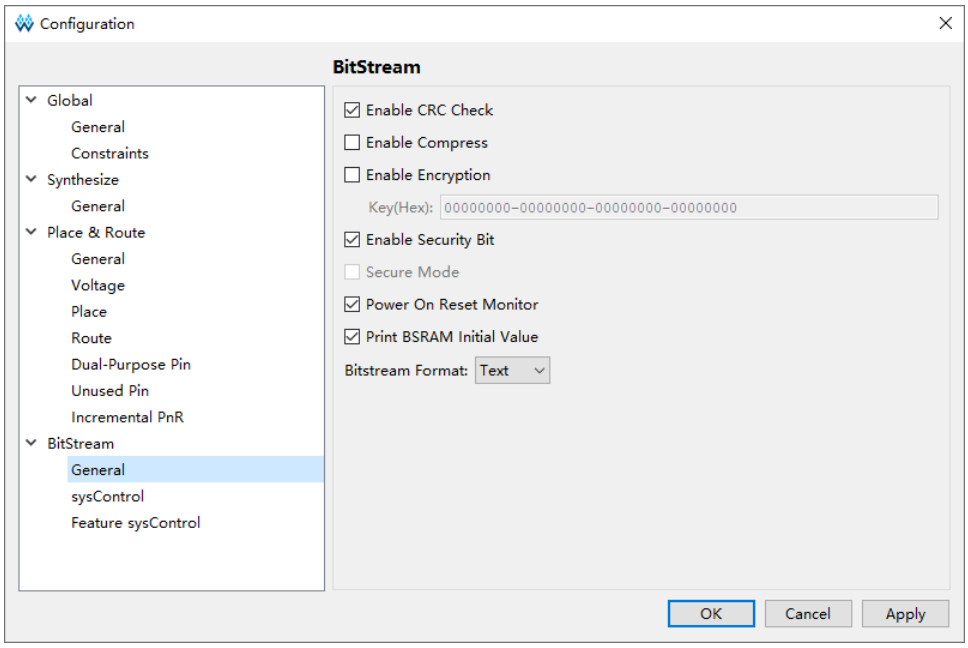
Figure 3-30 Dual-Purpose Pin Configuration



3.5.4 BitStream Configuration

Configure "Bitstream > General" and enable "Print BSRAM Initial Value", as shown in Figure 3-31.

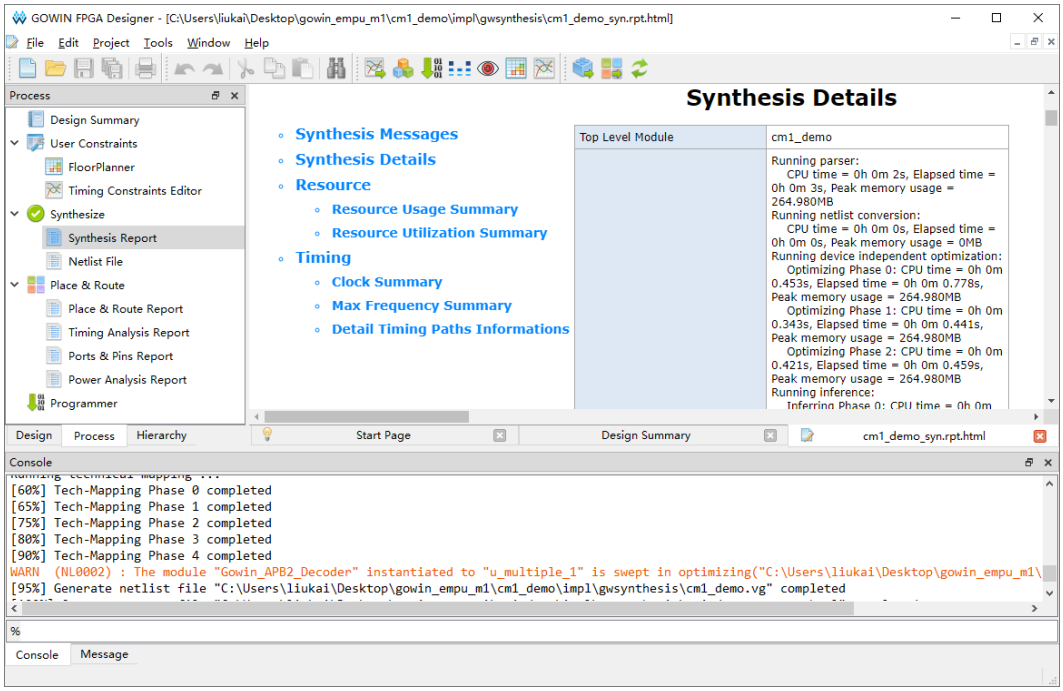
Figure 3-31 BitStream Configuration



3.6 Synthesize

Run GowinSynthesis, the synthesis tool, to complete the synthesis of RTL design, as shown in Figure 3-32.

Figure 3-32 Synthesis Configuration

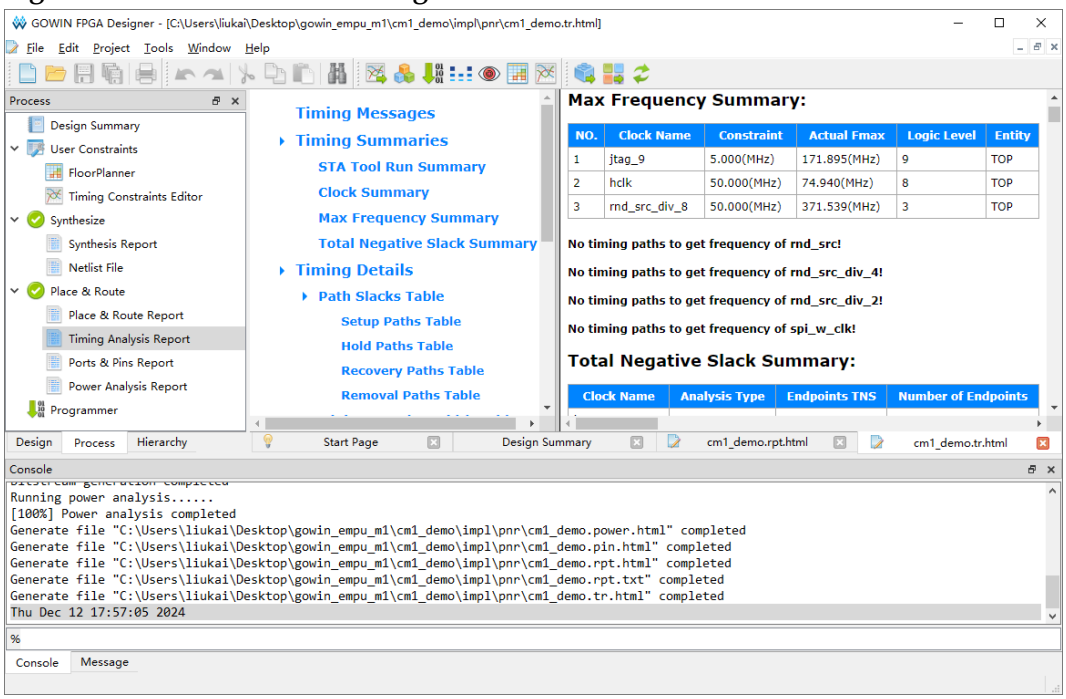


For the synthesis tool usage, please refer to *SUG100, Gowin Software User Guide*.

3.7 Place & Route

Run "Place & Route", the Place & Route tool, to generate the bitstream files, as shown in Figure 3-33.

Figure 3-33 Place & Route Configuration



For the Place & Route tool usage, please refer to *SUG100, Gowin Software User Guide*.

3.8 Download

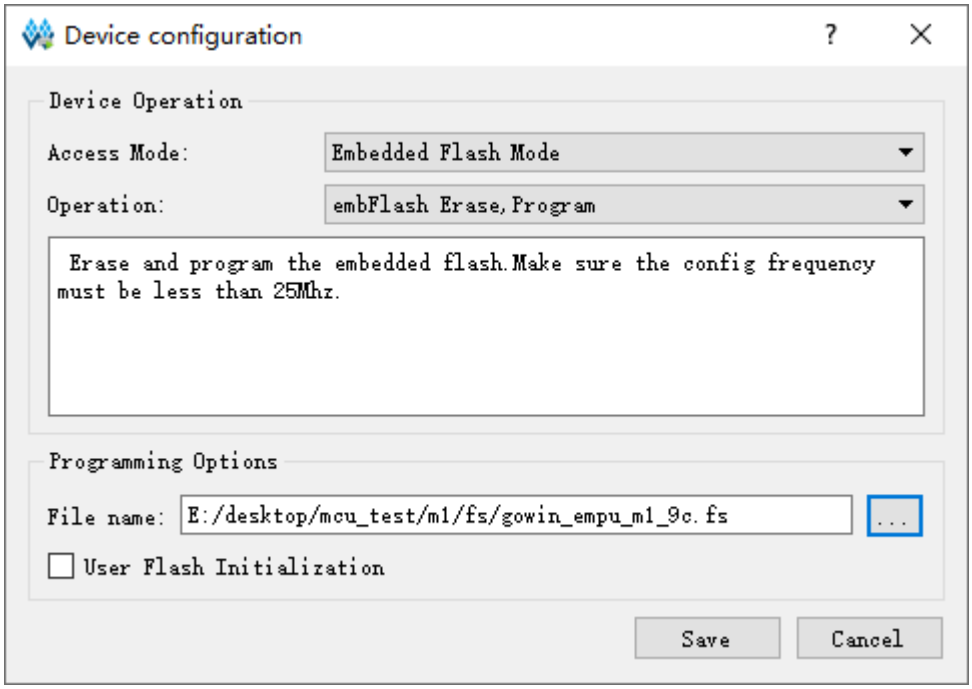
Run the "Programmer", the download tool, to download Hardware Design the bitstream file.

Run Programmer in Gowin Software or software installation path, click "Edit/Configure Device" or Configure Device "  " in the tool bar to open the "Device configuration" .

If "ITCM Select" is configured as "Internal Instruction Memory", then configuration options for GW1N/R-9 products are as shown in Figure 3-34.

- Select "Embedded Flash Mode" in "Access Mode" drop-down list.
- Select "embFlash Erase, Program" or "embFlash Erase, Program, Verify" in "Operation" drop-down list.
- Import the hardware design bitstream file to download in "Programming Options > File name" option.
- Click "Save" to complete the configuration of the hardware design bitstream file.

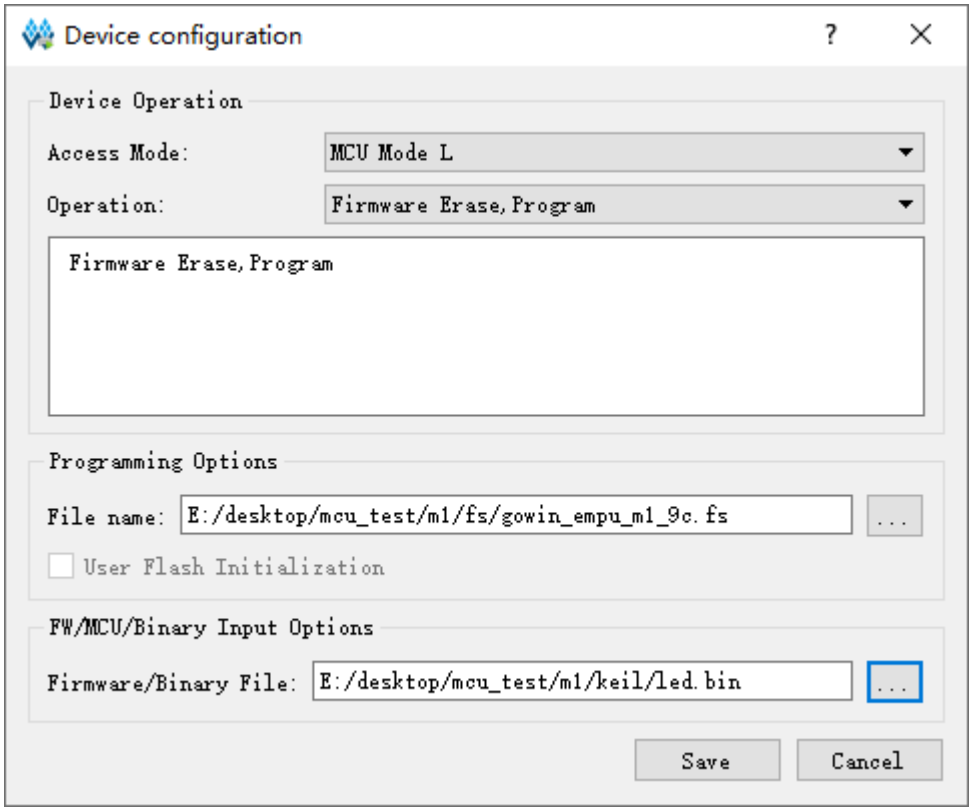
Figure 3-34 Embedded Flash Mode Configuration for GW1N/R-9



If "ITCM Select" is configured as "External Instruction Memory", and select embedded UserFlash as instruction memory, then configuration options for GW1N/R-9 are as shown in Figure 3-35.

- Select "MCU Model L" in "Access Mode" drop-down list.
- Select "Firmware Erase, Program" or "Firmware Erase, Program, Verify" in "Operation" drop-down list.
- Import the hardware design bitstream files to download in "Programming Options > File name" option.
- Import the software programming design BIN files to download in "FW/MCU/Binary Input Options > Firmware/Binary File" option.
- Click "Save" to complete the configuration of the hardware design bitstream files and software programming design BIN files.

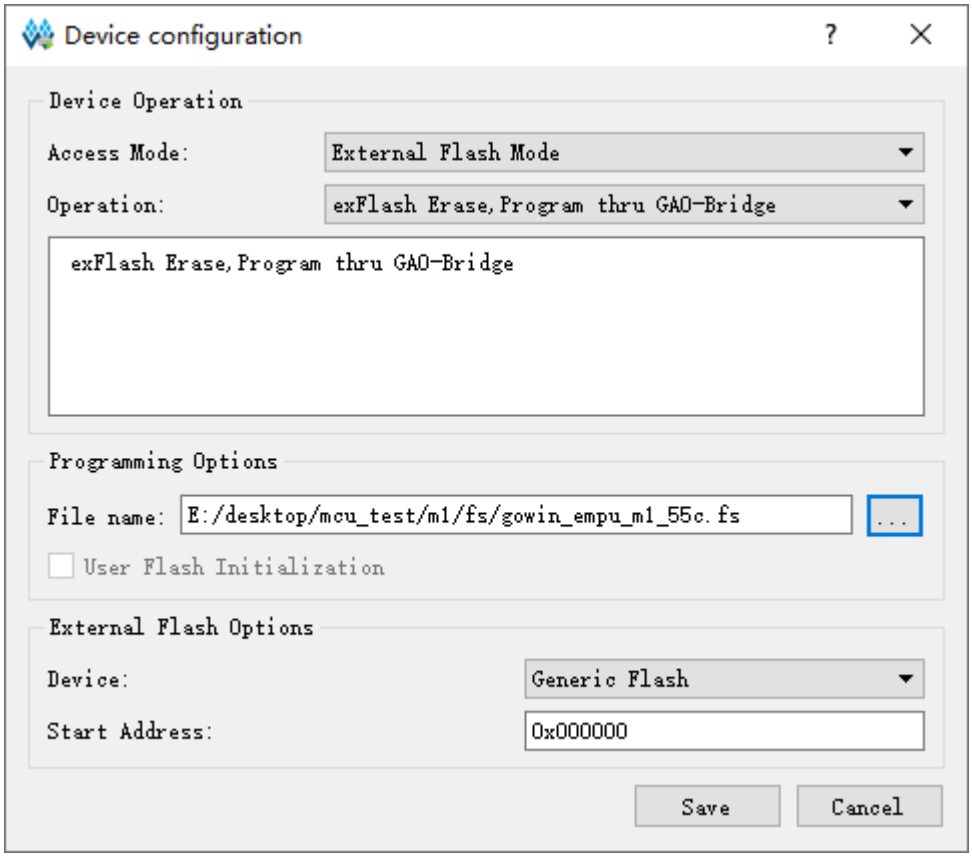
Figure 3-35 MCU Mode L Configuration for GW1N/R-9



Configuration options for GW2AN-9X/18X, GW2A/R/NR-18, and GW2A/N-55 are as shown in Figure 3-36.

- Select "External Flash Mode" in "Access Mode" drop-down list.
- Select "exFlash Erase, Program thru GAO-Bridge" or "exFlash Erase, Program, Verify thru GAO-Bridge" in "Operation" drop-down list.
- Import the hardware design bitstream file to download in "Programming Options > File name" option.
- Select "Generic Flash" in "External Flash Options".
- Configure the start address as "0x000000" in "External Flash Options > Start Address" option.
- Click "Save" to complete the configuration of the hardware design bitstream file.

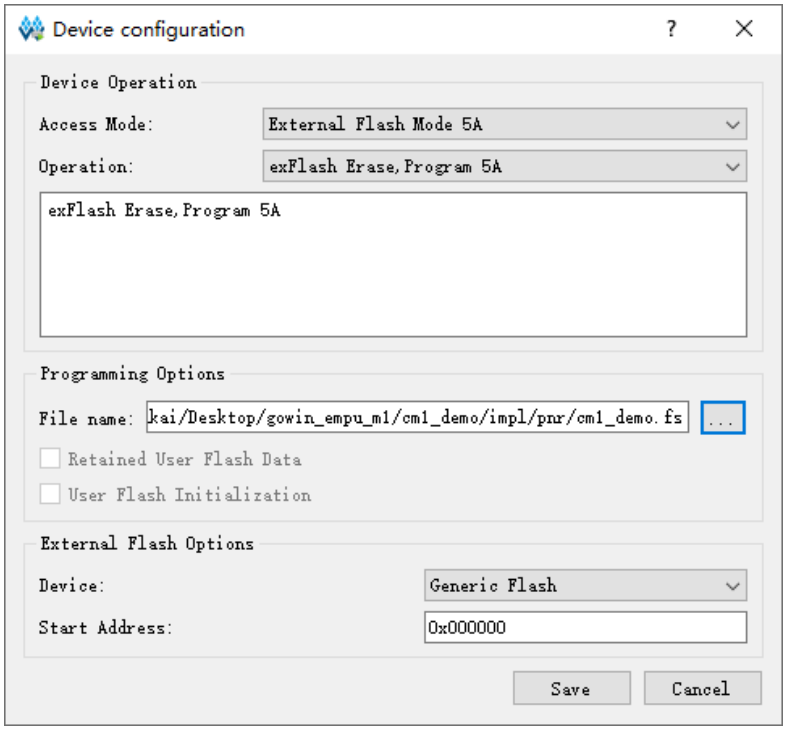
Figure 3-36 External Flash Mode Configuration for GW2AN-9X/18X, GW2A/R/NR-18, and GW2A/N-55



Configuration options for Arora V products are as shown in Figure 3-36.

- Select "External Flash Mode 5A" in "Access Mode" drop-down list.
- Select "exFlash Erase, Program 5A" or "exFlash Erase, Program, Verify 5A" in "Operation" drop-down list.
- Import the hardware design bitstream file to download in "Programming Options > File name" option.
- Select "Generic Flash" in "External Flash Options".
- Configure the start address as "0x000000" in "External Flash Options > Start Address" option.
- Click "Save" to complete the configuration of the hardware design bitstream file.

Figure 3-37 External Flash Mode Configuration for Arora V



After device configuration, click Program/Configure " " in the Programmer toolbar to complete downloading bitstream files in hardware design (If GW1N/R-9 use MCU Mode L, then download software programming BIN files at the same time).

For the usage of Programmer, please see *SUG502, Gowin Programmer User Guide*.

4 Reference Design

Gowin_EMPU_M1 provides hardware reference design:

- …\ref_design\FPGA_RefDesign\DK_START_DDR2_GW5A25_V1.0\gowin_empu_m1
- …\ref_design\FPGA_RefDesign\DK_START_GW1N9_V2.1\gowin_empu_m1
- …\ref_design\FPGA_RefDesign\DK_START_GW2A18_V2.0\gowin_empu_m1
- …\ref_design\FPGA_RefDesign\DK_START_GW2A55_V1.3\gowin_empu_m1
- …\ref_design\FPGA_RefDesign\DK_START_GW2AR18_V1.1\gowin_empu_m1
- …\ref_design\FPGA_RefDesign\DK_START_GW5A25_V2.0\gowin_empu_m1
- …\ref_design\FPGA_RefDesign\DK_START_GW5AST138_V1.0\gowin_empu_m1
- …\ref_design\FPGA_RefDesign\Tang_MEGA_138K_Pro_Dock\gowin_empu_m1
- …\ref_design\FPGA_RefDesign\DK_DP_GW5AT60_V1.0\gowin_empu_m1

Gowin_EMPU_M1provides solution reference design:

- …\solution\Embedded_Memory\ref_design\FPGA_RefDesign\gowin_empu_m1
- …\solution\External_Memory\ref_design\FPGA_RefDesign\gowin_empu_m1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