Gowin_EMPU_M1 Software Programming
Reference Manual

IPUG533-2.2E,01/17/2025

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Revision History

Date	Version	Description
02/19/2019	1.0E	Initial version published.
07/18/2019	1.1E	MCU hardware design and software programming design support extended peripherals: CAN, Ethernet, SPI-Flash, RTC, DualTimer, TRNG, I2C, SPI, SD-Card.
08/18/2019	1.2E	● MCU hardware design and software programming design support extended peripheral: DDR3 Memory. ● Known issues of ITCM, DTCM Size and IDE fixed.
09/27/2019	1.3E	● MCU hardware design and software programming design support read, write and erasure of SPI-Flash. ● MCU software programming design supports a continuous multi-byte read and write of I^2C. ● Fixed known issues of address mapping of AHB2 and APB2 extended interface in MCU software programming design. ● Fixed known issues of continuous read and write of DDR3 Memory in MCU software programming design.
12/06/2019	1.4E	● MCU hardware design and software programming design supports PSRAM. ● MCU compiling software GMD V1.0 updated. ● RTOS reference design updated. ● Hardware and software reference design of AHB2 and APB2 extension bus interface added.
03/09/2020	1.5E	MCU software programming design supports the read and write of SD-Card.
06/12/2020	1.6E	● MCU supports for external instruction memory. ● MCU supports for external data memory. ● Extension of 6 AHB bus interfaces. ● Extension of 16 APB bus interfaces. ● GPIO supports multiple interface types. ● I^2C supports multiple interface types.
07/16/2021	1.7E	● Known issues of read and write for SPI full-duplex fixed. ● The version of MCU updated.
05/11/2023	1.8E	● Extended external interrupt inputs supported. ● Arora V FPGA products supported. ● Software programming development library updated. ● Bootloader updated. ● Software programming reference design updated. ● RT-Thread Nano software reference design added. ● TCP/IP protocol stack software reference design added.
07/21/2023	1.9E	Tested software version updated.
03/07/2024	2.0E	● Software programming library updated. ● Software programming reference design updated.
06/28/2024	2.1E	● SPI Flash Memory driver function updated. ● QSPI Flash Memory driver function supported.
01/17/2025	2.2E	● The interrupt initialization issue of GPIO peripheral driver fixed.

Date	Version	Description
		● Software programming reference design updated.

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1 Software Programming Library

Gowin_EMPU_M1 offers software programming library: …\library.

Click this link to get the software programming library.

Three Gowin_EMPU_M1 software programming methods are supported:

- Microcontroller Unit software programming
- Embedded RTOS software programming
- Protocol stack software programming

1.1 Cortex-M1 Core Software Programming

The Microcontroller Unit software programming method provided in the Gowin_EMPU_M1 software programming library is shown in Table 1-1.

Table 1-1 Cortex-M1 Core Software Programming

Library File	Description
System Definition	
startup_GOWIN_M1.s	Cortex-M1 core bootloader
core_cm1.h	Cortex-M1 core register definition
GOWIN_M1.h	Definitions of interrupt vector table, peripheral register, and address mapping
system_GOWIN_M1.c system_GOWIN_M1.h	Cortex-M1 core system initialization and system clock definition
Linker Definition	
GOWIN_M1_flash_burn.ld GOWIN_M1_flash_xip.ld	GMD Flash linker: burn: Flash boot-up, ITCM running xip: Flash boot-up and running.
Peripheral Driver Definition	
GOWIN_M1_gpio.c GOWIN_M1_gpio.h	GPIO driver function definition
GOWIN_M1_can.c GOWIN_M1_can.h	CAN driver function definition
GOWIN_M1_ethernet.c GOWIN_M1_ethernet.h	Ethernet driver function definition

Library File	Description
System Definition	
GOWIN_M1_ddr3.c GOWIN_M1_ddr3.h	DDR3 memory driver function definition
GOWIN_M1_psram.c GOWIN_M1_psram.h	PSRAM memory driver function definition
GOWIN_M1_spi_flash.c GOWIN_M1_spi_flash.h	SPI-Flash memory read, write and erasure driver definitions
GOWIN_M1_qspi_flash.c GOWIN_M1_qspi_flash.h	QSPI-Flash Memory driver function definition
GOWIN_M1_timer.c GOWIN_M1_timer.h	Timer driver function definition
GOWIN_M1_wdog.c GOWIN_M1_wdog.h	Watch Dog driver function definition
GOWIN_M1_uart.c GOWIN_M1_uart.h	UART driver function definition
GOWIN_M1_rtc.c GOWIN_M1_rtc.h	RTC driver function definition
GOWIN_M1_trng.c GOWIN_M1_trng.h	TRNG driver function definition
GOWIN_M1_dualtimer.c GOWIN_M1_dualtimer.h	DualTimer driver function definition
GOWIN_M1_i2c.c GOWIN_M1_i2c.h	I2C Master driver function definition
GOWIN_M1_spi.c GOWIN_M1_spi.h	SPI Master driver function definition
GOWIN_M1_sdcard.c GOWIN_M1_sdcard.h	SD-Card driver function definition
GOWIN_M1_misc.c GOWIN_M1_misc.h	Interrupt priority management and SysTick definition
GOWIN_M1_it.c GOWIN_M1_it.h	Interrupt handling function definition
Middleware Definition	
retarget.c uart.c uart.h	Retarget UART printf function URAT initialization definition
malloc.c malloc.h	Dynamic memory management
gpio.c gpio.h	GPIO initialization definition
delay.c delay.h	Delay function definition

1.2 Embedded Operating System Software Programming

Gowin_EMPU_M1 supports the following embedded RTOS software programming:

- uC/OS-III
- FreeRTOS
- RT-Thread Nano version

1.3 Protocol Stack Software Programming

Gowin_EMPU_M1 supports Ethernet TCP/IP protocol stack software programming, provides open-source LwIP protocol stack and uIP protocol stack.

The LwIP protocol stack is a small open-source TCP/IP protocol stack that can run with or without an operating system. It can reduce memory usage while maintaining the main functions of the TCP protocol.

The uIP protocol stack is a simple embedded network protocol stack that does not require support from an operating system. It is programmed in an event-driven manner and implements four basic protocols: ARP, IP, ICMP, and TCP.

2 Memory System

2.1 Standard Peripherals Memory Mapping

The definition of memory mapping addresses of Gowin_EMPU_M1 standard peripherals are as shown in Table 2-1.

Table 2-1 Standard Peripheral Memory Mapping Definitions

Standard Peripheral	Type	Address Mapping	Description
ITCM	–	0x00000000	1KB, 2KB, 4KB, 8KB, 16KB, 32KB, 64KB, 128KB, 256KB, 512KB
DTCM	–	0x20000000	1KB, 2KB, 4KB, 8KB, 16KB, 32KB, 64KB, 128KB, 256KB,512KB
External Instruction Memory	–	0x00000000	External instruction memory
External Data Memory	–	0x20100000	External data memory
TIMER0	TIMER_TypeDef	0x50000000	Timer0
TIMER1	TIMER_TypeDef	0x50001000	Timer1
UART0	UART_TypeDef	0x50004000	UART0
UART1	UART_TypeDef	0x50005000	UART1
Watch Dog	WDOG_TypeDef	0x50008000	Watchdog
RTC	RTC_RegDef	0x50006000	Real-time clock
TRNG	TRNG_RegDef	0x5000F000	True Random Number Generator
DualTimer	DUALTIMER_RegDef	0x50002000	Dual Timer
SPI_FLASH	SPI_FLASH_RegDef	0x50003000	Serial Peripheral Interface Flash (SPI-Flash and QSPI-Flash Memory)
I2C	I2C_TypeDef	0x5000A000	Internal Integrated Circuit Bus
SPI	SPI_TypeDef	0x5000B000	SPI
SD-Card	SDCard_TypeDef	0x50009000	SD
GPIO0	GPIO_TypeDef	0x40000000	GPIO port
CAN	CAN_RegDef	0x45000000	Controller Area Network

Standard Peripheral	Type	Address Mapping	Description
Ethernet	ETH_RegDef	0x46000000	Ethernet
DDR3	DDR3_RegDef	0x88000000	DDR3 Memory
PSRAM	PSRAM_TypeDef	0x82000000	Pseudo Static Random Access Memory
APB Master [1]	-	0x60000000	Extension of APB Master [1]
APB Master [2]	-	0x60100000	Extension of APB Master [2]
APB Master [3]	-	0x60200000	Extension of APB Master [3]
APB Master [4]	-	0x60300000	Extension of APB Master [4]
APB Master [5]	-	0x60400000	Extension of APB Master [5]
APB Master [6]	-	0x60500000	Extension of APB Master [6]
APB Master [7]	-	0x60600000	Extension of APB Master [7]
APB Master [8]	-	0x60700000	Extension of APB Master [8]
APB Master [9]	-	0x60800000	Extension of APB Master [9]
APB Master [10]	-	0x60900000	Extension of APB Master [10]
APB Master [11]	-	0x60A00000	Extension of APB Master [11]
APB Master [12]	-	0x60B00000	Extension of APB Master [12]
APB Master [13]	-	0x60C00000	Extension of APB Master [13]
APB Master [14]	-	0x60D00000	Extension of APB Master [14]
APB Master [15]	-	0x60E00000	Extension of APB Master [15]
APB Master [16]	-	0x60F00000	Extension of APB Master [16]
AHB Master [1]	-	0x80000000	Extension of AHB Master [1]
AHB Master [2]	-	0x81000000	Extension of AHB Master [2]
AHB Master [3]	-	0x86000000	Extension of AHB Master [3]
AHB Master [4]	-	0x89000000	Extension of AHB Master [4]
AHB Master [5]	-	0x8A000000	Extension of AHB Master [5]
AHB Master [6]	-	0x8B000000	Extension of AHB Master [6]

2.2 Core System Memory Mapping

The definition of Cortex-M1 memory mapping of core system is as shown in Table 2-2.

Table 2-2 Definition of Memory Mapping of Core System

System Control	Type	Address Mapping	Description
SysTick	SysTick_Type	0xE000E010	SysTick configuration struct
NVIC	NVIC_BASE	0xE000E100	NVIC configuration struct
SCnSCB	SCnSCB_Type	0xE000E000	System control register not in SCB
SCB	SCB_Type	0xE000ED00	SCB configuration struct

3 Interrupt Handling

Gowin_EMPU_M1nested vectored interrupt controller (NVIC) includes the following features:

- Provides up to 32 interrupt processing signals that can be used; 1, 8,16, or 32 external interrupt processing signals can be configured.
- Provides 4 extended external interrupt signals
- Supports programmable priorities of 0-3.

The definition of Cortex-M1interrupt controller is as shown in Table 3-1.

Table 3-1 Definition of Interrupt Controller

Address	Type	Number	Description
0x00000000	_StackTop	–	Top of Stack
0x00000004	Reset_Handler	–	Reset Handler
0x00000008	NMI_Handler	-14	NMI Handler
0x0000000C	HardFault_Handler	-13	Hard Fault Handler
0x00000010	0	–	Reserved
0x00000014	0	–	Reserved
0x00000018	0	–	Reserved
0x0000001C	0	–	Reserved
0x00000020	0	–	Reserved
0x00000024	0	–	Reserved
0x00000028	0	–	Reserved
0x0000002C	SVC_Handler	-5	SVCall Handler
0x00000030	0	–	Reserved
0x00000034	0	–	Reserved
0x00000038	PendSV_Handler	-2	PendSV Handler
0x0000003C	SysTick_Handler	-1	SysTick Handler
0x00000040	UART0_Handler	0	16+ 0: UART 0 RX and TX Handler

Address	Type	Number	Description
0x00000044	UART1_Handler	1	16+ 1: UART 1 RX and TX Handler
0x00000048	TIMER0_Handler	2	16+ 2: TIMR 0 handler
0x0000004C	TIMER1_Handler	3	16+ 3: TIMER 1 handler
0x00000050	GPIO0_Handler	4	16+ 4: GPIO Port 0 Combined Handler
0x00000054	UARTOVF_Handler	5	16+ 5: UART 0,1 Overflow Handler
0x00000058	RTC_Handler	6	16+ 6: RTC Handler
0x0000005C	I2C_Handler	7	16+ 7: I2C Handler
0x00000060	CAN_Handler	8	16+ 8: CAN Handler
0x00000064	ETH_Handler	9	16+ 9: ETH Handler
0x00000068	EXTINT_0_Handler	10	16+10: External 0 Handler
0x0000006C	DTimer_Handler	11	16+11: DualTimer Handler
0x00000070	TRNG_Handler	12	16+12: TRNG Handler
0x00000074	EXTINT_1_Handler	13	16+13: External 1 Handler
0x00000078	EXTINT_2_Handler	14	16+14: External 2 Handler
0x0000007C	EXTINT_3_Handler	15	16+15: External 3 Handler
0x00000080	GPIO0_0_Handler	16	16+16: GPIO0_0 Handler
0x00000084	GPIO0_1_Handler	17	16+17: GPIO0_1 Handler
0x00000088	GPIO0_2_Handler	18	16+18: GPIO0_2 Handler
0x0000008C	GPIO0_3_Handler	19	16+19: GPIO0_3 Handler
0x00000090	GPIO0_4_Handler	20	16+20: GPIO0_4 Handler
0x00000094	GPIO0_5_Handler	21	16+21: GPIO0_5 Handler
0x00000098	GPIO0_6_Handler	22	16+22: GPIO0_6 Handler
0x0000009C	GPIO0_7_Handler	23	16+23: GPIO0_7 Handler
0x000000A0	GPIO0_8_Handler	24	16+24: GPIO0_8 Handler
0x000000A4	GPIO0_9_Handler	25	16+25: GPIO0_9 Handler
0x000000A8	GPIO0_10_Handler	26	16+26: GPIO0_10 Handler
0x000000AC	GPIO0_11_Handler	27	16+27: GPIO0_11 Handler
0x000000B0	GPIO0_12_Handler	28	16+28: GPIO0_12 Handler
0x000000B4	GPIO0_13_Handler	29	16+29: GPIO0_13 Handler
0x000000B8	GPIO0_14_Handler	30	16+30: GPIO0_14 Handler
0x000000BC	GPIO0_15_Handler	31	16+31: GPIO0_15 Handler

4 Universal Asynchronous Receiver/Transmitter

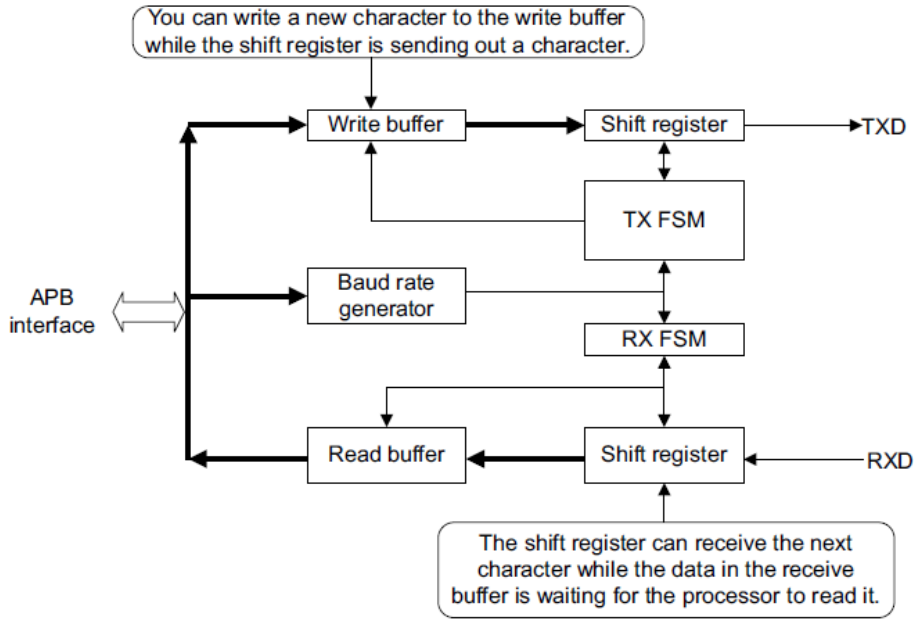
4.1 Features

Gowin_EMPU_M1 includes two UART peripherals accessed by APB bus:

- The max. baud rate is 921.6Kbit/s
- No parity bit
- 8-bit data bit
- 1-bit stop bit

UART structure diagram is as shown in Figure 4-1.

Figure 4-1 UART Structure Diagram



The UART supports the High Speed Test Mode (HSTM). When the register CTRL [6] is set to 1, the serial data is transmitted one bit per cycle,

and the text information can be transmitted in a short time.

The baud rate divider register should be set when using UART. For example, if the APB1 bus frequency is running at 12MHz and the baud rate is required to be 9600, the baud rate divider register can be set to 12000000/9600=1250.

4.2 Registers

The definition of UART registers is as shown in Table 4-1. UART register definition is located in library\libraries\cmsis\cm1\device_support\GOWIN_M1.h

Table 4-1 Definition of UART Registers

Register	Address Offset	Type	Width	Initial Value	Description
DATA	0x000	RW	8	0x--	[7:0] Data Value
STATE	0x004	RW	4	0x0	[3] RX buffer overrun, write 1 to clear [2] TX buffer overrun, write 1 to clear [1] RX buffer full, read-only [0] TX buffer full,read-only
CTRL	0x008	RW	7	0x00	[6] High speed test mode for TX only [5] RX overrun interrupt enable [4] TX overrun interrupt enable [3] RX interrupt enable [2] TX interrupt enable [1] RX enable [0] TX enable
INTSTATUS/ INTCLEAR	0x00C	RW	4	0x0	[3] RX overrun interrupt, write 1 to clear [2] TX overrun interrupt, write 1 to clear [1] RX interrupt, write 1 to clear [0] TX interrupt,write 1 to clear
BAUDDIV	0x010	RW	20	0x00000	[19:0] Baud rate divider,the minimum number is 16

4.3 Initialization

The definition of UART initialization is shown in Table 4-2. UART initialization definition is located in library\libraries\drivers\inc\GOWIN_M1_uart.h.

Table 4-2 UART Initialization Definition

Name	Type	Value	Description
UART_BaudRate	uint32_t	Max 921.6Kbit/s	Baud rate
UART_Mode	UARTMode_TypeDef	ENABLE/DISABLE	Enable/Disable TX/RX mode
UART_Int	UARTInt_TypeDef	ENABLE/DISABLE	Enable/Disable

Name	Type	Value	Description
			TX/RX interrupt
UART_Ovr	UARTOvr_TypeDef	ENABLE/DISABLE	Enable/Disable TX/RX overrun interrupt
UART_Hstm	FunctionalState	ENABLE/DISABLE	Enable/Disable TX hisgh speed test mode

4.4 Driver Usage

The usage of UART drivers is shown in Table 4-3. The UART driver definition is located in library\libraries\drivers\src\GOWIN_M1_uart.c.

Table 4-3 Usage of UART Drivers

Name	Description
UART_Init	Initialize UARTx
UART_GetRxBufferFull	Return UARTx RX buffer full status
UART_GetTxBufferFull	Return UARTx TX buffer full status
UART_GetRxBufferOverrunStatus	Return UARTx RX buffer overrun status
UART_GetTxBufferOverrunStatus	Return UARTx TX buffer overrun status
UART_ClearRxBufferOverrunStatus	Clear Rx buffer overrun status
UART_ClearTxBufferOverrunStatus	Clear Tx buffer overrun status
UART_SendChar	Send a character to UARTx TX buffer
UART_SendString	Send a string to UARTx TX buffer
UART_ReceiveChar	Receive a character from UARTx RX buffer
UART_GetBaudDivider	Return UARTx baud rate divider value
UART_GetTxIRQStatus	Return UARTx TX interrupt status
UART_GetRxIRQStatus	Return UARTx RX interrupt status
UART_ClearTxIRQ	Clear UARTx TX interrupt status
UART_ClearRxIRQ	Clear UARTx RX interrupt status
UART_GetTxOverrunIRQStatus	Return UARTx TX overrun interrupt status
UART_GetRxOverrunIRQStatus	Return UARTx RX overrun interrupt status
UART_ClearTxOverrunIRQ	Clear UARTx TX overrun interrupt request
UART_ClearRxOverrunIRQ	Clear UARTx RX overrun interrupt request
UART_SetHSTM	Set UARTx TX high speed test mode
UART_ClrHSTM	Clear UARTx TX high speed test mode

5 Timer

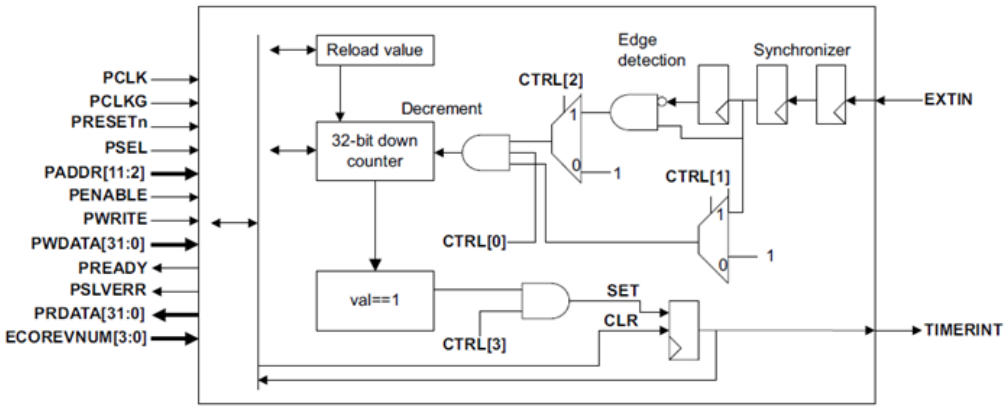
5.1 Features

Gowin_EMPU_M1 includes two standard timer peripherals accessed by APB bus:

- 32-bit counter
- Supports the interrupt request signal
- Supports the external input signal EXTIN enabling clock

The Timer structure diagram is as shown in Figure 5-1.

Figure 5-1 Timer Structure Diagram



5.2 Registers

The definition of Timer registers is as shown in Table 5-1. Timer register definition is located in library\libraries\cmsis\cm1\device_support\GOWIN_M1.h.

Table 5-1 Definition of Timer Registers

Register	Address Offset	Type	Width	Initial Value	Description
CTRL	0x000	RW	4	0x0	[3] Timer interrupt enable [2] Select external input as clock [1] Select external input as enable [0] Enable
VALUE	0x004	RW	32	0x0000000	[31:0] Current value

Register	Address Offset	Type	Width	Initial Value	Description
				0	
RELOAD	0x008	RW	32	0x00000000	[31:0] Reload value,writing to this register sets the current value
INTSTATUS/INTCLEAR	0x00C	RW	1	0x0	[0] Timer interrupt,write 1 to clear

5.3 Initialization

The definition of Timer initialization is as shown in Table 5-2. Timer initialization definition is located in library\libraries\drivers\inc\GOWIN_M1_timer.h.

Table 5-2 Timer Initialization Definition

Name	Type	Value	Description
Reload	uint32_t	-	Reload value
TIMER_Int	TIMERInt_TypeDef	SET/RESET	Enable/Disable interrupt
TIMER_Exti	TIMERExti_TypeDef	-	External input as enable or clock

5.4 Driver Usage

The usage of Timer drivers is as shown in Table 5-3. Timer driver definition is located in library\libraries\drivers\src\GOWIN_M1_timer.c.

Table 5-3 Usage of Timer Drivers

Name	Description
TIMER_Init	Initialize TIMERx
TIMER_StartTimer	Start TIMERx
TIMER_StopTimer	Stop TIMERx
TIMER_GetIRQStatus	Return TIMERx interrupt status
TIMER_ClearIRQ	Clear TIMERx interrupt status
TIMER_GetReload	Return TIMERx reload value
TIMER_SetReload	Set TIMERx reload value
TIMER_GetValue	Return TIMERx current value
TIMER_SetValue	Set TIMERx current value
TIMER_EnableIRQ	Enable TIMERx interrupt request
TIMER_DisableIRQ	Disable TIMERx interrupt request

6 Watchdog

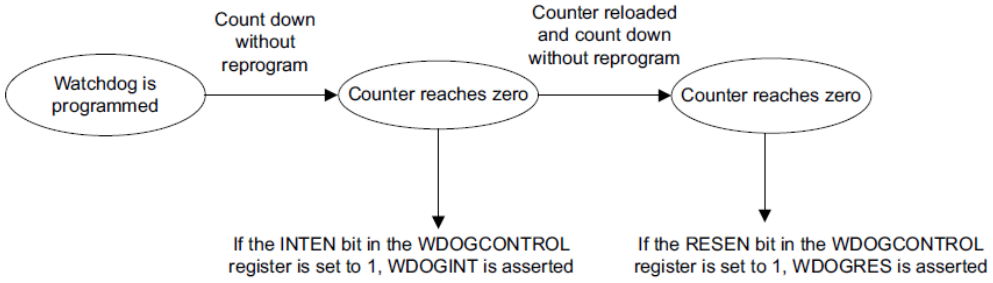
6.1 Features

Gowin_EMPU_M1 includes one Watch Dog peripheral accessed by APB bus:

- A 32-bit down-counter initialized by the LOAD register;
- Support interrupt request;
- When the clock is enabled, the counter is decremented by the posedge of the WDOGCLK signal;
- Monitor interrupts and a reset request is generated and the counter is stopped when the counter is decremented to 0;
- Respond to the software reset caused by software crashes, provide the software reset method;

The operation flow of Watch Dog is as shown in Figure 6-1.

Figure 6-1 Watch Dog Operation Flow



6.2 Registers

The definition of Watch Dog registers is as shown in Table 6-1. Watch Dog register definition is located in library\libraries\cmsis\cm1\device_support\GOWIN_M1.h.

Table 6-1 Definition of Watch Dog Registers

Register	Address Offset	Type	Width	Initial Value	Description
LOAD	0x00	RW	32	0xFFFFFFFF	The value from which the counter is to

Register	Address Offset	Type	Width	Initial Value	Description
				F	decrement
VALUE	0x04	RO	32	0xFFFFFFFF	The current value of the decrementing counter
CTRL	0x08	RW	2	0x0	[1] Enable reset output [0] Enable the interrupt
INTCLR	0x0C	WO	-	-	Clear the watchdog interrupt and reloads the counter
RIS	0x10	RO	1	0x0	Raw interrupt status from the counter
MIS	0x14	RO	1	0x0	Enable interrupt status from the counter
RESERVED	0xC00-0x014	-	-	-	Reserved
LOCK	0xC00	RW	32	0x00000000	[32:1] Enable register writes [0] Register write enable status
RESERVED	0xF00-0xC00	-	-	-	Reserved
ITCR	0xF00	RW	1	0x0	Integration test mode enable
ITOP	0xF04	WO	2	0x0	[1] Integration test WDOGRES value [0] Integration test WDOGINT value

6.3 Initialization

The initialization of Watch Dogs is as shown in Table 6-2. Watch Dog initialization definition is located in library\libraries\drivers\GOWIN_M1_wdog.h.

Table 6-2 Initialization of Watch Dogs

Name	Type	Value	Description
WDOG_Reload	uint32_t	-	Reload value
WDOG_Lock	WDOGLock_TypeDef	SET/RESET	Enable/Disable lock register write access
WDOG_Res	WDOGRes_TypeDef	SET/RESET	Enable/Disable reset flag
WDOG_Int	WDOGInt_TypeDef	SET/RESET	Enable/Disable interrupt flag
WDOG_ITMode	WDOGMode_Typedef	SET/RESET	Enable/Disable integration test mode flag

6.4 Driver Usage

The usage of Watch Dog drivers is as shown in Table 6-3. The Watch Dog driver definition is located in library\libraries/drivers\src\GOWIN_M1_wdog.c.

Table 6-3 Usage of Watch Dog Drivers

Name	Description
WDOG_Init	Initializes WatchDog
WDOG_RestartCounter	Restart watchdog counter
WDOG_GetCounterValue	Returns counter value

Name	Description
WDOG_SetResetEnable	Sets reset enable
WDOG_GetResStatus	Returns reset status
WDOG_SetIntEnable	Sets interrupt enable
WDOG_GetIntStatus	Returns interrupt enable
WDOG_ClrIntEnable	Clears interrupt enable
WDOG_GetRawIntStatus	Returns raw interrupt status
WDOG_GetMaskIntStatus	Returns masked interrupt status
WDOG_LockWriteAccess	Disable write access all registers
WDOG_UnlockWriteAccess	Enable write access all registers
WDOG_SetITModeEnable	Sets integration test mode enable
WDOG_ClrITModeEnable	Clears integration test mode enable
WDOG_GetITModeStatus	Returns integration test mode status
WDOG_SetITOP	Sets integration test output reset or interrupt
WDOG_GetITOPResStatus	Returns integration test output reset status
WDOG_GetITOPIntStatus	Returns integration test output interrupt status
WDOG_ClrITOP	Clears integration test output reset or interrupt

7 GPIO

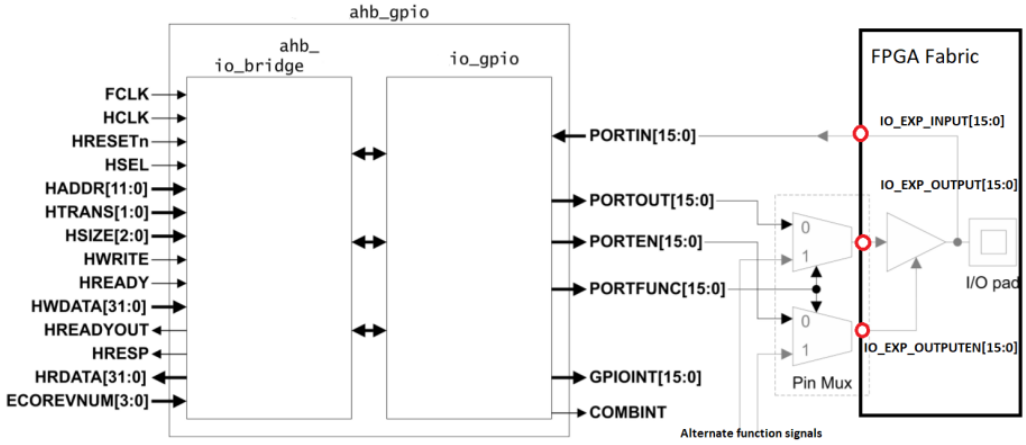
7.1 Features

Gowin_EMPU_M1 includes a GPIO peripheral with a 16-bit input and output interface accessed by AHB bus:

- Connected with FPGA Fabric
- Supports bit mask
- Supports dual-purpose pin

The GPIO structure diagram is as shown in Figure 7-1.

Figure 7-1 GPIO Structure Diagram



7.2 Registers

The definition of GPIO registers is as shown in Table 7-1. GPIO register definition is located in library\libraries\cmsis\cm1\device_support\GOWIN_M1.h.

Table 7-1 Definition of GPIO Registers

Register	Address Offset	Type	Width	Initial Value	Description
DATA	0x0000	RW	16	0x----	[15:0] Data value Read Sampled at pin Write to data output register Read back value goes through double flip-flop

Register	Address Offset	Type	Width	Initial Value	Description
					synchronize logic with delay of two cycles
DATAOUT	0x0004	RW	16	0x0000	[15:0] Data output register value Read current value of data output register Write to data output register
RESERVED	0x0008 -0x000C	–	–	–	Reserved
OUTENSET	0x0010	RW	16	0x0000	[15:0] Output enable set Write 1 to set the output enable bit Write 0 no effect Read back 0 indicates the signal direction as intput 1 indicates the signal direction as output
OUTENCLR	0x0014	RW	16	0x0000	[15:0] Output enable clear Write 1 to clear the output enable bit Write 0 no effect Read back 0 indicates the signal direction as intput 1 indicates the signal direction as output
ALTFUNCSET	0x0018	RW	16	0x0000	[15:0] Alternative function set Write 1 to set the ALTFUNC bit Write 0 no effect Read back 0 for I/O 1 for an alternate function
ALTFUNCCLR	0x001C	RW	16	0x0000	[15:0] Alternative function clear Write 1 to clear the ALTFUNC bit Write 0 no effect Read back 0 for I/O 1 for an alternate function
INTENSET	0x0020	RW	16	0x0000	[15:0] Interrupt enable set Write 1 to set the enable bit Write 0 no effect Read back 0 indicates interrupt disabled 1 indicates interrupt enabled
INTENCLR	0x0024	RW	16	0x0000	[15:0] Interrupt enable clear Write 1 to clear the enable bit Write 0 no effect Read back 0 indicates interrupt disabled 1 indicates interrupt enabled
INTTYPESET	0x0028	RW	16	0x0000	[15:0] Interrupt type set Write 1 to set the interrupt type bit Write 0 no effect

Register	Address Offset	Type	Width	Initial Value	Description
					Read back 0 for LOW/HIGH level 1 for falling edge or rising edge
INTTYPECLR	0x002C	RW	16	0x0000	[15:0] Interrupt type clear Write 1 to clear the interrupt type bit Write 0 no effect Read back 0 for LOW/HIGH level 1 for falling edge or rising edge
INTPOLSET	0x0030	RW	16	0x0000	[15:0] Polarity-level,edge IRQ config Write 1 to set the interrupt polarity bit Write 0 no effect Read back 0 for LOW level or falling edge 1 for HIGH level or rising edge
INTPOLCLR	0x0034	RW	16	0x0000	[15:0] Polarity-level,edge IRQ config Write 1 to clear the interrupt polarity bit Write 0 no effect Read back 0 for LOW level or falling edge 1 for HIGH level or rising edge
INTSTATUS /INTCLEAR	0x0038	RW	16	0x0000	[15:0] Write IRQ status clear register Write 1 to clear interrupt request Write 0 no effectx Read back IRQ status register
MASKLOWBYTE	0x0400 -0x07FC	RW	16	0x----	Lower 8-bits masked access [9:2] of the address value are used as enable bit mask for the access [15:8] not used [7:0] Data for lower byte access,with [9:2] of address value used as enable mask for each bit
MASKHIGHBYTE	0x0800 -0x0BFC	RW	16	0x----	Higher 8-bits masked access [9:2] of the address value are used as enable bit mask for the access [15:8] Data for higher byte access,with [9:2] of address value used as enable mask for each bit [7:0] not used
RESERVED	0x0C00 -0x0FCF	–	–	–	Reserved

7.3 Initialization

The definition of GPIO initialization is as shown in Table 7-2. GPIO initialization definition is located in library\libraries\drivers\inc\GOWIN_M1_gpio.h.

Table 7-2 GPIO Initialization

Name	Type	Value	Description
GPIO_Pin	uint32_t	GPIO_Pin_0 GPIO_Pin_1 GPIO_Pin_2 GPIO_Pin_3 GPIO_Pin_4 GPIO_Pin_5 GPIO_Pin_6 GPIO_Pin_7 GPIO_Pin_8 GPIO_Pin_9 GPIO_Pin_10 GPIO_Pin_11 GPIO_Pin_12 GPIO_Pin_13 GPIO_Pin_14 GPIO_Pin_15	16 bits GPIO Pins
GPIO_Mode	GPIOMode_TypeDef	GPIO_Mode_IN GPIO_Mode_OUT GPIO_Mode_AF	16 bits GPIO Pins mode
GPIO_Int	GPIOInt_TypeDef	GPIO_Int_Disable GPIO_Int_Low_Level GPIO_Int_High_Level GPIO_Int_Falling_Edge GPIO_Int_Rising_Edge	16 bits GPIO Pins interrupt

7.4 Driver Usage

The usage of GPIO drivers is as shown in Table 7-3. GPIO driver definition is located in library\libraries\drivers\src\GOWIN_M1_gpio.c.

Table 7-3 Usage of GPIO Drivers

Name	Description
GPIO_Init	Initialize GPIOx
GPIO_SetOutEnable	Set GPIOx output enable
GPIO_ClrOutEnable	Clear GPIOx output enable
GPIO_GetOutEnable	Return GPIOx output enable
GPIO_SetBit	GPIO output one
GPIO_ResetBit	GPIO output zero
GPIO_WriteBits	GPIO output

Name	Description
GPIO_ReadBits	GPIO input
GPIO_SetAltFunc	Set GPIOx alternate function enable
GPIO_ClrAltFunc	Clear GPIOx alternate function enable
GPIO_GetAltFunc	Return GPIOx alternate function enable
GPIO_IntClear	Clear GPIOx interrupt request
GPIO_GetIntStatus	Return GPIOx interrupt status
GPIO_SetIntEnable	Set GPIOx interrupt enable Return GPIOx interrupt status
GPIO_ClrIntEnable	Clear GPIOx interrupt enable Return GPIOx interrupt enable
GPIO_MaskedWrite	Setup GPIOx output value using masked access

8 I²C

8.1 Features

Gowin_EMPU_M1 includes an I²C Master peripheral accessed by AHB bus:

- APB bus interface
- Compliant with industry standard I²C protocol
- Bus arbitration and arbitration lost detection
- Bus busy detection
- Interrupt flag generation
- Generates Start, Stop, Repeated Start and Acknowledge
- Detects Start, Stop and Repeated Start
- Supports 7-bit addressing mode

8.2 Registers

The definition of I²C Master registers is as described in Table 8-1. I²C Master register definition is located in library\libraries\cmsis\cm1\device_support\GOWIN_M1.h.

Table 8-1 Definition of I²C Master Registers

Register	Address Offset	Type	Width	Initial Value	Description
PRER	0x00	RW	32	0x0000FFFF	Clock prescale register [31:15] Reserved [15:0] Prescale value = sys_clk/(5*SCL)-1
CTR	0x04	RW	32	0x00000000	[31:8] Reserved [7] Enable I2C function [6] Enable I2C interrupt [5:0] Reserved
TXR	0x08	WO	32	0x00000000	[31:8] Reserved [7:1] Next transmission data [0] Data direction
RXR	0x0C	RO	32	0x00000000	[31:8] Reserved

Register	Address Offset	Type	Width	Initial Value	Description
					[7:0] Last received data
CR	0x010	WO	32	0x00000000	[31:8] Reserved [7] STA, Start transmission status [6] STO, Over transmission status [5] RD, Read enable, read data from slave [4] WR, Write enable, write data to slave [3] Acknowledge [2:1] Reserved [0] Interrupt acknowledge
SR	0x14	RO	32	0x00000000	[31:8] Reserved [7] Receive acknowledge signal from slave [6] I2C busy status [5] Arbitration loss [4:2] Reserved [1] Data transmission status flag [0] Interrupt flag

8.3 Driver Usage

The usage of I²C Master drivers is as described in Table 8-2. The I²C Master driver definition is located in library\libraries\drivers\src\GOWIN_M1_i2c.c.

Table 8-2 Use of I²C Master Drivers

Name	Description
I2C_Init	I²C Initialization
I2C_SendByte	Send a byte to I²C bus
I2C_SendBytes	Send multiple bytes to I²C bus
I2C_SendData	Send multiple bytes to I²C bus once time
I2C_ReceiveByte	Read a byte from I²C bus
I2C_ReadBytes	Read multiple bytes from I²C bus
I2C_ReceiveData	Read multiple bytes from I²C bus once time
I2C_Rate_Set	Set I²C traffic rate
I2C_Enable	Enable I²C bus
I2C_UnEnable	Disable I²C bus
I2C_InterruptOpen	Open I²C interrupt
I2C_InterruptClose	Close I²C interrupt

9 SPI

9.1 Features

Gowin_EMPU_M1 includes a SPI Master peripheral accessed by AHB bus:

- APB bus interface
- Full duplex synchronous serial data transfer
- Supports Master working mode
- Supports configurable clock polarity and phase
- Configurable serial clock frequency generated by SPI
- Data rx register and tx register: 8-bit width

9.2 Registers

The definition of SPI Master registers is as described in Table 9-1. SPI Master register definition is located in library\libraries\cmsis\cm1\device_support\GOWIN_M1.h.

Table 9-1 Definition of SPI Master Registers

Register	Address Offset	Type	Width	Initial Value	Description
RDATA	0x00	RO	32	0x00000000	Read data register [31:8] Reserved [7:0] Read data
WDATA	0x04	WO	32	0x00000000	Write data register [31:8] Reserved [7:0] Write data
STATUS	0x08	RW	32	0x00000000	[31:8] Reserved [7] Overflow error status [6] Receive ready status [5] Transmit ready status [4] Be transmitting [3] Transmit overrun error status [2] Receive overrun error status [1:0] Reserved

Register	Address Offset	Type	Width	Initial Value	Description
SSMASK	0x0C	RW	32	0x00000000	[31:1] Reserved [0] Select and enable slave
CTRL	0x10	RW	32	0x00000000	[31:5] Reserved [4:3] Clock selected, CLK_I / 2/4/6/8 [2] Clock polarity [1] Clock polarity [0] Direction, 1 is MSB first

9.3 Initialization

The definition of SPI Master initialization is as described in Table 9-2. The SPI Master initialization definition is located in library\libraries\drivers\inc\GOWIN_M1_spi.h.

Table 9-2 SPI Master Initialization

Name	Type	Value	Description
DIRECTION	uint8_t	1/0	MSB/LSB first transmission 0: MSB first; 1: LSB first.
PHASE	uint8_t	1/0	Posedge/Negedge transmit data 0: Sample at posedge edge; 1: Sample at negedge edge.
POLARITY	uint8_t	1/0	Initialize polarity to one/zero 0: Idle sclk low; 1: Idle sclk high.
CLKSEL	uint8_t	CLKSEL_CLK_DIV_2 CLKSEL_CLK_DIV_4 CLKSEL_CLK_DIV_6 CLKSEL_CLK_DIV_8	Select clock divided 2/4/6/8

9.4 Driver Usage

The usage of SPI Master drivers is as described in Table 9-3. The SPI Master driver definition is located in library\libraries\drivers\src\GOWIN_M1_spi.c.

Table 9-3 Usage of SPI Master Drivers

Name	Description
SPI_Init	Initialize SPI
SPI_SetDirection	Set direction
SPI_ClrDirection	Clear direction
SPI_GetDirection	Return direction
SPI_SetPhase	Set phase
SPI_ClrPhase	Clear phase
SPI_GetPhase	Return phase
SPI_SetPolarity	Set polarity

Name	Description
SPI_ClrPolarity	Clear polarity
SPI_GetPolarity	Return polarity
SPI_SetClkSel	Set clock selection
SPI_GetClkSel	Return clock selection
SPI_GetToeStatus	Read transmit overrun error status
SPI_GetRoeStatus	Read receive overrun error status
SPI_GetTmtStatus	Read transmitting status
SPI_GetTrdyStatu	Read transmit ready status
SPI_GetRrdyStatus	Read receive ready error status
SPI_GetErrStatus	Read error status
SPI_ClrToeStatus	Clear transmit overrun error status
SPI_ClrRoeStatus	Clear receive overrun error status
SPI_ClrErrStatus	Clear error status
SPI_ReadWriteByte	Full duplex read and write a byte
SPI_WriteData	Write data
SPI_ReadData	Read data
SPI_Select_Slave	Select slave

10 Real-time Clock

10.1 Features

Gowin_EMPU_M1 includes a 32-bit real-time clock (RTC) peripheral accessed by AHB bus:

- APB bus interface
- 32-bit counter
- 32-bit Match register
- 32-bit comparator

MCU reads data, control, and status messages via APB bus interface and RTC. At the posedge of continuous input clock CLK1HZ (3.072MHz clock input must be provided to RTCSRCCLK. The division in RTC is 1Hz), 32-bit counter increases.

This counter is not synchronous and can not be overloaded. When system resets, this counter counts from 1 to the max. value (0xFFFFFFFF) and then goes back to 0 and keeps increasing.

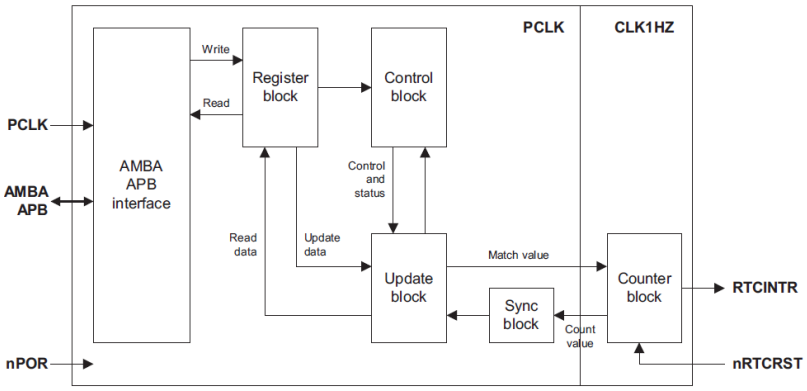
Realize RTC load or update via the write load register RTC_LOAD_VALUE

Obtain RTC current clock via the read data register RTC_CURRENT_DATA

Program Match register via the register of write RTC_MATCH_VALUE

RTC structure diagram is as shown in Figure 10-1.

Figure 10-1 RTC Structure Diagram



10.2 Registers

The definition of RTC registers is as described in Table 10-1. RTC register definition is located in library\libraries\cmsis\cm1\device_support\GOWIN_M1.h.

Table 10-1 Definition of I²C Registers

Register	Address Offset	Type	Width	Initial Value	Description
RTC_CURRENT_DATA	0x000	RO	32	0x00000000	Data Register [31:0] Current value
RTC_MATCH_VALUE	0x004	RW	32	0x00000000	Match Register If current value equals match register's value, generate interrupt [31:0] Match data
RTC_LOAD_VALUE	0x008	RW	32	0x00000000	Load Register Initialized value, start counter based on this value [31:0] Load data
RTC_CTROLLER_REG	0x00C	RW	32	0x00000000	Control Register Start RTC counter [31:1] Reserved [0] Start RTC counter
RTC_IMSC	0x010	RW	32	0x00000000	Interrupt mask set and clear register Enable or disable interrupt [31:1] Reserved [0] Enable interrupt
RTC_RIS	0x014	RO	32	0x00000000	Raw interrupt status register Get current raw unmasked interrupt status [31:1] Reserved [0] Current raw unmasked interrupt status
RTC_MIS	0x018	RO	32	0x00000000	Masked interrupt status register Get current masked interrupt status [31:1] Reserved [0] Current masked interrupt status
RTC_INTR_CL	0x01C	WO	32	0x0000000	Interrupt clear register

Register	Address Offset	Type	Width	Initial Value	Description
EAR				0	Clear current interrupt [31:1] Reserved [0] Clear current interrupt

10.3 Driver Usage

The usage of RTC drivers is as described in Table 10-2. The RTC driver definition is located at library\libraries\drivers\src\GOWIN_M1_rtc.c.

Table 10-2 Usage of RTC Drivers

Name	Description
RTC_init	Initialize RTC
Get_Current_Value	Get RTC current value of data register
Set_Match_Value	Set RTC match value of match register
Get_Match_Value	Get RTC match value of match register
Set_Load_Value	Set RTC load value of load register
Get_Load_Value	Get RTC load value of load register
Start_RTC	Start RTC counter
Close_RTC	Cloase RTC counter
RTC_Inter_Mask_Set	Set RTC interrupt mask
Get_RTC_Control_value	Get value of control register
RTC_Inter_Mask_Clr	Clear RTC interrupt mask
Get_RTC_Inter_Mask_value	Get RTC interrupt mask
Clear_RTC_interrupt	Clear RTC interrupt

11 True Random Number Generator

11.1 Features

Gowin_EMPU_M1 includes a 32-bit true random number generator (TRNG) peripheral accessed by AHB bus:

- Digital logic generates and adopts a true random number bitstream;
- Includes an internal entropy source based on a digital inverter chain;
- If MCU core runs at 200MHz, a10K bits/s entropy can be generated;
- APB bus interface.

11.2 Registers

The definition of TRNG registers is as described in Table 11-1. TRNG register definition is located in library\libraries\cmsis\cm1\device_support\GOWIN_M1.h.

Table 11-1 Definition of TRNG Registers

Register	Address Offset	Type	Width	Initial Value	Description
RESERVE1	0x000-0x0FC	-	-	-	Reserved
RNG_IMR	0x100	RW	32	0x0000000F	Interrupt mask register [31:4] Reserved [3] Mask the Von Neumann error [2] Mask the CRNGT error [1] Mask the Autocorrelation error [0] Mask when the TRNG has collected 192 bits
RNG_ISR	0x104	RO	32	0x00000000	Interrupt status register [31:4] Reserved [3] A Von Neumann error [2] A Continuos Random Number Generation Testing (CRNGT) error [1] The Autocorrelation test failed four timers in a row. [0] Set to 1, when 192 bits have

Register	Address Offset	Type	Width	Initial Value	Description
					been collected, and EHR_DATA[0-5] registers are ready to be read.
RNG_ICR	0x108	WO	32	0x00000000	Interrupt clear register [31:4] Reserved [3] Clear a Von Nenumann error [2] Clear a CRNGT error [1] Software cannot clear this bit, only a TRNG reset can clear this bit. [0] Set to 1 after EHR_DATA[0-5] have been read
TRNG_CONFIG	0x10C	RW	32	0x00000000	Configuration register [31:2] Reserved [1:0] Selects the number of inverters: 00 = Selects the shortest inverter chain length 01 = Selects the short inverter chain length 10 = Selects the long inverter chain length 11 = Selects the longest inverter chain length
TRNG_VALID	0x110	RO	32	0x00000000	Valid register [31:1] Reserved [0] TRNG is complete, data can be read from EHR_DATA[0-5]
EHR_DATA0	0x114—x128	RO	32	0x00000000	Entropy holding register data register Return 32 bits from the 192-bit EHR DATA0 returns bit[31:0] DATA1 returns bit[63:32] DATA2 returns bit[95:64] DATA3 returns bit[127:96] DATA4 returns bit[159:128] DATA5 returns bit[191:160]
EHR_DATA1					
EHR_DATA2					
EHR_DATA3					
EHR_DATA4					
EHR_DATA5					
RND_SOURCE_ENABLE	0x12C	RW	32	0x00000000	Random source enable register [31:1] Reserved [0] 1 = enable entropy source; 0 = disable entropy source
SAMPLE_CNT1	0x130	RW	32	0x0000FFFF	Sample count register [31:0] Sets the number of rng_clk cycles
AUTOCORR_STATISTIC	0x134	RW	32	0x00000000	Autocorrelation register [31:22] Reserved [21:14] Count each time an autocorrelation test fails

Register	Address Offset	Type	Width	Initial Value	Description
					[13:0] Count each time an autocorrelation test starts
TRNG_DEBUG_CONTROL	0x138	RO	32	0x00000000	Debug control register [31:4] Reserved [3] The autocorrelation test is bypassed [2] The CRNGT test is bypassed [1] The Von Neumann balancer is bypassed [0] Reserved
RESERVE2	0x13C	-	-	-	Reserved
TRNG_SW_RESET	0x140	WO	32	0x00000000	Reset register [31:1] Reserved [0] Writing 1 to this register causes an internal TRNG reset
RESERVE3	0x144-0x1B4	-	-	-	Reserved
TRNG_BUSY	0x1B8	RO	32	0x00000000	Busy register [31:1] Reserved [0] Relects the status of rng_busy signal
RST_BIT_COUNT	0x1BC	WO	32	0x00000000	Reset bit counter register [31:1] Reserved [0] Write any value to this bit resets the bits counter and TRNG valid registers
RESERVE4	0x1C0-0x1DC	-	-	-	Reserved
RNG_BIST_CNTR0	0x1E0-0x1E8	RO	32	0x00000000	BIST counter registers Return the collected BIST results [31:22] Reserved [21:0] Returns the results of the TRNG BIST counter
RNG_BIST_CNTR1					
RNG_BIST_CNTR2					

11.3 Driver Usage

The usage of TRNG drivers is as described in Table 11-2. The TRNG driver definition is located in library\libraries\drivers\src\GOWIN_M1_trng.c.

Table 11-2 Usage of TRNG Drivers

Name	Description
Init_TRNG	Initialized TRNG
Set_Interrupt_Mask	Set interrupt mask
Get_Int_State	Get interrupt status
Clear_Int	Clear interrupt
Set_Config	Set config register
Get_EHR_Data	Get Entropy holding data

Name	Description
Set_Random_Source_Enable	Set random source enable register
Clr_Random_Source_Enable	Clear random source enable register
Set_Sample_Count	Set sample count register
Trng_SW_Reset	Reset TRNG
Get_TRNG_State	Get TRNG state
Reset_Bit_Count	Reset bit count register
Get_BIT_Counter	Get bits count register
Set_Debug_Control	Set debug control register
Fail_Start_State_times	Get autocorrelation register
Clr_Fail_Start_State_register	Clear autocorrelation register

12 Dual Timer

12.1 Features

Gowin_EMPU_M1 includes a 32-bit and 16-bit DualTimer peripheral accessed by AHB bus:

- APB bus interface
- Includes two programmable 32-bit or 16-bit down-counters
- Generates interrupt when the down-counter reaches 0

12.2 Registers

The definition of down-counter registers is as described in Table 12-1. The DualTimer register definition is located in library\libraries\cmsis\cm1\device_support\GOWIN_M1.h.

Table 12-1 Definition of DualTimer Registers

Register	Address Offset	Type	Width	Initial Value	Description
TIMER1LOAD	0x00	RW	32	0x00000000	Timer1 load register [31:0] Timer1 load value
TIMER1VALUE	0x04	RO	32	0xFFFFFFFF	Timer1 current value register [31:0] Timer1 current value
TIMER1CONTROL	0x08	RW	32	0x00000020	Timer1 control register [31:8] Reserved [7] Timer enable [6] Timer mode [5] Interrupt enable [4] Reserved [3:2] Timer prescale 00 = clock is divided by 1 01 = clock is divided by 16 10 = clock is divided by 256 11 Undefined [1] Timer size 0 = 16-bit counter, default 1 = 32-bit counter [0] One-shot count

Register	Address Offset	Type	Width	Initial Value	Description
					0 = wrapping mode, default 1 = one-shot mode
TIMER1INTCLR	0x0C	WO	-	-	Timer1 interrupt clear register Any write clears the interrupt output of the counter
TIMER1RIS	0x10	RO	32	0x00000000	Timer1 raw interrupt status register [31:1] Reserved [0] Raw interrupt status from the counter
TIMER1MIS	0x14	RO	32	0x00000000	Timer1 interrupt status register [31:1] Reserved [0] Enable interrupt status from the counter
TIMER1BGLOAD	0x18	RW	32	0x00000000	Timer1 background load register [31:0] The value used to reload the counter
RESERVE1	-	-	-	-	Reserved
TIMER2LOAD	0x00	RW	32	0x00000000	Timer2 load register [31:0] Timer2 load value
TIMER2VALUE	0x04	RO	32	0xFFFFFFFF	Timer2 current value register [31:0] Timer2 current value
TIMER2CONTROL	0x08	RW	32	0x00000020	Timer2 control register [31:8] Reserved [7] Timer enable [6] Timer mode [5] Interrupt enable [4] Reserved [3:2] Timer prescale 00 = clock is divided by 1 01 = clock is divided by 16 10 = clock is divided by 256 11 Undefined [1] Timer size 0 = 16-bit counter, default 1 = 32-bit counter [0] One-shot count 0 = wrapping mode, default 1 = one-shot mode
TIMER2INTCLR	0x0C	WO	-	-	Timer2 interrupt clear register Any write clears the interrupt output of the counter
TIMER2RIS	0x10	RO	32	0x00000000	Timer2 raw interrupt status register [31:1] Reserved [0] Raw interrupt status from the counter

Register	Address Offset	Type	Width	Initial Value	Description
TIMER2MIS	0x14	RO	32	0x00000000	Timer2 interrupt status register [31:1] Reserved [0] Enable interrupt status from the counter
TIMER2BGLOAD	0x18	RW	32	0x00000000	Timer2 background load register [31:0] The value used to reload the counter

12.3 Driver Usage

The usage of DualTimer drivers is as described in Table 12-2. The DualTimer driver definition is located in library\libraries\drivers\src\GOWIN_M1_dualtimer.c.

Table 12-2 Usage of DualTimer Drivers

Name	Description
DUALTIMER1_Init	Initialized DualTimer1
DUALTIMER2_Init	Initialized DualTimer2
Clear_DULATIMER_interrupt	Clear DualTimer interrupt
Dtimer_MODE_function	Set timer mode of DualTimer1 or DualTimer2
Dtimer_PRE_function	Set timer prescale of DualTimer1 or DualTimer2
INIT_NUM_load_function	Set load value of DualTimer1 or DualTimer2
ENABLE_interrupt_Dtimer_function	Enable interrupt of DualTimer1 or DualTimer2
TIMER_SIZE_function	Set timer size of DualTimer1 or DualTimer2
ENABLE_Dtimer_function	Enable DualTimer1 or DualTime2
Get_DULATIMER_interrupt_num	Get timer ID of DualTimer1 or DualTimer2

13 SD Card

13.1 Features

Gowin_EMPU_M1 includes one SD-Card peripheral accessed by one APB:

- Supports SD/MMC cards
- Supports hardware initialization of cards
- Simple SPI bus access
- Supports block read and write
- Embedded receiving and transmitting buffer of 512 bytes
- APB bus interface
- Independent clocks for APB interface and SPI core logic
- The data transmitting speed close to the max. speed of SD/MMC cards
- Only supports FAT16 and SD cards up to 4GB

13.2 Registers

The definition of SD-Card registers is as described in Table 13-1. SD-Card register definition is located in library\libraries\cmsis\cm1\device_support\GOWIN_M1.h.

Table 13-1 Definition of SD-Card Registers

Register	Address Offset	Type	Width	Initial Value	Description
SPI_MASTER_VERSION	0x000	RW	8	0x00	SPI master version register [7:4] Major revision number [3:0] Minor revision number
SPI_MASTER_CONTROL	0x001	WO	8	0x00	SPI master control register [7:1] Reserved [0] Reset core logic and register 1 = Reset core logic and register, self clearing
TRANS_TYPE	0x002	RW	8	0x00	Transaction type register

Register	Address Offset	Type	Width	Initial Value	Description
					[7:2] Reserved [1:0] Set the transaction type 00 = Direct access 01 = Initialized SD 10 = Read SD block 11 = Write SD block
TRANS_CTRL	0x003	WO	8	0x00	Transaction control register [7:1] Reserved [0] Start transaction 1 = Start transaction, self clearing
TRANS_STS	0x004	RO	8	-	Transaction status register [7:1] Reserved [0] Transaction busy 1 = Transaction busy
TRANS_ERROR	0x005	RO	8	-	Transaction error register [7:6] Reserved [5:4] SD write error 00 = Write no error 01 = Write command error 10 = Write data error 11 = Write busy error [3:2] SD read error 00 = Read no error 01 = Read command error 10 = Read token error [1:0] SD initialize error 00 = Initialize no error 01 = Initialize command 0 error 10 = Initialize command 1 error
DIRECT_ACCESS_DATA	0x006	RW	8	0x00 / -	Data direct access register [7:0] Transmit data Set TX_DATA prior to starting a DIRECT_ACCESS transaction [7:0] Receive data Read RX_DATA after completing a DIRECT_ACCESS transaction
SD_ADDR_7_0	0x007	RW	8	0x00	SD address[7:0] bits register [7:0] SD_ADDR[7:0]
SD_ADDR_15_8	0x008	RW	8	0x00	SD address[15:8] bits register [7:0] SD_ADDR[15:8]
SD_ADDR_23_16	0x009	RW	8	0x00	SD address[23:16] bits register [7:0] SD_ADDR[23:16]

Register	Address Offset	Type	Width	Initial Value	Description
SD_ADDR_31_24	0x00A	RW	8	0x00	SD address[31:24] bits register [7:0] SD_ADDR[31:24]
SPI_CLK_DEL	0x00B	RW	8	0x00	SPI clock control register [7:0] Control the frequency of the SPI_CLK after SD initialization is completed
RESERVED0	0x00C-0x00F	-	-	-	Reserved
RX_FIFO_DATA	0x010	RW	8	-	SPI block reading data register [7:0] SD/MMC block read data, fifo size matches the SD/MMC block size of 512 bytes
RESERVED1	0x011	-	-	-	Reserved
RX_FIFO_DATA_COUNT_MSB	0x012	RO	8	-	MSB byte of reading data count register [7:0] MSByte of FIFO_DATA_COUNT, indicates the number of data entries within the fifo
RX_FIFO_DATA_COUNT_LSB	0x013	RO	8	-	LSB byte of reading data count register [7:0] LSByte of FIFO_DATA_COUNT, indicates the number of data entries within the fifo
RX_FIFO_CONTROL	0x014	WO	8	0x00	SD block reading data control register [7:1] Reserved [0] Force fifo empty 1 = Force fifo empty, delete all the data samples within the fifo, self clearing
RESERVED2	0x015-0x019	-	-	-	Reserved
TX_FIFO_DATA	0x020	WO	8	-	SD block writing data register [7:0] SD/MMC block write data, fifo size matches the SD/MMC block size of 512 bytes
RESERVED3	0x021-0x023	-	-	-	Reserved
TX_FIFO_CONTROL	0x024	WO	8	0x00	SD block writing data control register [7:1] Reserved [0] Force fifo empty 1 = Force fifo empty, delete all the data samples within the fifo, self clearing

13.3 Driver Usage

The usage of SD-Card drivers is as described in Table 13-2. The SD-Card driver definition is located at library\libraries\drivers\src\GOWIN_M1_sdcard.c.

Table 13-2 Usage of SD-Card Drivers

Name	Description
SD_Init	SD hardware initialization
SD_BlockWrite	SD block write data, block size is 512 bytes.
SD_BlockRead	SD block read data, block size is 512 bytes.

14 Controller Area Network

14.1 Features

Gowin_EMPU_M1 includes one CAN peripheral accessed by AHB:

- AHB bus interface
- Complies with CAN 2.0A and CAN 2.0B protocols and ISO 11898-1 standard
- Supports CAN-FD: non-ISO CAN FD, compliant with Bosch protocol, and ISO/DIS 11898-1.
- Independent system clock and CAN bus clock
- Flexible shared buffer scheme to achieve the optimal buffer size for storing TX and RX messages in the application. The total buffer depth can be configured through parameters when configuring the IP core; transmit buffer, receive buffer, and high-priority transmit buffer are supported; the CPU can configure the depth of each buffer separately for transmit, receive, and high-priority transmit buffers.
- The number of receive filters can be configured from 1 to 16
- Programmable baud rate prescaler (BRP): Generates TQ CLK based on the CAN bus clock, with an 8-bit BRP register supporting prescalers from 4 to 255.

14.2 Registers

The definition of CAN registers is as described in Table 14-1. CAN register definition is located in library\libraries\cmsis\cm1\device_support\GOWIN_M1.h.

Table 14-1 Definition of CAN Registers

Register	Address Offset	Type	Width	Initial Value	Description
SRST	0x0000	RW	32	0x00000000	Software reset register [31:1] Reserved [0] Control reset 1 = Hardware reset 0 = Software reset
CMD	0x0004	RW	32	0x00000000	Command register [31:1] Reserved [0] Command settings

Register	Address Offset	Type	Width	Initial Value	Description
					1 = Working mode 0 = Command mode
BRP	0x0008	RW	32	0x00000000	Baud rate prescalar register [31:8] Reserved [7:0] Baud rate prescalar
BTN	0x000C	RW	32	0x00000000	Bit timing (nominal) register [28:24] sjw_nom [13:8] phseg2_nom, PHASE_SEG2 window's width [5:0] phseg1_nom, PROP_SEG+PHASE_SEG1 window's width
BTD	0x0010	RW	32	0x00000000	Bit timing (data) register [26:24] sjw_d [11:8] phseg2_d, PHASE_SEG2 window's depth [3:0] phseg1_d, PROP_SEG+PHASE_SEG1 window's depth
RSVD0	0x001C	-	-	-	Reserved
IS	0x0020	RO	32	0x00000000	Interrupt status register [31] Bus off status [27] TX message successfully [26] TX message retry [25] TX message failed [23] TX high-priority message successfully [22] TX high-priority message retry [21] TX high-priority message failed [8] Error status [5] TX high-priority fifo overflow [4] TX fifo overflow [1] RX fifo overflow [0] RX fifo valid
IE	0x0024	RW	32	0x00000000	Interrupt enable register [31] Enable us off [27] Enable TX message successfully [26] Enable TX message retry [25] Enable TX message failed [23] Enable TX high-priority message successfully [22] Enabe TX high-priority message retry [21] Enable TX high-priority

Register	Address Offset	Type	Width	Initial Value	Description
					message failed [8] Enable Error status [5] Enabe TX high-priority fifo overflow [4] Enable TX fifo overflow [1] Enable RX fifo overflow [0] Enable RX fifo valid
IC	0x0028	WO	32	0x00000000	Interrupt clear register [31] Clear bus off status [27] Clear TX message successfully status [26] Clear TX message retry status [25] Clear TX message failed status [23] Clear TX high-priority message successfully status [22] Clear TX high-priority message retry status [21] Clear TX high-priority message failed status [8] Clear Error status status [5] Clear TX high-priority fifo overflow status [4] Clear TX fifo overflow status [1] Clear RX fifo overflow status [0] Clear RX fifo valid status
RSVD1	0x002C	-	-	-	Reserved
CFG	0x0030	RW	32	0x00000000	Configuration register [4] Configure disprotexceponres 1 = ‘res’ is FORM-ERROR 0 = ‘res’ is exception [0] Configure isofd 1 = ISO FD mode 0 = non ISO FD mode
RSVD2	0x0034-0x003C	-	-	-	Reserved
RXBCFG	0x0040	RW	32	0x00000000	RX buffer/fifo configuration register [31:16] RX buffer’s ending offset [15:0] RX buffer’s start offset
TXBCFG	0x0044	RW	32	0x00000000	TX buffer/fifo configuration register [31:16] TX buffer’s ending offset [15:0] TX buffer’s start offset
TXHBCFG	0x0048	RW	32	0x00000000	TX high-priority/fifo configuration register [31:16] TX high-priority buffer’s

Register	Address Offset	Type	Width	Initial Value	Description
					ending offset [15:0] TX high-priority buffer's start offset
RSVD3	0x004C	-	-	-	Reserved
TXBRETRY	0x0050	RW	32	0x00000000	TX buffer retry counter
TXHBRETRY	0x0054	RW	32	0x00000000	TX high-priority buffer retry counter
TXMSGSTS	0x0058	RO	32	0x00000000	Transmit message status register [31:30] TX message status 00 = Successfully 10 = Retry 11 = Failed [28:0] Message ID
TXHMSGSTS	0x005C	RO	32	0x00000000	Transmit high-priority message status register [31:30] TX high-priority message status 00 = Successfully 10 = Retry 11 = Failed [28:0] Message ID
ERRSTS	0x0060	RW	32	0x00000000	Error status register [4] CRC error [3] ACK error [2] FORM error [1] BIT error [0] STUFF error
ERRCNTR	0x0064	RO	32	0x00000000	Error counter register [24:16] TX error counter [8:0] RX error counter
RSVD4	0x0068-0x00FC	-	-	-	Reserved
AF	0x0100-0x100+(4*N)	RW	32	0x00000000	Receive acceptance filter register [31] Enable 1 = Valid 0 = Invalid [30] IDE 1 = Extended frame 0 = Normal frame [29] Extended data length 1 = Match FD frame 0 = Match normal frame [28:18] Basic ID [17:0] ID Extension
AFM	0x0140-0x140+(4*N)	RW	32	0x00000000	Receive acceptance filter mask register

Register	Address Offset	Type	Width	Initial Value	Description
					[28:18] Basic ID mask [17:0] ID Extension mask
RSVD5	0x0180-0x01FC	-	-	-	Reserved
RXB	0x0200	RO	32	0x00000000	Receive buffer/fifo window register
TXB	0x0204	WO	32	0x00000000	Transmit buffer/fifo window register
TXHB	0x0208	WO	32	0x00000000	Transmit high-priority buffer/fifo window register
TXBSTS	0x020C	RO	32	0x00000000	Transmit buffer/fifo status [31] txbwerr [15:0] txbspace
TXHBSTS	0x0210	RO	32	0x00000000	Transmit high-priority buffer/fifo status [31] txhbwerr [15:0] txhbspace
RXBSTS	0x0214	RO	32	0x00000000	Receive buffer/fifo status [15:0] rxbdepth

14.3 Driver Usage

The usage of CAN drivers is as described in Table 14-2. The CAN driver definition is located at library\libraries\drivers\src\GOWIN_M1_can.c.

Table 14-2 Usage of CAN Drivers

Name	Description
can_srst	Start hard reset
can_set_cmd	Enable working mode
can_set_brp	Set baud rate prescalar
can_set_btn_phseg1_nom	Set PROP_SEG+PHASE_SEG1 window's width
can_set_btn_phseg2_nom	Set PHASE_SEG2 window's width
can_set_btn_sjw_nom	Set sjw_nom
can_set_btn	Set BTN register
can_read_btn_phseg1_nom	Get PROP_SEG+PHASE_SEG1 window's width
can_read_btn_phseg2_nom	Get PHASE_SEG2 window's width
can_read_btn_sjw_nom	Get sjw_nom
can_set_btd_phseg1_d	Set PROP_SEG+PHASE_SEG1 window's depth
can_set_btd_phseg2_d	Set PHASE_SEG2 window's depth
can_set_btd_sjw_d	Set sjw_d
can_set_btd	Set BTD register
can_read_btd_phseg1_d	Get PROP_SEG+PHASE_SEG1 window's depth
can_read_btd_phseg2_d	Get PHASE_SEG2 window's depth
can_read_btd_sjw_d	Get sjw_d

Name	Description
can_read_is_bit	Get IS register bits function
can_set_ie_bit	Set IE register bits function
can_clear_ie_bit	Clear IE register bits function
can_read_ie_bit	Get IE register bits function
can_set_ic_bit	Set IC register bits function
can_set_cfg_bit_as_one	Set CFG register bits function
can_set_cfg_bit_as_zero	Clear CFG register bits function
can_read_cfg_bit	Get CFG register bits function
can_set_rxbcfg_rxb_start	Set RX buffer start offset in RXBCFG
can_read_rxbcfg_rxb_start	Get RX buffer start offset in RXBCFG
can_set_rxbcfg_rxb_end	Set RX buffer ending offset in RXBCFG
can_read_rxbcfg_rxb_end	Get RX buffer ending offset in RXBCFG
set_rxbcfg	Set RX buffer start and ending offset
can_set_txbcfg_txb_start	Set TX buffer start offset in TXBCFG
can_read_txbcfg_txb_start	Get TX buffer start offset in TXBCFG
can_set_txbcfg_txb_end	Set TX buffer ending offset in TXBCFG
can_read_txbcfg_txb_end	Get TX buffer ending offset in TXBCFG
set_txbcfg	Set TX buffer start and ending offset
can_set_txhbcfg_txhb_start	Set TX high-priority buffer start offset in TXHBCFG
can_read_txhbcfg_txhb_start	Get TX high-priority buffer start offset in TXHBCFG
can_set_txhbcfg_txhb_end	Set TX high-priority buffer ending offset in TXHBCFG
can_read_txhbcfg_txhb_end	Get TX high-priority buffer ending offset in TXHBCFG
set_txhbcfg	Set TX high-priority buffer start and ending offset
can_set_txbretry	Set TX buffer retry
can_read_txbretry	Get TX buffer retry
can_set_txhbretry	Set TX high-priority buffer retry counter
can_read_txhbretry	Get TX high-priority buffer retry counter
can_read_txmsgsts	Get TX message status
can_read_txmsgid	Get TX message ID
can_read_txhmsgsts	Get TX high-priority message status
can_read_txhmsgid	Get TX high-priority message ID
can_read_errsts	Get error status
can_read_errcntr_rec	Get RX error counter
can_read_errcntr_tec	Get TX error counter
can_set_af_bit_as_one	Set AF bits function
can_set_af_bit_as_zero	Clear AF bits function
can_read_af_bit	Get AF bits function

Name	Description
can_set_af_ie	Set AF ID Extension
can_read_af_ie	Get AF ID Extension
can_set_af_bid	Set AF basic ID
can_read_af_bid	Get AF basic ID
can_set_afm_ie	Set AFM ID Extension mask
can_read_afm_ie	Get AFM ID Extension mask
can_set_afm_bid	Set AFM basic ID mask
can_read_afm_bid	Get AFM basic ID mask
can_read_rxb	Get RXB register
can_set_txb	Set TXB register
can_set_txhb	Set TXHB register
can_read_txbsts_tdbspace	Get txbspace
can_read_txbsts_txbwerr	Get txbwerr
can_read_txhbsts_txhbspace	Get txhbspace
can_read_txhbsts_txhbwerr	Get txhbwerr
can_read_rxbsts	Get rxbdepth

15 Ethernet

15.1 Features

Gowin_EMPU_M1 includes one Ethernet peripheral accessed by AHB:

- AHB bus interface
- Realizes the function description of MAC layer in the IEEE802.3 protocol
- RGMII/GMII/MII interface
- Supports 10/100/1000M rate
- Supports full duplex and half duplex mode, and conflict detection can be supported in half duplex mode
- Supports users to choose whether to automatically add and verify CRC
- Supports to add pad function automatically
- Supports Ethernet frame classification statistics
- Supports Ethernet frame error statistics
- Supports IFG configurable functions
- Supports Jumbo mode
- Supports Flow Control in full duplex mode
- Supports Management interface mdc, mdio

15.2 Registers

The definition of Ethernet registers is as described in Table 15-1. Ethernet register definition is located in library\libraries\cmsis\cm1\device_support\GOWIN_M1.h.

Table 15-1 Definition of Ethernet Registers

Register	Address Offset	Type	Width	Initial Value	Description
ETH_TX_DATA	0x000-0x5FF	WO	32	0x00000000	Transmit data registers
ETH_RX_DATA	0x000-0x5FFF	RO	32	0x00000000	Receive data registers
ETH_TX_LENGT	0x600	RW	32	0x00000000	Transmit data length

Register	Address Offset	Type	Width	Initial Value	Description
H					[31:11] Reserved [10:0] TX data length
ETH_TX_EN	0x604	RW	32	0x00000000	Transmit enable [31:1] Reserved [0] Enable TX
ETH_TX_FAIL	0x608	RW	32	0x00000000	Transmit failed status [31:3] Reserved [2] TX late [1] TX excessive [0] TX failed
ETH_TX_IS	0x60C	RO	32	0x00000000	Transmit interrupt status [31:1] Reserved [0] TX interrupt status
ETH_TX_IC	0x610	WO	32	0x00000000	Transmit interrupt clear [31:1] Reserved [0] Clear TX interrupt
ETH_TX_IE	0x614	RW	32	0x00000000	Transmit interrupt enable [31:1] Reserved [0] Enable TX interrupt
RESERVED_1	0x618-0x67F	–	–	–	Reserved
ETH_RX_LEGHT	0x680	RO	32	0x00000000	Receive data length
ETH_RX_IS	0x684	RO	32	0x00000000	Receive interrupt status [31:1] Reserved [0] RX interrupt status
ETH_RX_IE	0x688	RW	32	0x00000000	Receive interrupt enable [31:1] Reserved [0] Enable RX interrupt
ETH_RX_IC	0x68C	WO	32	0x00000000	Receive interrupt clear [31:1] Reserved [0] Clear RX interrupt
RESERVED_2	0x690-0x6FFF	–	–	–	Reserved
MIIM_OP_MODE	0x700	RW	32	0x00000000	MIIM operation mode [31:1] Reserved [0] MIIM operation mode
MIIM_PHY_ADDR	0x704	RW	32	0x00000000	MIIM PHY address [31:5] Reserved [4:0] MIIM PHY address
MIIM_REG_ADDR	0x708	RW	32	0x00000000	MIIM reg address [31:5] Reserved [4:0] MIIM reg address
MIIM_WR_DATA	0x70C	RW	32	0x00000000	MIIM write data [31:16] Reserved [15:0] MIIM write data
MIIM_RD_DATA	0x710	RO	32	0x00000000	MIIM read data [31:16] Reserved

Register	Address Offset	Type	Width	Initial Value	Description
					[15:0] MIIM read data
MIIM_IS	0x714	RO	32	0x00000000	MIIM interrupt status [31:2] Reserved [1] MIIM operation end [0] MIIM read data valid
MIIM_IE	0x718	RW	32	0x00000000	MIIM interrupt enable [31:2] Reserved [1] MIIM operation end [0] MIIM read data valid
MIIM_IC	0x71C	WO	32	0x00000000	MIIM interrupt clear [31:2] Reserved [1] MIIM operation end [0] MIIM read data valid
MIIM_OP_EN	0x720	RW	32	0x00000000	MIIM operation enable [31:1] Reserved [0] Enable MIIM operation
ETH_MODE	0x724	RW	32	0x00000000	Ethernet operation mode [31:3] Reserved [2:0] Duplex mode and speed 000 = Full duplex 100M 001 = Full duplex 1000M 010 = Full duplex 10M 100 = Half duplex 100M 110 = Half duplex 10M

15.3 Driver Usage

The usage of Ethernet drivers is as described in Table 15-2. The Ethernet driver definition is located in library\libraries\drivers\src\GOWIN_M1_ethernet.c.

Table 15-2 Usage of Ethernet Drivers

Name	Description
eth_init	Initialize Ethernet
tx_int_event	TX interrupt
rx_int_event	RX interrupt
eth_tx	Ethernet TX
eth_set_mode	Set Ethernet duplex mode and speed
miim_wr_int_event	MIIM interface transmits interrupt
miim_rd_int_event	MIIM interface receives interrupt
miim_write	MIIM interface transmits data
miim_receive	MIIM interface receives data

16 DDR3 Memory

16.1 Features

Gowin_EMPU_M1 includes one DDR3 Memory peripheral accessed by AHB:

- AHB bus interface
- Compatible with DDR3 SDRAM device meeting industrial standard and the module compatible with JESD79-3F specification
- Supports memory data path width of 16 bits
- Supports UDIMM memory module
- Supports memory chip of x8 and x16 data width
- Programmable burst length 4
- Supports clock ratio 1:4 mode

16.2 Registers

The definition of DDR3 memory registers is as shown in Table 16-1. DDR3 Memory register definition is located in library\libraries\cmsis\cm1\device_support\GOWIN_M1.h.

Table 16-1 Definition of DDR3 Memory Registers

Register	Address Offset	Type	Width	Initial Value	Description
RESERVED	0x0000	–	–	–	Reserved
WR_ADDR	0x0004	RW	32	0x0	Write address register
WR_DATA	0x0008-0x0014	WO	128	0x0	Write data register
RD_ADDR	0x0018	RW	32	0x0	Read address register
RD_EN	0x001c	RW	32	0x0	Read enable register [31:1] Reserved [0] Read enable 1 = Enable 0 = Disable
RD_DATA	0x0020-0x002c	RO	128	0x0	Read data register
INIT	0x0030	RW	32	0x0	Initialized completely flag register

Register	Address Offset	Type	Width	Initial Value	Description
					[31:1] Reserved [0] Initialzed completely flag
WR_EN	0x0034	RW	32	0x0	Write enable and ending flag register [31:1] Reserved [0] Write enable and ending flag 1 = Enable 0 = Ending

16.3 Driver Usage

The usage of DDR3 memory drivers is as described in Table 16-2. The DDR3 Memory driver definition is located at library\libraries\drivers\src\GOWIN_M1_ddr3.c.

Table 16-2 Usage of DDR3 Drivers

Name	Description
DDR3_Init	Initialize DDR3
DDR3_Read	Read data from DDR3
DDR3_Write	Write data into DDR3

17 SPI-Flash Memory

17.1 Features

Gowin_EMPU_M1 includes one SPI-Flash peripheral accessed via AHB bus.

- SPI-Flash memory download is at AHB bus interface.
- SPI-Flash memory read, write, and erase functions are at APB bus interface.
- Support Quad SPI-Flash Memory read, write, and erase.

17.2 Registers

The definition of SPI-Flash memory registers is as shown in Table 17-1. SPI-Flash Memory register definition is located in library\libraries\cmsis\cm1\device_support\GOWIN_M1.h.

Table 17-1 Definition of SPI-Flash Memory Registers

Register	Address Offset	Type	Width	Initial Value	Description
IDREV	0x00	RO	32	0x02002000	ID and revision register [31:8] ID number [7:4] Major revision number [3:0] Minor revision number
RESERVED0[3]	0x04-0x0C	-	-	-	Reserved
TRANSFMT	0x10	RW	32	0x00020780	SPI transfer format register [31:18] Reserved [17:16] Address length in bytes 00 = 1 byte 01 = 2 bytes 10 = 3 bytes 11 = 4 bytes [15:13] Reserved [12:8] Data length [7] Enable data merge mode [6:5] Reserved [4] Bi-directional MOSI in single mode

Register	Address Offset	Type	Width	Initial Value	Description
					0 = MOSI is uni-directional signal 1 = MOSI is bi-directional signal [3] Transfer data with the lease significant bit first 0 = Most significant bit first 1 = Least significant bit first [2] SPI master/slave mode selection 0 = Master mode 1 = Slave mode [1] SPI clock polarity 0 = SCLK is LOW in the idle states 1 = SCLK is HIGH in the idle states [0] SPI clock phase 0 = Sampling data at odd SCLK edges 1 = Sampling data at even SCLK edges
DIRECTIO	0x14	RW	32	0x0	SPI direct IO control register [31:25] Reserved [24] Enable direct IO 0 = Disable 1 = Enable [23:22] Reserved [21] Output enable for SPI-Flash hold signal [20] Output enable for SPI-Flash write protect signal [19] Output enable for the SPI MISO signal [18] Output enable for the SPI MOSI signal [17] Output enable for SPI SCLK signal [16] Output enable for SPI CS signal [15:14] Reserved [13] Output value for SPI-Flash hold signal [12] Output value for SPI-Flash write protect signal [11] Output value for SPI MISO signal [10] Output value for SPI MOSI signal [9] Output value for SPI SCLK signal [8] Output value for SPI CS signal [7:6] Reserved [5] Status of SPI-Flash hold signal [4] Status of SPI-Flash write protect signal [3] Status of SPI MISO signal [2] Status of SPI MOSI signal [1] Status of SPI SCLK signal

Register	Address Offset	Type	Width	Initial Value	Description
					[0] Status of SPI CS signal
RESERVED1[2]	0x18-0x1C	-	-	-	Reserved
TRANSCTRL	0x20	RW	32	0x0	SPI transfer control register [31] Reserved [30] SPI command phase enable 0 = Disable the command phase 1 = Enable the command phase (Master mode only) [29] SPI address phase enable 0 = Disable the address phase 1 = Enable the address phase (Master mode only) [28] SPI address phase format 0 = Address phase is single mode 1 = The format of the address phase is the same as the DualQuad data phase (Master mode only) [27:24] Transfer mode 0000 = Write and read at the same time 0001 = Write only 0010 = Read only 0011 = Write, Read 0100 = Read, Write 0101 = Write, Dummy, Read 0110 = Read, Dummy, Write 0111 = None data 1000 = Dummy, Write 1001 = Dummy, Read 1010~1111 = Reserved [23:22] SPI data phase format 00 = Single mode 01 = Dual I/O mode 10 = Quad I/O mode 11 = Reserved [21] Append and one-byte special token following the address phase for SPI read transfers [20:12] Transfer count for write data [11] The value of the one-byte special token following the address phase for SPI read transfers 0 = token value is 0x00 1 = token value is 0x69 [10:9] Dummy data count [8:0] Transfer count for read data
CMD	0x24	RW	32	0x0	SPI command register

Register	Address Offset	Type	Width	Initial Value	Description
					[31:8] Reserved [7:0] SPI command
ADDR	0x28	RW	32	0x0	SPI address register [31:0] SPI address (Master mode only)
DATA	0x2C	RW	32	0x0	SPI data register [31:0] Data to transmit or the received data
CTRL	0x30	RW	32	0x0	SPI controller register [31:21] Reserved [20:16] Transmit FIFO threshold [15:13] Reserved [12:8] Receive FIFO threshold [7:5] Reserved [4] TX DMA enable [3] RX DMA enable [2] Transmit FIFO reset [1] Receive FIFO reset [0] SPI reset
STATUS	0x34	RO	32	0x0	SPI status register [31:24] Reserved [23] Transmit FIFO full flag [22] Transmit FIFO empty flag [21] Reserved [20:16] Number of valid entries int the transmit FIFO [15] Receive FIFO full flag [14] Receive FIFO empty flag [13] Reserved [12:8] Number of valid entries in the receive FIFO [7:1] Reserved [0] SPI register programming is in progress
INTREN	0x38	RW	32	0x0	SPI interrupt enable register [31:6] Reserved [5] Enable the slave command interrupt [4] Enable the end of SPI transfer interrupt [3] Enable the SPI transmit FIFO threshold interrupt [2] Enable the SPI receive FIFO threshold interrupt [1] Enable SPI transmit FIFO underrun interrupt (Slave mode only) [0] Enable SPI receive FIFO overrun interrupt (Slave mode only)
INTRST	0x3C	WO	32	0x0	SPI interrupt status register

Register	Address Offset	Type	Width	Initial Value	Description
					[31:6] Reserved [5] Slave command interrupt (Slave mode only) [4] End of SPI transfer interrupt [3] TX FIFO threshold interrupt [2] RX FIFO threshold interrupt [1] TX FIFO underrun interrupt (Slave mode only) [0] RX FIFO overrun interrupt (Slave mode only)
TIMING	0x40	RW	32	0x0	SPI interface timing register [31:14] Reserved [13:12] The minimum time between the edges of SPI CS and the edges of SCLK [11:8] The minimum time the SPI CS should stay HIGH [7:0] The clock frequency ratio between the clock source and SPI interface SCLK
RESERVED2[3]	0x44-0x4c	-	-	-	Reserved
MEMCTRL	0x50	RW	32	0x0	SPI memory access control register [31:9] Reserved [8] This bit is set when “MEMCTRL” / ”TIMING” is written [7:4] Reserved [3:0] Selects the SPI command
RESERVED3[3]	0x54-0x5C	-	-	-	Reserved
SLVST	0x60	RW	32	0x0	SPI slave status register [31:19] Reserved [18] Data underrun occurs in the last transaction [17] Data overrun occurs in the last transaction [16] SPI is ready for data transaction [15:0] User defined status flags
SLVDATACNT	0x64	RO	32	0x0	SPI slave data count register [31:25] Reserved [24:16] Slave transmitted data count [15:9] Reserved [8:0] Slave received data count
RESERVED4[5]	0x68-0x78	-	-	-	Reserved
CONFIG	0x7C	RO	32	0x0	Configuration register [31:15] Reserved [14] Support for SPI slave mode

Register	Address Offset	Type	Width	Initial Value	Description
					[13] Reserved [12] Support for memory-mapped access through AHB bus [11] Support for direct SPI IO [10] Reserved [9] Support for Quad I/O SPI [9] Support for Dual I/O SPI [7:6] Reserved [5:4] Depth of TX FIFO 00 = 2 words 01 = 4 words 10 = 8 words 11 = 16 words [3:2] Reserved [1:0] Depth of RX FIFO 00 = 2 words 01 = 4 words 10 = 8 words 11 = 16 words

17.3 Driver Usage

17.3.1 QSPI-Flash Driver

The usage of QSPI-Flash Memory drivers is as described in Table 17-2. The QSPI-Flash Memory driver definition is located in library\libraries\drivers\src\GOWIN_M1_qspi_flash.c.

Table 17-2 QSPI-Flash Memory Drivers

Name	Description
qspi_flash_init	Initialize QSPI-Flash Memory
change_mode_qspi_flash	Switch QSPI-Flash Memory mode between download and read, write, erase memory
qspi_flash_io_fast_read	Read data from QSPI-Flash Memory fastest, a single command and multi data
qspi_flash_fast_read	Read data from QSPI-Flash Memory fast, a single command and a single data
qspi_flash_write	Write data into QSPI-Flash Memory
qspi_flash_4ksector_erase	Erase 4KB sectors of QSPI-Flash Memory
qspi_flash_64ksector_erase	Erase 64KB sectors of QSPI-Flash Memory
qspi_flash_page_program	Write data into QSPI-Flash Memory with pages
qspi_flash_chip_erase	Erase full chip of QSPI-Flash Memory
qspi_flash_write_sr	Write status register of QSPI-Flash Memory
qspi_flash_read_sr	Read status register of QSPI-Flash Memory
qspi_flash_Enable	Enable QSPI-Flash Memory

17.3.2 SPI-Flash Driver

The usage of SPI-Flash memory drivers is as described in Table 17-3. The SPI-Flash Memory driver definition is located in library\libraries\drivers\src\GOWIN_M1_spi_flash.c.

Table 17-3 Use of SPI-Flash Memory Drivers

Name	Description
spi_flash_init	Initialize SPI-Flash Memory
change_mode_spi_flash	Switch SPI-Flash Memory mode between download and read, write, erase memory
spi_flash_read	Read data from SPI-Flash Memory
spi_flash_write	Write data into SPI-Flash Memory
spi_flash_4ksector_erase	Erase 4KB sectors of SPI-Flash Memory
spi_flash_page_program	Write data into SPI-Flash Memory with pages
spi_flash_64ksector_erase	Erase 64KB sectors of SPI-Flash Memory

18 PSRAM Memory

18.1 Features

Gowin_EMPU_M1 includes one PSRAM peripheral accessed via AHB bus:

- AHB bus interface
- Compatible with standard PSRAM memory devices
- Supports memory data path width of 8
- Support chips of x8 data width
- Programmable burst length of 32
- Clock ratio 1:2
- Supports initial delay of 6
- Supports regular delay mode
- Supports power off option
- Supports driving strength of 50
- Self-refreshing is full
- Refreshing rate is normal

18.2 Registers

The definition of PSRAM memory registers is as shown in Table 18-1. PSRAM Memory register definition is located in library\libraries\cmsis\cm1\device_support\GOWIN_M1.h.

Table 18-1 Definition of PSRAM Memory Registers

Register	Address Offset	Type	Width	Initial Value	Description
CMD	0x00	RW	1	0x0	Command register [0] Operation type 0 = Read operation 1 = Write operation
ADDRESS	0x04	RW	21	0x0	Address register [20:0] Address of reading and writing data

Register	Address Offset	Type	Width	Initial Value	Description
WR_DATA 0	0x08	RW	32	0x0	Write data register 0 [31:0] Write first 32bit data
WR_DATA 1	0x0C	RW	32	0x0	Write data register 1 [31:0] Write second 32bit data
WR_DATA 2	0x10	RW	32	0x0	Write data register 2 [31:0] Write third 32bit data
WR_DATA 3	0x14	RW	32	–	Write data register 3 [31:0] Write fourth 32bit data
CMD_EN	0x18	WO	1	–	Command enable register [0] Enable PSRAM
READ_DONE	0x1C	RW	1	–	Read status register [0] Read done flag, auto set 1 if it is done, and need mcu to clear
RD_DATA 0	0x20	RO	32	–	Read data register 0 [31:0] Read first 32bit data
RD_DATA 1	0x24	RO	32	–	Read data register 1 [31:0] Read second 32bit data
RD_DATA 2	0x28	RO	32	–	Read data register 2 [31:0] Read third 32bit data
RD_DATA 3	0x2C	RO	32	–	Read data register 3 [31:0] Read fourth 32bit data
INTI_DONE	0x30	RO	1	–	Initialization done register [0] PSRAM hardware initialization done flag 0 = Initialization failed 1 = Initialization done

18.3 Driver Usage

The usage of PSRAM memory drivers is as described in Table 18-2. The PSRAM Memory driver definition is located in library\libraries\drivers\src\GOWIN_M1_psram.c.

Table 18-2 Usage of PSRAM Memory Drivers

Name	Description
PSRAM_Check_Init_Status	Check the status of PSRAM Memory initialization
PSRAM_Mode_Set	Set the mode fo PSRAM Memory write and read
PSRAM_Address_Set	Set the address of PSRAM Memory and save data into this address
PSRAM_Read_Data_Buff	Read data from the buffer of PSRAM Memory
PSRAM_Cmd_Enable	Enable the command of PSRAM Memory
PSRAM_Read_Done_Flag	Get the flag of read PSRAM Memory done
PSRAM_Clear_Read_Done_Flag	Clear the flag of read PSRAM Memory

Name	Description
	done
PSRAM_Write_Data_Buff	Write data into the buffer of PSRAM Memory
PSRAM_Cmd_Unable	Disable the command of PSRAM Memory
PSRAM_Write_Data_Package	Write a package data into PSRAM Memory
PSRAM_Read_Data_Package	Read a package data from PSRAM Memory

19 Embedded Real-time Operating System

Gowin_EMPU_M1 supports uC/OS-III, FreeRTOS, and RT-Thread Nano version RTOS.

19.1 uC/OS-III

19.1.1 Features

- The uC/OS-III is an extensible, romable, and preemptive real-time core. There is no limit to the number of tasks that can be managed.
- uC/OS-III is the third generation core. It provides a real-time core's functions, including resource management, synchronization, and inter-task communication, etc.
- uC/OS-III also provides features that are not available for the other real-time cores. For example, it can measure operating performance during runtime and send signals or messages to tasks directly. Tasks can also wait for multiple semaphores and message queues simultaneously.
- Gowin_EMPU_M1 supports uC/OS-III.
- uC/OS-III source code is available at Micrium website: http://www.micrium.com.

19.1.2 Version

Gowin_EMPU_M1 supports uC/ os-iii V3.03.00 version.

19.1.3 Configuration

- UCOSIII_CONFIG\os_cfg.hn and os_cfg_app.h can be modified to configure uC/OS-III.
- UCOS_BSP\bsp.c and bsp.h can be modified to support the development board used.

19.2 FreeRTOS

19.2.1 Features

- FreeRTOS is a mini real-time operating system.
- FreeRTOS is a lightweight operating system. It offers functions of task management, time management, semaphore, message queue, memory management, recording, software timer, etc. It can basically meet the needs of small systems.
- FreeRTOS is a free operating system. It has features of open source, portability, reducibility, and flexible scheduling policy.
- Gowin_EMPU_M1 supports FreeRTOS.
- FreeRTOS source code is available at FreeRTOS website: http://www.FreeRTOS.org

19.2.2 Version

Gowin_EMPU_M1 supports FreeRTOS V10.2.1.

19.2.3 Configuration

"include\FreeRTOSConfig.h" can be modified to configure FreeRTOS.

19.3 RT-Thread Nano Version

19.3.1 Features

- RT-Thread Nano is a lite hard real-time core.
- It is developed in C with object-oriented programming and has a good code style, and it is a trimmable, preemptive real-time multitasking RTOS.
- It uses minimal memory resource with features including task handling, software timers, semaphores, mailboxes and real-time scheduling, etc.
- it is open source and free, and follows the Apache license 2.0. The real-time operating system core and all open source components can be used in commercial products for free without potential commercial risk, and you do not need to publish the application source code.
- Gowin_EMPU_M1 supports RT-Thread Nano.
- RT-Thread Nano source code is available on the RT-Thread website at https://www.rt-thread.org.

19.3.2 Version

Gowin_EMPU_M1 supports RT-Thread Nano V3.1.5.

19.3.3 Configuration

"bsp\cm1\rtconfig.h" can be modified to configure RT-Thread Nano.

"bsp\cm1\drivers\board.c" can be modified to support the development board.

20 Protocol Stack Software Programming

Gowin_EMPU_M1 supports the following protocol stack software programming: TCP/IP Protocol Stack

20.1 TCP/IP Protocol Stack

Gowin_EMPU_M1 supports the open-source TCP/IP protocol stack, LwIP.

The LwIP protocol stack is a lightweight open-source TCP/IP protocol stack designed for embedded systems and small devices. It is intended to provide TCP/IP network protocol support, enabling embedded systems to communicate with other devices over the network.

20.1.1 Features

- Lightweight: Occupies minimal memory and processor resources, ensuring efficient operation in embedded systems.
- Trimmability: Allows trimming based on specific requirements, including only essential protocols and functions to reduce storage space and processor overhead.
- High Performance: Utilizes performance optimization such as zero-copy and event-driven mechanisms to enhance network communication efficiency and throughput.
- Portability: Exhibits good portability and can run on various operating systems and hardware platforms, including RTOS like FreeRTOS and uC/OS-III.
- Versatility: Supports multiple application protocols, in addition to the TCP/IP protocol stack, providing implementations for common application layer protocols such as HTTP, SNMP, and MQTT.
- Gowin_EMPU_M1 supports LwIP protocol stack in MCU mode, RTOS FreeRTOS and uC/OS-III modes.

20.1.2 Version

Gowin_EMPU_M1 supports LwIP protocol stack version V2.1.2.

21 Application Programs

Gowin_EMPU_M1 provides application programs for the ARM Keil MDK IDE (tested software version: V5.26) and GMD IDE (tested software version: V1.2) software environments. The following sections will describe various application programs for Gowin_EMPU_M1.

21.1 UART

Gowin_EMPU_M1 provides UART application program:

…\ref_design\MCU_RefDesign\MDK_RefDesign\cm1_demo\project\printf

…\ref_design\MCU_RefDesign\GMD_RefDesign\cm1_demo\src\project\printf

…\ref_design\MCU_RefDesign\MDK_RefDesign\cm1_demo\project\uart_rx

…\ref_design\MCU_RefDesign\GMD_RefDesign\cm1_demo\src\project\uart_rx

…\ref_design\MCU_RefDesign\MDK_RefDesign\cm1_demo\project\uart_rx_intr

…\ref_design\MCU_RefDesign\GMD_RefDesign\cm1_demo\src\project\uart_rx_intr

21.2 Timer

Gowin_EMPU_M1 provides Timer application program:

…\ref_design\MCU_RefDesign\MDK_RefDesign\cm1_demo\project\timer

…\ref_design\MCU_RefDesign\GMD_RefDesign\cm1_demo\src\project\timer

21.3 Watch Dog

Gowin_EMPU_M1 provides Watch Dog application program:

…\ref_design\MCU_RefDesign\MDK_RefDesign\cm1_demo\project\watchdog

…\ref_design\MCU_RefDesign\GMD_RefDesign\cm1_demo\src\project\watchdog

21.4 GPIO

Gowin_EMPU_M1 provides GPIO application program:

…\ref_design\MCU_RefDesign\MDK_RefDesign\cm1_demo\project\led

…\ref_design\MCU_RefDesign\GMD_RefDesign\cm1_demo\src\project\led

…\ref_design\MCU_RefDesign\MDK_RefDesign\cm1_demo\project\gpio_in_intr

…\ref_design\MCU_RefDesign\GMD_RefDesign\cm1_demo\src\project\gpio_in_intr

…\ref_design\MCU_RefDesign\MDK_RefDesign\cm1_demo\project\keyscan

…\ref_design\MCU_RefDesign\GMD_RefDesign\cm1_demo\src\project\keyscan

21.5 I2C Master

Gowin_EMPU_M1 provides I^2C Master application program:

…\ref_design\MCU_RefDesign\MDK_RefDesign\cm1_demo\project\i2c_master

…\ref_design\MCU_RefDesign\GMD_RefDesign\cm1_demo\src\project\i2c_master

21.6 SPI Master

Gowin_EMPU_M1 provides SPI Master application program:

…\ref_design\MCU_RefDesign\MDK_RefDesign\cm1_demo\project\spi_master

…\ref_design\MCU_RefDesign\GMD_RefDesign\cm1_demo\src\project\spi_master

21.7 RTC

Gowin_EMPU_M1 provides RTC application program:

…\ref_design\MCU_RefDesign\MDK_RefDesign\cm1_demo\project\rtc

…\ref_design\MCU_RefDesign\GMD_RefDesign\cm1_demo\src\project\rtc

21.8 TRNG

Gowin_EMPU_M1 provides TRNG application program:

…\ref_design\MCU_RefDesign\MDK_RefDesign\cm1_demo\project\tr

ng

…\ref_design\MCU_RefDesign\GMD_RefDesign\cm1_demo\src\project\trng

21.9 Dual Timer

Gowin_EMPU_M1 provides DualTimer application program:

…\ref_design\MCU_RefDesign\MDK_RefDesign\cm1_demo\project\dualtimer

…\ref_design\MCU_RefDesign\GMD_RefDesign\cm1_demo\src\project\dualtimer

21.10 SD-Card

Gowin_EMPU_M1 provides SD-Card application program:

…\ref_design\MCU_RefDesign\MDK_RefDesign\cm1_fatfs

…\ref_design\MCU_RefDesign\GMD_RefDesign\cm1_fatfs

21.11 CAN

Gowin_EMPU_M1 provides CAN application program:

…\ref_design\MCU_RefDesign\MDK_RefDesign\cm1_demo\project\can

…\ref_design\MCU_RefDesign\GMD_RefDesign\cm1_demo\src\project\can

21.12 Ethernet

Gowin_EMPU_M1 provides Ethernet application program:

…\ref_design\MCU_RefDesign\MDK_RefDesign\cm1_demo\project\ethernet

…\ref_design\MCU_RefDesign\GMD_RefDesign\cm1_demo\src\project\ethernet

21.13 DDR3 Memory

Gowin_EMPU_M1 provides DDR3 Memory application program:

…\ref_design\MCU_RefDesign\MDK_RefDesign\cm1_demo\project\ddr3

…\ref_design\MCU_RefDesign\GMD_RefDesign\cm1_demo\src\project\ddr3

21.14 SPI-Flash Memory

Gowin_EMPU_M1 provides SPI-Flash Memory application program:

…\ref_design\MCU_RefDesign\MDK_RefDesign\cm1_demo\project\spi_flash

…\ref_design\MCU_RefDesign\GMD_RefDesign\cm1_demo\src\proje

ct\spi_flash

21.15 QSPI-Flash Memory

Gowin_EMPU_M1 provides QSPI-Flash Memory application program:

…\ref_design\MCU_RefDesign\MDK_RefDesign\cm1_demo\project\qspi_flash

…\ref_design\MCU_RefDesign\GMD_RefDesign\cm1_demo\src\project\qspi_flash

21.16 PSRAM Memory

Gowin_EMPU_M1 provides PSRAM Memory application program:

…\ref_design\MCU_RefDesign\MDK_RefDesign\cm1_demo\project\psram

…\ref_design\MCU_RefDesign\GMD_RefDesign\cm1_demo\src\project\psram

21.17 Interrupt

Gowin_EMPU_M1 provides Interrupt application program:

…\ref_design\MCU_RefDesign\MDK_RefDesign\cm1_demo\project\interrupt

…\ref_design\MCU_RefDesign\GMD_RefDesign\cm1_demo\src\project\interrupt

21.18 DMM

Gowin_EMPU_M1 provides Dynamic Memory Management application program:

…\ref_design\MCU_RefDesign\MDK_RefDesign\cm1_demo\project\dmm

…\ref_design\MCU_RefDesign\GMD_RefDesign\cm1_demo\src\project\dmm

21.19 AHB Master

Gowin_EMPU_M1 provides AHB Master application program:

…\ref_design\MCU_RefDesign\MDK_RefDesign\cm1_demo\project\ahb_master

…\ref_design\MCU_RefDesign\GMD_RefDesign\cm1_demo\src\project\ahb_master

21.20 APB Master

Gowin_EMPU_M1 provides APB Master application program:

…\ref_design\MCU_RefDesign\MDK_RefDesign\cm1_demo\project\apb_master

…\ref_design\MCU_RefDesign\GMD_RefDesign\cm1_demo\src\project\apb_master

21.21 uC/OS-III

Gowin_EMPU_M1 provides RTOS uC/OS-III application program:

…\ref_design\MCU_RefDesign\MDK_RefDesign\cm1_ucos_iii

…\ref_design\MCU_RefDesign\GMD_RefDesign\cm1_ucos_iii

21.22 FreeRTOS

Gowin_EMPU_M1 provides RTOS FreeRTOS application program:

…\ref_design\MCU_RefDesign\MDK_RefDesign\cm1_freertos

…\ref_design\MCU_RefDesign\GMD_RefDesign\cm1_freertos

21.23 RT-Thread Nano Version

Gowin_EMPU_M1 provides RT-Thread Nano version application program:

…\ref_design\MCU_RefDesign\MDK_RefDesign\cm1_rtthread_nano

…\ref_design\MCU_RefDesign\GMD_RefDesign\cm1_rtthread_nano

21.24 LwIP Protocol Stack

Gowin_EMPU_M1 provides LwIP protocol stack application program:

…\ref_design\MCU_RefDesign\MDK_RefDesign\cm1_tcpip\project\lwip_freertos_ping

…\ref_design\MCU_RefDesign\MDK_RefDesign\cm1_tcpip\project\lwip_freertos_tcp_netcon_client

…\ref_design\MCU_RefDesign\MDK_RefDesign\cm1_tcpip\project\lwip_freertos_tcp_socket_client

…\ref_design\MCU_RefDesign\MDK_RefDesign\cm1_tcpip\project\lwip_freertos_tcpserver_socket

…\ref_design\MCU_RefDesign\MDK_RefDesign\cm1_tcpip\project\lwip_raw_ping

…\ref_design\MCU_RefDesign\MDK_RefDesign\cm1_tcpip\project\lwip_raw_udp

…\ref_design\MCU_RefDesign\MDK_RefDesign\cm1_tcpip\project\lwip_uc3_client_ok

…\ref_design\MCU_RefDesign\MDK_RefDesign\cm1_tcpip\project\lwip_uc3_ping_ok

…\ref_design\MCU_RefDesign\MDK_RefDesign\cm1_tcpip\project\lwip_uc3_server_ok

21.25 Uip Protocol Stack

Gowin_EMPU_M1 provides Uip protocol stack application program:

…\ref_design\MCU_RefDesign\MDK_RefDesign\cm1_tcpip\project\uip_helloworld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