# Gowin Triple Speed Ethernet MAC

# User Guide

**IPUG538-1.0E, 2/20/2019**

**Disclaimer**

## Revision History

| Date | Version | Description |
|---|---|---|
| 2/20/2019 | 1.0E | Initial version published. |

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# 1 About This Guide

## 1.1 Purpose

This user guide is designed to help users quickly learn the function of Gowin Triple Speed Ethernet MAC IP. It mainly helps the user quickly understand the feature, characteristic and usage of Gowin Triple Speed Ethernet MAC IP.

## 1.2 Supported Products

The information presented in this guide applies to the following products:

1. GW1N series (except GW1N-1)
2. GW1NR series
3. GW2A series
4. GW2AR series

## 1.3 Related Documents

The user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

1. GW1N series FPGA Products Data Sheet
2. GW1NR series FPGA Products Data Sheet
3. GW2A series FPGA Products Data Sheet
4. GW2AR series FPGA Products Data Sheet
5. Gowin YunYuan Software User Guide

# 1.4 Terminology and Abbreviation

The terminology and abbreviation used in this manual are as shown in Table1-1 below.

**Table1-1 Terminology and Abbreviation**

| Terminology and Abbreviations | Full Name |
|---|---|
| IP | Intellectual Property |
| LUT | Look-up Table |

# 1.5 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com.cn

E-mail: support@gowinsemi.com

+Tel: +86 755 8262 0391

# 2 Overview

This document describes Triple Speed Ethernet MAC IP, which realizes the function description of MAC layer in the IEEE802.3 protocol. Triple Speed Ethernet MAC IP provides a universal access interface for users. It can be integrated into devices that require an Ethernet MAC, a connection typically used for communication applications.

**Table2-1 Gowin Triple Speed Ethernet MAC IP**

| Gowin Triple Speed Ethernet MAC IP | |
|---|---|
| Supporting devices | GW1N series (except GW1N) ,GW1NR series,GW2A series, GW2AR series |
| Logic Resource | See Table3-1。 |
| Delivered Doc. | |
| Design Files | Verilog (encryption) |
| Reference Design | Verilog |
| Testing platform | Verilog |
| Test and Design Flow | |
| Synthesis Software | Synplify_Pro |
| Application Software | GowinYunYuan |

# 3 Feature and Performance

## 3.1 Key Features

- Support MII/GMII/RGMII interface
- Conform to IEEE 802.3 protocol;
- Support 10/100/1000m rate
- Support full duplex and half duplex mode, conflict detection supported in half duplex mode
- Support users to choose whether to automatically add and verify CRC
- Support the function of adding pad automatically
- Support Ethernet frame classification statistics
- Support Ethernet frame error statistics
- Support IFG configurable functions
- Support Jumbo mode
- Support Flow Control in full duplex mode
- Support Management interface mdc, mdio.

## 3.2 Working Frequency

The Gowin Triple Speed Ethernet MAC IP working frequency depends on the current operation mode of IP. References are as follows:

- When IP is configured to RGMII mode, the working frequency supports 1000/100/10mhz
- When IP is configured to GMII mode, the working frequency supports 1000mhz
- When IP is configured to MII mode, the working frequency supports 100/10mhz
- When IP is configured to GMII/MII mode, the working frequency supports 1000/100/10mhz

## 3.3 Resource Utilization

Gowin Triple Speed Ethernet MAC IP adopts Verilog language, which applies in GW1N series (except GW1N-1 ), GW1NR series, GW2A series and GW2AR series FPGA devices. Different modes have different resource consumption.

An overview of resource utilization is given in Table3-1. For the resource utilization of other devices, please refer to the post release information.

**Table3-1 Resource Utilization**

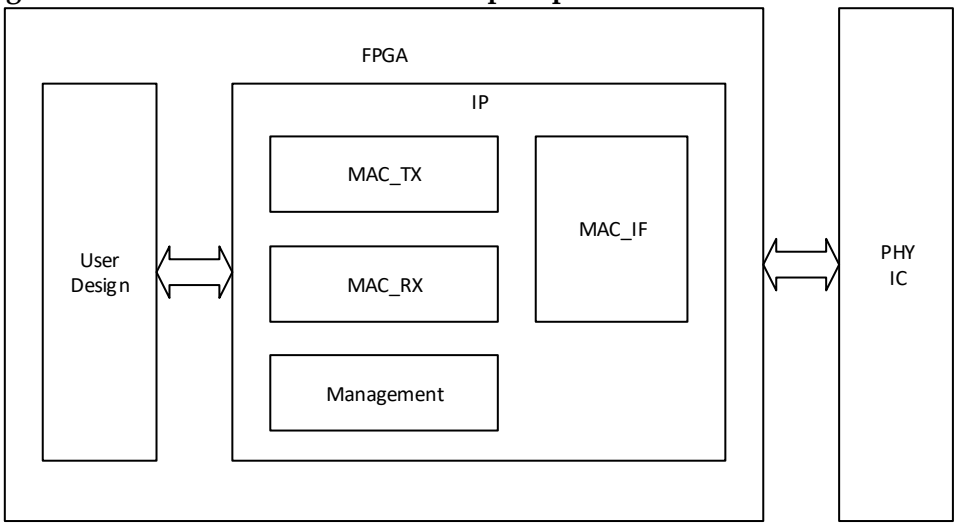
| Interface | LUTs | REGs | Device Series | Speed Level |
|---|---|---|---|---|
| RGMII | 1298 | 1284 | GW2A18 | -8 |
| GMII | 899 | 1041 | GW2A18 | -8 |
| MII | 1142 | 1224 | GW2A18 | -8 |
| GMII/MII | 1245 | 1261 | GW2A18 | -8 |

# 4 Function and Structure Description

## 4.1 Overall Structure

The basic structure of Gowin Triple Speed Ethernet MAC IP is shown in figure 4-1, mainly including MAC_IF, MAC_RX, MAC_TX, Management and other modules. The User Design in Figure 4-1 is the user design in FPGA, and the PHY IC is the chip of Ethernet PHY, which is externally connected.

**Figure 4-1 Structure Chart of Gowin Triple Speed Ethernet MAC IP**




- MAC_TX module realizes the conversion from user data format to Ethernet data format, as well as CRC, PAD, Flow Control, frame statistics and other functions.
- MAC_RX module realizes the conversion from Ethernet data format to user data format, as well as CRC, Flow Control, IFG configuration, frame statistics, error indication and other functions.
- AC_IF module realizes the function of Ethernet data adaption to various MAC interface, such as RGMII, GMII, MII.
- Management realizes MDC and MDIO functions of Ethernet management interface and facilitates users to configure PHY IC.

# 4.2 MAC Layer Interface

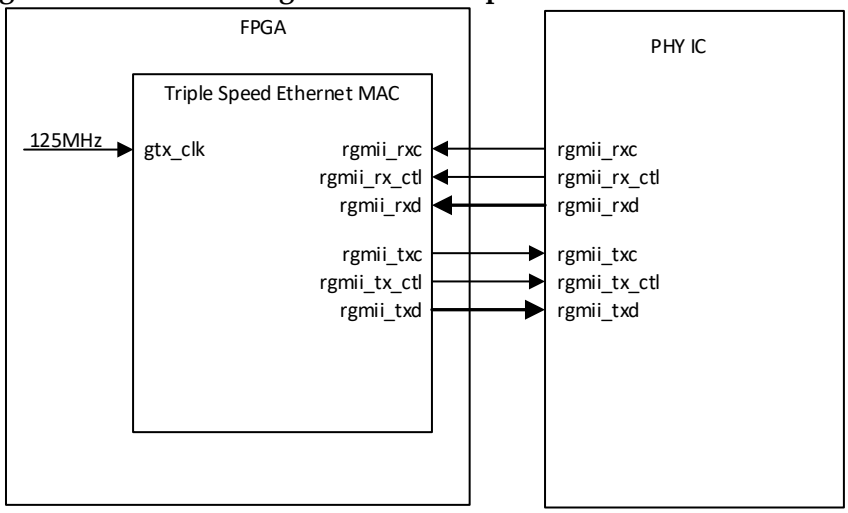
IP supports 4 MAC layer interfaces, namely RGMII interface, GMII interface, MII interface and GMII/MII interface. The supporting mode of each interface is listed as follows:

- RGMII interface supports 1000/100/10m full-duplex and 100/10m half-duplex;
- GMII interface supports 1000M full-duplex;
- MII interface supports 100/10m full-duplex and 100/10m half-duplex;
- GMII/MII interface supports 1000/100/10m full-duplex and 100/10m half-duplex.

## 4.2.1 RGMII Interface

The RGMII interface includes 12 lines, namely rgmii_rxc, rgmii_rx_ctl, rgmii_rxd[3:0], rgmii_txc, rgmii_tx_ctl, rgmii_txd[3:0]. The user needs to provide 125MHz clock for IP through gtx_clk. Figure4-2 is the schematic diagram of connecting pin of RGMII interface and PHY chip.

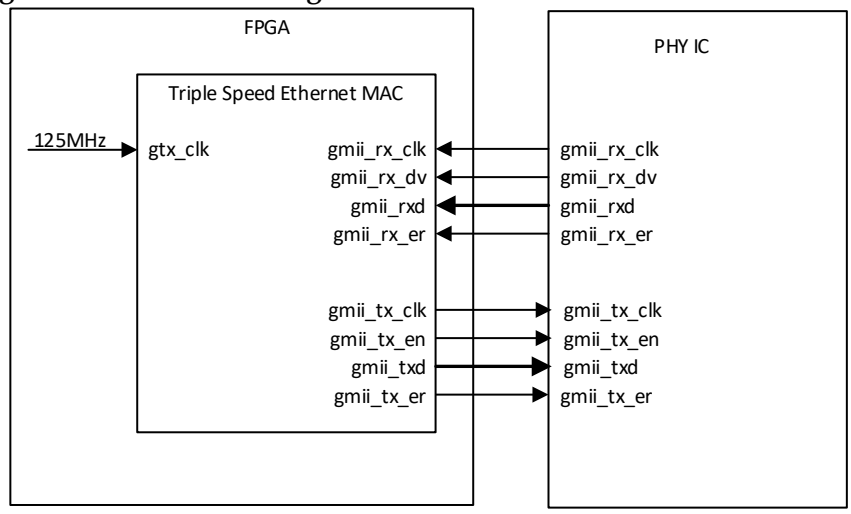
**Figure4-2 Schematic diagram of RGMII pin connection**




## 4.2.2 GMII Interface

GMII interface includes 22 lines, namely gmii_rx_clk, gmii_rx_dv, gmii_rxd[7:0], gmii_rx_er, gmii_tx_clk, gmii_tx_en, gmii_txd[7:0], gmii_tx_er. The user needs to provide 125MHz clock for IP through gtx_clk. Figure4-3 is the schematic diagram of connecting pin of GMII interface and PHY chip.

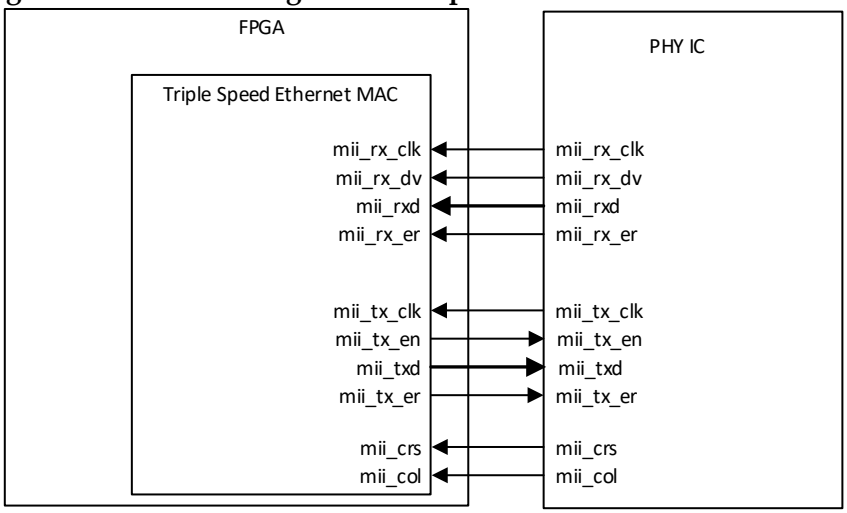
**Figure4-3 Schematic Diagram of GMII Pin Connection**



## 4.2.3 MII Interface

MII interface includes 16 lines, namely mii_rx_clk, mii_rx_dv, mii_rx_dv, mii_rxd[3:0], mii_rx_er, mii_tx_clk, mii_tx_en, mii_txd[3:0], mii_tx_er, mii_crs, mii_col. Figure4-4 is the schematic diagram of connecting pin of MII interface and PHY chip.

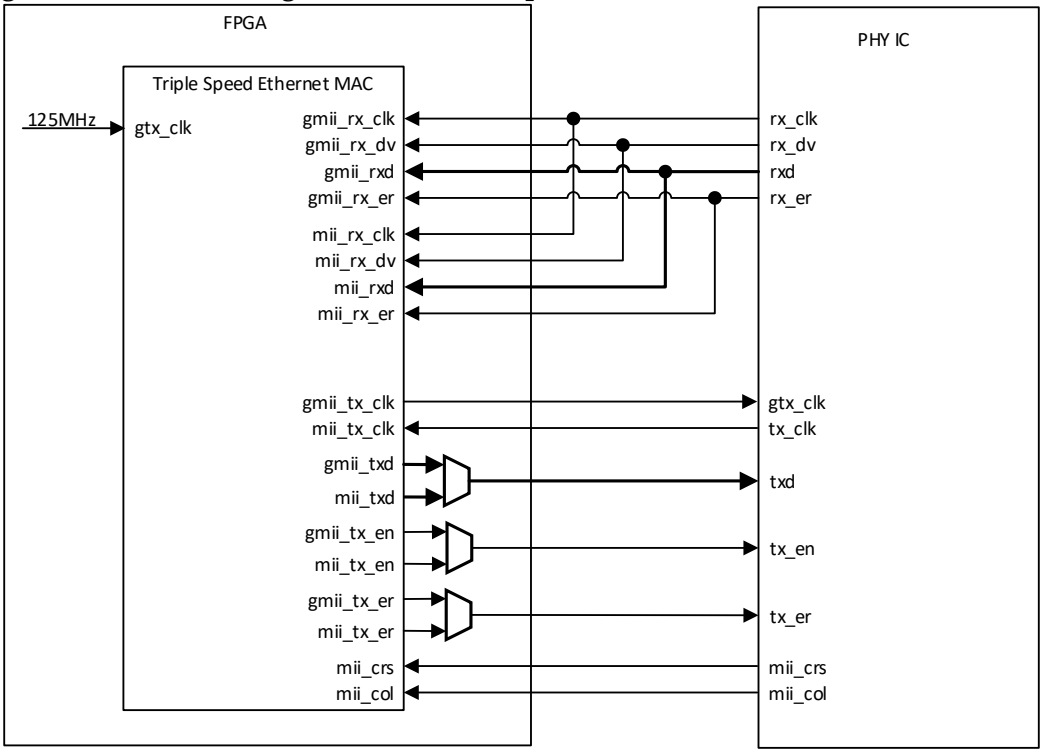
**Figure4-4 Schematic diagram of MII pin connection**




## 4.2.4 RGMII/MII Interface

GMII/MII interface is the combination of GMII interface and MII interface. It is usually connected to PHY chips supporting both GMII and MII. The transmit direction requires the user to select TXD, tx_en, and tx_er signals based on the current Ethernet rate. Figure4-5 is the schematic diagram of connecting pin of GMII/MII interface and PHY chip.

**Figure4-5 Schematic diagram of GMII/MII pin connection**



# 4.3 User Interface

## 4.3.1 Ethernet Frame Reception

Receiving Ethernet frame is the process of converting MAC interface data into user interface data. All received signals are synchronized with rx mac_clk.

**Normal Frame Reception**

Figure4-6 shows the normal Ethernet frame receiving process at1000M rate.

Figure4-7 shows the normal Ethernet frame receiving process at 10M/100M rate.

When rx_mac_valid is 1, it means that rx_mac_data for this period is valid; When rx_mac_valid and rx_mac_last are both 1, rx_mac_data for this period is valid and is the last byte of this Ethernet frame. It should be noted that there is no buffer in IP to cache the incoming Ethernet frames, so the user must always be ready to receive Ethernet frames. When the first byte of the frame begins to appear in the user interface, the data is received continuously until the entire frame is received.

**Figure4-6 Normal Ethernet Frame Reception at 1000M Rate**

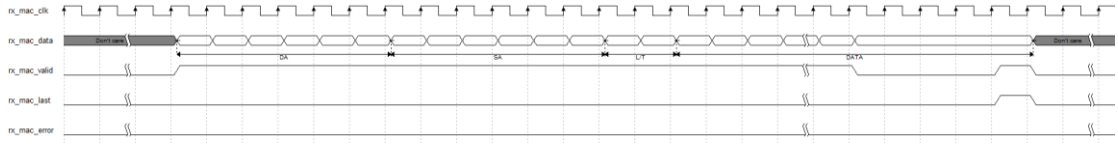
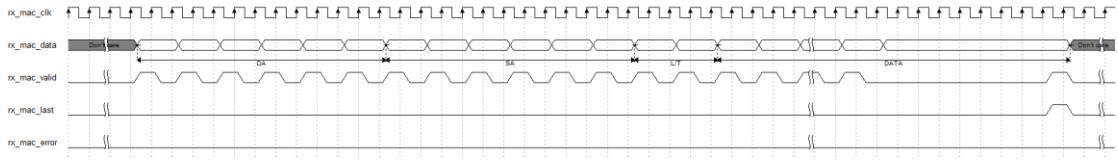



**Figure4-7 Normal Ethernet Frame Reception at 10M/100M Rate**




**Error Frame Reception**

When rx_mac_error is 1, it indicates that there are certain errors in the current frame, and the specific error type can be checked by rx_statistics_valid and rx_statistics_vector signals. Rx_mac_error indicates the error state of the current frame only if rx_mac_last is 1.Figure4-8 and Figure4-9 show the receiving process of an error frame at 1000M and 10M/100M rate respectively.

**Figure4-8 Error Ethernet Frame Reception at 1000M Rate**

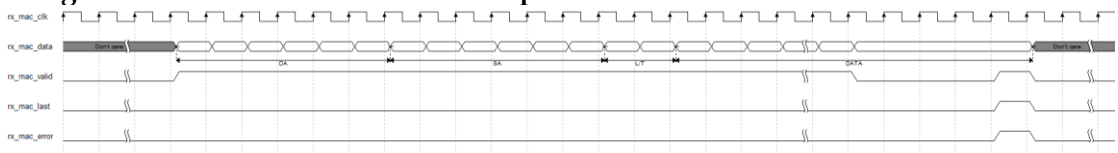
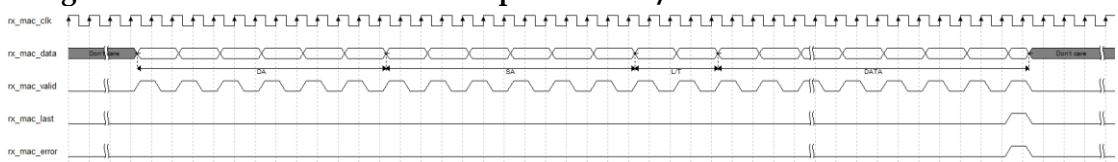



**Figure4-9 Error Ethernet Frame Reception at 10M/1000M Rate**




When the following errors occur, rx_mac_error will indicate:

1. Receiving FCS error frame ;
2. Receiving align frame;
3. In the receiving process, the MAC interface RX_ER valid signal is received ;
4. Conflicts occur in half duplex;
5. Frame length error. When the Jumbo function is disabled, receive non-vlan frame of less than 64 bytes or more than 1518 bytes, and vlan frames of less than 64 bytes or more than 1522 bytes; When Jumbo function is disabled, receive frame of less than 64 bytes.

**Received Frame FCS Forward**

When the user sets IP to the mode of receiving FCS Forward, IP will send the received FCS field to the user side, as shown in Figure4-10, Figure4-11, Figure4-12 and Figure4-13. Now, IP still automatically verifies the FCS field and indicates by rx_mac_error and rx_statistics_vector.

**Figure4-10 1000M Rate Enabling FCS Forward Correct Ethernet Frame Reception**

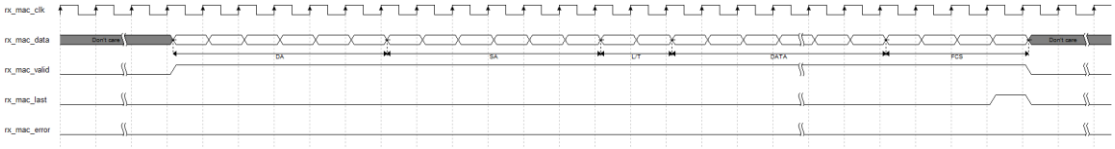



**Figure4-11 1000M Rate Enabling FCS Forward Error Ethernet Frame Reception**

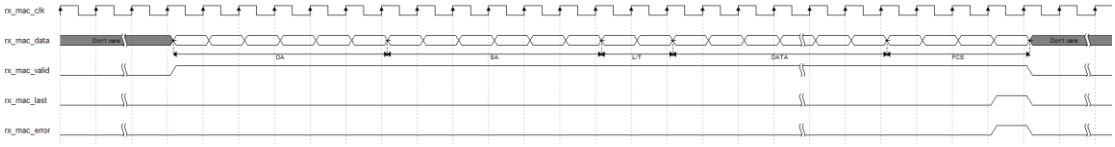



**Figure4-12 100M Rate Enabling FCS Forward Correct Ethernet Frame Reception**

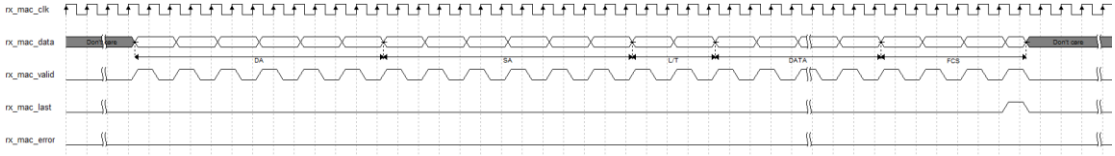
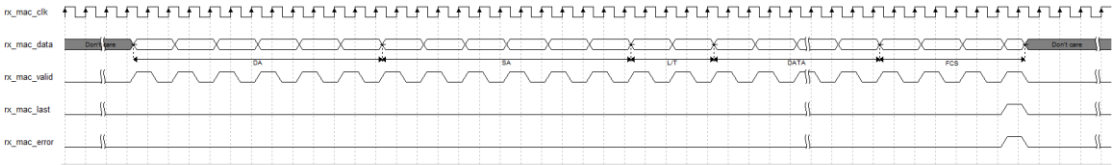


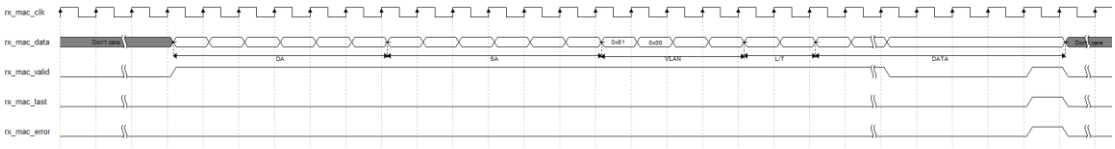

**Figure4-13 100M Rate Enabling FCS Forward Error Ethernet Frame Reception**




**VLAN Tagged Frame Reception**

When IP receives a VLAN Tagged frame, it indicates that this frame is a VLAN Tagged frame in rx_statistics_vector. VLAN Tagged frame is the 0x8100 frame which is two bits after the source MAC address. The VLAN field is defined as 4 bytes in IEEE802.3. The first two bytes is 0x8100 and the last two bytes is VLAN label, as shown in Figure4-14.

**Figure4-14 VLAN Tagged Frame Reception**



**Receiving MAC Control Frame**

When IP receives a MAC Control frame, it indicates that this frame is a MAC Control frame in rx_statistics_vector . MAC Control frame is a frame with L/T field of 0x8808 . When the L/T field is 0x8808, this frame is the MAC Control frame, which is defined in IEEE802.3.

**Reception when Ethernet line is abnormal**

Single-byte frame may occur on line in the event of an abnormal Ethernet line or a half-duplex collision. At this moment, the first rx_mac_valid and rx_mac_last of the user-side interface will be both 1, that is, after receiving a byte, the frame ends. The user application program needs to handle the occurrence of such an exception.

**Reception Statisitics**

Statistics of reception frames are output at rx_statistics_vector signal. When rx_statistics_valid is 1, it indicates that rx_statistics_vector is valid, and rx_statistics_vector indicates the statistical information of just received frames. The timing sequence is shown in Figure4-15. The bit definition of rx_statistics_vector is shown in Table 4-1

**Figure4-15 Reception Statistics**

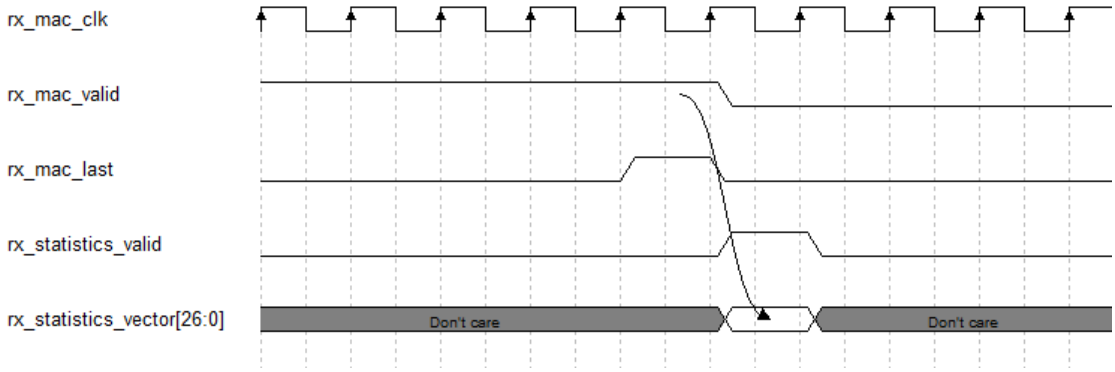


**Table 4-1 Rx_Statistics_Vector Bit Definition**

| Location | Name | Description |
|---|---|---|
| 26 | RX Alignment Error | If the received frame is not an integer multiple of bytes, set 1. |
| 25 | RX Length Error | If the received frame length does not meet the standard, set 1 |
| 24 | RX FCS Error | If the received frame has an FCS error, set 1 |
| 23 | RX_ER Error | If the MAC interface RX_ER signal is valid in the process of reception, set 1 |
| 22 | RX Collision Error | In half duplex mode, if a collision occurs during the frame reception, set 1 |
| 21:6 | RX Frame Length | The length of received frame, including FCS field |
| 5 | RX Flow Control Frame | In full duplex mode, if the received frame is a flow control frame, set 1 |
| 4 | RX MAC Control Frame | If the received frame is a MAC Control frame, set 1 |
| 3 | RX VLAN Frame | If the received frame is a VLAN frame, set 1 |
| 2 | RX Multicast Frame | If the received frame is a multicast frame, set 1 |
| 1 | RX Broadcast Frame | If the received frame is a broadcast frame, set 1 |
| 0 | RX Unicast Frame | If the received frame is a unicast frame, set 1 |

## 4.3.2 Ethernet Frame Transmission

Sending Ethernet frames is the process of converting user interface data to MAC interface data. All received signals are synchronized with tx_mac_clk.

**Normal Frame Reception**

Figure4-16 shows the normal Ethernet frame transmission process at 1000M rate.

Figure4-17 shows the normal Ethernet frame transmission process at a rate of 10M/100M in RGMII. mode. In RGMII mode, tx_mac_clk is 125MHz. At a rate of 10M, tx_mac_ready is valid for every 100 periods; At a rate of 100M, tx_mac_ready is valid for every 10 periods.

Figure4-18 shows the normal Ethernet frame transmission process at a rate of 10M/100M in MII mode.

During the entire frame transmission process, tx_mac_valid must remain at 1 until the end of the frame. When tx_mac_ready and tx_mac_last are both 1, tx_mac_data is transmitted in this period and is the last byte of the Ethernet frame for that frame. It should be noted that there is no buffer in the IP to cache the transmitted Ethernet frames. Therefore, when the first byte starts to be transmitted, the user needs to prepare subsequent bytes and assign to tx_mac_data in time when tx_mac_ready is 1 until the entire frame is transmitted.

**Figure4-16 Normal Ethernet Frame Transmission at 1000M Rate**

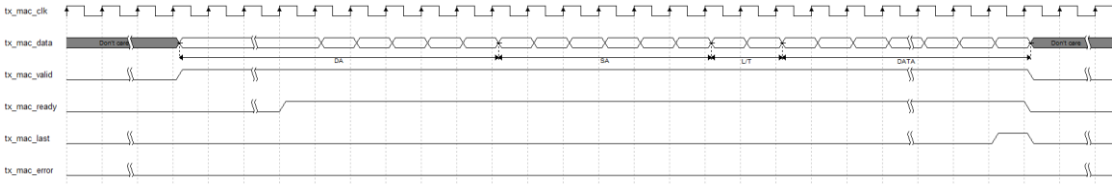



**Figure4-17 In RGMII Mode Normal Ethernet Frame Transmission at 10M/100M Rate**

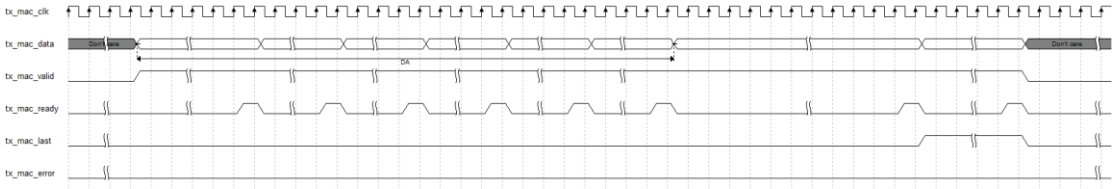
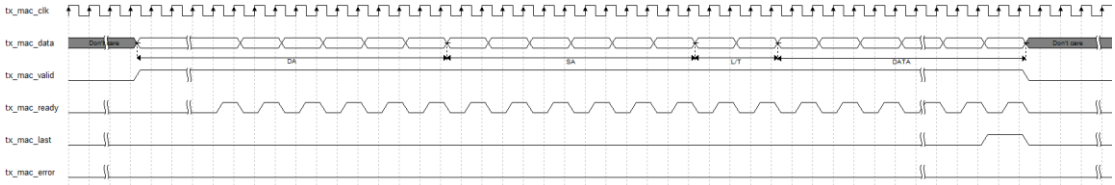



**Figure4-18 In MII Mode Normal Ethernet Frame Transmission at 10M/100M Rate**




### TX_ER Error Frame Transmission

During the transmission process, when tx_mac_error and tx_mac_ready are both 1, it indicates that there is an error in the current transmitted frame. IP will transmit TX_ER transmitted data error indication on the MAC interface.

Figure4-19 shows the transmission process of TX_ER Ethernet frame at a rate of 1000M.

Figure4-20 shows the transmission process of TX_ER Ethernet frame at a rate of 10M/100M in RGMII mode.

Figure4-21 shows the transmission process of TX_ER Ethernet frame at a rate of 10M/100M in MII mode.

**Figure4-19 TX_ER for Ethernet Frame Transmission at 1000M rate**

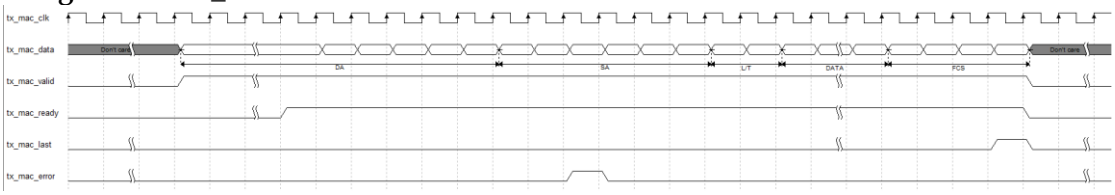



**Figure4-20 TX_ER Ethernet Frame Transmission at 10M/100M rate in RGMII Mode**

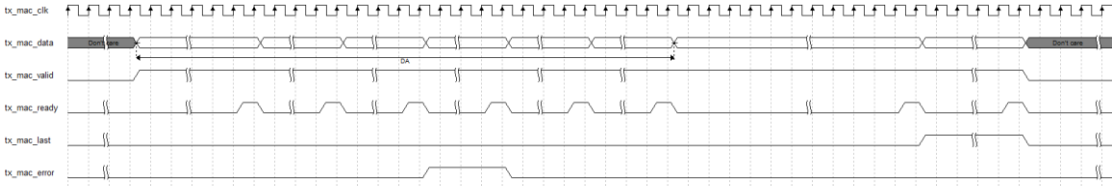
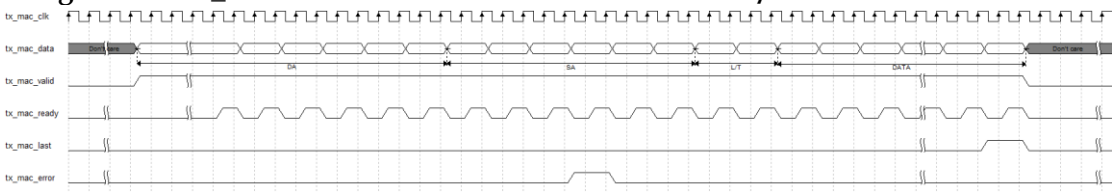



**Figure4-21 TX_ER Ethernet Frame Transmission at 10M/100M rate in MII Mode**



### Transmission Frame FCS Forward

When the user sets IP to be transmission FCS Forward mode, the IP will not automatically add FCS field. After the user transmits the DATA field, the FCS field needs to be calculated and added manually, as is shown in Figure4-22 and Figure4-23.

**Figure4-22 Enabling FCS Forward Ethernet Frames Transmission at 1000M rate**

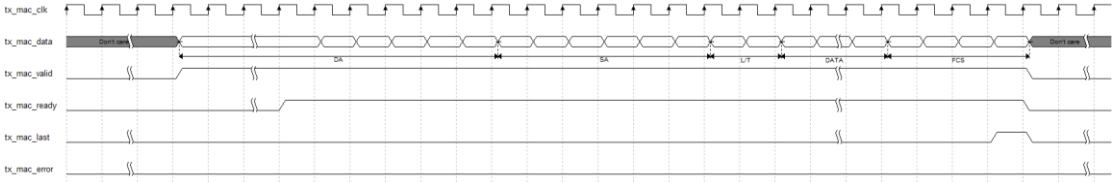
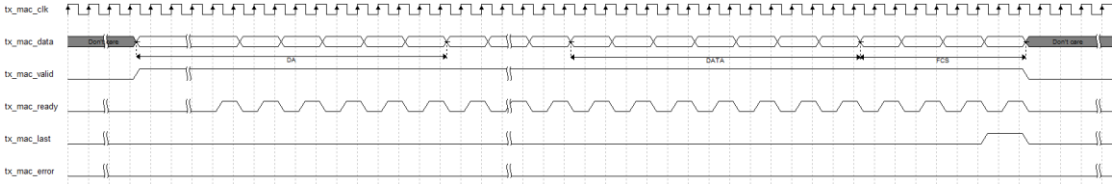



**Figure4-23 Enabling FCS Forward Ethernet Frames Transmission at 1000M rate in MII Mode**




### Transmission in half duplex mode

In half duplex mode, IP indicates the transmission state through tx_collision and tx_retransmit signal if the user does not detect any collision during the transmission. The Ethernet frames can be transmitted according to the above full duplex transmission process. If the user detects a collision during the transmission, the following should be done to ensure the correct transmission of data. When the user detects the tx_collision to be1, it means that there is a collision on the line. The user must immediately set tx_mac_valid to 0 when he detects the tx_collision to be 1, so as to end the Ethernet frame transmission. With the detection of tx_collision to be1, and if tx_retransmit is 1, it indicates that the collision is within a reasonable range, and the user can decide whether to retransmit the frame. If the user is ready to retransmit the frame, please set tx_mac_valid to 1 within 5 periods to prepare for the retransmission of the frame. If the user prepares to abort to retransmit the frame, please set tx_mac_valid to 1 after 5 periods to prepare for the next frame transmission. With the detection of tx_collision to be1, and if tx_retransmit is 0, it indicates that the collision is not within a reasonable range (a frame with more than 16 collisions, or collisions occurring after 64 bytes having been sent), then the user needs to abort the transmission of this frame.

Figure4-24 shows the retransmission process when a collision occurring.

Figure4-25 and Figure4-26 show respectively the non-retransmission process when a collision occurring.

**Figure4-24 Retransmission in Case of Collision**

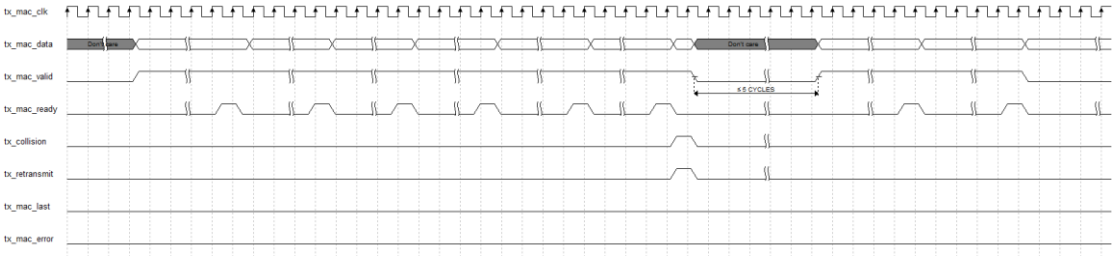



**Figure4-25Abort Retransmission in case of Collision (Actively)**

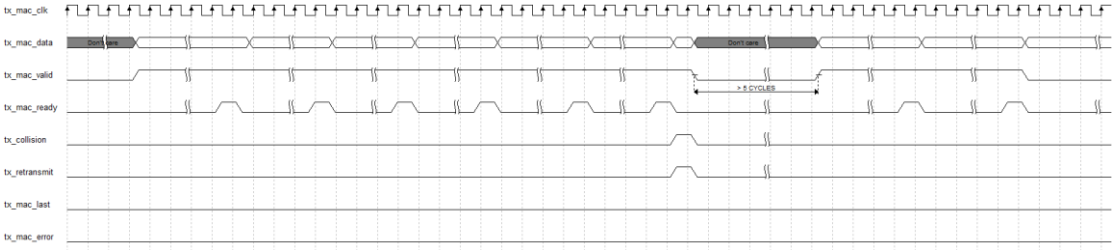
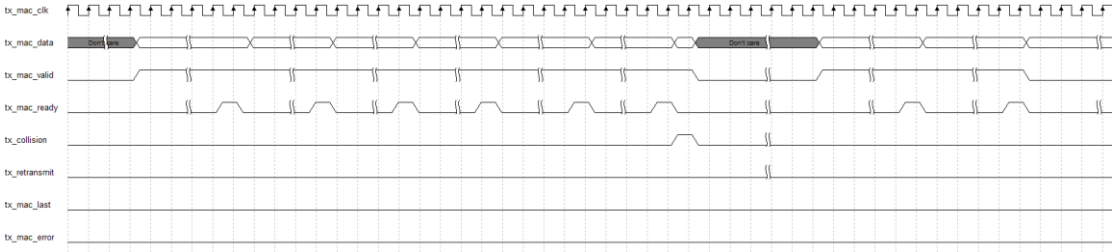



**Figure4-26Abort Retransmission in case of Collision (Passively)**




## Transmission Statisitics

Transmission frames statistics is output at tx_statistics_vector signal. When tx_statistics_valid is 1, it indicates that tx_statistics_vector is valid, and at this point tx_statistics_vector indicates the statistics information of just transmitted frames. The timing sequence is shown in Figure4-27. The bit definition of tx_statistics_vector is shown in Table 4-2..

**Figure4-27Transmission Statisitics**

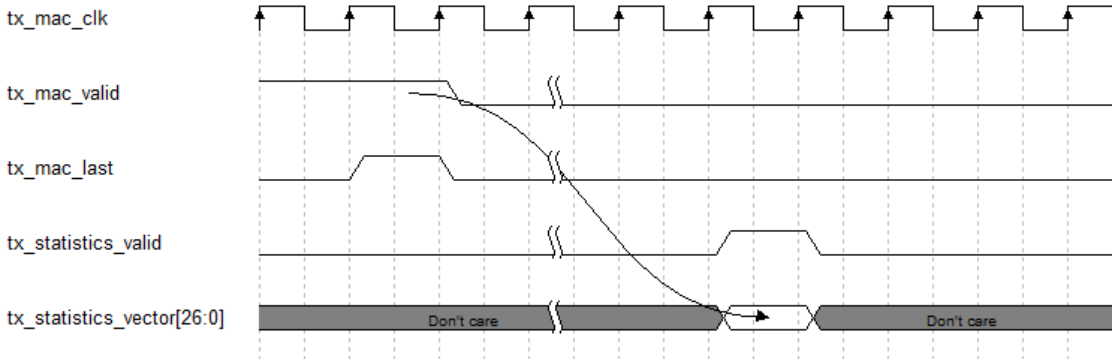


**Table 4-2 Bit Definition of tx_statistics_vector**

| Location | Name | Description |
|---|---|---|
| 28 | TX Collision | In half duplex mode, if a collision occurs when this frame is transmitted, set1. |
| 27:24 | TX Attempts | In half duplex mode, the number of times this frame was attempted to be transmitted, 0 represents the first transmission;1 represents the second transmission;15 represents the 16th transmission. |
| 23 | Excessive Collision | In half duplex mode, if the frame is on the 16th attempt to transmit, collision occurring, set 1. |
| 22 | Late Collision | If the collision occurs after 64 bytes having been transmitted, set 1 |
| 21:6 | TX Frame Length | Transmission frame length, including FCS field |
| 5 | TX Flow Control Frame | In full duplex mode, if the IP is configured to transmit a flow control frame, set 1 |
| 4 | TX MAC Control Frame | If the transmission frame is MAC Control frame, set 1 |
| 3 | TX VLAN Frame | If the transmission frame is VLAN frame, set 1 |
| 2 | TX Multicast Frame | If the transmission frame is Multicast frame, set 1 |
| 1 | TX Broadcast Frame | If the transmission frame is Broadcast frame, set 1 |
| 0 | TX Unicast Frame | If the transmission frame is Unicastt frame, set 1 |

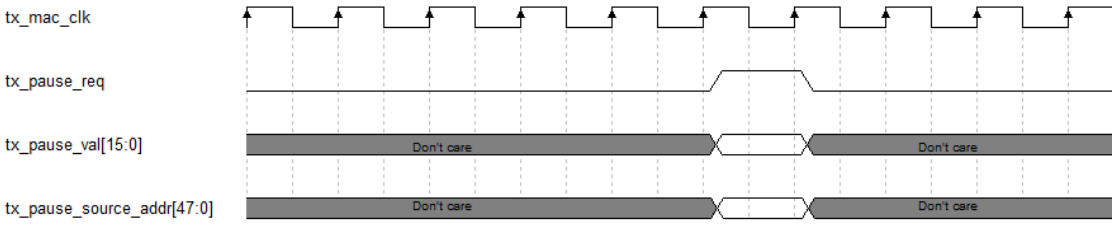
## 4.3.3 Flow Control Function

IP supports the Flow Control function in full duplex mode. In full duplex mode, user can configure IP to transmit or receive Pause frame to achieve flow control.

**Transmitting Pause Frame**

Users can set the tx_pause_req signal to 1 to transmit a pause frame. The value of tx_pause_val is inserted into the parameter field of the pause frame to calculate the pause time. Tx_pause_source_addr is transmitted as the source MAC address for the pause frame, and the transmission order is from the low to high bytes.

**Figure4-28Transmitting Pause Frame**

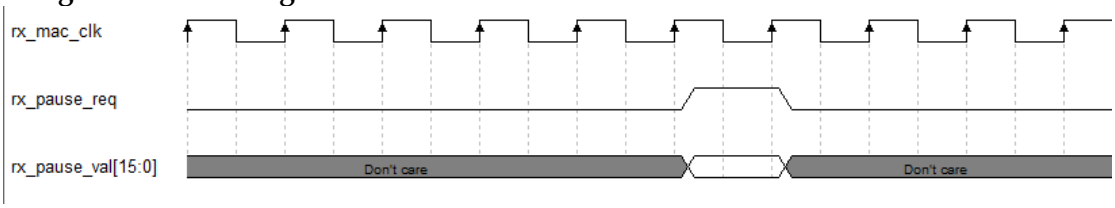



**Receiving Pause Frame**

When the IP receives a pause, it sets the rx_pause_req signal to 1. The value of rx_pause_val is the parameter field that receiving the pause

frame and is used to calculate the pause time.

**Figure4-29Receiving Pause Frame**




## 4.3.4 FCS Forward Function

IP supports FCS Forward function that configures transmission and reception respectively.

**Receiving FCS Forward function**

When the user disables the FCS Forward function, the FCS field will not be output to the user side. IP automatically verifies the FCS field and its results will be output to rx_statistics_vector corresponding field. When the user enables the FCS Forward function, the FCS field will be output to the user side. IP still automatically verifies the FCS field and its results will be output to rx_statistics_vector corresponding field.

**Transmitting FCS Forward Function**

When the user disables the FCS Forward function, the user does not need to calculate and transmit the FCS field. The IP calculates the FCS field and adds it to the Ethernet frame automatically. When the user enables the FCS Forward function, the user calculates the FCS field and transmits it to the IP on the user side.

## 4.3.5 PAD Function

When the user disables the FCS Forward function, if the frame transmitted by the user to IP is less than 60 bytes (excluding FCS), IP will automatically complement 0 to 60 bytes then add FCS field to ensure that the Ethernet frame transmitted meets the requirement of minimum 64 bytes. When the user enables the FCS Forward function, the IP will not automatically complement 64 bytes, and the actual transmitted data and length are completely determined by the user.

## 4.3.6 Transmitting IFG Setting Function

When the IP is in full duplex mode, the user can set the minimum IFG for the Ethernet transmission. When the IP is in half duplex mode, the minimum IFG transmission set by user is ignored, and the minimum IFG is still 12 bytes.

When the user disables the IFG function, IP transmits a minimum IFG of 12 bytes, or 96 bit. When the user enables the IFG function, IP determines the minimum IFG based on the user settings. If the minimum IFG set by the user is less than 8 bytes, the actual minimum IFG of IP is 8 bytes;If the user sets the minimum IFG to be greater than or equal to 8 bytes, the IP's actual minimum IFG is the value set by the user. The minimum IFG can be set to a maximum of 255 bytes.

## 4.3.7 Jumbo Setting Function

IP supports the Jumbo function. When the user disable the Jumbo function, IP judges that the correct Ethernet frame length was 64 bytes to 1518 bytes (non-vlan frames) or 64 bytes to 1522 bytes (VLAN frames). If the Ethernet frames received are not within the above range, rx_mac_error

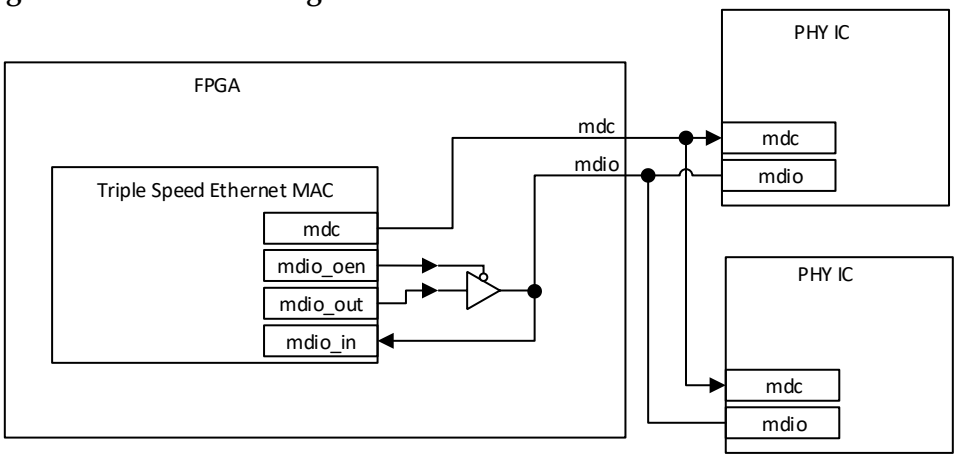
will indicate that there is an Error on this frame and RX Length Error is 1 in rx_statistics_vector. When the user enables the Jumbo function, IP judges an error only if the Ethernet frames received are smaller than 64 bytes.

### 4.3.8 Management Function

IP provides users with MIIM interface to facilitate them to configure PHY chip registers through MDC and MDIO.

MDC clock comes from CLK input clock frequency division. Users need to configure frequency divider according to CLK input clock to make MDC clock frequency meet the requirements of PHY chip. Please refer to table 6-1 for configuration method. Connection between MDC and MDIO is shown in Figure4-29.

**Figure4-30 Schematic Diagram of Connection between mdc and mdio**



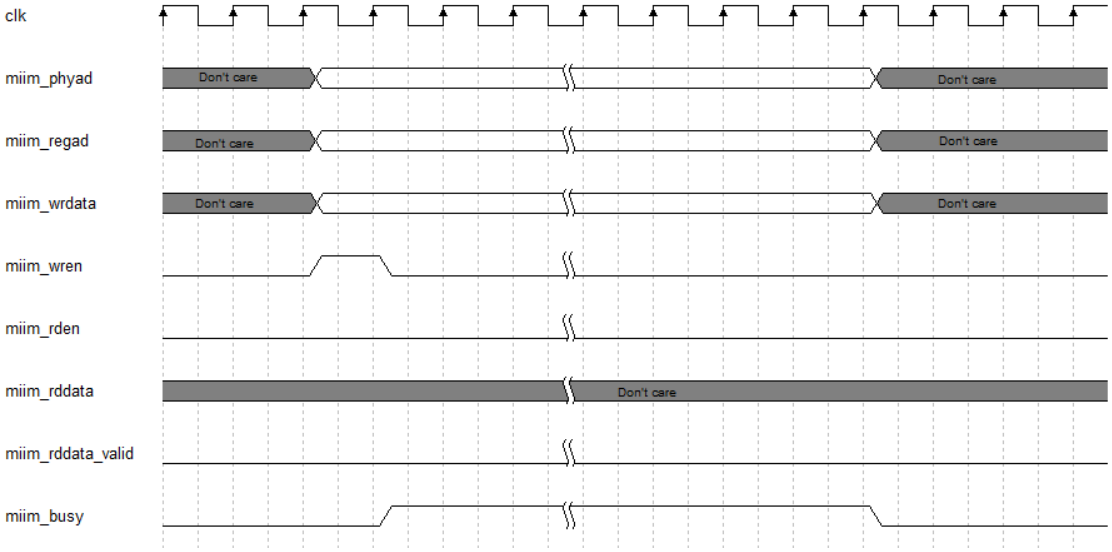

Mdio connection refers to verilog as follows:

```
assign mdio_in = mdio;
assign mdio = (!mdio_oen) ? mdio_out : 1'bz;
```

All miim interface signals are synchronized with the CLK clock.

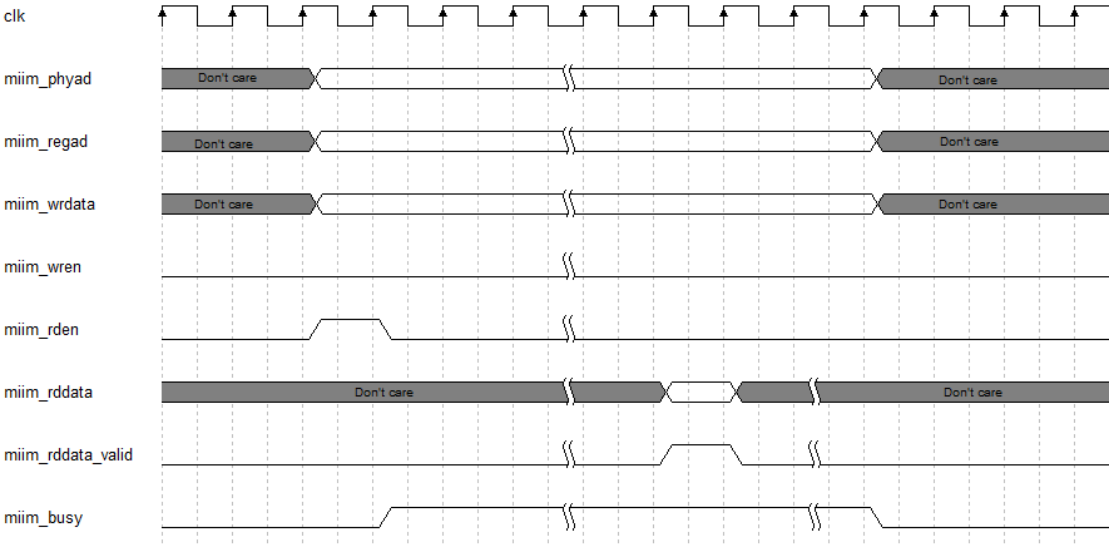
To write, the user needs to set miim_wren to 1 one period. IP will raise miim_busy, indicating that the miim bus is doing the write. When miim_busy is 0 again, it indicates this write has ended. And the user is ready for the next read or write. The miim_phyad, miim_regad, and miim_wrdata signals are ready on the bus when miim_wren is 1, and it remains unchanged when miim_wren is 1. The write timing of miim is shown in Figure4-30.

**Figure4-31 The Write Timing of miim**




To read, the user need to set miim_rden to 1 one period. IP will raise miim_busy, indicating that the miim bus is doing the read. When miim_busy is 0 again, it indicates that this read has ended and the user can do the next read or write. The miim_phyad and miim_regad signals are ready on the bus when miim_rden is 1, and it remains unchanged when miim_busy is 1. During the read, the user monitors the miim_rddata_valid signal. When miim_rddata_valid is 1, the user can sample the value of this read in the miim_rddata signal. The read timing of Miim is shown in Figure4-31.

**Figure4-32 Read Timing of Miim**



# 5 Port List

The IO port for Gowin Triple Speed Ethernet MAC IP is shown in Table 5-1.

**Table 5-1 The IO port for Gowin Triple Speed Ethernet MAC IP**

| Signal | I/O | Data Width | Description |
|---|---|---|---|
| **125MHz clock input** | | | |
| gtx_clk | input | 1 | 125M clock input. When IP uses RGMII or GMII interface, 125MHz clock should be input |
| **RGMII Interface** | | | |
| rgmii_rxc | input | 1 | RGMII receives clock |
| rgmii_rx_ctl | input | 1 | RGMII receives control |
| rgmii_rxd | input | 4 | RGMII/MII receive data |
| rgmii_txc | output | 1 | RGMII receives data |
| rgmii_tx_ctl | output | 1 | RGMII transmits control |
| rgmii_txd | output | 4 | RGMII transmits data |
| **GMII Interface** | | | |
| gmii_rx_clk | input | 1 | GMII receives clock |
| gmii_rx_dv | input | 1 | GMII receives enable |
| gmii_rxd | input | 8 | GMII receives data |
| gmii_rx_er | input | 1 | GMII receives error |
| gmii_gtx_clk | output | 1 | GMII receives clock |
| gmii_tx_en | output | 1 | GMII transmits enable |
| gmii_txd | output | 8 | GMII transmits data |
| gmii_tx_er | output | 1 | GMII transmits error |
| **MII Interface** | | | |
| mii_rx_clk | input | 1 | MII receives clock |
| mii_rx_dv | input | 1 | MII receives enable |
| mii_rxd | input | 4 | MII receives data |
| mii_rx_er | input | 1 | MII receives error |
| mii_tx_clk | input | 1 | MII transmits clock |
| mii_tx_en | output | 1 | MII transmits enable |
| mii_txd | output | 4 | MII transmits data |
| mii_tx_er | output | 1 | MII transmits error |
| mii_col | input | 1 | MII collision signal |
| mii_crs | input | 1 | MII carrier signal |
| **Interface Status Configure** | | | |
| speedis1000 | input | 1 | Selecting signal based on Ethernet rate. when IP works in RGMII or GMII/MII mode, configure IP to work at 1000M rate or 10M/100M rate:<br>1:1000M<br>0:10M/100M |
| speedis10 | input | 1 | Selecting signal based on Ethernet rate. When IP works in RGMII mode and speedis1000 is 0, the configured IP works at 10M or 100M rate:<br>1:10M<br>0:100M<br>It is should be noted when speedis1000 is1, this configuration pin is ignored |
| duplex_status | input | 1 | Ethernet duplex mode configures signal. When IP works in RGMII, MII or GMII/MII mode, configure IP working duplex mode :<br>1:half duplex<br>0:full duplex |
| **Reset** | | | |
| rstn | input | 1 | IP Reset signal, active low |
| **User Interface** | | | |
| rx_mac_clk | output | 1 | The user side receives clock |
| rx_mac_valid | output | 1 | The user side receives enable |

| Signal | I/O | Data Width | Description |
|---|---|---|---|
| rx_mac_data | output | 8 | The user side receives data |
| rx_mac_last | output | 1 | The user side receives the indication of last byte |
| rx_mac_error | output | 1 | The user side receives the indication of error frame |
| rx_statistics_valid | output | 1 | The user side receives the indication of valid statistics |
| rx_statistics_vector | output | 27 | The user side receives statistics |
| tx_mac_clk | output | 1 | The user side transmits clock |
| tx_mac_valid | input | 1 | The user side transmits enable |
| tx_mac_data | input | 8 | The user side transmits data |
| tx_mac_last | input | 1 | The user side transmits the indication of last byte |
| tx_mac_error | input | 1 | The user side transmits the indication of error frame |
| tx_mac_ready | output | 1 | The user side transmits a handshake signal. It indicates that tx_mac_data is received with a value of 1. |
| tx_collision | output | 1 | The user side transmits the line collision indicator signal. When the value is 1, it indicates that there is a line collision in this transmission and the user needs to end this transmission immediately. This signal is valid only in half duplex |
| tx_retransmit | output | 1 | The user side will transmit a retransmission indicator signal, which appears with tx_collision at the same time, and the value of 1 means that this frame needs to be retransmitted. This signal is valid only in half duplex |
| tx_statistics_valid | output | 1 | The user side transmits the indication of valid statistics |
| tx_statistics_vector | output | 29 | The user side transmits statistics |
| **IP Configure** | | | |
| rx_fcs_fwd_ena | input | 1 | Receiving FCS Forward function:<br>1:Enable receiving FCS Forward function<br>0:Disable receiving FCS Forward function |
| rx_jumbo_ena | input | 1 | Receiving Jumbo function:<br>1:Enable receiving Jumbo function<br>0:Disable receiving Jumbo function |
| rx_pause_req | output | 1 | Receiving the signal of pause frame |
| rx_pause_val | output | 16 | c |
| tx_fcs_fwd_ena | input | 1 | Transmitting FCS Forward Function<br>1:Enable receiving FCS Forward function<br>0:Disable receiving FCS Forward function |
| tx_ifg_delay_ena | input | 1 | Transmitting the minimum IFG configuration enable:<br>1: Enable the minimum IFG configuration<br>0: Disable minimum IFG configuration, and the default minimum IFG is 12 bytes |
| tx_ifg_delay | input | 8 | Transmitting minimum IFG:<br>When tx_ifg_delay_ena is 1, the minimum IFG transmitted by IP is determined by tx_ifg_delay. When tx_ifg_delay is less than 8, the minimum IFG is 8; When tx_ifg_delay is greater than or equal to 8, the minimum IFG is set by the user.<br>When tx_ifg_delay_ena is 0, this setting is invalid |
| tx_pause_req | input | 1 | Transmitting enable signal of pause frame |
| tx_pause_val | input | 16 | Transmitting the parameter field of pause frame , which means the counterpart needs to pause time. |
| tx_pause_source_addr | input | 48 | Transmitting the source address of pause frame. |
| **Management Interface** | | | |
| clk | input | 1 | Management module clock input |
| miim_phyad | input | 5 | PHY address |

| Signal | I/O | Data Width | Description |
|---|---|---|---|
| miim_regad | input | 5 | Address |
| miim_wrdata | input | 16 | Write data |
| miim_wren | input | 1 | Write enable |
| miim_rden | input | 1 | Read enable |
| miim_rddata | output | 16 | Read data |
| miim_rddata_valid | output | 1 | Read data valid |
| miim_busy | output | 1 | MIIM interface status indicator:<br>1: Reading/Writing<br>0: Idle |
| mdc | output | 1 | MDC clock |
| mdio_in | input | 1 | MDIO input |
| mdio_out | output | 1 | MDIO output |
| mdio_oen | output | 1 | MDIO output enable |

# 6 Parameter Configuration

Users are required to configure the various static and timing parameters of the Gowin Triple Speed Ethernet MAC according to the design requirements. Refer to Table 6-1.

**Table 6-1 Static and Timing Parameters of the Gowin Triple Speed Ethernet MAC**

| Name | Description | Options |
|---|---|---|
| Interface | Interface Type | RGMII,GMII,MII,GMII/MII |
| RGMII Input Delay | When using the RGMII interface, this option is used to adjust the Delay value of the input data RXD IODELAY. If the value adds 1 each time, it means the RXD IODELAY in the FPGA increases 0.025ns delay; If the value reduces 1 each time, it means the RXD IODELAY in the FPGA decreases 0.025ns delay. When the input clock and data are aligned along, this option is recommended to be set to 100, that is, RXD IODELAY in the FPGA is set to 2.5ns delay, at which time RXCLK samples RXD correctly. | User input, range from 0 to 127. |
| MIIM Clock Divider | CLK inputs clock frequency value then outputs to MDC, as the management interface clock output. If this option is less than 2, the actual frequency value is 2; If this option is greater than or equal to 2, the actual frequency value is the input value. | User input, range from 0~255 |

# 7 Reference Design

See the Triple Speed Ethernet MAC design reference for more information.

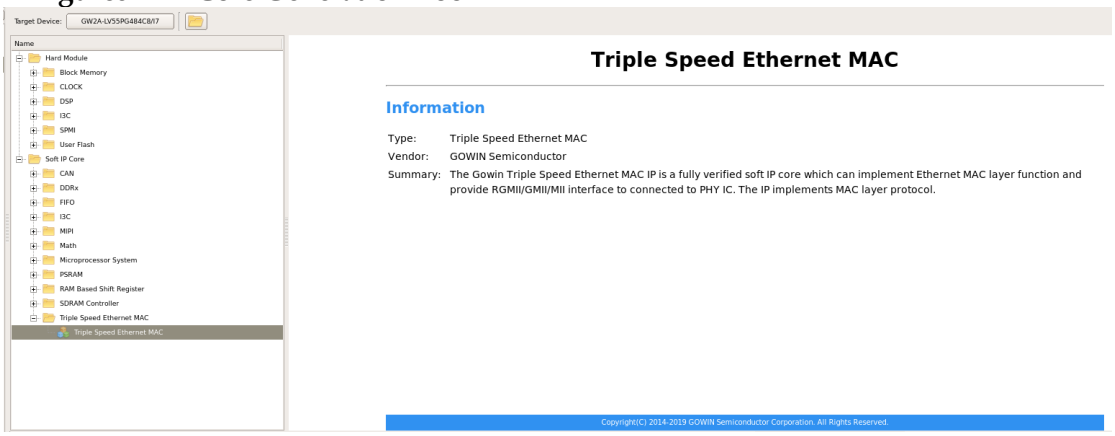
# 8 Interface Configuration

Users can invoke and configure Gowin Triple Speed Etherent MAC IP through the IP Core Generater tool in the IDE. Taking the RGMII interface pattern as an example, this section introduces the main configuration interface, the configuration process, and the implications of each configuration option.

1. Open IP Core Generater

After the user establishing the project, click on the Tools tab in the upper left corner, and pull down and click on the IP Core Generater option to open GOWIN's IP Core Generater tool and select Triple Speed Etherent MAC, as shown in Figure8-1.

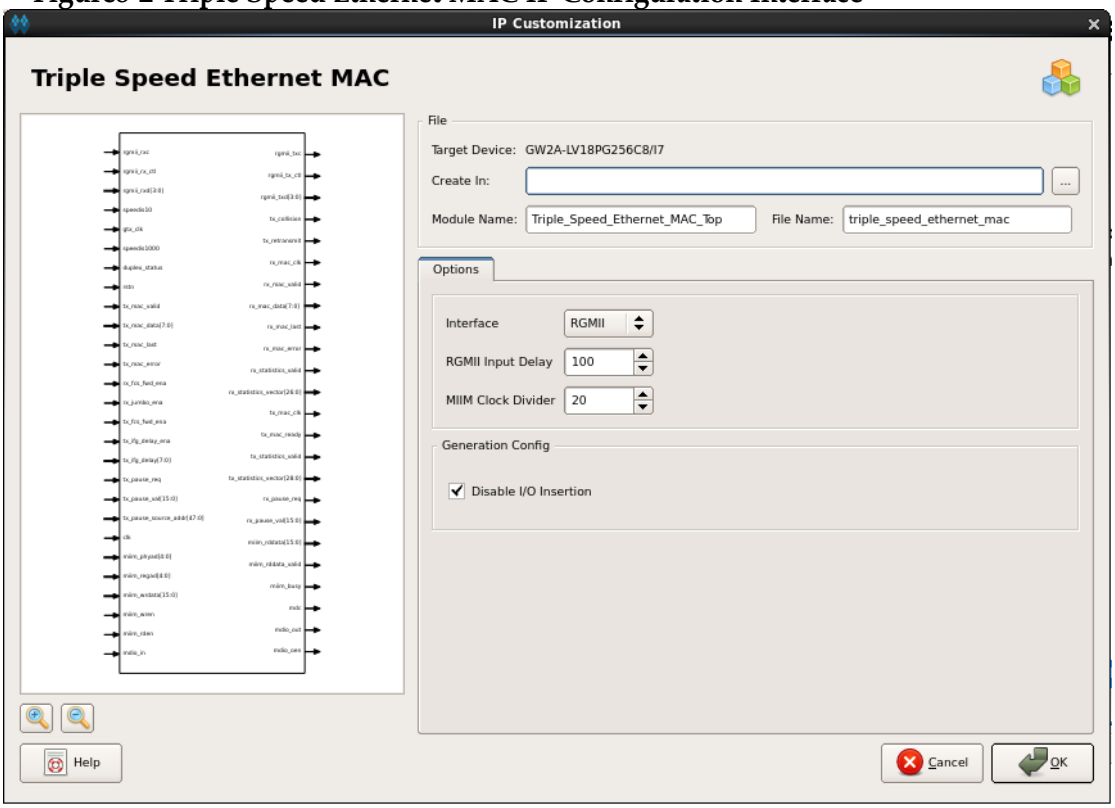
**Figure8-1 IP Core Generation Tool**




2. Triple Speed Etherent MAC port interface

On the left side of the configuration interface is the interface diagram of Triple Speed Etherent MAC IP, and on the right side are IP options, as shown in Figure8-2.

**Figure8-2 Triple Speed Ethernet MAC IP Configuration Interface**




3. Open the Help document

Users can click the Help button in the lower left corner of Figure8-2 to see the simple English introduction of various options in the configuration interface, so as to facilitate users to quickly complete the configuration of IP core, as shown in Figure8-3.

**Figure8-3 Triple Speed Ethernet MAC IP Help**

## Triple Speed Ethernet MAC

### Information

| | |
|---|---|
| Type: | Triple Speed Ethernet MAC |
| Vendor: | GOWIN Semiconductor |
| Summary: | The Gowin Triple Speed Ethernet MAC IP is a fully verified soft IP core which can implement Ethernet MAC layer function and provide RGMII/GMII/MII interface to connected to PHY IC. The IP implements MAC layer protocol. |

### Options

| Option | Description |
|---|---|
| Interface | MAC Interface connected to PHY. Providing RGMII/GMII/MII Interface. |
| RGMII Input Delay | When use RGMII Interface, the option is set to adjust the internal data delay. The range is 0 ~ 127. When the input clock and data are edge alignment, the option is suggested 100. |
| MIIM Clock Divider | The mdc divider value from pin clk. The range is 0 ~ 255. If the option is set smaller than 2, the actual divider is 2. If the option is set equal or bigger than 2, the actual divider is the value that user sets. |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