

# Gowin\_EMPU(GW1NS-4C) Hardware Design

## **Reference Manual**

IPUG932-2.0E, 03/14/2024

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## **Revision History**

Date	Version	Description		
04/20/2020	1.0E	Initial version published.		
02/08/2021	1.1E	<ul> <li>AHB PSRAM Memory Interface peripheral supported.</li> <li>AHB HyperRAM Memory Interface peripheral supported.</li> <li>APB SPI Nor Flash peripheral supported.</li> <li>GPIO supports multiple port types.</li> <li>I<sup>2</sup>C supports multiple port types.</li> <li>ARM Keil MDK as well as GOWIN MCU Designer upgraded.</li> </ul>		
06/21/2021	1.2E	<ul> <li>Known issue of SPI full duplex read and write fixed.</li> <li>Synplify Pro removed.</li> <li>FPGA software upgraded.</li> <li>Reference design updated.</li> </ul>		
12/16/2022	1.3E	<ul> <li>Known issue of port signal name fixed.</li> <li>MCU IP updated and logic resources optimized.</li> <li>Software development kit updated.</li> </ul>		
03/14/2024	2.0E	<ul><li>System clock frequency and performance boosted.</li><li>Hardware reference design updated.</li></ul>		

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## **1** Hardware Architecture

## **1.1 System Architecture**

Gowin\_EMPU(GW1NS-4C) is an on-chip system consisting of MCU core system and FPGA core system, as shown in Figure 1-1.



Figure 1-1 System Architecture

MCU core system consists of MCU Core, AHB and peripherals, AHB2APB Bridge, APB1 and peripherals.

FPGA core system consists of the clock and reset signal input, data

SRAM, instruction FLASH of MCU core system, APB2 Bridge, APB2 and peripherals.

## **1.2 System Feature**

Gowin\_EMPU(GW1NS-4C) includes two sub-systems:

- MCU core system
- FPGA core system

## 1.2.1 MCU Core System

MCU core system includes:

- MCU Core:
  - ARM Cortex-M3 Core, ARM architecture v7-M Thumb2 supporting 16-bit and 32-bit instruction set
  - DAP (Debug Access Port)
  - Bus Matrix
  - NVIC (Nested Vector Interrupt Controller)
  - TPIU (Trace Port Interface Unit)
- AHB and peripherals
  - GPIO
  - AHB2 Master user extension interface
  - AHB2 Slave user extension interface
- AHB2APB Bridge
- APB and peripherals
  - UART0
  - UART1
  - Timer0
  - Timer1
  - Watch Dog
  - RTC
  - APB2 Extension Interface

## 1.2.2 FPGA Core System

FPGA core system includes:

- External crystal oscillator clock input or internal crystal oscillator clock can be as the system clock source of MCU core system. The max. frequency of the system clock is up to 200MHz (Subject to the project design and the chip in use).
- The reset signal input can be as the system reset signal of MCU core system.
- Six user interrupt handling signals for user extension peripherals
- AHB Extension interface
  - SRAM and FLASH can be as the data and instruction memory respectively of MCU core system
  - One AHB2 Master user extension interface
  - One AHB2 Slave user extension interface
- APB2 Extension Interface
  - SPI Master
  - I<sup>2</sup>C Master
  - Twelve APB2 Master user extension interfaces
- Memory
  - The SRAM Size can be configured as 2KB, 4KB, 8KB and 16KB.
  - The FLASH Size as 32KB.

## 1.3 System Port

The definition of system ports is as shown in Table 1-1.

Name	I/O	Data Width	Description	Module
sys_clk	in	1	System clock signal	-
reset_n	in	1	System reset signal	-
trace_clk	out	1	TPIU clock signal	трш
trace_data	out	[3:0]	TPIU data output signal	TPIO
user_int_0	in	1	User Interrupt handling signal 0	
user_int_1	in	1	User Interrupt handling signal 1	NVIC

#### Table 1-1 Definition of System Ports

Name	I/O	Data Width	Description	Module
user_int_2	in	1	User Interrupt handling signal 2	
user_int_3	in	1	User Interrupt handling signal 3	
user_int_4	in	1	User Interrupt handling signal 4	
user_int_5	in	1	User Interrupt handling signal 5	
gpio	inout	[15:0]	GPIO signal	GPIO I/O
gpioin	in	[15:0]	GPIO input signal	
gpioout	out	[15:0]	GPIO output signal	GPIO non-I/O
gpioouten	out	[15:0]	GPIO output enable signal	
uart0_rxd	in	1	UART0 receive signal	
uart0_txd	out	1	UART0 transmit signal	UARTU
uart1_rxd	in	1	UART1 receive signal	
uart1_txd	out	1	UART1 transmit signal	UARI1
scl	inout	1	I <sup>2</sup> C serial clock signal	l <sup>2</sup> C Master I/O
sda	inout	1	I <sup>2</sup> C serial data signal	
sclin	in	1	I <sup>2</sup> C serial clock input signal	· I <sup>2</sup> C Master non-I/O
sclout	out	1	I <sup>2</sup> C serial clock output signal	
sclouten	out	1	I <sup>2</sup> C serial clock output enable	
sdain	in	1	l <sup>2</sup> C sorial data input signal	
sdaout		1	1 <sup>2</sup> C sorial data autout signal	
sdaouton	out	1		
Suadulen	out	1	signal	
mosi	out	1	SPI master output / slave input	
miso	in	1	SPI master input / slave output	
sclk	out	1	SPI clock signal	SPI Master
nss	out	1	SPI slave selection signal	
rtc_src_clk	in	1	RTC signal	RTC
master_hclk	out	1	Master clock signal	
master_hrst	out	1	Master reset signal	AHB2 Master
master_hsel	out	1	Master selection signal	
master_haddr	out	[31:0]	Master address signal	
master_htrans	out	[1:0]	Master transmit type signal	

Name	I/O	Data Width	Description	Module
master_hwrite	out	1	I/O of Master read and write signal	
master_hsize	out	[2:0]	Master transmit Size signal	
master_hburst	out	[2:0]	Master burst type signal	
master_hprot	out	[3:0]	Master protect and control signal	
master_memattr	out	[1:0]	Master memattr signal	
master_exreq	out	1	Matter exreq signal	
master_hmaster	out	[3:0]	Master label signal	
master_hwdata	out	[31:0]	Master write data signal	
master_hmastlock	out	1	Master lock signal	
master_hreadymux	out	1	Master hreadymux signal	
master_hauser	out	1	Master hauser signal	
master_hwuser	out	[3:0]	Master hwuser signal	
master_hrdata	in	[31:0]	Master read data signal	
master_hreadyout	in	1	Master hreadyout signal	
master_hresp	in	1	Master transmit status signal	
master_exresp	in	1	Master exresp signal	
master_hruser	in	[2:0]	Master hruser signal	
slave_hsel	in	1	Slave selection signal	
slave_haddr	in	[31:0]	Slave address signal	
slave_htrans	in	[1:0]	Slave transmit type signal	
slave_hwrite	in	1	I/O of Slave read and write signal	
slave_hsize	in	[2:0]	Slave transmit Size signal	
slave_hburst	in	[2:0]	Slave burst type signal	
slave_hprot	in	[3:0]	Slave protect and control signal	
slave_hmaster	in	[3:0]	Slave label signal	ADD2 Slave
slave_hwdata	in	[31:0]	Slave write data signal	
slave_hmastlock	in	1	Slave lock signal	
slave_hrdata	out	[31:0]	Slave read data signal	
slave_hready	out	1	Slave ready signal	
slave_hresp	out	1	Slave transmit status signal	
slave_hexresp	out	1	Slave hexresp signal	

Name	I/O	Data Width	Description	Module
slave_hruser	out	[2:0]	Slave hruser signal	
slave_hmemattr	in	[1:0]	Slave hmemattr signal	
slave_hexreq	in	1	Slave hexreq signal	
slave_hauser	in	1	Slave hauser signal	
slave_hwuser	in	[3:0]	Slave hwuser signal	
master_pclk	out	1	APB2 Master clock signal	
master_prst	out	1	APB2 Master reset signal	
master_penable	out	1	APB2 Master enable signal	
master_paddr	out	[7:0]	APB2 Master address signal	ADD2 Mostor
master_pwrite	out	1	I/O of APB2 Master read and write signal	[1-12]
master_pwdata	out	[31:0]	APB2 Master write data signal	
master_pstrb	out	[3:0]	APB2 Master write strobe signal	
master_pprot	out	[2:0]	APB2 Master protect type signal	
master_psel1	out	1	APB2 Master [1] selection signal	
master_pready1	in	1	APB2 Master [1] ready Signal	
master_prdata1	in	[31:0]	APB2 Master [1 ] read data signal	APB2 Master [1]
master_pslverr1	in	1	APB2 Master[ ] transmit failure signal	
master_psel2	out	1	APB2 Master [2] selection signal	
master_pready2	in	1	APB2 Master [2] ready Signal	
master_prdata2	in	[31:0]	APB2 Master [2 ] read data signal	APB2 Master [2]
master_pslverr2	in	1	APB2 Master[ ] transmit failure signal	
master_psel3	out	1	APB2 Master [3] selection signal	
master_pready3	in	1	APB2 Master [3] ready Signal	
master_prdata3	in	[31:0]	APB2 Master [3 ] read data signal	APB2 Master [3]
master_pslverr3	in	1	APB2 Master[ ] transmit failure signal	
master_psel4	out	1	APB2 Master [4] selection signal	
master_pready4	in	1	APB2 Master [4] ready signal	AFDZ WASIER [4]

Name	I/O	Data Width	Description	Module
master_prdata4	in	[31:0]	APB2 Master [4 ] read data signal	
master_pslverr4	in	1	APB2 Master[] transmit failure signal	
master_psel5	out	1	APB2 Master [5] selection signal	
master_pready5	in	1	APB2 Master [5] ready signal	
master_prdata5	in	[31:0]	APB2 Master [5 ] read data signal	APB2 Master [5]
master_pslverr5	in	1	APB2 Master[ ] transmit failure signal	
master_psel6	out	1	APB2 Master [6] selection signal	
master_pready6	in	1	APB2 Master [6] ready signal	
master_prdata6	in	[31:0]	APB2 Master [6 ] read data signal	APB2 Master [6]
master_pslverr6	in	1	APB2 Master[] transmit failure signal	
master_psel7	out	1	APB2 Master [7] selection signal	
master_pready7	in	1	APB2 Master [7] ready signal	
master_prdata7	in	[31:0]	APB2 Master [7 ] read data signal	APB2 Master [7]
master_pslverr7	in	1	APB2 Master[ ] transmit failure signal	
master_psel8	out	1	APB2 Master [8] selection signal	
master_pready8	in	1	APB2 Master [8] ready signal	
master_prdata8	in	[31:0]	APB2 Master [8 ] read data signal	APB2 Master [8]
master_pslverr8	in	1	APB2 Master[] transmit failure signal	
master_psel9	out	1	APB2 Master [9] selection signal	
master_pready9	in	1	APB2 Master [9] ready signal	
master_prdata9	in	[31:0]	APB2 Master [9 ] read data signal	APB2 Master [9]
master_pslverr9	in	1	APB2 Master[] transmit failure signal	
master_psel10	out	1	APB2 Master [10] selection	APB2 Master [10]

Name	I/O	Data Width	Description	Module
			signal	
master_pready10	in	1	APB2 Master [10] ready signal	
master_prdata10	in	[31:0]	APB2 Master [10 ] read data signal	
master_pslverr10	in	1	APB2 Master[ ] transmit failure signal	
master_psel11	out	1	APB2 Master [11 ] selection signal	
master_pready11	in	1	APB2 Master [11 ] ready signal	
master_prdata11	in	[31:0]	APB2 Master [11 ] read data signal	APB2 Master [11]
master_pslverr11	in	1	APB2 Master[11] transmit failure signal	
master_psel12	out	1	APB2 Master [12] selection signal	
master_pready12	in	1	APB2 Master [12] ready signal	
master_prdata12	in	[31:0]	APB2 Master [12 ] read data signal	APB2 Master [12]
master_pslverr12	in	1	APB2 Master[12] transmit failure signal	

## **1.4 System Resource Utilization and Performance**

## **Statistics**

The system resource utilization and performance statistics of Gowin\_EMPU(GW1NS-4C) are as shown in Table 1-2 .

Table 1-2 System Resource Uti	lization and Performance Statistics
-------------------------------	-------------------------------------

Resources	1     Te	Registers	BSRAMe	Frequency
Configuration	LUIS	Tregisters	DOIVAIVIS	(MHz)
MCU core system	33	19	4	200
MCU core system + I2C Master + SPI Master	456	282	4	100
MCU core system + APB SPI-Flash Memory	1073	618	4	50
MCU core system + AHB PSRAM Memory	1709	1464	4	100
MCU core ssystem + AHB HyperRAM Memory	1163	1008	4	100

# **2** Hardware Design Flow

## 2.1 Hardware Target

- DK-START-GW1NSR4C-QN48G V1.1
   GW1NSR-LV4CQN48GC7/I6
- DK-START-GW1NSR4C-QN48P V1.1
   GW1NSR-LV4CQN48PC7/I6
- DK-START-GW1NSR4C-MG64P V1.1
   GW1NSR-LV4CMG64PC7/I6

## 2.2 Software Version

Tested software version: Gowin\_V1.9.9.01 (64-bit)

## 2.3 IP Core Generator

The IP Core Generator tool from Gowin Software is used to configure and generate Gowin\_EMPU(GW1NS-4C) IP Core.

## 2.4 Programmer

Gowin Programmer tool is used to download the bitstream file of Gowin\_EMPU(GW1NS-4C).

For the Gowin Programmer usage, please refer to <u>SUG502, Gowin</u> <u>Programmer User Guide</u>.

## 2.5 Design Flow

Gowin\_EMPU(GW1NS-4C) hardware design flow is as follows:

• Configure and generate Gowin\_EMPU(GW1NS-4C) IP Core using IP

Core Generator and import the current project.

- Instantiate Gowin\_EMPU(GW1NS-4C), import user design, and connect user design with Gowin\_EMPU Top Module.
- Add physical and timing Constraints.
- Use GowinSynthesis to synthesize and generate post-synthesis netlist file.
- Use Place & Route to generate bitstream file.
- Use Programmer to download bitstream file to chip to chip.

# **3** Project Template

## 3.1 Project Creation

#### 3.1.1 Create a New Project

Double click to open the Gowin Software. Click "File > New... > FPGA Design Project" on the menu bar, as shown in Figure 3-1.

Figure 3-1 Create a FPGA Design Project

🗱 GOWIN FPGA Designer - [Start Page]	_	
♀ File Edit Project Tools Window	Help	_ 8 ×
	» 🔁 🛍 🛛 🔀 👶 👫 🎫 🎟 🖂	
Recent Projects:	Quick Start           Image: Project solution of the sol	· · · · · · · · · · · · · · · · · · ·
% Console Message		

#### 3.1.2 Set Project Name and Path

Enter the project name and select the project path, as shown in Figure 3-2.

Figure 3-2 Set Project Name and Path

🐳 Project Wizard		×
🔿 Project Name	Project Name	
Select Device Summary	Enter a name for your project, and specify a directory where the project will be stored. The directory will be created if it doesn't exist.	
	Name: gowin_empu Create in: F:/	]
	Next > Canc	el

#### 3.1.3 Select Device

Configure "Series", "Device", "Device Version", "Package", "Speed", and "Part Number", as shown in Figure 3-3.

Take DK\_START\_GW1NSR4C\_QN48G\_V1.1 reference design as an instance.

- Series: GW1NSR
- Device: GW1NSR-4C
- Device Version: Any
- Package: QFN48G
- Speed: C7/I6
- Part Number: GW1NSR-LV4CQN48GC7/I6

W Project Wizard								
Project Name	Select Device							
Select Device	Specify a target device for your Filter	r proj	ect					
	Series:	GW	1NSR	~	Package:	QFN48G		~
	Device:	GW	1NSR-4C	~	Speed:	C7/I6		~
	Device Version: *no version number is initial version	Any		~				
	Part Number		Device	Device	Version	Package	Speed	Voltage
	GW1NSR-LV4CQN48GC7/I6		GW1NSR-4C			QFN48G	C7/I6	LV
	<							>
						< <u>B</u> ack	<u>N</u> ext >	Cancel

#### Figure 3-3 Select Device

## 3.1.4 Project Creation Completed

Project creation is completed, as shown in Figure 3-4.

#### **Figure 3-4 Project Creation Completed**

🐳 Project Wizard			×
♀ Project Wizard Project Name Select Device ♥ Summary	Summary Project Name: gowin_empu Directory: F:\ Source Directory: F:\gowin_empu\src Implementation Directory: F:\gowin_empu\impl Device Part Number: GWINSR-LV4CQN48GC7/I6 Series: GWINSR Device: GWINSR-C		×
	Package: QFN48G Speed: C7/I6		
		< <u>B</u> ack <u>Finish</u> Cancel	

## 3.2 Hardware Design

Use IP Core Generator to generate Gowin\_EMPU(GW1NS-4C) hardware design.

Select "Tools > IP Core Generator" in the menu bar or " to open the IP Core Generator.

Select " Soft IP Core > Microprocessor System > Hard-Core-MCU > Gowin EMPU(GW1NS-4C) 2.0", as shown in Figure 3-5.



Figure 3-5 Select Gowin\_EMPU(GW1NS-4C) IP Core

The system architecture of Gowin\_EMPU(GW1NS-4C) is as shown in Figure 3-6.

The grayed modules are the default, and you can not configure; If the modules are not grayed, you can open the modules to configure.

The modules that you can choose to configure include:

- TPIU
- NVIC: six user interrupt handling signals USER\_INT0~5
- AHB2 Slave: FPGA core system can extend AHB2 Slave peripherals.
- AHB2 Master: FPGA core system can extend AHB2 Master peripherals.

- GPIO
- UART0 and UART1
- RTC
- The SRAM can be configured as 2KB, 4KB, 8KB or 16KB, 16KB by default.
- I<sup>2</sup>C: FPGA core system integrates I<sup>2</sup>C Master.
- SPI: FPGA core system integrates SPI Master.
- APB2 Master[1 -12]: FPGA core system can extend twelve APB2 Master user devices.

**Figure 3-6 System Architecture** 🐳 Gowin EMPU ?  $\times$ General Device: GW1NSR-4C Part Number: GW1NSR-LV4CQN48GC7/I6 ... Create In: F:\gowin\_empu\src\gowin\_empu File Name: gowin\_empu Module Name: Gowin\_EMPU\_Top Language: Verilog ~ MCU JTAG IF DAP Cortex-M3 TPIU IF TPIU Bus Matrio FPGA Fabric USER\_INT[0-5] NVIC AHB2 Slave Extension SRAM FLASH AHB2 Slave AHB AHB2 Master Extension AH B2 Master LITE SRAM/FLASH IF GPIO IF BUS GPIO Clock/Reset AHB2APB Clock/Res APB1 A PB2 82 Extension IF A PB2 Bridge UARTO IF Timer0 UARTO A PB2 12C SPI Master[1-12] UART1 IF UART1 Timer1 æ, RTCIF RTC Natch Dog Q ОК Cancel

The system configuration options of Gowin\_EMPU(GW1NS-4C) are as shown in Table 3-1.

Options	Description
Enable TPIU	Enable TPIU, disabled by default
Enable USER_INT_0	Enable user interrupt handling signal [0], disabled by default.
Enable USER_INT_1	Enable user interrupt handling signal [1], disabled by default.
Enable USER_INT_2	Enable user interrupt handling signal [2], disabled by default.
Enable USER_INT_3	Enable user interrupt handling signal [3], disabled by default.
Enable USER_INT_4	Enable user interrupt handling signal [4], disabled by default.
Enable USER_INT_5	Enable user interrupt handling signal [5], disabled by default.
Enable GPIO	Enable GPIO, disabled by default.
Enable GPIO I/O	Enable GPIO inout port, enabled by default.
Enable UART0	Enable UART0, disabled by default.
Enable UART1	Enable UART1, disabled by default.
Enable RTC	Enable RTC, disabled by default.
Enable AHB2 Master	Enable AHB2 Master user extension interface, disabled by default.
Enable AHB2 Slave	Enable AHB2 Slave user extension interface, disabled by default.
Enable I <sup>2</sup> C	Enable I <sup>2</sup> C Master, disabled by default.
Enable I <sup>2</sup> C I/O	Enable I <sup>2</sup> C inout port, enabled by default.
Enable SPI	Enable SPI Master, disabled by default.
Enable APB2 Master 1	Enable APB2 Master [1] user extension interface, disabled by default.
Enable APB2 Master 2	Enable APB2 Master [2] user extension interface, disabled by default.
Enable APB2 Master 3	Enable APB2 Master [3] user extension interface, disabled by default.
Enable APB2 Master 4	Enable APB2 Master [4] user extension interface, disabled by default.
Enable APB2 Master 5	Enable APB2 Master [5] user extension interface, disabled by default.
Enable APB2 Master 6	Enable APB2 Master [6] user extension interface, disabled by default.
Enable APB2 Master 7	Enable APB2 Master [7] user extension interface, disabled by default.
Enable APB2 Master 8	Enable APB2 Master [8] user extension interface, disabled by default.
Enable APB2 Master 9	Enable APB2 Master [9] user extension interface, disabled by default.
Enable APB2 Master 10	Enable APB2 Master [10] user extension interface, disabled by default.
Enable APB2 Master 11	Enable APB2 Master [11] user extension interface, disabled by default.
Enable APB2 Master 12	Enable APB2 Master [12] user extension interface, disabled by default.
SRAM Size	The SRAM Size can be configured as 2KB, 4KB, 8KB and 16KB, 16KB by default.

## 3.2.1 TPIU Configuration

Double click to configure TPIU, as shown in Figure 3-7.

If "Enable TPIU" is selected, Gowin\_EMPU(GW1NS-4C) supports TPIU, disabled by default.

Figure 3-7 TPIU Configuration



#### 3.2.2 NVIC Configuration

Double click to open NVIC to configure USER\_INT\_0~5 for user extension peripherals of FPGA core system, as shown in Figure 3-8.

- If Enable USER\_INT\_0 is selected, Gowin\_EMPU(GW1NS-4C) supports user interrupt handling signal [0], disabled by default.
- If Enable USER\_INT\_1 is selected, Gowin\_EMPU(GW1NS-4C) supports user interrupt handling signal [1], disabled by default.
- If Enable USER\_INT\_2 is selected, Gowin\_EMPU(GW1NS-4C) supports user interrupt handling signal [2], disabled by default.
- If Enable USER\_INT\_3 is selected, Gowin\_EMPU(GW1NS-4C) supports user interrupt handling signal [3], disabled by default.
- If Enable USER\_INT\_4 is selected, Gowin\_EMPU(GW1NS-4C) supports user interrupt handling signal [4], disabled by default.

 If Enable USER\_INT\_5 is selected, Gowin\_EMPU(GW1NS-4C) supports user interrupt handling signal [5], disabled by default.

Figure 3-8 NVIC Configuration

🚴 NVIC	? ×
NVIC	
ys_ck	There are six user interrupt signals from NVIC of Gowin_EMPU to FPGA Fabric.If user extends soft- core peripherals, USER_INT_0~5 can be as interrupt signals for soft-core peripherals.
use_int_2 use_int_3 use_int_4	Options Configuration Enable USER_INT_0 Enable USER_INT_1
Gowin EMPU	Cancel

#### 3.2.3 GPIO Configuration

Double click to configure GPIO, as shown in Figure 3-9.

- If "Enable GPIO" is selected, Gowin\_EMPU(GW1NS-4C) supports GPIO, disabled by default.
- If "Enable GPIO" is selected, you can configure GPIO port type.
- If "Enable GPIO I/O" is selected, GPIO supports inout port, supported by default.

👶 GPIO	? ×
GPIO	<b>&amp;</b>
sys ck	Gowin_EMPU contains a set of GPIO,which can be accessed and controlled through AHB bus. The GPIO block interconnects with the FPGA Fabric where user implements general purpose I/O functions. This AHB GPIO is a general-purpose I/O interface unit and provides a 16-bit I/O interface.
apid (5.0	Options
Grwin FMPU	Interface: Enable GPIO I/O
	OK Cancel

#### Figure 3-9 GPIO Configuration

## 3.2.4 UART Configuration

Double click to configure UART0 or UART1, as shown in Figure 3-10.

- If "Enable UART0" is selected, Gowin\_EMPU(GW1NS-4C) supports UART0, disabled by default.
- If "Enable UART1" is selected, Gowin\_EMPU(GW1NS-4C) supports UART1, disabled by default.

錄 UARTO/UART1	? ×
UART0/UART1	
ys_ck west_n	asynchronous receiver / transceiver, which can be accessed and controlled through APB1 bus.Both UART supports maximum BAUD rate at 921.6Kbit/s. The APB UART supports 8-bit communication without parity, fixed at one stop bit per configuration.
uarti_tod	Options
	<ul> <li>✓ Enable UART0</li> <li>✓ Enable UART1</li> </ul>
Gowin EMPU	
	OK Cancel

#### Figure 3-10 UART Configuration

#### 3.2.5 AHB2 Master / Slave Configuration

Double click to configure AHB2 Master or AHB2 Slave, as shown in Figure 3-11.

- If "Enable AHB2 Master" is selected, Gowin\_EMPU(GW1NS-4C) supports AHB2 Master, disabled by default.
- If "Enable AHB2 Slave" is selected, Gowin\_EMPU(GW1NS-4C) supports AHB2 Slave, disabled by default.
- The base address mapping of AHB2 Master user extension peripherals is 0xA0000000.

HB2 Master/Slave			?	
HB2 Mast	er/Slave			
		The user can extend AHB2 bus to support a high speed peripheral as master, or support Gowin_EMPU as a slave.Extend AHB2 bus to FPGA fabric, user can design AHB2 high speed		
▶ sys_clk	master_hck	peripherals soft core as master or design Gowin_EMPU as high speed slave.		
reset_n	master_hrst			
save_hrdata(310)	master_hsel			
slave_hready	master_haddi(310)			
save_hresp	master_htrans(1:0)			
save_hexresp	master_hwrite			
save_hruser(2:0)	master_hsize(20)			
save heel	master_hburst(20)			
dwo baddd21-0	master_hprot(30)			
anve_nadulat.of	master_hmemattr(1:0)			
slave_htrans(1:0)	master_hexreq			
siave_hwrite	master_hmaster(30)	Ontions		
slave_hsize(2:0)	master_hwdata(31:0)			
save_hburst(20)	master_hmastlock	AHB2 Master		
slave_hprot(3:0)	master hreadymux	AHB2 Master Address Size(KB)		
slave_hmemattr(1:0)	master hauser	Gradie AHP2 Master, 0x0000000 64		
slave_hexreq	marter burrent 200			
slave_hmaster(30)	maske_invoise(30)	AHB2 Slave		
slave_hwdata(31:0)	master_nicata( s to)	☑ Enable AHB2 Slave		
save hmasterlock	master_hreadyout			
	master_hresp			
save_nauser	master_hexresp			
<ul> <li>sbve_hwuser(3:0)</li> </ul>	master_hruser(20)			
Gowin	EMPU 🔍 🔍			

Figure 3-11	AHB2	Master/Slave	Configuration
riguie 5-11	AIIDZ	wiaster Slave	Comiguiation

## 3.2.6 SRAM Configuration

Double click to configure SRAM Size, as shown in Figure 3-12.

The SRAM Size can be configured as 2KB, 4KB, 8KB or16KB, 16KB by default.

💑 SRAM	? ×
SRAM	<b>&amp;</b>
→ ys_⊆k	There are four SRAM sizes for Gowin_EMPU.First size is 2KB, uses one BSRAM as SRAM.Second size is 4KB, uses two BSRAM as SRAM.Third size is 8KB, uses four BSRAM as SRAM.The other size is 16KB, uses eight BSRAM as SRAM.The default size is 16KB.
	Options
Gowin EMPU	Configuration SRAM Size: 16KB

Figure 3-12 SRAM Configuration

## 3.2.7 I<sup>2</sup>C Configuration

Double click to configure I<sup>2</sup>C Master, as shown in Figure 3-13.

- If "Enable I<sup>2</sup>C" is selected, Gowin\_EMPU(GW1NS-4C) supports I<sup>2</sup>C Master, disabled by default.
- If "Enable I2C" is selected, you can configure I<sup>2</sup>C Master port type.
- If "Enable I2C I/O" is selected, I<sup>2</sup>C Master supports inout port, supported by default.

IPUG932-2.0E





#### 3.2.8 SPI Configuration

Double click to configure SPI Master, as shown in Figure 3-14.

If "Enable SPI" is selected, Gowin\_EMPU(GW1NS-4C) supports SPI Master, disabled by default.



Figure 3-14 SPI Configuration

## 3.2.9 RTC Configuration

Double click to configure RTC, as shown in Figure 3-15.

If "Enable RTC" is selected, Gowin EMPU(GW1NS-4C) supports RTC, disabled by default.

The port rtc src clk is input a 3.072MHz clock, internally divided by the RTC to 1Hz.



Figure 3-15 RTC Configuration

#### 3.2.10 APB2 Master Configuration

Double click to configure APB2 Master[1 -12], as shown in Figure 3-16.

- If "Enable APB2 Master 1" is selected, Gowin EMPU(GW1NS-4C) supports APB2 Master [1], disabled by default.
- If "Enable APB2 Master 2" is selected, Gowin EMPU(GW1NS-4C) supports APB2 Master [2], disabled by default.
- If "Enable APB2 Master 3" is selected, Gowin EMPU(GW1NS-4C) supports APB2 Master [3], disabled by default.
- If "Enable APB2 Master 4" is selected, Gowin EMPU(GW1NS-4C) supports APB2 Master [4], disabled by default.
- If "Enable APB2 Master 5" is selected, Gowin\_EMPU(GW1NS-4C)

supports APB2 Master [5], disabled by default.

- If "Enable APB2 Master 6" is selected, Gowin\_EMPU(GW1NS-4C) supports APB2 Master [6], disabled by default.
- If "Enable APB2 Master 7" is selected, Gowin\_EMPU(GW1NS-4C) supports APB2 Master [7], disabled by default.
- If "Enable APB2 Master 8" is selected, Gowin\_EMPU(GW1NS-4C) supports APB2 Master [8], disabled by default.
- If "Enable APB2 Master 9" is selected, Gowin\_EMPU(GW1NS-4C) supports APB2 Master [9], disabled by default.
- If "Enable APB2 Master 10" is selected, Gowin\_EMPU(GW1NS-4C) supports APB2 Master [10], disabled by default.
- If "Enable APB2 Master 11" is selected, Gowin\_EMPU(GW1NS-4C) supports APB2 Master [11], disabled by default.
- If "Enable APB2 Master 12" is selected, Gowin\_EMPU(GW1NS-4C) supports APB2 Master [12], disabled by default.



Figure 3-16 APB2 Master[1-12] Configuration

The base address mapping of APB2 Master [1-12] user extension peripherals is as shown in Table 3-2.

APB2 Master	Address	Size(Byte)
1	0x40002400	256
2	0x40002500	256
3	0x40002600	256
4	0x40002700	256
5	0x40002800	256
6	0x40002900	256
7	0x40002A00	256
8	0x40002B00	256
9	0x40002C00	256
10	0x40002E00	256
11	0x40002E00	256
12	0x40002F00	256

Table 3-2 Base Address Mapping of APB2 Master [1-12]

#### 3.2.11 PSRAM Memory Interface

If FPGA product GW1NSR-4C MG64P is selected, Gowin\_EMPU (GW1NS-4C) supports the FPGA core system extended external device PSRAM Memory Interface.

The software development kit provides the external device PSRAM Memory Interface as a reference design.

#### Hardware Design Flow

- IP Core Generator is used to configure and generate Gowin\_EMPU (GW1NS-4C) IP Core, and the AHB2 Master user extension interface is enabled.
- IP Core Generator is used to configure and generate PSRAM Memory Interface IP Core.
  - Memory Clock 100MHz
  - For other options, you can select default configuration.
- Design the AHB PSRAM Memory Interface IP implementing the AHB bus interface, refer to gw\_ahb\_psram.v.
- Instantiate Gowin\_EMPU(GW1NS-4C) Top Module and AHB PSRAM Memory Interface Top Module.
- Connect Gowin\_EMPU(GW1NS-4C) to AHB interface of AHB PSRAM

Memory Interface.

#### **Reference Design**

You can click here to get the following reference design:

- Hardware Reference Design ····
   \ref\_design\FPGA\_RefDesign\DK\_START\_GW1NSR4C\_MG64P\_V1.
   1\gowin\_empu\cm3\_psram\_demo
- Software Programming Reference Design
  - ...\ref\_design\MCU\_RefDesign\MDK\_RefDesign\cm3\_demo\proje ct\psram
  - ...\ref\_design\MCU\_RefDesign\GMD\_RefDesign\cm3\_demo\proje ct\psram

#### 3.2.12 HyperRAM Memory Interface

If FPGA product GW1NSR-4C or GW1NSER-4C QN48P is selected, Gowin\_EMPU (GW1NS-4C) supports the FPGA core system extended external device HyperRAM Memory Interface.

The software development kit provides the external device HyperRAM Memory Interface as a reference design.

#### Hardware Design Flow

- IP Core Generator is used to configure and generate Gowin\_EMPU (GW1NS-4C), and AHB2 Master user extension interface is enabled.
- IP Core Generator is used to configure and generate HyperRAM Memory Interface embedded IP Core.
  - Memory Clock 100MHz
  - For other options, you can select default configuration.
- Design AHB HyperRAM Memory Interface IP implementing the AHB bus interface, refer to gw\_ahb\_hyperram.v.
- Instantiate Gowin\_EMPU(GW1NS-4C) Top Module and AHB HyperRAM Memory Interface Top Module.
- Connect Gowin\_EMPU(GW1NS-4C) to AHB interface of AHB HyperRAM Memory Interface.

#### **Reference Design**

You can click <u>here</u> to get the following reference design:

Hardware Reference Design

•••

\ref\_design\FPGA\_RefDesign\DK\_START\_GW1NSR4C\_QN48P\_V1.
1\gowin\_empu\cm3\_hyperram\_demo

- Software Programming Reference Design
  - ...\ref\_design\MCU\_RefDesign\MDK\_RefDesign\cm3\_demo\proje ct\hyper\_ram
  - ...\ref\_design\MCU\_RefDesign\GMD\_RefDesign\cm3\_demo\proje ct\hyper\_ram

#### 3.2.13 SPI-Flash Memory

If FPGA product GW1NSR-4C or GW1NSER-4C QN48G is selected, Gowin\_EMPU (GW1NS-4C) supports the FPGA core system extended external device SPI-Flash Memory.

The software development kit provides the external device SPI-Flash Memory as a reference design.

#### Hardware Design Flow

- You can configure and generate Gowin\_EMPU (GW1NS-4C) IP Core using IP Core Generator, and APB2 Master [1] user extension interface is enabled.
- Design SPI-Flash Memory IP, refer to gw\_spiflash.v.
- Design APB SPI-Flash Memory IP implementing the APB bus interface, refer to gw\_spiflash.v.
- Instantiate Gowin\_EMPU(GW1NS-4C) Top Module and APB SPI-Flash Memory Top Module.
- Connect Gowin\_EMPU(GW1NS-4C) to APB interface of APB SPI-Flash Memory.

#### **Reference Design**

You can click <u>here</u> to get the following reference design:

- Hardware Reference Design ···· \ref\_design\FPGA\_RefDesign\DK\_START\_GW1NSR4C\_QN48G\_V1.
   1\gowin\_empu\cm3\_spiflash\_demo
- Software Programming Reference Design
  - ...\ref\_design\MCU\_RefDesign\MDK\_RefDesign\cm3\_demo\proje ct\spi\_flash
  - ...\ref\_design\MCU\_RefDesign\GMD\_RefDesign\cm3\_demo\proje ct\spi\_flash

## 3.3 User Design

- After configuration, you can generate Gowin\_EMPU(GW1NS-4C) IP Core.
- Instantiate Gowin\_EMPU(GW1NS-4C) Top Module.
- Import user design and connect it with Gowin\_EMPU(GW1NS-4C) Top Module to form a complete RTL design.

## 3.4 Constraint

After RTL design is completed, physical constraints can be generated according to the used development board and the IO.

Timing constraints file can be generated according to timing requirements.

For the details on physical constraints generation, please refer to <u>SUG940, Gowin Design Timing Constraints Guide</u>, <u>SUG935, Gowin</u> <u>Design Physical Constraints Guide</u>.

## 3.5 Configuration

#### 3.5.1 Synthesize Configuration

The "Synthesize" configuration is as shown in Figure 3-17.

- Configure "Top Module/Entity" according to the top module name in the design.
- Configure "Include Path" according to the file path in the design.
- Configure Verilog Language, such as System Verilog 2017.

Synthesize         General         Constraints         Synthesize         General         General         Synthesize         General         General         V Place & Route         General         Voltage         Place         Route         Dual-Purpose Pin         Unused Pin         Show All Warnings         Show All Warnings         Disable Insert Pad         Ram R/W Check	🐳 Configuration	>	
Route     Looplimit:     2000       Dual-Purpose Pin     Show All Warnings       V BitStream     Disable Insert Pad       General     Ram R/W Check       sysControl     Feature sysControl	<ul> <li>Configuration</li> <li>Global General Constraints</li> <li>Synthesize General</li> <li>Place &amp; Route General Voltage Place</li> </ul>	Synthesize General Synthesis Tool:  GowinSynthesis Top Module/Entity: gowin_empu_demo Include Path: TclPre GowinSynthesis Varilog Language: Surtem Varilog 2017, x	
	Place Route Dual-Purpose Pin Unused Pin ❤ BitStream General sysControl Feature sysControl	Verilog Language: System Verilog 2017 V Looplimit: 2000 Show All Warnings Disable Insert Pad Ram R/W Check	

#### Figure 3-17 Synthesize Configuration

## 3.5.2 Place Configuration

Configure the "Place" option as shown in Figure 3-18.

For example, select "2" for "Place Option" to enhance the software timing.

🗱 Configuration		
	Place	
✓ Global General Constraints	Category: All V Label	Reset all to default Value
✓ Synthesize General	Place input registers to IOB Place output registers to IOB	True True
✓ Place & Route General	Place inout registers to IOB Place Option	True 2
Voltage Place	Replicate Resources	False
Route Dual-Purpose Pin Unused Pin		
✓ BitStream General sysControl		
Feature sysControl		
		OK Cancel Apply

#### Figure 3-18 Place Configuration

## 3.5.3 Route Configuration

Configure the "Route" option as shown in Figure 3-19.

For example, select "2" for "Route Option" to enhance the software timing.

🔆 Configuration		
	Route	
✓ Global General	Category: All ~	Reset all to default
Constraints	Label	Value
✓ Synthesize	Clock Route Order	0
General	Run Timing Driven	True
✓ Place & Route	Route Option	2
General	Route Maxfan	23
Voltage Place	Correct Hold Violation	True
Route		
Dual-Purpose Pin Unused Pin		
✓ BitStream		
General		
sysControl		
Feature sysControl		
		OK Cancel Apply

#### Figure 3-19 Route Configuration

## 3.5.4 Bitstream Configuration

Configure the "Bitstream" option as shown in Figure 3-20.

🔆 Configuration		×
	BitStream	
<ul> <li>Global         <ul> <li>General</li> <li>Constraints</li> </ul> </li> <li>Synthesize             <ul></ul></li></ul>	<ul> <li>☑ Enable CRC Check</li> <li>□ Enable Compress</li> <li>☑ Enable Security Bit</li> <li>□ Secure Mode</li> <li>☑ Power On Reset Monitor</li> <li>☑ Print BSRAM Initial Value</li> <li>Bitstream Format: Text ∨</li> </ul>	
	OK Cancel Appl	у

## 3.6 Synthesize

Run GowinSynthesis to complete the synthesis of RTL design to generate post-synthesis netlist file, as shown in Figure 3-21.





For the tool usage, please refer to <u>SUG100, Gowin Software User</u> <u>Guide.</u>

## 3.7 Place & Route

Run the Place & Route tool in Gowin software and generate the bitstream file, as shown in Figure 3-22.

GOWIN FPGA Designer - [F:\gowin_empu	\impl\pnr\gowin_empu.rpt.html] - 🗆	×
📄 <u>F</u> ile <u>E</u> dit <u>P</u> roject <u>T</u> ools <u>W</u> indow <u>H</u>	delp	- 8 ×
	. 🗅 🗈 👪 🔀 👶 👭 💷 🎟 🖂 🏟 🔡 🏈	
Process & X	PnR Details	*
<ul> <li>User Constraints</li> <li>FloorPlanner</li> <li>Timing Constraints Editor</li> <li>Synthesize</li> <li>Synthesis Report</li> <li>Netlist File</li> <li>Place &amp; Route</li> <li>Place &amp; Route Report</li> <li>Timing Analysis Report</li> <li>Ports &amp; Pins Report</li> <li>Power Analysis Report</li> </ul>	<ul> <li>PnR Messages</li> <li>PnR Details</li> <li>PnR Details</li> <li>Resource</li> <li>Resource Usage Summary</li> <li>Global Clock Usage Summary</li> <li>Global Clock Signals</li> <li>Pinout by Port Name</li> <li>All Package Pins</li> <li>All Package Pins</li> <li>CPU time = 0h om 2.308s, Elapsed time = 0h 0m 0.308</li> <li>Pitot Time and Memory Usage</li> <li>CPU time = 0h om 0.308s, Elapsed time = 0h 0m 0.308</li> <li>Pinout by Port Name</li> <li>CPU time = 0h om 0.308</li> <li>Pinout by Port Name</li> <li>CPU time = 0h om 0.328</li> <li>Pitot Time and Memory Usage</li> <li>CPU time = 0h om 0.308s, Elapsed time = 0h 0m 0.325</li> <li>CPU time = 0h om 0.5, Elapsed time = 0h 0m 0.259s</li> <li>Routing Phase 1: CPU time = 0h om 0.259s, Elapsed time = 0h 0m 0.259s</li> <li>CPU time = 0h om 0.384s, Elapsed time = 0h 0m 0.382s</li> <li>Global Clock Signals</li> <li>Pinout by Port Name</li> <li>CPU time = 0h om 3s, Elapsed time = 0h om 0.382s</li> <li>CPU time = 0h om 3s, Elapsed time = 0h om 0.382s</li> </ul>	35 75 75 75
- Programmer		-
Design Process Hierarchy	9 Start Page 🛛 Design Summary 🖾 🔽 gowin empu demo.y 🖾 💆 gowin empurat.htm	
Console Ternerate file "F:\gowin_empu\impl Generate file "F:\gowin_empu\impl Generate file "F:\gowin_empu\impl Generate file "F:\gowin_empu\impl Wed Jan 17 13:29:36 2024	<pre>\pmr\gowin_empu.power.ntml completed \pmr\gowin_empu.pin.html" completed \pnr\gowin_empu.rpt.html" completed \pnr\gowin_empu.rpt.txt" completed \pnr\gowin_empu.tr.html" completed</pre>	₽ ×
% Console Message		

#### Figure 3-22 Place & Route

For the tool usage, please refer to <u>SUG100, Gowin Software User</u> Guide.

## 3.8 Download

Download the bitstream file using Gowin Programmer.

Open Programmer in Gowin software or under the installation path.

Click "Edit > Configure Device" on the menu bar or "Configure Device" (, on the tool bar to open the "Device configuration".

If FPGA product GW1NS-4C or GW1NSR-4C is selected, configuration options are as shown in Figure 3-23.

- Select "MCU Mode" in "Access Mode" drop-down list.
- Select "Firmware Erase, Program" or "Firmware Erase, Program, Verify" in "Operation" drop-down list.

	_
🙀 Device configuration	? ×
Device Operation	
Access Mode:	MCV Mode 🗸 🗸
Operation:	Firmware Erase, Program 🗸 🗸
Firmware Erase, Progr	an
File name: F:/gowin_er	npu/impl/pnr/gowin_empu.fs
-FW/MCU/Binary Input Op Firmware/Binary File:	tions _demo/project/spi_flash/mdk_v5/spi_flash.bin Save Cancel

Figure 3-23 Download Configuration for GW1NS-4C/GW1NSR-4C

If FPGA product GW1NSER-4C is selected, configuration options are as shown in Figure 3-24.

- Select "SecureFPGA Mode" in "Access Mode" drop-down list.
- Select "Firmware Erase, Program Securely" in "Operation" drop-down list.

Figure 3-24 Download Configuration for GW1NSER-4C

🙀 Device configuration		? ×
Device Operation		
Access Mode:	SecureFPGA Mode	$\sim$
Operation:	Firmware Erase, Program Securely	$\sim$
Firmware Erase, Progra Key Authentication Cod	um,Verify with Security(One Time Programma le)	ble For
Programming Options		
File name: F:/gowin_em	pu/impl/pnr/gowin_empu.fs	
User Flash Initiali:	ration	
FW/MCU/Binary Input Op	tions	
Firmware/Binary File:	_demo/project/spi_flash/mdk_v5/spi_flash.1	bin
	Save	Cancel

Import hardware design bitstream file in "Programming Options > File

name".

• Click "Save" to complete the configuration.

#### Note!

Import software programming Binary file in " FW/MCU Input Options > Firmware/Binary File", please refer to <u>IPUG928, Gowin\_EMPU(GW1NS-4C) IDE Software Reference</u> <u>Manual</u>.

After device configuration, click Program/Configure ", on the Programmer tool bar to complete downloading of hardware design bitstream file and software programming Binary file.

For the usage of Programmer, please refer to <u>SUG502, Gowin</u> <u>Programmer User Guide</u>.

# **4** Reference Design

Gowin\_EMPU(GW1NS-4C) provides hardware reference design in Gowin Software (tested software version V1.9.9.01 (64-bit)). You can click <u>here</u> to get the following reference design.

- ...\ref\_design\FPGA\_RefDesign\DK\_START\_GW1NSR4C\_MG64P\_V
   1.1\gowin\_empu\cm3\_psram\_demo
- ...\ref\_design\FPGA\_RefDesign\DK\_START\_GW1NSR4C\_QN48G\_V
   1.1\gowin\_empu\cm3\_i2c\_demo
- ...\ref\_design\FPGA\_RefDesign\DK\_START\_GW1NSR4C\_QN48G\_V
   1.1\gowin\_empu\cm3\_spiflash\_demo
- ...\ref\_design\FPGA\_RefDesign\DK\_START\_GW1NSR4C\_QN48P\_V
   1.1\gowin\_empu\cm3\_ahb2\_demo
- ...\ref\_design\FPGA\_RefDesign\DK\_START\_GW1NSR4C\_QN48P\_V
   1.1\gowin\_empu\cm3\_apb2\_demo
- ...\ref\_design\FPGA\_RefDesign\DK\_START\_GW1NSR4C\_QN48P\_V
   1.1\gowin\_empu\cm3\_demo
- ...\ref\_design\FPGA\_RefDesign\DK\_START\_GW1NSR4C\_QN48P\_V
   1.1\gowin\_empu\cm3\_hyperram\_demo
- ...\solution\RTOS\ref\_design\FPGA\_RefDesign\gowin\_empu
- ...\solution\RunInSRAM\_FromEmbFlash\ref\_design\FPGA\_RefDesign \gowin\_empu
- ...\solution\RunInSRAM\_FromSIPFlash\ref\_design\FPGA\_RefDesign\ gowin\_empu

