Gowin Power Analyzer

User Guide

SUG282-2.6E, 05/09/2024

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Revision History

Date	Version	Description
01/30/2018	1.2E	Initial version published.
08/16/2018	1.3E	● The value range of V_{CC}/V_{CCX} updated; ● Interface screenshots updated.
10/26/2018	1.4E	GW1NZ-1 and GW1NSR-2C supported.
11/15/2018	1.5E	● GW1NSR-2 supported; ● GW1N-6ES, GW1N-9ES and GW1NR-9ES removed.
02/25/2019	1.6E	● The voltage configuration updated; ● VCD File configuration supported; ● Specified IO toggle rate configuration removed.
05/17/2019	1.7E	GW1N-1S supported;
03/09/2020	1.8E	GW1NRF-4B, GW1NS-4, GW1NS-4C, GW1NSE-2C, GW1NSER-4C GW1NSR-4, GW1NSR-4C, GW2A-18C, GW2A-55C and GW2AR-18C supported.
05/09/2020	1.9E	● GW1N-9C, GW1NR-9C and GW2ANR-18C supported; ● GW1N-2, GW1N-2B and GW1N-6 removed.
09/17/2020	2.0E	Power analysis of automotive grade devices supported.
06/16/2021	2.1E	● Some figures updated; ● The descriptions of operating conditions updated.
08/05/2021	2.2E	● Changed 1.9.8Beta to 1.9.8 version. ● Chapter 5 Gowin Power Estimator" added.
11/02/2021	2.3E	Interface screenshots and corresponding descriptions updated.
12/20/2022	2.4E	Interface screenshots and corresponding descriptions updated.
11/30/2023	2.4.1E	Interface screenshots updated.
02/02/2024	2.5E	● Figure 4-1 GPA Report updated. ● The descriptions of Section 4.1 Power Message updated.
05/09/2024	2.6E	● Junction temperature configuration supported in the configuration interface. ● Range for ambient temperature and board temperature updated. ● Power report structure updated.

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1 About This Guide

1.1 Purpose

This manual describes how to use the Gowin Power Analyzer. It provides the descriptions of tool and analysis of the power consumption report. It helps you estimate and analyze power consumption more easily. As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- SUG100, Gowin Software User Guide
- SUG918, Gowin Software Quick Start Guide

1.3 Terminology and Abbreviations

Table 1-1 shows the abbreviations and terminology that are used in this manual.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
FPGA	Field Programmable Gate Array
GPA	Power Analysis
GPE	Gowin Power Estimator
θ_{JA}	Junction to Ambient
θ_{JB}	Junction to Board
θ_{SA}	Sink to Ambient

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Introduction

The GPA tool is designed in-house by Gowin. It is used to analyze FPGA power consumption to help you estimate system power and improve the performance and reliability of the design.

Users set the part number, operating environment, and signal toggle rate, etc. according to their requirements. The parameters have an impact on chip power consumption. The GPA automatically estimates the power consumption and produces a power consumption analysis report according to the parameters.

Primary Function

- Calculate Quiescent Power Consumption
  Quiescent power consumption refers to the power consumption caused by leakage current in the device. It is determined by the design, package, process, voltage, and working environment of the chip.
- Calculate Dynamic Power Consumption
  Dynamic power consumption refers to the power consumption during operating, which is determined dynamic power by the user-designed logic circuit and the characteristics of the circuit.

Primary Feature

- Supports setting the various factors that affects quiescent power consumption
  - Supports setting junction temperature
  - Supports setting ambient temperature
  - Supports setting air flow
  - Supports setting heat sink performance and Board Thermal Model
  - Supports setting customized thermal impedance parameters
- Supports various ways to calculate signal toggle rate
  - User-specified IO and Net signal toggle rate
  - Toggle rate calculated from the waveform file generated by simulation
  - Supports specified default toggle rate

- Enables/disables clock, BSRAM, I/O, and DFF
- Power consumption analysis report supports various ways to analysis power consumption
  - Supports analyzing power consumption based on voltage type
  - Supports analyzing power consumption based on Block type
  - Supports analyzing power consumption based on hierarchy
  - Supports analyzing power consumption based on clock domain

3 GPA

The GPA helps you accurately estimate the power consumption by part number, operating environment, voltage, signal toggle rate and clock configuration. For a simple GPA example, see *SUG918, Gowin Software Quick Start Guide*.

3.1 Start GPA

Before starting GPA, you need to create or load the config file (.gpa).

3.1.1 Create/Load Config File

Create Config File

The steps are as follows.

1. In the "Design" view, right-click to select "New File...".
   The "New" dialog box pops up.
2. Create "GPA Config File", as shown in Figure 3-1.
3. Click "OK", and the "New GPA Config File" dialog box will open, as shown in Figure 3-2.
4. Enter Config File name and select create path, then click "OK". The GPA Config File appear in "Design > GPA Config Files".

Figure 3-1 Create Config File

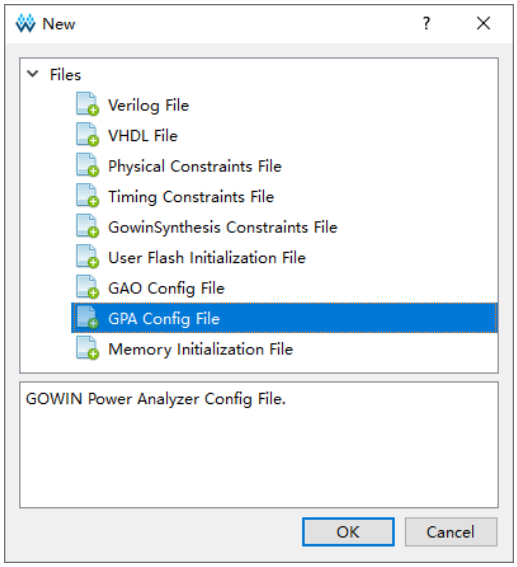
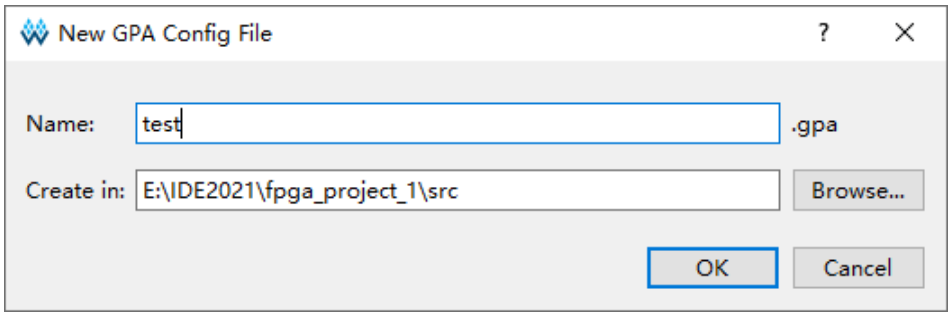


Figure 3-2 New GPA Config File Dialog Box

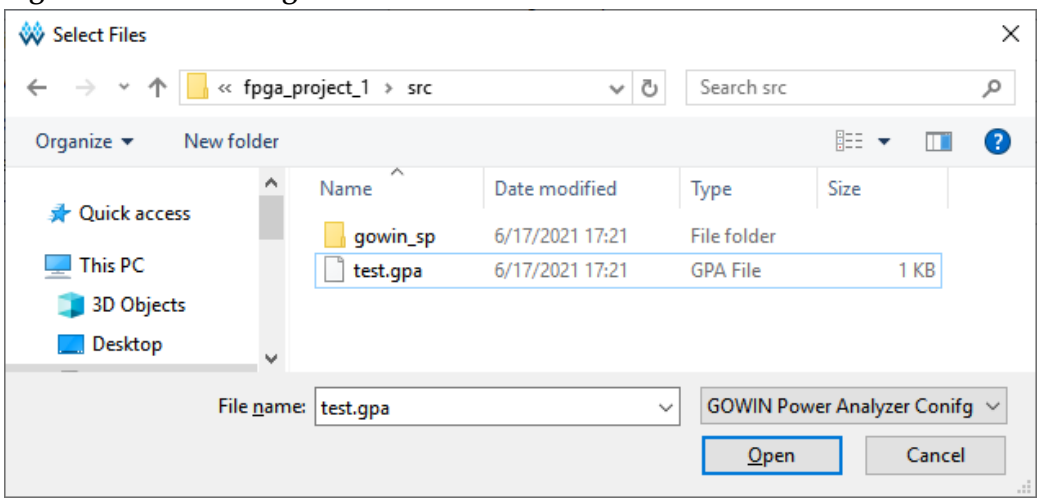


Add Config File

The steps are as follows:

1. In "Design", right-click to select "Add Files...". The "Select Files" window will open.
2. Select the existing Config File (.gpa), as shown in Figure 3-3, click "Open". See GPA Config File in "Design > gpa Config Files".

Figure 3-3 Load Config File

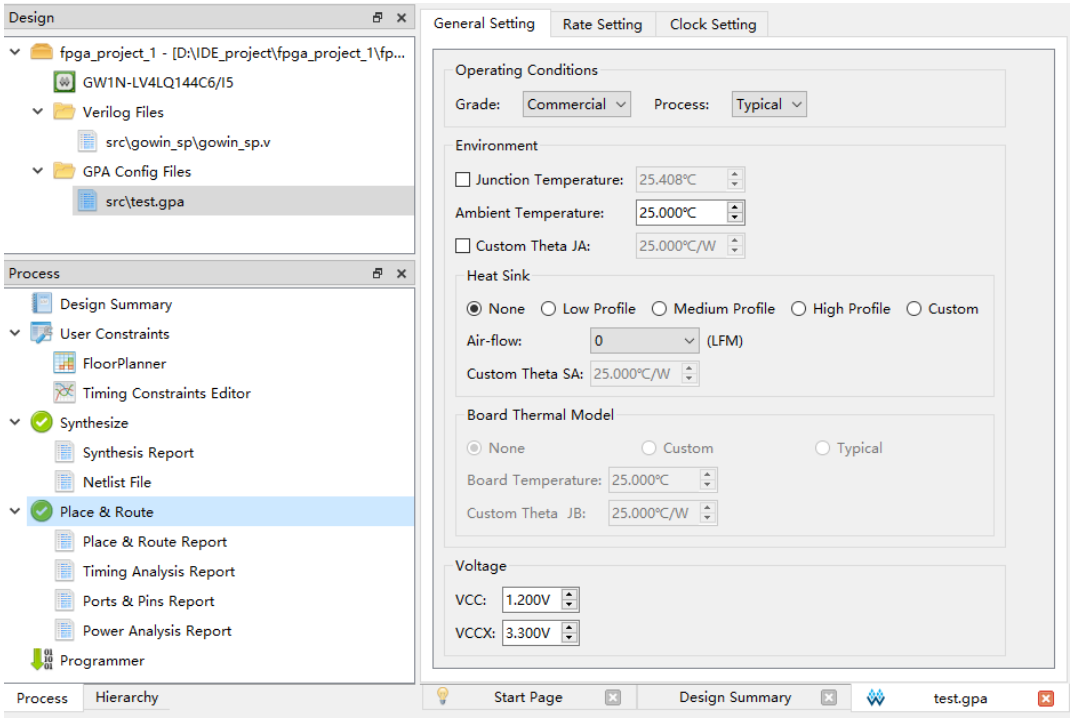


3.1.2 Open GPA View

After successful synthesis, double-click the Config File (.gpa) in "Design" window, and GPA view opens, as shown in Figure 3-4.

The GPA view includes "General Setting" (used for configuring operating conditions), "Rate Setting" (used for configuring signal toggle rate), and "Clock Setting" (used for configuring clock enable).

Figure 3-4 GPA View



3.2 GPA Configuration

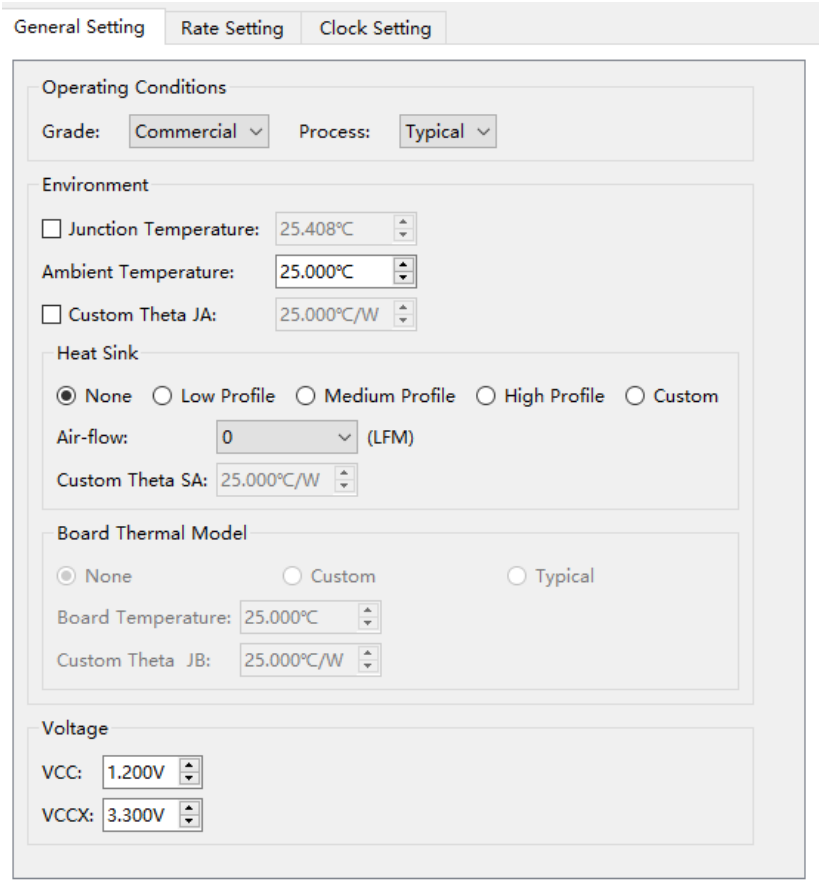
To ensure the accuracy of the power consumption analysis, it is necessary to set the chip operating conditions, toggle rate of the signal, and enable/disable clock, BSRAM, I/O, DFF, etc. according to the design.

3.2.1 Operating Conditions

The "General Setting" view displays the operating conditions, thermal impedance, and voltage.

As shown in Figure 3-5, the "General Setting" view displays "Operating Conditions" for setting the chip temperature grade and process, "Environment" for setting the chip operating conditions, and "Voltage" for setting the chip voltage.

Figure 3-5 General Setting View



Parameter

1. Operating Conditions

   - Grade: The grade includes Commercial, Industrial, and Automotive. And the grade setting affects the minimum and maximum operating temperature of the chip. The operating temperature of commercial devices is from 0 ℃ to 85 ℃; the operating temperature of industrial devices is from 40 ℃ to 100 ℃; and the operating temperature of automotive devices is from 40 ℃ to 125 ℃.
   - Process: The process of the chip includes Typical or Worst.

2. Environment

"Environment" is used to configure the junction temperature, ambient temperature, air flow, heat sink and Board Thermal Model, etc. Operating environment affects quiescent power consumption. Different operating environments will affect the FPGA chip temperature and quiescent power consumption. Air flow affects the thermal performance of the chip. The heat sink is used for the heat dissipation of the specified chip through the auxiliary device; The circuit Board Thermal Model is used for the heat dissipation of the specified chip through the board.

Junction temperature is determined by external temperature, chip power consumption, and thermal impedance. Please refer to *Appendix A Calculation Principle for Junction Temperature* for calculation principle of

junction temperature. Details of Environment configuration parameters are as follows.

- Junction Temperature: The unit is ℃; the temperature range is related to Grade. It is the operating temperature of the chip in different Grades, and the default is 25.408℃.
- Ambient Temperature: The unit is ℃.; and the range is from minus 60 ℃ ~ 160℃, and the default is 25.000 ℃.
- Custom Theta JA: You can specify the thermal impedance θ_{JA} between the chip and environment. The unit is ℃/W. The range is from 0.001℃/W ~ 100℃/W, and the default is 25.000℃/W.
- Heat Sink: Heat Sink includes 5 modes: None, Low Profile, Medium Profile, High Profile and Custom. "None" indicates heat sink is unused, and only thermal impedance θ_{JA} influences junction temperature; Custom indicates that the user specifies the thermal impedance θ_{SA} from the heat sink to the environment; Low Profile, Medium Profile and High Profile modes represent θ_{JA} is automatically calculated by GPA.
- Air Flow: The unit is LFM or m/s. The unit displayed in the user interface is LFM. There are four selection modes, including 0LFM, 100LFM (0.5 m/s), 200 LFM (1.0 m/s), 400 LFM (2.0 m/s); the larger the Air Flow is, the smaller the thermal impedance from the chip to the ambient is, and the smaller the junction temperature is.
- Custom Theta JA: thermal impedance θ_{SA} between Heat Sink and environment. The unit is ℃/W. The range is from 0.001℃/W ~ 100℃/W, and the default is 25.000℃/W.
- Board Thermal Model: Heat dissipation model of development board. Thermal impedance model of the development board is the path that dissipating heat from the development board to outside, which includes three modes: None, Custom, and Typical. None means board thermal is not to be considered; Custom indicates the user specifies thermal impedance θ_{JB} from device to development board; Typical indicates θ_{JB} is automatically determined by chip package.
- Board Temperature: Temperature of the circuit board
- CustomTheta JB: Thermal impedance θ_{JB} from junction to board. The user can specify only if selecting Custom from Board Thermal Model.

3. Voltage
   - VCC: core voltage. The unit is V, and for the voltage range of each series device, you can see the pinout manuals at our website.
   - VCCX: auxiliary voltage. The unit is V, and for the voltage range of each series device, you can see the pinout manuals at our website.

3.2.2 Signal Toggle Rate Configuration

Rate Setting is used for configuring signal toggle rate. You can set toggle rate of IO or Net or use default toggle rate.

As shown in Figure 3-6, Rate Setting view displays Net Rate, VCD File and Default Rate Setting.

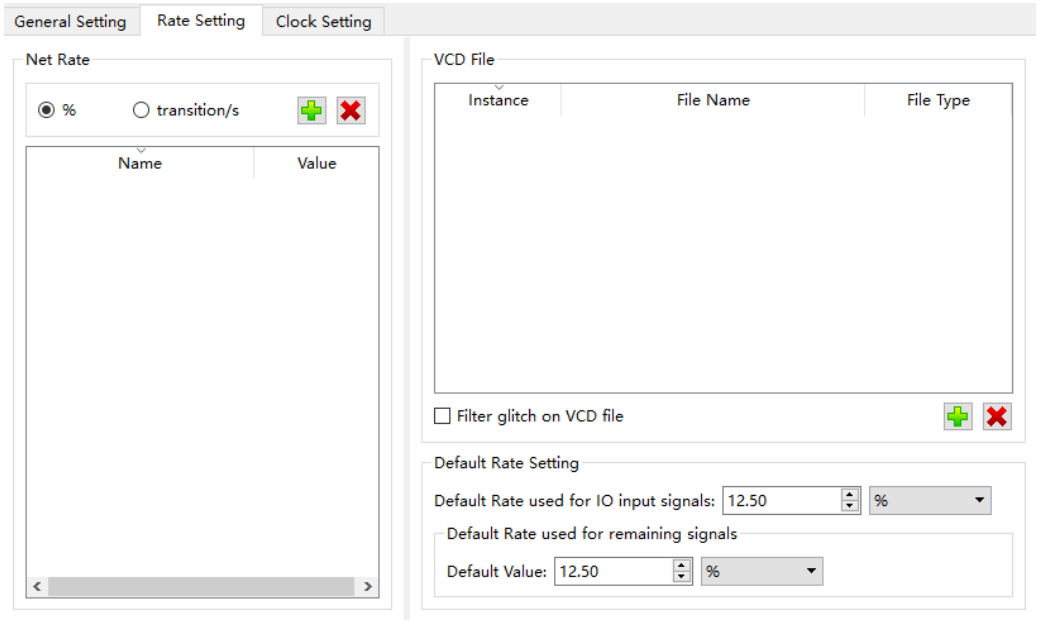
The descriptions of each option are as follows.

- Net Rate is used to configure specified net toggle rate.
- VCD File is used to load waveform files generated by simulation.
- Default Rate Setting is used to configure general default toggle rate for IO and Net.

Note!

Net toggle rate specified by users is of the highest priority, Net toggle rate specified by the waveform files generated by simulation is of the second-highest priority, and the default IO and Net toggle rate is of the lowset priority.

Figure 3-6 Rate Setting View

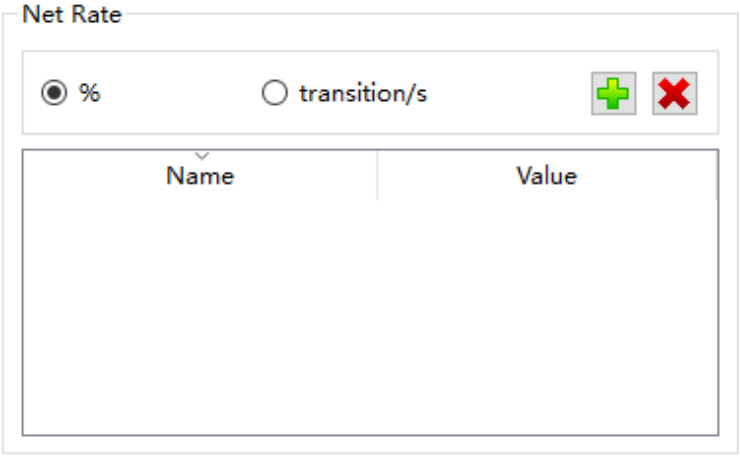


Specified Net Toggle Rate

Net Rate is used to set net signal toggle rate specified by users, as shown in Figure 3-7. Net toggle rate includes TOGGLE RATE mode and SIGNAL RATE mode.

Click "%" to select TOGGLE RATE mode; Or click "transition/s" to select SIGNAL RATE mode.

Figure 3-7 Net Rate View



Note!

- TOGGLE RATE mode: The ratio of signal toggle rate to clock rate, and the unit is %;
- SIGNAL RATE mode: The signal toggle rate, and the unit is transition/s.

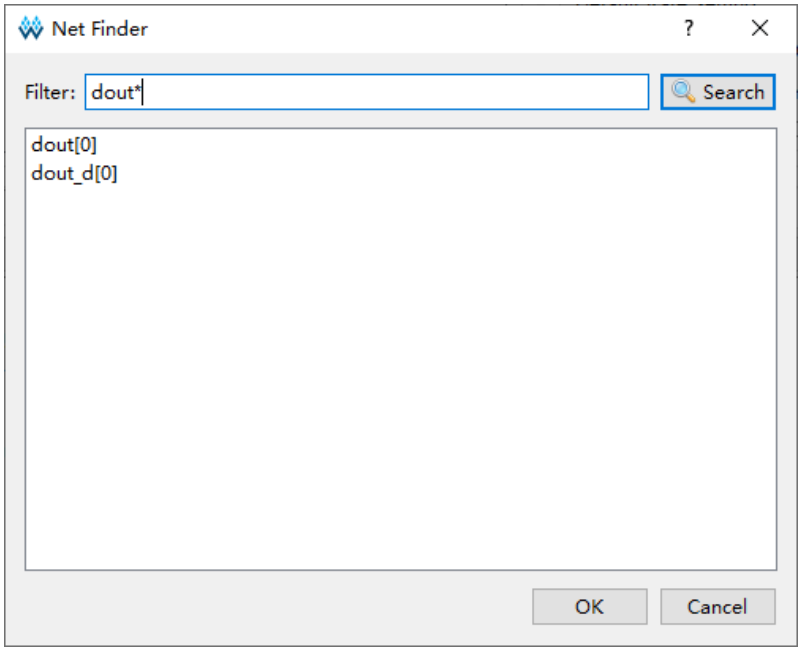
Select Net signal. The steps are as follows.

1. Click "  " , and "Net Finder" dialog box pops up, as shown in Figure 3-8.
2. Enter net name in Filter text box, click "Search".
3. Select the specified net in list.
4. Click "OK" to finish selecting net signal.

Note!

You can also right-click to select "Add" in pop-up menu.

Figure 3-8 Net Finder Dialog Box

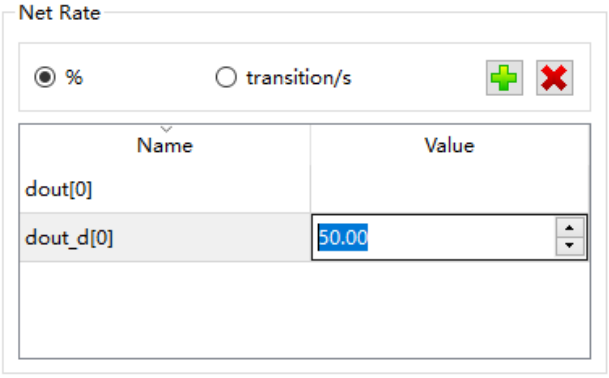


Note!

- "Filter" supports wildcard screening.
- The list supports options of left-click, Shift + left, and Ctrl + left.

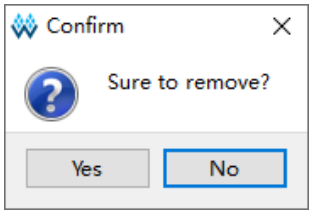
5. See Net signals in Net Rate table, and double-click the corresponding value column and enter signal toggle rate, as shown in Figure 3-9.

Figure 3-9 Set Net Toggle Rate



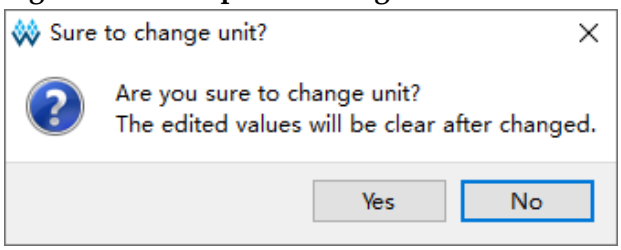
6. Select the row to be deleted in the editing area, and click " " or right-click to select "Remove" in the pop-up menu. The "Confirm" dialog box will pop up, click "Yes" to delete the net toggle rate, as shown in Figure 3-10.

Figure 3-10 Delete Toggle Rate



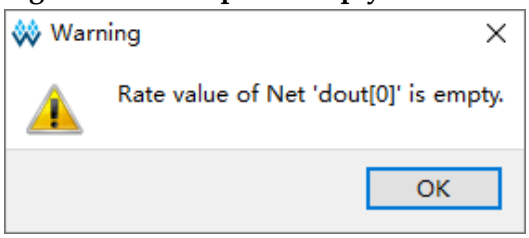
7. For the net toggle rate that has been set, the shift between TOGGLE RATE and SIGNAL RATE is not supported. If one of settings is selected, "Sure to change the unit" will pop up, as shown in Figure 3-11.

Figure 3-11 Prompt for Setting Rate



8. For the net added in the editing table, value should be set, or when clicking "save", a "Warning" dialog box will pop up, as shown in Figure 3-12.

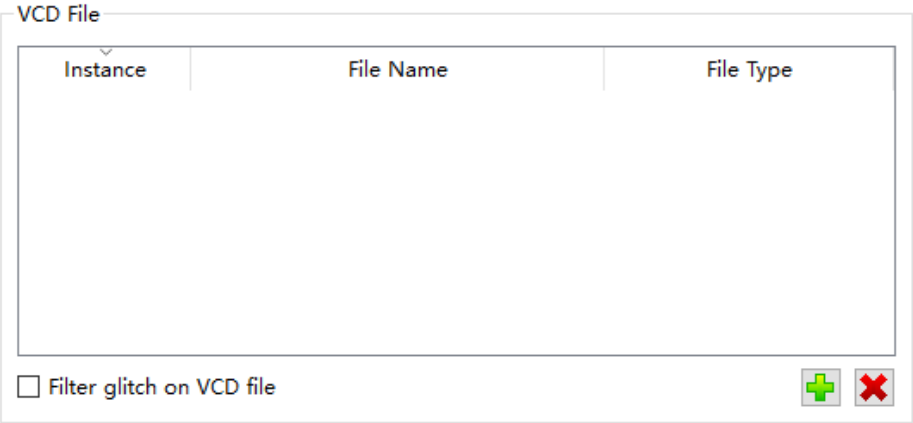
Figure 3-12 Prompt for Empty Value



Load Waveform File Generated by Simulation

VCD File is used to load waveform files generated by simulation, as shown in Figure 3-13. Waveform files are the basis for calculating IO and NET toggle rate. Two types of waveform files generated by VCS or modelsim simulation tools are supported: VCD (Value Change Dump) and SAIF (Switching Activity Interchange) files.

Figure 3-13 VCD File View



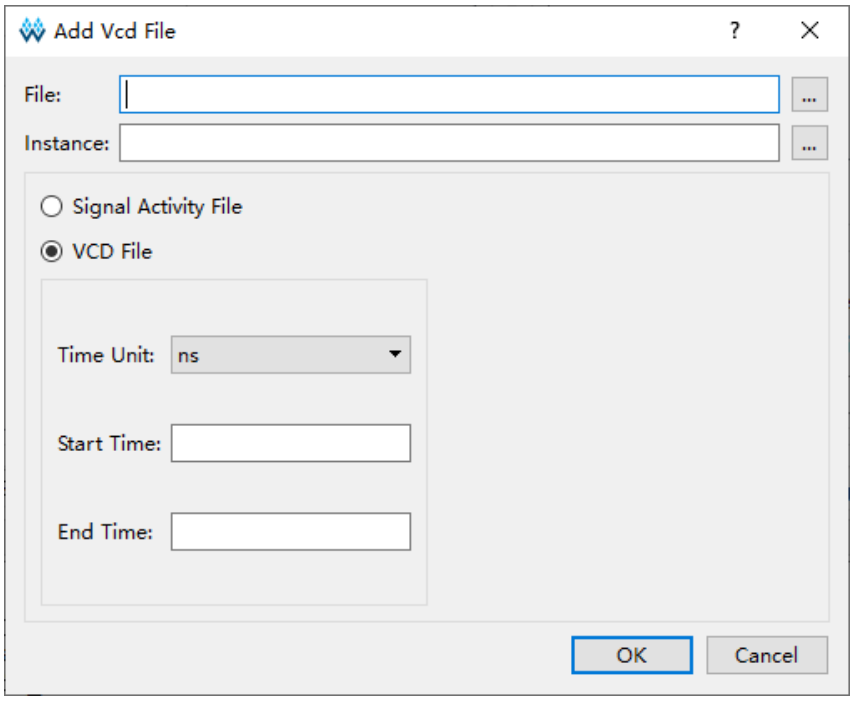
Note!

You need to obtain a license from the third party to use VCS and modelsim tools.

The steps of loading the waveform files are as follows.

1. Click "  ", and "Add Vcd File" dialog box pops up, as shown in Figure 3-14.

Figure 3-14 Add Vcd File Dialog Box



Note!

You can also right-click to select "Add Input File" in the editing table.

2. Click the " ... " button on the right of "File", and the "Select VCD File" dialog box pops up, as shown in Figure 3-15; Select the *.vcd or *.saif file to be loaded and click "OK" to finish.

3. Click the " ... " button on the right of "Instance", and the "Select Instance" dialog box pops up, as shown in Figure 3-16. Select the Instance to be loaded, and click the "OK".

4. If "File" loads *.saif file, select "Signal Activity File"; If "File" loads *.vcd file, select "VCD File".

5. When "VCD File" is selected, the time configuration is highlighted, and part of the time in the VCD File can be set as the basis for power analysis. Click the drop-down box at Time Unit and select s, ms, us, ns or ps in the drop-down list, as shown in Figure 3-17. Enter the start Time in the "Start Time" text box and the end time in the "End Time" text box.

6. Click the "OK" to complete the loading the waveform file. The configured Instance name, waveform File name, and File type are displayed in the VCD File view.

7. As shown in Figure 3-13, click the check box before "Filter glitch on VCD file" to filter out the glitches in the loaded waveform file.

Figure 3-15 Select VCD File Dialog Box

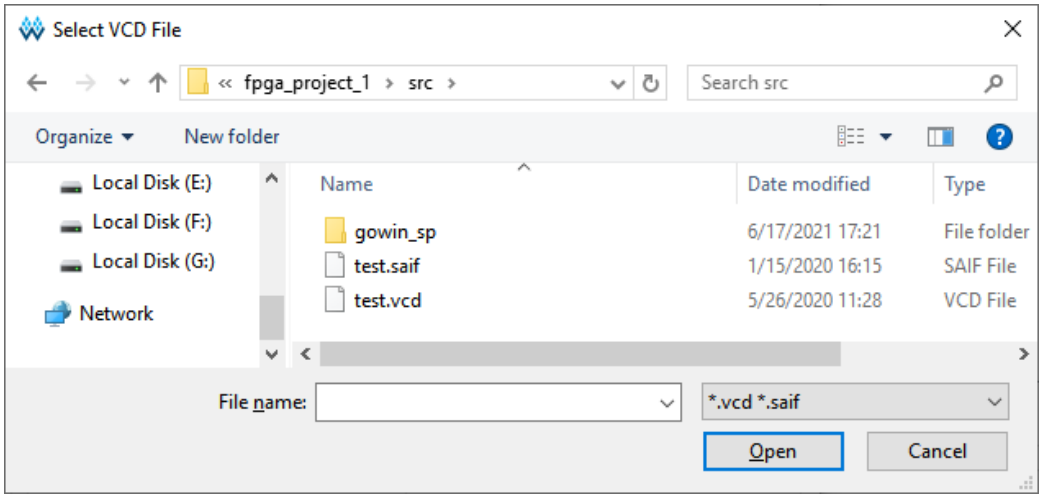


Figure 3-16 Select Instance Dialog Box

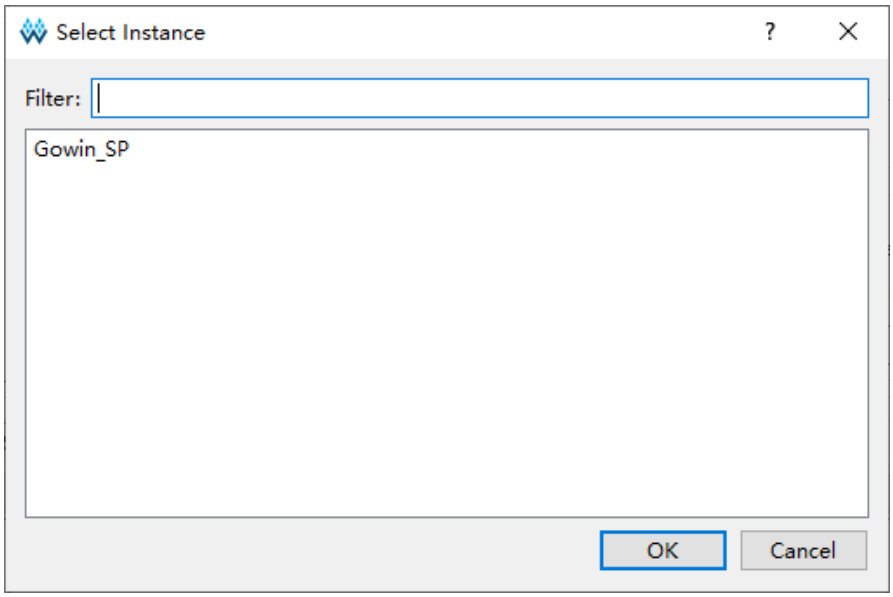
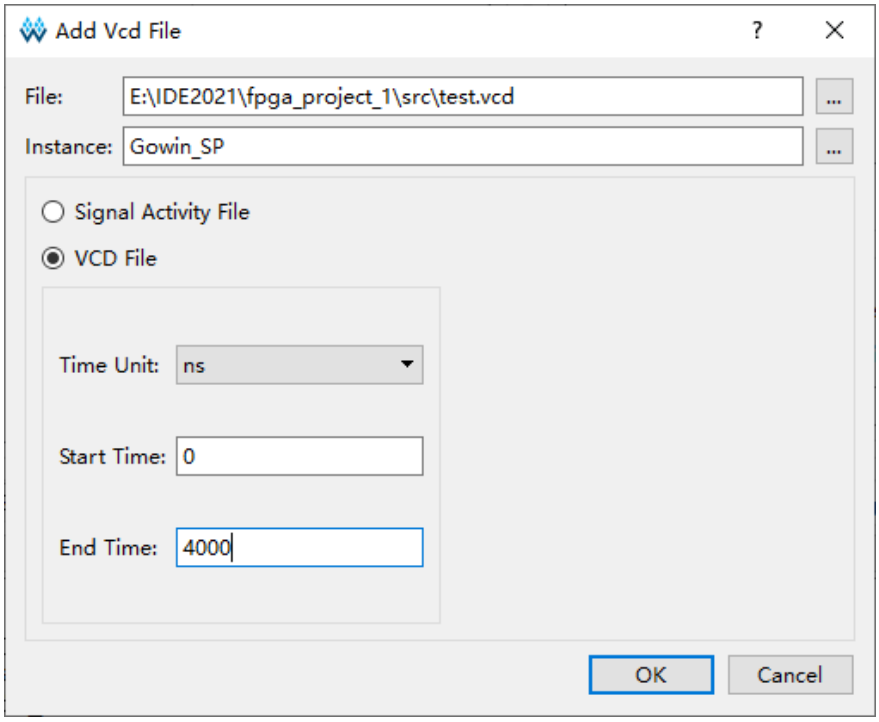


Figure 3-17 Set the Start and End Time of the Waveform File

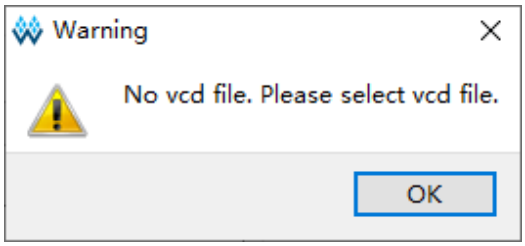


Note!

- "Signal Activity File" and "VCD File" are used for the specified type of loaded file, which should be consistent with the type of loaded waveform.
- After clicking the "Signal Activity File" button, the time unit and the start and end time are greyed.

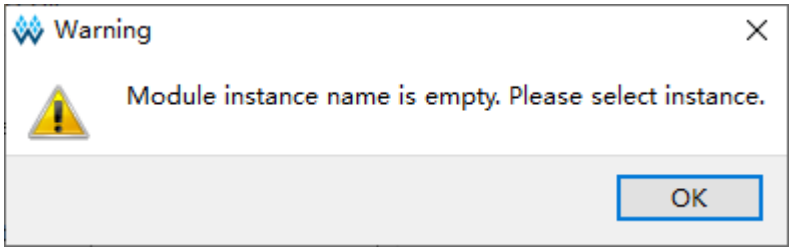
In the "Add Vcd File" dialog box, if the "File" configuration is empty, click the "OK" to pop up a "Warning" prompt, as shown in Figure 3-18.

Figure 3-18 Prompt



In the "Add Vcd File" dialog box, if the "Instance" configuration is empty, click the "OK" to pop up a Warning prompt, as shown in Figure 3-19.

Figure 3-19 Prompt



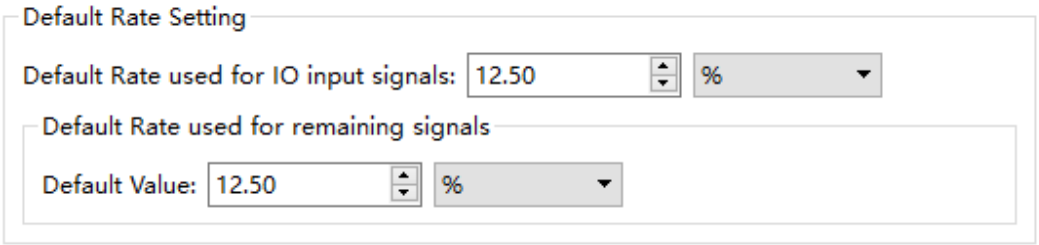
Global Default Toggle Rate Configuration

Default Rate Setting is used to set global default toggle rate of IO and Net signals, as shown in Figure 3-20.

Enter toggle rate in Default Rate used for IO input signals text box. Click the drop-down box on the right side and select the toggle rate unit "%" (TOGGLE RATE mode) or "transition/s" (SIGNAL RATE mode) in drop-down list.

Enter IO (except IO input signal) and unspecified net toggle rate in Default Rate used for remaining signals > Default Value text box, click the drop-down list on the right side and select toggle rate unit "%" (TOGGLE RATE mode) or "transition/s" (SIGNAL RATE mode).

Figure 3-20 Default Rate Setting View



Note!

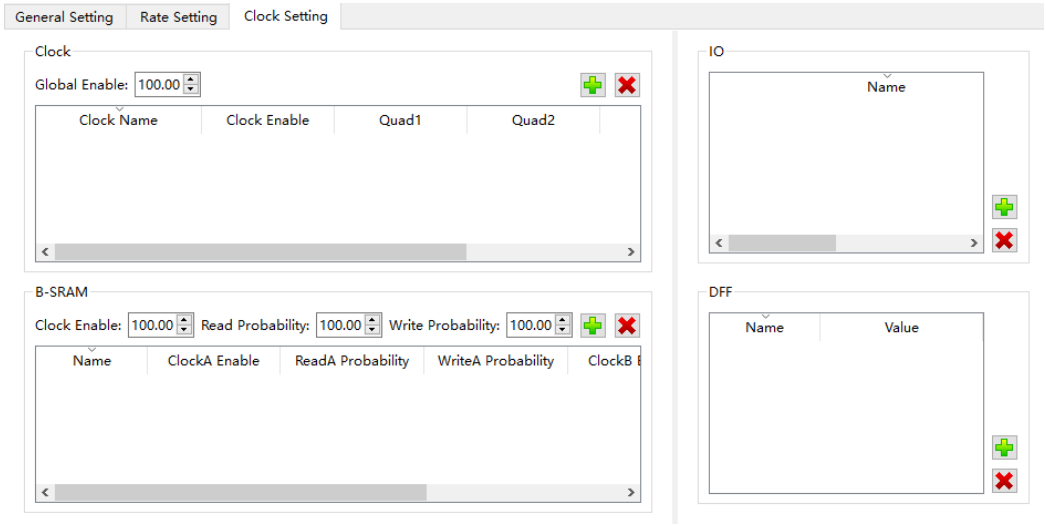
- TOGGLE RATE mode: The ratio of signal toggle rate to clock rate, and the unit is %.
- SIGNAL RATE mode: Toggle rate of signal, unit: transition/s.
- In other cases, toggle rate of IO and net is determined according to the priority in each view area.

3.2.3 Clock Enable Configuration

"Clock Setting" is used to configure clock and enable of BSRAM, IO and DFF.

As shown in Figure 3-21, "Clock Setting" includes Clock, BSRAM, IO and DFF.

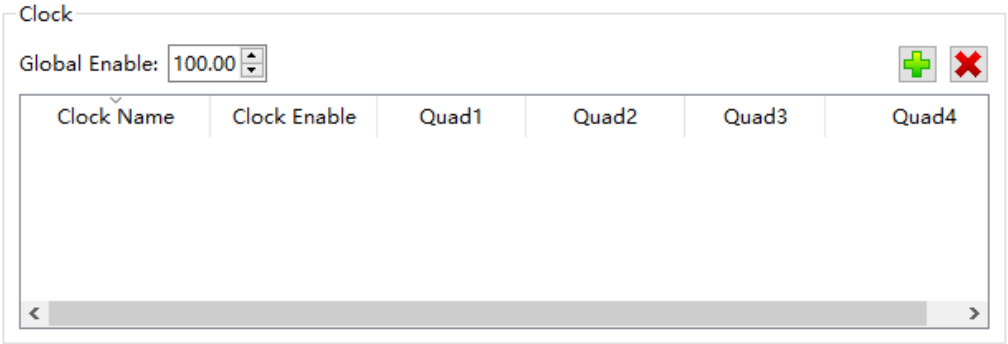
Figure 3-21 Clock Setting View



Clock Enable Configuration

"Clock" is used to configure clock enable, as shown in Figure 3-22. Clock is specified from SDC timing constraints file. You can enable all clocks or the specified clock, or the clock in quadrant. The priority of settings is quadrant, specified clock, and clock global enable.

Figure 3-22 Clock View

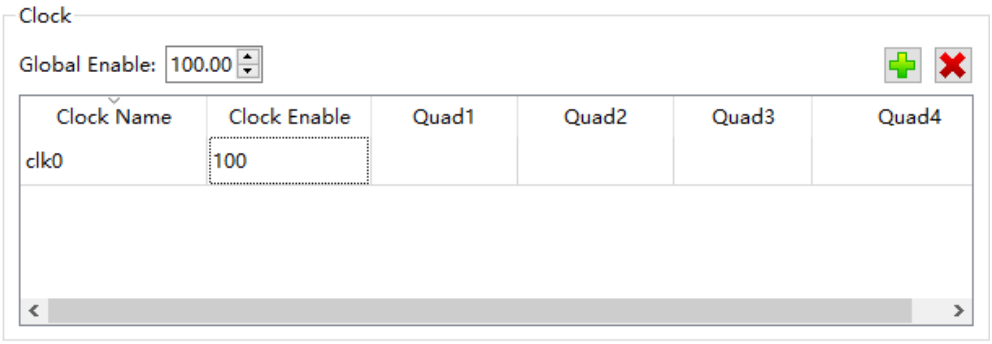


The steps are as follows.

1. Enter rate of global enable time percentage for all clocks in "Global Enable".
2. Click "  " to add a editable row, as shown in Figure 3-23.
3. Specify a row, double-click cell corresponding to "Clock Name" and enter clock Name.

4. Double-click the cell corresponding to "Clock Enable", enter rate of clock enable time.
5. Double click cells corresponding to "Quad1", "Quad2", "Quad3" and "Quad4", and set enable time rate of clock in 4 quadrants.

Figure 3-23 Clock Enable Configuration

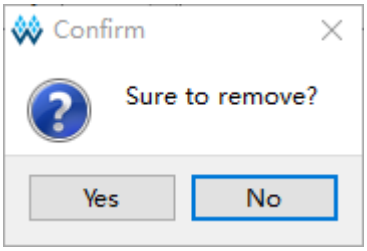


Note!

- You can also add an editable row by right clicking in the blank and selecting "Add" in menu.
- Clock Name should be consistent with the Name in design file and SDC timing constraints file.

6. Select the row needed to be removed in editing area, click "  ", and "Confirm" dialog will pop up, as shown in Figure 3-24. Click "Yes" to remove.

Figure 3-24 Remove Clock Enable



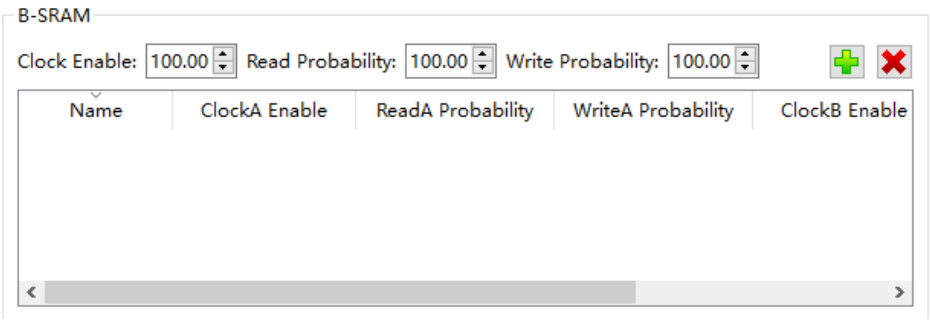
Note!

Right click to select ″Remove″ in menu, and "Confirm" pops up.

BSRAM Enable Configuration

BSRAM is used to set enable of BSRAM clock and Read-Write, as shown in Figure 3-25. You can set global enable for all BSRAM clocks and read-write, or for a specified BSRAM. A single BSRAM enable takes priority over all BSRAM global enable setting.

Figure 3-25 BSRAM View



As shown in Figure 3-26, the relevant settings are as follows.

1. Enter rate of BSRAM work clock enable time in "Clock Enable".
2. Enter rate of BSRAM read data time in "Read Probability".
3. Enter rate of BSRAM write data time in "Write Probability".

Figure 3-26 Clock Enable for All BSRAMs

Note!

- Clock Enable, Read Probability, and Write Probability parameters are valid for all BSRAMs in design file.
- If BSRAM has no read function, ignore Read Probability parameter; if no write function exists, ignore Write Probability parameter.

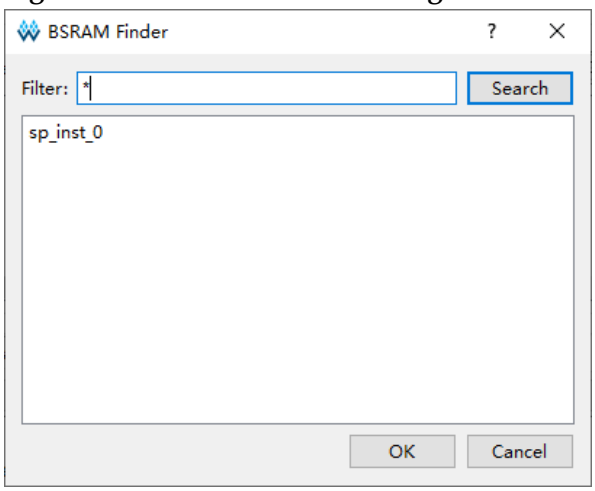
Set enable for the specified BSRAM after adding.

Add BSRAM

Click "  ", and "BSRAM Finder" dialog will pop up, as shown in Figure 3-27.

1. Enter the instance name of BSRAM in Filter, and click "Search".
2. Select the specified BSRAM in list, and click "OK" to finish adding BSRAM.

Figure 3-27 BSRAM Finder Dialog Box



Note!

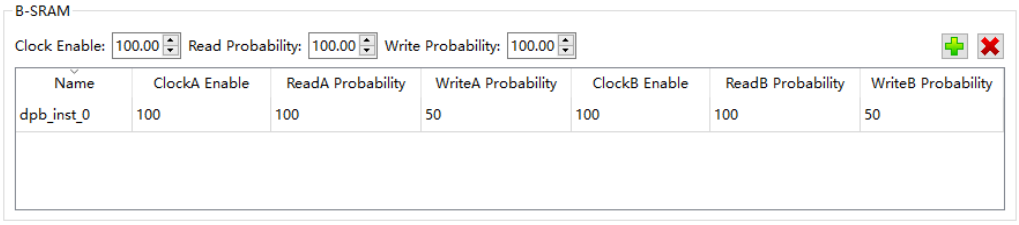
- You can also right-click in the blank of table to select "Add", and "BSRAM Finder" will pop up.
- "Filter" supports wildcard screening.
- The list supports options of left-click, Shift + left, and Ctrl + left.

BSRAM Enable

See the instance name of added BSRAM in BSRAM table, as shown in Figure 3-28, and the steps are as follows.

1. Select a row, double-click cell corresponding to "ClockA Enable", enter the time percentage of BSRAM ClockA enable.
2. Double-click the cell corresponding to "ReadA Probability", enter rate of BSRAM ClockA read data time.
3. Double-click the cell corresponding to "WriteA Probability", enter rate of BSRAM ClockA write data time.
4. Double-click the cell corresponding to "ClockB Enable", enter rate of BSRAM ClockB enable time.
5. Double-click the cell corresponding to "ReadB Probability", enter rate of BSRAM ClockB read data time.
6. Double-click the cell corresponding to "WriteB Probability", enter rate of BSRAM ClockB write data time.

Figure 3-28 Specified BSRAM Clock Enable



Note!

- If the specified BSRAM has no read function of port A, ReadA Probability can not be edited. If there is no write function of port B, WriteA Probability can not be edited.
- If specified BSRAM has no port B, the ClockB Enable, ReadB Probability, and WriteB Probability can not be edited.

Remove BSRAM Enable

1. Select the row needed to be removed in editing table, click "  ", and the "Confirm" dialog box will pop up, as shown in Figure 3-24.
2. Click "Yes" to remove BSRAM Enable Setting.

Note!

Right click to select ″Remove″ in menu, and "Confirm" pops up.

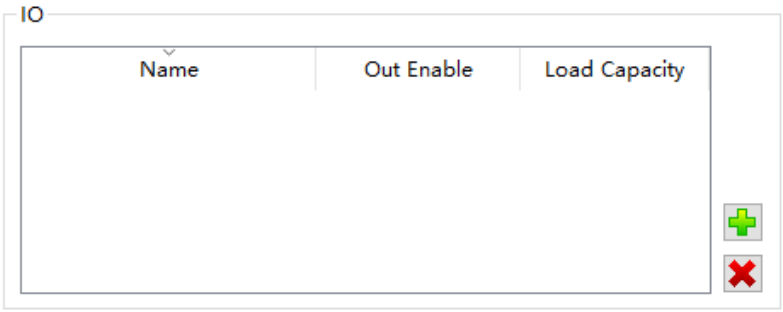
IO Enable

"IO" is used to configure OEN enable and output load of IO, as shown in Figure 3-29.

You can set OEN enable rate for bidirectional Buffer in design file to calculate I/O power consumption. If not specified, take the fault value "50%"; You can set the load capacitance value of TLVDS Buffer (pF) in the design file for calculating output power consumption, if not specified, take

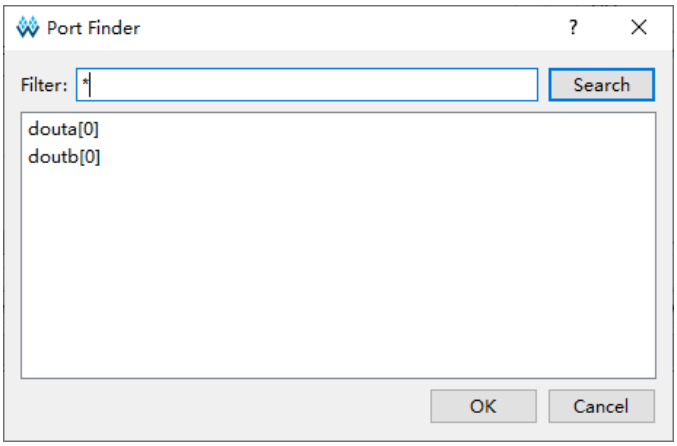
default value "5pF".

Figure 3-29 IO View



1. Click "  ", and "Port Finder" dialog box will pop up, as shown in Figure 3-30.
   a) Enter Port name in Filter and click "Search".
   b) Select the specified port in list, click "OK" to finish adding Port.

Figure 3-30 Port Finder Dialog Box

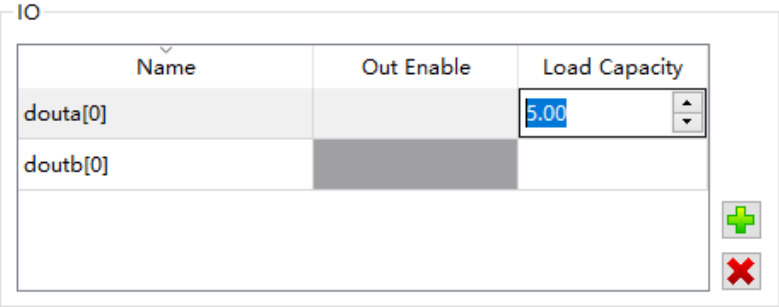


Note!

- You can also right-click in the blank of table to select "Add", and "Port Finder" will pop up.
- "Filter" supports wildcard screening.
- The list supports options of left-click, Shift + left, and Ctrl + left.

2. Specified IO Enable Configuration
   a) See the added Port name in the table of IO, as shown in Figure 3-31.
   b) Specify a row, double-click cell corresponding to "Out Enable", and enter rate of OEN enable time.
   c) Double-click cell corresponding to "Load Capacity", and enter load capacitance value.

Figure 3-31 Specified I/O Enable Configuration



Note!

If there is no OEN function for the specified Buffer, "Out Enable" is not available.

3. Remove IO Enable Setting

   a) Select the row needed to be removed in editing table, click " ". "Confirm" dialog will pop up, as shown in Figure 3-24.

   b) Click "Yes" to remove I/O enable setting.

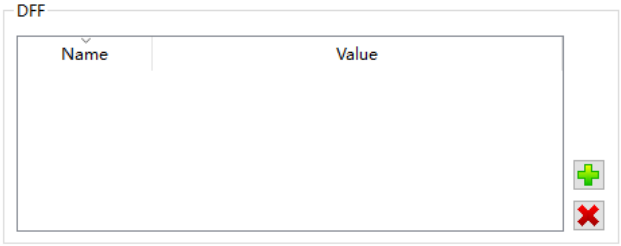
   Note!

   You can also right-click to select "Remove", and the "Confirm" dialog box will pop up.

DFF Enable Configuration

"DFF" is used to configure DFF clock enable, as shown in Figure 3-32.

Figure 3-32 DFF View



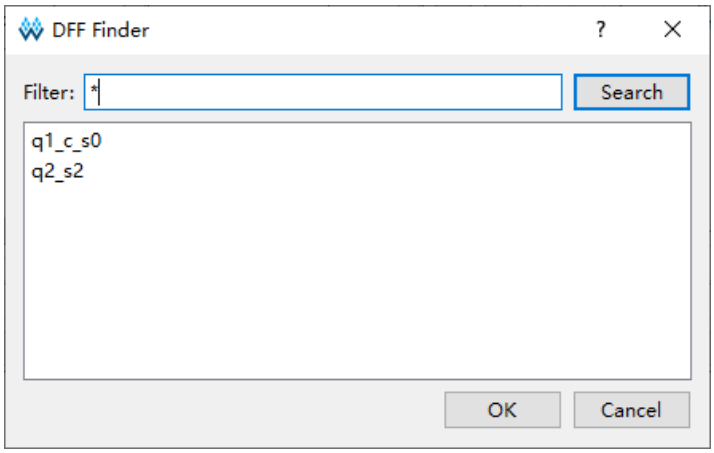
1. Add DFF

   a) Click " " and "DFF Finder" dialog will pop up, as shown in Figure 3-33.

   b) Enter instance name of DFF in Filter and click "Search".

   c) Select the specified DFF in list and click "OK" to finish adding DFF.

Figure 3-33 DFF Finder Dialog Box



Note!

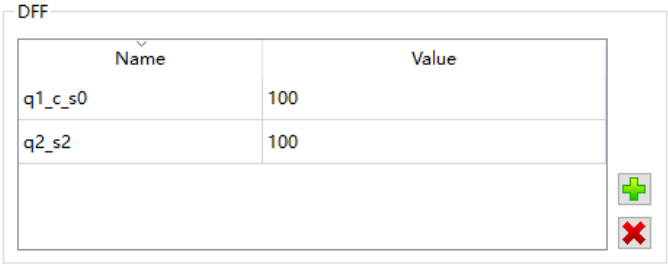
- You can also right-click in the blank of table to select "Add". "DFF Finder" dialog box will pop-up.
- "Filter" supports wildcard screening.
- The list supports options of left-click, Shift + left, and Ctrl + left.

2. Specified DFF Enable Configuration

   a) See instance name of the added DFF in DFF table, as shown in Figure 3-34.

   b) Specify a row, double-click cell corresponding to "Value", and enter rate of DFF clock enable time.

Figure 3-34 Specified DFF Enable Configuration



3. Remove DFF clock enable setting

   a) Select the row needed to be removed in editing table, click " ", and the "Confirm" dialog box will pop up, as shown in Figure 3-24.

   b) Click "Yes" to remove DFF clock enable.

   Note!

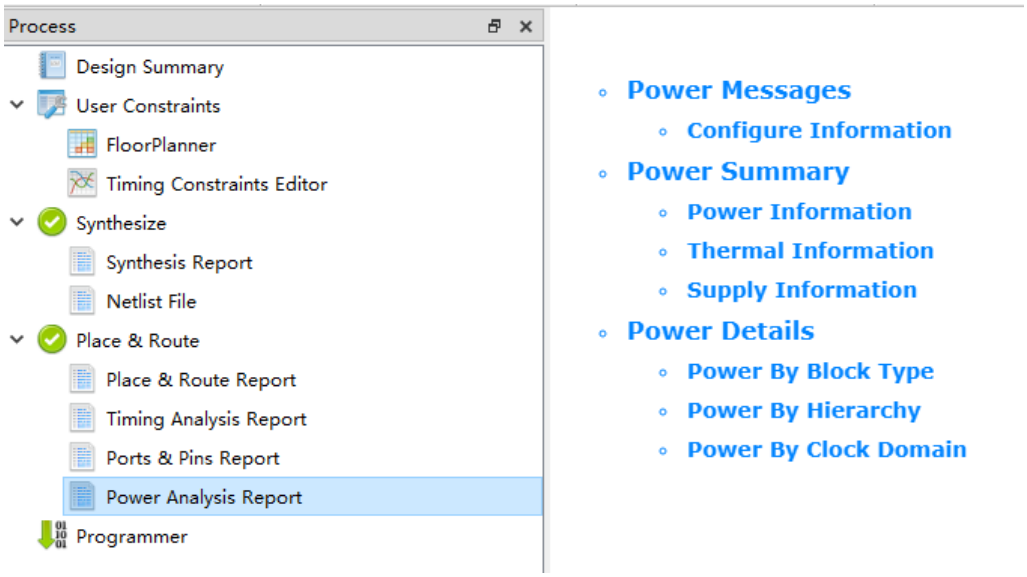
   Right click to select "Remove" in menu, and "Confirm" pops up.

3.3 GPA Power Analysis Report

After configuring GPA, click " " to save. Double-click "Place&Route" in Process to perform the place & route to generate GPA report.

Double-click "Place&Route > Power Analysis Report" in Process, and GPA Report pops up, as shown in Figure 3-35.

Figure 3-35 Open GPA Report



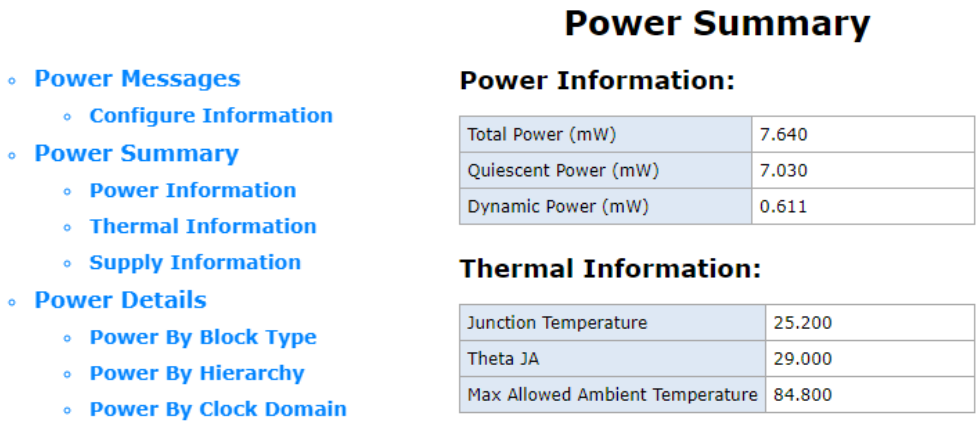
4 Power Analysis Report

GPA report shows the estimated result of power consumption calculated by the user-defined parameters, which helps you more easily to analyze and design power consumption.

GPA report includes two parts: Navigation tree and content, as shown in Figure 4-1. The navigation tree is used to hierarchically display report titles using hyperlinks with content, which helps you to find the required content more easily.

Power Analysis Report content is divided into three parts: Power Message, Power Summary, and Power Details. Power Messages mainly introduces the device information, some GPA configuration information, and design files; Power Summary mainly introduces parameters set by the user and power consumption. Power Detail mainly introduces the power consumption of Block type, design hierarchy, and clock domain.

Figure 4-1 GPA Report



4.1 Power Message

Power Message includes "Report Title", "Design File", "Physical Constraints File", "Timing Constraints File", "Tool Version", "Part Number", "Device"," Device Version" (if the device has no version history, the line is not displayed), "Created Time", and "Legal Announcement".

4.1.1 Configure Information

Configure Information is used to report some configuration information of the GPA configuration, as shown in Figure 4-2.

Figure 4-2 Configure Information

Configure Information:

Grade	Commercial	①
Process	Typical	②
Ambient Temperature	25.000	③
Use Custom Theta JA	false	④
Heat Sink	Medium Profile	⑤
Air Flow	LFM_0	⑥
Use Custom Theta SA	false	⑦
Board Thermal Model	Custom	⑧
Board Temperature	25.000	⑨
Use Custom Theta JB	true	⑩
Related Vcd File		⑪
Related Saif File		⑫
Filter Glitches	false	⑬
Default IO Toggle Rate	0.125	⑭
Default Remain Toggle Rate	0.125	⑮

① Temperature Grade
② Process
③ Ambient Temperature
④ Whether the user customizes θ_{JA}
⑤ Heat Sink
⑥ Air Flow
⑦ Whether the user customizes θ_{SA}
⑧ Board Thermal Model
⑨ Board Temperature
⑩ Whether the user customizes θ_{JB}
⑪ The path of the vcd file loaded by the user
⑫ The path of the saif file loaded by the user
⑬ Filter Glitches
⑭ IO Toggle Rate
⑮ Remain Toggle Rtate

4.2 Power Summary

Power Summary includes Power Information, Thermal Information, and Supply Information.

4.2.1 Power Information

Power Information is used to report total power consumption, total quiescent power consumption, and total dynamic power consumption, as shown in Figure 4-3.

Figure 4-3 Power Information

Power Information:

Total Power (mW)	1.925
Quiescent Power (mW)	1.354
Dynamic Power (mW)	0.570

4.2.2 Thermal Information

Thermal Information is used to report junction temperature, Theta θ_{JA}, θ_{JB}, and allowed max. ambient temperature, as shown in Figure 4-4.

Figure 4-4 Thermal Information

Thermal Information:

Junction Temperature	25.019	①
Theta JA	5.550	②
Theta JB	3.600	③
Max Allowed Ambient Temperature	84.981	④

① Junction Temperature ② Theta JA θ_{JA},

③ Theta JB θ_{JB} ④ Max Allowed Ambient Temperature

Note!

- Junction Temperature: Operating temperature of die.
- When the junction temperature is greater than the maximum operating temperature of the chip, the junction temperature is marked red.

4.2.3 Supply Information

Supply Information is used for reporting the core voltage, auxiliary voltage, and IO Bank voltage, and also reporting dynamic current, quiescent current, and power consumption, as shown in Figure 4-5.

Figure 4-5 Supply Information

Supply Information:

Voltage Source	Voltage	Dynamic Current(mA)	Quiescent Current(mA)	Power(mW)
VCC	1.200	0.208	2.461	3.202
VCCX	2.500	0.085	0.682	1.918
VCCIO12	1.200	0.070	0.016	0.103
VCCIO18	1.800	0.015	0.013	0.050

4.3 Power Details

Power Details include Power by Block Type, Power by Hierarchy and Power by Clock Domain.

4.3.1 Power by Block Type

Power By Block Type reports total power consumption of Blocks, static power, and average toggle rate included in file according to Block, as shown in Figure 4-6. Block includes Logic, IO, BSRAM, DSP, PLL, DQS, and DLLDLY, etc.

Figure 4-6 Power by Block Type

Power Details

Power By Block Type:

Block Type	Total Power(mW)	Static Power(mW)	Average Toggle Rate(millions of transitions/sec)
IO	1.624	0.296	23.438
BSRAM	2.033	NA	NA

Note!

NA indicates that the parameter is not considered.

4.3.2 Power by Hierarchy

Power By Hierarchy is used for reporting total power consumption, dynamic power consumption from top to bottom module in design file, as shown in Figure 4-7.

Figure 4-7 Power by Hierarchy

Power By Hierarchy:

Hierarchy Entity	Total Power(mW)	Block Dynamic Power(mW)
top	0.015	0.015(0.015)
top/sub_inst1/	0.008	0.008(0.000)
top/sub_inst2/	0.008	0.008(0.000)

4.3.3 Power by Clock Domain

Power By Clock Domain is used for reporting the name, frequency, and dynamic power consumption of clock based on Clock Domain, as shown in Figure 4-8.

Figure 4-8 Power by Clock Domain

Power By Clock Domain:

Clock Domain	Clock Frequency(Mhz)	Total Dynamic Power(mW)
clk2	100.000	0.053
clk1	100.000	0.072

5 Gowin Power Estimator

Gowin Power Estimator helps you accurately estimate the power consumption in design by configuring part number, operating environment, voltage, signal toggle rate and clock enable, etc. And Gowin Power Estimator shows the power consumption in the form of table.

5.1 POWER SUMMARY

POWER SUMMARY includes DEVICE, THERMAL INFO, VOLTAGE SOURCE POWER, BLOCK POWER, and POWER SUMMARY.

- DEVICE: Configure chip
- THERMAL INFO: Configure ambient temperature and thermal impedance, calculate the junction temperature.
- VOLTAGE SOURCE POWER: Show current and power consumption of each voltage source.
- BLOCK POWER: Show total dynamic power consumption of each module.
- POWER SUMMARY: Show total quiescent power consumption, total dynamic power consumption and total power consumption of each voltage source.

5.1.1 DEVICE

DEVICE configuration is as shown in Figure 5-1. It includes device, package, speed grade, and process, etc.

Figure 5-1 DEVICE

DEVICE	
DEVICE	GW2A_55C
PACKAGE	PBGA484
SPEED GRADE	8
PROCESS	WORST
TEMP GRADE	COMMERCIAL

- DEVICE: Device info.
- PACKAGE: Package info.
- SPEED GRADE: Speed grade info.
- Process: The process of the chip includes TYPICAL and WORST.
- TEMP GRADE: COMMERCIAL, INDUSTRIAL and AUTOMOTIVE

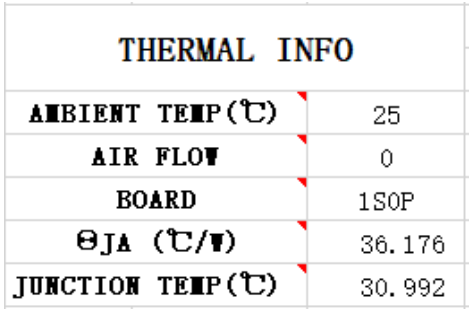
Note!

Device GW2A_55C is the GW2A-55C in Gowin Software.

5.1.2 THERMAL INFO

THERMAL INFO configuration is as shown in Figure 5-2. It includes ambient temperature, air flow, and board, etc.

Figure 5-2 THERMAL INFO



- AMBIENT TEMP: The range is -40~125℃, where the COMMERCIAL grade is 0~85℃; the INDUSTRIAL grade is -40~100℃, and the AUTOMOTIVE grade is -40~125℃.
- AIR FLOW: 0, 100, 200, 400, with unit of LFM
- BOARD: JEDEC-compliant PCB
- θ_{JA}: θ_{JA} is not configurable, and θ_{JA} is determined by the device package, air flow and board.
- JUNCTION TEMP: Junction temperature is not configurable, and it is determined by the external temperature, chip power consumption, and thermal impedance. When the junction temperature is greater than the maximum operating temperature of the chip, the bottom color of the junction temperature cell is marked red.

Note!

Move the mouse to the red triangle to show the explanation of the meaning of the item, same below.

5.1.3 VOLTAGE SOURCE POWER SUMMARY

VOLTAGE SOURCE POWER SUMMARY configuration is as shown in Figure 5-3, and it includes quiescent current, dynamic current, and power of each voltage source.

Figure 5-3 VOLTAGE SOURCE POWER SUMMARY

VOLTAGE SOURCE POWER SUMMARY

	VOLTAGE(V)	ICCQ(A)	ICC(A)	POWER(W)
VCC	1	0.080	0.000	0.080
VCCX	3.3	0.026	0.000	0.086
VCCO 3.3	3.3	0.000	0.000	0.000
VCCO 2.5	2.5	0.000	0.000	0.000
VCCO 1.8	1.8	0.000	0.000	0.000
VCCO 1.5	1.5	0.000	0.000	0.000
VCCO 1.2	1.2	0.000	0.000	0.000

- VOLTAGE: Source voltage, including VCC, VCCX in V
- ICCQ: Quiescent current (A) of each voltage source
- ICC: Dynamic current (A) of each voltage source
- POWER: The power consumption of each voltage source, i.e., quiescent power consumption + dynamic power consumption, with unit of W.
- VCC: Core voltage
- VCCX: Auxiliary voltage
- VCCO: Bank voltage VCCO 3.3 means the bank voltage is 3.3V, and for VCCO 2.5, VCCO 1.8, VCCO 1.5, VCCO 1.2 is also the same. The bank voltage is not configurable and is determined by the IO_TYPE in IO BLOCK.

5.1.4 BLOCK POWER

BLOCK POWER configuration is as shown in Figure 5-4, and it includes the dynamic power consumption of each module.

Figure 5-4 BLOCK POWER

BLOCK POWER

BLOCK	POWER(W)
CLOCK TREE	0.000
IO	0.000
LOGIC	0.000
BSRAM	0.000
DSP	0.000
PLL	0.000
DLLDLY	0.000

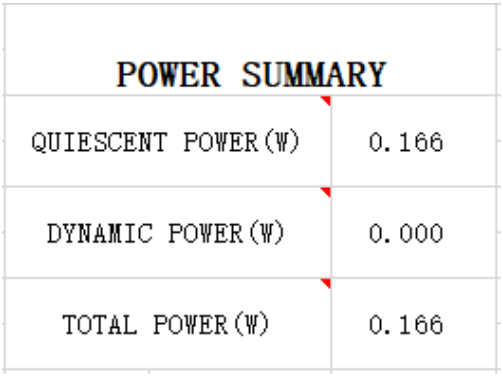
- BLOCK: Include CLOCK TREE module, IO module, LOGIC module, BSRAM module, DSP module, PLL module, DLLDLY module; click each module, and you can jump to the power consumption sheet to see the details.

- POWER: Dynamic power consumption, with unit of W

5.1.5 POWER SUMMARY

POWER SUMMARY configuration is as shown in Figure 5-5, and it includes quiescent current, dynamic current, and total power of all voltage sources.

Figure 5-5 POWER SUMMARY



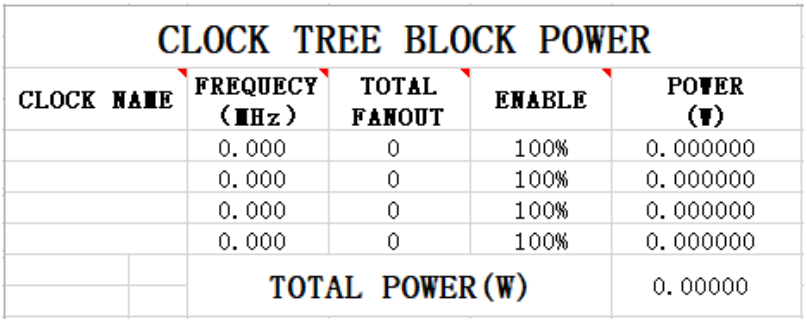
POWER SUMMARY	
QUIESCENT POWER(W)	0.166
DYNAMIC POWER(W)	0.000
TOTAL POWER(W)	0.166

- QUIESCENT POWER: Total quiescent power consumption of all voltage sources, with unit of W
- DYNAMIC POWER: Total dynamic power consumption of all voltage sources, with unit of W
- TOTAL POWER: Total power consumption of all voltage sources, with unit of W

5.2 CLOCK TREE BLOCK POWER

CLOCK TREE BLOCK POWER is as shown in Figure 5-6. The power consumption of the clock tree is calculated by configuring the clock frequency, the total fanout of the clock signal, and the clock enable.

Figure 5-6 CLOCK TREE BLOCK POWER



CLOCK TREE BLOCK POWER				
CLOCK NAME	FREQUECY (MHz)	TOTAL FANOUT	ENABLE	POWER (W)
	0.000	0	100%	0.000000
	0.000	0	100%	0.000000
	0.000	0	100%	0.000000
	0.000	0	100%	0.000000
	TOTAL POWER(W)			0.00000

- CLOCK NAME: Clock name
- FREQUENCY: Clock frequency in MHz
- TOTAL FANOUT: Total fanout of clock signal
- ENABLE: Percentage of clock enable
- POWER: The power consumption of each clock in the table, with unit of W

- TOTAL POWER: The total power consumption of all clocks, with unit of W

5.3 IO BLOCK POWER

5.3.1 INPUT & OUTPUT POWER

INPUT & OUTPUT POWER is used to configure the IO power consumption of input Buffer and output Buffer, as shown in Figure 5-7. The power consumption of IO is calculated by configuring clock frequency, IO_TYPE, IO data rate, IO toggle rate, capacitive load, and the number of I/Os.

Figure 5-7 INPUT & OUTPUT POWER

INPUT & OUTPUT POWER									
CLOCK NAME	FREQUECY (MHz)	IO TYPE	IO DATA RATE	TOGGLE RATE	OUTPUT CAPACITIVE LOAD(pF)	IN PINs	OUT PINs	BANK	POWER (W)
	0.000	LVCMOS18_8mA	SDR	12.50%	0	0	0	0	0.000000
	0.000	LVCMOS18_8mA	SDR	12.50%	0	0	0	0	0.000000
	0.000	LVCMOS18_8mA	SDR	12.50%	0	0	0	0	0.000000
	0.000	LVCMOS18_8mA	SDR	12.50%	0	0	0	0	0.000000
	0.000	LVCMOS18_8mA	SDR	12.50%	0	0	0	0	0.000000
	0.000	LVCMOS18_8mA	SDR	12.50%	0	0	0	0	0.000000
							TOTAL POWER (W)		0.000000

- CLOCK NAME: Clock name
- FREQUENCY: Clock frequency in MHz
- IO_TYPE: IO_TYPE and DRIVE
- IO DATA RATE: SDR and DDR
- TOGGLE RATE: Ratio of IO toggle rate to clock frequency
- OUTPUT CAPACITIVE LOAD: Capacitive load acting on the output signal
- IN PINs: Number of input pin or differential pair
- OUT PINs: Number of output pin or differential pair
- BANK: I/O bank
- POWER: Power consumption of each IO in the table, with unit of W.
- TOTAL POWER: Total power consumption of the IO configured by the INPUT & OUTPUT POWER module, with unit of W

5.3.2 BIDIRECTIONAL & TRI_STATE POWER

BIDIRECTIONAL & TRI_STATE POWER is used to configure the IO power consumption of bidirectional Buffer and three-state Buffer, as shown in Figure 5-8. The power consumption of IO is calculated by configuring clock frequency, IO_TYPE, IO data rate, IO toggle rate, capacitive load, output enable, and the number of INOUT.

Figure 5-8 BIDIRECTIONAL & TRI_STATE POWER

BIDIRECTIONAL & TRI_STATE POWER

CLOCK NAME	FREQUECY (MHz)	IO TYPE	IO DATA RATE	TOGGLE RATE	OUTPUT CAPACITIVE LOAD(pF)	INOUT PINs	OUTPUT ENABLE	BANK	POWER (W)
	0.000	LVCMOS18_8mA	SDR	12.50%	0	0	100.00%	0	0.000000
	0.000	LVCMOS18_8mA	SDR	12.50%	0	0	100.00%	0	0.000000
	0.000	LVCMOS18_8mA	SDR	12.50%	0	0	100.00%	0	0.000000
	0.000	LVCMOS18_8mA	SDR	12.50%	0	0	100.00%	0	0.000000
	0.000	LVCMOS18_8mA	SDR	12.50%	0	0	100.00%	0	0.000000
							TOTAL POWER (W)		0.000000
							IO POWER(W)		0

- CLOCK NAME: Clock name
- FREQUENCY: Clock frequency in MHz
- IO_TYPE: IO_TYPE and DRIVE
- IO DATA RATE: SDR and DDR
- TOGGLE RATE: Ratio of IO toggle rate to clock frequency
- OUTPUT CAPACITIVE LOAD: Capacitive load acting on the output signal
- INOUT PINs: Number of bidirectional Buffer, tri-state Buffer, or differential pair
- OUTPUT ENABLE: Percentage of output enable
- BANK: I/O bank, and the power consumption of each bank can be known by setting.
- POWER: Power consumption of each IO in the table, with unit of W
- TOTAL POWER: Total power consumption of the IO configured by the BIDIRECTIONAL & TRI_STATE POWER module, with unit of W
- IO POWER: Total power consumption of all I/Os, i.e. the power consumption of all I/Os of INPUT & OUTPUT POWER module and BIDIRECTIONAL & TRI_STATE POWER module, with unit of W

5.4 LOGIC BLOCK POWER

LOGIC BLOCK POWER configuration is as shown in Figure 5-9. The power consumption of Logic is calculated by configuring the clock frequency, the number of LUTs, SSRAMs, ALUs, FFs, the average fanout, and toggle rate of signals.

Figure 5-9 LOGIC BLOCK POWER

LOGIC BLOCK POWER

CLOCK NAME	FREQUECY (MHz)	LUTs	SSRAMs	ALUs	FFs	AVERAGE FANOUT	TOGGLE RATE	POWER (W)
	0.000	0	0	0	0	1	12.50%	0.000000
	0.000	0	0	0	0	1	12.50%	0.000000
	0.000	0	0	0	0	1	12.50%	0.000000
	0.000	0	0	0	0	1	12.50%	0.000000
	0.000	0	0	0	0	1	12.50%	0.000000
	0.000	0	0	0	0	1	12.50%	0.000000
					TOTAL POWER(W)			0.000000

- CLOCK NAME
- FREQUENCY: Clock frequency in MHz
- LUTs: Number of LUTs of the clock drive
- SSRAMs: Number of SSRAMs of the clock driver
- ALUs: Number of ALUs of the clock driver
- FFs: Number of FFs of the clock driver
- AVERAGE FANOUT: Average signal fanout of the clock drive logic module, which can take the values of 1, 2, 3, 4, 5.
- TOGGLE RATE: Average signal toggle rate of the clock drive logic module, with unit of %, indicating the ratio of the signal toggle rate to the clock frequency.
- POWER: Power consumption of each logic in the table, with unit of W
- TOTAL POWER: Total power consumption of all logics, with unit of W

5.5 BSRAM BLOCK POWER

5.5.1 SINGLE PORT BSRAM POWER

SINGLE PORT BSRAM POWER configuration is as shown in Figure 5-10. The power consumption of single port BSRAM is calculated by configuring the clock frequency, clock enable, read enable, write enable, data bit width, data signal toggle rate, and the number of BSRAMs.

Figure 5-10 SINGLE PORT BSRAM POWER

SINGLE PORT BSRAM POWER

CLOCK NAME	FREQUECY (MHz)	ENABLE RATE	READ RATE	WRITE RATE	BIT WIDTH	TOGGLE RATE	SPs	POWER (W)
	0.000	100%	100%	50%	1	12.50%	0	0.000000
	0.000	100%	100%	50%	1	12.50%	0	0.000000
	0.000	100%	100%	50%	1	12.50%	0	0.000000
	0.000	100%	100%	50%	1	12.50%	0	0.000000
	0.000	100%	100%	50%	1	12.50%	0	0.000000
						TOTAL POWER (W)		0.000000

- CLOCK NAME
- FREQUENCY: Signal port BSRAM clock frequency in MHz

- ENABLE RATE: Percentage of single port BSRAM clock enable
- READ ENABLE: Percentage of single port BSRAM read enable
- WRITE ENABLE: Percentage of single port BSRAM write enable
- BIT WIDTH: Bit width of single port BSRAM
- TOGGLE RATE: Average data signal toggle rate of single port BSRAM
- SPs: Number of single port BSRAM, the type of single port BSRAM in LittleBee and Arora family includes SP and SPX9.
- POWER: Power consumption of each single port BSRAM in the table, with unit of W
- TOTAL POWER: Total power consumption of all single port BSRAMs, with unit of W

5.5.2 SEMI DUAL-PORT BSRAM POWER

SEMI DUAL-PORT BSRAM POWER configuration is as shown in Figure 5-11. The power consumption of semi dual-port BSRAM is calculated by configuring the clock frequency, clock enable, read enable, write enable, data bit width, data signal toggle rate, and the number of BSRAMs.

Figure 5-11 SEMI DUAL-PORT BSRAM POWER

SEMI DUAL-PORT BSRAM POWER													
PORTA						PORTB							
PORTA CLOCK NAME	FREQUECY (MHz)	ENABLE RATE	WRITE RATE	BIT WIDTH	TOGGLE RATE	PORTB CLOCK NAME	FREQUECY (MHz)	ENABLE RATE	READ RATE	BIT WIDTH	TOGGLE RATE	SDPs	POWER (W)
	0.000	100%	100%	1	12.50%		0.000	100%	100%	1	12.50%	0	0.000000
	0.000	100%	100%	1	12.50%		0.000	100%	100%	1	12.50%	0	0.000000
	0.000	100%	100%	1	12.50%		0.000	100%	100%	1	12.50%	0	0.000000
	0.000	100%	100%	1	12.50%		0.000	100%	100%	1	12.50%	0	0.000000
	0.000	100%	100%	1	12.50%		0.000	100%	100%	1	12.50%	0	0.000000
											TOTAL POWER (W)		0.000000

- PORTA: Configure the clock frequency, clock enable, write enable, data bit width and toggle rate of port A.
- PORTB: Configure the clock frequency, clock enable, write enable, data bit width and toggle rate of port B.
- PORTA CLOCK NAME: Semi dual-port BSRAM port A clock name
- PORTA CLOCK NAME: Semi dual-port BSRAM port B clock name
- FREQUENCY: SEMI dual-port BSRAM clock frequency in MHz
- ENABLE RATE: Percentage of semi dual-port BSRAM clock enable
- READ RATE: Percentage of semi dual-port BSRAM read enable
- WRITE RATE: Percentage of semi dual-port BSRAM write enable
- BIT WIDTH: Bit width of semi dual-port BSRAM
- TOGGLE RATE: Average data signal toggle rate of semi dual-port BSRAM
- SPs: Number of semi dual-port BSRAM, the type of semi dual-port BSRAM in LittleBee and Arora family includes SDPB and SDPX9B.
- POWER: Power consumption of each semi dual-port BSRAM in the

table, with unit of W

- TOTAL POWER: Total power consumption of all semi dual-port BSRAM, with unit of W

5.5.3 DUAL-PORT BSRAM POWER

DUAL-PORT BSRAM POWER configuration is as shown in Figure 5-12. The power consumption of dual-port BSRAM is calculated by configuring the clock frequency, clock enable, read enable, write enable, data bit width, data signal toggle rate, and the number of BSRAMs.

Figure 5-12 DUAL-PORT BSRAM POWER

DUAL-PORT BSRAM POWER														
	PORTA						PORTB							
PORTA CLOCK NAME	FREQUECY (MHz)	ENABLE RATE	READ RATE	WRITE RATE	BIT WIDTH	PORTB CLOCK NAME	FREQUECY (MHz)	ENABLE RATE	READ RATE	WRITE RATE	BIT WIDTH	TOGGLE RATE	DPs	POWER (W)
	0.000	100%	100%	50%	1		0.000	100%	100%	50%	1	12.50%	0	0.000000
	0.000	100%	100%	50%	1		0.000	100%	100%	50%	1	12.50%	0	0.000000
	0.000	100%	100%	50%	1		0.000	100%	100%	50%	1	12.50%	0	0.000000
	0.000	100%	100%	50%	1		0.000	100%	100%	50%	1	12.50%	0	0.000000
	0.000	100%	100%	50%	1		0.000	100%	100%	50%	1	12.50%	0	0.000000
												TOTAL POWER		0.000000

- PORTA: Configure the clock frequency, clock enable, read enable, write enable, data bit width and toggle rate of port A.
- PORTB: Configure the clock frequency, clock enable, read enable, write enable, data bit width and toggle rate of port B.
- PORTA CLOCK NAME: Dual-port BSRAM port A clock name
- PORTA CLOCK NAME: Dual-port BSRAM port B clock name
- FREQUENCY: Dual-port BSRAM clock frequency in MHz
- ENABLE RATE: Percentage dual-port BSRAM clock enable
- READ RATE: Percentage dual-port BSRAM read enable
- WRITE ENABLE: Percentage dual-port BSRAM write enable
- BIT WIDTH: The bit width of dual-port
- TOGGLE RATE: Average data signal toggle rate of dual-port BSRAM
- DPs: Number of dual-port BSRAM, the type of dual-port BSRAM in LittleBee and Arora family includes DPB and DPX9B.
- POWER: Power consumption of each dual-port BSRAM in the table, with unit of W
- TOTAL POWER: Total power consumption of all dual-port BSRAMs, with unit of W

5.5.4 BLOCK ROM POWER

BLOCK ROM POWER configuration is as shown in Figure 5-13. The power consumption of BLOCK ROM is calculated by configuring the clock frequency, clock enable, read enable, data signal toggle rate, and the number of BSRAMs.

Figure 5-13 BLOCK ROM POWER

BLOCK ROM POWER							
CLOCK NAME	FREQUECY (MHz)	ENABLE RATE	READ RATE	BIT WIDTH	TOGGLE RATE	ROMs	POWER (W)
	0.000	100%	100%	1	12.50%	0	0.000000
	0.000	100%	100%	1	12.50%	0	0.000000
	0.000	100%	100%	1	12.50%	0	0.000000
	0.000	100%	100%	1	12.50%	0	0.000000
	0.000	100%	100%	1	12.50%	0	0.000000
					TOTAL POWER (W)		0.000000
					BSRAM TOTAL POWER		0.000000

- CLOCK NAME
- FREQUENCY: ROM clock frequency in MHz
- ENABLE RATE: Percentage ROM clock enable
- READ RATE: Percentage ROM read enable
- BIT WIDTH: ROM bit width
- TOGGLE RATE: Average data signal toggle rate of ROM
- ROMs: Number of ROMs, the type of ROM in LittleBee and Arora family includes pROM and pROMX9.
- POWER: Power consumption of each BLOCK ROM in the table, with unit of W
- TOTAL POWER: Total power consumption of all BLOCK ROM, with unit of W
- BSRAM TOTAL POWER: Power consumption of all BSRAMs, including single port BSRAM, semi dual-port BSRAM, dual-port BSRAM and BLOCK ROM, with unit of W

5.6 DSP BLOCK POWER

DSP BLOCK POWER configuration is as shown in Figure 5-14. The power consumption of DSP is calculated by configuring clock frequency, toggle rate, DSP type, and the number of DSP.

Figure 5-14 DSP BLOCK POWER

DSP BLOCK POWER					
CLOCK NAME	FREQUECY (MHz)	TOGGLE RATE	DSP TYPE	DSPs	POWER (W)
	0.000	12.50%	MULT9X9	0	0.000000
	0.000	12.50%	MULT9X9	0	0.000000
	0.000	12.50%	MULT9X9	0	0.000000
	0.000	12.50%	MULT9X9	0	0.000000
	0.000	12.50%	MULT9X9	0	0.000000
	0.000	12.50%	MULT9X9	0	0.000000
	0.000	12.50%	MULT9X9	0	0.000000
	0.000	12.50%	MULT9X9	0	0.000000
	0.000	12.50%	MULT9X9	0	0.000000
				TOTAL POWER	0.000000

- CLOCK NAME
- FREQUENCY: Clock frequency in MHz
- TOGGLE RATE: Average toggle rate of DSP output signal
- DSP TYPE: The type of DSP in LittleBee and Arora family includes MULT9X9, MULT18X18, MULT36X36, PADD9, PADD18, MAULTALU18X18, MAULTALU36X18, MULTADDALU18X18, ALU54D.
- DSPs: Number of DSPs
- POWER: Power consumption of each DSP in the table, with unit of W
- TOTAL POWER: Total power consumption of all DSPs,with unit of W

5.7 PLL BLOCK POWER

PLL BLOCK POWER configuration is as shown in Figure 5-15. The power consumption is calculated by configuring input clock frequency and the number of PLL.

Figure 5-15 PLL BLOCK POWER

PLL BLOCK POWER

CLOCK NAME	FREQUECY (MHz)	PLLs	POWER (W)
	0.000	0	0.000000
	0.000	0	0.000000
	0.000	0	0.000000
	0.000	0	0.000000
	0.000	0	0.000000
	0.000	0	0.000000
	0.000	0	0.000000
	0.000	0	0.000000
	TOTAL POWER(W)		0.000000

- CLOCK NAME
- FREQUENCY: PLL input clock frequency in MHz
- PLLs: Number of PLLs
- POWER: Power consumption of each PLL in the table, with unit of W
- TOTAL POWER: Total power consumption of all PLLs, with unit of W

5.8 DLLDLY BLOCK POWER

DLLDLY BLOCK POWER configuration is as shown in Figure 5-16. The power consumption is calculated by configuring input clock frequency and the number of DLLDLYs.

Figure 5-16 DLLDLY BLOCK POWER

DLLDLY BLOCK POWER			
CLOCK NAME	FREQUECY (MHz)	DLLDLYs	POWER (W)
	0.000	0	0.000000
	0.000	0	0.000000
	0.000	0	0.000000
	0.000	0	0.000000
	0.000	0	0.000000
	0.000	0	0.000000
	0.000	0	0.000000
	0.000	0	0.000000
	TOTAL POWER(W)		0.000000

- CLOCK NAME
- FREQUENCY: DLLDLY input clock frequency in MHz
- DLLDLYs: Number of DLLDLYs
- POWER: Power consumption of each DLLDLY in the table, with unit of W
- TOTAL POWER: Total power consumption of all DSPs, with unit of W

Appendix A Calculation Principle for Junction Temperature

Junction temperature (TJ) refers to the operating temperature of die, which is determined by ambient temperature (TA), power consumption (P) and heat sink features of chip and outside. The temperature of die is balanced by heat sink and ambient environment. Heat sink includes two types: heat sink and no heat sink.

- No heat sink

The model mainly dissipates heat through development board and CASE. Thermal impedance (θ_{JA}) means rising temperature corresponding to power consumption (℃ / W), which is influenced by air flow; In no heat sink mode, The relationships between power P and thermal impedance θ_{JA}, TJ, TA are shown in Formula 1.

$$P = (TJ - TA) / \theta_{JA} \text{ (Formula 1)}$$

- Heat Sink

Chip dissipates heat by heat sink, and the total thermal impedance of it is called θ_{JA}. Chip dissipates heat by board thermal, and the thermal impedance of it is called θ_{JB}.

θ_{JA} consists of three parts: thermal impedance θ_{JC} from chip to case, thermal impedance θCS from case to heat sink, and thermal impedance θ_{SA} from heat sink to ambient environment. The calculation formula is as follow:

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA} \text{ (Formula 2)}$$

The relationship between power P and thermal impedance θ_{JA}, θ_{JB} and TJ, TA, TB (board temperature) is shown in formula 3:

$$P = (TJ - TA) / \theta_{JA} + (TJ - TB) / \theta_{JB} \text{ (Formula 3)}$$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