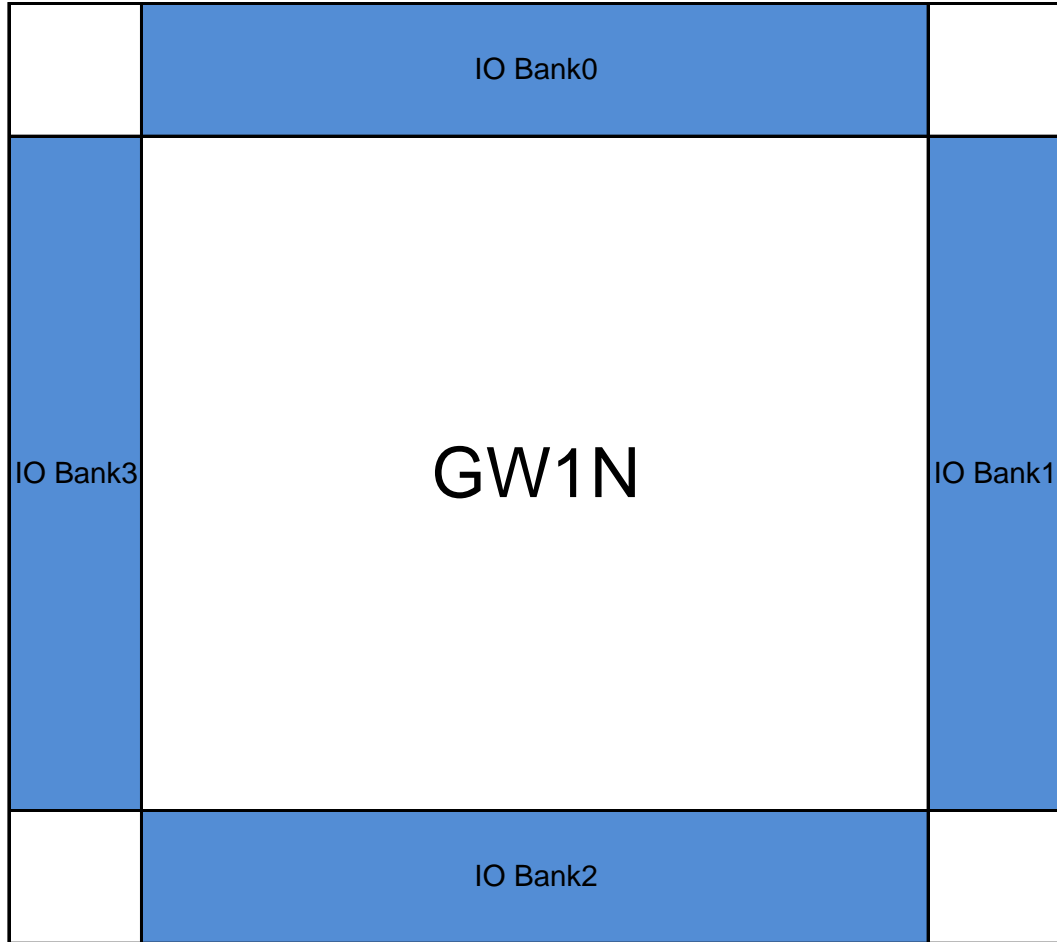


Date	Version	Description
03/01/2016	1.05E	Initial version published.
04/20/2016	1.06E	The info. of pin list and True LVDS for GW1N-2 & GW1N-4 updated.
06/16/2016	1.07E	Pin K11 of PG256 package added.
06/22/2016	1.08E	Pin A2 of PG256 package updated.
07/04/2016	1.09E	This version is the Pinout manual for the Production version of the GW1N-2/4 device. The assignment of the dual-purpose function R_PLL_in has been updated from IOR2A/B to IOR3A/B. R_PLL_in has been packaged in the LQ100, LQ144, MG160 and PG256 packages, but not in the package CS72.
07/18/2016	1.10E	The True LVDS corresponding to the IOR2A/B in BANK 1 of LQ100, LQ144 and MG160 packages are not packaged. The info. of Package QN32 added. Other pin info. of MG160 package for GW1N-2/4.
02/18/2019	1.2E	Recommended operating conditions of VCC UV version updated.
05/15/2019	1.3E	Recommended operating conditions of VCCO UV version updated.
03/03/2020	1.4E	The info. of MG132X package added.
03/30/2020	1.5E	The info. of MG132X package added. The pin descriptions of MODE0/MODE1/MODE2 added. The info. of Power improved.
04/16/2020	1.6E	The info. of GW1N-2/GW1N-2B devices removed.
10/12/2021	1.7E	Pin definitions updated.
03/25/2022	1.8E	The info. of UG169 package added.
06/10/2022	1.8.1E	Pin G5 and H6 of UG169 package updated.
10/20/2022	1.8.2E	The note in Power sheet updated. The note in Pin Definitions sheet updated.
05/04/2023	1.8.3E	The description of CLKHOLD_N pin in Pin Definitions sheet updated. The notes of QN48, QN32, and QN88 packages in Power sheet updated.
06/30/2023	1.8.4E	The descriptions of Pin Definitions and info. for MODE0, MODE1, MODE2 pins optimized.
11/01/2024	1.8.5E	The description of EPAD pin in Pin Definitions sheet added. The I/O descriptions of Ready and Done pins in Pin Definitions sheet optimized.

Pin Name	I/O	Description
User I/O		
IO[End][Row/Column Number][A/B]	I/O	[End] indicates the pin location, including L(left), R(right), B(bottom), and T(top).
		[Row/Column Number] indicates the pin row/column number. If [End] is T(top) or B(bottom), the pin indicates the column number of the corresponding CFU. If [End] is L(left) or R(right), the pin indicates the row number of the corresponding CFU.
		[A/B] indicates differential signal pair information.
Multi-Function Pins		
IO[End][Row/Column Number][A/B]/MMM		/MMM represents one or more of the other functions in addition to being general purpose user I/O. When these functions are not in use, these pins can be used as user I/O.
D0	I/O	Data port D0 in CPU mode
D1	I/O	Data port D1 in CPU mode
D2	I/O	Data port D2 in CPU mode
D3	I/O	Data port D3 in CPU mode
D4	I/O	Data port D4 in CPU mode
D5	I/O	Data port D5 in CPU mode
D6	I/O	Data port D6 in CPU mode
D7	I/O	Data port D7 in CPU mode
WE_N	I	Select data input/output of D[7:0] in CPU mode.0: Write;1: Read.
DOUT	O	Data output in SERIAL mode
DIN	I, internal weak pull-up	Data input in SERIAL mode
TMS	I, internal weak pull-up	Serial mode input in JTAG mode
TCK	I	Serial clock input in JTAG mode
TDO	O	Serial data output in JTAG mode
TDI	I, internal weak pull-up	Serial data input in JTAG mode
JTAGSEL_N	I, internal weak pull-up	Reconfigure JTAG download function signal
RECONFIG_N	I, internal weak pull-up	Global reset GowinCONFIG logic signal, active low
FASTRD_N	I	Access SPI FLASH to select signal. Low, Fast Read mode; High, Read mode.
DONE ^[1]	O, internal weak pull-up	High, the programming configuration has been completed successfully; Low, the programming configuration has not been completed or failed.
	I, internal weak pull-up	When the DONE signal is low, delay the chip to activate. Activate the chip until the DONE signal is high.
READY ^[1]	I/O, internal weak pull-up	High, the device can be programmed and configured currently; Low, the device cannot be programmed and configured currently.
MI	I	MI in MSPI mode

Pin Name	I/O	Description
MO	O	MO in MSPI mode
MCS_N	O	Enable signal MCS_N in MSPI mode, active-low
MCLK	O	Clock output MCLK in MSPI mode, with default frequency of 2.5Mhz
SCLK	I	Clock input in SSPI, SERIAL, and CPU modes
SO	O	SO in SSPI mode
SI	I/O	SI in SSPI mode
SSPI_CS_N	I/O	Enable signal SSPI_CS_N in SSPI mode, active-low, and internal weak pull-up
CLKHOLD_N	I, internal weak pull-up	Active-high in SSPI mode; Active-low in CPU mode.
GCLKC_[x]	I	Differential input pin of GCLKT_[x], C(Comp), [x] is global clock number ^[2]
GCLKT_[x]	I	Global clock input pin, T(True), [x] is global clock number
LPLL_C_fb/RPLL_C_fb	I	Left/Right PLL feedback input pin, C(Comp)
LPLL_T_fb/RPLL_T_fb	I	Left/Right PLL feedback input pin, T(True)
LPLL_C_in/RPLL_C_in	I	Left/Right PLL clock input pin, C(Comp)
LPLL_T_in/RPLL_T_in	I	Left/Right PLL clock input pin, T(True)
MODE2	I, internal weak pull-up	GowinCONFIG modes selection pin; if this pin is marked as "VCCIO", it's internally powered; if this pin is marked as "GND", it's internally grounded.
MODE1	I, internal weak pull-up	GowinCONFIG modes selection pin; if this pin is marked as "VCCIO", it's internally powered; if this pin is marked as "GND", it's internally grounded.
MODE0	I, internal weak pull-up	GowinCONFIG modes selection pin; if this pin is marked as "VCCIO", it's internally powered; if this pin is marked as "GND", it's internally grounded.
Other Pins		
NC	NA	Reserved
VSS	NA	Ground
VCC	NA	Power supply pin of core voltage
VCCIO#	NA	Power supply pin of I/O voltage for I/O BANK#
VCCX	NA	Power supply pin of auxiliary voltage
EPAD	NA	Exposed pad. Connect to ground.
Note!		
^[1] The default state of READY and DONE is open-drain output, internal weak pull-up. DONE outputs 0 during configuration. ^[2] When the input is single-ended, GCLKC_[x] pin is not a global clock.		



Note!

- [1] Each Bank has independent reference voltage (VREF).
- [2] You can select to use IOB internal VREF (equals to 0.5 X VCCIO).
- [3] You can also select to use external VREF input (use any I/O pins as external VREF input).

Note!
^[1] The pin is internally grounded.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	QN32	QN48	CS72	QN88	LQ100	MG132X	LQ144	MG160	UG169	PG256	PG256M
IOB10A	I/O	2		True_of_IOB10B	NONE				29	31	J13	44	N4		C1	R3
IOB10B	I/O	2		Comp_of_IOB10A	NONE				30	32	K12	45	P4		D2	R4
IOB11A	I/O	2		True_of_IOB11B	NONE							46	N5		E1	P5
IOB11B	I/O	2		Comp_of_IOB11A	NONE							47	P5		F2	R5
IOB12A	I/O	2		True_of_IOB12B	TRUE		15	D6	31	33	J12	48	L6	M7	F4	M7
IOB12B	I/O	2		Comp_of_IOB12A	TRUE		16	E6	32	34	J14	49	M6	N6	G6	M8
IOB13A	I/O	2		True_of_IOB13B	NONE										F3	R6
IOB13B	I/O	2		Comp_of_IOB13A	NONE										F1	P6
IOB14A	I/O	2		True_of_IOB14B	TRUE			H6	33	35		50	L7	N8	G5	T4
IOB14B	I/O	2		Comp_of_IOB14A	TRUE			G6		36		51	M7	N7	G4	T5
IOB15A	I/O	2		True_of_IOB15B	NONE				34						G2	N7
IOB15B	I/O	2		Comp_of_IOB15A	NONE										G3	P7
IOB16A	I/O	2		True_of_IOB16B	TRUE						G12	52	N6	K6	F5	T6
IOB16B	I/O	2		Comp_of_IOB16A	TRUE						G14	54	P6	J6	H6	T7
IOB17A	I/O	2		True_of_IOB17B	NONE									M9	G1	R7
IOB17B	I/O	2		Comp_of_IOB17A	NONE									M8	H2	T8
IOB18A	I/O	2		True_of_IOB18B	TRUE		17							K7	H4	N8
IOB18B	I/O	2		Comp_of_IOB18A	TRUE		18							J7	J6	P8
IOB19A/GCLKT_5	I/O	2	GCLKT_5	True_of_IOB19B	NONE					39	G13	56	N7	N12	J1	R8
IOB19B/GCLKC_5	I/O	2	GCLKC_5	Comp_of_IOB19A	NONE					40	H12	57	P7	N11	J3	T9
IOB20A/GCLKT_4	I/O	2	GCLKT_4	True_of_IOB20B	TRUE	4	19	G5	35	41		58	L8	M12	L2	T10
IOB20B/GCLKC_4	I/O	2	GCLKC_4	Comp_of_IOB20A	TRUE	5	20	F5	36	42		59	M8	M13	M1	R9
IOB21A	I/O	2		True_of_IOB21B	NONE							60	L9		H3	P9
IOB21B	I/O	2		Comp_of_IOB21A	NONE							61	M9		H1	N9
IOB22A	I/O	2		True_of_IOB22B	TRUE			D4			F13	62	N8		J2	T11
IOB22B	I/O	2		Comp_of_IOB22A	TRUE			D5			F14	63	P8		K1	R10
IOB23A	I/O	2		True_of_IOB23B	NONE										H5	P10
IOB23B	I/O	2		Comp_of_IOB23A	NONE										J4	R11
IOB24A	I/O	2		True_of_IOB24B	TRUE			E4		43	E13	64	N9		K3	M9
IOB24B	I/O	2		Comp_of_IOB24A	TRUE			E5		44	F12	65	P9		K2	M10
IOB25A	I/O	2		True_of_IOB25B	NONE										J5	T12
IOB25B	I/O	2		Comp_of_IOB25A	NONE										K6	R12
IOB26A	I/O	2		True_of_IOB26B	TRUE		21	H4		45	E12	66	L10	N9	L1	N10
IOB26B	I/O	2		Comp_of_IOB26A	TRUE		22	G4	37	46	E14	67	M10	N10	L3	P11
IOB27A	I/O	2		True_of_IOB27B	NONE										K4	T13
IOB27B	I/O	2		Comp_of_IOB27A	NONE				38						L5	R13
IOB28A	I/O	2		True_of_IOB28B	NONE				39			68	N10		K5	N11
IOB28B	I/O	2		Comp_of_IOB28A	NONE				40			69	P10		L4	P12
IOB29A	I/O	2		True_of_IOB29B	NONE										N2	R14
IOB29B	I/O	2		Comp_of_IOB29A	NONE										P1	T15

Note!																
[1] The pin is internally grounded.																
Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	QN32	QN48	CS72	QN88	LQ100	MG132X	LQ144	MG160	UG169	PG256	PG256M
I/OB2A	I/O	2		True_of_I/OB2B	TRUE				17		N13			L4	A4	L3
I/OB2B	I/O	2		Comp_of_I/OB2A	TRUE				18		N14			L5	C5	M3
I/OB30A	I/O	2		True_of_I/OB30B	TRUE			F4	41	47	C14	70	P11		M3	N12
I/OB30B	I/O	2		Comp_of_I/OB30A	TRUE			F3	42	48	D12	71	N11		N1	P13
I/OB31A	I/O	2		True_of_I/OB31B	NONE										M2	M11
I/OB31B	I/O	2		Comp_of_I/OB31A	NONE										N3	L11
I/OB32A	I/O	2		True_of_I/OB32B	TRUE		23	H3		49	B14		P12	L11	R1	P15
I/OB32B	I/O	2		Comp_of_I/OB32A	TRUE		24	G3		50	C13		N12	M11	P2	R16
I/OB33A	I/O	2		True_of_I/OB33B	NONE								P13		P4	M12
I/OB33B	I/O	2		Comp_of_I/OB33A	NONE										T4	N13
I/OB34A	I/O	2		True_of_I/OB34B	TRUE					55		75	M14	K8	T2	M13
I/OB34B	I/O	2		Comp_of_I/OB34A	TRUE					53		72	N14	J8	R3	L12
I/OB35A	I/O	2		True_of_I/OB35B	NONE								K13		R5	N14
I/OB35B	I/O	2		Comp_of_I/OB35A	NONE								L14		P5	P14
I/OB36A	I/O	2		True_of_I/OB36B	TRUE			G1				78	J13	L10	T3	N16
I/OB36B	I/O	2		Comp_of_I/OB36A	TRUE			G2	47			76	L13	M10	R4	N15
I/OB37A	I/O	2		True_of_I/OB37B	NONE										T5	L13
I/OB37B	I/O	2		Comp_of_I/OB37A	NONE										R6	L14
I/OB3A	I/O	2		True_of_I/OB3B	NONE										D6	
I/OB3B	I/O	2		Comp_of_I/OB3A	NONE										E7	
I/OB4A	I/O	2		True_of_I/OB4B	TRUE	32			19		M12			M5	A3	N1
I/OB4B	I/O	2		Comp_of_I/OB4A	TRUE	1			20	22	M14	32	L1	M4	B4	N2
I/OB5A	I/O	2		True_of_I/OB5B	NONE									J5	A5	L4
I/OB5B	I/O	2		Comp_of_I/OB5A	NONE					23		34	M1	K5	B6	L5
I/OB6A	I/O	2		True_of_I/OB6B	TRUE		13	H7	25	27	L14	38	N1		B1	P2
I/OB6B	I/O	2		Comp_of_I/OB6A	TRUE		14	G7	26	28	M13	39	P2		C2	N3
I/OB7A	I/O	2		True_of_I/OB7B	NONE							40	N3		D3	N6
I/OB7B	I/O	2		Comp_of_I/OB7A	NONE							41	P3		D1	M6
I/OB8A	I/O	2		True_of_I/OB8B	TRUE			F7	27	29	K13	42	L5	N5	E2	P4
I/OB8B	I/O	2		Comp_of_I/OB8A	TRUE			F6	28	30	K14	43	M5	N4	E3	N5
I/OB9A	I/O	2		True_of_I/OB9B	NONE										B3	T2
I/OB9B	I/O	2		Comp_of_I/OB9A	NONE										A2	R1
I/OIOL10A/TMS	I/O	3	TMS	True_of_I/OIOL10B	NONE	24	4	D8	5	8	A6	13	F1	G1	B8	N4
I/OIOL10B/TCK	I/O	3	TCK	Comp_of_I/OIOL10A	NONE	25	5	D7	6	9	B6	14	G1	G2	A7	P3
I/OIOL10C/SCLK	I/O	3	SCLK	True_of_I/OIOL10D	NONE			D3		10		15	F3		C10	K5
I/OIOL10D/TDI	I/O	3	TDI	Comp_of_I/OIOL10C	NONE	27	6	E7	7	11	B4	16	G4	F5	A6	L6
I/OIOL10E/TDO	I/O	3	TDO	True_of_I/OIOL10F	NONE	28	7	E8	8	12	A4	18	G3	F6	C6	M5
I/OIOL10F/RECONFIG_N	I/O	3	RECONFIG_N	Comp_of_I/OIOL10E	NONE	29	8		9	14	C10	20	H3	H1	B10	M4
I/OIOL10G/DONE	I/O	3	DONE	True_of_I/OIOL10H	NONE	30	9		10	15	A13	21	J4	H4	C13	G3
I/OIOL10H/READY	I/O	3	READY	Comp_of_I/OIOL10G	NONE					16	B13	22	H2	H5	A13	G2

Note!
^[1] The pin is internally grounded.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	QN32	QN48	CS72	QN88	LQ100	MG132X	LQ144	MG160	UG169	PG256	PG256M
IOL10I	I/O	3		True_of_IOL10J	NONE							23	H1		F9	H4
IOL10J	I/O	3		Comp_of_IOL10I	NONE							24	K3		E11	H3
IOL11A/GCLKT_6	I/O	3	GCLKT_6	True_of_IOL11B	TRUE		10	F9	11	17	A7	25	J2	G4	C8	J5
IOL11B/GCLKC_6	I/O	3	GCLKC_6	Comp_of_IOL11A	TRUE		11	F8		18	B7	26	J3	F4	A8	J4
IOL12A	I/O	3		True_of_IOL12B	NONE									H3	B9	G1
IOL12B	I/O	3		Comp_of_IOL12A	NONE									H2	A10	H2
IOL13A	I/O	3		True_of_IOL13B	TRUE			G9		19	B5	27	J1	J2	F8	H1
IOL13B	I/O	3		Comp_of_IOL13A	TRUE			G8		20	C6	28	K1	J1	D9	J1
IOL14A	I/O	3		True_of_IOL14B	NONE									L1	D8	J3
IOL14B	I/O	3		Comp_of_IOL14A	NONE									L2	E9	J2
IOL15A	I/O	3		True_of_IOL15B	TRUE				13		A3	29	K2	M2	B7	K1
IOL15B	I/O	3		Comp_of_IOL15A	TRUE				14		C4	30	L2	M1	C7	K2
IOL16A	I/O	3		True_of_IOL16B	NONE									N3	F7	L1
IOL16B	I/O	3		Comp_of_IOL16A	NONE									N2	E8	L2
IOL17A	I/O	3		True_of_IOL17B	TRUE				15		A2			L3	C4	K3
IOL17B	I/O	3		Comp_of_IOL17A	TRUE				16		B3			M3	B5	K4
IOL18A	I/O	3		True_of_IOL18B	NONE									K2	E6	M1
IOL18B	I/O	3		Comp_of_IOL18A	NONE									K1	D7	M2
IOL2A	I/O	3		True_of_IOL2B	TRUE				3		C12	3	C1	C2	B14	C2
IOL2B	I/O	3		Comp_of_IOL2A	TRUE						A12		D2	D1	A15	D3
IOL3A/JTAGSEL_N/LPLL_T_in	I/O	3	JTAGSEL_N/LPLL_T_in	True_of_IOL3B	NONE		3	B7	4	3	B9	4	E2	E5	C12	E4
IOL3B/LPLL_C_in	I/O	3	LPLL_C_in	Comp_of_IOL3A	NONE			C7		5		6	E3		B12	E3
IOL4A/LPLL_T_fb	I/O	3	LPLL_T_fb	True_of_IOL4B	TRUE			B9				7	E4	E4	B13	D2
IOL4B/LPLL_C_fb	I/O	3	LPLL_C_fb	Comp_of_IOL4A	TRUE			B8				8	F4	E3	A14	D1
IOL5A	I/O	3		True_of_IOL5B	NONE						A11			B1	F10	F5
IOL5B	I/O	3		Comp_of_IOL5A	NONE						B12			C1	D11	G5
IOL6A	I/O	3		True_of_IOL6B	TRUE			C9			A10	9	D1	E1	B11	F4
IOL6B	I/O	3		Comp_of_IOL6A	TRUE			C8			C11	10	E1	F1	A12	F3
IOL7A	I/O	3		True_of_IOL7B	NONE										A11	E2
IOL7B	I/O	3		Comp_of_IOL7A	NONE										C11	E1
IOL8A	I/O	3		True_of_IOL8B	TRUE						C9		H4		D10	F2
IOL8B	I/O	3		Comp_of_IOL8A	TRUE						A9		K4		E10	F1
IOL9A/GCLKT_7	I/O	3	GCLKT_7	True_of_IOL9B	NONE	26				6	C8	11	F2	H6	A9	H5
IOL9B/GCLKC_7	I/O	3	GCLKC_7	Comp_of_IOL9A	NONE					7	B8	12	G2	G5	C9	G4
IOR10A/MI/D7	I/O	1	MI/D7	True_of_IOR10B	NONE	13	34		62	68	N4	96	F14	H9	P10	D16
IOR10B/MO/D6	I/O	1	MO/D6	Comp_of_IOR10A	NONE	12	33		61	67	P13	95	G14	H8	R10	E16
IOR10C/MCS_N/D5	I/O	1	MCS_N/D5	True_of_IOR10D	NONE	11	32		60	66	P3	94	E12	F12	M9	F14
IOR10D/MCLK/D4	I/O	1	MCLK/D4	Comp_of_IOR10C	NONE	10	31		59	65	M4	93	G12	E12	L10	G14
IOR10E/FASTRD_N/D3	I/O	1	FASTRD_N/D3	True_of_IOR10F	NONE				57	64		92	G11	G13	R9	F15

Note!																
[1] The pin is internally grounded.																
Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	QN32	QN48	CS72	QN88	LQ100	MG132X	LQ144	MG160	UG169	PG256	PG256M
IOR10F/SI/D2	I/O	1	SI/D2	Comp_of_IOR10E	NONE			E2		62		90	G13	G12	T10	G15
IOR10G/SO/D1	I/O	1	SO/D1	True_of_IOR10H	NONE			E3	56	61		88	H14	F8	M8	F16
IOR10H/SSPI_CS_N/D0	I/O	1	SSPI_CS_N/D0	Comp_of_IOR10G	NONE			D2	55	60	N12	87	J11	E9	N9	G16
IOR10I/DIN/CLKHOLD_N	I/O	1	DIN/CLKHOLD_N	True_of_IOR10J	NONE				54	59		86	H13	J13	T9	H14
IOR10J/DOUT/WE_N	I/O	1	DOUT/WE_N	Comp_of_IOR10I	NONE				53	58		85	H12	H13	P9	H15
IOR11A/GCLKT_3	I/O	1	GCLKT_3	True_of_IOR11B	TRUE	9	30	F1	52	57	M7	84	J14	G9	T7	H12
IOR11B/GCLKC_3	I/O	1	GCLKC_3	Comp_of_IOR11A	TRUE	8	29	F2	51	56	N8	83	K14	G10	R8	H13
IOR12A	I/O	1		True_of_IOR12B	NONE						P7				N8	H16
IOR12B	I/O	1		Comp_of_IOR12A	NONE						N7				L9	J15
IOR13A	I/O	1		True_of_IOR13B	TRUE						P9		E11	J9	P8	J13
IOR13B	I/O	1		Comp_of_IOR13A	TRUE						N9		F11	H10	T8	J14
IOR14A	I/O	1		True_of_IOR14B	NONE						N5			L13	M6	J16
IOR14B	I/O	1		Comp_of_IOR14A	NONE						M5			K13	L8	K16
IOR15A	I/O	1		True_of_IOR15B	TRUE						P8	82	J12	K12	M7	K15
IOR15B	I/O	1		Comp_of_IOR15A	TRUE				50		M8	81	H11	J12	N7	L15
IOR16A	I/O	1		True_of_IOR16B	NONE						N3				R7	K14
IOR16B	I/O	1		Comp_of_IOR16A	NONE						P4				P7	K13
IOR17A	I/O	1		True_of_IOR17B	TRUE		28		49			80	K12	K11	N6	L16
IOR17B	I/O	1		Comp_of_IOR17A	TRUE		27		48		M3	79	K11	L12	L7	M16
IOR18A	I/O	1		True_of_IOR18B	NONE						P2			K10	P6	M15
IOR18B	I/O	1		Comp_of_IOR18A	NONE						N2			J10	T6	M14
IOR2A	I/O	1		True_of_IOR2B	TRUE			B1						D12	T15	C13
IOR2B	I/O	1		Comp_of_IOR2A	TRUE			B2						D11	R14	C14
IOR3A/RPLL_T_in	I/O	1	RPLL_T_in	True_of_IOR3B	NONE	17	35		63	73		106	B14	E10	R12	F11
IOR3B/RPLL_C_in	I/O	1	RPLL_C_in	Comp_of_IOR3A	NONE	16				72		104	C14	D9	P13	F12
IOR4A/RPLL_T_fb	I/O	1	RPLL_T_fb	True_of_IOR4B	TRUE			C3				102	D14	B13	P12	E13
IOR4B/RPLL_C_fb	I/O	1	RPLL_C_fb	Comp_of_IOR4A	TRUE			B3				101	E14	A12	T13	D14
IOR5A	I/O	1		True_of_IOR5B	NONE									C12	R11	C15
IOR5B	I/O	1		Comp_of_IOR5A	NONE									C11	T12	B16
IOR6A	I/O	1		True_of_IOR6B	TRUE						M11	100	D13	B12	R13	E14
IOR6B	I/O	1		Comp_of_IOR6A	TRUE						P12	99	E13	B11	T14	F13
IOR7A	I/O	1		True_of_IOR7B	NONE						M10			C13	M10	G13
IOR7B	I/O	1		Comp_of_IOR7A	NONE						P11			D13	N11	G12
IOR8A	I/O	1		True_of_IOR8B	TRUE			C1			M9			F9	T11	D15
IOR8B	I/O	1		Comp_of_IOR8A	TRUE			C2			N10			F10	P11	E15
IOR9A/GCLKT_2	I/O	1	GCLKT_2	True_of_IOR9B	NONE	14				70	N6	98	F13	F13	N10	J12
IOR9B/GCLKC_2	I/O	1	GCLKC_2	Comp_of_IOR9A	NONE					69	P6	97	F12	E13	M11	K12
IOT12A	I/O	0		True_of_IOT12B	NONE				79		C1	134	A6			
IOT12B	I/O	0		Comp_of_IOT12A	NONE						C3	133	A7			
IOT13A	I/O	0		True_of_IOT13B	NONE									A4	G15	C7

Note!																
[1] The pin is internally grounded.																
Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	QN32	QN48	CS72	QN88	LQ100	MG132X	LQ144	MG160	UG169	PG256	PG256M
IOT13B	I/O	0		Comp_of_IOT13A	NONE									A3	G14	D7
IOT14A	I/O	0		True_of_IOT14B	NONE			B6		93	B1	132	C6	B7	G11	B6
IOT14B	I/O	0		Comp_of_IOT14A	NONE			C6		92	B2	131	D6		H12	B5
IOT15A	I/O	0		True_of_IOT15B	NONE									A5	G16	A6
IOT15B	I/O	0		Comp_of_IOT15A	NONE										H15	B7
IOT16A	I/O	0		True_of_IOT16B	NONE	22	45			91	K1	130	C7	C4	H13	E7
IOT16B	I/O	0		Comp_of_IOT16A	NONE	21	44			90	K3	129	D7	C5	J12	E8
IOT17A	I/O	0		True_of_IOT17B	NONE	20				89		128	B7	B6	H14	D8
IOT17B	I/O	0		Comp_of_IOT17A	NONE								B8	B5	H16	C8
IOT18A	I/O	0		True_of_IOT18B	NONE						G3		A8		J16	A7
IOT18B	I/O	0		Comp_of_IOT18A	NONE						H2	126	A9		J14	B8
IOT20A	I/O	0		True_of_IOT20B	NONE					86		124				
IOT20B	I/O	0		Comp_of_IOT20A	NONE					85						
IOT21A	I/O	0		True_of_IOT21B	NONE						M1				J15	A8
IOT21B	I/O	0		Comp_of_IOT21A	NONE						M2				K16	A9
IOT22A	I/O	0		True_of_IOT22B	NONE							123	C8		H11	D9
IOT22B	I/O	0		Comp_of_IOT22A	NONE							122	D8		J13	C9
IOT23A	I/O	0		True_of_IOT23B	NONE						C7			A7	K14	B9
IOT23B	I/O	0		Comp_of_IOT23A	NONE						L3			A6	K15	B10
IOT24A	I/O	0		True_of_IOT24B	NONE		43	B5		84		121	B9		J11	A10
IOT24B	I/O	0		Comp_of_IOT24A	NONE		42	C5		83		120	B10		L12	A11
IOT25A	I/O	0		True_of_IOT25B	NONE						J3			D8	L16	C10
IOT25B	I/O	0		Comp_of_IOT25A	NONE						K2			E8	L14	D10
IOT26A	I/O	0		True_of_IOT26B	NONE							119	D9		K13	B11
IOT26B	I/O	0		Comp_of_IOT26A	NONE							118	C9		K12	C11
IOT27A	I/O	0		True_of_IOT27B	NONE						J1			E7		
IOT27B	I/O	0		Comp_of_IOT27A	NONE						J2			D7		
IOT2A	I/O	0		True_of_IOT2B	NONE										L15	D4
IOT2B/MODE0	I/O	0	MODE0	Comp_of_IOT2A	NONE	GND ^[1]	GND ^[1]	A7	88	100	GND ^[1]	144	B1	GND ^[1]	M16	E5
IOT30A	I/O	0		True_of_IOT30B	NONE		41	B4		82		117	A11		K11	A12
IOT30B	I/O	0		Comp_of_IOT30A	NONE		40	C4	77	81		116	A10		L13	B12
IOT31A	I/O	0		True_of_IOT31B	NONE						H1			A10		E9
IOT31B	I/O	0		Comp_of_IOT31A	NONE				76		H3			A11		E10
IOT32A	I/O	0		True_of_IOT32B	NONE										M14	A13
IOT32B	I/O	0		Comp_of_IOT32A	NONE				75						M15	B13
IOT33A	I/O	0		True_of_IOT33B	NONE						F1	115	B11	B10	D14	C12
IOT33B	I/O	0		Comp_of_IOT33A	NONE				74		F3	114	B12	B9	E15	D11
IOT34A	I/O	0		True_of_IOT34B	NONE											
IOT34B	I/O	0		Comp_of_IOT34A	NONE											
IOT35A	I/O	0		True_of_IOT35B	NONE		39	A3	73	80	E3	113	D10	A8	N15	B14

Note!
^[1] The pin is internally grounded.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	QN32	QN48	CS72	QN88	LQ100	MG132X	LQ144	MG160	UG169	PG256	PG256M
IOT35B	I/O	0		Comp_of_IOT35A	NONE		38	A4	72	79	F2	112	C10	A9	P16	A15
IOT36A	I/O	0		True_of_IOT36B	NONE				71						N16	E12
IOT36B	I/O	0		Comp_of_IOT36A	NONE				70						N14	E11
IOT37A	I/O	0		True_of_IOT37B	NONE				69	78	E1	111	A12	C10	P15	D13
IOT37B	I/O	0		Comp_of_IOT37A	NONE				68	77	E2	110	A13	C9	R16	D12
IOT3A/MODE2	I/O	0	MODE2	True_of_IOT3B	NONE	GND ^[1]	GND ^[1]	GND ^[1]	GND ^[1]	GND ^[1]	GND ^[1]	GND ^[1]	A2	GND ^[1]	C15	A2
IOT3B/MODE1	I/O	0	MODE1	Comp_of_IOT3A	NONE	23	48	GND ^[1]	87	GND ^[1]	GND ^[1]	143	A3	GND ^[1]	B16	B1
IOT4A	I/O	0		True_of_IOT4B	NONE			A6	86	99		142	B3		D16	E6
IOT4B	I/O	0		Comp_of_IOT4A	NONE				85	98		141	B4		E14	F6
IOT5A	I/O	0		True_of_IOT5B	NONE				84					B3	C16	C4
IOT5B	I/O	0		Comp_of_IOT5A	NONE				83					B4	D15	D5
IOT6A	I/O	0		True_of_IOT6B	NONE				82	97		140	A4		E16	B3
IOT6B	I/O	0		Comp_of_IOT6A	NONE				81	96		139	A5		F15	C3
IOT7A	I/O	0		True_of_IOT7B	NONE							138	B5	E6	F13	B4
IOT7B	I/O	0		Comp_of_IOT7A	NONE							137	B6	D6	G12	C5
IOT8A	I/O	0		True_of_IOT8B	NONE						C2				F14	D6
IOT8B	I/O	0		Comp_of_IOT8A	NONE						D1				F16	C6
IOT9A	I/O	0		True_of_IOT9B	NONE		47		80	95		136	C5	A2	F12	A4
IOT9B	I/O	0		Comp_of_IOT9A	NONE		46			94		135	D5	B2	G13	A5
VCC	Power	N/A				2	12	H8	22	25	N1	36		H7		
VCC	Power	N/A				18	37	A2	66	75	P14	108		G8		
VCC	Power	N/A						A8	1	1	A14	1		F7		
VCC	Power	N/A							45	51	A1	73		G6		
VCC	Power	N/A											A1		A1	F10
VCC	Power	N/A											A14		A16	G11
VCC	Power	N/A											P1		G7	H8
VCC	Power	N/A											P14		G10	H10
VCC	Power	N/A													K10	J9
VCC	Power	N/A													K7	J7
VCC	Power	N/A													T1	K6
VCC	Power	N/A													T16	L7
VCCIO0	Power	N/A				19				88	D3	127		C6		
VCCIO0	Power	N/A						A5	67	76	G1	109		C8		
VCCIO0	Power	N/A									L1		C11	C7	J10	A14
VCCIO0	Power	N/A											C4		E13	A3
VCCIO0	Power	N/A													H10	F9
VCCIO0	Power	N/A													M13	F8
VCCIO0/VCCIO3	Power	N/A					1									
VCCIO1	Power	N/A				7		D1		54	P1	77		H11		
VCCIO1	Power	N/A							58	63	N11	91		J11		

Note!
^[1] The pin is internally grounded.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	QN32	QN48	CS72	QN88	LQ100	MG132X	LQ144	MG160	UG169	PG256	PG256M
VCCIO1	Power	N/A									M6		D12	G11	K8	C16
VCCIO1	Power	N/A											L12	F11	N5	J11
VCCIO1	Power	N/A													N12	P16
VCCIO1/VCCIO2	Power	N/A					25									
VCCIO2	Power	N/A				6								L8		
VCCIO2	Power	N/A						H5	23	26		37		L6		
VCCIO2	Power	N/A							44					L7		
VCCIO2	Power	N/A								38		55				
VCCIO2	Power	N/A									L12		M11		H7	L9
VCCIO2	Power	N/A									H14		M4		E4	L8
VCCIO2	Power	N/A									D14				J7	T14
VCCIO2	Power	N/A													M4	T3
VCCIO3	Power	N/A				31			12					G3		
VCCIO3	Power	N/A						E9		4		5		K3		
VCCIO3	Power	N/A								13		19		F2		
VCCIO3	Power	N/A											D3	J3	D12	C1
VCCIO3	Power	N/A											L3		D5	H6
VCCIO3	Power	N/A													G9	P1
VCCIO3/VCCX	Power	N/A									B10					
VCCIO3/VCCX	Power	N/A									A8					
VCCIO3/VCCX	Power	N/A									C5					
VCCX	Power	N/A				15	36		64	71		103		K4		
VCCX	Power	N/A						H2		21		31		D10		
VCCX	Power	N/A							78					K9		
VCCX	Power	N/A											C13	D3		J6
VCCX	Power	N/A											C2	D4		H11
VCCX	Power	N/A											M13		K9	
VCCX	Power	N/A											M2		G8	
VSS	Ground	N/A				3		H9	21	24		35				
VSS	Ground	N/A					2	A9	2	2		2				
VSS	Ground	N/A					26	H1	46	52		74				
VSS	Ground	N/A						A1	65	74		107				
VSS	Ground	N/A						D9								
VSS	Ground	N/A						E1								
VSS	Ground	N/A							24							
VSS	Ground	N/A							43							
VSS	Ground	N/A								37		53				
VSS	Ground	N/A								87		125				
VSS	Ground	N/A										17				
VSS	Ground	N/A										33				

Note!
^[1] The pin is internally grounded.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	QN32	QN48	CS72	QN88	LQ100	MG132X	LQ144	MG160	UG169	PG256	PG256M
VSS	Ground	N/A										89				
VSS	Ground	N/A										105				
VSS	Ground	N/A									D2		B13	D2	B15	G6
VSS	Ground	N/A									G2		B2	E2	B2	F7
VSS	Ground	N/A									L2		C12	N13	C14	H9
VSS	Ground	N/A									P5		C3	N1	C3	H7
VSS	Ground	N/A									P10		D11	M6	D13	J10
VSS	Ground	N/A									L13		D4	L9	D4	J8
VSS	Ground	N/A									A5		L11	J4	E12	L10
VSS	Ground	N/A									B11		L4	H12	E5	K11
VSS	Ground	N/A									D13		M12	G7	F11	A16
VSS	Ground	N/A									H13		M3	F3	F6	A1
VSS	Ground	N/A											N13	E11	H9	B15
VSS	Ground	N/A											N2	D5	H8	G7
VSS	Ground	N/A												C3	J8	B2
VSS	Ground	N/A												B8	J9	K10
VSS	Ground	N/A												A13	L11	K8
VSS	Ground	N/A												A1	L6	G10
VSS	Ground	N/A													M12	R15
VSS	Ground	N/A													M5	
VSS	Ground	N/A													N13	T16
VSS	Ground	N/A													N4	T1
VSS	Ground	N/A													P14	G9
VSS	Ground	N/A													P3	G8
VSS	Ground	N/A													R15	R2
VSS	Ground	N/A													R2	K9
VSS	Ground	N/A														K7

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	QN32	QN48	CS72	QN88	LQ100	MG132X	LQ144	MG160	UG169	PG256	PG256M
BANK3 True LVDS Pair																
IOL11A/GCLKT_6	I/O	3	GCLKT_6	True_of_IOL11B	TRUE		10	F9		17	A7	25	J2	G4	C8	J5
IOL11B/GCLKC_6	I/O	3	GCLKC_6	Comp_of_IOL11A	TRUE		11	F8		18	B7	26	J3	F4	A8	J4
IOL13A	I/O	3		True_of_IOL13B	TRUE			G9		19	B5	27	J1	J2	F8	H1
IOL13B	I/O	3		Comp_of_IOL13A	TRUE			G8		20	C6	28	K1	J1	D9	J1
IOL15A	I/O	3		True_of_IOL15B	TRUE				13		A3	29	K2	M2	B7	K1
IOL15B	I/O	3		Comp_of_IOL15A	TRUE				14		C4	30	L2	M1	C7	K2
IOL17A	I/O	3		True_of_IOL17B	TRUE				15		A2			L3	C4	K3
IOL17B	I/O	3		Comp_of_IOL17A	TRUE				16		B3			M3	B5	K4
IOL2A	I/O	3		True_of_IOL2B	TRUE						C12	3	C1	C2	B14	C2
IOL2B	I/O	3		Comp_of_IOL2A	TRUE						A12		D2	D1	A15	D3
IOL4A/LPLL_T_fb	I/O	3	LPLL_T_fb	True_of_IOL4B	TRUE			B9				7	E4	E4	B13	D2
IOL4B/LPLL_C_fb	I/O	3	LPLL_C_fb	Comp_of_IOL4A	TRUE			B8				8	F4	E3	A14	D1
IOL6A	I/O	3		True_of_IOL6B	TRUE			C9			A10	9	D1	E1	B11	F4
IOL6B	I/O	3		Comp_of_IOL6A	TRUE			C8			C11	10	E1	F1	A12	F3
IOL8A	I/O	3		True_of_IOL8B	TRUE						C9		H4		D10	F2
IOL8B	I/O	3		Comp_of_IOL8A	TRUE						A9		K4		E10	F1
BANK2 True LVDS Pair																
IOB12A	I/O	2		True_of_IOB12B	TRUE		15	D6	31	33	J12	48	L6	M7	F4	M7
IOB12B	I/O	2		Comp_of_IOB12A	TRUE		16	E6	32	34	J14	49	M6	N6	G6	M8
IOB14A	I/O	2		True_of_IOB14B	TRUE			H6		35		50	L7	N8	G5	T4
IOB14B	I/O	2		Comp_of_IOB14A	TRUE			G6		36		51	M7	N7	G4	T5
IOB16A	I/O	2		True_of_IOB16B	TRUE						G12	52	N6	K6	F5	T6
IOB16B	I/O	2		Comp_of_IOB16A	TRUE						G14	54	P6	J6	H6	T7
IOB18A	I/O	2		True_of_IOB18B	TRUE		17							K7	H4	N8
IOB18B	I/O	2		Comp_of_IOB18A	TRUE		18							J7	J6	P8
IOB20A/GCLKT_4	I/O	2	GCLKT_4	True_of_IOB20B	TRUE	4	19	G5	35	41		58	L8	M12	L2	T10
IOB20B/GCLKC_4	I/O	2	GCLKC_4	Comp_of_IOB20A	TRUE	5	20	F5	36	42		59	M8	M13	M1	R9
IOB22A	I/O	2		True_of_IOB22B	TRUE			D4			F13	62	N8		J2	T11
IOB22B	I/O	2		Comp_of_IOB22A	TRUE			D5			F14	63	P8		K1	R10
IOB24A	I/O	2		True_of_IOB24B	TRUE			E4		43	E13	64	N9		K3	M9
IOB24B	I/O	2		Comp_of_IOB24A	TRUE			E5		44	F12	65	P9		K2	M10
IOB26A	I/O	2		True_of_IOB26B	TRUE		21	H4		45	E12	66	L10	N9	L1	N10
IOB26B	I/O	2		Comp_of_IOB26A	TRUE		22	G4		46	E14	67	M10	N10	L3	P11
IOB2A	I/O	2		True_of_IOB2B	TRUE				17		N13			L4	A4	L3
IOB2B	I/O	2		Comp_of_IOB2A	TRUE				18		N14			L5	C5	M3
IOB30A	I/O	2		True_of_IOB30B	TRUE			F4	41	47	C14	70	P11		M3	N12

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	QN32	QN48	CS72	QN88	LQ100	MG132X	LQ144	MG160	UG169	PG256	PG256M
IOB30B	I/O	2		Comp_of_IOB30A	TRUE			F3	42	48	D12	71	N11		N1	P13
IOB32A	I/O	2		True_of_IOB32B	TRUE		23	H3		49	B14		P12	L11	R1	P15
IOB32B	I/O	2		Comp_of_IOB32A	TRUE		24	G3		50	C13		N12	M11	P2	R16
IOB34A	I/O	2		True_of_IOB34B	TRUE					55		75	M14	K8	T2	M13
IOB34B	I/O	2		Comp_of_IOB34A	TRUE					53		72	N14	J8	R3	L12
IOB36A	I/O	2		True_of_IOB36B	TRUE			G1				78	J13	L10	T3	N16
IOB36B	I/O	2		Comp_of_IOB36A	TRUE			G2				76	L13	M10	R4	N15
IOB4A	I/O	2		True_of_IOB4B	TRUE	32			19		M12			M5	A3	N1
IOB4B	I/O	2		Comp_of_IOB4A	TRUE	1			20		M14	32		M4	B4	N2
IOB6A	I/O	2		True_of_IOB6B	TRUE		13	H7	25	27	L14	38	N1		B1	P2
IOB6B	I/O	2		Comp_of_IOB6A	TRUE		14	G7	26	28	M13	39	P2		C2	N3
IOB8A	I/O	2		True_of_IOB8B	TRUE			F7	27	29	K13	42	L5	N5	E2	P4
IOB8B	I/O	2		Comp_of_IOB8A	TRUE			F6	28	30	K14	43	M5	N4	E3	N5
BANK1 True LVDS Pair																
IOR11A/GCLKT_3	I/O	1	GCLKT_3	True_of_IOR11B	TRUE	9	30	F1	52	57	M7	84	J14	G9	T7	H12
IOR11B/GCLKC_3	I/O	1	GCLKC_3	Comp_of_IOR11A	TRUE	8	29	F2	51	56	N8	83	K14	G10	R8	H13
IOR13A	I/O	1		True_of_IOR13B	TRUE						P9		E11	J9	P8	J13
IOR13B	I/O	1		Comp_of_IOR13A	TRUE						N9		F11	H10	T8	J14
IOR15A	I/O	1		True_of_IOR15B	TRUE						P8	82	J12	K12	M7	K15
IOR15B	I/O	1		Comp_of_IOR15A	TRUE						M8	81	H11	J12	N7	L15
IOR17A	I/O	1		True_of_IOR17B	TRUE		28		49			80	K12	K11	N6	L16
IOR17B	I/O	1		Comp_of_IOR17A	TRUE		27		48		M3	79	K11	L12	L7	M16
IOR2A	I/O	1		True_of_IOR2B	TRUE			B1						D12	T15	C13
IOR2B	I/O	1		Comp_of_IOR2A	TRUE			B2						D11	R14	C14
IOR4A/RPLL_T_fb	I/O	1	RPLL_T_fb	True_of_IOR4B	TRUE			C3				102	D14	B13	P12	E13
IOR4B/RPLL_C_fb	I/O	1	RPLL_C_fb	Comp_of_IOR4A	TRUE			B3				101	E14	A12	T13	D14
IOR6A	I/O	1		True_of_IOR6B	TRUE						M11	100	D13	B12	R13	E14
IOR6B	I/O	1		Comp_of_IOR6A	TRUE						P12	99	E13	B11	T14	F13
IOR8A	I/O	1		True_of_IOR8B	TRUE			C1			M9			F9	T11	D15
IOR8B	I/O	1		Comp_of_IOR8A	TRUE			C2			N10			F10	P11	E15

Note !			
VCCX should be greater than or equal to VCCIO.			
Recommended Operating Conditions of QN48 Package in GW1N-4			
Name	Description	Min.	Max.
VCC	LV: Core voltage	1.14V	1.26V
	UV: Core voltage	1.71V	3.6V
VCCIO0, VCCIO3	VCCIO0 and VCCIO3 are internally short-circuited.	LV: I/O Bank voltage	3.6V
		UV: I/O Bank voltage	1.14V
VCCIO1, VCCIO2	VCCIO0 and VCCIO2 are internally short-circuited.	LV: I/O Bank voltage	3.6V
		UV: I/O Bank voltage	1.14V
VCCX	Auxiliary voltage	2.375V	3.6V
Note !			
It is highly recommended that the epad connect to GND, but not a requirement.			
Recommended Operating Conditions of MG132X Package in GW1N-4			
Name	Description	Min.	Max.
VCC	LV: Core voltage	1.14V	1.26V
	UV: Core voltage	1.71V	3.6V
VCCIO0, VCCIO1, VCCIO2	LV: I/O Bank voltage	1.14V	3.6V
		UV: I/O Bank voltage	1.14V
VCCX/VCCIO3	VCCX and VCCIO3 are internally short-circuited.	2.375V	3.6V
Recommended Operating Conditions of QN32/QN88 Packages in GW1N-4			
Name	Description	Min.	Max.
VCC	LV: Core voltage	1.14V	1.26V
	UV: Core voltage	1.71V	3.6V
VCCIO0, VCCIO1 VCCIO2, VCCIO3	LV: I/O Bank voltage	1.14V	3.6V
	UV: I/O Bank voltage	1.14V	3.6V
VCCX	Auxiliary voltage	2.375V	3.6V
Note !			
It is highly recommended that the epad connect to GND, but not a requirement.			

Recommended Operating Conditions of CS72/LQ100/LQ144/MG160/UG169/PG256/PG256M Packages in GW1N-4			
Name	Description	Min.	Max.
VCC	LV: Core voltage	1.14V	1.26V
	UV: Core voltage	1.71V	3.6V
VCCIO0, VCCIO1 VCCIO2, VCCIO3	LV: I/O Bank voltage	1.14V	3.6V
	UV: I/O Bank voltage	1.14V	3.6V
VCCX	Auxiliary voltage	2.375V	3.6V