Date	Version	Description
09/28/2023	1.0E	Initial version published. UG324A package supported.
10/24/2023	1.0.1E	The Max. voltage value and the note of VCC_REG in Power sheet updated.
02/01/2024	1.0.2E	The info. of X16 removed. The configuration info. of MCKTEST pin removed. The I/O descriptions of Ready and Done pins in Pin Definitions sheet optimized. The note of SGCLKC_[x]/MGCLKC_[x]/SGCLKT_[x]/MGCLKT_[x] pins in Pin Definitions sheet added.
04/18/2024	1.0.3E	The description of CFGBVS pin in Pin Definitions sheet optimized. The Max. value of VCC voltage in Power sheet updated.
07/05/2024	1.0.4E	Power sheet optimized. The names and descriptions of voltage pins updated.
02/07/2025	1.0.5E	The note of MIPI voltage in Power sheet added.
03/07/2025	1.0.6E	The names of power supply pins updated. The information of VEFUSE voltage removed. The configuration function of ADCTN/ADCTP/ADCVN/ADCVP pins removed.

Pin Name	I/O	Description
User I/O		
IO[End][Row/Column Number][A/B]	I/O/LVDS	[End] indicates the pin location, including L(left), R(right), B(bottom), and T(top).
		[Row/Column Number] indicates the pin row/column number. If [End] is T(top) or B(bottom), the pin indicates the column number of the corresponding CFU. If [End] is L(left) or R(right), the pin indicates the row number of the corresponding CFU.
		[A/B] indicates differential signal pair information.
		LVDS indicates that the pin only supports LVDS output.
Multi-Function Pins		
IO[End][Row/Column Number][A/B]/MMM		/MMM represents one or more of the other functions in addition to being general purpose user I/O. When these functions are not in use, these pins can be used as user I/O.
D00	I/O	CPU Mode: Data input/output (bidirectional) pin D00
D01	I/O	CPU Mode: Data input/output (bidirectional) pin D01 MSPI Mode: In X1 mode, serial data input; In X2 and X4 modes, the input pin of parallel data bit 1 that connects to pin DQ1/Q/SO/IO1 of external Flash device
D02	I/O	CPU Mode: Data input/output (bidirectional) pin D02 MSPI Mode: In X4 mode, the input pin of parallel data bit 2 that connects to pin DQ2/W#/IO2 of external Flash device respectively
D03	I/O	CPU Mode: Data input/output (bidirectional) pin D03 MSPI Mode: In X4 mode, the input pin of parallel data bit 3 that connects to pin DQ3/HOLD#/IO3 of external Flash device respectively
D04~D07	I/O	CPU Mode: Data input/output port D04~D07
D08~D31	I	CPU Mode: Data input port D08~D31
ADCINCK0	I/O	ADC0 dedicated clock input pin
ADCINCK1	I/O	ADC1 dedicated clock input pin
CCLK	I/O	Configuration Clock Slave Mode: CCLK is input and need connect to external clock source Master Mode: CCLK is output
CFGBVS	I/O	Configuration Bank Voltage Selection Signal The bank where the configuration IO (JTAG, MSPI, etc.) is located refers to bank3, bank4, and bank10 When the VCCIO of the bank where the configuration IO is located is 2.5V and 3.3V, CFGBVS is connected to 1 When the VCCIO of the bank where the configuration IO is located is less than 1.8V, CFGBVS is connected to 0
CFGPU	I/O	selection signal pin that is internal weak pull-up during configuration
EMCCLK	I	External Input Clock Signal Master Mode: EMCCLK is used as the clock source of FPGA configuration logic and output CCLK Slave Mode: EMCCLK is not associated with slave mode

Pin Name	I/O	Description
MOSI	I/O	MSPI Mode: Serial instruction and address output, in X2 and X4 modes, the input pin of parallel data bit 0 that connects to DQ0/D/SI/IO0 pins of external Flash device
MCS_N	O	MSPI Mode: Enable signal MCS_N, active-low
CSI_B	I	CPU Mode: Chip select signal, active-low Master CPU Mode: The chip select signal can connect to external configuration controller and can be grounded directly or grounded in series with a 1KΩ resistor Slave CPU Mode: External configuration controller can select FPGA through controlling CSI_B signal In Master and Slave modes, CSI_B signal is sent from external controller; In other modes, CSI_B signal is not associated with external controller
DOUT_CSO_B	O	FPGA cascade configuration mode (Daisy Chain): Connect the next level device SERIAL mode: Output the configuration data of the next level device Master SPI mode: output the configuration data of the next level device CPU mode: output the chip select signal of the next level device
PUDC_B	I	Active-low, weak pull-up selection signal pin during configuration： Enable internal weak pull-up resistor during configuration after FPGA power up PUDC_B low: all GPIOs except PUDC_B weak pull-up PUDC_B high: all GPIOs are in high impedance PUDC_B are not allowed to be left floating during configuration
RDWR_B	I	CPU Mode: Data write/read controlling signal When RDWR is high, FPGA outputs data, while RDWR is low, external controller writes data into FPGA Master CPU Mode: Connect external controller RDWR signal; Connect directly or in series with resistor ⩽ 1KΩ to GND Slave CPU Mode: External controller RDWR signal In CPU mode, low 8-bit dedicated IO will be affected by RDWR status after wakeup; low 8-bit dedicated IO will not be affected by RDWR status if it is set as multiplexed IO
SI	I/O	SI in SSPI mode
SO	O	SO in SSPI mode
SSPI_CLK	I/O	SSPI/QSSPI Configuration Mode: Clock input pin
SSPI_CS_N	I/O	SSPI Mode: Enable signal SSPI_CS_N, active-low, and internal weak pull-up
SSPI_WPN	I/O	QSSPI Configuration Mode: Data input pin
SGCLKC_[x][2]	I	Differential input pin of SGCLKT_[x], C(Comp), [x] is clock number
SGCLKT_[x][2]	I	Dedicated clock input pin, drive the same clock region, T(True), [x] is clock number
MGCLKC_[x][2]	I	Differential input pin of MGCLKT/C_[x], C(Comp), [x] is clock number
MGCLKT_[x][2]	I	Dedicated clock input pin, drive multiple clock regions, T(True), [x] is clock number

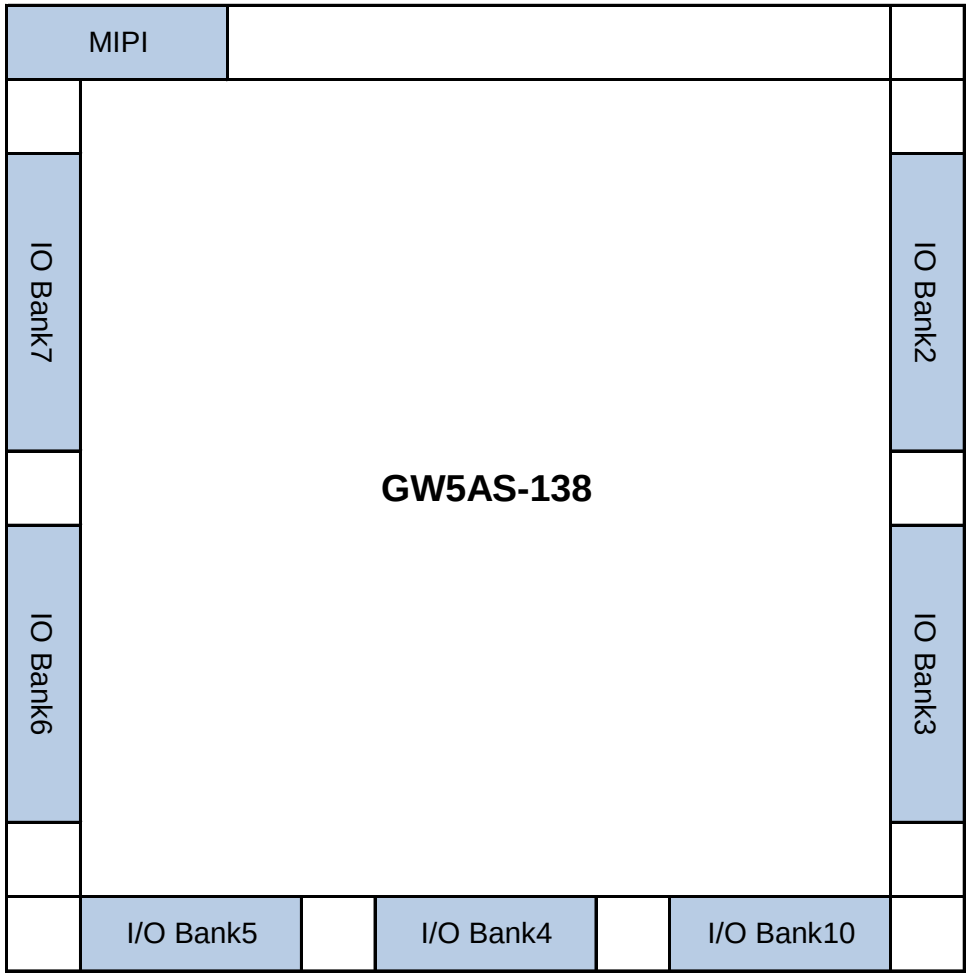
Pin Name	I/O	Description
DIN	I, internal weak pull-down	SERIAL Mode: Data input
TMS	I, internal weak pull-up	JTAG Mode: Serial mode input
TCK	I	JTAG Mode: Serial clock input
TDO	O	JTAG Mode: Serial data output
TDI	I, internal weak pull-up	JTAG mode: Serial data input
RECONFIG_N	I, internal weak pull-up	Global reset GowinCONFIG logic signal, active low
DONE[1]	O, internal weak pull-up	High, the programming configuration has been completed successfully; Low, the programming configuration has not been completed or failed.
	I, internal weak pull-up	When the DONE signal is low, delay the chip to activate. Activate the chip until the DONE signal is high.
READY[1]	O, internal weak pull-up	High, the device can be programmed and configured currently; Low, the device cannot be programmed and configured currently.
CLKHOLD_N	I, internal weak pull-down	In SSPI mode, active high In CPU mode, active low
LPLL_C_FB/RPLL_C_FB	I	Left/Right PLL feedback input pin, C(Comp)
LPLL_T_FB/RPLL_T_FB	I	Left/Right PLL feedback input pin, T(True)
LPLL_C_IN/RPLL_C_IN	I	Left/Right PLL clock input pin, C(Comp)
LPLL_T_IN/RPLL_T_IN	I	Left/Right PLL clock input pin, T(True)
MODE2	I, internal weak pull-down	GowinCONFIG mode selection pin If this pin is not bonded, it's internally grounded.
MODE1	I, internal weak pull-down	GowinCONFIG mode selection pin If this pin is not bonded, it's internally grounded.
MODE0	I, internal weak pull-down	GowinCONFIG mode selection pin If this pin is not bonded, it's internally grounded.
Other Pins		
ADCTN	DIO	SENSOR1/SENSOR2 differential analog signal input pin
ADCTP	DIO	SENSOR1/SENSOR2 differential analog signal input pin
ADCVN	DIO	SENSOR1/SENSOR2 differential analog signal input pin
ADCVP	DIO	SENSOR1/SENSOR2 differential analog signal input pin
M0_CKN	DIO	The clock channel differential input pin of MIPI_DPHY_RX M0
M0_CKP	DIO	The clock channel differential input pin of MIPI_DPHY_RX M0
M0_D0N	DIO	The data channel 0 differential input pin of MIPI_DPHY_RX M0

Pin Name	I/O	Description
M0_D0P	DIO	The data channel 0 differential input pin of MIPI_DPHY_RX M0
M0_D1N	DIO	The data channel 1 differential input pin of MIPI_DPHY_RX M0
M0_D1P	DIO	The data channel 1 differential input pin of MIPI_DPHY_RX M0
M0_D2N	DIO	The data channel 2 differential input pin of MIPI_DPHY_RX M0
M0_D2P	DIO	The data channel 2 differential input pin of MIPI_DPHY_RX M0
M0_D3N	DIO	The data channel 3 differential input pin of MIPI_DPHY_RX M0
M0_D3P	DIO	The data channel 3 differential input pin of MIPI_DPHY_RX M0
M1_CKN	DIO	The clock channel differential input pin of MIPI_DPHY_RX M1
M1_CKP	DIO	The clock channel differential input pin of MIPI_DPHY_RX M1
M1_D0N	DIO	The data channel 0 differential input pin of MIPI_DPHY_RX M1
M1_D0P	DIO	The data channel 0 differential input pin of MIPI_DPHY_RX M1
M1_D1N	DIO	The data channel 1 differential input pin of MIPI_DPHY_RX M1
M1_D1P	DIO	The data channel 1 differential input pin of MIPI_DPHY_RX M1
M1_D2N	DIO	The data channel 2 differential input pin of MIPI_DPHY_RX M1
M1_D2P	DIO	The data channel 2 differential input pin of MIPI_DPHY_RX M1
M1_D3N	DIO	The data channel 3 differential input pin of MIPI_DPHY_RX M1
M1_D3P	DIO	The data channel 3 differential input pin of MIPI_DPHY_RX M1
VSS	NA	Ground pin
VCC	NA	Core power supply pin
VCCIO#	NA	I/O power supply pin of I/O BANK#
VCCX	NA	Auxiliary power supply pin
VCCLDO	NA	Power supply pin of internal LDO module voltage that provides voltage for PLL and SRAM
VDDXM	NA	Auxiliary power supply pin of MIPI module

Note!

[1] The default state of READY/DONE is open-drain output, internal weak pull-up. DONE outputs 0 during configuration.

[2] The SGCLKC_[x] pin is equivalent to the MGCLKC_[x] pin; the SGCLKT_[x] pin is equivalent to the MGCLKT_[x] pin.



Note!

[1] Each Bank has independent reference voltage (VREF).

[2] You can choose to use the embedded VREF source of IOB (0.6V, 0.675, 0.75V, 0.9V), and VCCIO-based scaled voltages (33%, 43%, 50%,58%)).

[3] You can also select to use external VREF input (use any IO pins as external VREF input).

Name	Description	Min.	Max.
FPGA Logic			
V_{CC}	Core voltage	0.87V	1.03V
V_{CCIO}	I/O Bank voltage	1V	3.465V
V_{CCX}	Auxiliary voltage	1.71V	1.89V
V_{CCLDO}[1]	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	1.89V
MIPI[2]			
V_{DDAM}	Analog core power supply voltage	0.87V	1.03V
V_{DDXM}	Analog auxiliary power supply voltage	1.71V	1.89V
V_{DDDM}	Digital core power supply voltage	0.87V	1.03V

Note!

[1] The greater the V_{CCLDO} voltage, the higher the power consumption.

[2] For packages that do not support MIPI hard core, the MIPI voltage can be excluded.
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.

Pin Name	Function	BANK	DQS	Configuration Function	Differential Pair	LVDS	UG324A
IOB102A/MCS_N	I/O	4	DQ12	MCS_N	True_of_IOB102B	True	L13
IOB102B/D08/SO	I/O	4	DQ12	D08/SO	Comp_of_IOB102A	True	M13
IOB104A/PUDC_B	I/O	4	DQS12	PUDC_B	True_of_IOB104B	True	L15
IOB104B/EMCCLK	I/O	4	DQS12	EMCCLK	Comp_of_IOB104A	True	L16
IOB106A/CSI_B	I/O	4	DQ13	CSI_B	True_of_IOB106B	True	V15
IOB106B/D31	I/O	4	DQ13	D31	Comp_of_IOB106A	True	V16
IOB108A/D30	I/O	4	DQ13	D30	True_of_IOB108B	True	U17
IOB108B/D29	I/O	4	DQ13	D29	Comp_of_IOB108A	True	U18
IOB110A/RDWR	I/O	4	DQS13	RDWR	True_of_IOB110B	True	R16
IOB110B/DOUT_CSO_B	I/O	4	DQS13	DOUT_CSO_B	Comp_of_IOB110A	True	T16
IOB112A/D28	I/O	4	DQ13	D28	True_of_IOB112B	True	U16
IOB112B/D27	I/O	4	DQ13	D27	Comp_of_IOB112A	True	V17
IOB114A/SGCLKT_4/BPLL2_T_FB1/BPLL3_T_FB1	I/O	4	DQ13	SGCLKT_4/BPLL2_T_FB1/BPLL3_T_FB1	True_of_IOB114B	True	T14
IOB114B/SGCLKC_4/BPLL2_C_FB1/BPLL3_C_FB1	I/O	4	DQ13	SGCLKC_4/BPLL2_C_FB1/BPLL3_C_FB1	Comp_of_IOB114A	True	T15
IOB116A/MGCLKT_4/BPLL2_T_FB0/BPLL3_T_FB0	I/O	4	DQ13	MGCLKT_4/BPLL2_T_FB0/BPLL3_T_FB0	True_of_IOB116B	True	P15
IOB116B/MGCLKC_4/BPLL2_C_FB0/BPLL3_C_FB0	I/O	4	DQ13	MGCLKC_4/BPLL2_C_FB0/BPLL3_C_FB0	Comp_of_IOB116A	True	R15
IOB120A/SGCLKT_5/BPLL2_T_IN0/BPLL3_T_IN0	I/O	4	DQ14	SGCLKT_5/BPLL2_T_IN0/BPLL3_T_IN0	True_of_IOB120B	True	N15
IOB120B/SGCLKC_5/BPLL2_C_IN0/BPLL3_C_IN0	I/O	4	DQ14	SGCLKC_5/BPLL2_C_IN0/BPLL3_C_IN0	Comp_of_IOB120A	True	N16
IOB122A/MGCLKT_5/BPLL2_T_IN1/BPLL3_T_IN1	I/O	4	DQ14	MGCLKT_5/BPLL2_T_IN1/BPLL3_T_IN1	True_of_IOB122B	True	P17
IOB122B/MGCLKC_5/BPLL2_C_IN1/BPLL3_C_IN1	I/O	4	DQ14	MGCLKC_5/BPLL2_C_IN1/BPLL3_C_IN1	Comp_of_IOB122A	True	R17
IOB124A/D09	I/O	4	DQ14	D09	True_of_IOB124B	True	R18
IOB124B/D10	I/O	4	DQ14	D10	Comp_of_IOB124A	True	T18
IOB126A/D11	I/O	4	DQ14	D11	True_of_IOB126B	True	N14
IOB126B/D12	I/O	4	DQ14	D12	Comp_of_IOB126A	True	P14

Pin Name	Function	BANK	DQS	Configuration Function	Differential Pair	LVDS	UG324A
IOB129A/D14	I/O	4	DQ14	D14	True_of_IOB129B	True	M16
IOB129B/D15	I/O	4	DQ14	D15	Comp_of_IOB129A	True	M17
IOB131A/SSPI_CS_N	I/O	4	DQS14	SSPI_CS_N	True_of_IOB131B	True	N17
IOB131B/D13	I/O	4	DQS14	D13	Comp_of_IOB131A	True	P18
IOB133A/D26	I/O	4	DQ15	D26	True_of_IOB133B	True	T11
IOB133B/D25	I/O	4	DQ15	D25	Comp_of_IOB133A	True	U11
IOB135A/CLKHOLD_N	I/O	4	DQS15	CLKHOLD_N	True_of_IOB135B	True	V10
IOB135B/D22	I/O	4	DQS15	D22	Comp_of_IOB135A	True	V11
IOB138A/D24	I/O	4	DQ15	D24	True_of_IOB138B	True	U12
IOB138B/D23	I/O	4	DQ15	D23	Comp_of_IOB138A	True	V12
IOB140A/D21	I/O	4	DQ15	D21	True_of_IOB140B	True	U14
IOB140B/D20	I/O	4	DQ15	D20	Comp_of_IOB140A	True	V14
IOB142A/D19	I/O	4	DQ15	D19	True_of_IOB142B	True	T13
IOB142B/D18	I/O	4	DQ15	D18	Comp_of_IOB142A	True	U13
IOB144A/D17	I/O	4	DQ15	D17	True_of_IOB144B	True	T9
IOB144B/D16	I/O	4	DQ15	D16	Comp_of_IOB144A	True	T10
IOB146A	I/O	4	none			none	R10
IOB169A/TDO	I/O	10	none	TDO	True_of_IOB169B	True	E13
IOB169B/TMS	I/O	10	none	TMS	Comp_of_IOB169A	True	E12
IOB171A/READY	I/O	10	none	READY	True_of_IOB171B	True	P7
IOB171B/DONE	I/O	10	none	DONE	Comp_of_IOB171A	True	P10
IOB173A/TCK	I/O	10	none	TCK	True_of_IOB173B	True	E10
IOB173B/TDI	I/O	10	none	TDI	Comp_of_IOB173A	True	E11
IOB175A/MODE0	I/O	10	none	MODE0	True_of_IOB175B	True	P12
IOB175B/CCLK	I/O	10	none	CCLK	Comp_of_IOB175A	True	E9
IOB177A/MODE1	I/O	10	none	MODE1	True_of_IOB177B	True	P13
IOB177B/MODE2	I/O	10	none	MODE2	Comp_of_IOB177A	True	P11
IOB179A/CFGBVS	I/O	10	none	CFGBVS	True_of_IOB179B	True	P8
IOB179B/RECONFIG_N	I/O	10	none	RECONFIG_N	Comp_of_IOB179A	True	P9
IOB37A	I/O	5	none			none	K6
IOB38A	I/O	5	DQ8		True_of_IOB38B	True	L1
IOB38B	I/O	5	DQ8		Comp_of_IOB38A	True	M1

Pin Name	Function	BANK	DQS	Configuration Function	Differential Pair	LVDS	UG324A
IOB40A	I/O	5	DQ8		True_of_IOB40B	True	K3
IOB40B	I/O	5	DQ8		Comp_of_IOB40A	True	L3
IOB42A	I/O	5	DQS8		True_of_IOB42B	True	N2
IOB42B	I/O	5	DQS8		Comp_of_IOB42A	True	N1
IOB44A	I/O	5	DQ8		True_of_IOB44B	True	M3
IOB44B	I/O	5	DQ8		Comp_of_IOB44A	True	M2
IOB47A	I/O	5	DQ8		True_of_IOB47B	True	K5
IOB47B	I/O	5	DQ8		Comp_of_IOB47A	True	L4
IOB49A	I/O	5	DQ8		True_of_IOB49B	True	L6
IOB49B	I/O	5	DQ8		Comp_of_IOB49A	True	L5
IOB51A	I/O	5	DQ9		True_of_IOB51B	True	U1
IOB51B	I/O	5	DQ9		Comp_of_IOB51A	True	V1
IOB53A	I/O	5	DQ9		True_of_IOB53B	True	U4
IOB53B	I/O	5	DQ9		Comp_of_IOB53A	True	U3
IOB56A	I/O	5	DQS9		True_of_IOB56B	True	U2
IOB56B	I/O	5	DQS9		Comp_of_IOB56A	True	V2
IOB58A	I/O	5	DQ9		True_of_IOB58B	True	V5
IOB58B	I/O	5	DQ9		Comp_of_IOB58A	True	V4
IOB60A/SGCLKT_6/BPLL0_T_IN0/BPLL1_T_IN0	I/O	5	DQ9	SGCLKT_6/BPLL0_T_IN0/BPLL1_T_IN0	True_of_IOB60B	True	R3
IOB60B/SGCLKC_6/BPLL0_C_IN0/BPLL1_C_IN0	I/O	5	DQ9	SGCLKC_6/BPLL0_C_IN0/BPLL1_C_IN0	Comp_of_IOB60A	True	T3
IOB62A/MGCLKT_6/BPLL0_T_IN1/BPLL1_T_IN1	I/O	5	DQ9	MGCLKT_6/BPLL0_T_IN1/BPLL1_T_IN1	True_of_IOB62B	True	T5
IOB62B/MGCLKC_6/BPLL0_C_IN1/BPLL1_C_IN1	I/O	5	DQ9	MGCLKC_6/BPLL0_C_IN1/BPLL1_C_IN1	Comp_of_IOB62A	True	T4
IOB66A/MGCLKT_7/BPLL0_T_FB0/BPLL1_T_FB0	I/O	5	DQ10	MGCLKT_7/BPLL0_T_FB0/BPLL1_T_FB0	True_of_IOB66B	True	N5
IOB66B/MGCLKC_7/BPLL0_C_FB0/BPLL1_C_FB0	I/O	5	DQ10	MGCLKC_7/BPLL0_C_FB0/BPLL1_C_FB0	Comp_of_IOB66A	True	P5
IOB68A/SGCLKT_7/BPLL0_T_FB1/BPLL1_T_FB1	I/O	5	DQ10	SGCLKT_7/BPLL0_T_FB1/BPLL1_T_FB1	True_of_IOB68B	True	P4

Pin Name	Function	BANK	DQS	Configuration Function	Differential Pair	LVDS	UG324A
IOB68B/SGCLKC_7/BPLL0_C_FB1/BPLL1_C_FB1	I/O	5	DQ10	SGCLKC_7/BPLL0_C_FB1/BPLL1_C_FB1	Comp_of_IOB68A	True	P3
IOB70A	I/O	5	DQS10		True_of_IOB70B	True	P2
IOB70B	I/O	5	DQS10		Comp_of_IOB70A	True	R2
IOB72A	I/O	5	DQ10		True_of_IOB72B	True	M4
IOB72B	I/O	5	DQ10		Comp_of_IOB72A	True	N4
IOB74A	I/O	5	DQ10		True_of_IOB74B	True	R1
IOB74B	I/O	5	DQ10		Comp_of_IOB74A	True	T1
IOB76A	I/O	5	DQ10		True_of_IOB76B	True	M6
IOB76B	I/O	5	DQ10		Comp_of_IOB76A	True	N6
IOB78A	I/O	5	DQ11		True_of_IOB78B	True	U7
IOB78B	I/O	5	DQ11		Comp_of_IOB78A	True	U6
IOB80A	I/O	5	DQ11		True_of_IOB80B	True	V7
IOB80B	I/O	5	DQ11		Comp_of_IOB80A	True	V6
IOB83A	I/O	5	DQ11		True_of_IOB83B	True	R8
IOB83B	I/O	5	DQ11		Comp_of_IOB83A	True	T8
IOB85A	I/O	5	DQ11		True_of_IOB85B	True	R6
IOB85B	I/O	5	DQ11		Comp_of_IOB85A	True	R5
IOB87A	I/O	5	DQ11		True_of_IOB87B	True	R7
IOB87B	I/O	5	DQ11		Comp_of_IOB87A	True	T6
IOB89A	I/O	5	DQS11		True_of_IOB89B	True	U9
IOB89B	I/O	5	DQS11		Comp_of_IOB89A	True	V9
IOB91A	I/O	5	none			none	U8
IOB92A	I/O	4	none			none	R11
IOB93A/D00/MOSI	I/O	4	DQ12	D00/MOSI	True_of_IOB93B	True	K17
IOB93B/D01/DIN	I/O	4	DQ12	D01/DIN	Comp_of_IOB93A	True	K18
IOB95A/D02	I/O	4	DQ12	D02	True_of_IOB95B	True	L14
IOB95B/D03	I/O	4	DQ12	D03	Comp_of_IOB95A	True	M14
IOB97A/D04	I/O	4	DQ12	D04	True_of_IOB97B	True	L18
IOB97B/D05/SI	I/O	4	DQ12	D05/SI	Comp_of_IOB97A	True	M18
IOB99A/D06/SSPI_CLK	I/O	4	DQ12	D06/SSPI_CLK	True_of_IOB99B	True	R12
IOB99B/D07/SSPI_WPN	I/O	4	DQ12	D07/SSPI_WPN	Comp_of_IOB99A	True	R13

Pin Name	Function	BANK	DQS	Configuration Function	Differential Pair	LVDS	UG324A
IOL101A	I/O	6	DQ7		True_of_IOL101B	True	J3
IOL101B	I/O	6	DQ7		Comp_of_IOL101A	True	J2
IOL103A	I/O	6	DQ7		True_of_IOL103B	True	K2
IOL103B	I/O	6	DQ7		Comp_of_IOL103A	True	K1
IOL105A	I/O	6	DQ7		True_of_IOL105B	True	H6
IOL105B	I/O	6	DQ7		Comp_of_IOL105A	True	H5
IOL107A	I/O	6	DQ7		True_of_IOL107B	True	G6
IOL107B	I/O	6	DQ7		Comp_of_IOL107A	True	F6
IOL109A	I/O	6	none			none	J5
IOL22A	I/O	7	DQS1		True_of_IOL22B	True	D9
IOL24A/MGCLKT_11/LPLL0_T_IN1/LPLL1_T_IN1	I/O	7	DQ1	MGCLKT_11/LPLL0_T_IN1/LPLL1_T_IN1	True_of_IOL24B	True	B8
IOL24B/MGCLKC_11/LPLL0_C_IN1/LPLL1_C_IN1	I/O	7	DQ1	MGCLKC_11/LPLL0_C_IN1/LPLL1_C_IN1	Comp_of_IOL24A	True	A8
IOL26A/SGCLKT_11/LPLL0_T_IN0/LPLL1_T_IN0	I/O	7	DQ1	SGCLKT_11/LPLL0_T_IN0/LPLL1_T_IN0	True_of_IOL26B	True	C9
IOL26B/SGCLKC_11/LPLL0_C_IN0/LPLL1_C_IN0	I/O	7	DQ1	SGCLKC_11/LPLL0_C_IN0/LPLL1_C_IN0	Comp_of_IOL26A	True	B9
IOL29A/MGCLKT_10/LPLL0_T_FB1/LPLL1_T_FB1	I/O	7	DQ2	MGCLKT_10/LPLL0_T_FB1/LPLL1_T_FB1	True_of_IOL29B	True	C11
IOL29B/MGCLKC_10/LPLL0_C_FB1/LPLL1_C_FB1	I/O	7	DQ2	MGCLKC_10/LPLL0_C_FB1/LPLL1_C_FB1	Comp_of_IOL29A	True	C10
IOL31A/SGCLKT_10/LPLL0_T_FB0/LPLL1_T_FB0	I/O	7	DQ2	SGCLKT_10/LPLL0_T_FB0/LPLL1_T_FB0	True_of_IOL31B	True	A10
IOL31B/SGCLKC_10/LPLL0_C_FB0/LPLL1_C_FB0	I/O	7	DQ2	SGCLKC_10/LPLL0_C_FB0/LPLL1_C_FB0	Comp_of_IOL31A	True	A9
IOL35A	I/O	7	DQS2		True_of_IOL35B	True	D10
IOL56A	I/O	6	DQ4		True_of_IOL56B	True	C6
IOL56B	I/O	6	DQ4		Comp_of_IOL56A	True	C5
IOL58A	I/O	6	DQ4		True_of_IOL58B	True	B7
IOL58B	I/O	6	DQ4		Comp_of_IOL58A	True	B6
IOL60A	I/O	6	DQ4		True_of_IOL60B	True	E7

Pin Name	Function	BANK	DQS	Configuration Function	Differential Pair	LVDS	UG324A
IOL60B	I/O	6	DQ4		Comp_of_IOL60A	True	D7
IOL62A	I/O	6	DQ4		True_of_IOL62B	True	D8
IOL62B	I/O	6	DQ4		Comp_of_IOL62A	True	C7
IOL65A	I/O	6	DQS4		True_of_IOL65B	True	A6
IOL65B	I/O	6	DQS4		Comp_of_IOL65A	True	A5
IOL67A	I/O	6	DQ4		True_of_IOL67B	True	E6
IOL67B	I/O	6	DQ4		Comp_of_IOL67A	True	E5
IOL69A	I/O	6	DQS5		True_of_IOL69B	True	B1
IOL69B	I/O	6	DQS5		Comp_of_IOL69A	True	A1
IOL71A	I/O	6	DQ5		True_of_IOL71B	True	A4
IOL71B	I/O	6	DQ5		Comp_of_IOL71A	True	A3
IOL73A	I/O	6	none			none	F5
IOL74A	I/O	6	DQ5		True_of_IOL74B	True	C4
IOL74B	I/O	6	DQ5		Comp_of_IOL74A	True	B4
IOL76A	I/O	6	DQ5		True_of_IOL76B	True	B3
IOL76B	I/O	6	DQ5		Comp_of_IOL76A	True	B2
IOL78A/SGCLKT_8/LPLL2_T_IN0/LPLL3_T_IN0	I/O	6	DQ5	SGCLKT_8/LPLL2_T_IN0/LPLL3_T_IN0	True_of_IOL78B	True	D5
IOL78B/SGCLKC_8/LPLL2_C_IN0/LPLL3_C_IN0	I/O	6	DQ5	SGCLKC_8/LPLL2_C_IN0/LPLL3_C_IN0	Comp_of_IOL78A	True	D4
IOL80A/MGCLKT_8/LPLL2_T_IN1/LPLL3_T_IN1	I/O	6	DQ5	MGCLKT_8/LPLL2_T_IN1/LPLL3_T_IN1	True_of_IOL80B	True	E3
IOL80B/MGCLKC_8/LPLL2_C_IN1/LPLL3_C_IN1	I/O	6	DQ5	MGCLKC_8/LPLL2_C_IN1/LPLL3_C_IN1	Comp_of_IOL80A	True	D3
IOL83A/MGCLKT_9/LPLL2_T_FB1/LPLL3_T_FB1	I/O	6	DQ6	MGCLKT_9/LPLL2_T_FB1/LPLL3_T_FB1	True_of_IOL83B	True	F4
IOL83B/MGCLKC_9/LPLL2_C_FB1/LPLL3_C_FB1	I/O	6	DQ6	MGCLKC_9/LPLL2_C_FB1/LPLL3_C_FB1	Comp_of_IOL83A	True	F3
IOL85A/SGCLKT_9/LPLL2_T_FB0/LPLL3_T_FB0	I/O	6	DQ6	SGCLKT_9/LPLL2_T_FB0/LPLL3_T_FB0	True_of_IOL85B	True	E2
IOL85B/SGCLKC_9/LPLL2_C_FB0/LPLL3_C_FB0	I/O	6	DQ6	SGCLKC_9/LPLL2_C_FB0/LPLL3_C_FB0	Comp_of_IOL85A	True	D2

Pin Name	Function	BANK	DQS	Configuration Function	Differential Pair	LVDS	UG324A
IOL87A	I/O	6	DQ6		True_of_IOL87B	True	F1
IOL87B	I/O	6	DQ6		Comp_of_IOL87A	True	E1
IOL89A	I/O	6	DQ6		True_of_IOL89B	True	C2
IOL89B	I/O	6	DQ6		Comp_of_IOL89A	True	C1
IOL92A	I/O	6	DQ6		True_of_IOL92B	True	H1
IOL92B	I/O	6	DQ6		Comp_of_IOL92A	True	G1
IOL94A	I/O	6	DQS6		True_of_IOL94B	True	H2
IOL94B	I/O	6	DQS6		Comp_of_IOL94A	True	G2
IOL96A	I/O	6	DQS7		True_of_IOL96B	True	J4
IOL96B	I/O	6	DQS7		Comp_of_IOL96A	True	H4
IOL98A	I/O	6	DQ7		True_of_IOL98B	True	G4
IOL98B	I/O	6	DQ7		Comp_of_IOL98A	True	G3
IOR11A	I/O	2	DQ23		True_of_IOR11B	True	G18
IOR11B	I/O	2	DQ23		Comp_of_IOR11A	True	F18
IOR13A	I/O	2	DQ23		True_of_IOR13B	True	C16
IOR13B	I/O	2	DQ23		Comp_of_IOR13A	True	C17
IOR15A	I/O	2	DQ22		True_of_IOR15B	True	H17
IOR15B	I/O	2	DQ22		Comp_of_IOR15A	True	G17
IOR17A	I/O	2	DQ22		True_of_IOR17B	True	K13
IOR17B	I/O	2	DQ22		Comp_of_IOR17A	True	J13
IOR1A	I/O	2	none			none	K16
IOR20A	I/O	2	DQS22		True_of_IOR20B	True	H14
IOR20B	I/O	2	DQS22		Comp_of_IOR20A	True	G14
IOR22A	I/O	2	DQ22		True_of_IOR22B	True	E17
IOR22B	I/O	2	DQ22		Comp_of_IOR22A	True	D17
IOR24A/SGCLKT_1/RPLL0_T_FB0/RPLL1_T_FB0	I/O	2	DQ22	SGCLKT_1/RPLL0_T_FB0/RPLL1_T_FB0	True_of_IOR24B	True	F15
IOR24B/SGCLKC_1/RPLL0_C_FB0/RPLL1_C_FB0	I/O	2	DQ22	SGCLKC_1/RPLL0_C_FB0/RPLL1_C_FB0	Comp_of_IOR24A	True	F16
IOR26A/MGCLKT_1/RPLL0_T_FB1/RPLL1_T_FB1	I/O	2	DQ22	MGCLKT_1/RPLL0_T_FB1/RPLL1_T_FB1	True_of_IOR26B	True	H16

Pin Name	Function	BANK	DQS	Configuration Function	Differential Pair	LVDS	UG324A
IOR26B/MGCLKC_1/RPLL0_C_FB1/RPLL1_C_FB1	I/O	2	DQ22	MGCLKC_1/RPLL0_C_FB1/RPLL1_C_FB1	Comp_of_IOR26A	True	G16
IOR29A/SGCLKT_0/RPLL0_T_IN0/RPLL1_T_IN0	I/O	2	DQ21	SGCLKT_0/RPLL0_T_IN0/RPLL1_T_IN0	True_of_IOR29B	True	E15
IOR29B/SGCLKC_0/RPLL0_C_IN0/RPLL1_C_IN0	I/O	2	DQ21	SGCLKC_0/RPLL0_C_IN0/RPLL1_C_IN0	Comp_of_IOR29A	True	E16
IOR2A	I/O	2	DQ23		True_of_IOR2B	True	K15
IOR2B	I/O	2	DQ23		Comp_of_IOR2A	True	J15
IOR31A/MGCLKT_0/RPLL0_T_IN1/RPLL1_T_IN1	I/O	2	DQ21	MGCLKT_0/RPLL0_T_IN1/RPLL1_T_IN1	True_of_IOR31B	True	D15
IOR31B/MGCLKC_0/RPLL0_C_IN1/RPLL1_C_IN1	I/O	2	DQ21	MGCLKC_0/RPLL0_C_IN1/RPLL1_C_IN1	Comp_of_IOR31A	True	C15
IOR33A	I/O	2	DQ21		True_of_IOR33B	True	B18
IOR33B	I/O	2	DQ21		Comp_of_IOR33A	True	A18
IOR35A	I/O	2	DQS21		True_of_IOR35B	True	A13
IOR35B	I/O	2	DQS21		Comp_of_IOR35A	True	A14
IOR38A	I/O	2	DQ21		True_of_IOR38B	True	A15
IOR38B	I/O	2	DQ21		Comp_of_IOR38A	True	A16
IOR40A	I/O	2	DQ21		True_of_IOR40B	True	B16
IOR40B	I/O	2	DQ21		Comp_of_IOR40A	True	B17
IOR42A	I/O	2	DQ20		True_of_IOR42B	True	F13
IOR42B	I/O	2	DQ20		Comp_of_IOR42A	True	F14
IOR44A	I/O	2	DQS20		True_of_IOR44B	True	C12
IOR44B	I/O	2	DQS20		Comp_of_IOR44A	True	B12
IOR47A	I/O	2	DQ20		True_of_IOR47B	True	D12
IOR47B	I/O	2	DQ20		Comp_of_IOR47A	True	D13
IOR49A	I/O	2	DQ20		True_of_IOR49B	True	B11
IOR49B	I/O	2	DQ20		Comp_of_IOR49A	True	A11
IOR4A	I/O	2	DQ23		True_of_IOR4B	True	J14
IOR4B	I/O	2	DQ23		Comp_of_IOR4A	True	H15
IOR51A	I/O	2	DQ20		True_of_IOR51B	True	B13
IOR51B	I/O	2	DQ20		Comp_of_IOR51A	True	B14

Pin Name	Function	BANK	DQS	Configuration Function	Differential Pair	LVDS	UG324A
IOR53A	I/O	2	DQ20		True_of_IOR53B	True	D14
IOR53B	I/O	2	DQ20		Comp_of_IOR53A	True	C14
IOR55A	I/O	2	none			none	G13
IOR6A	I/O	2	DQ23		True_of_IOR6B	True	J17
IOR6B	I/O	2	DQ23		Comp_of_IOR6A	True	J18
IOR8A	I/O	2	DQS23		True_of_IOR8B	True	E18
IOR8B	I/O	2	DQS23		Comp_of_IOR8A	True	D18
ADCTN	DIO	ADC	none			none	L9
ADCTP	DIO	ADC	none			none	L10
ADCVN	DIO	ADC	none			none	K9
ADCVP	DIO	ADC	none			none	J10
NC	N/A	N/A					E8
NC	N/A	N/A					K10
NC	N/A	N/A					J9
NC	N/A	N/A					G11
NC	N/A	N/A					F10
VCC	Power	N/A					N7
VCC	Power	N/A					F8
VCC	Power	N/A					G7
VCC	Power	N/A					L7
VCC	Power	N/A					H8
VCC	Power	N/A					L11
VCC	Power	N/A					N9
VCC	Power	N/A					M10
VCC	Power	N/A					J11
VCC	Power	N/A					K8
VCC	Power	N/A					J7
VCC	Power	N/A					G9
VCC	Power	N/A					N11
VCC	Power	N/A					M8
VCCLDO	Power	N/A					H10
VCCIO10	Power	N/A					R9

Pin Name	Function	BANK	DQS	Configuration Function	Differential Pair	LVDS	UG324A
VCCX_VDDXM	Power	N/A					H12
VCCX_VDDXM	Power	N/A					K12
VCCX_VDDXM	Power	N/A					F12
VCCX_VDDXM	Power	N/A					M12
VCCIO2	Power	N/A					C13
VCCIO2	Power	N/A					H18
VCCIO2	Power	N/A					G15
VCCIO2	Power	N/A					K14
VCCIO2	Power	N/A					A17
VCCIO2	Power	N/A					D16
VCCIO4	Power	N/A					N13
VCCIO4	Power	N/A					U15
VCCIO4	Power	N/A					T12
VCCIO4	Power	N/A					P16
VCCIO4	Power	N/A					L17
VCCIO4	Power	N/A					V18
VCCIO5	Power	N/A					K4
VCCIO5	Power	N/A					V8
VCCIO5	Power	N/A					T2
VCCIO5	Power	N/A					N3
VCCIO5	Power	N/A					U5
VCCIO5	Power	N/A					P6
VCCIO6	Power	N/A					D6
VCCIO6	Power	N/A					F2
VCCIO6	Power	N/A					G5
VCCIO6	Power	N/A					A7
VCCIO6	Power	N/A					J1
VCCIO6	Power	N/A					C3
VCCIO7	Power	N/A					B10
VSS	Ground	N/A					A12
VSS	Ground	N/A					A2
VSS	Ground	N/A					B15

Pin Name	Function	BANK	DQS	Configuration Function	Differential Pair	LVDS	UG324A
VSS	Ground	N/A					B5
VSS	Ground	N/A					C18
VSS	Ground	N/A					C8
VSS	Ground	N/A					D11
VSS	Ground	N/A					D1
VSS	Ground	N/A					E14
VSS	Ground	N/A					E4
VSS	Ground	N/A					F17
VSS	Ground	N/A					F11
VSS	Ground	N/A					F9
VSS	Ground	N/A					F7
VSS	Ground	N/A					G12
VSS	Ground	N/A					G10
VSS	Ground	N/A					G8
VSS	Ground	N/A					H13
VSS	Ground	N/A					H11
VSS	Ground	N/A					H7
VSS	Ground	N/A					H3
VSS	Ground	N/A					J16
VSS	Ground	N/A					J12
VSS	Ground	N/A					J8
VSS	Ground	N/A					J6
VSS	Ground	N/A					K11
VSS	Ground	N/A					K7
VSS	Ground	N/A					L12
VSS	Ground	N/A					L8
VSS	Ground	N/A					L2
VSS	Ground	N/A					M15
VSS	Ground	N/A					M11
VSS	Ground	N/A					M9
VSS	Ground	N/A					M7
VSS	Ground	N/A					M5

Pin Name	Function	BANK	DQS	Configuration Function	Differential Pair	LVDS	UG324A
VSS	Ground	N/A					N18
VSS	Ground	N/A					N12
VSS	Ground	N/A					N10
VSS	Ground	N/A					N8
VSS	Ground	N/A					P1
VSS	Ground	N/A					R14
VSS	Ground	N/A					R4
VSS	Ground	N/A					T17
VSS	Ground	N/A					T7
VSS	Ground	N/A					U10
VSS	Ground	N/A					V13
VSS	Ground	N/A					H9
VSS	Ground	N/A					V3

Pin Name	Function	BANK	DQS	Configuration Function	Differential Pair	LVDS	UG324A
BANK10 True LVDS Pair							
IOB169A/TDO	I/O	10	none	TDO	True_of_IOB169B	True	E13
IOB169B/TMS	I/O	10	none	TMS	Comp_of_IOB169A	True	E12
IOB171A/READY	I/O	10	none	READY	True_of_IOB171B	True	P7
IOB171B/DONE	I/O	10	none	DONE	Comp_of_IOB171A	True	P10
IOB173A/TCK	I/O	10	none	TCK	True_of_IOB173B	True	E10
IOB173B/TDI	I/O	10	none	TDI	Comp_of_IOB173A	True	E11
IOB175A/MODE0	I/O	10	none	MODE0	True_of_IOB175B	True	P12
IOB175B/CCLK	I/O	10	none	CCLK	Comp_of_IOB175A	True	E9
IOB177A/MODE1	I/O	10	none	MODE1	True_of_IOB177B	True	P13
IOB177B/MODE2	I/O	10	none	MODE2	Comp_of_IOB177A	True	P11
IOB179A/CFGBVS	I/O	10	none	CFGBVS	True_of_IOB179B	True	P8
IOB179B/RECONFIG_N	I/O	10	none	RECONFIG_N	Comp_of_IOB179A	True	P9
BANK7 True LVDS Pair							
IOL22A	I/O	7	DQS1		True_of_IOL22B	True	D9
IOL24A/MGCLKT_11/LPLL0_T_IN1/LPLL1_T_IN1	I/O	7	DQ1	MGCLKT_11/LPLL0_T_IN1/LPLL1_T_IN1	True_of_IOL24B	True	B8
IOL24B/MGCLKC_11/LPLL0_C_IN1/LPLL1_C_IN1	I/O	7	DQ1	MGCLKC_11/LPLL0_C_IN1/LPLL1_C_IN1	Comp_of_IOL24A	True	A8
IOL26A/SGCLKT_11/LPLL0_T_IN0/LPLL1_T_IN0	I/O	7	DQ1	SGCLKT_11/LPLL0_T_IN0/LPLL1_T_IN0	True_of_IOL26B	True	C9
IOL26B/SGCLKC_11/LPLL0_C_IN0/LPLL1_C_IN0	I/O	7	DQ1	SGCLKC_11/LPLL0_C_IN0/LPLL1_C_IN0	Comp_of_IOL26A	True	B9
IOL29A/MGCLKT_10/LPLL0_T_FB1/LPLL1_T_FB1	I/O	7	DQ2	MGCLKT_10/LPLL0_T_FB1/LPLL1_T_FB1	True_of_IOL29B	True	C11
IOL29B/MGCLKC_10/LPLL0_C_FB1/LPLL1_C_FB1	I/O	7	DQ2	MGCLKC_10/LPLL0_C_FB1/LPLL1_C_FB1	Comp_of_IOL29A	True	C10
IOL31A/SGCLKT_10/LPLL0_T_FB0/LPLL1_T_FB0	I/O	7	DQ2	SGCLKT_10/LPLL0_T_FB0/LPLL1_T_FB0	True_of_IOL31B	True	A10
IOL31B/SGCLKC_10/LPLL0_C_FB0/LPLL1_C_FB0	I/O	7	DQ2	SGCLKC_10/LPLL0_C_FB0/LPLL1_C_FB0	Comp_of_IOL31A	True	A9
IOL35A	I/O	7	DQS2		True_of_IOL35B	True	D10

Pin Name	Function	BANK	DQS	Configuration Function	Differential Pair	LVDS	UG324A
BANK6 True LVDS Pair							
IOL101A	I/O	6	DQ7		True_of_IOL101B	True	J3
IOL101B	I/O	6	DQ7		Comp_of_IOL101A	True	J2
IOL103A	I/O	6	DQ7		True_of_IOL103B	True	K2
IOL103B	I/O	6	DQ7		Comp_of_IOL103A	True	K1
IOL105A	I/O	6	DQ7		True_of_IOL105B	True	H6
IOL105B	I/O	6	DQ7		Comp_of_IOL105A	True	H5
IOL107A	I/O	6	DQ7		True_of_IOL107B	True	G6
IOL107B	I/O	6	DQ7		Comp_of_IOL107A	True	F6
IOL56A	I/O	6	DQ4		True_of_IOL56B	True	C6
IOL56B	I/O	6	DQ4		Comp_of_IOL56A	True	C5
IOL58A	I/O	6	DQ4		True_of_IOL58B	True	B7
IOL58B	I/O	6	DQ4		Comp_of_IOL58A	True	B6
IOL60A	I/O	6	DQ4		True_of_IOL60B	True	E7
IOL60B	I/O	6	DQ4		Comp_of_IOL60A	True	D7
IOL62A	I/O	6	DQ4		True_of_IOL62B	True	D8
IOL62B	I/O	6	DQ4		Comp_of_IOL62A	True	C7
IOL65A	I/O	6	DQS4		True_of_IOL65B	True	A6
IOL65B	I/O	6	DQS4		Comp_of_IOL65A	True	A5
IOL67A	I/O	6	DQ4		True_of_IOL67B	True	E6
IOL67B	I/O	6	DQ4		Comp_of_IOL67A	True	E5
IOL69A	I/O	6	DQS5		True_of_IOL69B	True	B1
IOL69B	I/O	6	DQS5		Comp_of_IOL69A	True	A1
IOL71A	I/O	6	DQ5		True_of_IOL71B	True	A4
IOL71B	I/O	6	DQ5		Comp_of_IOL71A	True	A3
IOL74A	I/O	6	DQ5		True_of_IOL74B	True	C4
IOL74B	I/O	6	DQ5		Comp_of_IOL74A	True	B4
IOL76A	I/O	6	DQ5		True_of_IOL76B	True	B3
IOL76B	I/O	6	DQ5		Comp_of_IOL76A	True	B2
IOL78A/SGCLKT_8/LPLL2_T_IN0/LPLL3_T_IN0	I/O	6	DQ5	SGCLKT_8/LPLL2_T_IN0/LPLL3_T_IN0	True_of_IOL78B	True	D5
IOL78B/SGCLKC_8/LPLL2_C_IN0/LPLL3_C_IN0	I/O	6	DQ5	SGCLKC_8/LPLL2_C_IN0/LPLL3_C_IN0	Comp_of_IOL78A	True	D4

Pin Name	Function	BANK	DQS	Configuration Function	Differential Pair	LVDS	UG324A
IOL80A/MGCLKT_8/LPLL2_T_IN1/LPLL3_T_IN1	I/O	6	DQ5	MGCLKT_8/LPLL2_T_IN1/LPLL3_T_IN1	True_of_IOL80B	True	E3
IOL80B/MGCLKC_8/LPLL2_C_IN1/LPLL3_C_IN1	I/O	6	DQ5	MGCLKC_8/LPLL2_C_IN1/LPLL3_C_IN1	Comp_of_IOL80A	True	D3
IOL83A/MGCLKT_9/LPLL2_T_FB1/LPLL3_T_FB1	I/O	6	DQ6	MGCLKT_9/LPLL2_T_FB1/LPLL3_T_FB1	True_of_IOL83B	True	F4
IOL83B/MGCLKC_9/LPLL2_C_FB1/LPLL3_C_FB1	I/O	6	DQ6	MGCLKC_9/LPLL2_C_FB1/LPLL3_C_FB1	Comp_of_IOL83A	True	F3
IOL85A/SGCLKT_9/LPLL2_T_FB0/LPLL3_T_FB0	I/O	6	DQ6	SGCLKT_9/LPLL2_T_FB0/LPLL3_T_FB0	True_of_IOL85B	True	E2
IOL85B/SGCLKC_9/LPLL2_C_FB0/LPLL3_C_FB0	I/O	6	DQ6	SGCLKC_9/LPLL2_C_FB0/LPLL3_C_FB0	Comp_of_IOL85A	True	D2
IOL87A	I/O	6	DQ6		True_of_IOL87B	True	F1
IOL87B	I/O	6	DQ6		Comp_of_IOL87A	True	E1
IOL89A	I/O	6	DQ6		True_of_IOL89B	True	C2
IOL89B	I/O	6	DQ6		Comp_of_IOL89A	True	C1
IOL92A	I/O	6	DQ6		True_of_IOL92B	True	H1
IOL92B	I/O	6	DQ6		Comp_of_IOL92A	True	G1
IOL94A	I/O	6	DQS6		True_of_IOL94B	True	H2
IOL94B	I/O	6	DQS6		Comp_of_IOL94A	True	G2
IOL96A	I/O	6	DQS7		True_of_IOL96B	True	J4
IOL96B	I/O	6	DQS7		Comp_of_IOL96A	True	H4
IOL98A	I/O	6	DQ7		True_of_IOL98B	True	G4
IOL98B	I/O	6	DQ7		Comp_of_IOL98A	True	G3
BANK5 True LVDS Pair							
IOB38A	I/O	5	DQ8		True_of_IOB38B	True	L1
IOB38B	I/O	5	DQ8		Comp_of_IOB38A	True	M1
IOB40A	I/O	5	DQ8		True_of_IOB40B	True	K3
IOB40B	I/O	5	DQ8		Comp_of_IOB40A	True	L3
IOB42A	I/O	5	DQS8		True_of_IOB42B	True	N2
IOB42B	I/O	5	DQS8		Comp_of_IOB42A	True	N1
IOB44A	I/O	5	DQ8		True_of_IOB44B	True	M3
IOB44B	I/O	5	DQ8		Comp_of_IOB44A	True	M2

Pin Name	Function	BANK	DQS	Configuration Function	Differential Pair	LVDS	UG324A
IOB47A	I/O	5	DQ8		True_of_IOB47B	True	K5
IOB47B	I/O	5	DQ8		Comp_of_IOB47A	True	L4
IOB49A	I/O	5	DQ8		True_of_IOB49B	True	L6
IOB49B	I/O	5	DQ8		Comp_of_IOB49A	True	L5
IOB51A	I/O	5	DQ9		True_of_IOB51B	True	U1
IOB51B	I/O	5	DQ9		Comp_of_IOB51A	True	V1
IOB53A	I/O	5	DQ9		True_of_IOB53B	True	U4
IOB53B	I/O	5	DQ9		Comp_of_IOB53A	True	U3
IOB56A	I/O	5	DQS9		True_of_IOB56B	True	U2
IOB56B	I/O	5	DQS9		Comp_of_IOB56A	True	V2
IOB58A	I/O	5	DQ9		True_of_IOB58B	True	V5
IOB58B	I/O	5	DQ9		Comp_of_IOB58A	True	V4
IOB60A/SGCLKT_6/BPLL0_T_IN0/BPLL1_T_IN0	I/O	5	DQ9	SGCLKT_6/BPLL0_T_IN0/BPLL1_T_IN0	True_of_IOB60B	True	R3
IOB60B/SGCLKC_6/BPLL0_C_IN0/BPLL1_C_IN0	I/O	5	DQ9	SGCLKC_6/BPLL0_C_IN0/BPLL1_C_IN0	Comp_of_IOB60A	True	T3
IOB62A/MGCLKT_6/BPLL0_T_IN1/BPLL1_T_IN1	I/O	5	DQ9	MGCLKT_6/BPLL0_T_IN1/BPLL1_T_IN1	True_of_IOB62B	True	T5
IOB62B/MGCLKC_6/BPLL0_C_IN1/BPLL1_C_IN1	I/O	5	DQ9	MGCLKC_6/BPLL0_C_IN1/BPLL1_C_IN1	Comp_of_IOB62A	True	T4
IOB66A/MGCLKT_7/BPLL0_T_FB0/BPLL1_T_FB0	I/O	5	DQ10	MGCLKT_7/BPLL0_T_FB0/BPLL1_T_FB0	True_of_IOB66B	True	N5
IOB66B/MGCLKC_7/BPLL0_C_FB0/BPLL1_C_FB0	I/O	5	DQ10	MGCLKC_7/BPLL0_C_FB0/BPLL1_C_FB0	Comp_of_IOB66A	True	P5
IOB68A/SGCLKT_7/BPLL0_T_FB1/BPLL1_T_FB1	I/O	5	DQ10	SGCLKT_7/BPLL0_T_FB1/BPLL1_T_FB1	True_of_IOB68B	True	P4
IOB68B/SGCLKC_7/BPLL0_C_FB1/BPLL1_C_FB1	I/O	5	DQ10	SGCLKC_7/BPLL0_C_FB1/BPLL1_C_FB1	Comp_of_IOB68A	True	P3
IOB70A	I/O	5	DQS10		True_of_IOB70B	True	P2
IOB70B	I/O	5	DQS10		Comp_of_IOB70A	True	R2
IOB72A	I/O	5	DQ10		True_of_IOB72B	True	M4
IOB72B	I/O	5	DQ10		Comp_of_IOB72A	True	N4
IOB74A	I/O	5	DQ10		True_of_IOB74B	True	R1

Pin Name	Function	BANK	DQS	Configuration Function	Differential Pair	LVDS	UG324A
IOB74B	I/O	5	DQ10		Comp_of_IOB74A	True	T1
IOB76A	I/O	5	DQ10		True_of_IOB76B	True	M6
IOB76B	I/O	5	DQ10		Comp_of_IOB76A	True	N6
IOB78A	I/O	5	DQ11		True_of_IOB78B	True	U7
IOB78B	I/O	5	DQ11		Comp_of_IOB78A	True	U6
IOB80A	I/O	5	DQ11		True_of_IOB80B	True	V7
IOB80B	I/O	5	DQ11		Comp_of_IOB80A	True	V6
IOB83A	I/O	5	DQ11		True_of_IOB83B	True	R8
IOB83B	I/O	5	DQ11		Comp_of_IOB83A	True	T8
IOB85A	I/O	5	DQ11		True_of_IOB85B	True	R6
IOB85B	I/O	5	DQ11		Comp_of_IOB85A	True	R5
IOB87A	I/O	5	DQ11		True_of_IOB87B	True	R7
IOB87B	I/O	5	DQ11		Comp_of_IOB87A	True	T6
IOB89A	I/O	5	DQS11		True_of_IOB89B	True	U9
IOB89B	I/O	5	DQS11		Comp_of_IOB89A	True	V9
BANK4 True LVDS Pair							
IOB102A/MCS_N	I/O	4	DQ12	MCS_N	True_of_IOB102B	True	L13
IOB102B/D08/SO	I/O	4	DQ12	D08/SO	Comp_of_IOB102A	True	M13
IOB104A/PUDC_B	I/O	4	DQS12	PUDC_B	True_of_IOB104B	True	L15
IOB104B/EMCCLK	I/O	4	DQS12	EMCCLK	Comp_of_IOB104A	True	L16
IOB106A/CSI_B	I/O	4	DQ13	CSI_B	True_of_IOB106B	True	V15
IOB106B/D31	I/O	4	DQ13	D31	Comp_of_IOB106A	True	V16
IOB108A/D30	I/O	4	DQ13	D30	True_of_IOB108B	True	U17
IOB108B/D29	I/O	4	DQ13	D29	Comp_of_IOB108A	True	U18
IOB110A/RDWR	I/O	4	DQS13	RDWR	True_of_IOB110B	True	R16
IOB110B/DOUT_CSO_B	I/O	4	DQS13	DOUT_CSO_B	Comp_of_IOB110A	True	T16
IOB112A/D28	I/O	4	DQ13	D28	True_of_IOB112B	True	U16
IOB112B/D27	I/O	4	DQ13	D27	Comp_of_IOB112A	True	V17
IOB114A/SGCLKT_4/BPLL2_T_FB1/BPLL3_T_FB1	I/O	4	DQ13	SGCLKT_4/BPLL2_T_FB1/BPLL3_T_FB1	True_of_IOB114B	True	T14
IOB114B/SGCLKC_4/BPLL2_C_FB1/BPLL3_C_FB1	I/O	4	DQ13	SGCLKC_4/BPLL2_C_FB1/BPLL3_C_FB1	Comp_of_IOB114A	True	T15

Pin Name	Function	BANK	DQS	Configuration Function	Differential Pair	LVDS	UG324A
IOB116A/MGCLKT_4/BPLL2_T_FB0/BPLL3_T_FB0	I/O	4	DQ13	MGCLKT_4/BPLL2_T_FB0/BPLL3_T_FB0	True_of_IOB116B	True	P15
IOB116B/MGCLKC_4/BPLL2_C_FB0/BPLL3_C_FB0	I/O	4	DQ13	MGCLKC_4/BPLL2_C_FB0/BPLL3_C_FB0	Comp_of_IOB116A	True	R15
IOB120A/SGCLKT_5/BPLL2_T_IN0/BPLL3_T_IN0	I/O	4	DQ14	SGCLKT_5/BPLL2_T_IN0/BPLL3_T_IN0	True_of_IOB120B	True	N15
IOB120B/SGCLKC_5/BPLL2_C_IN0/BPLL3_C_IN0	I/O	4	DQ14	SGCLKC_5/BPLL2_C_IN0/BPLL3_C_IN0	Comp_of_IOB120A	True	N16
IOB122A/MGCLKT_5/BPLL2_T_IN1/BPLL3_T_IN1	I/O	4	DQ14	MGCLKT_5/BPLL2_T_IN1/BPLL3_T_IN1	True_of_IOB122B	True	P17
IOB122B/MGCLKC_5/BPLL2_C_IN1/BPLL3_C_IN1	I/O	4	DQ14	MGCLKC_5/BPLL2_C_IN1/BPLL3_C_IN1	Comp_of_IOB122A	True	R17
IOB124A/D09	I/O	4	DQ14	D09	True_of_IOB124B	True	R18
IOB124B/D10	I/O	4	DQ14	D10	Comp_of_IOB124A	True	T18
IOB126A/D11	I/O	4	DQ14	D11	True_of_IOB126B	True	N14
IOB126B/D12	I/O	4	DQ14	D12	Comp_of_IOB126A	True	P14
IOB129A/D14	I/O	4	DQ14	D14	True_of_IOB129B	True	M16
IOB129B/D15	I/O	4	DQ14	D15	Comp_of_IOB129A	True	M17
IOB131A/SSPI_CS_N	I/O	4	DQS14	SSPI_CS_N	True_of_IOB131B	True	N17
IOB131B/D13	I/O	4	DQS14	D13	Comp_of_IOB131A	True	P18
IOB133A/D26	I/O	4	DQ15	D26	True_of_IOB133B	True	T11
IOB133B/D25	I/O	4	DQ15	D25	Comp_of_IOB133A	True	U11
IOB135A/CLKHOLD_N	I/O	4	DQS15	CLKHOLD_N	True_of_IOB135B	True	V10
IOB135B/D22	I/O	4	DQS15	D22	Comp_of_IOB135A	True	V11
IOB138A/D24	I/O	4	DQ15	D24	True_of_IOB138B	True	U12
IOB138B/D23	I/O	4	DQ15	D23	Comp_of_IOB138A	True	V12
IOB140A/D21	I/O	4	DQ15	D21	True_of_IOB140B	True	U14
IOB140B/D20	I/O	4	DQ15	D20	Comp_of_IOB140A	True	V14
IOB142A/D19	I/O	4	DQ15	D19	True_of_IOB142B	True	T13
IOB142B/D18	I/O	4	DQ15	D18	Comp_of_IOB142A	True	U13
IOB144A/D17	I/O	4	DQ15	D17	True_of_IOB144B	True	T9
IOB144B/D16	I/O	4	DQ15	D16	Comp_of_IOB144A	True	T10
IOB93A/D00/MOSI	I/O	4	DQ12	D00/MOSI	True_of_IOB93B	True	K17

Pin Name	Function	BANK	DQS	Configuration Function	Differential Pair	LVDS	UG324A
IOB93B/D01/DIN	I/O	4	DQ12	D01/DIN	Comp_of_IOB93A	True	K18
IOB95A/D02	I/O	4	DQ12	D02	True_of_IOB95B	True	L14
IOB95B/D03	I/O	4	DQ12	D03	Comp_of_IOB95A	True	M14
IOB97A/D04	I/O	4	DQ12	D04	True_of_IOB97B	True	L18
IOB97B/D05/SI	I/O	4	DQ12	D05/SI	Comp_of_IOB97A	True	M18
IOB99A/D06/SSPI_CLK	I/O	4	DQ12	D06/SSPI_CLK	True_of_IOB99B	True	R12
IOB99B/D07/SSPI_WPN	I/O	4	DQ12	D07/SSPI_WPN	Comp_of_IOB99A	True	R13
BANK2 True LVDS Pair							
IOR11A	I/O	2	DQ23		True_of_IOR11B	True	G18
IOR11B	I/O	2	DQ23		Comp_of_IOR11A	True	F18
IOR13A	I/O	2	DQ23		True_of_IOR13B	True	C16
IOR13B	I/O	2	DQ23		Comp_of_IOR13A	True	C17
IOR15A	I/O	2	DQ22		True_of_IOR15B	True	H17
IOR15B	I/O	2	DQ22		Comp_of_IOR15A	True	G17
IOR17A	I/O	2	DQ22		True_of_IOR17B	True	K13
IOR17B	I/O	2	DQ22		Comp_of_IOR17A	True	J13
IOR20A	I/O	2	DQS22		True_of_IOR20B	True	H14
IOR20B	I/O	2	DQS22		Comp_of_IOR20A	True	G14
IOR22A	I/O	2	DQ22		True_of_IOR22B	True	E17
IOR22B	I/O	2	DQ22		Comp_of_IOR22A	True	D17
IOR24A/SGCLKT_1/RPLL0_T_FB0/RPLL1_T_FB0	I/O	2	DQ22	SGCLKT_1/RPLL0_T_FB0/RPLL1_T_FB0	True_of_IOR24B	True	F15
IOR24B/SGCLKC_1/RPLL0_C_FB0/RPLL1_C_FB0	I/O	2	DQ22	SGCLKC_1/RPLL0_C_FB0/RPLL1_C_FB0	Comp_of_IOR24A	True	F16
IOR26A/MGCLKT_1/RPLL0_T_FB1/RPLL1_T_FB1	I/O	2	DQ22	MGCLKT_1/RPLL0_T_FB1/RPLL1_T_FB1	True_of_IOR26B	True	H16
IOR26B/MGCLKC_1/RPLL0_C_FB1/RPLL1_C_FB1	I/O	2	DQ22	MGCLKC_1/RPLL0_C_FB1/RPLL1_C_FB1	Comp_of_IOR26A	True	G16
IOR29A/SGCLKT_0/RPLL0_T_IN0/RPLL1_T_IN0	I/O	2	DQ21	SGCLKT_0/RPLL0_T_IN0/RPLL1_T_IN0	True_of_IOR29B	True	E15
IOR29B/SGCLKC_0/RPLL0_C_IN0/RPLL1_C_IN0	I/O	2	DQ21	SGCLKC_0/RPLL0_C_IN0/RPLL1_C_IN0	Comp_of_IOR29A	True	E16
IOR2A	I/O	2	DQ23		True_of_IOR2B	True	K15

Pin Name	Function	BANK	DQS	Configuration Function	Differential Pair	LVDS	UG324A
IOR2B	I/O	2	DQ23		Comp_of_IOR2A	True	J15
IOR31A/MGCLKT_0/RPLL0_T_IN1/RPLL1_T_IN1	I/O	2	DQ21	MGCLKT_0/RPLL0_T_IN1/RPLL1_T_IN1	True_of_IOR31B	True	D15
IOR31B/MGCLKC_0/RPLL0_C_IN1/RPLL1_C_IN1	I/O	2	DQ21	MGCLKC_0/RPLL0_C_IN1/RPLL1_C_IN1	Comp_of_IOR31A	True	C15
IOR33A	I/O	2	DQ21		True_of_IOR33B	True	B18
IOR33B	I/O	2	DQ21		Comp_of_IOR33A	True	A18
IOR35A	I/O	2	DQS21		True_of_IOR35B	True	A13
IOR35B	I/O	2	DQS21		Comp_of_IOR35A	True	A14
IOR38A	I/O	2	DQ21		True_of_IOR38B	True	A15
IOR38B	I/O	2	DQ21		Comp_of_IOR38A	True	A16
IOR40A	I/O	2	DQ21		True_of_IOR40B	True	B16
IOR40B	I/O	2	DQ21		Comp_of_IOR40A	True	B17
IOR42A	I/O	2	DQ20		True_of_IOR42B	True	F13
IOR42B	I/O	2	DQ20		Comp_of_IOR42A	True	F14
IOR44A	I/O	2	DQS20		True_of_IOR44B	True	C12
IOR44B	I/O	2	DQS20		Comp_of_IOR44A	True	B12
IOR47A	I/O	2	DQ20		True_of_IOR47B	True	D12
IOR47B	I/O	2	DQ20		Comp_of_IOR47A	True	D13
IOR49A	I/O	2	DQ20		True_of_IOR49B	True	B11
IOR49B	I/O	2	DQ20		Comp_of_IOR49A	True	A11
IOR4A	I/O	2	DQ23		True_of_IOR4B	True	J14
IOR4B	I/O	2	DQ23		Comp_of_IOR4A	True	H15
IOR51A	I/O	2	DQ20		True_of_IOR51B	True	B13
IOR51B	I/O	2	DQ20		Comp_of_IOR51A	True	B14
IOR53A	I/O	2	DQ20		True_of_IOR53B	True	D14
IOR53B	I/O	2	DQ20		Comp_of_IOR53A	True	C14
IOR6A	I/O	2	DQ23		True_of_IOR6B	True	J17
IOR6B	I/O	2	DQ23		Comp_of_IOR6A	True	J18
IOR8A	I/O	2	DQS23		True_of_IOR8B	True	E18
IOR8B	I/O	2	DQS23		Comp_of_IOR8A	True	D18