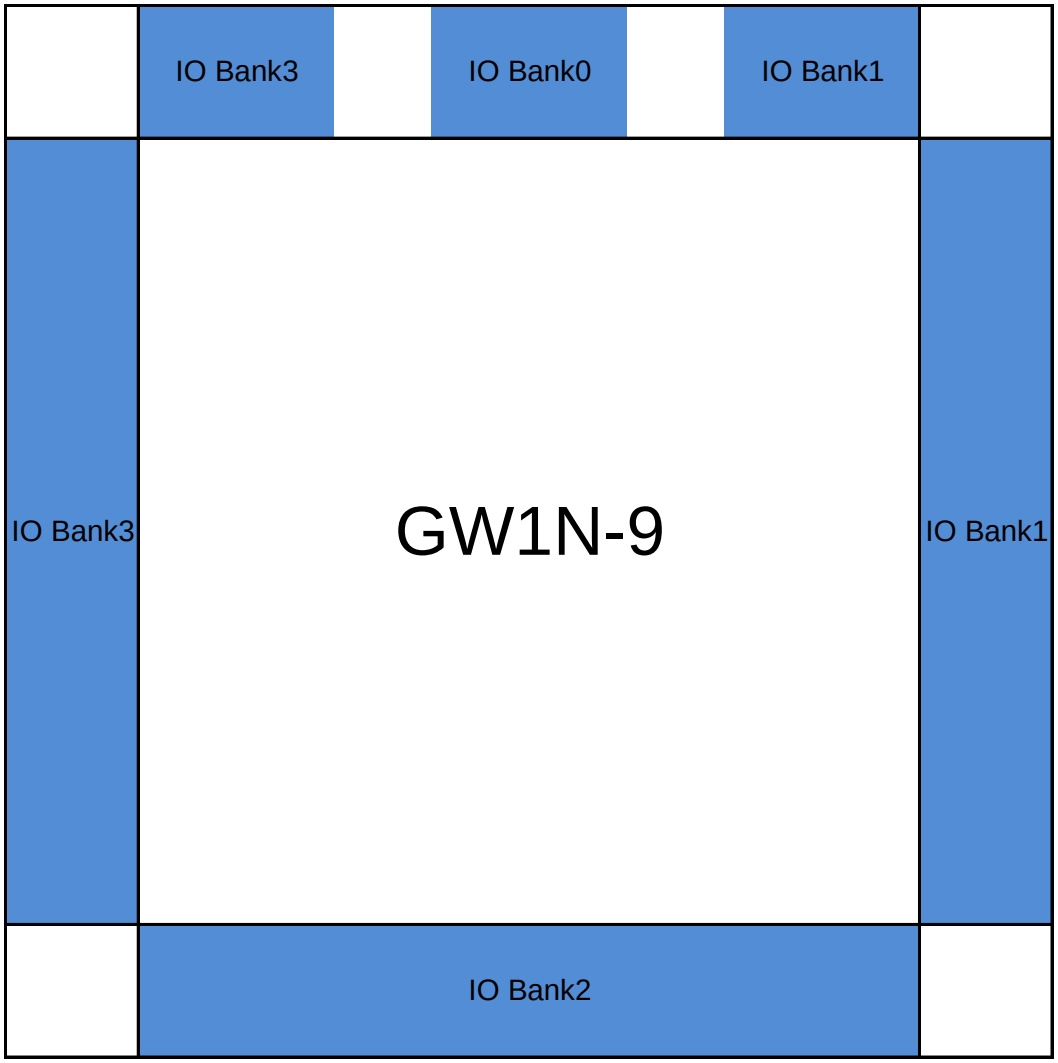
Date	Version	Description
08/23/2016	1.0E	Initial version published.
06/20/2019	1.1E	The info. of UG169 and EQ176 packages added.
03/30/2020	1.2E	The info. of CS81M package added. The info. of Power improved. The descriptions of pin MODE0/MODE1/MODE2 improved.
04/16/2020	1.3E	The info. of GW1N-6 devices removed.
07/03/2020	1.4E	The info. of MG100 and QN48F packages added.
03/17/2021	1.4.1E	The info. of True LVDS improved.
05/19/2021	1.5E	The info. of MG100T package added.
10/20/2022	1.6E	Pin definitions updated. The note in Power sheet updated.
05/04/2023	1.6.1E	The note of QN48 package in Power sheet added. The description of CLKHOLD_N pin in Pin Definitions sheet updated.
06/30/2023	1.7E	QN60 package added. The descriptions of pin definitions and info. for MODE0, MODE1, MODE2 pins optimized.
08/18/2023	1.7.1E	The info. of QN60 package in Pin List sheet and True LVDS sheet updated.
10/31/2023	1.8E	The info. of QN88F package added. The MODE2 pin of QN60 updated.

Pin Name	I/O	Description
User I/O		
IO[End][Row/Column Number][A/B]	I/O	[End] indicates the pin location, including L(left), R(right), B(bottom), and T(top).
		[Row/Column Number] indicates the pin row/column number. If [End] is T(top) or B(bottom), the pin indicates the column number of the corresponding CFU. If [End] is L(left) or R(right), the pin indicates the row number of the corresponding CFU.
		[A/B] indicates differential signal pair information.
Multi-Function Pins		
IO[End][Row/Column Number][A/B]/MMM		/MMM represents one or more of the other functions in addition to being general purpose user I/O. When these functions are not in use, these pins can be used as user I/O.
D0	I/O	Data port D0 in CPU mode
D1	I/O	Data port D1 in CPU mode
D2	I/O	Data port D2 in CPU mode
D3	I/O	Data port D3 in CPU mode
D4	I/O	Data port D4 in CPU mode
D5	I/O	Data port D5 in CPU mode
D6	I/O	Data port D6 in CPU mode
D7	I/O	Data port D7 in CPU mode
WE_N	I	Select data input/output of D[7:0] in CPU mode.0: Write;1: Read.
DOUT	O	Data output in SERIAL mode
DIN	I, internal weak pull-up	Data input in SERIAL mode
TMS	I, internal weak pull-up	Serial mode input in JTAG mode
TCK	I	Serial clock input in JTAG mode
TDO	O	Serial data output in JTAG mode
TDI	I, internal weak pull-up	Serial data input in JTAG mode
JTAGSEL_N	I, internal weak pull-up	Reconfigure JTAG download function signal
RECONFIG_N	I, internal weak pull-up	Global reset GowinCONFIG logic signal, active low
FASTRD_N	I	Access SPI FLASH to select signal. Low, Fast Read mode; High, Read mode.
DONE[1]	O, internal weak pull-up	High, the programming configuration has been completed successfully; Low, the programming configuration has not been completed or failed.
	I, internal weak pull-up	When the DONE signal is low, delay the chip to activate. Activate the chip until the DONE signal is high.
READY[1]	I/O, internal weak pull-up	High, the device can be programmed and configured currently; Low, the device cannot be programmed and configured currently.

Pin Name	I/O	Description
MI	I	MI in MSPI mode
MO	O	MO in MSPI mode
MCS_N	O	Enable signal MCS_N in MSPI mode, active-low
MCLK	O	Clock output MCLK in MSPI mode, with default frequency of 2.5Mhz
SCLK	I	Clock input in SSPI, SERIAL, and CPU modes
SO	O	SO in SSPI mode
SI	I/O	SI in SSPI mode
SSPI_CS_N	I/O	Enable signal SSPI_CS_N in SSPI mode, active-low, and internal weak pull-up
CLKHOLD_N	I, internal weak pull-up	Active-high in SSPI mode; Active-low in CPU mode.
GCLKC_[x]	I	Differential input pin of GCLKT_[x], C(Comp), [x]: global clock No.[2]
GCLKT_[x]	I	Global clock input pin, T(True), [x]: global clock No.
LPLL_C_fb/RPLL_C_fb	I	Left/Right PLL feedback input pin, C(Comp)
LPLL_T_fb/RPLL_T_fb	I	Left/Right PLL feedback input pin, T(True)
LPLL_C_in/RPLL_C_in	I	Left/Right PLL clock input pin, C(Comp)
LPLL_T_in/RPLL_T_in	I	Left/Right PLL clock input pin, T(True)
MODE2	I, internal weak pull-up	GowinCONFIG modes selection pin; if this pin is marked as “VCCIO”, it's internally powered; if this pin is marked as "GND", it's internally grounded.
MODE1	I, internal weak pull-up	GowinCONFIG modes selection pin; if this pin is marked as “VCCIO”, it's internally powered; if this pin is marked as "GND", it's internally grounded.
MODE0	I, internal weak pull-up	GowinCONFIG modes selection pin; if this pin is marked as “VCCIO”, it's internally powered; if this pin is marked as "GND", it's internally grounded.
Other Pins		
NC	NA	Reserved
VSS	NA	Ground
VCC	NA	Power supply pin of core voltage
VCCIO#	NA	Power supply pin of I/O voltage for I/O BANK#
VCCX	NA	Power supply pin of auxiliary voltage

Note!
[1] The default state of READY/DONE is open-drain output, internal weak pull-up. DONE outputs 0 during configuration.
[2] When the input is single-ended, GCLKC_[x] pin is not a global clock pin.



Note!

[1] Each Bank has independent reference voltage (VREF).

[2] You can select to use IOB internal VREF (equals to 0.5 * VCCIO).

[3] You can also select to use external VREF input (use any IO pins as external VREF input).

Note!
[1] The pin is internally grounded.
[2] LV Version.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	QN48	CM64	CS81M	QN88	LQ100	MG100	LQ144	EQ144	MG160	UG169	LQ176	EQ176	MG196	UG256	PG256	UG332	QN48F	MG100T	QN60[2]	QN88F[2]
IOB10A	I/O	2		True_of_IOB10B	NONE	NONE														C1	C1	D3				
IOB10B	I/O	2		Comp_of_IOB10A	NONE	NONE														D2	D2	E4				
IOB11A	I/O	2		True_of_IOB11B	TRUE	x16				27	29	J3	42	42	L5	M7	51	51	N2	B1	B1	B1		J3	18	27
IOB11B	I/O	2		Comp_of_IOB11A	TRUE	NONE				28	30	H3	43	43	M5	N6	52	52	P2	C2	C2	C2		H3	19	28
IOB12A	I/O	2		True_of_IOB12B	NONE	NONE							44	44							B3	F4				
IOB12B	I/O	2		Comp_of_IOB12A	NONE	NONE							45	45							A2	E3				
IOB13A	I/O	2		True_of_IOB13B	TRUE	x16		H7		29	31	E4	46	46	N4	N8	53	53		E2	E2	G5		E4	20	29
IOB13B	I/O	2		Comp_of_IOB13A	TRUE	NONE		G7		30	32	F4	47	47	P4	N7	54	54		E3	E3	H5		F4	21	30
IOB14A	I/O	2		True_of_IOB14B	NONE	NONE														E1	E1	D2				
IOB14B	I/O	2		Comp_of_IOB14A	NONE	NONE														F2	F2	C1				
IOB15A	I/O	2		True_of_IOB15B	TRUE	x16					33	K3	48	48	N5	K6	55	55	N3	F4	F4	G4		K3	22	31
IOB15B	I/O	2		Comp_of_IOB15A	TRUE	NONE					34	K4	49	49	P5	J6	56	56	P3	G6	G6	F3		K4	23	32
IOB16A	I/O	2		True_of_IOB16B	NONE	NONE														F3	F3	E2				
IOB16B	I/O	2		Comp_of_IOB16A	NONE	NONE														F1	F1	D1				
IOB17A	I/O	2		True_of_IOB17B	TRUE	x16	15	H6	C4	31	35	J4	50	50	L6	M9	57	57		G5	G5	G3	15	J4		33
IOB17B	I/O	2		Comp_of_IOB17A	TRUE	NONE	16	G6	C3	32	36	H4	51	51	M6	M8	58	58		G4	G4	H4	16	H4		34
IOB18A	I/O	2		True_of_IOB18B	NONE	NONE																F2				
IOB18B	I/O	2		Comp_of_IOB18A	NONE	NONE											59	59				E1				
IOB19A	I/O	2		True_of_IOB19B	NONE	NONE											60	60				F1				
IOB19B	I/O	2		Comp_of_IOB19A	NONE	NONE																G2				
IOB20A	I/O	2		True_of_IOB20B	NONE	NONE																J5				
IOB20B	I/O	2		Comp_of_IOB20A	NONE	NONE																J4				
IOB21A	I/O	2		True_of_IOB21B	TRUE	x16						K5			L7	K7	61	61	L4			H2		K5		35
IOB21B	I/O	2		Comp_of_IOB21A	TRUE	NONE						K6			M7	J7	62	62	M4			H1		K6		36
IOB22A	I/O	2		True_of_IOB22B	NONE	NONE														G2	G2	J3				
IOB22B	I/O	2		Comp_of_IOB22A	NONE	NONE														G3	G3	J2				
IOB23A	I/O	2		True_of_IOB23B	TRUE	x16		H5	B3	33		H5	52	52	N6	N12	63	63	N4	F5	F5	K4		H5		37
IOB23B	I/O	2		Comp_of_IOB23A	TRUE	NONE		G5	A2	34		G5	54	54	P6	N11	64	64	P4	H6	H6	K3		G5		38
IOB24A	I/O	2		True_of_IOB24B	NONE	NONE																J1				
IOB24B	I/O	2		Comp_of_IOB24A	NONE	NONE																K2				
IOB25A	I/O	2		True_of_IOB25B	TRUE	x16									L9		67	67	N5			K1				40
IOB25B	I/O	2		Comp_of_IOB25A	TRUE	NONE									M9		68	68	P5			L1				39
IOB26A	I/O	2		True_of_IOB26B	NONE	NONE														G1	G1	L4				
IOB26B	I/O	2		Comp_of_IOB26A	NONE	NONE														H2	H2	L3				
IOB27A	I/O	2		True_of_IOB27B	TRUE	x16	17	H4	A3						N8		69	69	N6	H4	H4	L2	17		25	
IOB27B	I/O	2		Comp_of_IOB27A	TRUE	NONE	18	G4	C5						P8		70	70	P6	J6	J6	M1	18		26	
IOB28A/GCLKT_5	I/O	2	GCLKT_5	True_of_IOB28B	NONE	NONE					39	F5	56	56	N7				N7	J1	J1	M2		F5		
IOB28B/GCLKC_5	I/O	2	GCLKC_5	Comp_of_IOB28A	NONE	NONE					40	E5	57	57	P7				P7	J3	J3	M3		E5		
IOB29A/GCLKT_4	I/O	2	GCLKT_4	True_of_IOB29B	TRUE	x16	19	F5	D6	35	41	J6	58	58	L8	M12	71	71	N8	L2	L2	M5	19	J6	28	42
IOB29B/GCLKC_4	I/O	2	GCLKC_4	Comp_of_IOB29A	TRUE	NONE	20	F4	C6	36	42	H6	59	59	M8	M13	72	72	P8	M1	M1	M4	20	H6	27	41
IOB2A	I/O	2		True_of_IOB2B	TRUE	x16				17						L4	36	36				C6				
IOB2B	I/O	2		Comp_of_IOB2A	TRUE	NONE				18						L5	37	37				D7				
IOB30A	I/O	2		True_of_IOB30B	NONE	NONE							60	60						H3	H3	N1				
IOB30B	I/O	2		Comp_of_IOB30A	NONE	NONE							61	61						H1	H1	N2				
IOB31A	I/O	2		True_of_IOB31B	TRUE	x16				37	43	K7	62	62	N9		73	73	L8	J2	J2	N3	21	K7		
IOB31B	I/O	2		Comp_of_IOB31A	TRUE	NONE				38	44	K8	63	63	P9		74	74	M8	K1	K1	N4	22	K8		
IOB32A	I/O	2		True_of_IOB32B	NONE	NONE														H5	H5	P1				
IOB32B	I/O	2		Comp_of_IOB32A	NONE	NONE														J4	J4	R1				
IOB33A	I/O	2		True_of_IOB33B	TRUE	x16		H3	A4	39	45	J7	64	64	L10		75	75	N9	K3	K3	P2		J7		
IOB33B	I/O	2		Comp_of_IOB33A	TRUE	NONE		G3	B5	40	46	H7	65	65	M10		76	76	P9	K2	K2	P3		H7		
IOB34A	I/O	2		True_of_IOB34B	NONE	NONE											77	77		J5	J5	R2				
IOB34B	I/O	2		Comp_of_IOB34A	NONE	NONE											78	78		K6	K6	T1				
IOB35A	I/O	2		True_of_IOB35B	TRUE	x16	21		A6		47	F6	66	66	N10	N9	79	79	N10	L1	L1	P4	24	F6		
IOB35B	I/O	2		Comp_of_IOB35A	TRUE	NONE	22		A5		48	G6	67	67	P10	N10	80	80	P10	L3	L3	R3	23	G6		
IOB36A	I/O	2		True_of_IOB36B	NONE	NONE														K4	K4	N5				
IOB36B	I/O	2		Comp_of_IOB36A	NONE	NONE														L5	L5	P5				
IOB37A	I/O	2		True_of_IOB37B	NONE	NONE							68	68			81	81		K5	K5	T2				
IOB37B	I/O	2		Comp_of_IOB37A	NONE	NONE							69	69			82	82		L4	L4	U1				
IOB38A	I/O	2		True_of_IOB38B	NONE	NONE														N2	N2	R4				
IOB38B	I/O	2		Comp_of_IOB38A	NONE	NONE														P1	P1	T3				
IOB39A	I/O	2		True_of_IOB39B	TRUE	x16	23	H2	A7		49	F7	70	70	P11		83	83	N11	M3	M3	V1		F7	30	48

Note!
[1] The pin is internally grounded.
[2] LV Version.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	QN48	CM64	CS81M	QN88	LQ100	MG100	LQ144	EQ144	MG160	UG169	LQ176	EQ176	MG196	UG256	PG256	UG332	QN48F	MG100T	QN60[2]	QN88F[2]
IOB39B	I/O	2		Comp_of_IOB39A	TRUE	NONE	24	G2	B6		50	G7	71	71	N11		84	84	P11	N1	N1	U2		G7	29	47
IOB3A	I/O	2		True_of_IOB3B	NONE	NONE						H1										B5				
IOB3B	I/O	2		Comp_of_IOB3A	NONE	NONE																A5		H1		
IOB40A	I/O	2		True_of_IOB40B	NONE	NONE														M2	M2	T4				
IOB40B	I/O	2		Comp_of_IOB40A	NONE	NONE									P13					N3	N3	R5				
IOB41A	I/O	2		True_of_IOB41B	TRUE	x16		H1		41		K10	72	72	P12	L11	85	85	N12	R1	R1	U3		K10		
IOB41B	I/O	2		Comp_of_IOB41A	TRUE	NONE		G1		42		K9			N12	M11	86	86	P12	P2	P2	V2		K9		
IOB42A	I/O	2		True_of_IOB42B	NONE	NONE											92	92			T4	U4				
IOB42B	I/O	2		Comp_of_IOB42A	NONE	NONE							75	75			91	91			P4	T6				
IOB43A	I/O	2		True_of_IOB43B	TRUE	x16					55	J10	78	78	M14	K8	94	94	L12		T2	W2		J10		
IOB43B	I/O	2		Comp_of_IOB43A	TRUE	NONE				47	53		76	76	N14	J8	93	93	M12		R3	W1				
IOB44A	I/O	2		True_of_IOB44B	NONE	NONE									K13		97	97			R5	T7				
IOB44B	I/O	2		Comp_of_IOB44A	NONE	NONE									L14		96	96			P5	T8				
IOB45A	I/O	2		True_of_IOB45B	TRUE	x16									J13	L10	99	99	N13		T3	U5				
IOB45B	I/O	2		Comp_of_IOB45A	TRUE	NONE									L13	M10	98	98	P13		R4	V4				
IOB46A	I/O	2		True_of_IOB46B	NONE	NONE											101	101				U6				
IOB46B	I/O	2		Comp_of_IOB46A	NONE	NONE											100	100				V5				
IOB4A	I/O	2		True_of_IOB4B	TRUE	x16				19		K1	29	29	L1	M5	38	38	L2			D6		K1		
IOB4B	I/O	2		Comp_of_IOB4A	TRUE	NONE				20		K2	30	30	M1	M4	39	39	L1			E7		K2		
IOB5A	I/O	2		True_of_IOB5B	NONE	NONE															D6	C5				
IOB5B	I/O	2		Comp_of_IOB5A	NONE	NONE															E7	D5				
IOB6A	I/O	2		True_of_IOB6B	TRUE	x16					22		32	32	N1	J5	41	41	N1		A4	E6				
IOB6B	I/O	2		Comp_of_IOB6A	TRUE	NONE					23		34	34	P2	K5	42	42			C5	F5				
IOB7A	I/O	2		True_of_IOB7B	NONE	NONE															A5	B4				
IOB7B	I/O	2		Comp_of_IOB7A	NONE	NONE															B6	A4				
IOB8A	I/O	2		True_of_IOB8B	TRUE	x16	13	H8		25	27	G4	38	38	N3	N5	47	47	M2		A3	C4	13	G4		26
IOB8B	I/O	2		Comp_of_IOB8A	TRUE	NONE	14	G8		26	28	G3	39	39	P3	N4	48	48	M1		B4	A3	14	G3		25
IOB9A	I/O	2		True_of_IOB9B	NONE	NONE							40	40			49	49		D3	D3	B3				
IOB9B	I/O	2		Comp_of_IOB9A	NONE	NONE							41	41			50	50		D1	D1	D4				
IOL11A/TMS	I/O	3	TMS	True_of_IOL11B	TRUE	NONE	4	D7	D3	5	8	E2	13	13	F1	G1	16	16	B14	B8	B8	C9	4	E2	9	5
IOL11B/TCK	I/O	3	TCK	Comp_of_IOL11A	TRUE	NONE	5	D6	D4	6	9	E3	14	14	G1	G2	17	17	B13	A7	A7	A8	5	E3	8	6
IOL12A/SCLK	I/O	3	SCLK	True_of_IOL12B	NONE	NONE					10		15	15	F3		18	18		C10	C10	B13	6			
IOL12B/TDI	I/O	3	TDI	Comp_of_IOL12A	NONE	NONE	6	E7	E1	7	11	F3	16	16	G4	F5	19	19	A13	A6	A6	B7	7	F3	10	7
IOL13A/TDO	I/O	3	TDO	True_of_IOL13B	TRUE	NONE	7	E6	E2	8	12	F2	18	18	G3	F6	20	20	C14	C6	C6	C7	8	F2	12	8
IOL13B/RECONFIG_N	I/O	3	RECONFIG_N	Comp_of_IOL13A	TRUE	NONE	8			9	14	D3	20	20	H3		21	21		B10	B10	A14	9	D3		9
IOL14A/DONE	I/O	3	DONE	True_of_IOL14B	NONE	NONE	9			10	15		21	21	J4	H1	23	23	N14	C13	C13	B17				
IOL14B/READY	I/O	3	READY	Comp_of_IOL14A	NONE	NONE					16		22	22	H2					A13	A13	A13		D1		
IOL15A/GCLKT_6	I/O	3	GCLKT_6	True_of_IOL15B	TRUE	NONE	10	D8	F2	11	17	F1	23	23	J2	H4	24	24	G2	C8	C8	D12	10		14	10
IOL15B/GCLKC_6	I/O	3	GCLKC_6	Comp_of_IOL15A	TRUE	NONE	11	E8	F1		18	D1	24	24	J3	H5	25	25	G1	A8	A8	C12	11	F1	13	11
IOL16A	I/O	3		True_of_IOL16B	NONE	NONE														F8	F9	B12				
IOL16B	I/O	3		Comp_of_IOL16A	NONE	NONE														D9	E11	A12		D2		
IOL17A	I/O	3		True_of_IOL17B	TRUE	NONE									H1	G4	26	26	J2	D8		D11				
IOL17B	I/O	3		Comp_of_IOL17A	TRUE	NONE									K3	F4	27	27	J1	E9		C11				
IOL18A	I/O	3		True_of_IOL18B	NONE	NONE														B7	B9	B11				
IOL18B	I/O	3		Comp_of_IOL18A	NONE	NONE														C7	A10	A11				
IOL20A	I/O	3		True_of_IOL20B	TRUE	NONE					19	D2			J1	H3	28	28	J4	F7	F8	E10				13
IOL20B	I/O	3		Comp_of_IOL20A	TRUE	NONE					20	G2			K1	H2	29	29	J3	E8	D9	D10				14
IOL21A	I/O	3		True_of_IOL21B	NONE	NONE														C4	D8	C10				
IOL21B	I/O	3		Comp_of_IOL21A	NONE	NONE														B5	E9	B10		G2		
IOL22A	I/O	3		True_of_IOL22B	TRUE	NONE		F8	C1	13			25	25	K2	J2	30	30	K2	E6	B7	E12				15
IOL22B	I/O	3		Comp_of_IOL22A	TRUE	NONE		F7	C2	14			26	26	L2	J1	31	31	K1	D7	C7	B9		G1		16
IOL23A	I/O	3		True_of_IOL23B	NONE	NONE										L1				D6	F7	D9				
IOL23B	I/O	3		Comp_of_IOL23A	NONE	NONE										L2				E7	E8	E9				
IOL24A	I/O	3		True_of_IOL24B	TRUE	NONE						G1				M2	32	32		A4	C4	A9				17
IOL24B	I/O	3		Comp_of_IOL24A	TRUE	NONE						H2				M1	33	33		C5	B5	B8				18
IOL25A	I/O	3		True_of_IOL25B	NONE	NONE										N3				B3	E6	A7				
IOL25B	I/O	3		Comp_of_IOL25A	NONE	NONE										N2				A2	D7	C8		H2		
IOL26A	I/O	3		True_of_IOL26B	TRUE	NONE				15			27	27		L3				A5		D8				19
IOL26B	I/O	3		Comp_of_IOL26A	TRUE	NONE				16			28	28		M3				B6		E8				20
IOL27A	I/O	3		True_of_IOL27B	NONE	NONE										K2	35	35		A3		B6				

Note!
[1] The pin is internally grounded.
[2] LV Version.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	QN48	CM64	CS81M	QN88	LQ100	MG100	LQ144	EQ144	MG160	UG169	LQ176	EQ176	MG196	UG256	PG256	UG332	QN48F	MG100T	QN60[2]	QN88F[2]
IOL27B	I/O	3		Comp_of_IOL27A	NONE	NONE										K1				B4		A6				
IOL2A	I/O	3		True_of_IOL2B	TRUE	NONE				3			3	3	C1	C2	3	3		B11	B14	A18				88
IOL2B	I/O	3		Comp_of_IOL2A	TRUE	NONE									D2	D1	4	4		A12	A15	A17				3
IOL3A	I/O	3		True_of_IOL3B	NONE	NONE											5	5		C12	F10	D15				
IOL3B	I/O	3		Comp_of_IOL3A	NONE	NONE											6	6		B12	D11	E14				
IOL4A	I/O	3		True_of_IOL4B	TRUE	NONE									D1	E4	7	7	E2	B13	B11	C16				
IOL4B	I/O	3		Comp_of_IOL4A	TRUE	NONE									E1	E3	8	8	E1	A14	A12	B16		B2		
IOL5A/JTAGSEL_N/LPLL_T_in	I/O	3	JTAGSEL_N/LPLL_T_in	True_of_IOL5B	NONE	NONE	3	C8	D2	4	3	B1	4	4	E2	E5	9	9	D2	A11	C12	C15	3	B1	2	
IOL5B/LPLL_C_in	I/O	3	LPLL_C_in	Comp_of_IOL5A	NONE	NONE		C7	E3			B3			E3		10	10	D1	C11	B12	D14		B3	3	
IOL6A/LPLL_T_fb	I/O	3	LPLL_T_fb	True_of_IOL6B	TRUE	NONE						B2			E4	B1	11	11	F4	D10	B13	A16				
IOL6B/LPLL_C_fb	I/O	3	LPLL_C_fb	Comp_of_IOL6A	TRUE	NONE						C1	6	6	F4	C1	12	12	F3	E10	A14	A15				
IOL7A	I/O	3		True_of_IOL7B	NONE	NONE							7	7						F9	A11	E13				
IOL7B	I/O	3		Comp_of_IOL7A	NONE	NONE					5		8	8						E11	C11	D13		C1		
IOL8A	I/O	3		True_of_IOL8B	TRUE	NONE			G3				9	9	H4	E1			F2	A9	D10	B15				
IOL8B	I/O	3		Comp_of_IOL8A	TRUE	NONE			F3				10	10	K4	F1			F1	B9	E10	C14		C2		
IOL9A/GCLKT_7	I/O	3	GCLKT_7	True_of_IOL9B	NONE	NONE			G1		6	C2	11	11	F2	H6	14	14	H2	A10	A9	B14			6	
IOL9B/GCLKC_7	I/O	3	GCLKC_7	Comp_of_IOL9A	NONE	NONE			G2		7	C3	12	12	G2	G5	15	15	H1	C9	C9	C13		C3	7	
IOR11A/MI/D7	I/O	1	MI/D7	True_of_IOR11B	TRUE	NONE	34			62	68	G9	96	96	F14	H9	122	122		M9	P10	W13			42	61
IOR11B/MO/D6	I/O	1	MO/D6	Comp_of_IOR11A	TRUE	NONE	33			61	67	F9	95	95	G14	H8	121	121		L10	R10	Y14		F9	41	60
IOR12A/MCS_N/D5	I/O	1	MCS_N/D5	True_of_IOR12B	NONE	NONE	32			60	66	F10	94	94	E12	F12	120	120		R9	M9	T12			40	57
IOR12B/MCLK/D4	I/O	1	MCLK/D4	Comp_of_IOR12A	NONE	NONE	31			59	65	E10	93	93	G12	E12	119	119		T10	L10	U13	34	E10	39	59
IOR13A/FASTRD_N/D3	I/O	1	FASTRD_N/D3	True_of_IOR13B	TRUE	NONE				57	64		92	92	G11	G13	118	118	J13	M8	R9	T11				
IOR13B/SI/D2	I/O	1	SI/D2	Comp_of_IOR13A	TRUE	NONE					62		90	90	G13	G12	117	117	J14	N9	T10	U11	33			
IOR14A/SO/D1	I/O	1	SO/D1	True_of_IOR14B	NONE	NONE				56	61		88	88	H14	F8	116	116		N8	M8	W10	32			
IOR14B/SSPI_CS_N/D0	I/O	1	SSPI_CS_N/D0	Comp_of_IOR14A	NONE	NONE				55	60		87	87	J11	E9	114	114		L9	N9	Y9	31	G9		
IOR15A/DIN/CLKHOLD_N	I/O	1	DIN/CLKHOLD_N	True_of_IOR15B	TRUE	NONE				54	59		86	86	H13	J13	113	113	H13	P8	T9	Y8				
IOR15B/DOUT/WE_N	I/O	1	DOUT/WE_N	Comp_of_IOR15A	TRUE	NONE				53	58		85	85	H12	H13	112	112	H14	T8	P9	W9				
IOR16A	I/O	1		True_of_IOR16B	NONE	NONE														M6		V10				
IOR16B	I/O	1		Comp_of_IOR16A	NONE	NONE														L8		U10		F10		
IOR17A/GCLKT_3	I/O	1	GCLKT_3	True_of_IOR17B	TRUE	NONE	30	E3	D8	52	57	F8	84	84	J14	G9	111	111	H11	T7	T7	V9	30	F8		56
IOR17B/GCLKC_3	I/O	1	GCLKC_3	Comp_of_IOR17A	TRUE	NONE	29	D3	D9	51	56	G8	83	83	K14	G10			H12	R8	R8	W8	29	G8		55
IOR18A	I/O	1		True_of_IOR18B	NONE	NONE														M7	N8	Y7				
IOR18B	I/O	1		Comp_of_IOR18A	NONE	NONE														N7	L9	W7		H8		
IOR20A	I/O	1		True_of_IOR20B	TRUE	NONE						H8				J9			J11	R7	P8	V8				54
IOR20B	I/O	1		Comp_of_IOR20A	TRUE	NONE						G10				H10			J12	P7	T8	U9				53
IOR21A	I/O	1		True_of_IOR21B	NONE	NONE										L13				N6	M6	Y6				
IOR21B	I/O	1		Comp_of_IOR21A	NONE	NONE										K13				L7	L8	W6		G10		
IOR22A	I/O	1		True_of_IOR22B	TRUE	NONE		E1	C8				82	82	E11	K12	109	109	K13	P6	M7	Y5				52
IOR22B	I/O	1		Comp_of_IOR22A	TRUE	NONE		E2	C9	50			81	81	F11	J12	108	108	K14	T6	N7	Y4				51
IOR23A	I/O	1		True_of_IOR23B	NONE	NONE														T5	R7	V7				
IOR23B	I/O	1		Comp_of_IOR23A	NONE	NONE														R6	P7	U8				
IOR24A	I/O	1		True_of_IOR24B	TRUE	NONE	28	F1	F8	49		H9	80	80	J12	K11	107	107	L13	T3	N6	W5	28		37	50
IOR24B	I/O	1		Comp_of_IOR24A	TRUE	NONE	27	F2	F9	48		H10	79	79	H11	L12	106	106	L14	R4	L7	V6	27	H9	36	49
IOR25A	I/O	1		True_of_IOR25B	NONE	NONE														R5	P6	U7				
IOR25B	I/O	1		Comp_of_IOR25A	NONE	NONE														P5	T6	T9		H10		
IOR26A	I/O	1		True_of_IOR26B	TRUE	NONE									K12	K10	105	105	M13	T2		Y3			35	
IOR26B	I/O	1		Comp_of_IOR26A	TRUE	NONE									K11	J10	104	104	M14	R3		W4			34	
IOR27A	I/O	1		True_of_IOR27B	NONE	NONE											103	103		T4	T5	W3				
IOR27B	I/O	1		Comp_of_IOR27A	NONE	NONE											102	102		P4	R6	Y2				
IOR2A	I/O	1		True_of_IOR2B	TRUE	NONE						C10				D12			C12	R13						
IOR2B	I/O	1		Comp_of_IOR2A	TRUE	NONE						B10				D11			C13	T14				C10		
IOR3A	I/O	1		True_of_IOR3B	NONE	NONE										E10				T15	R11	V14				
IOR3B	I/O	1		Comp_of_IOR3A	NONE	NONE										D9				R14	T12	U14		B10		
IOR4A	I/O	1		True_of_IOR4B	TRUE	NONE			G8							B13			E13	P12	R13	T14				
IOR4B	I/O	1		Comp_of_IOR4A	TRUE	NONE			G9							A12			E14	T13	T14	T13				
IOR5A/RPLL_T_in	I/O	1	RPLL_T_in	True_of_IOR5B	NONE	NONE	35	C1	C7	63	73	C9	106	106	B14	C12	129	129	D13	M10	T15	W14	35	C9		

Note!
[1] The pin is internally grounded.
[2] LV Version.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	QN48	CM64	CS81M	QN88	LQ100	MG100	LQ144	EQ144	MG160	UG169	LQ176	EQ176	MG196	UG256	PG256	UG332	QN48F	MG100T	QN60[2]	QN88F[2]
IOR5B/RPLL_C_in	I/O	1	RPLL_C_in	Comp_of_IOR5A	NONE	NONE		C2	B7		72	D9	104	104	C14	C11	128	128	D14	N11	R14	V13		D9		
IOR6A/RPLL_T_fb	I/O	1	RPLL_T_fb	True_of_IOR6B	TRUE	NONE		D1					102	102	D14	B12	127	127	F11	T11	P12	Y13				
IOR6B/RPLL_C_fb	I/O	1	RPLL_C_fb	Comp_of_IOR6A	TRUE	NONE		D2					101	101	E14	B11	126	126	F12	P11	T13	Y12				
IOR7A	I/O	1		True_of_IOR7B	NONE	NONE										C13				N10	M10	W12				
IOR7B	I/O	1		Comp_of_IOR7A	NONE	NONE										D13				M11	N11	V12		D10		
IOR8A	I/O	1		True_of_IOR8B	TRUE	NONE			G7				100	100	D13	F9			G13	P10	T11	U12				63
IOR8B	I/O	1		Comp_of_IOR8A	TRUE	NONE			F7				99	99	E13	F10	125	125	G14	R10	P11	V11				62
IOR9A/GCLKT_2	I/O	1	GCLKT_2	True_of_IOR9B	NONE	NONE			E8		70	D10	98	98	F13	F13	124	124	F13	T9	N10	W11		E8	44	
IOR9B/GCLKC_2	I/O	1	GCLKC_2	Comp_of_IOR9A	NONE	NONE			E7		69	E8	97	97	F12	E13	123	123	F14	P9	M11	Y10			43	
IOT10A	I/O	3		True_of_IOT10B	NONE	NONE				84			140	140			169	169			C16	G16				
IOT10B	I/O	3		Comp_of_IOT10A	NONE	NONE				83			139	139			168	168			D15	F17				
IOT11A	I/O	3		True_of_IOT11B	NONE	x16		A7		82							167	167				D20		C4		
IOT11B	I/O	3		Comp_of_IOT11A	NONE	NONE		B7		81							166	166				E19		B4		
IOT12A	I/O	3		True_of_IOT12B	NONE	NONE	47			80	97		138	138	A4		165	165				H16				
IOT12B	I/O	3		Comp_of_IOT12A	NONE	NONE	46			79	96		137	137	A5		164	164				G17				
IOT13A	I/O	0		True_of_IOT13B	NONE	x16						A4				B3			D3	L15	E16	G18		D5	58	
IOT13B	I/O	0		Comp_of_IOT13A	NONE	NONE						A3				B4			D4	M16	F15	H17		D6	59	
IOT14A	I/O	0		True_of_IOT14B	NONE	NONE									B5					C16	F14	F20				
IOT14B	I/O	0		Comp_of_IOT14A	NONE	NONE									B6					D15	F16	G19				
IOT15A	I/O	0		True_of_IOT15B	NONE	x16		A6			95	B4	136	136		E6	163	163	B1	C15	F13	E20	46			85
IOT15B	I/O	0		Comp_of_IOT15A	NONE	NONE		B6			94	C4	135	135		D6	162	162	C1	B16	G12	F19				86
IOT16A	I/O	0		True_of_IOT16B	NONE	NONE										A2				D16	F12	H18				
IOT16B	I/O	0		Comp_of_IOT16A	NONE	NONE										B2				E14	G13	H19				
IOT17A	I/O	0		True_of_IOT17B	NONE	x16		A5	H7		93	D5	134	134		A4	161	161	B2	E16	G15	G20		C5	57	83
IOT17B	I/O	0		Comp_of_IOT17A	NONE	NONE		B5	G6		92	D6	133	133		A3	160	160	A2	F15	G14	H20		B5	56	84
IOT18A	I/O	0		True_of_IOT18B	NONE	NONE									C5	B7			B3	F12		J18				
IOT18B	I/O	0		Comp_of_IOT18A	NONE	NONE									D5				A3	G13		J19				
IOT19A	I/O	0		True_of_IOT19B	NONE	NONE										A5				F13	G11	J17				
IOT19B	I/O	0		Comp_of_IOT19A	NONE	NONE														G12	H12	J16				
IOT20A	I/O	0		True_of_IOT20B	NONE	NONE					91		132	132			159	159		F14	G16	J20				
IOT20B	I/O	0		Comp_of_IOT20A	NONE	NONE							131	131			158	158		F16	H15	K18				
IOT21A	I/O	0		True_of_IOT21B	NONE	x16			J2			C5				C4			B4	G15		K17	45	C6		82
IOT21B	I/O	0		Comp_of_IOT21A	NONE	NONE			H3			B5				C5			A4	G14		K16	44	B6		81
IOT22A	I/O	0		True_of_IOT22B	NONE	NONE	45				90		130	130	A6		157	157	B5	G11	H13	K19				
IOT22B	I/O	0		Comp_of_IOT22A	NONE	NONE	44				89		129	129	A7		156	156	A5	H12	J12	L20				
IOT23A	I/O	0		True_of_IOT23B	NONE	x16		C5	J6			C6				B6				G16	H14	L19				80
IOT23B	I/O	0		Comp_of_IOT23A	NONE	NONE		C4	H6			B6				B5				H15	H16	L18				79
IOT24A	I/O	0		True_of_IOT24B	NONE	NONE							128	128	C6					H13		M20				
IOT24B	I/O	0		Comp_of_IOT24A	NONE	NONE							126	126	D6					J12		M19				
IOT25A	I/O	0		True_of_IOT25B	NONE	x16			J8							A7			B6	H11	J16	L17				77
IOT25B	I/O	0		Comp_of_IOT25A	NONE	NONE			J7							A6	153	153	A6	J13	J14	M18				76
IOT26A	I/O	0		True_of_IOT26B	NONE	NONE									C7					J16		M16				
IOT26B	I/O	0		Comp_of_IOT26A	NONE	NONE									D7					J14		M17				
IOT27A	I/O	0		True_of_IOT27B	NONE	x16		A4	J5			A6	125	125		D8	152	152	B7	J15	J15	N20		A6	54	75
IOT27B	I/O	0		Comp_of_IOT27A	NONE	NONE		B4	J4			A7	124	124		E8	151	151	A7	K16	K16	N19		A7	53	74
IOT28A/GCLKT_0	I/O	0	GCLKT_0	True_of_IOT28B	NONE	NONE						E7			B7	E7			B8	H14	H11	P19				73
IOT28B/GCLKC_0	I/O	0	GCLKC_0	Comp_of_IOT28A	NONE	NONE						E6			B8	D7			D8	H16	J13	P18				72
IOT29A/GCLKT_1	I/O	0	GCLKT_1	True_of_IOT29B	NONE	x16		A3	H4			B7	123	123		A10	150	150	A8	K14	K14	R19	43	E6	52	70
IOT29B/GCLKC_1	I/O	0	GCLKC_1	Comp_of_IOT29A	NONE	NONE		B3	J3			C7	122	122		A11	149	149	B10	K15	K15	R18	42	E7	51	71
IOT2A	I/O	3		True_of_IOT2B	NONE	x16														F10	L15	A19				
IOT2B	I/O	3		Comp_of_IOT2A	NONE	NONE														D11		B18				
IOT30A	I/O	0		True_of_IOT30B	NONE	NONE									A8				A9	L16	J11	T18				
IOT30B	I/O	0		Comp_of_IOT30A	NONE	NONE									A9				A10	L14	L12	U18				
IOT31A	I/O	0		True_of_IOT31B	NONE	x16						B8				B10			C8	J11		R20				
IOT31B	I/O	0		Comp_of_IOT31A	NONE	NONE						C8				B9			B9	L12		T20				
IOT32A	I/O	0		True_of_IOT32B	NONE	NONE	43				86		121	121	C8		148	148		K13	L16	U20				
IOT32B	I/O	0		Comp_of_IOT32A	NONE	NONE	42				85		120	120	D8		147	147		K12	L14	V20				
IOT33A	I/O	0		True_of_IOT33B	NONE	x16		A2	G5			D8			B9	A8			A11	L13		T19	41	C7	49	
IOT33B	I/O	0		Comp_of_IOT33A	NONE	NONE		B2	G4			D7			B10	A9			B12	M14		U19	40	B7	50	
IOT34A	I/O	0		True_of_IOT34B	NONE	NONE							119	119	D9		146	146	D11	D14	K13	N16				
IOT34B	I/O	0		Comp_of_IOT34A	NONE	NONE							118	118	C9		145	145	C11	E15	K12	N17				

Note!
[1] The pin is internally grounded.
[2] LV Version.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	QN48	CM64	CS81M	QN88	LQ100	MG100	LQ144	EQ144	MG160	UG169	LQ176	EQ176	MG196	UG256	PG256	UG332	QN48F	MG100T	QN60[2]	QN88F[2]
IOT35A	I/O	0		True_of_IOT35B	NONE	x16						B9				C10			B11	K11		V19	39		48	69
IOT35B	I/O	0		Comp_of_IOT35A	NONE	NONE						A10				C9			A12	M15		W19	38		47	68
IOT36A	I/O	1		True_of_IOT36B	NONE	NONE									A11						K11	P16				
IOT36B	I/O	1		Comp_of_IOT36A	NONE	NONE									A10						L13	P17				
IOT37A	I/O	1		True_of_IOT37B	NONE	NONE	41			77	84		117	117			144	144		N15	M14	T17				
IOT37B	I/O	1		Comp_of_IOT37A	NONE	NONE	40			76	83		116	116			143	143		P16	M15	R17				
IOT38A	I/O	1		True_of_IOT38B	NONE	NONE				75					B11		142	142		N16	D14	W18				
IOT38B	I/O	1		Comp_of_IOT38A	NONE	NONE				74					B12		141	141		N14	E15	Y18				
IOT39A	I/O	1		True_of_IOT39B	NONE	x16		A1		73	82		115	115			140	140		P15	N15	V17		B8		
IOT39B	I/O	1		Comp_of_IOT39A	NONE	NONE		B1		72	81		114	114			139	139		R16	P16	U17		C8		
IOT3A	I/O	3		True_of_IOT3B	NONE	NONE														B14		D16				
IOT3B	I/O	3		Comp_of_IOT3A	NONE	NONE														A15		E15				
IOT40A	I/O	1		True_of_IOT40B	NONE	NONE																Y19				
IOT40B	I/O	1		Comp_of_IOT40A	NONE	NONE																W20				
IOT41A	I/O	1		True_of_IOT41B	NONE	x16				71	80		113	113			138	138			N16	U16		D7		
IOT41B	I/O	1		Comp_of_IOT41A	NONE	NONE				70	79		112	112			137	137			N14	R16		D8		
IOT42A	I/O	1		True_of_IOT42B	NONE	NONE	39			69	78		111	111	A12		136	136			P15	W16				
IOT42B	I/O	1		Comp_of_IOT42A	NONE	NONE	38			68	77		110	110	A13		135	135			R16	V16				
IOT43A	I/O	1		True_of_IOT43B	NONE	x16																Y16				
IOT43B	I/O	1		Comp_of_IOT43A	NONE	NONE																W15				
IOT44A	I/O	1		True_of_IOT44B	NONE	NONE									D10							W17				
IOT44B	I/O	1		Comp_of_IOT44A	NONE	NONE									C10							Y17				
IOT45A	I/O	1		True_of_IOT45B	NONE	x16														R12		T15		B9		
IOT45B	I/O	1		Comp_of_IOT45A	NONE	NONE														P13		U15		A10		
IOT46A	I/O	1		True_of_IOT46B	NONE	NONE														R11	R12	V15				
IOT46B	I/O	1		Comp_of_IOT46A	NONE	NONE														T12	P13	Y15				
IOT4A	I/O	3		True_of_IOT4B	NONE	x16																C19				
IOT4B	I/O	3		Comp_of_IOT4A	NONE	NONE																B20				
IOT5A/MODE0	I/O	3	MODE0	True_of_IOT5B	NONE	NONE	GND[1]	GND[1]	GND[1]	88	100	GND[1]	144	144	B1	GND[1]	174	174	GND[1]	GND[1]	M16	C17	48	GND[1]	GND[1]	GND[1]
IOT5B/MODE2	I/O	3	MODE2	Comp_of_IOT5A	NONE	NONE	48	GND[1]	GND[1]	GND[1]	GND[1]	GND[1]	GND[1]	GND[1]	A2	GND[1]	173	173	GND[1]	GND[1]	C15	D17	GND[1]	GND[1]	60	GND[1]
IOT6A	I/O	3		True_of_IOT6B	NONE	x16																F16				
IOT6B/MODE1	I/O	3	MODE1	Comp_of_IOT6A	NONE	NONE	48	GND[1]	GND[1]	87	GND[1]	D4	143	143	A3	GND[1]	172	172	GND[1]	GND[1]	B16	E17	GND[1]	D4	60	87
IOT7A	I/O	3		True_of_IOT7B	NONE	NONE																D18				
IOT7B	I/O	3		Comp_of_IOT7A	NONE	NONE																B19				
IOT8A	I/O	3		True_of_IOT8B	NONE	x16		A8		86	99		142	142	B3		171	171				D19		A3		
IOT8B	I/O	3		Comp_of_IOT8A	NONE	NONE		B8		85	98		141	141	B4		170	170				C20		A4		
IOT9A	I/O	3		True_of_IOT9B	NONE	NONE															D16	E18				
IOT9B	I/O	3		Comp_of_IOT9A	NONE	NONE															E14	F18				
VCC	Power	N/A					12	E5	H2	22	25	J2	36	36		F7	44	44					12	J2	31	45
VCC	Power	N/A					37	D4	A8	66	75	A8	108	108		G6	132	132					37	A8	45	22
VCC	Power	N/A							B2	1	1	A2	1	1		G8	1	1						A2	1	1
VCC	Power	N/A							B9	45	51		73	73		H7	89	89							16	66
VCC	Power	N/A							H8						A1				E10	A1	A1	J10				
VCC	Power	N/A													A14				E5	A16	A16	J11				
VCC	Power	N/A													P1				E6	G7	G7	K9				
VCC	Power	N/A													P14				E9	G10	G10	K12				
VCC	Power	N/A																	F10	K7	K7	L9				
VCC	Power	N/A																	F5	K10	K10	L12				
VCC	Power	N/A																	F6	T1	T1	M10				
VCC	Power	N/A																	F9	T16	T16	M11				
VCC	Power	N/A																	J5							
VCC	Power	N/A																	J6							
VCC	Power	N/A																	J9							
VCC	Power	N/A																	K10							
VCC	Power	N/A																	K5							
VCC	Power	N/A																	K6							
VCC	Power	N/A																	K9							
VCCIO0	Power	N/A							F5	67	76	A5	109	109		C6	133	133					47	A5	46	
VCCIO0	Power	N/A									88		127	127		C7	155	155							55	
VCCIO0	Power	N/A													C11	C8			C4	H10	H10	K13				

Note!
[1] The pin is internally grounded.
[2] LV Version.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	QN48	CM64	CS81M	QN88	LQ100	MG100	LQ144	EQ144	MG160	UG169	LQ176	EQ176	MG196	UG256	PG256	UG332	QN48F	MG100T	QN60[2]	QN88F[2]
VCCIO0	Power	N/A													C4				C10	E13	E13	J13				
VCCIO0	Power	N/A															176	176								
VCCIO0	Power	N/A																	C5	J10	J10	L13				
VCCIO0	Power	N/A																	C9	M13	M13					
VCCIO0/VCCIO2	Power	N/A						C6																		
VCCIO0/VCCIO3	Power	N/A					1																			
VCCIO1	Power	N/A							E6	58	63	E9	91	91			115	115						E9	38	58
VCCIO1	Power	N/A									71		103	103		F11										64
VCCIO1	Power	N/A													D12	G11			D12	K9		N9				
VCCIO1	Power	N/A													L12	H11			E12	K8	K8	N10				
VCCIO1	Power	N/A														J11	95	95								
VCCIO1	Power	N/A															110	110								
VCCIO1	Power	N/A																	G11	N12	N12	N11				
VCCIO1	Power	N/A																	G12	N5	N5	N12				
VCCIO1	Power	N/A																	K11							
VCCIO1	Power	N/A																	K12							
VCCIO1/VCCIO2	Power	N/A					25																25			
VCCIO1/VCCIO3	Power	N/A						F3																		
VCCIO2	Power	N/A							D5	23	26	J5	37	37		L6	45	45						J5	24	44
VCCIO2	Power	N/A								44						L7	88	88								23
VCCIO2	Power	N/A									38		55	55		L8	65	65								
VCCIO2	Power	N/A													M11				M5	J7	J7	K5				
VCCIO2	Power	N/A													M4				M10	H7	H7	J8				
VCCIO2	Power	N/A																	M6	M4	M4	K8				
VCCIO2	Power	N/A																	M9			L8				
VCCIO2	Power	N/A																		E4	E4	M8				
VCCIO3	Power	N/A							E4	12													1	E1	5	12
VCCIO3	Power	N/A									4	E1	5	5		F2	13	13							11	4
VCCIO3	Power	N/A									13		19	19		G3	22	22								
VCCIO3	Power	N/A													D3	J3			E3	G9	G9	H11				
VCCIO3	Power	N/A													L3	K3			E4	D12	D12	H12				
VCCIO3	Power	N/A															34	34								
VCCIO3	Power	N/A																	G3	D5	D5	H9				
VCCIO3	Power	N/A																	H3							
VCCIO3	Power	N/A																	K3							
VCCIO3	Power	N/A																	K4							
VCCIO0/VCCX	Power	N/A																								67
VCCIO0/VCCX	Power	N/A																								78
VCCX	Power	N/A					36	C3	B1	64						D10	130	130					36	J8	33	
VCCX	Power	N/A						F6	J1		21	J8	31	31		D3	40	40							15	
VCCX	Power	N/A							B8	78						D4	154	154								
VCCX	Power	N/A							J9		54		77	77		K4										
VCCX	Power	N/A													C13	K9			L7							
VCCX	Power	N/A													C2				K7							
VCCX	Power	N/A													M13				H6	G8	G8	M13				
VCCX	Power	N/A													M2				H5		K9	H10				
VCCX	Power	N/A															66	66								
VCCX	Power	N/A																	D7							
VCCX	Power	N/A																	E7							
VCCX	Power	N/A																	G10							
VCCX	Power	N/A																	G9							
VSS	Ground	N/A					2		H9	2	2	A1	2	2		A1	2	2					26	A1	4	2
VSS	Ground	N/A					26		H5	46	52	A9	74	74		A13	90	90					2	A9	17	21
VSS	Ground	N/A						D5	H1		24	J1	35	35		B8	43	43						J1	32	24
VSS	Ground	N/A						E4	F6		J9					C3	134	134						J9		43
VSS	Ground	N/A							F4	21			33	33		D2										46
VSS	Ground	N/A							E9	24						D5	46	46								65
VSS	Ground	N/A							E5	43						E11	87	87								
VSS	Ground	N/A							D7	65	74					E2										
VSS	Ground	N/A							D1		37					F3										
VSS	Ground	N/A							B4		87					G7										

Note!
[1] The pin is internally grounded.
[2] LV Version.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	QN48	CM64	CS81M	QN88	LQ100	MG100	LQ144	EQ144	MG160	UG169	LQ176	EQ176	MG196	UG256	PG256	UG332	QN48F	MG100T	QN60[2]	QN88F[2]
VSS	Ground	N/A							A9				17	17		H12										
VSS	Ground	N/A							A1				53	53		J4										
VSS	Ground	N/A											89	89		L9										
VSS	Ground	N/A											105	105		M6										
VSS	Ground	N/A											107	107		N1	131	131								
VSS	Ground	N/A													B13	N13			A14	C3	C3	A10				
VSS	Ground	N/A													B2				A1	B15	B15	A1				
VSS	Ground	N/A													C12				C3	D4	D4	C3				
VSS	Ground	N/A													C3				C2	C14	C14	A20				
VSS	Ground	N/A													D11				C7	E5	E5	E11				
VSS	Ground	N/A													D4				C6	D13	D13	C18				
VSS	Ground	N/A													L11				D5	F6	F6	H13				
VSS	Ground	N/A													L4				D10	E12	E12	H8				
VSS	Ground	N/A													M12				D9	H8	H8	J12				
VSS	Ground	N/A													M3				D6	F11	F11	J9				
VSS	Ground	N/A													N13				E8	J8	J8	K11				
VSS	Ground	N/A													N2				E11	H9	H9	K10				
VSS	Ground	N/A															175	175								
VSS	Ground	N/A																	F7	J9	J9	K20				
VSS	Ground	N/A																	F8	L6	L6	L5				
VSS	Ground	N/A																	G4							
VSS	Ground	N/A																	G5	L11	L11	L10				
VSS	Ground	N/A																	G6	M5	M5	L11				
VSS	Ground	N/A																	G7	M12	M12	L16				
VSS	Ground	N/A																	G8	N4	N4	M9				
VSS	Ground	N/A																	H10	N13	N13	M12				
VSS	Ground	N/A																	H4	P3	P3	N8				
VSS	Ground	N/A																	H7	P14	P14	N13				
VSS	Ground	N/A																	H8	R2	R2	T10				
VSS	Ground	N/A																	H9	R15	R15	V3				
VSS	Ground	N/A																	J10	B2	B2	V18				
VSS	Ground	N/A																	J7			Y1				
VSS	Ground	N/A																	J8			Y11				
VSS	Ground	N/A																	K8			Y20				
VSS	Ground	N/A																	L10							
VSS	Ground	N/A																	L11							
VSS	Ground	N/A																	L3							
VSS	Ground	N/A																	L5							
VSS	Ground	N/A																	L6							
VSS	Ground	N/A																	L9							
VSS	Ground	N/A																	M11							
VSS	Ground	N/A																	M3							
VSS	Ground	N/A																	M7							
VSS	Ground	N/A																	P1							
VSS	Ground	N/A																	P14							
NC	N/A	N/A																				A2				
NC	N/A	N/A																				B2				
NC	N/A	N/A																				G1				
NC	N/A	N/A																				H3				
NC	N/A	N/A																				N18				
NC	N/A	N/A																				P20				

Note!
[1] LV Version.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	QN48	CM64	CS81M	QN88	LQ100	MG100	LQ144	EQ144	MG160	UG169	LQ176	EQ176	MG196	UG256	PG256	UG332	QN48F	MG100T	QN60[1]	QN88F[1]
BANK3 True LVDS Pair																										
IOL11A/TMS	I/O	3	TMS	True_of_IOL11B	TRUE	NONE	4	D7	D3	5	8	E2	13	13	F1	G1	16	16	B14	B8	B8	C9	4	E2	9	5
IOL11B/TCK	I/O	3	TCK	Comp_of_IOL11A	TRUE	NONE	5	D6	D4	6	9	E3	14	14	G1	G2	17	17	B13	A7	A7	A8	5	E3	8	6
IOL13A/TDO	I/O	3	TDO	True_of_IOL13B	TRUE	NONE	7	E6	E2	8	12	F2	18	18	G3	F6	20	20	C14	C6	C6	C7	8	F2	12	8
IOL13B/RECONFIG_N	I/O	3	RECONFIG_N	Comp_of_IOL13A	TRUE	NONE	8			9	14	D3	20	20	H3		21	21		B10	B10	A14	9	D3		9
IOL15A/GCLKT_6	I/O	3	GCLKT_6	True_of_IOL15B	TRUE	NONE	10	D8	F2		17	F1	23	23	J2	H4	24	24	G2	C8	C8	D12	10		14	10
IOL15B/GCLKC_6	I/O	3	GCLKC_6	Comp_of_IOL15A	TRUE	NONE	11	E8	F1		18	D1	24	24	J3	H5	25	25	G1	A8	A8	C12	11	F1	13	11
IOL17A	I/O	3		True_of_IOL17B	TRUE	NONE									H1	G4	26	26	J2	D8		D11				
IOL17B	I/O	3		Comp_of_IOL17A	TRUE	NONE									K3	F4	27	27	J1	E9		C11				
IOL20A	I/O	3		True_of_IOL20B	TRUE	NONE					19	D2			J1	H3	28	28	J4	F7	F8	E10				13
IOL20B	I/O	3		Comp_of_IOL20A	TRUE	NONE					20	G2			K1	H2	29	29	J3	E8	D9	D10				14
IOL22A	I/O	3		True_of_IOL22B	TRUE	NONE		F8	C1	13			25	25	K2	J2	30	30	K2	E6	B7	E12				15
IOL22B	I/O	3		Comp_of_IOL22A	TRUE	NONE		F7	C2	14			26	26	L2	J1	31	31	K1	D7	C7	B9				16
IOL24A	I/O	3		True_of_IOL24B	TRUE	NONE						G1				M2	32	32		A4	C4	A9				17
IOL24B	I/O	3		Comp_of_IOL24A	TRUE	NONE						H2				M1	33	33		C5	B5	B8				18
IOL26A	I/O	3		True_of_IOL26B	TRUE	NONE				15			27	27		L3				A5		D8				19
IOL26B	I/O	3		Comp_of_IOL26A	TRUE	NONE				16			28	28		M3				B6		E8				20
IOL2A	I/O	3		True_of_IOL2B	TRUE	NONE									C1	C2	3	3		B11	B14	A18				88
IOL2B	I/O	3		Comp_of_IOL2A	TRUE	NONE									D2	D1	4	4		A12	A15	A17				3
IOL4A	I/O	3		True_of_IOL4B	TRUE	NONE									D1	E4	7	7	E2	B13	B11	C16				
IOL4B	I/O	3		Comp_of_IOL4A	TRUE	NONE									E1	E3	8	8	E1	A14	A12	B16				
IOL6A/LPLL_T_fb	I/O	3	LPLL_T_fb	True_of_IOL6B	TRUE	NONE						B2			E4	B1	11	11	F4	D10	B13	A16				
IOL6B/LPLL_C_fb	I/O	3	LPLL_C_fb	Comp_of_IOL6A	TRUE	NONE						C1	6	6	F4	C1	12	12	F3	E10	A14	A15				
IOL8A	I/O	3		True_of_IOL8B	TRUE	NONE			G3				9	9	H4	E1			F2	A9	D10	B15				
IOL8B	I/O	3		Comp_of_IOL8A	TRUE	NONE			F3				10	10	K4	F1			F1	B9	E10	C14				
BANK2 True LVDS Pair																										
IOB11A	I/O	2		True_of_IOB11B	TRUE	x16				27	29	J3	42	42	L5	M7	51	51	N2	B1	B1	B1		J3	18	27
IOB11B	I/O	2		Comp_of_IOB11A	TRUE	NONE				28	30	H3	43	43	M5	N6	52	52	P2	C2	C2	C2		H3	19	28
IOB13A	I/O	2		True_of_IOB13B	TRUE	x16		H7		29	31	E4	46	46	N4	N8	53	53		E2	E2	G5		E4	20	29
IOB13B	I/O	2		Comp_of_IOB13A	TRUE	NONE		G7		30	32	F4	47	47	P4	N7	54	54		E3	E3	H5		F4	21	30
IOB15A	I/O	2		True_of_IOB15B	TRUE	x16					33	K3	48	48	N5	K6	55	55	N3	F4	F4	G4		K3	22	31
IOB15B	I/O	2		Comp_of_IOB15A	TRUE	NONE					34	K4	49	49	P5	J6	56	56	P3	G6	G6	F3		K4	23	32
IOB17A	I/O	2		True_of_IOB17B	TRUE	x16	15	H6	C4	31	35	J4	50	50	L6	M9	57	57		G5	G5	G3	15	J4		33
IOB17B	I/O	2		Comp_of_IOB17A	TRUE	NONE	16	G6	C3	32	36	H4	51	51	M6	M8	58	58		G4	G4	H4	16	H4		34
IOB21A	I/O	2		True_of_IOB21B	TRUE	x16						K5			L7	K7	61	61	L4			H2		K5		35
IOB21B	I/O	2		Comp_of_IOB21A	TRUE	NONE						K6			M7	J7	62	62	M4			H1		K6		36
IOB23A	I/O	2		True_of_IOB23B	TRUE	x16		H5	B3	33		H5	52	52	N6	N12	63	63	N4	F5	F5	K4		H5		37
IOB23B	I/O	2		Comp_of_IOB23A	TRUE	NONE		G5	A2	34		G5	54	54	P6	N11	64	64	P4	H6	H6	K3		G5		38
IOB25A	I/O	2		True_of_IOB25B	TRUE	x16									L9		67	67	N5			K1				40
IOB25B	I/O	2		Comp_of_IOB25A	TRUE	NONE									M9		68	68	P5			L1				39
IOB27A	I/O	2		True_of_IOB27B	TRUE	x16	17	H4	A3						N8		69	69	N6	H4	H4	L2	17		25	
IOB27B	I/O	2		Comp_of_IOB27A	TRUE	NONE	18	G4	C5						P8		70	70	P6	J6	J6	M1	18		26	
IOB29A/GCLKT_4	I/O	2	GCLKT_4	True_of_IOB29B	TRUE	x16	19	F5	D6	35	41	J6	58	58	L8	M12	71	71	N8	L2	L2	M5	19	J6	28	42
IOB29B/GCLKC_4	I/O	2	GCLKC_4	Comp_of_IOB29A	TRUE	NONE	20	F4	C6	36	42	H6	59	59	M8	M13	72	72	P8	M1	M1	M4	20	H6	27	41
IOB2A	I/O	2		True_of_IOB2B	TRUE	x16				17						L4	36	36				C6				
IOB2B	I/O	2		Comp_of_IOB2A	TRUE	NONE				18						L5	37	37				D7				
IOB31A	I/O	2		True_of_IOB31B	TRUE	x16				37	43	K7	62	62	N9		73	73	L8	J2	J2	N3	21	K7		
IOB31B	I/O	2		Comp_of_IOB31A	TRUE	NONE				38	44	K8	63	63	P9		74	74	M8	K1	K1	N4	22	K8		
IOB33A	I/O	2		True_of_IOB33B	TRUE	x16		H3	A4	39	45	J7	64	64	L10		75	75	N9	K3	K3	P2		J7		
IOB33B	I/O	2		Comp_of_IOB33A	TRUE	NONE		G3	B5	40	46	H7	65	65	M10		76	76	P9	K2	K2	P3		H7		
IOB35A	I/O	2		True_of_IOB35B	TRUE	x16	21		A6		47	F6	66	66	N10	N9	79	79	N10	L1	L1	P4	24	F6		
IOB35B	I/O	2		Comp_of_IOB35A	TRUE	NONE	22		A5		48	G6	67	67	P10	N10	80	80	P10	L3	L3	R3	23	G6		
IOB39A	I/O	2		True_of_IOB39B	TRUE	x16	23	H2	A7		49	F7	70	70	P11		83	83	N11	M3	M3	V1		F7	30	48
IOB39B	I/O	2		Comp_of_IOB39A	TRUE	NONE	24	G2	B6		50	G7	71	71	N11		84	84	P11	N1	N1	U2		G7	29	47
IOB41A	I/O	2		True_of_IOB41B	TRUE	x16		H1		41		K10	72	72	P12	L11	85	85	N12	R1	R1	U3		K10		
IOB41B	I/O	2		Comp_of_IOB41A	TRUE	NONE		G1		42		K9			N12	M11	86	86	P12	P2	P2	V2		K9		
IOB43A	I/O	2		True_of_IOB43B	TRUE	x16					55		78	78	M14	K8	94	94	L12		T2	W2				
IOB43B	I/O	2		Comp_of_IOB43A	TRUE	NONE					53		76	76	N14	J8	93	93	M12		R3	W1				

Note!
[1] LV Version.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	QN48	CM64	CS81M	QN88	LQ100	MG100	LQ144	EQ144	MG160	UG169	LQ176	EQ176	MG196	UG256	PG256	UG332	QN48F	MG100T	QN60[1]	QN88F[1]
IOB45A	I/O	2		True_of_IOB45B	TRUE	x16									J13	L10	99	99	N13		T3	U5				
IOB45B	I/O	2		Comp_of_IOB45A	TRUE	NONE									L13	M10	98	98	P13		R4	V4				
IOB4A	I/O	2		True_of_IOB4B	TRUE	x16				19		K1	29	29	L1	M5	38	38	L2			D6		K1		
IOB4B	I/O	2		Comp_of_IOB4A	TRUE	NONE				20		K2	30	30	M1	M4	39	39	L1			E7		K2		
IOB6A	I/O	2		True_of_IOB6B	TRUE	x16					22		32	32	N1	J5	41	41			A4	E6				
IOB6B	I/O	2		Comp_of_IOB6A	TRUE	NONE					23		34	34	P2	K5	42	42			C5	F5				
IOB8A	I/O	2		True_of_IOB8B	TRUE	x16	13	H8		25	27	G4	38	38	N3	N5	47	47	M2		A3	C4	13	G4		26
IOB8B	I/O	2		Comp_of_IOB8A	TRUE	NONE	14	G8		26	28	G3	39	39	P3	N4	48	48	M1		B4	A3	14	G3		25
BANK1 True LVDS Pair																										
IOR11A/MI/D7	I/O	1	MI/D7	True_of_IOR11B	TRUE	NONE	34			62	68	G9	96	96	F14	H9	122	122		M9	P10	W13			42	61
IOR11B/MO/D6	I/O	1	MO/D6	Comp_of_IOR11A	TRUE	NONE	33			61	67	F9	95	95	G14	H8	121	121		L10	R10	Y14			41	60
IOR13A/FASTRD_N/D3	I/O	1	FASTRD_N/D3	True_of_IOR13B	TRUE	NONE					64		92	92	G11	G13	118	118	J13	M8	R9	T11				
IOR13B/SI/D2	I/O	1	SI/D2	Comp_of_IOR13A	TRUE	NONE					62		90	90	G13	G12	117	117	J14	N9	T10	U11				
IOR15A/DIN/CLKHOLD_N	I/O	1	DIN/CLKHOLD_N	True_of_IOR15B	TRUE	NONE				54	59		86	86	H13	J13	113	113	H13	P8	T9	Y8				
IOR15B/DOUT/WE_N	I/O	1	DOUT/WE_N	Comp_of_IOR15A	TRUE	NONE				53	58		85	85	H12	H13	112	112	H14	T8	P9	W9				
IOR17A/GCLKT_3	I/O	1	GCLKT_3	True_of_IOR17B	TRUE	NONE	30	E3	D8	52	57	F8	84	84	J14	G9	111	111	H11	T7	T7	V9	30	F8		56
IOR17B/GCLKC_3	I/O	1	GCLKC_3	Comp_of_IOR17A	TRUE	NONE	29	D3	D9	51	56	G8	83	83	K14	G10			H12	R8	R8	W8	29	G8		55
IOR20A	I/O	1		True_of_IOR20B	TRUE	NONE						H8				J9			J11	R7	P8	V8				54
IOR20B	I/O	1		Comp_of_IOR20A	TRUE	NONE						G10				H10			J12	P7	T8	U9				53
IOR22A	I/O	1		True_of_IOR22B	TRUE	NONE		E1	C8				82	82	E11	K12	109	109	K13	P6	M7	Y5				52
IOR22B	I/O	1		Comp_of_IOR22A	TRUE	NONE		E2	C9	50			81	81	F11	J12	108	108	K14	T6	N7	Y4				51
IOR24A	I/O	1		True_of_IOR24B	TRUE	NONE	28	F1	F8	49		H9	80	80	J12	K11	107	107	L13	T3	N6	W5	28		37	50
IOR24B	I/O	1		Comp_of_IOR24A	TRUE	NONE	27	F2	F9	48		H10	79	79	H11	L12	106	106	L14	R4	L7	V6	27		36	49
IOR26A	I/O	1		True_of_IOR26B	TRUE	NONE									K12	K10	105	105	M13	T2		Y3			35	
IOR26B	I/O	1		Comp_of_IOR26A	TRUE	NONE									K11	J10	104	104	M14	R3		W4			34	
IOR2A	I/O	1		True_of_IOR2B	TRUE	NONE						C10				D12			C12	R13						
IOR2B	I/O	1		Comp_of_IOR2A	TRUE	NONE						B10				D11			C13	T14						
IOR4A	I/O	1		True_of_IOR4B	TRUE	NONE			G8							B13			E13	P12	R13	T14				
IOR4B	I/O	1		Comp_of_IOR4A	TRUE	NONE			G9							A12			E14	T13	T14	T13				
IOR6A/RPLL_T_fb	I/O	1	RPLL_T_fb	True_of_IOR6B	TRUE	NONE		D1					102	102	D14	B12	127	127	F11	T11	P12	Y13				
IOR6B/RPLL_C_fb	I/O	1	RPLL_C_fb	Comp_of_IOR6A	TRUE	NONE		D2					101	101	E14	B11	126	126	F12	P11	T13	Y12				
IOR8A	I/O	1		True_of_IOR8B	TRUE	NONE			G7				100	100	D13	F9			G13	P10	T11	U12				63
IOR8B	I/O	1		Comp_of_IOR8A	TRUE	NONE			F7				99	99	E13	F10			G14	R10	P11	V11				62

Note!
VCCX should be greater than or equal to VCCIO.

Recommended Operating Conditions of QN48 Package in GW1N-9				
Name	**Description**		**Min.**	**Max.**
VCC	LV: Core voltage		1.14V	1.26V
	UV: Core voltage		1.71V	3.6V
VCCIO1/VCCIO2	VCCIO1 and VCCIO2 are internally short-circuited.	LV: I/O Bank voltage	1.14V	3.6V
		UV: I/O Bank voltage	1.14V	3.6V
		When MIPI output is used in BANK2, VCCIO2 should provide 1.2V voltage.	1.14V	1.26V
VCCIO0/VCCIO3	VCCIO0 and VCCIO3 are internally short-circuited.	LV: I/O Bank voltage	1.14V	3.6V
		UV: I/O Bank voltage	1.14V	3.6V
VCCX	Auxiliary voltage		2.375V	3.6V

Note !
It is highly recommended that the epad connect to GND, but not a requirement.

Recommended Operating Conditions of CM64 Package in GW1N-9				
Name	**Description**		**Min.**	**Max.**
VCC	LV: Core voltage		1.14V	1.26V
	UV: Core voltage		1.71V	3.6V
VCCIO0/VCCIO2	VCCIO0 and VCCIO2 are internally short-circuited.	LV: I/O Bank voltage	1.14V	3.6V
		UV: I/O Bank voltage	1.14V	3.6V
		When MIPI output is used in BANK2, VCCIO2 should provide 1.2V voltage.	1.14V	1.26V
VCCIO1/VCCIO3	VCCIO1 and VCCIO3 are internally short-circuited.	LV: I/O Bank voltage	1.14V	3.6V
		UV: I/O Bank voltage	1.14V	3.6V
VCCX	Auxiliary voltage		2.375V	3.6V

Recommended Operating Conditions of CS81M/MG100/MG100T Packages in GW1N-9			
Name	**Description**	**Min.**	**Max.**
VCC	Core voltage	1.14V	1.26V
VCCIO0, VCCIO1, VCCIO2, VCCIO3	I/O Bank voltage	1.14V	3.6V
	When MIPI output is used in BANK2, VCCIO2 should provide 1.2V voltage.	1.14V	1.26V
VCCX	Auxiliary voltage	2.375V	3.6V

Note!
VCCX should be greater than or equal to VCCIO.

Recommended Operating Conditions of QN48F Package in GW1N-9

Name	Description		Min.	Max.
VCC	Core voltage		1.14V	1.26V
VCCIO0, VCCIO3	I/O Bank voltage		1.14V	3.6V
VCCIO1/VCCIO2	VCCIO1 and VCCIO2 are internally short-circuited.	I/O Bank voltage	1.14V	3.6V
		When MIPI output is used in BANK2, VCCIO2 should provide 1.2V voltage.	1.14V	1.26V
VCCX	Auxiliary voltage		2.375V	3.6V

Note !
It is highly recommended that the epad connect to GND, but not a requirement.

Recommended Operating Conditions of QN60 Package in GW1N-9

Name	Description	Min.	Max.
VCC	LV: Core voltage	1.14V	1.26V
VCCIO0, VCCIO1, VCCIO2, VCCIO3	LV: I/O Bank voltage	1.14V	3.6V
	When MIPI output is used in BANK2, VCCIO2 should provide 1.2V voltage.	1.14V	1.26V
VCCX	Auxiliary voltage	2.375V	3.6V

Note !
It is highly recommended that the epad connect to GND, but not a requirement.

Recommended Operating Conditions of QN88F Package in GW1N-9

Name	Description	Min.	Max.
VCC	LV: Core voltage	1.14V	1.26V
VCCIO1, VCCIO2 VCCIO3	LV: I/O Bank voltage	1.14V	3.6V
	When MIPI output is used in BANK2, VCCIO2 should provide 1.2V voltage.	1.14V	1.26V
VCCIO0/VCCX	Auxiliary voltage VCCX and VCCIO0 are internally short-circuited.	2.375V	3.6V

Note !
It is highly recommended that the epad connect to GND, but not a requirement.

Note! VCCX should be greater than or equal to VCCIO.			
Recommended Operating Conditions of Other Packages in GW1N-9			
Name	**Description**	**Min.**	**Max.**
VCC	LV: Core voltage	1.14V	1.26V
	UV: Core voltage	1.71V	3.6V
VCCIO0, VCCIO1, VCCIO2, VCCIO3	LV: I/O Bank voltage	1.14V	3.6V
	UV: I/O Bank voltage	1.14V	3.6V
	When MIPI output is used in BANK2, VCCIO2 should provide 1.2V voltage.	1.14V	1.26V
VCCX	Auxiliary voltage	2.375V	3.6V