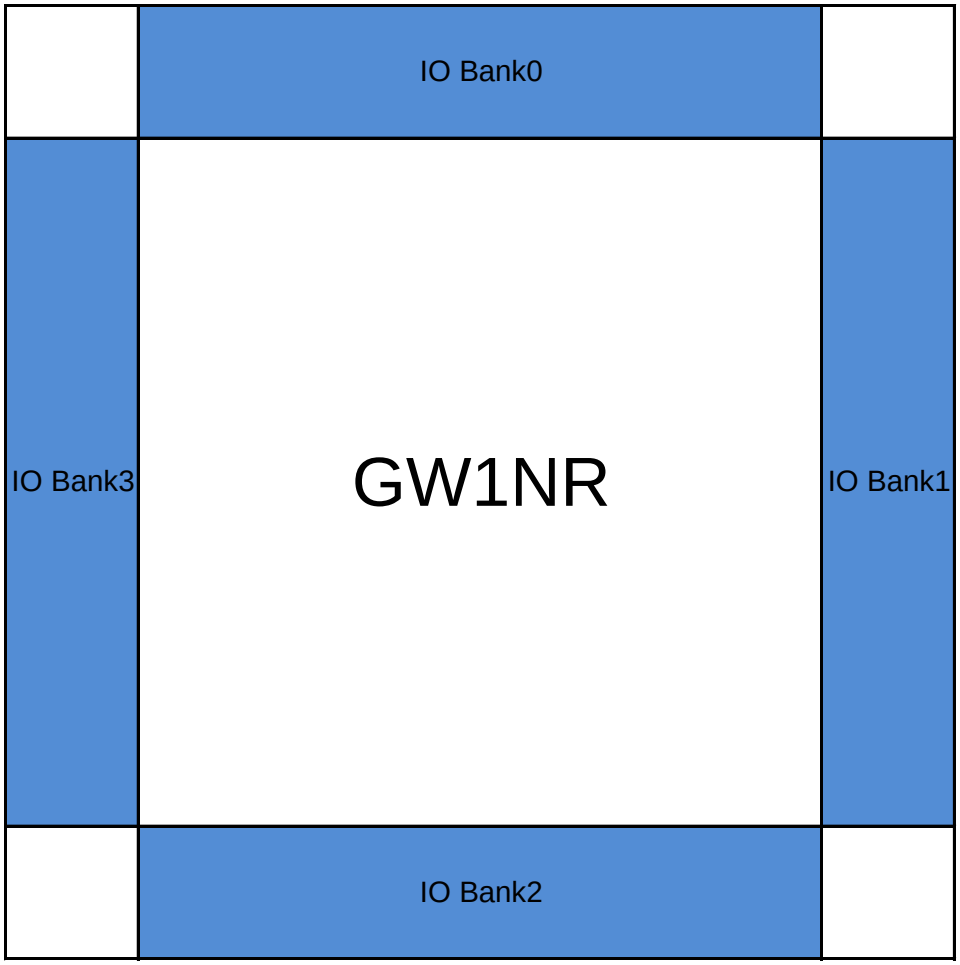
Date	Version	Description
02/09/2017	1.00E	Initial version published.
04/10/2017	1.01E	Pin 81 changed from IOT6B to IOT7A。
06/09/2017	1.02E	The location of MO/MI modified.
05/28/2018	1.03E	Multiplexing pins modified. GCLK[n]_[x], RPLL_[n]_fb, and RPLL_[n]_in are divided into GCLKT_[x] GCLKC_[x], LPLL_T_fb/RPLL_T_fb LPLL_C_fb/RPLL_C_fb, and LPLL_T_in/RPLL_T_in LPLL_C_in/RPLL_C_in. The descriptions of MODE modified. MODE is no longer used as a dedicated pin and can be multiplexed as GPIO.
06/19/2018	1.04E	The info. of package MG81 added.
11/26/2018	1.05E	Recommended operating conditions added.
01/08/2021	1.06E	The info. of package QN88 embedded with PSRAM added.
10/20/2022	1.1E	Pin definitions updated. The note in Power sheet updated.
05/04/2023	1.1.1E	QN88 package embedded with PSRAM renamed to QN88P; MG81 package renamed to MG81P. The description of CLKHOLD_N pin in Pin Definitions sheet updated. The note of QN88/QN88P package in Power sheet added.
06/30/2023	1.1.2E	The descriptions of pin definitions and info. for MODE0, MODE1, MODE2 pins optimized.
11/30/2023	1.1.3E	The I/O descriptions of Ready and Done pins in Pin Definitions sheet optimized. The Min. value of IO Bank power supply voltage in Power sheet updated.

Pin Name	I/O	Description
User I/O		
IO[End][Row/Column Number][A/B]	I/O	[End] indicates the pin location, including L(left), R(right), B(bottom), and T(top).
		[Row/Column Number] indicates the pin row/column number. If [End] is T(top) or B(bottom), the pin indicates the column number of the corresponding CFU. If [End] is L(left) or R(right), the pin indicates the row number of the corresponding CFU.
		[A/B] indicates differential signal pair information.
Multi-Function Pins		
IO[End][Row/Column Number][A/B]/MMM		/MMM represents one or more of the other functions in addition to being general purpose user I/O. When these functions are not in use, these pins can be used as user I/O.
D0	I/O	Data port D0 in CPU mode
D1	I/O	Data port D1 in CPU mode
D2	I/O	Data port D2 in CPU mode
D3	I/O	Data port D3 in CPU mode
D4	I/O	Data port D4 in CPU mode
D5	I/O	Data port D5 in CPU mode
D6	I/O	Data port D6 in CPU mode
D7	I/O	Data port D7 in CPU mode
WE_N	I	Select data input/output of D[7:0] in CPU mode.0: Write;1: Read.
DOUT	O	Data output in SERIAL mode
DIN	I, internal weak pull-up	Data input in SERIAL mode
TMS	I, internal weak pull-up	Serial mode input in JTAG mode
TCK	I	Serial clock input in JTAG mode
TDO	O	Serial data output in JTAG mode
TDI	I, internal weak pull-up	Serial data input in JTAG mode
JTAGSEL_N	I, internal weak pull-up	Reconfigure JTAG download function signal
RECONFIG_N	I, internal weak pull-up	Global reset GowinCONFIG logic signal, active low
FASTRD_N	I	Access SPI FLASH to select signal. Low, Fast Read mode; High, Read mode.
DONE[1]	O, internal weak pull-up	High, the programming configuration has been completed successfully; Low, the programming configuration has not been completed or failed.
	I, internal weak pull-up	When the DONE signal is low, delay the chip to activate. Activate the chip until the DONE signal is high.
READY[1]	I/O, internal weak pull-up	High, the device can be programmed and configured currently; Low, the device cannot be programmed and configured currently.
MI	I	MI in MSPI mode

Pin Name	I/O	Description
MO	O	MO in MSPI mode
MCS_N	O	Enable signal MCS_N in MSPI mode, active-low
MCLK	O	Clock output MCLK in MSPI mode, with default frequency of 2.5Mhz
SCLK	I	Clock input in SSPI, SERIAL, and CPU modes
SO	O	SO in SSPI mode
SI	I/O	SI in SSPI mode
SSPI_CS_N	I/O	Enable signal SSPI_CS_N in SSPI mode, active-low, and internal weak pull-up
CLKHOLD_N	I, internal weak pull-up	Active-high in SSPI mode; Active-low in CPU mode.
GCLKC_[x]	I	Differential input pin of GCLKT_[x], C(Comp), [x]: global clock No.[2]
GCLKT_[x]	I	Global clock input pin, T(True), [x]: global clock No.
LPLL_C_fb/RPLL_C_fb	I	Left/Right PLL feedback input pin, C(Comp)
LPLL_T_fb/RPLL_T_fb	I	Left/Right PLL feedback input pin, T(True)
LPLL_C_in/RPLL_C_in	I	Left/Right PLL clock input pin, C(Comp)
LPLL_T_in/RPLL_T_in	I	Left/Right PLL clock input pin, T(True)
MODE2	I, internal weak pull-up	GowinCONFIG modes selection pin; if this pin is marked as “VCCIO”, it's internally powered; if this pin is marked as "GND", it's internally grounded.
MODE1	I, internal weak pull-up	GowinCONFIG modes selection pin; if this pin is marked as “VCCIO”, it's internally powered; if this pin is marked as "GND", it's internally grounded.
MODE0	I, internal weak pull-up	GowinCONFIG modes selection pin; if this pin is marked as “VCCIO”, it's internally powered; if this pin is marked as "GND", it's internally grounded.
Other Pins		
NC	NA	Reserved
VSS	NA	Ground
VCC	NA	Power supply pin of core voltage
VCCIO#	NA	Power supply pin of I/O voltage for I/O BANK#
VCCX	NA	Power supply pin of auxiliary voltage

Note!
[1] The default state of READY/DONE is open-drain output, internal weak pull-up. DONE outputs 0 during configuration.
[2] When the input is single-ended, GCLKC_[x] pin is not a global clock.



Note!

[1] Each Bank has independent reference voltage (VREF).

[2] You can select to use IOB internal VREF (equals to 0.5 X VCCIO).

[3] You can also select to use external VREF input (use any IO pins as external VREF input).

Note!
[1] SDRAM embedded
[2] PSRAM embedded
[3] The pin is internally grounded.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	QN88[1]	QN88P[2]	MG81P[2]
IOB10A	I/O	2		True_of_IOB10B	NONE	29	29	
IOB10B	I/O	2		Comp_of_IOB10A	NONE	30	30	
IOB11A	I/O	2		True_of_IOB11B	NONE			
IOB11B	I/O	2		Comp_of_IOB11A	NONE			
IOB12A	I/O	2		True_of_IOB12B	TRUE	31	31	E4
IOB12B	I/O	2		Comp_of_IOB12A	TRUE	32	32	F4
IOB13A	I/O	2		True_of_IOB13B	NONE			
IOB13B	I/O	2		Comp_of_IOB13A	NONE			
IOB14A	I/O	2		True_of_IOB14B	TRUE	33	33	J4
IOB14B	I/O	2		Comp_of_IOB14A	TRUE			H4
IOB15A	I/O	2		True_of_IOB15B	NONE	34	34	
IOB15B	I/O	2		Comp_of_IOB15A	NONE			
IOB16A	I/O	2		True_of_IOB16B	TRUE			
IOB16B	I/O	2		Comp_of_IOB16A	TRUE			
IOB17A	I/O	2		True_of_IOB17B	NONE			
IOB17B	I/O	2		Comp_of_IOB17A	NONE			
IOB18A	I/O	2		True_of_IOB18B	TRUE			
IOB18B	I/O	2		Comp_of_IOB18A	TRUE			
IOB19A/GCLKT_5	I/O	2	GCLKT_5	True_of_IOB19B	NONE			
IOB19B/GCLKC_5	I/O	2	GCLKC_5	Comp_of_IOB19A	NONE			
IOB20A/GCLKT_4	I/O	2	GCLKT_4	True_of_IOB20B	TRUE	35	35	H5
IOB20B/GCLKC_4	I/O	2	GCLKC_4	Comp_of_IOB20A	TRUE	36	36	G5
IOB21A	I/O	2		True_of_IOB21B	NONE			
IOB21B	I/O	2		Comp_of_IOB21A	NONE			
IOB22A	I/O	2		True_of_IOB22B	TRUE			E6
IOB22B	I/O	2		Comp_of_IOB22A	TRUE			E5
IOB23A	I/O	2		True_of_IOB23B	NONE			
IOB23B	I/O	2		Comp_of_IOB23A	NONE			
IOB24A	I/O	2		True_of_IOB24B	TRUE			F6
IOB24B	I/O	2		Comp_of_IOB24A	TRUE			F5

Note!
[1] SDRAM embedded
[2] PSRAM embedded
[3] The pin is internally grounded.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	QN88[1]	QN88P[2]	MG81P[2]
IOB25A	I/O	2		True_of_IOB25B	NONE			
IOB25B	I/O	2		Comp_of_IOB25A	NONE			
IOB26A	I/O	2		True_of_IOB26B	TRUE			J6
IOB26B	I/O	2		Comp_of_IOB26A	TRUE	37	37	H6
IOB27A	I/O	2		True_of_IOB27B	NONE			
IOB27B	I/O	2		Comp_of_IOB27A	NONE	38	38	
IOB28A	I/O	2		True_of_IOB28B	NONE	39	39	
IOB28B	I/O	2		Comp_of_IOB28A	NONE	40	40	
IOB29A	I/O	2		True_of_IOB29B	NONE			
IOB29B	I/O	2		Comp_of_IOB29A	NONE			
IOB2A	I/O	2		True_of_IOB2B	TRUE	17	17	
IOB2B	I/O	2		Comp_of_IOB2A	TRUE	18	18	
IOB30A	I/O	2		True_of_IOB30B	TRUE	41	41	G6
IOB30B	I/O	2		Comp_of_IOB30A	TRUE	42	42	G7
IOB31A	I/O	2		True_of_IOB31B	NONE			
IOB31B	I/O	2		Comp_of_IOB31A	NONE			
IOB32A	I/O	2		True_of_IOB32B	TRUE			J7
IOB32B	I/O	2		Comp_of_IOB32A	TRUE			H7
IOB33A	I/O	2		True_of_IOB33B	NONE			
IOB33B	I/O	2		Comp_of_IOB33A	NONE			
IOB34A	I/O	2		True_of_IOB34B	TRUE			
IOB34B	I/O	2		Comp_of_IOB34A	TRUE			
IOB35A	I/O	2		True_of_IOB35B	NONE			
IOB35B	I/O	2		Comp_of_IOB35A	NONE			
IOB36A	I/O	2		True_of_IOB36B	TRUE			
IOB36B	I/O	2		Comp_of_IOB36A	TRUE	47	47	H8
IOB37A	I/O	2		True_of_IOB37B	NONE			
IOB37B	I/O	2		Comp_of_IOB37A	NONE			
IOB3A	I/O	2		True_of_IOB3B	NONE			
IOB3B	I/O	2		Comp_of_IOB3A	NONE			

Note!
[1] SDRAM embedded
[2] PSRAM embedded
[3] The pin is internally grounded.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	QN88[1]	QN88P[2]	MG81P[2]
IOB4A	I/O	2		True_of_IOB4B	TRUE	19	19	
IOB4B	I/O	2		Comp_of_IOB4A	TRUE	20	20	
IOB5A	I/O	2		True_of_IOB5B	NONE			
IOB5B	I/O	2		Comp_of_IOB5A	NONE			
IOB6A	I/O	2		True_of_IOB6B	TRUE	25	25	J3
IOB6B	I/O	2		Comp_of_IOB6A	TRUE	26	26	H3
IOB7A	I/O	2		True_of_IOB7B	NONE			
IOB7B	I/O	2		Comp_of_IOB7A	NONE			
IOB8A	I/O	2		True_of_IOB8B	TRUE	27	27	G3
IOB8B	I/O	2		Comp_of_IOB8A	TRUE	28	28	G4
IOB9A	I/O	2		True_of_IOB9B	NONE			
IOB9B	I/O	2		Comp_of_IOB9A	NONE			
IOL10A/TMS	I/O	3	TMS	True_of_IOL10B	NONE	5	5	E2
IOL10B/TCK	I/O	3	TCK	Comp_of_IOL10A	NONE	6	6	E3
IOL10C/SCLK	I/O	3	SCLK	True_of_IOL10D	NONE			
IOL10D/TDI	I/O	3	TDI	Comp_of_IOL10C	NONE	7	7	F3
IOL10E/TDO	I/O	3	TDO	True_of_IOL10F	NONE	8	8	F2
IOL10F/RECONFIG_N	I/O	3	RECONFIG_N	Comp_of_IOL10E	NONE	9	9	B2
IOL10G/DONE	I/O	3	DONE	True_of_IOL10H	NONE	10	10	B1
IOL10H/READY	I/O	3	READY	Comp_of_IOL10G	NONE			
IOL10I	I/O	3		True_of_IOL10J	NONE			
IOL10J	I/O	3		Comp_of_IOL10I	NONE			
IOL11A/GCLKT_6	I/O	3	GCLKT_6	True_of_IOL11B	TRUE	11	11	
IOL11B/GCLKC_6	I/O	3	GCLKC_6	Comp_of_IOL11A	TRUE			G1
IOL12A	I/O	3		True_of_IOL12B	NONE			
IOL12B	I/O	3		Comp_of_IOL12A	NONE			G2
IOL13A	I/O	3		True_of_IOL13B	TRUE			
IOL13B	I/O	3		Comp_of_IOL13A	TRUE			
IOL14A	I/O	3		True_of_IOL14B	NONE			
IOL14B	I/O	3		Comp_of_IOL14A	NONE			H1

Note!
[1] SDRAM embedded
[2] PSRAM embedded
[3] The pin is internally grounded.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	QN88[1]	QN88P[2]	MG81P[2]
IOL15A	I/O	3		True_of_IOL15B	TRUE	13	13	
IOL15B	I/O	3		Comp_of_IOL15A	TRUE	14	14	H2
IOL16A	I/O	3		True_of_IOL16B	NONE			
IOL16B	I/O	3		Comp_of_IOL16A	NONE			
IOL17A	I/O	3		True_of_IOL17B	TRUE	15	15	
IOL17B	I/O	3		Comp_of_IOL17A	TRUE	16	16	
IOL18A	I/O	3		True_of_IOL18B	NONE			
IOL18B	I/O	3		Comp_of_IOL18A	NONE			
IOL2A	I/O	3		True_of_IOL2B	TRUE	3	3	
IOL2B	I/O	3		Comp_of_IOL2A	TRUE			F1
IOL3A/JTAGSEL_N/LPLL_T_in	I/O	3	JTAGSEL_N/LPLL_T_in	True_of_IOL3B	NONE	4	4	B3
IOL3B/LPLL_C_in	I/O	3	LPLL_C_in	Comp_of_IOL3A	NONE			
IOL4A/LPLL_T_fb	I/O	3	LPLL_T_fb	True_of_IOL4B	TRUE			
IOL4B/LPLL_C_fb	I/O	3	LPLL_C_fb	Comp_of_IOL4A	TRUE			C3
IOL5A	I/O	3		True_of_IOL5B	NONE			
IOL5B	I/O	3		Comp_of_IOL5A	NONE			D3
IOL6A	I/O	3		True_of_IOL6B	TRUE			
IOL6B	I/O	3		Comp_of_IOL6A	TRUE			C1
IOL7A	I/O	3		True_of_IOL7B	NONE			
IOL7B	I/O	3		Comp_of_IOL7A	NONE			C2
IOL8A	I/O	3		True_of_IOL8B	TRUE			
IOL8B	I/O	3		Comp_of_IOL8A	TRUE			D1
IOL9A/GCLKT_7	I/O	3	GCLKT_7	True_of_IOL9B	NONE			
IOL9B/GCLKC_7	I/O	3	GCLKC_7	Comp_of_IOL9A	NONE			D2
IOR10A/MI/D7	I/O	1	MI/D7	True_of_IOR10B	NONE	62	62	E7
IOR10B/MO/D6	I/O	1	MO/D6	Comp_of_IOR10A	NONE	61	61	F7
IOR10C/MCS_N/D5	I/O	1	MCS_N/D5	True_of_IOR10D	NONE	60	60	E8
IOR10D/MCLK/D4	I/O	1	MCLK/D4	Comp_of_IOR10C	NONE	59	59	F8
IOR10E/FASTRD_N/D3	I/O	1	FASTRD_N /D3	True_of_IOR10F	NONE	57	57	
IOR10F/SI/D2	I/O	1	SI/D2	Comp_of_IOR10E	NONE			

Note!
[1] SDRAM embedded
[2] PSRAM embedded
[3] The pin is internally grounded.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	QN88[1]	QN88P[2]	MG81P[2]
IOR10G/SO/D1	I/O	1	SO/D1	True_of_IOR10H	NONE	56	56	
IOR10H/SSPI_CS_N/D0	I/O	1	SSPI_CS_N/D0	Comp_of_IOR10G	NONE	55	55	
IOR10I/DIN/CLKHOLD_N	I/O	1	DIN/CLKHOLD_N	True_of_IOR10J	NONE	54	54	
IOR10J/DOUT/WE_N	I/O	1	DOUT/WE_N	Comp_of_IOR10I	NONE	53	53	
IOR11A/GCLKT_3	I/O	1	GCLKT_3	True_of_IOR11B	TRUE	52	52	
IOR11B/GCLKC_3	I/O	1	GCLKC_3	Comp_of_IOR11A	TRUE	51	51	D7
IOR12A	I/O	1		True_of_IOR12B	NONE			
IOR12B	I/O	1		Comp_of_IOR12A	NONE			F9
IOR13A	I/O	1		True_of_IOR13B	TRUE			
IOR13B	I/O	1		Comp_of_IOR13A	TRUE			
IOR14A	I/O	1		True_of_IOR14B	NONE			
IOR14B	I/O	1		Comp_of_IOR14A	NONE			G8
IOR15A	I/O	1		True_of_IOR15B	TRUE			
IOR15B	I/O	1		Comp_of_IOR15A	TRUE	50	50	G9
IOR16A	I/O	1		True_of_IOR16B	NONE			
IOR16B	I/O	1		Comp_of_IOR16A	NONE			H9
IOR17A	I/O	1		True_of_IOR17B	TRUE	49	49	
IOR17B	I/O	1		Comp_of_IOR17A	TRUE	48	48	
IOR18A	I/O	1		True_of_IOR18B	NONE			
IOR18B	I/O	1		Comp_of_IOR18A	NONE			
IOR2A	I/O	1		True_of_IOR2B	TRUE			
IOR2B	I/O	1		Comp_of_IOR2A	TRUE			
IOR3A/RPLL_T_in	I/O	1	RPLL_T_in	True_of_IOR3B	NONE	63	63	B9
IOR3B/RPLL_C_in	I/O	1	RPLL_C_in	Comp_of_IOR3A	NONE			B8
IOR4A/RPLL_T_fb	I/O	1	RPLL_T_fb	True_of_IOR4B	TRUE			
IOR4B/RPLL_C_fb	I/O	1	RPLL_C_fb	Comp_of_IOR4A	TRUE			C9
IOR5A	I/O	1		True_of_IOR5B	NONE			
IOR5B	I/O	1		Comp_of_IOR5A	NONE			C8
IOR6A	I/O	1		True_of_IOR6B	TRUE			
IOR6B	I/O	1		Comp_of_IOR6A	TRUE			B7

Note!
[1] SDRAM embedded
[2] PSRAM embedded
[3] The pin is internally grounded.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	QN88[1]	QN88P[2]	MG81P[2]
IOR7A	I/O	1		True_of_IOR7B	NONE			
IOR7B	I/O	1		Comp_of_IOR7A	NONE			D9
IOR8A	I/O	1		True_of_IOR8B	TRUE			
IOR8B	I/O	1		Comp_of_IOR8A	TRUE			C7
IOR9A/GCLKT_2	I/O	1	GCLKT_2	True_of_IOR9B	NONE			
IOR9B/GCLKC_2	I/O	1	GCLKC_2	Comp_of_IOR9A	NONE			D8
IOT12A	I/O	0		True_of_IOT12B	NONE	79	79	
IOT12B	I/O	0		Comp_of_IOT12A	NONE			
IOT13A	I/O	0		True_of_IOT13B	NONE			
IOT13B	I/O	0		Comp_of_IOT13A	NONE			
IOT14A	I/O	0		True_of_IOT14B	NONE			B4
IOT14B	I/O	0		Comp_of_IOT14A	NONE			C4
IOT15A	I/O	0		True_of_IOT15B	NONE			
IOT15B	I/O	0		Comp_of_IOT15A	NONE			
IOT16A	I/O	0		True_of_IOT16B	NONE			
IOT16B	I/O	0		Comp_of_IOT16A	NONE			
IOT17A	I/O	0		True_of_IOT17B	NONE			
IOT17B	I/O	0		Comp_of_IOT17A	NONE			
IOT18A	I/O	0		True_of_IOT18B	NONE			
IOT18B	I/O	0		Comp_of_IOT18A	NONE			
IOT20A	I/O	0		True_of_IOT20B	NONE			
IOT20B	I/O	0		Comp_of_IOT20A	NONE			
IOT21A	I/O	0		True_of_IOT21B	NONE			D5
IOT21B	I/O	0		Comp_of_IOT21A	NONE			D6
IOT22A	I/O	0		True_of_IOT22B	NONE			
IOT22B	I/O	0		Comp_of_IOT22A	NONE			
IOT23A	I/O	0		True_of_IOT23B	NONE			
IOT23B	I/O	0		Comp_of_IOT23A	NONE			
IOT24A	I/O	0		True_of_IOT24B	NONE			C5
IOT24B	I/O	0		Comp_of_IOT24A	NONE			C6

Note!
[1] SDRAM embedded
[2] PSRAM embedded
[3] The pin is internally grounded.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	QN88[1]	QN88P[2]	MG81P[2]
IOT25A	I/O	0		True_of_IOT25B	NONE			
IOT25B	I/O	0		Comp_of_IOT25A	NONE			
IOT26A	I/O	0		True_of_IOT26B	NONE			
IOT26B	I/O	0		Comp_of_IOT26A	NONE			
IOT27A	I/O	0		True_of_IOT27B	NONE			
IOT27B	I/O	0		Comp_of_IOT27A	NONE			
IOT2A	I/O	0		True_of_IOT2B	NONE			
IOT2B/MODE0	I/O	0	MODE0	Comp_of_IOT2A	NONE	88	88	GND[3]
IOT30A	I/O	0		True_of_IOT30B	NONE			B5
IOT30B	I/O	0		Comp_of_IOT30A	NONE	77	77	B6
IOT31A	I/O	0		True_of_IOT31B	NONE			
IOT31B	I/O	0		Comp_of_IOT31A	NONE	76	76	
IOT32A	I/O	0		True_of_IOT32B	NONE			
IOT32B	I/O	0		Comp_of_IOT32A	NONE	75	75	
IOT33A	I/O	0		True_of_IOT33B	NONE			
IOT33B	I/O	0		Comp_of_IOT33A	NONE	74	74	
IOT34A	I/O	0		True_of_IOT34B	NONE			
IOT34B	I/O	0		Comp_of_IOT34A	NONE			
IOT35A	I/O	0		True_of_IOT35B	NONE	73	73	A6
IOT35B	I/O	0		Comp_of_IOT35A	NONE	72	72	A7
IOT36A	I/O	0		True_of_IOT36B	NONE	71	71	
IOT36B	I/O	0		Comp_of_IOT36A	NONE	70	70	
IOT37A	I/O	0		True_of_IOT37B	NONE	69	69	
IOT37B	I/O	0		Comp_of_IOT37A	NONE	68	68	
IOT3A/MODE2	I/O	0	MODE2	True_of_IOT3B	NONE	GND[3]	GND[3]	GND[3]
IOT3B/MODE1	I/O	0	MODE1	Comp_of_IOT3A	NONE	87	87	D4
IOT4A	I/O	0		True_of_IOT4B	NONE	86	86	
IOT4B	I/O	0		Comp_of_IOT4A	NONE	85	85	
IOT5A	I/O	0		True_of_IOT5B	NONE	84	84	
IOT5B	I/O	0		Comp_of_IOT5A	NONE	83	83	

Note!
[1] SDRAM embedded
[2] PSRAM embedded
[3] The pin is internally grounded.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	QN88[1]	QN88P[2]	MG81P[2]
IOT6A	I/O	0		True_of_IOT6B	NONE	82	82	
IOT6B	I/O	0		Comp_of_IOT6A	NONE			
IOT7A	I/O	0		True_of_IOT7B	NONE	81	81	A3
IOT7B	I/O	0		Comp_of_IOT7A	NONE			A4
IOT8A	I/O	0		True_of_IOT8B	NONE			
IOT8B	I/O	0		Comp_of_IOT8A	NONE			
IOT9A	I/O	0		True_of_IOT9B	NONE	80	80	
IOT9B	I/O	0		Comp_of_IOT9A	NONE			
VCC	Power	N/A				1	1	A2
VCC	Power	N/A				22	22	J2
VCC	Power	N/A				45	45	
VCC	Power	N/A				66	66	A8
VCCIO0	Power	N/A						A5
VCCIO1	Power	N/A				58	58	E9
VCCIO2	Power	N/A					23	J5
VCCIO2	Power	N/A					44	
VCCIO3	Power	N/A				12	12	E1
VCCX	Power	N/A						J8
VCCX/VCCIO0	Power	N/A					64	
VCCX/VCCIO0	Power	N/A					67	
VCCX/VCCIO0	Power	N/A					78	
VCCX/VCCIO0/VCCIO2	Power	N/A				23		
VCCX/VCCIO0/VCCIO2	Power	N/A				44		
VCCX/VCCIO0/VCCIO2	Power	N/A				64		
VCCX/VCCIO0/VCCIO2	Power	N/A				67		
VCCX/VCCIO0/VCCIO2	Power	N/A				78		
VSS	Ground	N/A				2	2	
VSS	Ground	N/A				21	21	
VSS	Ground	N/A				24	24	
VSS	Ground	N/A				43	43	

Note!
[1] SDRAM embedded
[2] PSRAM embedded
[3] The pin is internally grounded.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	QN88[1]	QN88P[2]	MG81P[2]
VSS	Ground	N/A				46	46	
VSS	Ground	N/A				65	65	
VSS	Ground	N/A						A1
VSS	Ground	N/A						A9
VSS	Ground	N/A						J1
VSS	Ground	N/A						J9

Note!
[1] SDRAM embedded
[2] PSRAM embedded

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	QN88[1]	QN88P[2]	MG81P[2]
BANK3 True LVDS Pair								
IOL11A/GCLKT_6	I/O	3	GCLKT_6	True_of_IOL11B	TRUE			
IOL11B/GCLKC_6	I/O	3	GCLKC_6	Comp_of_IOL11A	TRUE			
IOL13A	I/O	3		True_of_IOL13B	TRUE			
IOL13B	I/O	3		Comp_of_IOL13A	TRUE			
IOL15A	I/O	3		True_of_IOL15B	TRUE	13	13	
IOL15B	I/O	3		Comp_of_IOL15A	TRUE	14	14	
IOL17A	I/O	3		True_of_IOL17B	TRUE	15	15	
IOL17B	I/O	3		Comp_of_IOL17A	TRUE	16	16	
IOL2A	I/O	3		True_of_IOL2B	TRUE			
IOL2B	I/O	3		Comp_of_IOL2A	TRUE			
IOL4A/LPLL_T_fb	I/O	3	LPLL_T_fb	True_of_IOL4B	TRUE			
IOL4B/LPLL_C_fb	I/O	3	LPLL_C_fb	Comp_of_IOL4A	TRUE			
IOL6A	I/O	3		True_of_IOL6B	TRUE			
IOL6B	I/O	3		Comp_of_IOL6A	TRUE			
IOL8A	I/O	3		True_of_IOL8B	TRUE			
IOL8B	I/O	3		Comp_of_IOL8A	TRUE			
BANK2 True LVDS Pair								
IOB12A	I/O	2		True_of_IOB12B	TRUE	31	31	E4
IOB12B	I/O	2		Comp_of_IOB12A	TRUE	32	32	F4
IOB14A	I/O	2		True_of_IOB14B	TRUE			J4
IOB14B	I/O	2		Comp_of_IOB14A	TRUE			H4
IOB16A	I/O	2		True_of_IOB16B	TRUE			
IOB16B	I/O	2		Comp_of_IOB16A	TRUE			
IOB18A	I/O	2		True_of_IOB18B	TRUE			
IOB18B	I/O	2		Comp_of_IOB18A	TRUE			
IOB20A/GCLKT_4	I/O	2	GCLKT_4	True_of_IOB20B	TRUE	35	35	H5
IOB20B/GCLKC_4	I/O	2	GCLKC_4	Comp_of_IOB20A	TRUE	36	36	G5
IOB22A	I/O	2		True_of_IOB22B	TRUE			E6
IOB22B	I/O	2		Comp_of_IOB22A	TRUE			E5
IOB24A	I/O	2		True_of_IOB24B	TRUE			F6

Note!
[1] SDRAM embedded
[2] PSRAM embedded

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	QN88[1]	QN88P[2]	MG81P[2]
IOB24B	I/O	2		Comp_of_IOB24A	TRUE			F5
IOB26A	I/O	2		True_of_IOB26B	TRUE			J6
IOB26B	I/O	2		Comp_of_IOB26A	TRUE			H6
IOB2A	I/O	2		True_of_IOB2B	TRUE	17	17	
IOB2B	I/O	2		Comp_of_IOB2A	TRUE	18	18	
IOB30A	I/O	2		True_of_IOB30B	TRUE	41	41	G6
IOB30B	I/O	2		Comp_of_IOB30A	TRUE	42	42	G7
IOB32A	I/O	2		True_of_IOB32B	TRUE			J7
IOB32B	I/O	2		Comp_of_IOB32A	TRUE			H7
IOB34A	I/O	2		True_of_IOB34B	TRUE			
IOB34B	I/O	2		Comp_of_IOB34A	TRUE			
IOB36A	I/O	2		True_of_IOB36B	TRUE			
IOB36B	I/O	2		Comp_of_IOB36A	TRUE			
IOB4A	I/O	2		True_of_IOB4B	TRUE	19	19	
IOB4B	I/O	2		Comp_of_IOB4A	TRUE	20	20	
IOB6A	I/O	2		True_of_IOB6B	TRUE	25	25	J3
IOB6B	I/O	2		Comp_of_IOB6A	TRUE	26	26	H3
IOB8A	I/O	2		True_of_IOB8B	TRUE	27	27	G3
IOB8B	I/O	2		Comp_of_IOB8A	TRUE	28	28	G4
BANK1 True LVDS Pair								
IOR11A/GCLKT_3	I/O	1	GCLKT_3	True_of_IOR11B	TRUE	52	52	
IOR11B/GCLKC_3	I/O	1	GCLKC_3	Comp_of_IOR11A	TRUE	51	51	
IOR13A	I/O	1		True_of_IOR13B	TRUE			
IOR13B	I/O	1		Comp_of_IOR13A	TRUE			
IOR15A	I/O	1		True_of_IOR15B	TRUE			
IOR15B	I/O	1		Comp_of_IOR15A	TRUE			
IOR17A	I/O	1		True_of_IOR17B	TRUE	49	49	
IOR17B	I/O	1		Comp_of_IOR17A	TRUE	48	48	
IOR2A	I/O	1		True_of_IOR2B	TRUE			
IOR2B	I/O	1		Comp_of_IOR2A	TRUE			
IOR4A/RPLL_T_fb	I/O	1	RPLL_T_fb	True_of_IOR4B	TRUE			

Note!
[1] SDRAM embedded
[2] PSRAM embedded

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	QN88[1]	QN88P[2]	MG81P[2]
IOR4B/RPLL_C_fb	I/O	1	RPLL_C_fb	Comp_of_IOR4A	TRUE			
IOR6A	I/O	1		True_of_IOR6B	TRUE			
IOR6B	I/O	1		Comp_of_IOR6A	TRUE			
IOR8A	I/O	1		True_of_IOR8B	TRUE			
IOR8B	I/O	1		Comp_of_IOR8A	TRUE			

Note!
VCCX should be greater than or equal to VCCIO.

Recommended Operating Conditions of QN88 Package Embedded with SDR SDRMA in GW1NR-4			
Name	**Description**	**Min.**	**Max.**
VCC	LV: Core voltage	1.14V	1.26V
	UV: Core voltage	3.135V	3.6V
VCCIO1, VCCIO3	LV: I/O Bank power supply voltage	1.14V	3.6V
	UV: I/O Bank power supply voltage	1.14V	3.6V
VCCIO0, VCCIO2	I/O Bank power supply voltage, connected to SDR SDRAM port	3.135V	3.6V
VCCX/VCCIO0/VCCIO2	VCCX and VCCIO2 provide power supply for SDRAM, VCCX/VCCIO0/VCCIO2 are internally connected.	3.135V	3.6V

Note!
It is highly recommended that the epad connect to GND, but not a requirement.

Recommended Operating Conditions of MG81P Package Embedded with PSRAM in GW1NR-4			
Name	**Description**	**Min.**	**Max.**
VCC	LV: Core voltage	1.14V	1.26V
	UV: Core voltage	1.71V	3.6V
VCCIO0, VCCIO2	LV: I/O Bank power supply voltage	1.14V	3.6V
	UV: I/O Bank power supply voltage	1.14V	3.6V
VCCIO1, VCCIO3	I/O Bank power supply voltage, connected to PSRAM. VCCIO3 provides power for PSRAM.	1.71V	1.89V
VCCX	Auxiliary voltage	2.375V	3.6V

Recommended Operating Conditions of QN88P Package Embedded with PSRAM in GW1NR-4			
Name	**Description**	**Min.**	**Max.**
VCC	LV: Core voltage	1.14V	1.26V
	UV: Core voltage	1.71V	3.6V
VCCIO2, VCCIO3	LV: I/O Bank power supply voltage	1.14V	3.6V
	UV: I/O Bank power supply voltage	1.14V	3.6V
VCCX/VCCIO0	VCCX/VCCIO0 voltage are internally connected.	2.375V	3.6V
VCCIO1	I/O Bank power supply voltage, connected to PSRAM port. VCCIO1 provides power for	1.71V	1.89V

Note!
It is highly recommended that the epad connect to GND, but not a requirement.