GOWIN
PROGRAMMING FOR THE FUTURE

GW1NR series of FPGA products

# Package & Pinout User Guide

**UG119-1.7.1E, 12/14/2023**

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## Revision History

| Date | Version | Description |
|---|---|---|
| 04/03/2018 | 1.04E | Initial version Published. |
| 06/25/2018 | 1.05E | MG81 package info. Added. |
| 09/13/2018 | 1.06E | The pins distribution view and package outline of MG81added. |
| 12/12/2018 | 1.07E | ● LVDS pairs added in Table 2-1;<br>● Packages of the devices embedded with PSRAM added. |
| 01/09/2019 | 1.08E | ● QN88 of GW1NR4 embedded with PSRAM added;<br>● View of pin distribution and I/O bank description updated. |
| 07/09/2019 | 1.09E | The GW1NR-9 MG100 package added. |
| 04/16/2020 | 1.1E | GW1NR-9c added. |
| 05/18/2020 | 1.1.1E | GW1NR-9 MG100PF added. |
| 06/12/2020 | 1.1.2E | GW1NR-9C revised to GW1NR-9. |
| 06/30/2020 | 1.2E | GW1NR-1 added. |
| 07/28/2020 | 1.3E | GW1NR-9 MG100PD added. |
| 09/27/2020 | 1.4E | ● GW1NR-9 MG100PA, MG100PT, and MG100PS added;<br>● GW1NR-9 MG100PD removed. |
| 02/02/2021 | 1.5E | GW1NR-2 MG49P/MG49PG/MG49G added. |
| 10/26/2021 | 1.6E | GW1NR-1 EQ144G and QN48G added. |
| 01/20/2022 | 1.7E | ● GW1NR-1 QN48X, LQ100G, and QN32X added;<br>● GW1NR-1 QN48G removed. |
| 12/14/2023 | 1.7.1E | ● “Figure 3-12 View of GW1NR-9 QN88 Pins Distribution (Top View)” in “3.4 View of GW1NR-9 Pins Distribution” updated.<br>● “Figure 4-1 Package Outline QN88/QN88P” and the note in “4.1 QN88/QN88P Package Outline (10mm x 10mm)” updated.<br>● Recommended PCB Layout in “4 Package Diagrams” added. |

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# 1 About This Guide

## 1.1 Purpose

This manual contains an introduction to the GW1NR series of FPGA products together with a definition of the pins, list of pin numbers, distribution of pins, and package diagrams.

## 1.2 Related Documents

The latest user guidelines are available on the GOWIN website at www.gowinsemi.com:

- DS117, GW1NR series of FPGA Products Data Sheet
- UG290, Gowin FPGA Products Programming and Configuration User Guide
- UG119, GW1NR series of FPGA Products Package and Pinout
- UG804, GW1NR-1 Pinout
- UG805, GW1NR-2 Pinout
- UG116, GW1NR-4 Pinout
- UG803, GW1NR-9 Pinout

## 1.3 Abbreviations and Terminology

The abbreviations and terminologies that are used in this manual are delineated in Table 1-1.

**Table 1-1 Abbreviations and Terminologies**

| Abbreviations and Terminology | Full Name |
|---|---|
| FPGA | Field Programmable Gate Array |
| SIP | System in Package |
| SDRAM | Synchronous Dynamic RAM |
| PSRAM | Pseudo Static Random Access Memory |
| GPIO | Gowin Programmable IO |

| Abbreviations and Terminology | Full Name |
|---|---|
| FN | QFN |
| QN | QFN |
| MG | MBGA |
| LQ | LQFP |
| EQ | ELQFP |

# 1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

# 2 Overview

The GW1NR series of FPGA Products are the first-generation products of GOWINSEMI® (LittleBee®) family. They are available in various forms that offer high I/O compatibility and flexible usage.

## 2.1 PB-Free Package

The GW1NR series of FPGA products are PB free in line with the EU ROHS environmental directives. The substances used in the GW1NR series of FPGA products are in full compliance with the IPC-1752 standards.

## 2.2 Package and Max. User I/O Information

**Table 2-1 Package and Max. User I/O Information, LVDS Pairs**

| Package | Pitch(mm) | Size (mm) | GW1NR-1 | GW1NR-2 | GW1NR-4 | GW1NR-9 |
|---|---|---|---|---|---|---|
| FN32G | 0.4 | 4 x 4 | 26 | - | - | - |
| MG49P | 0.5 | 3.8 x 3.8 | – | 30（8） | – | – |
| MG49PG | 0.5 | 3.8 x 3.8 | – | 30（8） | – | – |
| MG49G | 0.5 | 3.8 x 3.8 | – | 30（8） | – | – |
| QN88 | 0.4 | 10 x 10 | – | – | 70(11) | 70（19） |
| QN88P | 0.4 | 10 x 10 | – | – | 70(11) | 70（18） |
| MG81P | 0.5 | 4.5 x 4.5 | – | – | 68(10) | - |
| MG100P | 0.5 | 5 x 5 | – | – | - | 87（16） |
| MG100PF[1] | 0.5 | 5 x 5 | – | – | - | 87（16） |
| MG100PA | 0.5 | 5 x 5 | – | – | – | 87（17） |
| MG100PT | 0.5 | 5 x 5 | – | – | – | 87（17） |
| MG100PS | 0.5 | 5 x 5 | – | – | – | 87（17） |
| LQ144P | 0.5 | 20 x 20 | – | – | - | 120（20） |
| EQ144G | 0.5 | 20 x 20 | 112 | – | – | – |
| QN32X | 0.5 | 5 x 5 | 21 | – | – | – |

| Package | Pitch(mm) | Size (mm) | GW1NR-1 | GW1NR-2 | GW1NR-4 | GW1NR-9 |
|---|---|---|---|---|---|---|
| QN48X | 0.5 | 7 x 7 | 39 | - | - | - |
| LQ100G | 0.5 | 14 x 14 | 79 | - | - | - |

**Note!**

- [1]MG100PF: The pinout of ball C1/C2/D2/F1/F9/A7/A6 adjusted on the basis of MG100P.
- In this manual, abbreviations are employed to refer to the package types. See 1.3 Abbreviations and Terminology.
- See GW1NR series Pinouts for more details.
- The JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The data noted in this table is when the loaded four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O. When mode [2:0] = 001, JTAGSEL_N and the four JTAG pins (TCK, TDI, TDO, and TMS) can be used as GPIO simultaneously, and the Max. user I/O plus one.

# 2.3 Power Pin

**Table 2-2 Other Pins in the GW1NR Series**

| | | | |
|---|---|---|---|
| VCC | VCCIO0 | VCCIO1 | VCCIO2 |
| VCCIO3 | VCCX | VSS | NC |

# 2.4 Pin Quantity

## 2.4.1 Quantity of GW1NR-1 Pins

**Table 2-3 Quantity of GW1NR-1 Pins**

| Pin Type | | GW1NR-1 | | | | |
|---|---|---|---|---|---|---|
| | | FN32G | EQ144G | LQ100G | QN32X | QN48X |
| I/O Single end/Differential pair[1] | BANK0 | 8/4 | 31/15 | 22/10 | 2/1 | 10/5 |
| | BANK1 | 5/2 | 22/11 | 18/9 | 9/4 | 10/5 |
| | BANK2 | 6/2 | 34/17 | 22/9 | 2/1 | 10/5 |
| | BANK3 | 8/3 | 25/12 | 17/8 | 8/2 | 9/3 |
| Max. User I/O [2] | | 27 | 112 | 79 | 21 | 39 |
| Differential Pair | | 11 | 55 | 36 | 8 | 18 |
| VCC | | 1 | 4 | 4 | 2 | 2 |
| VCCIO0 | | 0 | 2 | 2 | 1 | 1 |
| VCCIO1 | | 0 | 3 | 3 | 2 | 2 |
| VCCIO2 | | 1 | 2 | 2 | 1 | 1 |
| VCCIO3 | | 1 | 3 | 3 | 2 | 2 |
| VCCIO0/VCCIO1[3] | | 1 | 0 | 0 | 0 | 0 |
| VCCIO0/VCCIO3 | | 0 | 0 | 0 | 0 | 0 |
| VSS | | 1 | 10 | 6 | 2 | 0 |
| MODE0 | | 0 | 1 | 0 | 0 | 0 |
| MODE1 | | 0 | 1 | 1 | 0 | 0 |
| MODE2 | | 0 | 0 | 0 | 0 | 0 |

| Pin Type | GW1NR-1 | | | | |
|---|---|---|---|---|---|
| | FN32G | EQ144G | LQ100G | QN32X | QN48X |
| JTAGSEL_N | 0 | 1 | 1 | 1 | 1 |
| NC | 0 | 7 | 0 | 0 | 0 |

**Note!**

- [1] Quantity of single end/ differential/LVDS I/O include CLK pins, and download pins.
- [2] The JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The Max. I/O noted in this table is when the loaded four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O.
- [3] Pin multiplexing.

## 2.4.2 Quantity of GW1NR-2 Pins

**Table 2-4 Quantity of GW1NR-2 Pins**

| Pin Type | | GW1NR-2 | | |
|---|---|---|---|---|
| | | MG49P | MG49PG | MG49G |
| I/O Single end/Differential pair/LVDS[1] | BANK0 | 14/7/4 | 14/7/4 | 14/7/4 |
| | BANK1 | 0/0/0 | 0/0/0 | 0/0/0 |
| | BANK2 | 8/4/2 | 8/4/2 | 8/4/2 |
| | BANK3 | 4/2/1 | 4/2/1 | 4/2/1 |
| | BANK4 | 4/2/1 | 4/2/1 | 4/2/1 |
| | BANK5 | 0/0/0 | 0/0/0 | 0/0/0 |
| | BANK6 | 10/5/0 | 10/5/0 | 10/5/0 |
| Max. User I/O [2] | | 40 | 40 | 40 |
| Differential Pair | | 20 | 20 | 20 |
| True LVDS output | | 8 | 8 | 8 |
| VCC | | 1 | 1 | 1 |
| VCCX | | 1 | 1 | 1 |
| VCCIO0 | | 1 | 1 | 1 |
| VCCIO1 | | 1 | 1 | 1 |
| VCCIO2/VCCIO3/VCCIO4/VCCIO5[3] | | 1 | 1 | 1 |
| VCCD | | 1 | 1 | 1 |
| VCCIOD | | 1 | 1 | 1 |
| VSS | | 2 | 2 | 2 |
| MODE0 | | 0 | 0 | 0 |
| MODE1 | | 0 | 0 | 0 |
| MODE2 | | 0 | 0 | 0 |
| JTAGSEL_N | | 0 | 0 | 0 |

**Note!**

- [1] Quantity of single end/ differential/LVDS I/O include CLK pins, and download pins.
- [2] The JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The Max. I/O noted in this table is when the loaded four JTAG pins (TCK, TDI, TDO,

and TMS) are used as I/O.
- [3] Pin multiplexing.

## 2.4.3 Quantity of GW1NR-4 Pins

**Table 2-5 Quantity of GW1NR-4 Pins (SDRAM embedded)**

| Pin Type | | GW1NR-4 |
|---|---|---|
| | | QN88 |
| I/O Single end/Differential pair/LVDS[1] | BANK0 | 20/5/0 |
| | BANK1 | 15/6/2 |
| | BANK2 | 23/9/7 |
| | BANK3 | 12/4/2 |
| Max. User I/O [2] | | 70 |
| Differential Pair | | 24 |
| True LVDS output | | 11 |
| VCC | | 4 |
| VCCX | | 0 |
| VCCIO0 | | 0 |
| VCCIO1 | | 1 |
| VCCIO2 | | 2 |
| VCCIO3 | | 1 |
| VCCX/VCCIO0[3] | | 3 |
| VSS | | 6 |
| MODE0 | | 1 |
| MODE1 | | 1 |
| MODE2 | | 0 |
| JTAGSEL_N | | 1 |

**Table 2-6 Quantity of GW1NR-4 Pins (PSRAM embedded)**

| Pin Type | | GW1NR-4 | |
|---|---|---|---|
| | | MG81P | QN88P |
| I/O Single end/Differential pair/LVDS [1] | BANK0 | 13/6/0 | 20/5/0 |
| | BANK1 | 17/3/0 | 15/6/2 |
| | BANK2 | 21/10/10 | 23/9/7 |
| | BANK3 | 17/2/0 | 12/4/2 |
| Max. User I/O[2] | | 68 | 70 |
| Differential Pair | | 21 | 24 |
| True LVDS output | | 10 | 11 |
| VCC | | 3 | 4 |
| VCCX | | 1 | 0 |
| VCCIO0 | | 1 | 0 |
| VCCIO1 | | 1 | 1 |

| Pin Type | GW1NR-4 | |
|---|---|---|
| | MG81P | QN88P |
| VCCIO2 | 1 | 2 |
| VCCIO3 | 1 | 1 |
| VCCX/VCCIO0[3] | 0 | 3 |
| VSS | 4 | 6 |
| MODE0 | 0 | 1 |
| MODE1 | 1 | 1 |
| MODE2 | 0 | 0 |
| JTAGSEL_N | 1 | 1 |

**Note!**

- [1] Quantity of single end/ differential/LVDS I/O include CLK pins, and download pins.
- [2] The JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The Max. I/O noted in this table is when the loaded four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O.
- [3] Pin multiplexing.

## 2.4.4 Quantity of GW1NR-9 Pins

**Table 2-7 Quantity of GW1NR-9 Pins**

| Pin Type | | GW1NR-9 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | QN88 | QN88P | LQ144P | MG100P | MG100PF | MG100PA | MG100PT | MG100PS |
| I/O Single end/Differential pair/LVDS[1] | BANK0 | 0/0/0 | 0/0/0 | 18/9/0 | 12/6/0 | 12/6/0 | 12/6/0 | 12/6/0 | 12/6/0 |
| | BANK1 | 25/11/4 | 25/11/4 | 32/12/4 | 22/5/1 | 22/6/1 | 22/6/1 | 22/5/1 | 22/6/1 |
| | BANK2 | 23/11/11 | 23/11/11 | 40/19/14 | 32/15/14 | 32/15/14 | 32/15/14 | 32/15/14 | 32/15/14 |
| | BANK3 | 22/8/4 | 22/6/3 | 30/8/2 | 21/4/1 | 21/6/1 | 21/6/2 | 21/4/2 | 21/6/2 |
| Max. User I/O [2] | | 70 | 70 | 120 | 87 | 87 | 87 | 87 | 87 |
| Differential Pair | | 30 | 28 | 48 | 30 | 33 | 33 | 30 | 33 |
| True LVDS output | | 19 | 18 | 20 | 16 | 16 | 17 | 17 | 17 |
| VCC | | 4 | 4 | 4 | 3 | 3 | 3 | 3 | 3 |
| VCCX | | 0 | 0 | 2 | 1 | 1 | 1 | 1 | 1 |
| VCCIO0 | | 0 | 0 | 2 | 1 | 1 | 1 | 1 | 1 |
| VCCIO1 | | 1 | 1 | 2 | 1 | 1 | 1 | 1 | 1 |
| VCCIO2 | | 2 | 2 | 2 | 1 | 1 | 1 | 1 | 1 |
| VCCIO3 | | 1 | 1 | 2 | 1 | 1 | 1 | 1 | 1 |
| VCCX/VCCIO0[3] | | 3 | 3 | 0 | 0 | 0 | 0 | 0 | 0 |
| VSS | | 6 | 6 | 9 | 4 | 4 | 4 | 4 | 4 |
| MODE0 | | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| MODE1 | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| MODE2 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| JTAGSEL_N | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**Note!**

- [1] Quantity of single end/ differential/LVDS I/O include CLK pins, and download pins.
- [2] The JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The data in this table is when the loaded four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O.
- [3] Pin multiplexing.

# 2.5 Introduction to the I/O BANK

GW1NR-1/4/9 includes four I/O Banks.

GW1NR-2 MG49P/MG49PG/MG49G includes seven I/O Banks.

This manual provides an overview of the distribution view of the pins in the GW1NR series of FPGA products. Please refer to 3 View of Pin Distribution for further details. Different IO Banks in the GW1NR series FPGA products are marked with different colors.

User I/O, power, and ground are also marked with different symbols and colors. The various symbols and colors used for the various pins are defined as follows:

- “  ” denotes I/Os in BANK0.
- ”  ” denotes I/Os in BANK1.
- ”  ” denotes I/Os in BANK2.
- ”  ” denotes I/Os in BANK3.
- ”  ” denotes I/Os in BANK4.
- ”  ” denotes I/Os in BANK5.
- ”  ” denotes I/Os in BANK6.
- “  ” denotes VCC, VCCX, and VCCIO. The filling color does not change.
- ”  ” denotes VCC. The filling color does not change.
- “  ” denotes NC.

# 3 View of Pin Distribution

## 3.1 View of GW1NR-1 Pins Distribution

### 3.1.1 View of FN32G Pins Distribution

**Figure 3-1 View of GW1NR-1 FN32G Pins Distribution (Top View)**

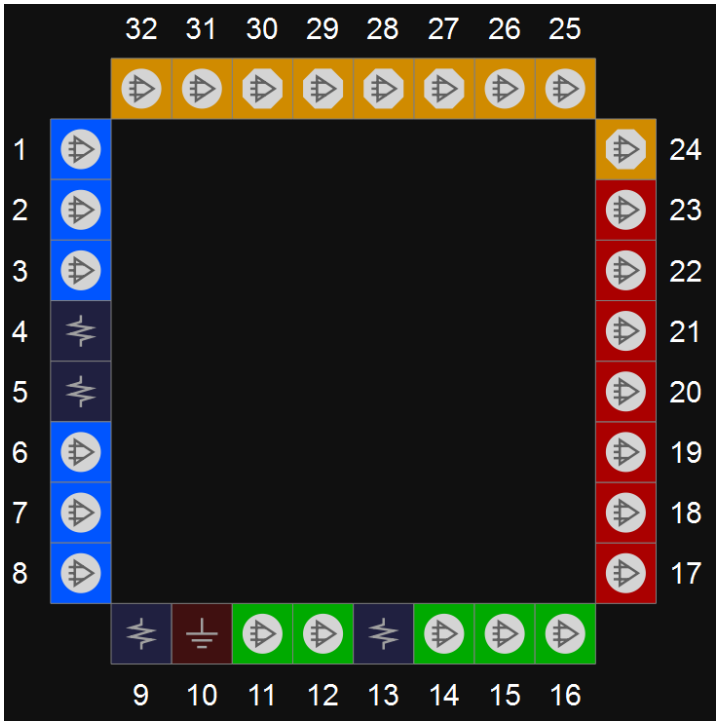



**Table 3-1 Other pins in GW1NR-1 FN32G**

| | |
|---|---|
| VCC | 9 |
| VCCIO0/VCCIO1 | 13 |
| VCCIO2 | 5 |
| VCCIO3 | 4 |
| VSS | 10 |

## 3.1.2 View of EQ144G Pins Distribution

**Figure 3-2 View of GW1NR-1 EQ144G Pins Distribution (Top View)**


**Table 3-2 Other pins in GW1NR-1 EQ144G**

| | |
|---|---|
| VCC | 1,36,73,108 |
| VCCIO0 | 109,127 |
| VCCIO1 | 77,91,103 |
| VCCIO2 | 37,55 |
| VCCIO3 | 5,19,31 |
| VSS | 2,35,74,107,125,89,105,53,17,33 |
| NC | 93,94,95,96,110,111,112 |

### 3.1.3 View of LQ100G Pins Distribution

**Figure 3-3 View of GW1NR-1 LQ100G Pins Distribution (Top View)**

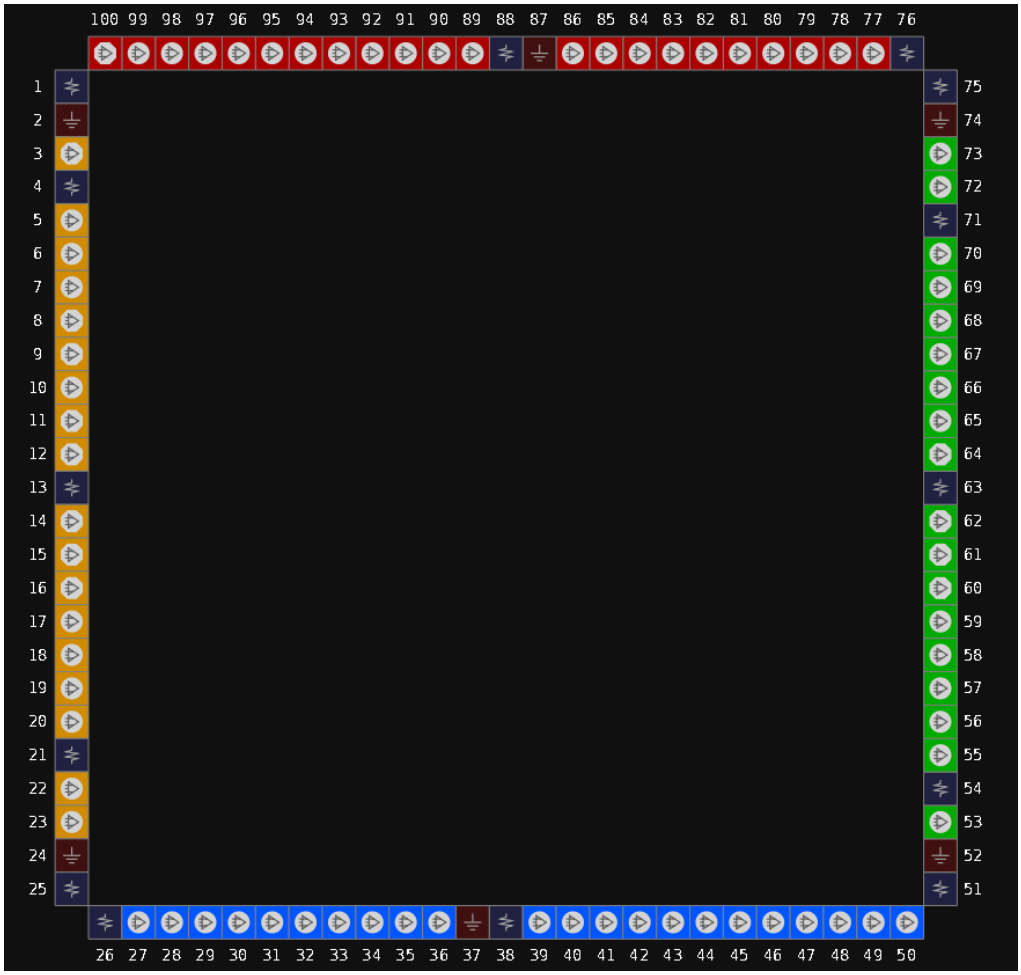



**Table 3-3 Other pins in GW1NR-1 LQ100G**

| | |
|---|---|
| VCC | 1,25,51,75 |
| VCCIO0 | 76,88 |
| VCCIO1 | 54,63,71 |
| VCCIO2 | 26,38 |
| VCCIO3 | 4,13,21 |
| VSS | 2,24,52,74,87,37 |

### 3.1.4 View of QN32X Pins Distribution

**Figure 3-4 View of GW1NR-1 QN32X Pins Distribution (Top View)**

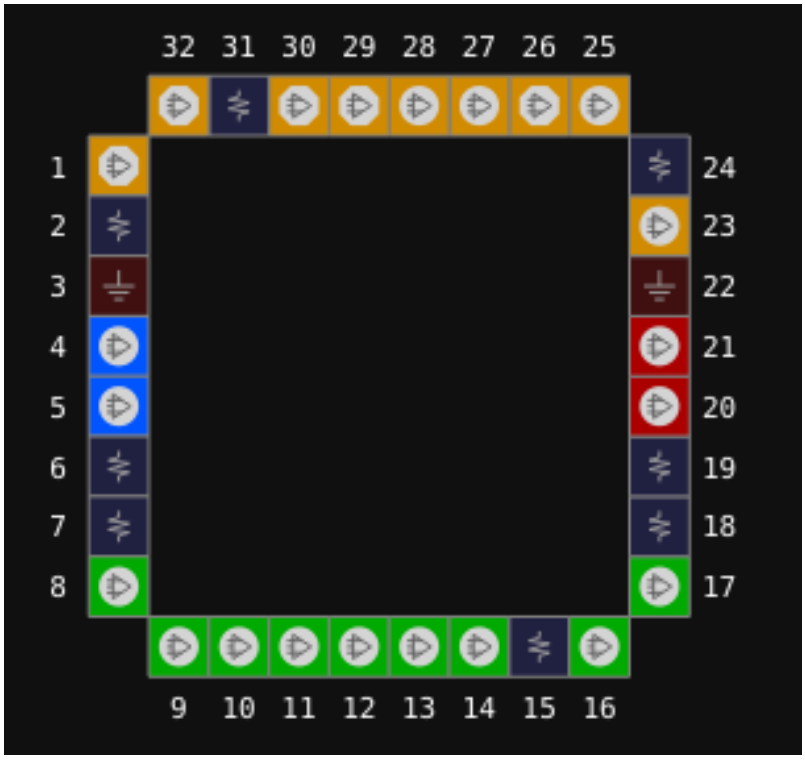



**Table 3-4 Other pins in GW1NR-1 QN32X**

| | |
|---|---|
| VCC | 2,18 |
| VCCIO0 | 19 |
| VCCIO1 | 7,15 |
| VCCIO2 | 6 |
| VCCIO3 | 24,31 |
| VSS | 3,22 |

### 3.1.5 View of QN48X Pins Distribution

**Figure 3-5 View of GW1NR-1 QN48X Pins Distribution (Top View)**

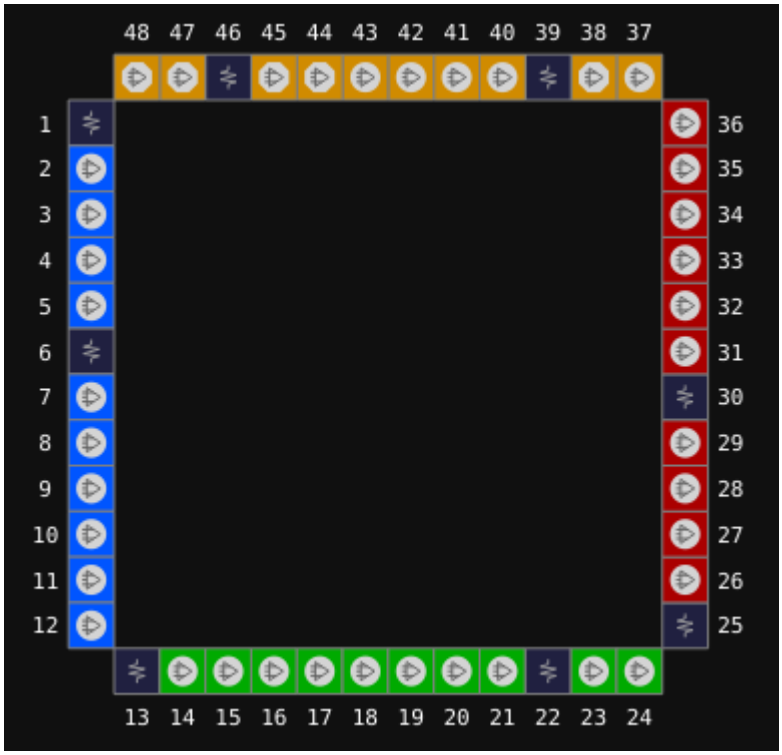



**Table 3-5 Other pins in GW1NR-1 QN48X**

| | |
|---|---|
| VCC | 1,25 |
| VCCIO0 | 30 |
| VCCIO1 | 13,22 |
| VCCIO2 | 6 |
| VCCIO3 | 39,46 |

# 3.2 View of GW1NR-2 Pins Distribution

## 3.2.1 View of MG49P Pins Distribution (PSRAM Embedded)

**Figure 3-6 View of GW1NR-2 MG49P Pins Distribution (Top View, PSRAM Embedded)**

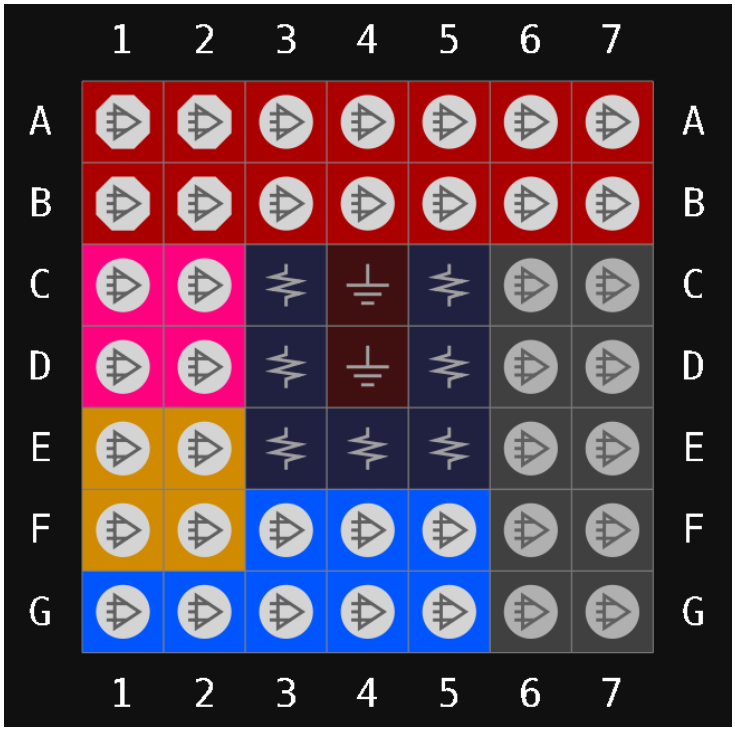



**Table 3-6 Other pins in GW1NR-2 MG49P (PSRAM Embedded)**

| | |
|---|---|
| VCC | C3 |
| VCCD | E4 |
| VCCIOD | E5 |
| VCCIO0 | C5 |
| VCCIO1 | D5 |
| VCCIO2/VCCIO3/VCCIO4/VCCIO5 | D3 |
| VCCX | E3 |
| VSS | C4,D4 |

### 3.2.2 View of MG49PG Pins Distribution (PSRAM and Flash Embedded)

**Figure 3-7 View of GW1NR-2 MG49PG Pins Distribution (Top View, PSRAM and Flash Embedded)**

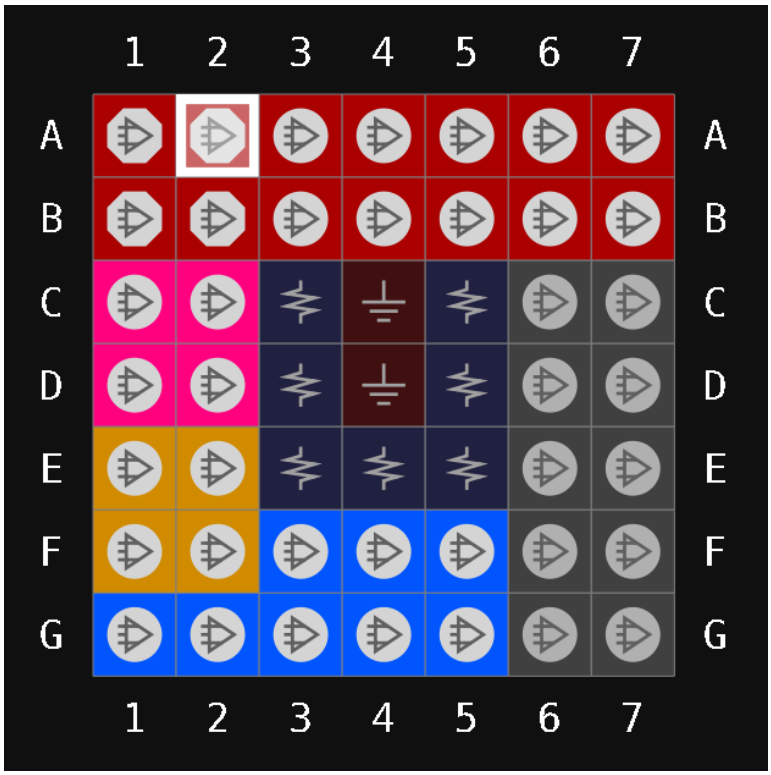



**Table 3-7 Other pins in GW1NR-2 MG49PG (PSRAM and Flash Embedded)**

| | |
|---|---|
| VCC | C3 |
| VCCD | E4 |
| VCCIOD | E5 |
| VCCIO0 | C5 |
| VCCIO1 | D5 |
| VCCIO2/VCCIO3/VCCIO4/VCCIO5 | D3 |
| VCCX | E3 |
| VSS | C4,D4 |

### 3.2.3 View of MG49G Pins Distribution (Flash Embedded)

**Figure 3-8 View of GW1NR-2 MG49G Pins Distribution (Top View, Flash Embedded)**

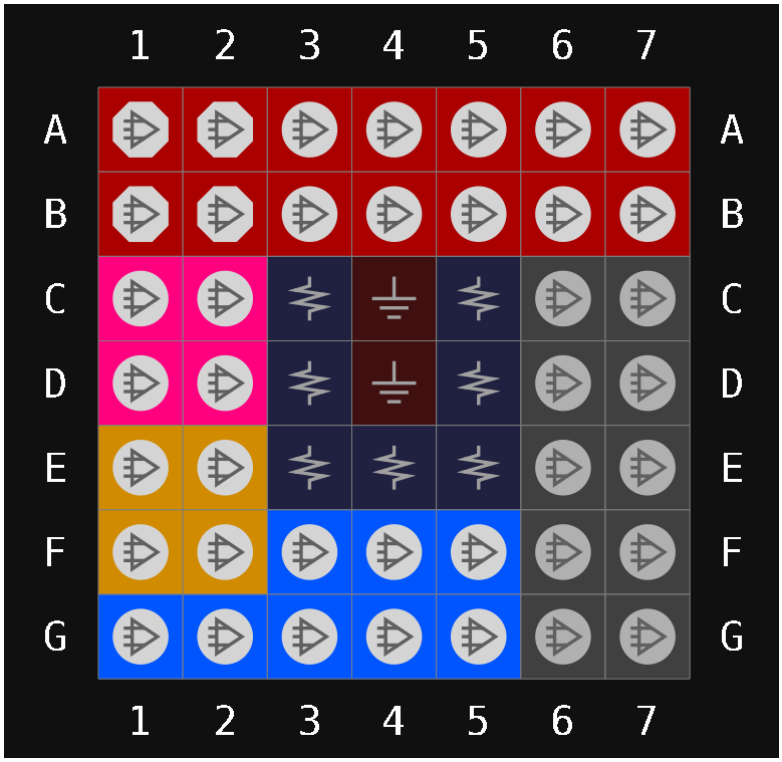



**Table 3-8 Other pins in GW1NR-2 MG49G (Flash Embedded)**

| | |
|---|---|
| VCC | C3 |
| VCCD | E4 |
| VCCIOD | E5 |
| VCCIO0 | C5 |
| VCCIO1 | D5 |
| VCCIO2/VCCIO3/VCCIO4/VCCIO5 | D3 |
| VCCX | E3 |
| VSS | C4,D4 |

# 3.3 View of GW1NR-4 Pins Distribution

## 3.3.1 View of MG81P Pins Distribution (PSRAM Embedded)

**Figure 3-9 View of GW1NR-4 MG81P Pins Distribution (Top View, PSRAM Embedded)**

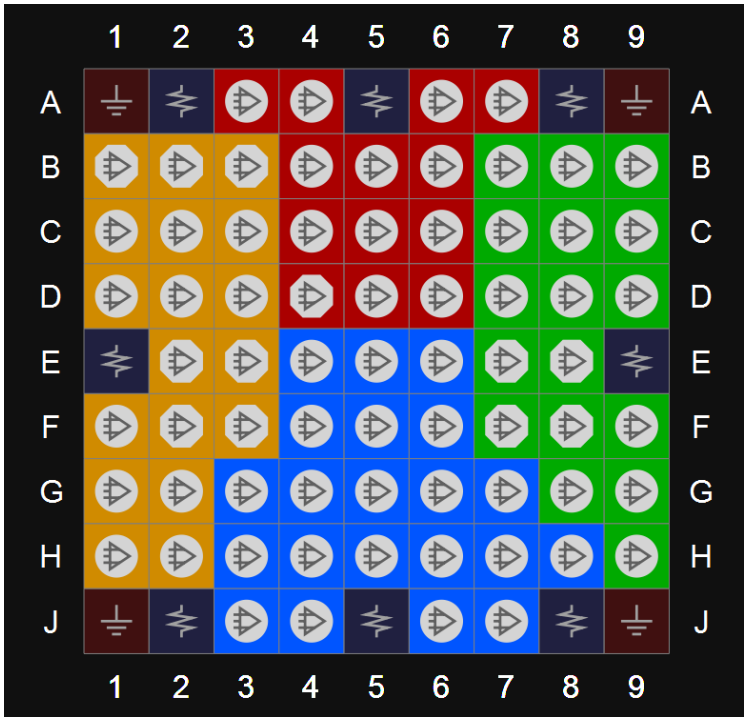



**Table 3-9 Other pins in GW1NR-4 MG81P (PSRAM Embedded)**

| | |
|---|---|
| VCC | A2, A8, J2 |
| VCCX | J8 |
| VCCIO0 | A5 |
| VCCIO1 | E9 |
| VCCIO2 | J5 |
| VCCIO3 | E1 |
| VSS | A1, A9, J1, J9 |

## 3.3.2 View of QN88P Pins Distribution (PSRAM Embedded)

**Figure 3-10 View of GW1NR-4 QN88P Pins Distribution (Top View, PSRAM Embedded)**

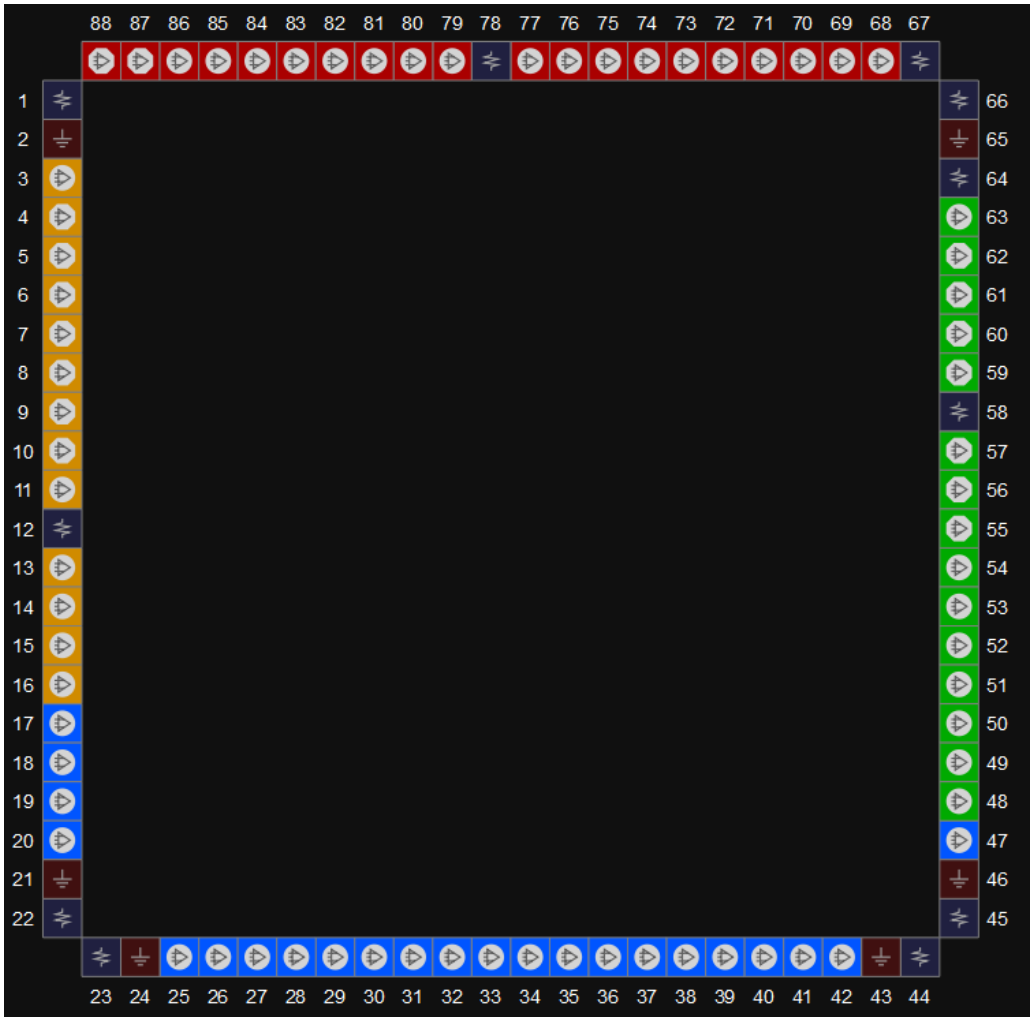



**Table 3-10 Other pins in GW1NR-4 QN88P (PSRAM Embedded)**

| | |
|---|---|
| VCC | 1, 22, 45, 66 |
| VCCX/VCCIO0 | 64, 67, 78 |
| VCCIO1 | 58 |
| VCCIO2 | 23, 44 |
| VCCIO3 | 12 |
| VSS | 2, 21, 24, 43, 46, 65 |

### 3.3.3 View of QN88 Pins Distribution (SDRAM Embedded)

**Figure 3-11 View of GW1NR-4 QN88 Pins Distribution (Top View, SDRAM Embedded)**

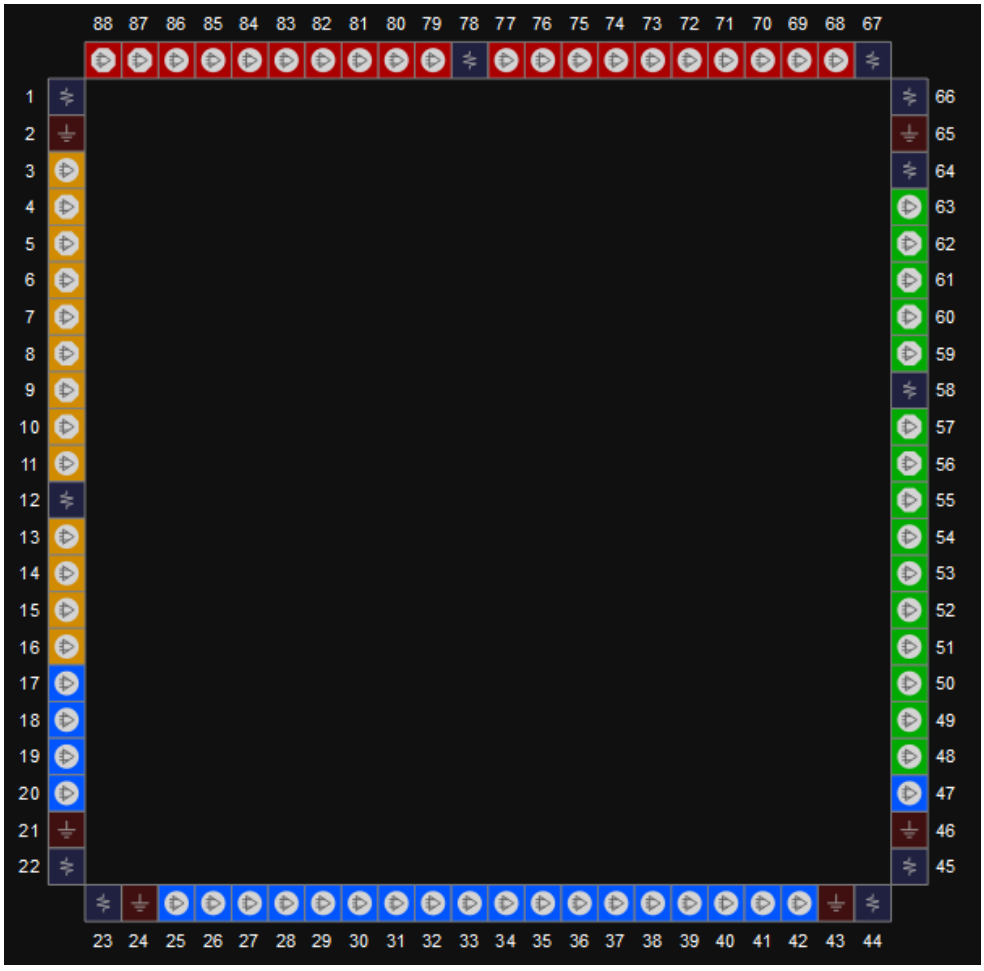



**Table 3-11 Other pins in GW1NR-4 QN88 (SDRAM Embedded)**

| | |
|---|---|
| VCC | 1, 22, 45, 66 |
| VCCX/VCCIO0 | 64, 67, 78 |
| VCCIO1 | 58 |
| VCCIO2 | 23, 44 |
| VCCIO3 | 12 |
| VSS | 2, 21, 24, 43, 46, 65 |

# 3.4 View of GW1NR-9 Pins Distribution

## 3.4.1 View of QN88 Pins Distribution

**Figure 3-12 View of GW1NR-9 QN88 Pins Distribution (Top View)**

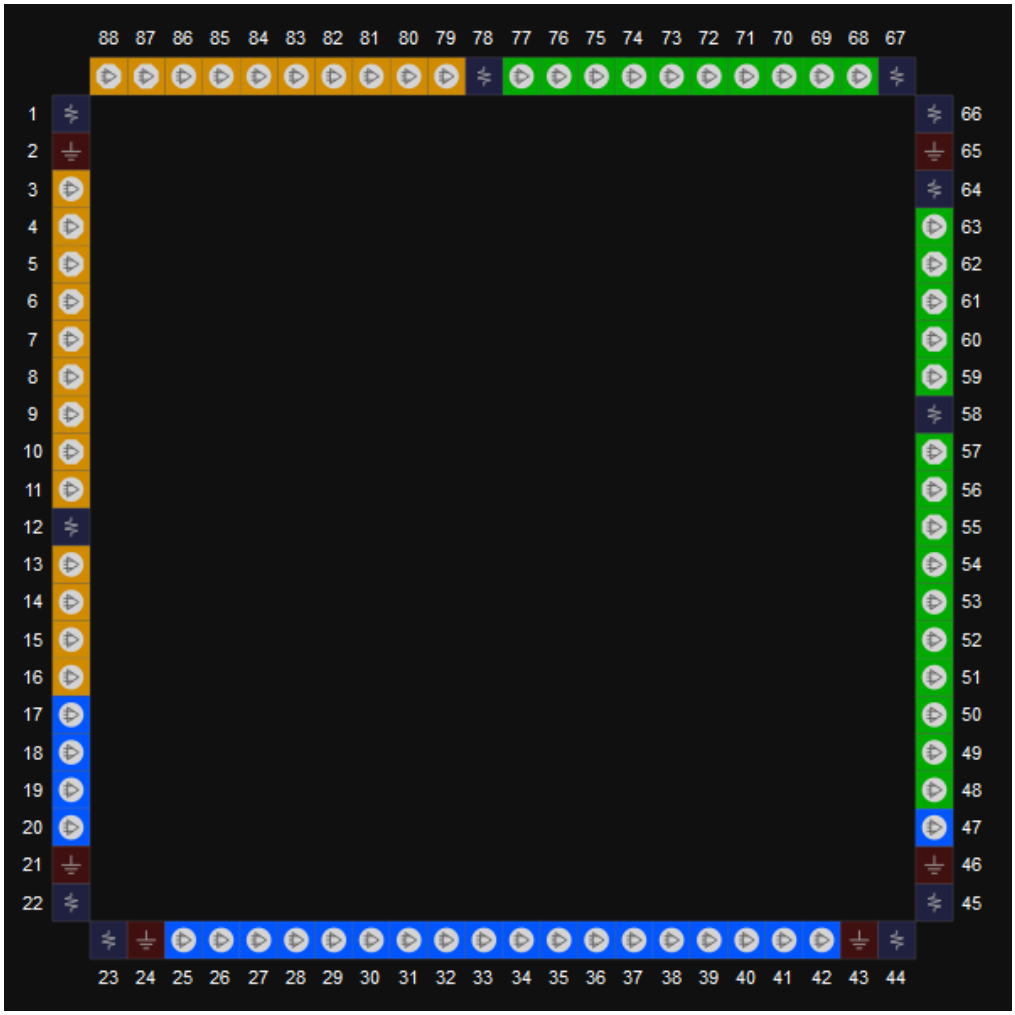



**Table 3-12 Other pins in GW1NR-9 QN88**

| | |
|---|---|
| VCC | 1, 22, 45, 66 |
| VCCX/VCCIO0 | 64, 67, 78 |
| VCCIO1 | 58 |
| VCCIO2 | 23, 44 |
| VCCIO3 | 12 |
| MODE | 87, 88 |
| VSS | 2, 21, 24, 43, 46, 65 |

## 3.4.2 View of QN88P Pins Distribution

**Figure 3-13 View of GW1NR-9 QN88P Pins Distribution (Top View)**

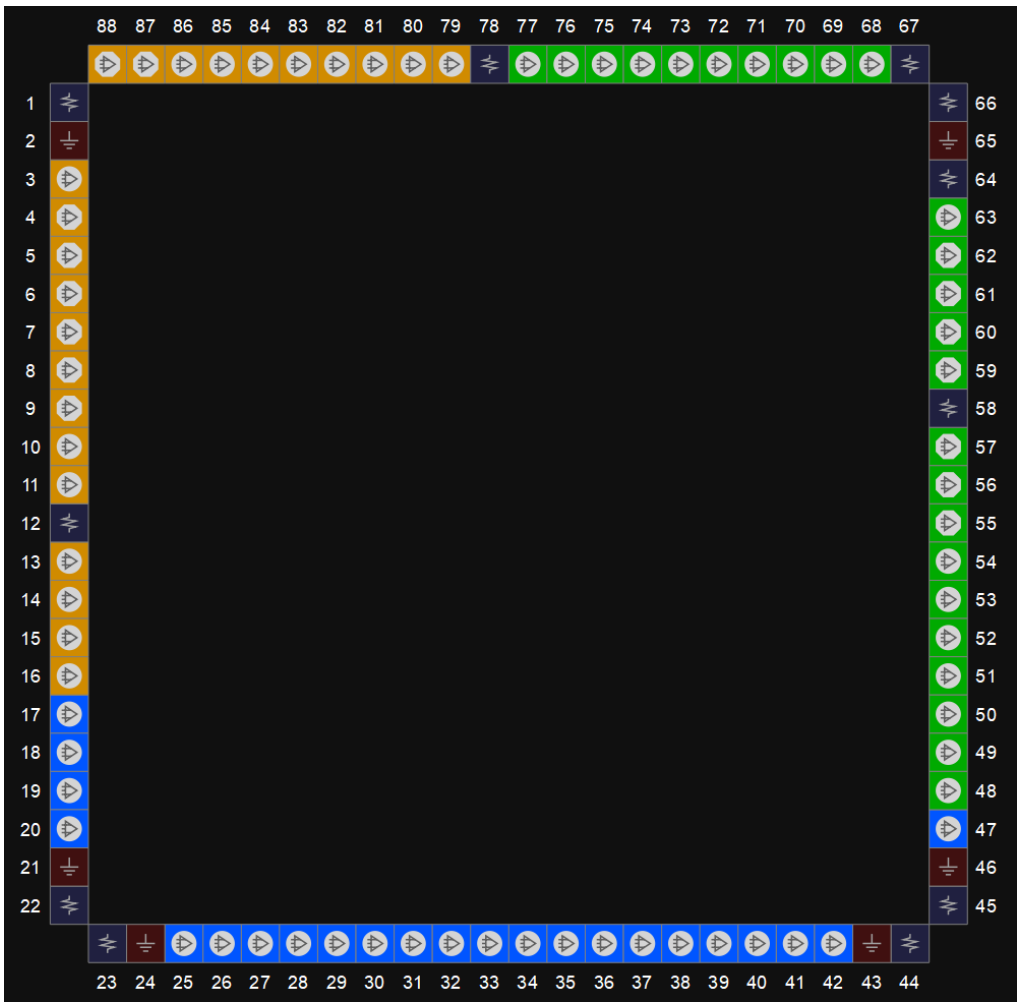



**Table 3-13 Other pins in GW1NR-9 QN88P**

| | |
|---|---|
| VCC | 1, 22, 45, 66 |
| VCCX/VCCIO0 | 64, 67, 78 |
| VCCIO1 | 58 |
| VCCIO2 | 23, 44 |
| VCCIO3 | 12 |
| MODE | 87, 88 |
| VSS | 2, 21, 24, 43, 46, 65 |

### 3.4.3 View of MG100P Pins Distribution

**Figure 3-14 View of GW1NR-9 MG100P Pins Distribution (Top View)**

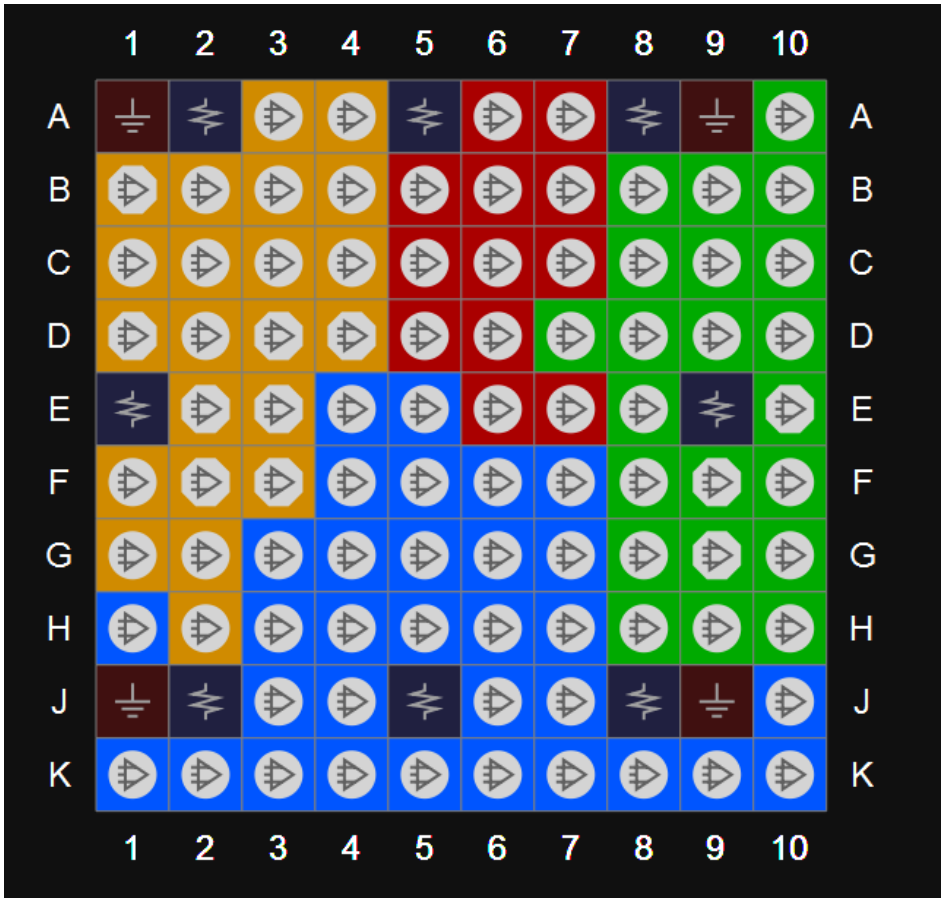



**Table 3-14 Other pins in GW1NR-9 MG100P**

| | |
|---|---|
| VCC | A2,J2,A8 |
| VCCIO0 | A5 |
| VCCIO1 | E9 |
| VCCIO2 | J5 |
| VCCIO3 | E1 |
| VCCX | J8 |
| MODE | D4 |
| VSS | A1,A9,J1,J9 |

### 3.4.4 View of MG100PF Pins Distribution

**Figure 3-15 View of GW1NR-9 MG100PF Pins Distribution (Top View)**

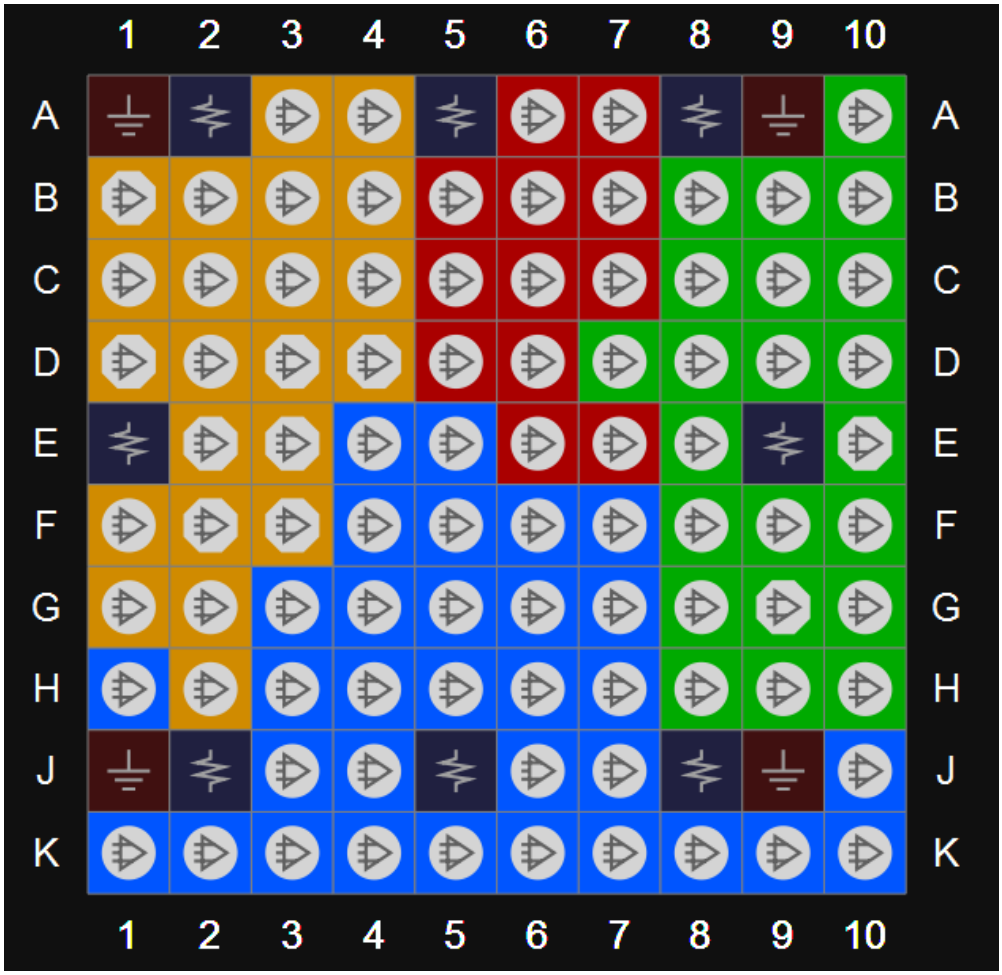



**Table 3-15 Other pins in GW1NR-9 MG100PF**

| | |
|---|---|
| VCC | A2,J2,A8 |
| VCCIO0 | A5 |
| VCCIO1 | E9 |
| VCCIO2 | J5 |
| VCCIO3 | E1 |
| VCCX | J8 |
| MODE | D4 |
| VSS | A1,A9,J1,J9 |

## 3.4.5 View of LQ144P Pins Distribution

**Figure 3-16 View of GW1NR-9 LQ144P Pins Distribution (Top View)**


**Table 3-16 Other pins in GW1NR-9 LQ144P**

| | |
|---|---|
| VCC | 1, 36, 73, 108 |
| VCCIO0 | 109, 127 |
| VCCIO1 | 91, 103 |
| VCCIO2 | 37, 55 |
| VCCIO3 | 9, 19 |
| VCCX | 31, 77 |
| MODE | 143, 144 |
| VSS | 2, 17, 33, 35, 53, 74, 89, 105, 107 |

### 3.4.6 View of MG100PA Pins Distribution

**Figure 3-17 View of GW1NR-9 MG100PA Pins Distribution (Top View)**

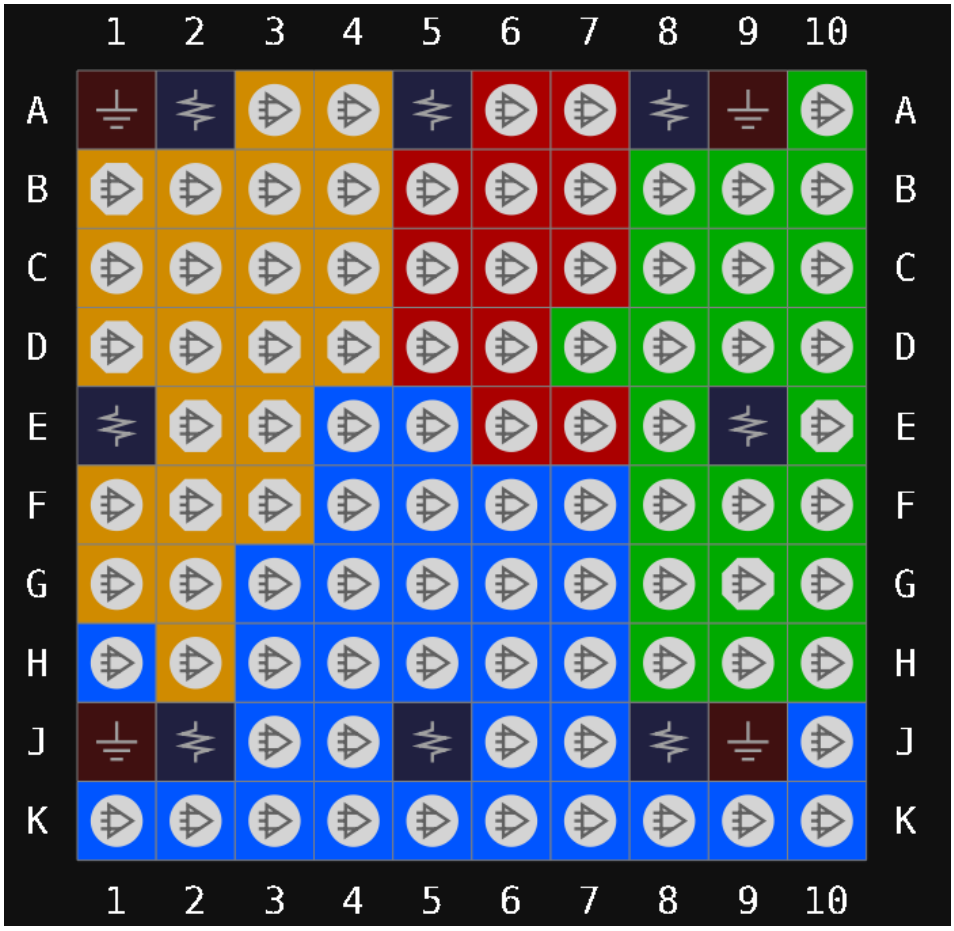



**Table 3-17 Other pins in GW1NR-9 MG100PA**

| | |
|---|---|
| VCC | A2,J2,A8 |
| VCCIO0 | A5 |
| VCCIO1 | E9 |
| VCCIO2 | J5 |
| VCCIO3 | E1 |
| VCCX | J8 |
| MODE | D4 |
| VSS | A1,A9,J1,J9 |

## 3.4.7 View of MG100PS Pins Distribution

**Figure 3-18 View of GW1NR-9 MG100PS Pins Distribution (Top View)**

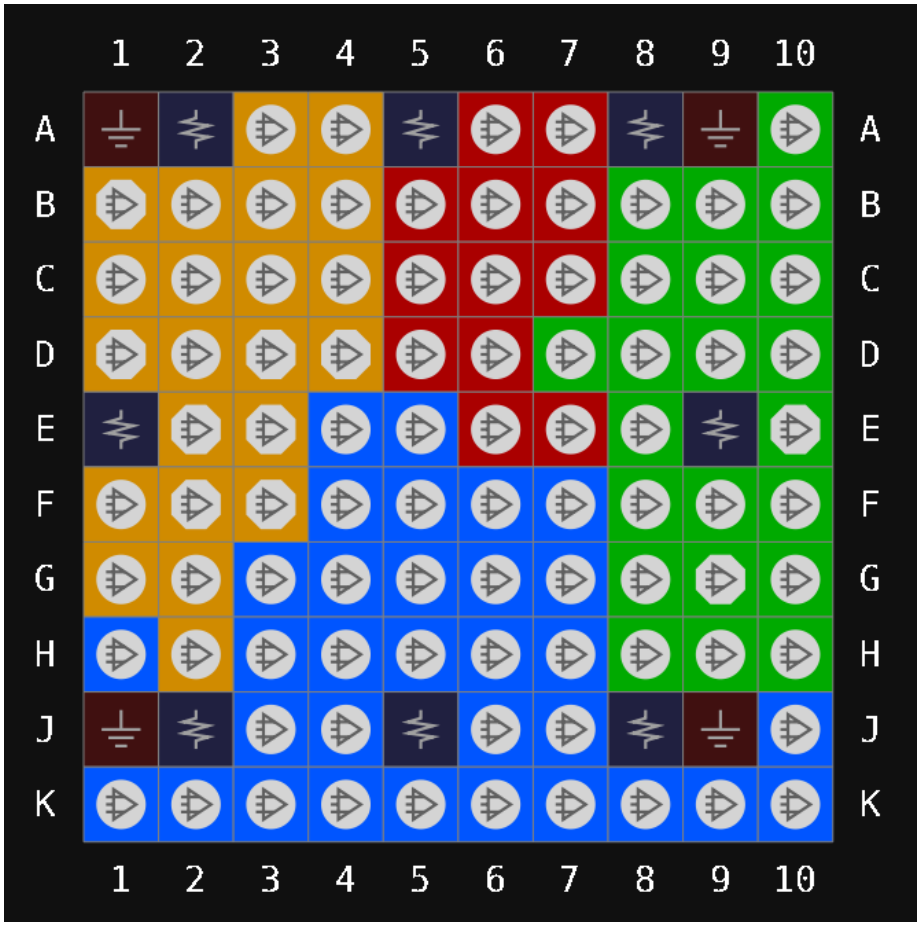



**Table 3-18 Other pins in GW1NR-9 MG100PS**

| | |
|---|---|
| VCC | A2,A8,J2 |
| VCCIO0 | A5 |
| VCCIO1 | E9 |
| VCCIO2 | J5 |
| VCCIO3 | E1 |
| VCCX | J8 |
| MODE | D4 |
| VSS | A1,A9,J1,J9 |

### 3.4.8 View of MG100PT Pins Distribution

**Figure 3-19 View of GW1NR-9 MG100PT Pins Distribution (Top View)**

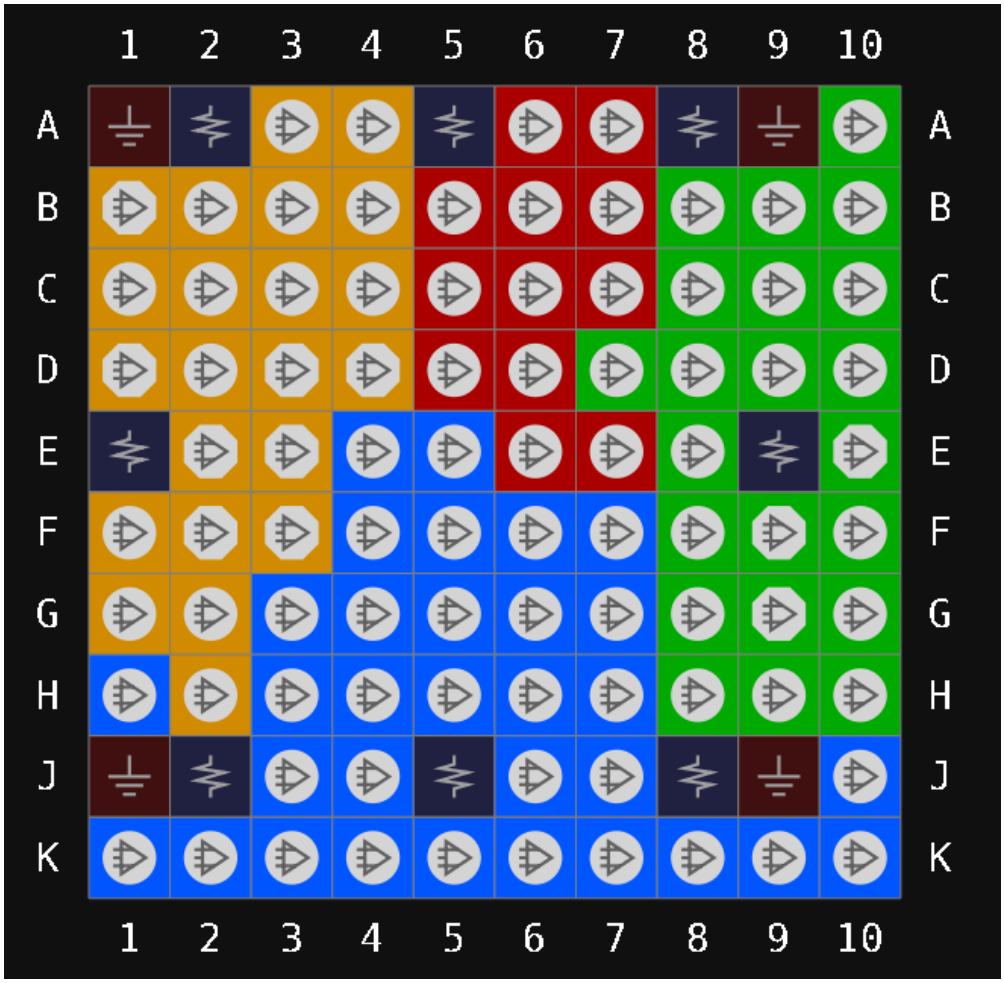


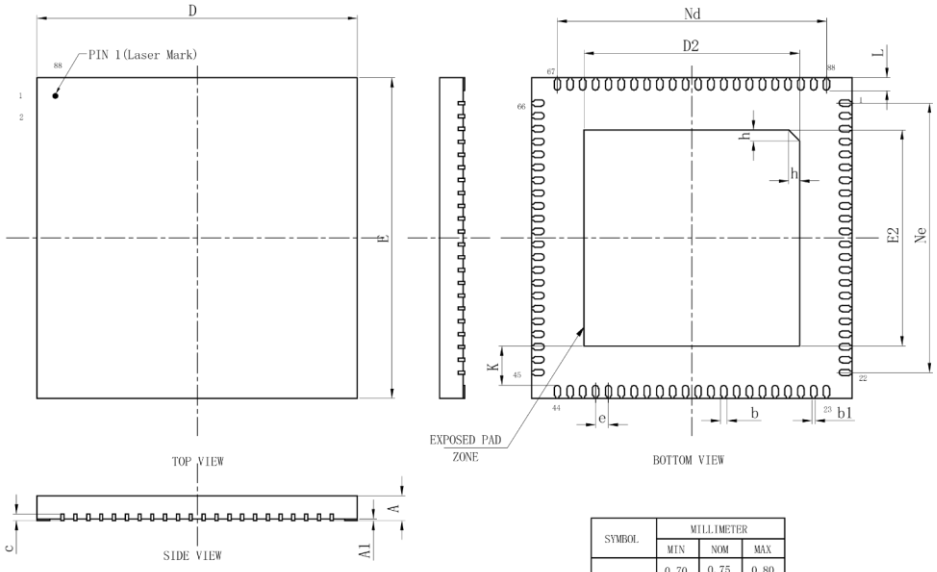

**Table 3-19 Other pins in GW1NR-9 MG100PT**

| | |
|---|---|
| VCC | A2,A8,J2 |
| VCCIO0 | A5 |
| VCCIO1 | E9 |
| VCCIO2 | J5 |
| VCCIO3 | E1 |
| VCCX | J8 |
| MODE | D4 |
| VSS | A1,A9,J1,J9 |

# 4 Package Diagrams

## 4.1 QN88/QN88P Package Outline (10mm x 10mm)

**Figure 4-1 Package Outline QN88/QN88P**

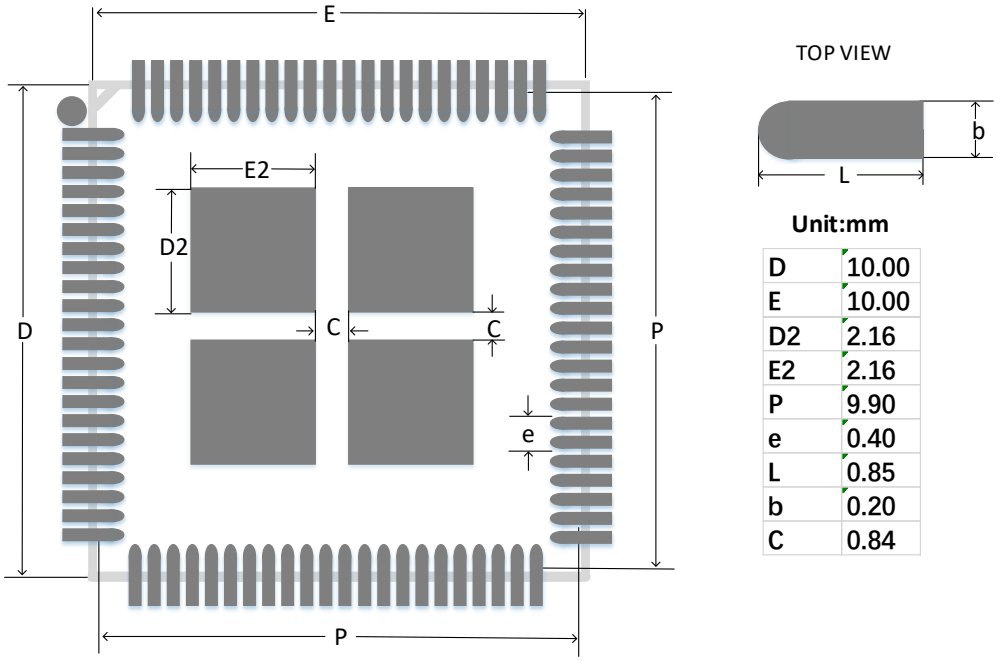



| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.70 | 0.75 | 0.80 |
| | 0.80 | 0.85 | 0.90 |
| | 0.85 | 0.90 | 0.95 |
| A1 | 0 | 0.02 | 0.05 |
| b | 0.15 | 0.20 | 0.25 |
| b1 | 0.10REF | | |
| c | 0.18 | 0.20 | 0.25 |
| D | 9.90 | 10.00 | 10.10 |
| D2 | 6.64 | 6.74 | 6.84 |
| e | 0.40BSC | | |
| Nd | 8.40REF | | |
| E | 9.90 | 10.00 | 10.10 |
| E2 | 6.64 | 6.74 | 6.84 |
| Ne | 8.40REF | | |
| L | 0.30 | 0.40 | 0.50 |
| K | 0.20 | – | – |
| h | 0.30 | 0.35 | 0.40 |

注！

- For GW1NR-LV4QN88, GW1NR-UV4QN88, and GW1NR-LV9QN88, the value of A(NOM) is 0.85mm.
- For GW1NR-LV4QN88P, GW1NR-UV4QN88P, GW1NR-LV9QN88P, and GW1NR-UV9QN88P, the value of A(NOM) is 0.75mm.

**Figure 4-2 Recommended PCB Layout QN88/QN88P**

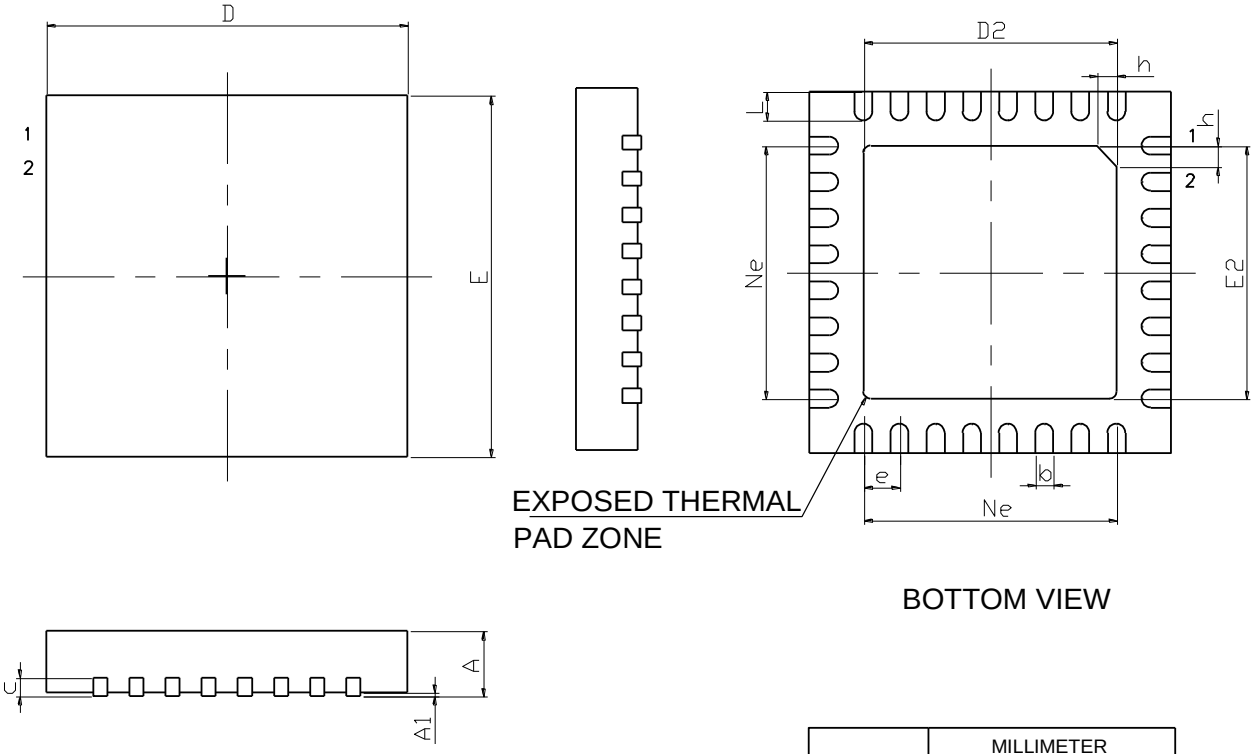



Unit:mm

| | |
|---|---|
| D | 10.00 |
| E | 10.00 |
| D2 | 2.16 |
| E2 | 2.16 |
| P | 9.90 |
| e | 0.40 |
| L | 0.85 |
| b | 0.20 |
| C | 0.84 |

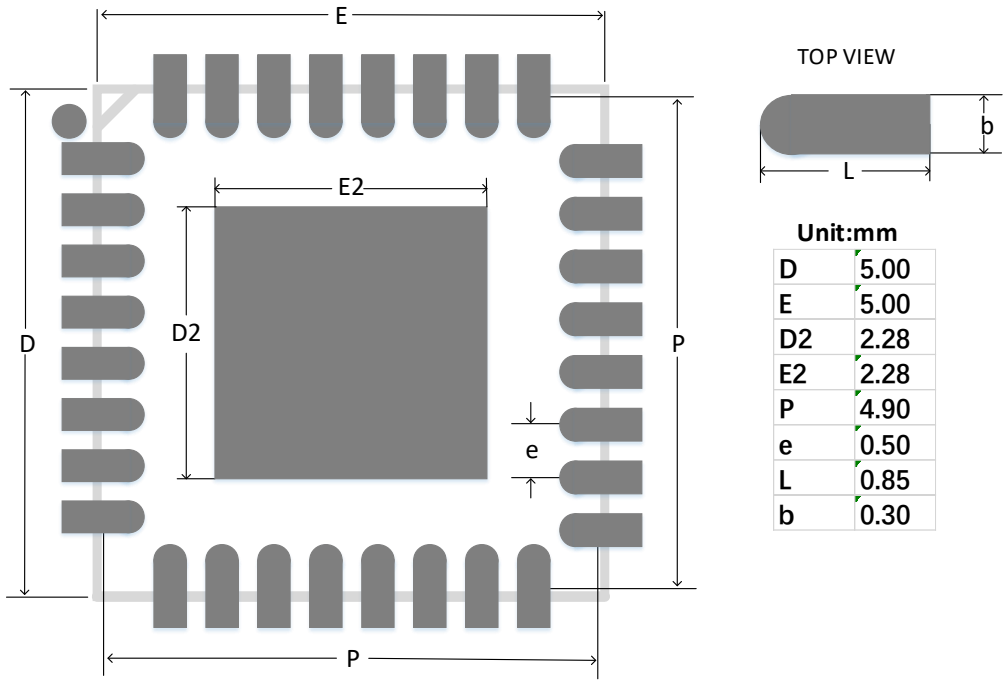
# 4.2 QN32X Package Outline (5mm x 5mm)

**Figure 4-3 Package Outline QN32X**




| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0 | 0.02 | 0.05 |
| b | 0.18 | 0.25 | 0.30 |
| c | 0.18 | 0.20 | 0.25 |
| D | 4.90 | 5.00 | 5.10 |
| D2 | 3.40 | 3.50 | 3.60 |
| e | 0.50BSC | | |
| Ne | 3.50BSC | | |
| E | 4.90 | 5.00 | 5.10 |
| E2 | 3.40 | 3.50 | 3.60 |
| L | 0.35 | 0.40 | 0.45 |
| h | 0.30 | 0.35 | 0.40 |

**Figure 4-4 Recommended PCB Layout QN32X**

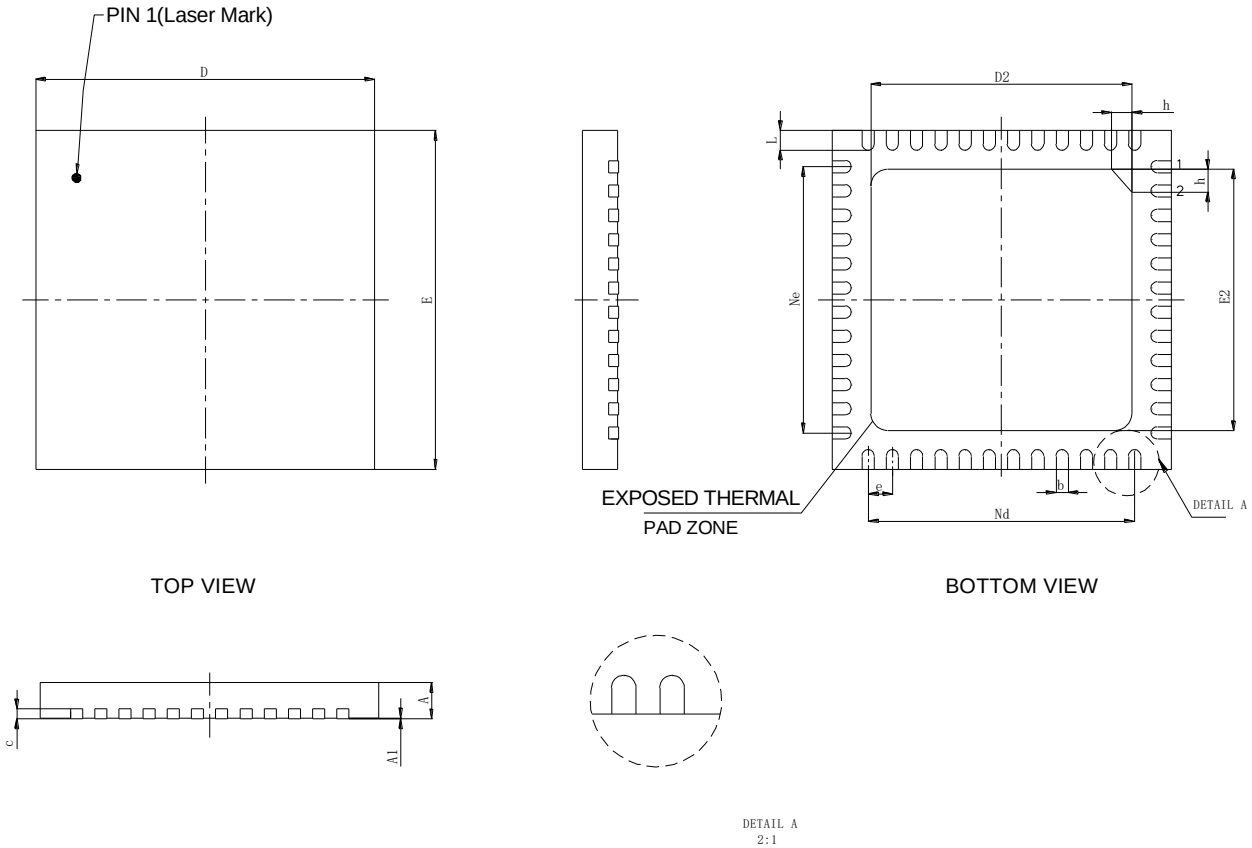



Unit:mm

| | |
|---|---|
| D | 5.00 |
| E | 5.00 |
| D2 | 2.28 |
| E2 | 2.28 |
| P | 4.90 |
| e | 0.50 |
| L | 0.85 |
| b | 0.30 |

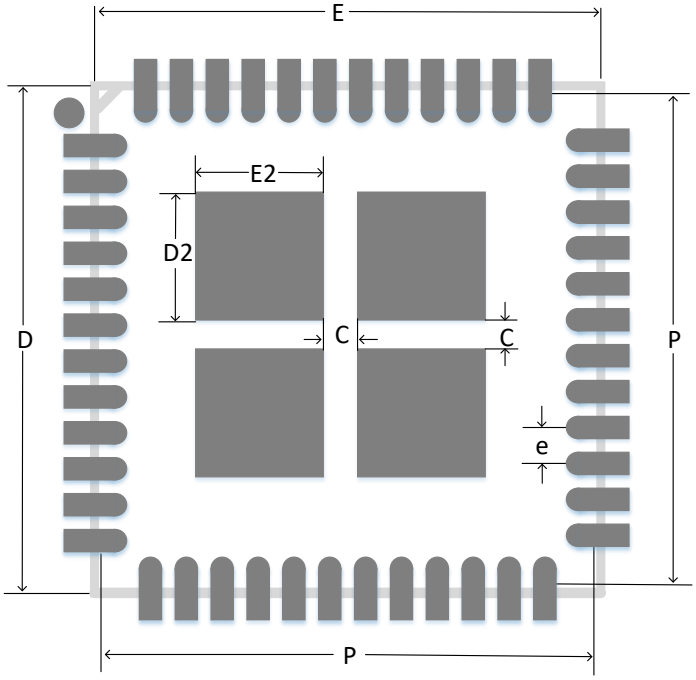
# 4.3 QN48X Package Outline (7mm x 7mm)

**Figure 4-5 Package Outline QN48X**




| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0 | 0.02 | 0.05 |
| b | 0.18 | 0.25 | 0.30 |
| c | 0.18 | 0.20 | 0.23 |
| D | 6.90 | 7.00 | 7.10 |
| D2 | 5.30 | 5.40 | 5.50 |
| e | 0.50BSC | | |
| Ne | 5.50BSC | | |
| Nd | 5.50BSC | | |
| E | 6.90 | 7.00 | 7.10 |
| E2 | 5.30 | 5.40 | 5.50 |
| L | 0.35 | 0.40 | 0.45 |
| h | 0.30 | 0.35 | 0.40 |

**Figure 4-6 Recommended PCB Layout QN48X**



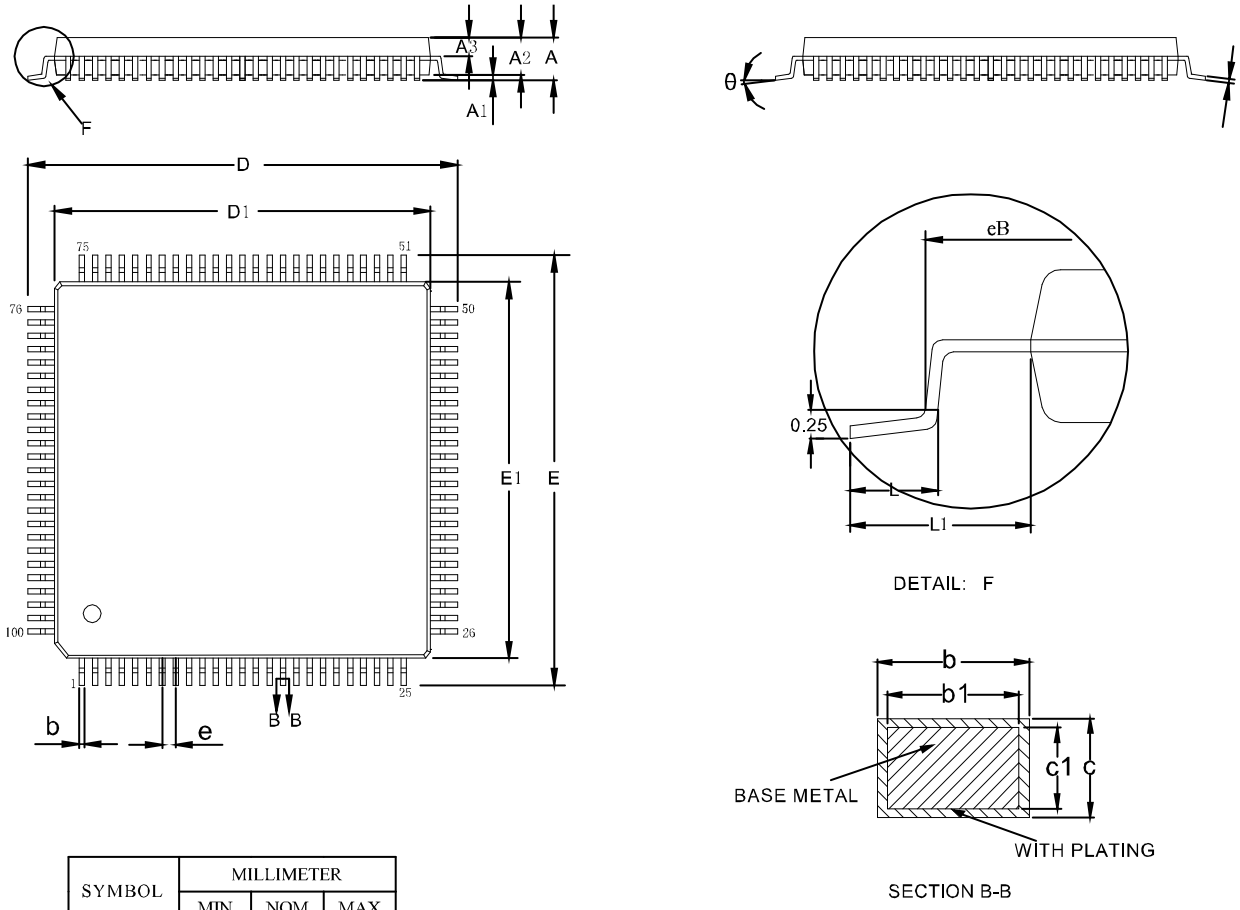

TOP VIEW


Unit:mm

| | |
|---|---|
| D | 7.00 |
| E | 7.00 |
| D2 | 1.74 |
| E2 | 1.74 |
| P | 6.90 |
| e | 0.50 |
| L | 0.85 |
| b | 0.30 |
| C | 0.68 |

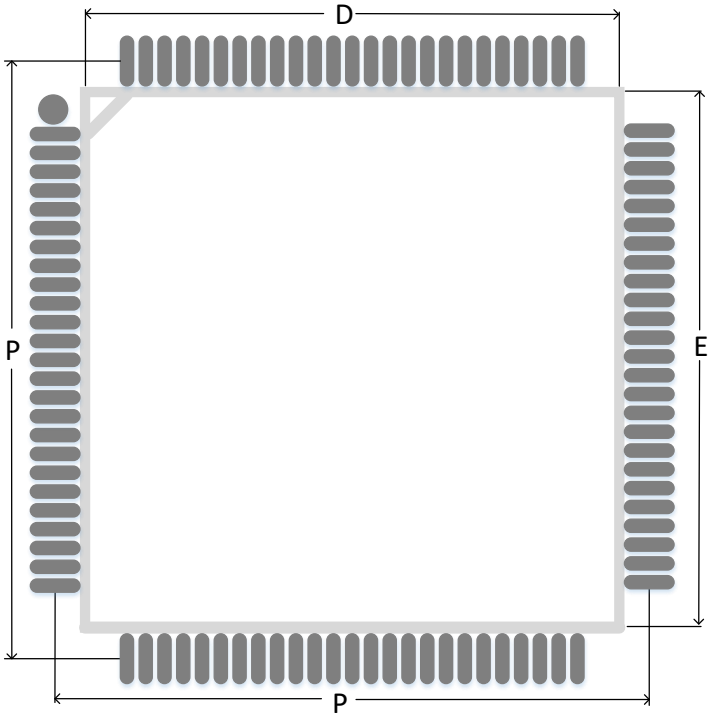
# 4.4 LQ100G Package Outline (14mm x 14mm)

**Figure 4-7 Package Outline LQ100G**




| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | — | — | 1.60 |
| A1 | 0.05 | — | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| A3 | 0.59 | 0.64 | 0.69 |
| b | 0.18 | — | 0.26 |
| b1 | 0.17 | 0.20 | 0.23 |
| c | 0.13 | — | 0.17 |
| c1 | 0.12 | 0.13 | 0.14 |
| D | 15.80 | 16.00 | 16.20 |
| D1 | 13.90 | 14.00 | 14.10 |
| E | 15.80 | 16.00 | 16.20 |
| E1 | 13.90 | 14.00 | 14.10 |
| eB | 15.05 | — | 15.35 |
| e | 0.50BSC | | |
| L | 0.45 | — | 0.75 |
| L1 | 1.00REF | | |
| 0 | 0 | — | 7° |

**Figure 4-8 Recommended PCB Layout LQ100G**

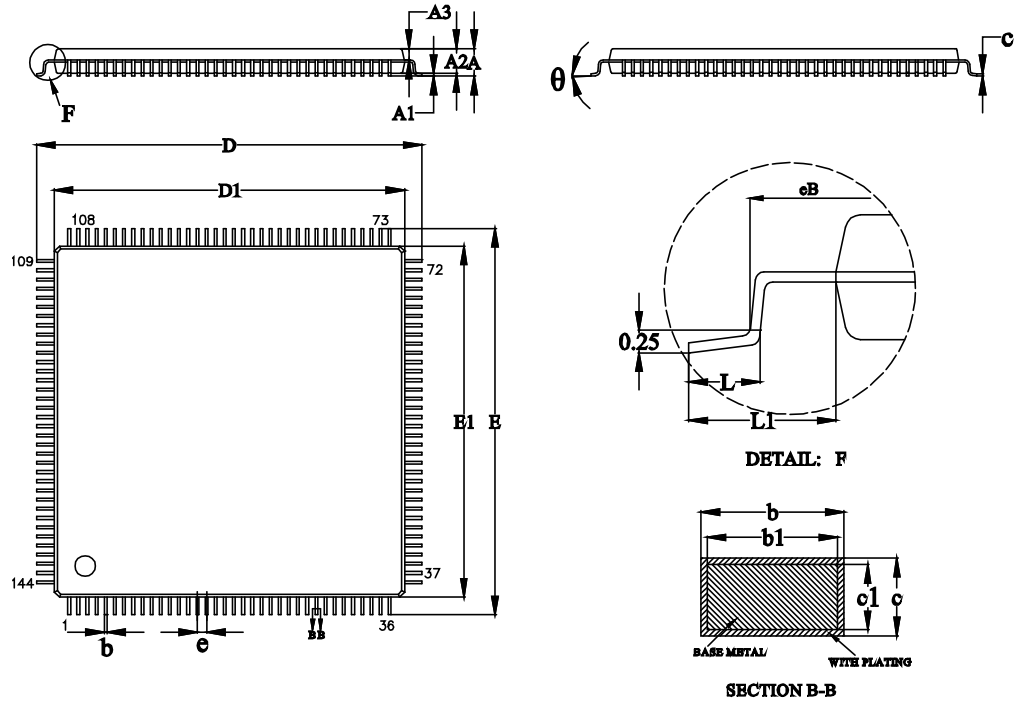



**Unit:mm**

| | |
|---|---|
| D | 14.00 |
| E | 14.00 |
| P | 15.40 |
| e | 0.50 |
| L | 1.55 |
| b | 0.30 |

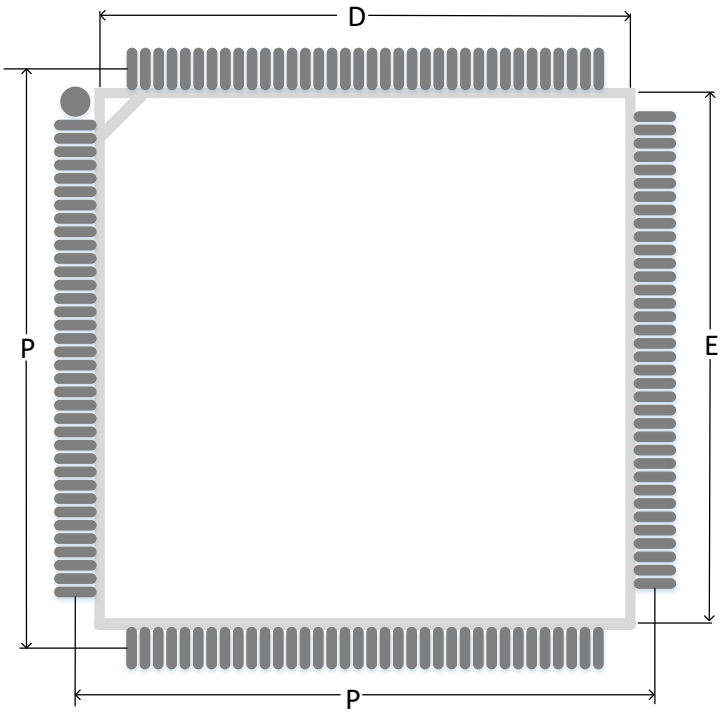
# 4.5 LQ144/LQ144P Package Outline (20mm x 20mm)

**Figure 4-9 Package Outline LQ144/LQ144P**

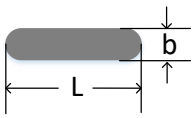



| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | — | — | 1.60 |
| A1 | 0.05 | — | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| A3 | 0.59 | 0.64 | 0.69 |
| b | 0.18 | — | 0.26 |
| b1 | 0.17 | 0.20 | 0.23 |
| c | 0.13 | — | 0.17 |
| c1 | 0.12 | 0.13 | 0.14 |
| D | 21.80 | 22.00 | 22.20 |
| D1 | 19.90 | 20.00 | 20.10 |
| E | 21.80 | 22.00 | 22.20 |
| E1 | 19.90 | 20.00 | 20.10 |
| e | 0.50BSC | | |
| L | 0.45 | — | 0.75 |
| L1 | 1.00REF | | |
| θ | 0 | — | 7° |

**Figure 4-10 Recommended PCB Layout LQ144/LQ144P**




TOP VIEW

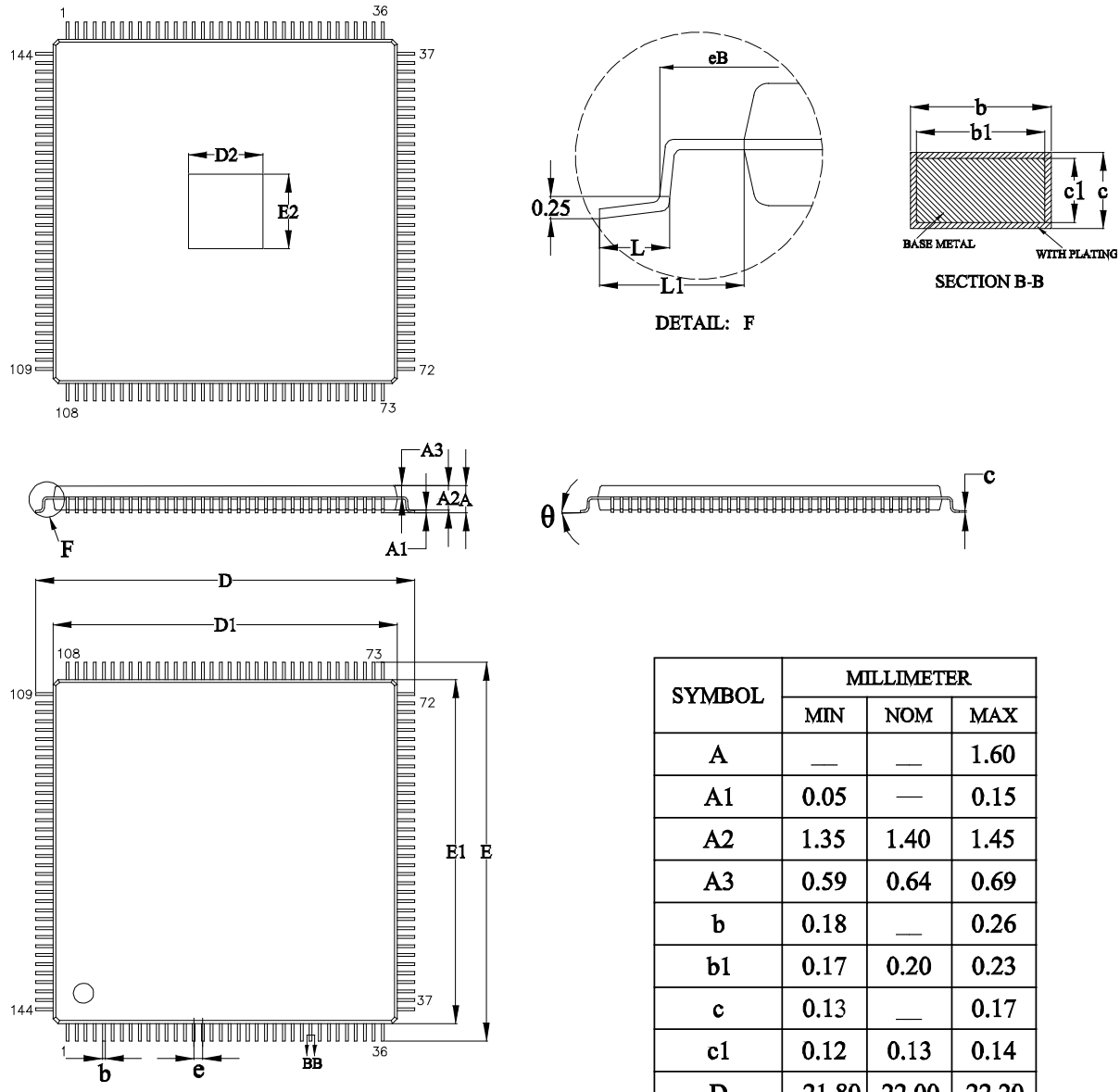



**Unit:mm**

| | |
|---|---|
| D | 20.00 |
| E | 20.00 |
| P | 21.40 |
| e | 0.50 |
| L | 1.55 |
| b | 0.30 |

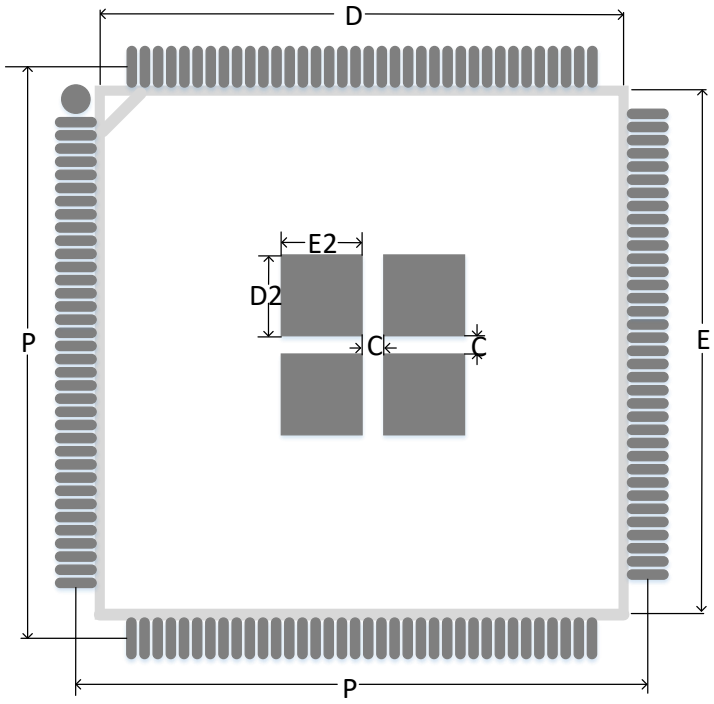
# 4.6 EQ144G Package Outline (20mm x 20mm)

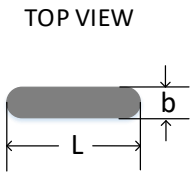
**Figure 4-11 Package Outline EQ144G**




| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | — | — | 1.60 |
| A1 | 0.05 | — | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| A3 | 0.59 | 0.64 | 0.69 |
| b | 0.18 | — | 0.26 |
| b1 | 0.17 | 0.20 | 0.23 |
| c | 0.13 | — | 0.17 |
| c1 | 0.12 | 0.13 | 0.14 |
| D | 21.80 | 22.00 | 22.20 |
| D1 | 19.90 | 20.00 | 20.10 |
| E | 21.80 | 22.00 | 22.20 |
| E1 | 19.90 | 20.00 | 20.10 |
| e | 0.50BSC | | |
| eB | 21.15 | | 21.40 |
| L | 0.45 | — | 0.75 |
| D2 | 5.00REF | | |
| E2 | 5.00REF | | |
| L1 | 1.00REF | | |
| θ | 0 | — | 7° |

**Figure 4-12 Recommended PCB Layout EQ144G**



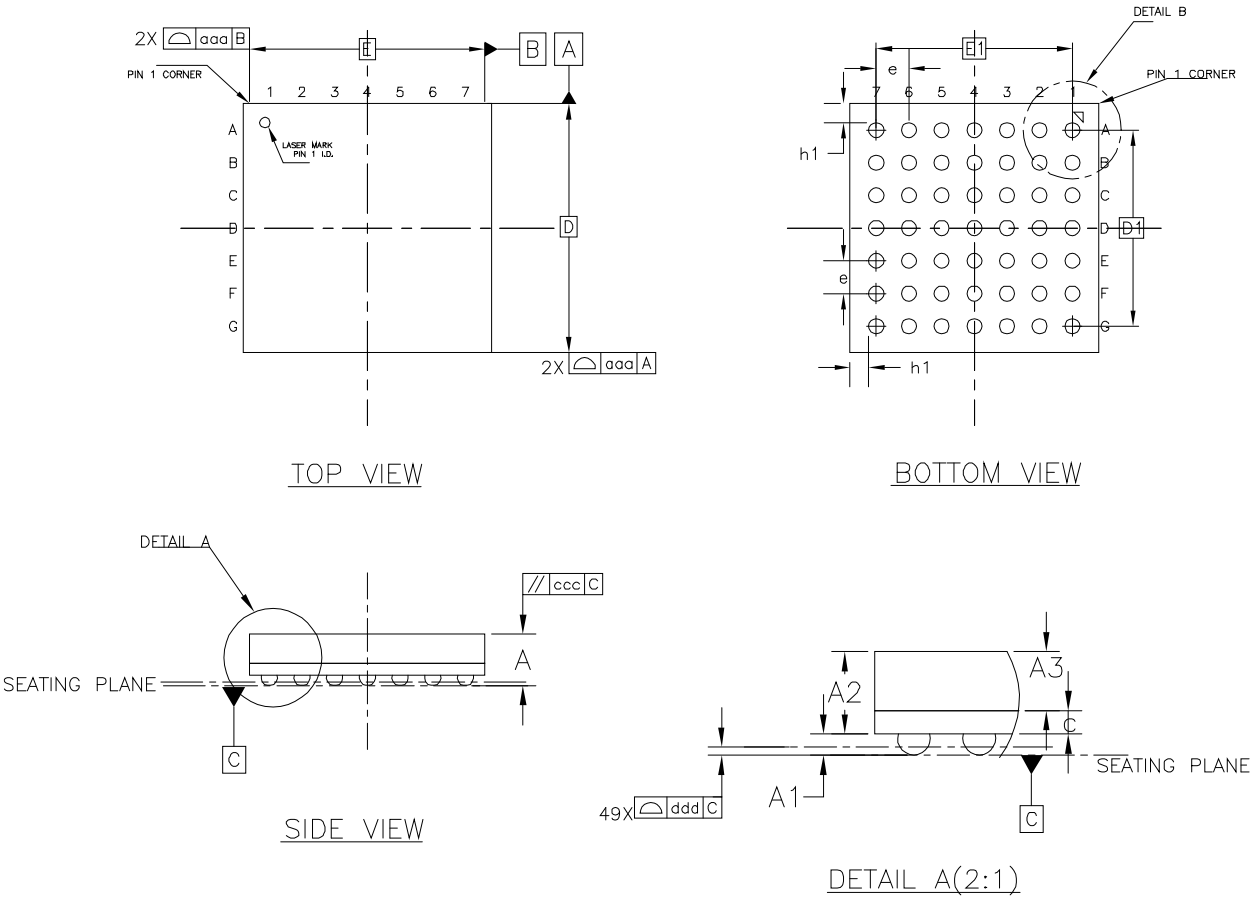




**Unit:mm**

| | |
|---|---|
| D | 20.00 |
| E | 20.00 |
| P | 21.40 |
| D2 | 1.58 |
| E2 | 1.58 |
| C | 0.40 |
| e | 0.50 |
| L | 1.55 |
| b | 0.62 |

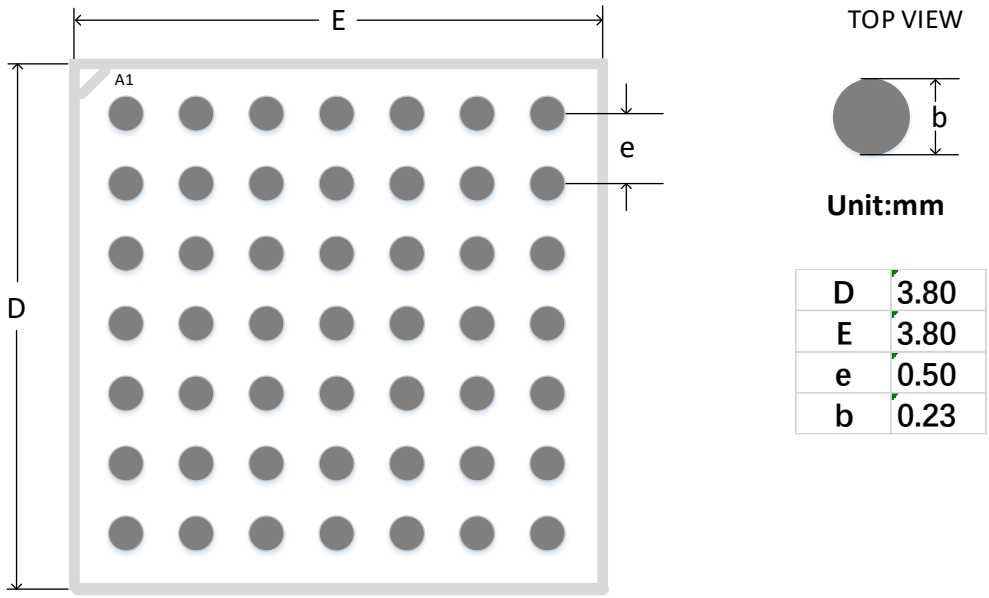
# 4.7 MG49P/MG49PG/MG49G Package Outline (3.8mm x 3.8mm)

**Figure 4-13 Package Outline MG49P/ MG49PG/MG49G**




| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.71 | 0.79 | 0.87 |
| A1 | 0.11 | 0.16 | 0.21 |
| A2 | 0.58 | 0.63 | 0.68 |
| A3 | | 0.45 BASIC | |
| c | 0.15 | 0.18 | 0.21 |
| D | 3.70 | 3.80 | 3.90 |
| D1 | | 3.00 BASIC | |
| E | 3.70 | 3.80 | 3.90 |
| E1 | | 3.00 BASIC | |
| e | | 0.50 BASIC | |
| b | 0.18 | 0.23 | 0.28 |
| h1 | | 0.285 REF | |
| aaa | | 0.10 | |
| ccc | | 0.08 | |
| ddd | | 0.08 | |
| eee | | 0.15 | |
| fff | | 0.05 | |

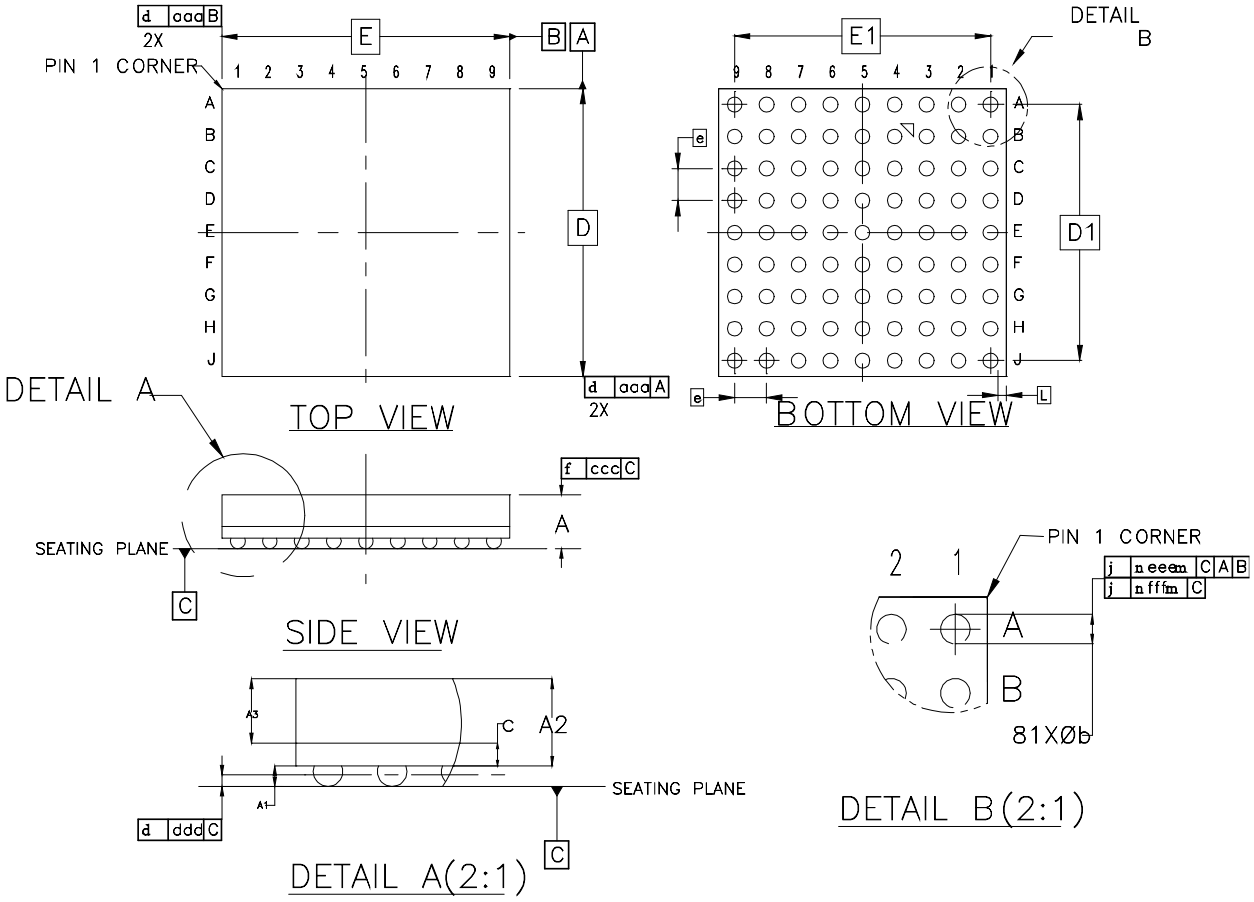
**Figure 4-14 Recommended PCB Layout MG49P/MG49PG/MG49G**




| | |
|---|---|
| D | 3.80 |
| E | 3.80 |
| e | 0.50 |
| b | 0.23 |

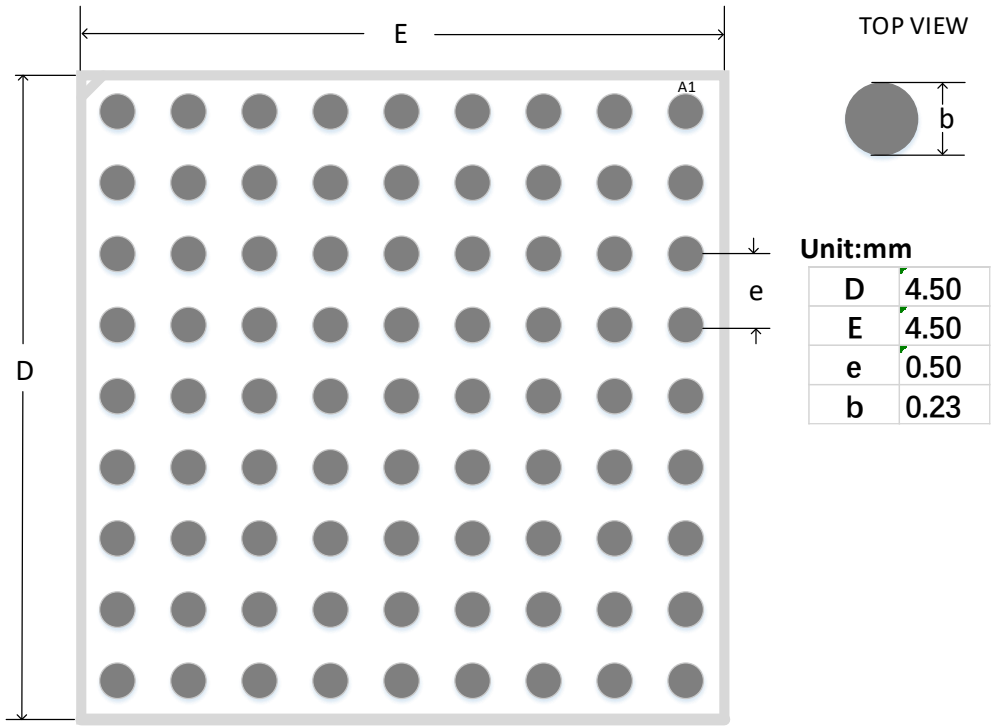
# 4.8 MG81P Package Outline (4.5mm x 4.5mm)

**Figure 4-15 Package Outline MG81P**



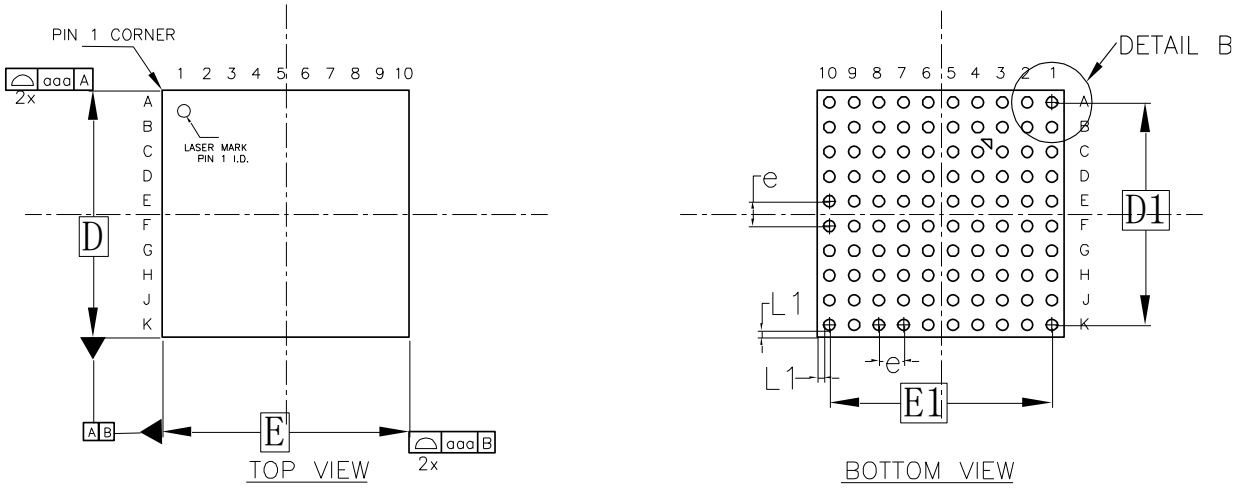

| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | -- | 0.84 | 0.90 |
| A1 | 0.11 | 0.16 | 0.21 |
| A2 | 0.63 | 0.68 | 0.73 |
| A3 | 0.50 BASIC | | |
| c | 0.15 | 0.18 | 0.21 |
| D | 4.40 | 4.50 | 4.60 |
| D1 | 4.00 BASIC | | |
| E | 4.40 | 4.50 | 4.60 |
| E1 | 4.00 BASIC | | |
| e | 0.50 BASIC | | |
| b | 0.18 | 0.23 | 0.28 |
| L | 0.135 TYP | | |
| aaa | 0.10 | | |
| ccc | 0.15 | | |
| ddd | 0.10 | | |
| eee | 0.15 | | |
| fff | 0.05 | | |

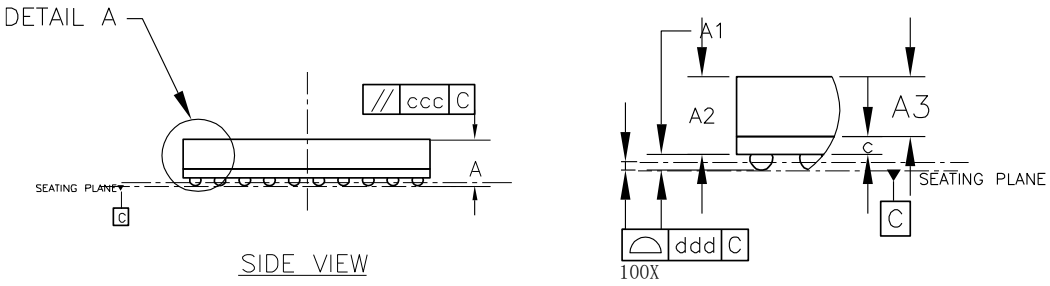
**Figure 4-16 Recommended PCB Layout MG81P**

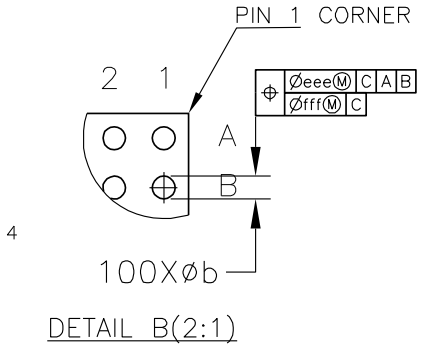


# 4.9 MG100P/MG100PF/MG100PA/MG100PT MG100PS Package Outline (5mm x 5mm)

**Figure 4-17 Package Outline MG100P/MG100PF/MG100PA/ MG100PT**

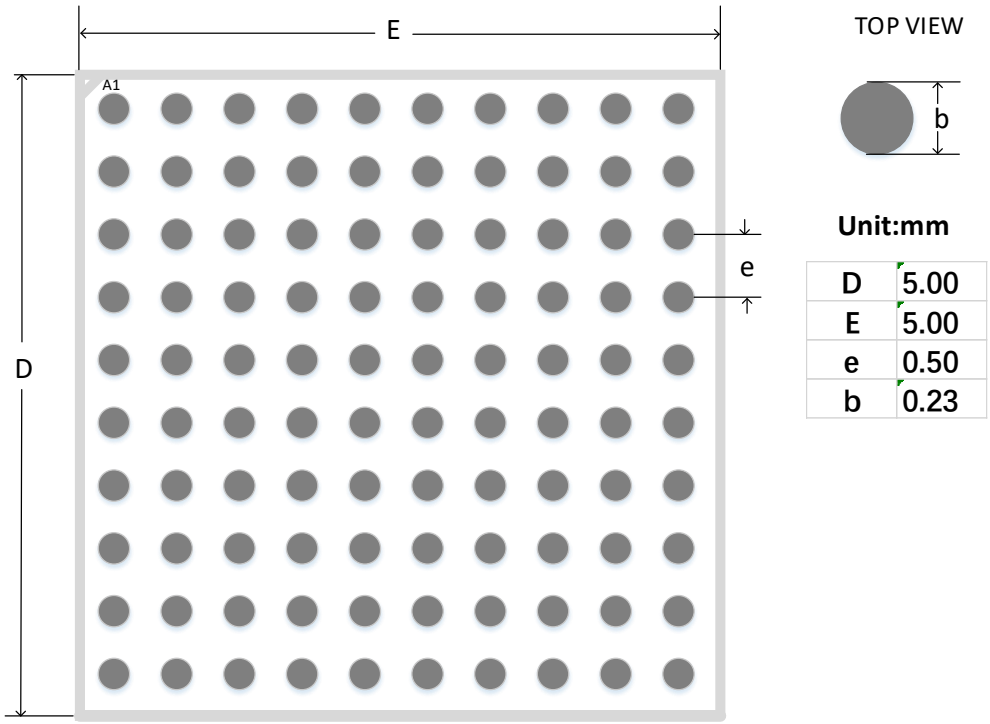


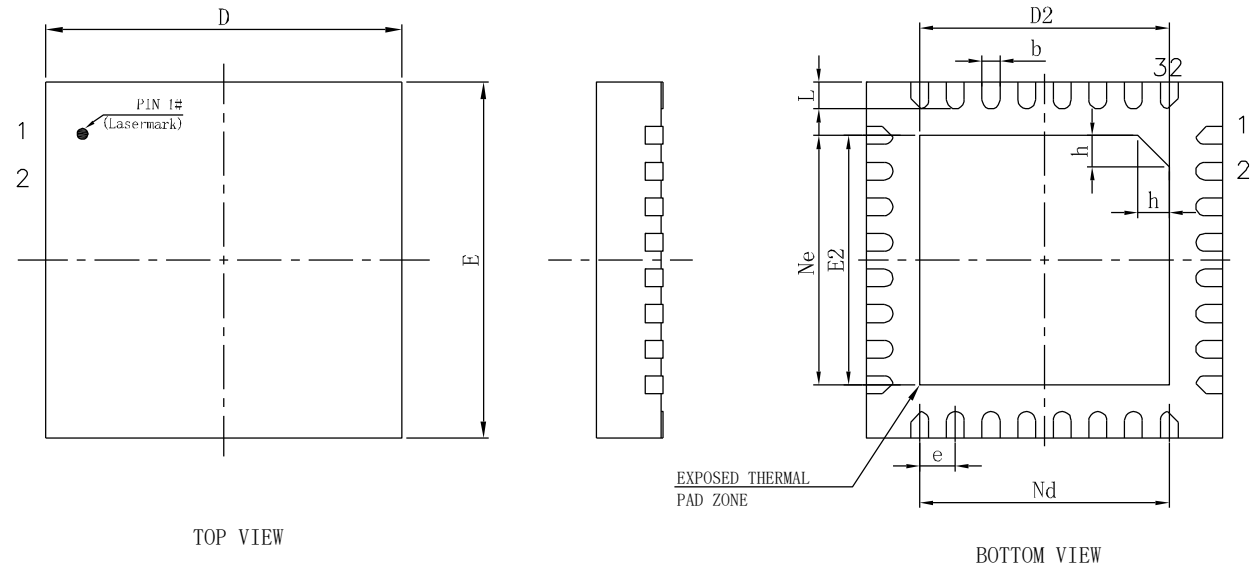

| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | -- | 0.94 | 1.00 |
| A1 | 0.11 | 0.16 | 0.21 |
| A2 | 0.73 | 0.78 | 0.83 |
| A3 | 0.60 BASIC | | |
| c | 0.15 | 0.18 | 0.21 |
| D | 4.90 | 5.00 | 5.10 |
| D1 | 4.50 BASIC | | |
| E | 4.90 | 5.00 | 5.10 |
| E1 | 4.50 BASIC | | |
| e | 0.50 BASIC | | |
| b | 0.18 | 0.23 | 0.28 |
| L1 | 0.135 REF | | |
| aaa | 0.15 | | |
| ccc | 0.15 | | |
| ddd | 0.10 | | |
| eee | 0.15 | | |
| fff | 0.05 | | |

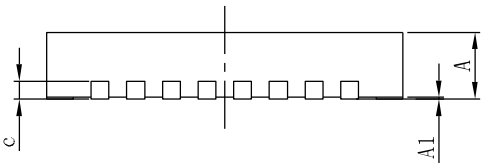
**Figure 4-18 Recommended PCB Layout**
**MG100P/MG100PF/MG100PA/MG100PT/MG100PS**



# 4.10 FN32G Package Outline (4mm x 4mm)

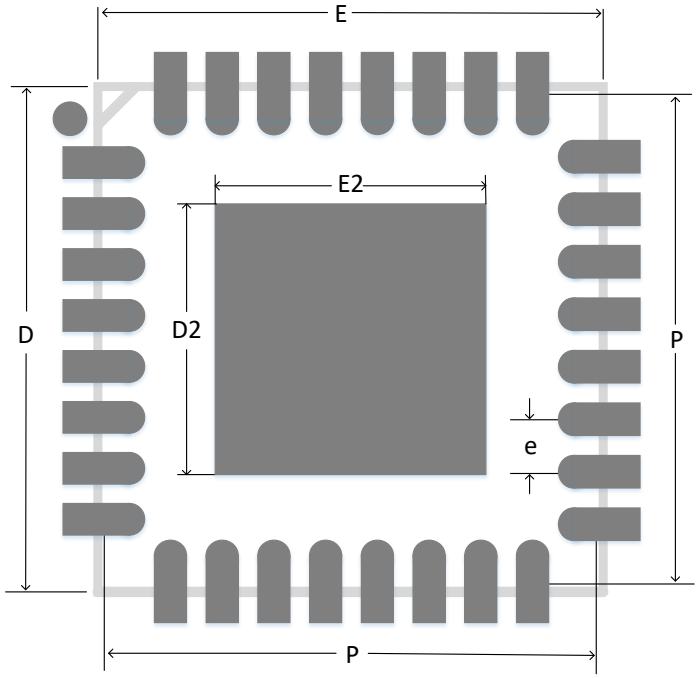
**Figure 4-19 Package Outline FN32G**




| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0 | 0.02 | 0.05 |
| b | 0.15 | 0.20 | 0.25 |
| c | 0.18 | 0.20 | 0.25 |
| D | 3.90 | 4.00 | 4.10 |
| D2 | 2.70 | 2.80 | 2.90 |
| e | 0.40BSC | | |
| Ne | 2.80BSC | | |
| Nd | 2.80BSC | | |
| E | 3.90 | 4.00 | 4.10 |
| E2 | 2.70 | 2.80 | 2.90 |
| L | 0.25 | 0.30 | 0.35 |
| h | 0.30 | 0.35 | 0.40 |

**Figure 4-20 Recommended PCB Layout FN32G**




Unit:mm

| | |
|---|---|
| D | 4.00 |
| E | 4.00 |
| D2 | 1.83 |
| E2 | 1.83 |
| P | 4.10 |
| e | 0.40 |
| L | 0.70 |
| b | 0.20 |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