GOWIN
PROGRAMMING FOR THE FUTURE

GW2AR series of FPGA Products

Package & Pinout User Guide

UG229-1.6.2E, 02/02/2024

Disclaimer

GOWINSEMI assumes no liability and provides no warranty (either expressed or implied) and is not responsible for any damage incurred to your hardware, software, data, or property resulting from usage of the materials or intellectual property except as outlined in the GOWINSEMI Terms and Conditions of Sale. GOWINSEMI may make changes to this document at any time without prior notice. Anyone relying on this documentation should contact GOWINSEMI for the current documentation and errata.

Revision History

Date	Version	Description
05/11/2018	1.0.6E	Initial version published.
03/27/2019	1.1E	The EQ176 package added.
03/10/2020	1.2E	A note for the Max. user I/O added.
06/30/2020	1.2.1E	The package name of QN88/EQ144 (PSRAM embedded) updated to QN88P/EQ144P.
08/07/2020	1.3E	QN88PF and EQ144PF added.
05/14/2021	1.4E	PG256S added.
09/27/2022	1.5E	● GW2AR-18 PG256S removed. ● The note of A (NOM) value in QN88 added. ● EQ144/EQ144P/EQ144PF/EQ176 package outline modified.
03/10/2023	1.6E	GW2AR-18 LQ144 and LQ176 packages removed.
12/28/2023	1.6.1E	● The description of “2.5 Introduction to the I/O BANK” optimized. ● Recommended PCB Layout diagrams added.
02/02/2024	1.6.2E	“Figure 4-4 Recommended PCB Layout EQ144/EQ144P/EQ144PF” in “4 Package Diagrams” updated.

Contents

List of Figures

List of Tables

1 About This Guide

1.1 Purpose

This manual contains an introduction to the GW2AR series of FPGA products together with a definition of the pins, a list of pin numbers, distribution of pins, and package diagrams.

1.2 Related Documents

The latest user guides are available on GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

1. DS226, GW2AR series of FPGA Products Data Sheet
2. UG290, Gowin FPGA Products Programming and Configuration User Guide
3. UG115, GW2AR-18 Pinout

1.3 Abbreviations and Terminology

The abbreviations and terminologies used in this manual are delineated in Table 1-1 below.

Table 1-1 Abbreviations and Terminology

Abbreviations and Terminology	Name
EQ	eLQFP package
FPGA	Field Programmable Gate Array
QN	QFN package

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

The GW2AR series of FPGA products are the first generation products of Arora family, and they are one kind of SIP chip. Compared with GW2A series, the difference is that GW2AR series of integrates abundant SDRAM. GW2AR series of products also provide the high-performance DSP resources, high-speed LVDS interface, and abundant BSRAM memory resources. These embedded resources with a streamlined FPGA architecture and 55nm process make GW2AR series of FPGA products suitable for high-speed and low-cost applications.

GOWINSEMI provides a new generation of FPGA hardware development environment through the market-oriented independent research and development. This supports GW2AR series of FPGA products and applies to FPGA synthesizing, layout, place and routing, data bitstream generation and download, etc.

2.1 PB-Free Package

The GW2AR series of FPGA Products are PB free in line with the EU RoHS environmental directives. The substances used in the GW2AR series of FPGA products are in full compliance with the IPC-1752 standards.

2.2 Max. I/O Information and LVDS Pair

Table 2-1 Max. I/O Information and LVDS Pair

Package	Pitch (mm)	Size (mm)	E-pad Size(mm)	GW2AR-18
EQ144	0.5	20 x 20	9.74 x 9.74	120(35)
EQ144P	0.5	20 x 20	9.74 x 9.74	120(35)
EQ144PF	0.5	20 x 20	9.74 x 9.74	120(35)
QN88	0.4	10 x 10	6.74 x 6.74	66(22)
QN88P	0.4	10 x 10	6.74 x 6.74	66(22)
QN88PF	0.4	10 x 10	6.74 x 6.74	66(22)
EQ176	0.4	20 x 20	6 x 6	140(45)

Note!

- The package types in this manual are written with abbreviations. See 1.3 Abbreviations and Terminology.

- The JTAGSEL_N and JTAG pins are exclusive. The JTAGSEL_N pin and the four pins of JTAG (TCK, TDI, TDO, and TMS) cannot be simultaneously used as I/O.

2.3 Power Pin

Table 2-2 GW2AR Power Pin

VCC	VCCIO0	VCCIO1	VCCIO2
VCCIO3	VCCIO4	VCCIO5	VCCIO6
VCCIO7	VCCX	VSS	NC
VCCPLLL0	VCCPLLL1	VCCPLLR0	VCCPLLR1

2.4 Pin Quantity

Table 2-3 Quantity of GW2AR-18 Pins (Devices Embedded With SDRAM)

Pin Type		GW2AR-18		
		QN88	EQ144	EQ176
I/O Single ended/Differential pair/LVDS[1]	BANK0	8/4/2	19/8/4	19/9/6
	BANK1	9/4/4	12/6/6	18/9/8
	BANK2	4/2/1	12/6/3	12/5/3
	BANK3	17/6/3	24/11/6	20/8/4
	BANK4	8/3/3	17/8/6	19/9/8
	BANK5	10/5/5	16/8/5	18/8/5
	BANK6	9/4/4	12/6/3	17/8/6
	BANK7	1/0/0	8/4/2	17/6/5
Max. User I/O[2]		66	120	140
Differential Pair		28	57	62
True LVDS Output		22	35	45
VCC		4	0	4
VCC/VCCPLLL1[3]		0	4	0
VCCX		0	0	4
VCCX/ VCCIO2/ VCCIO6/VCCIO7[3]		3	4	0
VCCIO2/VCCIO3/VCCIO6/VCCIO7		0	0	8
VCCX/VCCIO2/VCCIO3/VCCIO6/ VCCIO7		0	0	0
VCCIO0		1	1	2
VCCIO1		1	1	2
VCCIO2		0	0	0
VCCIO3		1	2	0
VCCIO4		1	1	2
VCCIO5		1	1	2
VCCIO6		0	0	0
VCCIO7		0	0	0

Pin Type	GW2AR-18		
	QN88	EQ144	EQ176
VCCPLLL0	0	1	0
VCCPLLL1	1	0	1
VCCPLLR0	0	1	1
VCCPLLR1	1	1	1
VCCPLLL	0	0	0
VCCPLLR	0	0	0
VSS	7	6	8
MODE0	1	1	1
MODE1	1	1	1
MODE2	0	1	1
EXTR	1	1	1
JTAGSEL_N	0	0	0
NC	0	0	0

Table 2-4 Quantity of GW2AR-18 Pins (Devices Embedded With PSRAM)

Pin Type		GW2AR-18			
		QN88P	EQ144P	QN88PF	EQ144PF
I/O Single end/ Differential pair[1]	BANK0	8/4/2	19/8/4	8/4/2	19/8/4
	BANK1	9/4/4	12/6/6	9/4/4	12/6/6
	BANK2	4/2/1	12/6/3	4/2/1	12/6/3
	BANK3	17/6/3	24/11/6	17/6/3	24/11/6
	BANK4	8/3/3	17/8/6	8/3/3	17/8/6
	BANK5	10/5/5	16/8/5	10/5/5	16/8/5
	BANK6	9/4/4	12/6/3	9/4/4	12/6/3
	BANK7	1/0/0	8/4/2	1/0/0	8/4/2
Max. User I/O[2]		66	120	66	120
Differential Pair		28	57	28	57
True LVDS output		22	35	22	35
VCC		4	0	4	0
VCC/VCCPLLL1[3]		0	4	0	4
VCCX		0	0	0	0
VCCX/VCCIO1/VCCIO6[3]		2	0	2	0
VCCX/VCCIO4/VCCIO6[3]		0	2	0	2
VCCIO2/VCCIO73		2	3	0	0
VCCIO0		1	1	1	1
VCCIO1		0	1	0	1
VCCIO2		0	0	1	1
VCCIO3		1	2	1	2

Pin Type	GW2AR-18			
	QN88P	EQ144P	QN88PF	EQ144PF
VCCIO4	1	0	1	0
VCCIO5	1	1	1	1
VCCIO6	0	0	0	0
VCCIO7	0	0	1	2
VCCPLLL0	0	1	0	1
VCCPLLL1	1	0	1	0
VCCPLLR0	0	1	0	1
VCCPLLR1	1	1	1	1
VSS	7	6	7	6
MODE0	1	1	1	1
MODE1	1	1	1	1
MODE2	0	1	0	1
EXTR	1	1	1	1
JTAGSEL_N	0	0	0	0

Note!

- [1] Single end/Differential/LVDS I/O quantity include CLK pins, and download pins.
- [2] The JTAGSEL_N and JTAG pins are exclusive. The JTAGSEL_N pin and the four pins of JTAG (TCK, TDI, TDO, and TMS) cannot be simultaneously used as I/O.
- [3] Pin multiplexing.

2.5 Introduction to the I/O BANK

There are eight I/O Banks in the GW2AR series of FPGA products.

Please refer to DS226, GW2AR series of FPGA Products Data Sheet > 2.4 Input/Output Blocks for detailed Bank distribution schematic.

This manual provides an overview of the distribution view of the pins in the GW2AR series of FPGA products. Different IO Banks in GW2AR series of FPGA products are marked with different colors.

User I/O, power, and ground are also marked with different symbols and colors. The different symbols and colors used for different pins are defined as follows:

- "  " denotes I/Os in BANK0. The filling color changes with the BANK.
- "  " denotes I/Os in BANK1. The filling color changes with the BANK.
- "  " denotes I/Os in BANK2. The filling color changes with the BANK.
- "  " denotes I/Os in BANK3. The filling color changes with the BANK.
- "  " denotes I/Os in BANK4. The filling color changes with the BANK.
- "  " denotes I/Os in BANK5. The filling color changes with the BANK.
- "  " denotes I/Os in BANK6. The filling color changes with the BANK.
- "  " denotes I/Os in BANK7. The filling color changes with the BANK.
- "  " denotes VCC, VCCX, and VCCIO. The filling color does not change.
- "  " denotes VSS. The filling color does not change.
- "  " denotes NC.
- "  " denotes dedicated pins EXTR.

3 View of Pin Distribution

3.1 GW2AR-18 Pins Distribution View

3.1.1 View of QN88 Pins Distribution (Embedded with SDRAM)

Figure 3-1 View of GW2AR-18 QN88 Pins Distribution (Embedded with SDRAM)

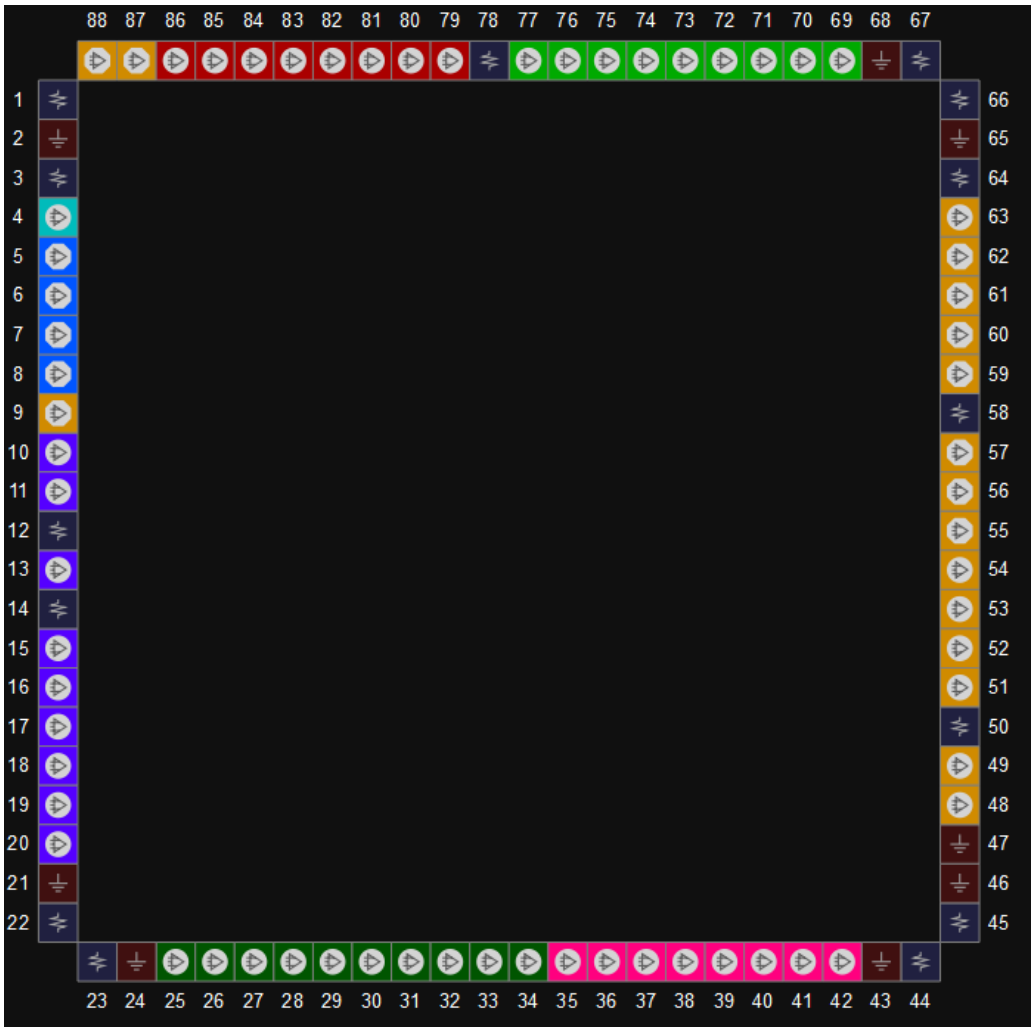


Table 3-1 Other pins in GW2AR-18 QN88 (Embedded with SDRAM)

VCC	1, 22, 45, 66
VCCIO0	78
VCCIO1	67
VCCIO3	58
VCCIO4	44
VCCIO5	23
VCCX/VCCIO2/VCCIO6/VCCIO7	3,12, 64
VCCPLLL1	14
VCCPLLR1	50
VSS	2, 21, 24, 43, 46, 65, 68
EXTR	47
MODE	87, 88

3.1.2 View of QN88P Pins Distribution (Embedded with PSRAM)

Figure 3-2 View of GW2AR-18 QN88P Pins Distribution (Embedded with PSRAM)

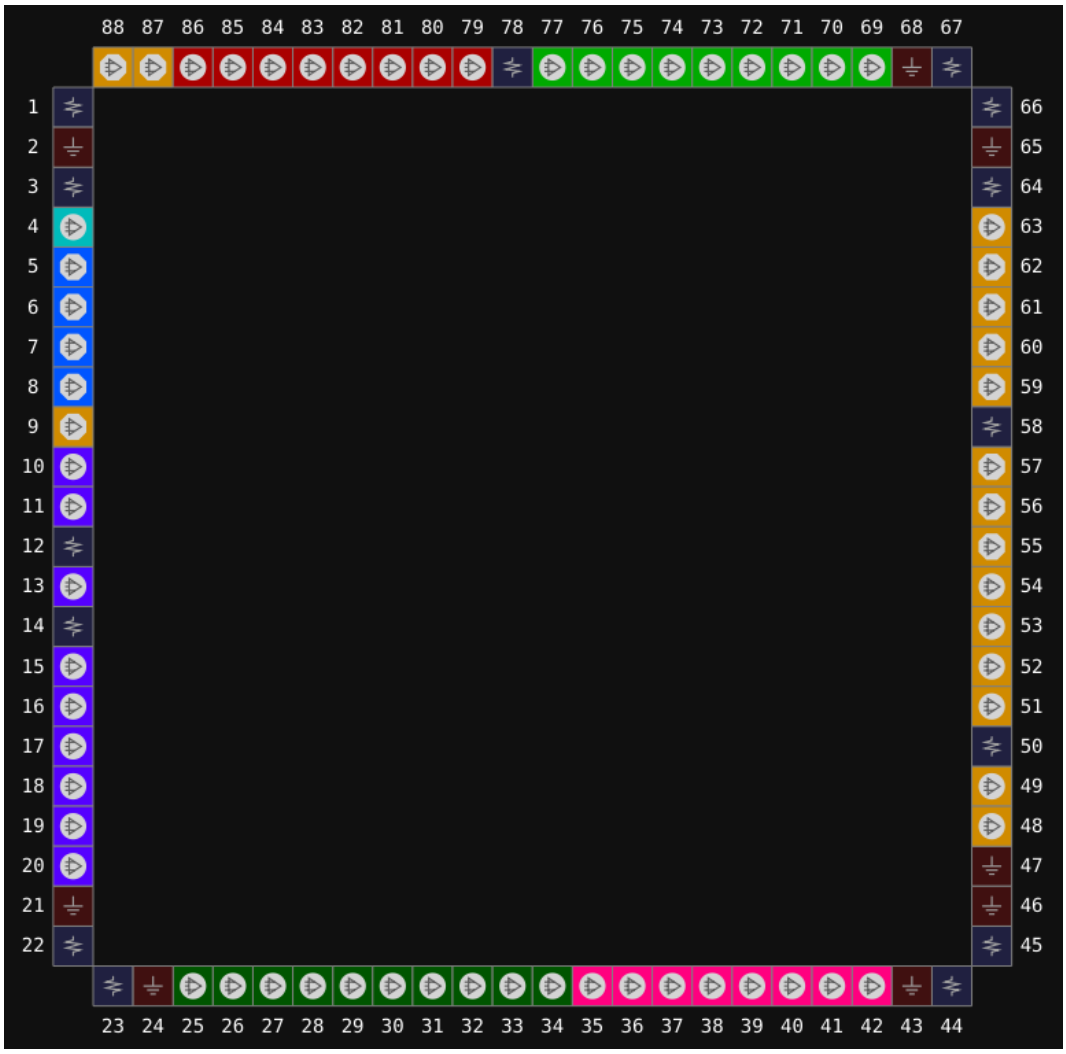


Table 3-2 Other pins in GW2AR-18 QN88P (Embedded with PSRAM)

VCC	1, 22, 45, 66
VCCIO0	78
VCCIO2/VCCIO7	3，64
VCCIO3	58
VCCIO4	44
VCCIO5	23
VCCX/VCCIO1/VCCIO6	12, 67
VCCPLLL1	14
VCCPLLR1	50
VSS	2, 21, 24, 43, 46, 65, 68
EXTR	47
MODE	87, 88

3.1.3 View of QN88PF Pins Distribution (Embedded with PSRAM)

Figure 3-3 View of GW2AR-18 QN88PF Pins Distribution (Embedded with PSRAM)

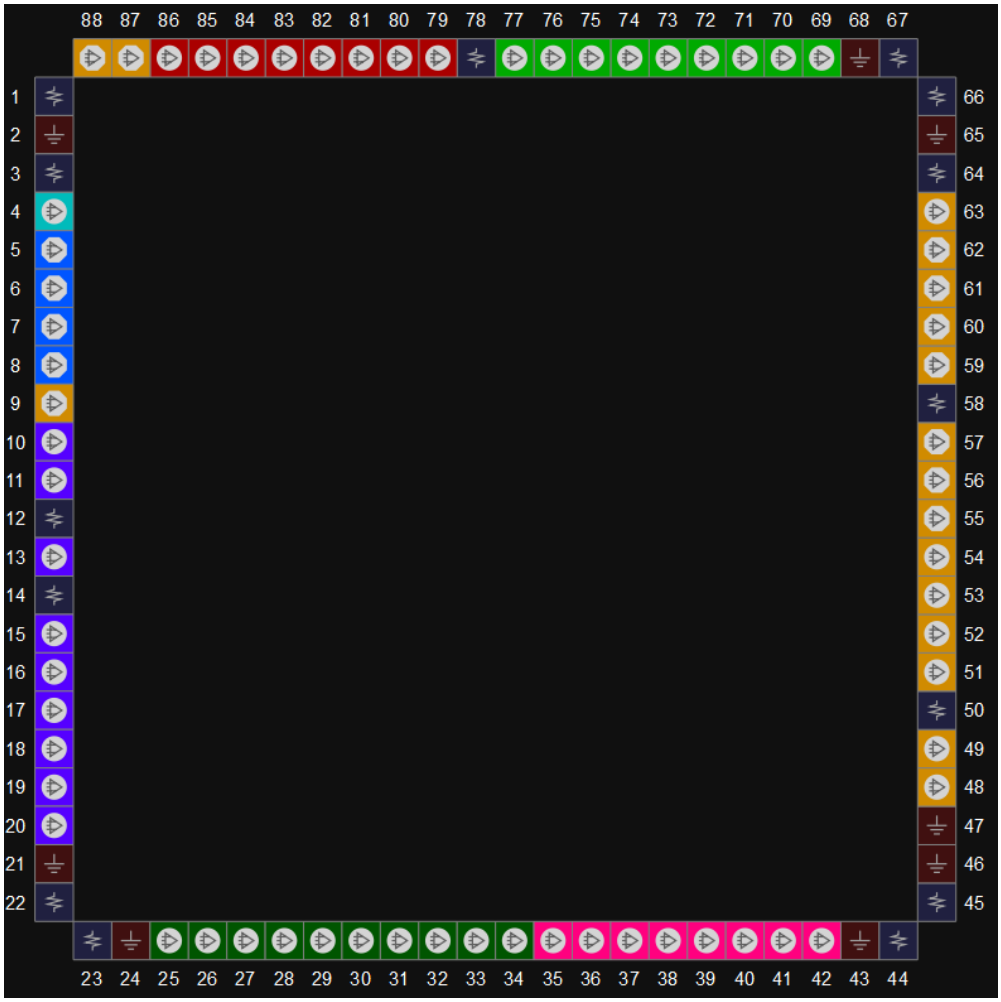


Table 3-3 Other pins in GW2AR-18 QN88PF (Embedded with PSRAM)

VCC	1, 22, 45, 66
VCCIO0	78
VCCIO2	64
VCCIO3	58
VCCIO4	44
VCCIO5	23
VCCIO7	3
VCCX/VCCIO1/VCCIO6	12, 67
VCCPLLL1	14
VCCPLLR1	50
VSS	2, 21, 24, 43, 46, 65, 68
EXTR	47
MODE	87, 88

3.1.4 View of EQ144 Pins Distribution (Embedded with SDRAM)

Figure 3-4 GW2AR-18 EQ144 Pins Distribution View (Embedded with SDRAM)

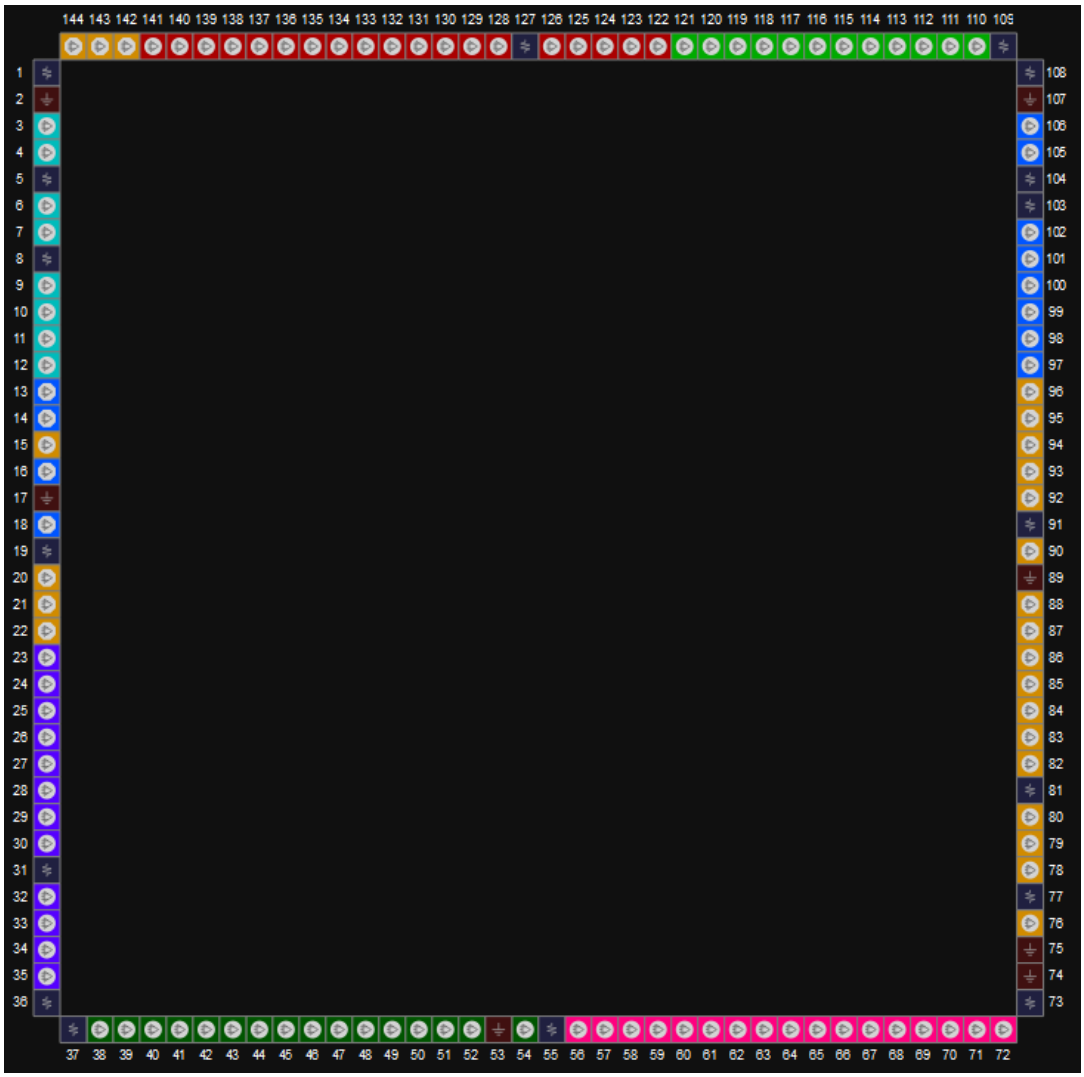


Table 3-4 Other pins in GW2AR-18 EQ144 (Embedded with SDRAM)

VCC/VCCPLLL1	1, 36, 73, 108
VCCIO0	127
VCCIO1	109
VCCIO3	77, 91
VCCIO4	55
VCCIO5	37
VCCX/ VCCIO2/ VCCIO6/ VCCIO7	5,19,31,103
VCCPLLL0	8
VCCPLLR0	104
VCCPLLR1	81
VSS	2, 17, 53, 74, 89, 107
EXTR	75
MODE	142, 143, 144

3.1.5 View of EQ144P Pins Distribution (Embedded with PSRAM)

Figure 3-5 GW2AR-18 EQ144P Pins Distribution View (Embedded with PSRAM)

Table 3-5 Other pins in GW2AR-18 EQ144P (Embedded with PSRAM)

VCC/VCCPLLL1	1, 36, 73, 108
VCCIO0	127
VCCIO1	109
VCCIO3	77, 91
VCCIO5	37
VCCIO2/VCCIO7	5,19,103
VCCX/VCCIO4/VCCIO6	31,55
VCCPLLL0	8
VCCPLLR0	104
VCCPLLR1	81
VSS	2, 17, 53, 74, 89, 107
EXTR	75
MODE	142, 143, 144

3.1.6 View of EQ144PF Pins Distribution (Embedded with PSRAM)

Figure 3-6 GW2AR-18 EQ144PF Pins Distribution View (Embedded with PSRAM)

Table 3-6 Other pins in GW2AR-18 EQ144PF (Embedded with PSRAM)

VCC/VCCPLLL1	1, 36, 73, 108
VCCIO0	127
VCCIO1	109
VCCIO2	103
VCCIO3	77, 91
VCCIO5	37
VCCIO7	5,19
VCCX/VCCIO4/VCCIO6	31,55
VCCPLLL0	8
VCCPLLR0	104
VCCPLLR1	81
VSS	2, 17, 53, 74, 89, 107
EXTR	75
MODE	142, 143, 144

3.1.7 View of EQ176 Pins Distribution (Embedded with SDRAM)

Figure 3-7 GW2AR-18 EQ176 Pins Distribution View (Embedded with SDRAM)

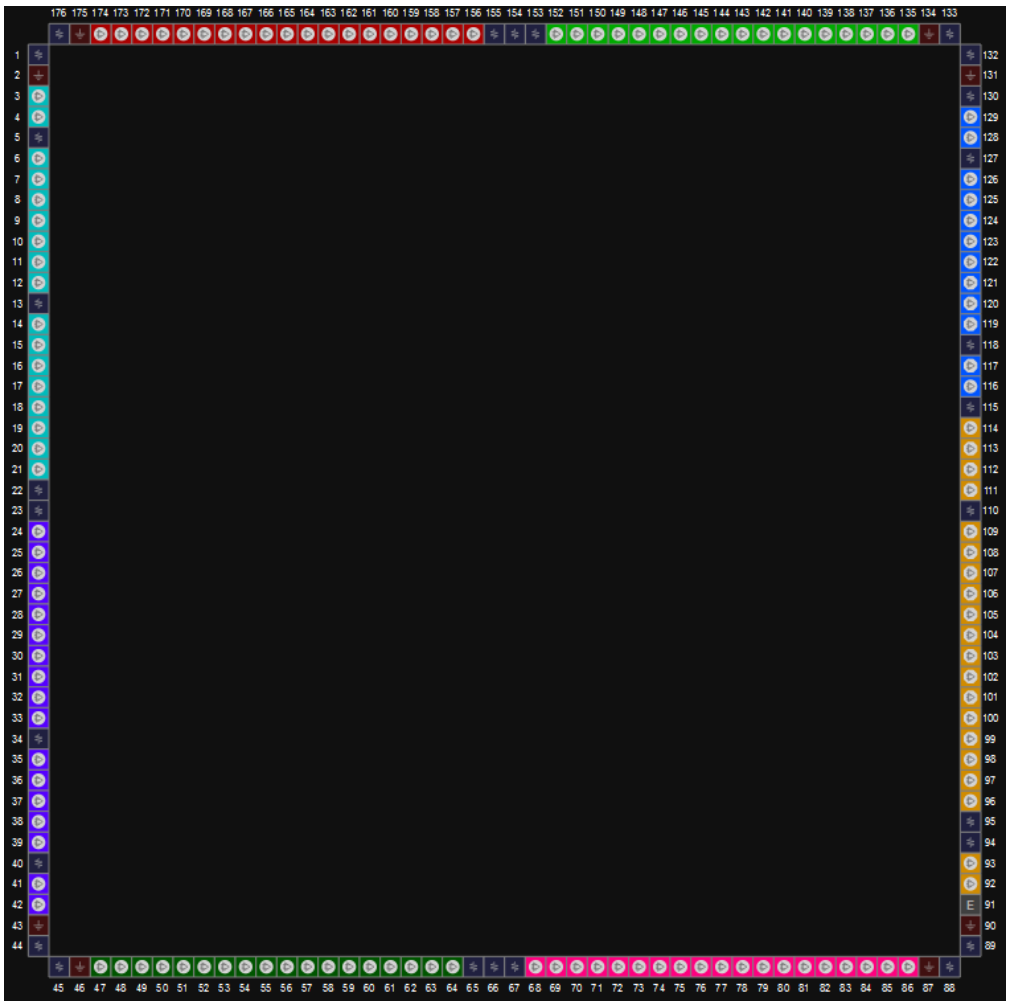


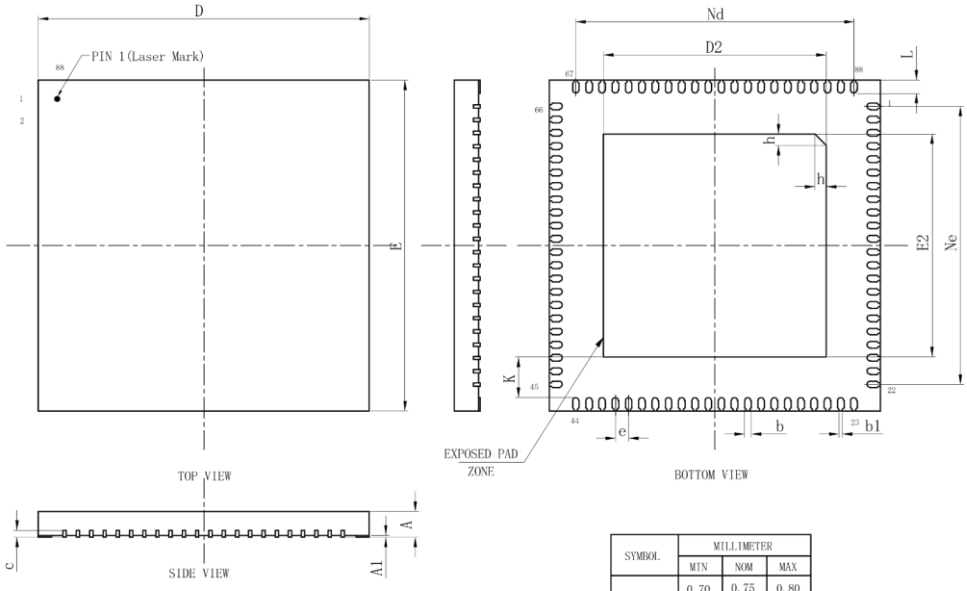
Table 3-7 Other pins in GW2AR-18 EQ176 (Embedded with SDRAM)

VCC	1, 44, 89, 132
VCCIO0	155, 176
VCCIO1	133, 153
VCCIO4	67, 88
VCCIO5	45, 65
VCCX	23, 66, 115, 154
VCCIO2/VCCIO3/VCCIO6/VCCIO7	5,13,22,40,95,110,130
VCCPLLL1	34
VCCPLLR0	127
VCCPLLR1	94
VSS	2, 43, 46, 87, 90, 131, 134, 175
EXTR	91
MODE	111, 112, 113

4 Package Diagrams

4.1 QN88/QN88P/QN88PF Package Outline (10mm x 10mm)

Figure 4-1 Package Outline QN88/QN88P/QN88PF

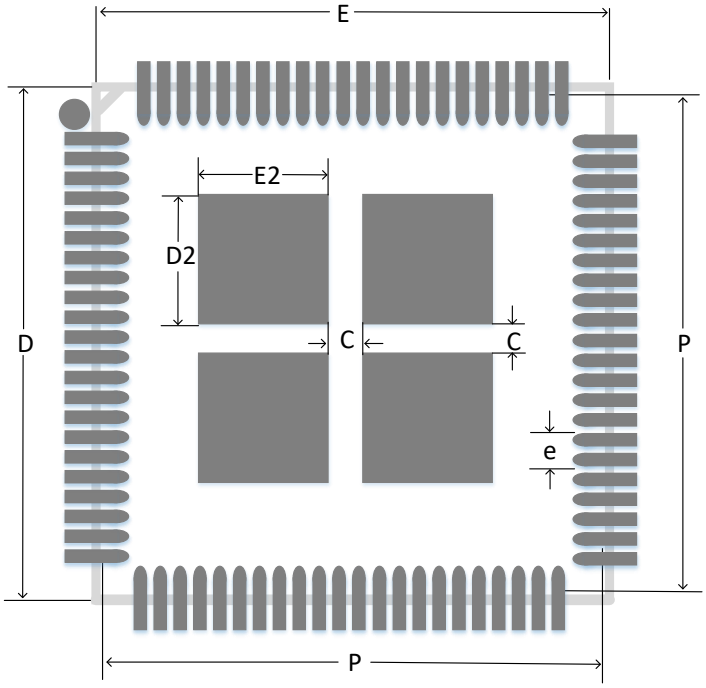


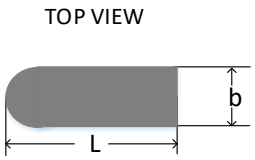
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
	0.80	0.85	0.90
	0.85	0.90	0.95
A1	0	0.02	0.05
b	0.15	0.20	0.25
b1	0.10REF		
c	0.18	0.20	0.25
D	9.90	10.00	10.10
D2	6.64	6.74	6.84
e	0.40BSC		
Nd	8.40REF		
E	9.90	10.00	10.10
E2	6.64	6.74	6.84
Ne	8.40REF		
L	0.30	0.40	0.50
K	0.20	-	-
h	0.30	0.35	0.40

Note!

- For GW2AR-LV18QN88, the value of A (NOM) is 0.9mm.
- For GW2AR-LV18QN88P and GW2AR-LV18QN88PF, the value of A (NOM) is 0.9mm.

Figure 4-2 Recommended PCB Layout QN88/QN88P/QN88PF



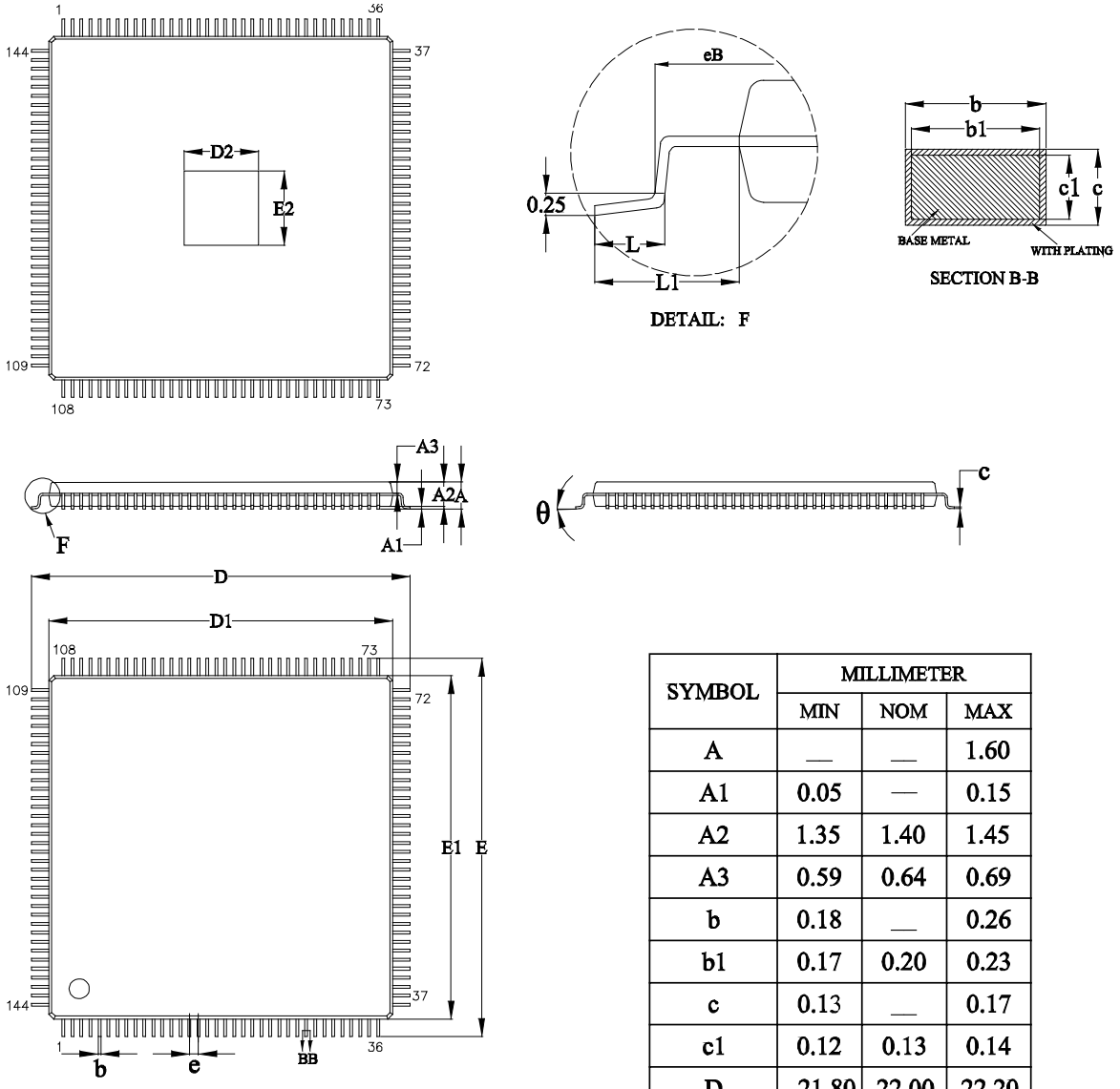


Unit:mm

D	10.00
E	10.00
D2	2.16
E2	2.16
P	9.90
e	0.40
L	0.85
b	0.20
C	0.84

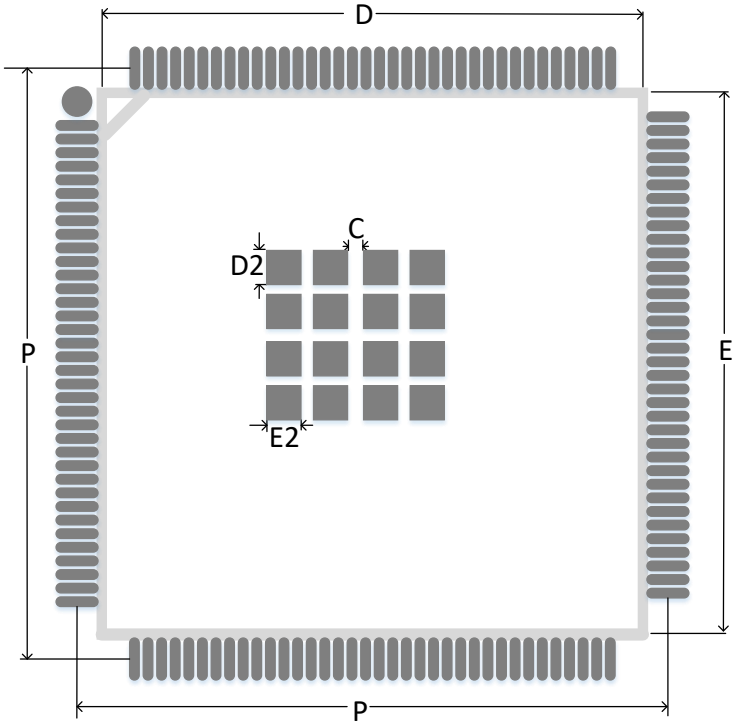
4.2 EQ144/ EQ144P/EQ144PF Package Outline (20mm x 20mm)

Figure 4-3 Package Outline EQ144/EQ144P/EQ144PF

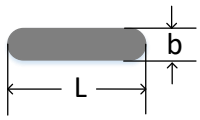


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	21.80	22.00	22.20
D1	19.90	20.00	20.10
E	21.80	22.00	22.20
E1	19.90	20.00	20.10
e	0.50BSC		
eB	21.15		21.40
L	0.45	—	0.75
D2	9.74REF		
E2	9.74REF		
L1	1.00REF		
θ	0	—	7°

Figure 4-4 Recommended PCB Layout EQ144/EQ144P/EQ144PF



TOP VIEW

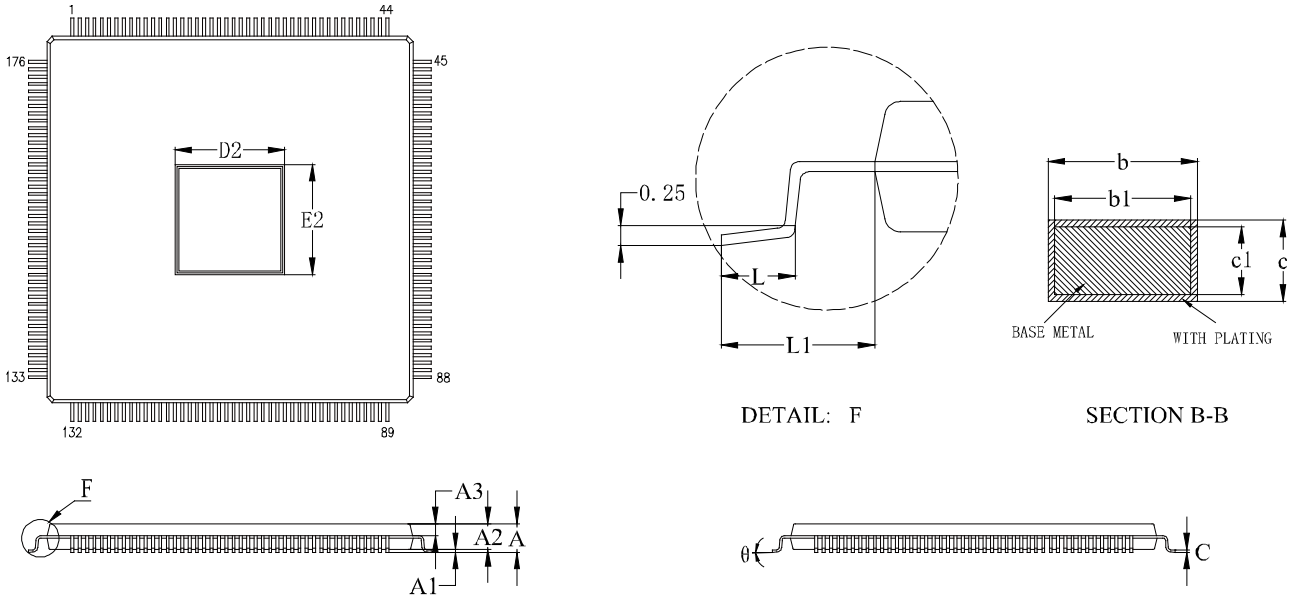


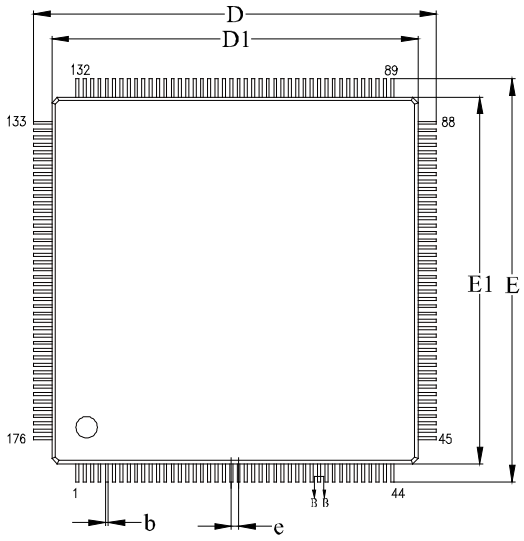
Unit:mm

D	20.00
E	20.00
P	21.40
D2	1.54
E2	1.54
C	1.16
e	0.50
L	1.50
b	0.30

4.3 EQ176 Package Outline (20mm x 20mm)

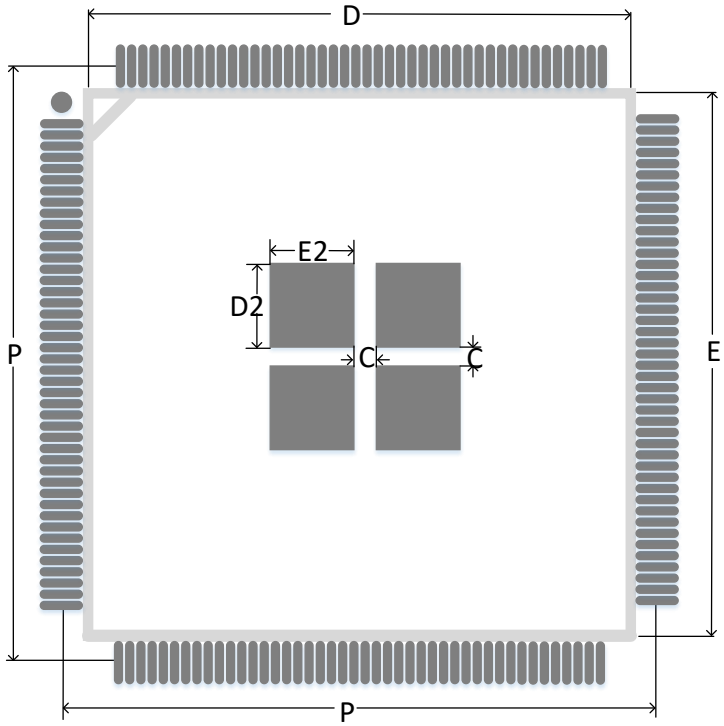
Figure 4-5 Package Outline EQ176

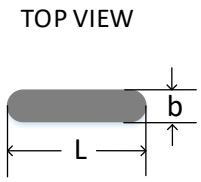




SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	0.10	0.15
A2	1.30	1.40	1.50
A3	0.59	0.64	0.69
b	0.14	—	0.22
b1	0.13	0.16	0.19
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	21.80	22.00	22.20
D1	19.90	20.00	20.10
E	21.80	22.00	22.20
E1	19.90	20.00	20.10
e	0.40BSC		
L	0.45	0.60	0.75
D2	6.00REF		
E2	6.00REF		
L1	1.00REF		
θ	0	—	7°

Figure 4-6 Recommended PCB Layout EQ176





Unit:mm

D	20.00
E	20.00
P	21.40
D2	1.90
E2	1.90
C	0.74
e	0.40
L	1.55
b	0.20


GOWIN
PROGRAMMING FOR THE FUTURE