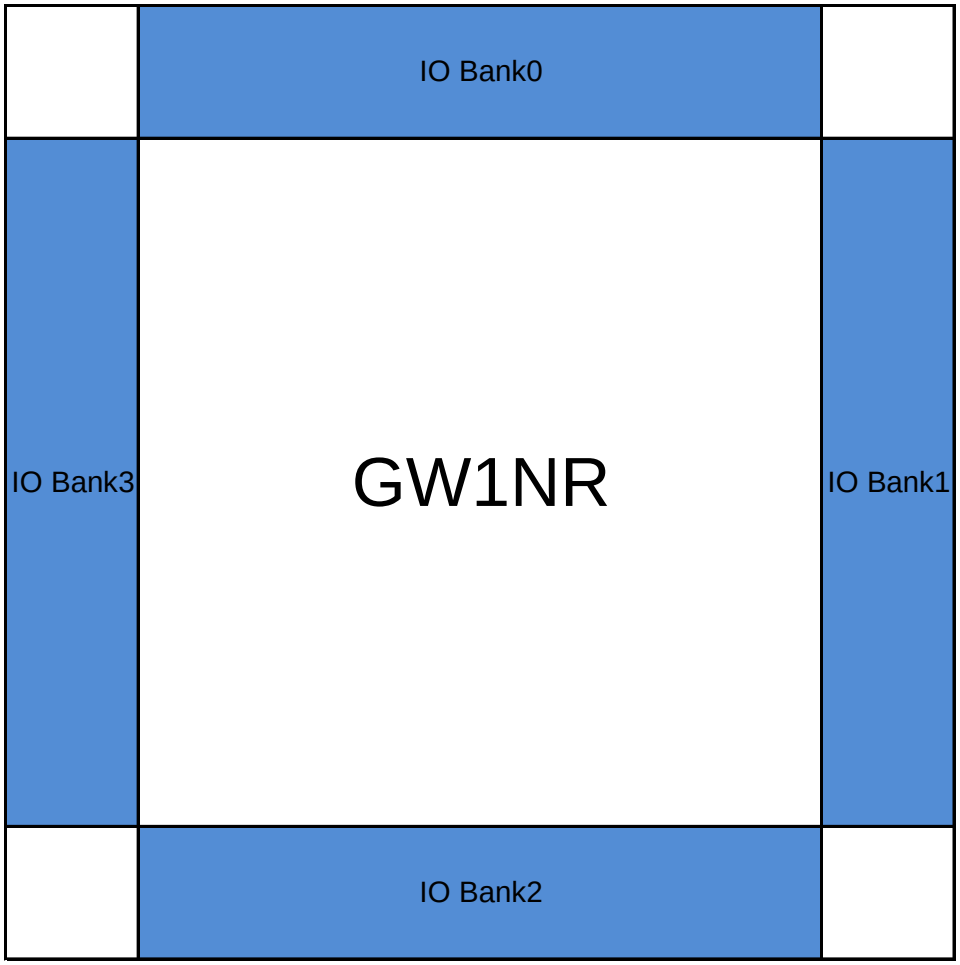
Version History

Data	Version	Description
06/05/2018	1.2E	Initial version published.
2018/9/10	1.3E	X16 of B pins changed to NONE.
2018/12/8	1.4E	The power supply pins connection modified; The new packages of QN88 and LQ144(embedded with PSRAM) added; Power requirements added.
2019/6/4	1.5E	The package of MG100 added.

Pin Definitions

Pins Name	Direction	Description
User I/O Pins		
IO [End][Row/Column Number][A/B]	I/O	[End] indicates the pin location, including L(left), R(right), B(bottom), and T(top)
		[Row/Column Number] indicates the pin Row/Column number. If [End] is T(top) or B(bottom), the pin indicates the column number of the corresponding CFU. If [End] is L(left) or R(right), the pin indicates the row number of the corresponding CFU.
		[A/B] indicaties differential signal pair information.
Multi-Function Pins		
IO [End][Row/Column Number][A/B]/MMM		/MMM represents one or more of the other functions in addition to being general purpose user I/O. When not used for the specical functions, these pins can be user I/O.
RECONFIG_N	I, Internal Weak Pull Up	Start new GowinCONFIG mode when low pulse
READY	I/O	When high, device can be programmed and configured
		When low, device cannot be programmed and configured
DONE	I/O	High indicates successful completion of programming and configuration
		Low indicates incomplete or failed programming and configuration
FASTRD_N/D3	I/O	In MSPI mode, FASTRD_N is used as Flash access speed port. Low indicates high-speed Flash access mode; high indicates regular Flash access mode.
		Data port D3 in CPU mode
MCLK/D4	I/O	Clock output MCLK in MSPI mode
		Data port D4 in CPU mode
MCS_N/D5	I/O	Enable signal MCS_N in MSPI mode, active-low
		Data port D5 in CPU mode
MO/D6	I/O	MOSI in MSPI mode:Master data output/Slave data input
		Data port D6 in CPU mode
MI/D7	I/O	MISO in MSPI mode:Master data input/Slave data output
		Data port D7 in CPU mode
SSPI_CS_N/D0	I/O	Enable signal SSPI_CS_N in SSPI mode,active-low
		Data port D0 in CPU mode
SO/D1	I/O	MISO in SSPI mode:Master data input/Slave data output
		Data port D1 in CPU mode
SI/D2	I/O	MOSI in SSPI mode:Master data output/Slave data input
		Data port D2 in CPU mode
TMS	I,Internal Weak Pull Up	Serial mode input in JTAG mode

Pins Name	Direction	Description
TCK	I	Serial clock input in JTAG mode, the 4.7k pull-down resistance is needed to be connected to PCB.
TDI	I,Internal Weak Pull Up	Serial data input in JTAG mode
TDO	O	Serial data output in JTAG mode
JTAGSEL_N	I, Internal Weak Pull Up	JTAG mode selection, active-low
SCLK	I	Clock input in SSPI, SERIAL, and CPU modes
DIN	I, Internal Weak Pull Up	Data input in SERIAL mode
DOUT	O	Data output in SERIAL mode
CLKHOLD_N	I, Internal Weak Pull Up	High, SCLK will be connected internally in SSPI mode or CPU mode
		Low, SCLK will be disconnected from SSPI mode or CPU mode
WE_N	I	Select data input/output of D[7:0] in CPU mode
GCLKT_[x]	I	Pins for Global clock input, T(True), [x]:global clock number.
GCLKC_[x]	I	Pins for Global clock input, C(Comp), [x]: global clock number.
LPLL_T_fb/RPLL_T_fb	I	L/R PLL feedback the input pins, T(True)
LPLL_C_fb/RPLL_C_fb	I	L/R PLL feedback the input pins, C(Comp)
LPLL_T_in/RPLL_T_in	I	L/R PLL clock input pins,T(True)
LPLL_C_in/RPLL_C_in	I	L/R PLL clock input pins, C(Comp)
MODE2	I, Internal Weak Pull Up	GowinCONFIG modes selection pin
MODE1	I, Internal Weak Pull Up	GowinCONFIG modes selection pin
MODE0	I, Internal Weak Pull Up	GowinCONFIG modes selection pin
Other Pins		
NC	NA	Reserved.
VSS	NA	Ground.
VCC	NA	Power supply pins in the core voltage.
VCCO#	NA	Power supply pins in I/O voltage of I/O BANK#.
VCCX	NA	Power supply pins in auxiliary voltage.



Note！

1.Each Bank has independent reference volatge (VREF);

2.Users can select to use IOB internal VREF(equals to 0.5*VCCO)
or external VREF input (use any IO pins as external VREF input).

Note!
[1]SDRAM embedded.
[2]PSRAM embedded.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	QN88[1]	QN88[2]	MG100[2]	LQ144[2]
IOB10A	I/O	2		True_of_IOB10B	NONE	NONE				
IOB10B	I/O	2		Comp_of_IOB10A	NONE	NONE				
IOB11A	I/O	2		True_of_IOB11B	TRUE	x16	27	27	J3	42
IOB11B	I/O	2		Comp_of_IOB11A	TRUE	NONE	28	28	H3	43
IOB12A	I/O	2		True_of_IOB12B	NONE	NONE				44
IOB12B	I/O	2		Comp_of_IOB12A	NONE	NONE				45
IOB13A	I/O	2		True_of_IOB13B	TRUE	x16	29	29	E4	46
IOB13B	I/O	2		Comp_of_IOB13A	TRUE	NONE	30	30	F4	47
IOB14A	I/O	2		True_of_IOB14B	NONE	NONE				
IOB14B	I/O	2		Comp_of_IOB14A	NONE	NONE				
IOB15A	I/O	2		True_of_IOB15B	TRUE	x16	31	31	K3	48
IOB15B	I/O	2		Comp_of_IOB15A	TRUE	NONE	32	32	K4	49
IOB16A	I/O	2		True_of_IOB16B	NONE	NONE				
IOB16B	I/O	2		Comp_of_IOB16A	NONE	NONE				
IOB17A	I/O	2		True_of_IOB17B	TRUE	x16			J4	50
IOB17B	I/O	2		Comp_of_IOB17A	TRUE	NONE			H4	51
IOB18A	I/O	2		True_of_IOB18B	NONE	NONE				
IOB18B	I/O	2		Comp_of_IOB18A	NONE	NONE				
IOB19A	I/O	2		True_of_IOB19B	NONE	NONE				
IOB19B	I/O	2		Comp_of_IOB19A	NONE	NONE				
IOB20A	I/O	2		True_of_IOB20B	NONE	NONE				
IOB20B	I/O	2		Comp_of_IOB20A	NONE	NONE				
IOB21A	I/O	2		True_of_IOB21B	TRUE	x16			K5	
IOB21B	I/O	2		Comp_of_IOB21A	TRUE	NONE			K6	
IOB22A	I/O	2		True_of_IOB22B	NONE	NONE				
IOB22B	I/O	2		Comp_of_IOB22A	NONE	NONE				
IOB23A	I/O	2		True_of_IOB23B	TRUE	x16	33	33	H5	52
IOB23B	I/O	2		Comp_of_IOB23A	TRUE	NONE	34	34	G5	54
IOB24A	I/O	2		True_of_IOB24B	NONE	NONE				

Note!
[1]SDRAM embedded.
[2]PSRAM embedded.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	QN88[1]	QN88[2]	MG100[2]	LQ144[2]
IOB24B	I/O	2		Comp_of_IOB24A	NONE	NONE				
IOB25A	I/O	2		True_of_IOB25B	TRUE	x16				
IOB25B	I/O	2		Comp_of_IOB25A	TRUE	NONE				
IOB26A	I/O	2		True_of_IOB26B	NONE	NONE				
IOB26B	I/O	2		Comp_of_IOB26A	NONE	NONE				
IOB27A	I/O	2		True_of_IOB27B	TRUE	x16				
IOB27B	I/O	2		Comp_of_IOB27A	TRUE	NONE				
IOB28A/GCLKT_5	I/O	2	GCLKT_5	True_of_IOB28B	NONE	NONE			F5	56
IOB28B/GCLKC_5	I/O	2	GCLKC_5	Comp_of_IOB28A	NONE	NONE			E5	57
IOB29A/GCLKT_4	I/O	2	GCLKT_4	True_of_IOB29B	TRUE	x16	35	35	J6	58
IOB29B/GCLKC_4	I/O	2	GCLKC_4	Comp_of_IOB29A	TRUE	NONE	36	36	H6	59
IOB2A	I/O	2		True_of_IOB2B	TRUE	x16	17	17		
IOB2B	I/O	2		Comp_of_IOB2A	TRUE	NONE	18	18		
IOB30A	I/O	2		True_of_IOB30B	NONE	NONE				60
IOB30B	I/O	2		Comp_of_IOB30A	NONE	NONE				61
IOB31A	I/O	2		True_of_IOB31B	TRUE	x16	37	37	K7	62
IOB31B	I/O	2		Comp_of_IOB31A	TRUE	NONE	38	38	K8	63
IOB32A	I/O	2		True_of_IOB32B	NONE	NONE				
IOB32B	I/O	2		Comp_of_IOB32A	NONE	NONE				
IOB33A	I/O	2		True_of_IOB33B	TRUE	x16	39	39	J7	64
IOB33B	I/O	2		Comp_of_IOB33A	TRUE	NONE	40	40	H7	65
IOB34A	I/O	2		True_of_IOB34B	NONE	NONE				
IOB34B	I/O	2		Comp_of_IOB34A	NONE	NONE				
IOB35A	I/O	2		True_of_IOB35B	TRUE	x16			F6	66
IOB35B	I/O	2		Comp_of_IOB35A	TRUE	NONE			G6	67
IOB36A	I/O	2		True_of_IOB36B	NONE	NONE				
IOB36B	I/O	2		Comp_of_IOB36A	NONE	NONE				
IOB37A	I/O	2		True_of_IOB37B	NONE	NONE				68
IOB37B	I/O	2		Comp_of_IOB37A	NONE	NONE				69

Note!
[1]SDRAM embedded.
[2]PSRAM embedded.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	QN88[1]	QN88[2]	MG100[2]	LQ144[2]
IOB38A	I/O	2		True_of_IOB38B	NONE	NONE				
IOB38B	I/O	2		Comp_of_IOB38A	NONE	NONE				
IOB39A	I/O	2		True_of_IOB39B	TRUE	x16			F7	70
IOB39B	I/O	2		Comp_of_IOB39A	TRUE	NONE			G7	71
IOB3A	I/O	2		True_of_IOB3B	NONE	NONE				
IOB3B	I/O	2		Comp_of_IOB3A	NONE	NONE			H1	
IOB40A	I/O	2		True_of_IOB40B	NONE	NONE				
IOB40B	I/O	2		Comp_of_IOB40A	NONE	NONE				
IOB41A	I/O	2		True_of_IOB41B	TRUE	x16	41	41	K10	72
IOB41B	I/O	2		Comp_of_IOB41A	TRUE	NONE	42	42	K9	
IOB42A	I/O	2		True_of_IOB42B	NONE	NONE				
IOB42B	I/O	2		Comp_of_IOB42A	NONE	NONE				75
IOB43A	I/O	2		True_of_IOB43B	TRUE	x16			J10	78
IOB43B	I/O	2		Comp_of_IOB43A	TRUE	NONE	47	47		76
IOB44A	I/O	2		True_of_IOB44B	NONE	NONE				
IOB44B	I/O	2		Comp_of_IOB44A	NONE	NONE				
IOB45A	I/O	2		True_of_IOB45B	TRUE	x16				
IOB45B	I/O	2		Comp_of_IOB45A	TRUE	NONE				
IOB46A	I/O	2		True_of_IOB46B	NONE	NONE				
IOB46B	I/O	2		Comp_of_IOB46A	NONE	NONE				
IOB4A	I/O	2		True_of_IOB4B	TRUE	x16	19	19	K1	29
IOB4B	I/O	2		Comp_of_IOB4A	TRUE	NONE	20	20	K2	30
IOB5A	I/O	2		True_of_IOB5B	NONE	NONE				
IOB5B	I/O	2		Comp_of_IOB5A	NONE	NONE				
IOB6A	I/O	2		True_of_IOB6B	TRUE	x16				32
IOB6B	I/O	2		Comp_of_IOB6A	TRUE	NONE				34
IOB7A	I/O	2		True_of_IOB7B	NONE	NONE				
IOB7B	I/O	2		Comp_of_IOB7A	NONE	NONE				
IOB8A	I/O	2		True_of_IOB8B	TRUE	x16	25	25	G4	38

Note!
[1]SDRAM embedded.
[2]PSRAM embedded.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	QN88[1]	QN88[2]	MG100[2]	LQ144[2]
IOB8B	I/O	2		Comp_of_IOB8A	TRUE	NONE	26	26	G3	39
IOB9A	I/O	2		True_of_IOB9B	NONE	NONE				40
IOB9B	I/O	2		Comp_of_IOB9A	NONE	NONE				41
IOL11A/TMS	I/O	3	TMS	True_of_IOL11B	TRUE	NONE	5	5	E2	13
IOL11B/TCK	I/O	3	TCK	Comp_of_IOL11A	TRUE	NONE	6	6	E3	14
IOL12A/SCLK	I/O	3	SCLK	True_of_IOL12B	NONE	NONE				15
IOL12B/TDI	I/O	3	TDI	Comp_of_IOL12A	NONE	NONE	7	7	F3	16
IOL13A/TDO	I/O	3	TDO	True_of_IOL13B	TRUE	NONE	8	8	F2	18
IOL13B/RECONFIG_N	I/O	3	RECONFIG_N	Comp_of_IOL13A	TRUE	NONE	9	9	D3	20
IOL14A/DONE	I/O	3	DONE	True_of_IOL14B	NONE	NONE	10			21
IOL14B/READY	I/O	3	READY	Comp_of_IOL14A	NONE	NONE			D1	22
IOL15A/GCLKT_6	I/O	3	GCLKT_6	True_of_IOL15B	TRUE	NONE	11	10		
IOL15B/GCLKC_6	I/O	3	GCLKC_6	Comp_of_IOL15A	TRUE	NONE			F1	23
IOL16A	I/O	3		True_of_IOL16B	NONE	NONE				
IOL16B	I/O	3		Comp_of_IOL16A	NONE	NONE		11	D2	24
IOL17A	I/O	3		True_of_IOL17B	TRUE	NONE				
IOL17B	I/O	3		Comp_of_IOL17A	TRUE	NONE				
IOL18A	I/O	3		True_of_IOL18B	NONE	NONE				
IOL18B	I/O	3		Comp_of_IOL18A	NONE	NONE				
IOL20A	I/O	3		True_of_IOL20B	TRUE	NONE				
IOL20B	I/O	3		Comp_of_IOL20A	TRUE	NONE				
IOL21A	I/O	3		True_of_IOL21B	NONE	NONE				
IOL21B	I/O	3		Comp_of_IOL21A	NONE	NONE		13	G2	25
IOL22A	I/O	3		True_of_IOL22B	TRUE	NONE	13			
IOL22B	I/O	3		Comp_of_IOL22A	TRUE	NONE	14	14	G1	26
IOL23A	I/O	3		True_of_IOL23B	NONE	NONE				
IOL23B	I/O	3		Comp_of_IOL23A	NONE	NONE				
IOL24A	I/O	3		True_of_IOL24B	TRUE	NONE				
IOL24B	I/O	3		Comp_of_IOL24A	TRUE	NONE				27

Note!
[1]SDRAM embedded.
[2]PSRAM embedded.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	QN88[1]	QN88[2]	MG100[2]	LQ144[2]
IOL25A	I/O	3		True_of_IOL25B	NONE	NONE				
IOL25B	I/O	3		Comp_of_IOL25A	NONE	NONE		15	H2	28
IOL26A	I/O	3		True_of_IOL26B	TRUE	NONE	15			
IOL26B	I/O	3		Comp_of_IOL26A	TRUE	NONE	16	16		
IOL27A	I/O	3		True_of_IOL27B	NONE	NONE				
IOL27B	I/O	3		Comp_of_IOL27A	NONE	NONE				
IOL2A	I/O	3		True_of_IOL2B	TRUE	NONE	3			
IOL2B	I/O	3		Comp_of_IOL2A	TRUE	NONE				
IOL3A	I/O	3		True_of_IOL3B	NONE	NONE				
IOL3B	I/O	3		Comp_of_IOL3A	NONE	NONE				5
IOL4A	I/O	3		True_of_IOL4B	TRUE	NONE				
IOL4B	I/O	3		Comp_of_IOL4A	TRUE	NONE			B2	6
IOL5A/JTAGSEL_N/LPLL_T_in	I/O	3	JTAGSEL_N/LPLL_T_in	True_of_IOL5B	NONE	NONE	4	4	B1	7
IOL5B/LPLL_C_in	I/O	3	LPLL_C_in	Comp_of_IOL5A	NONE	NONE			B3	8
IOL6A/LPLL_T_fb	I/O	3	LPLL_T_fb	True_of_IOL6B	TRUE	NONE				
IOL6B/LPLL_C_fb	I/O	3	LPLL_C_fb	Comp_of_IOL6A	TRUE	NONE				
IOL7A	I/O	3		True_of_IOL7B	NONE	NONE				
IOL7B	I/O	3		Comp_of_IOL7A	NONE	NONE			C1	10
IOL8A	I/O	3		True_of_IOL8B	TRUE	NONE				
IOL8B	I/O	3		Comp_of_IOL8A	TRUE	NONE			C2	11
IOL9A/GCLKT_7	I/O	3	GCLKT_7	True_of_IOL9B	NONE	NONE				
IOL9B/GCLKC_7	I/O	3	GCLKC_7	Comp_of_IOL9A	NONE	NONE			C3	12
IOR11A/MI/D7	I/O	1	MI/D7	True_of_IOR11B	TRUE	NONE	62	62		96
IOR11B/MO/D6	I/O	1	MO/D6	Comp_of_IOR11A	TRUE	NONE	61	61	F9	95
IOR12A/MCS_N/D5	I/O	1	MCS_N/D5	True_of_IOR12B	NONE	NONE	60	60		94
IOR12B/MCLK/D4	I/O	1	MCLK/D4	Comp_of_IOR12A	NONE	NONE	59	59	E10	93
IOR13A/FASTRD_N/D3	I/O	1	FASTRD_N/D3	True_of_IOR13B	TRUE	NONE	57	57		92
IOR13B/SI/D2	I/O	1	SI/D2	Comp_of_IOR13A	TRUE	NONE				90

Note!
[1]SDRAM embedded.
[2]PSRAM embedded.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	QN88[1]	QN88[2]	MG100[2]	LQ144[2]
IOR14A/SO/D1	I/O	1	SO/D1	True_of_IOR14B	NONE	NONE	56	56		88
IOR14B/SSPI_CS_N/D0	I/O	1	SSPI_CS_N/D0	Comp_of_IOR14A	NONE	NONE	55	55	G9	87
IOR15A/DIN/CLKHOLD_N	I/O	1	DIN/CLKHOLD_N	True_of_IOR15B	TRUE	NONE	54	54		86
IOR15B/DOUT/WE_N	I/O	1	DOUT/WE_N	Comp_of_IOR15A	TRUE	NONE	53	53		85
IOR16A	I/O	1		True_of_IOR16B	NONE	NONE				
IOR16B	I/O	1		Comp_of_IOR16A	NONE	NONE			F10	84
IOR17A/GCLKT_3	I/O	1	GCLKT_3	True_of_IOR17B	TRUE	NONE	52	52	F8	
IOR17B/GCLKC_3	I/O	1	GCLKC_3	Comp_of_IOR17A	TRUE	NONE	51	51	G8	83
IOR18A	I/O	1		True_of_IOR18B	NONE	NONE				
IOR18B	I/O	1		Comp_of_IOR18A	NONE	NONE			H8	
IOR20A	I/O	1		True_of_IOR20B	TRUE	NONE				
IOR20B	I/O	1		Comp_of_IOR20A	TRUE	NONE				
IOR21A	I/O	1		True_of_IOR21B	NONE	NONE				
IOR21B	I/O	1		Comp_of_IOR21A	NONE	NONE			G10	82
IOR22A	I/O	1		True_of_IOR22B	TRUE	NONE				
IOR22B	I/O	1		Comp_of_IOR22A	TRUE	NONE	50	50		81
IOR23A	I/O	1		True_of_IOR23B	NONE	NONE				
IOR23B	I/O	1		Comp_of_IOR23A	NONE	NONE				80
IOR24A	I/O	1		True_of_IOR24B	TRUE	NONE	49	49		
IOR24B	I/O	1		Comp_of_IOR24A	TRUE	NONE	48	48	H9	79
IOR25A	I/O	1		True_of_IOR25B	NONE	NONE				
IOR25B	I/O	1		Comp_of_IOR25A	NONE	NONE			H10	
IOR26A	I/O	1		True_of_IOR26B	TRUE	NONE				
IOR26B	I/O	1		Comp_of_IOR26A	TRUE	NONE				
IOR27A	I/O	1		True_of_IOR27B	NONE	NONE				
IOR27B	I/O	1		Comp_of_IOR27A	NONE	NONE				
IOR2A	I/O	1		True_of_IOR2B	TRUE	NONE				
IOR2B	I/O	1		Comp_of_IOR2A	TRUE	NONE			C10	
IOR3A	I/O	1		True_of_IOR3B	NONE	NONE				

Note!
[1]SDRAM embedded.
[2]PSRAM embedded.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	QN88[1]	QN88[2]	MG100[2]	LQ144[2]
IOR3B	I/O	1		Comp_of_IOR3A	NONE	NONE			B10	
IOR4A	I/O	1		True_of_IOR4B	TRUE	NONE				
IOR4B	I/O	1		Comp_of_IOR4A	TRUE	NONE				
IOR5A/RPLL_T_in	I/O	1	RPLL_T_in	True_of_IOR5B	NONE	NONE	63	63	C9	106
IOR5B/RPLL_C_in	I/O	1	RPLL_C_in	Comp_of_IOR5A	NONE	NONE			D9	104
IOR6A/RPLL_T_fb	I/O	1	RPLL_T_fb	True_of_IOR6B	TRUE	NONE				102
IOR6B/RPLL_C_fb	I/O	1	RPLL_C_fb	Comp_of_IOR6A	TRUE	NONE				101
IOR7A	I/O	1		True_of_IOR7B	NONE	NONE				
IOR7B	I/O	1		Comp_of_IOR7A	NONE	NONE			D10	100
IOR8A	I/O	1		True_of_IOR8B	TRUE	NONE				
IOR8B	I/O	1		Comp_of_IOR8A	TRUE	NONE				99
IOR9A/GCLKT_2	I/O	1	GCLKT_2	True_of_IOR9B	NONE	NONE			E8	98
IOR9B/GCLKC_2	I/O	1	GCLKC_2	Comp_of_IOR9A	NONE	NONE				97
IOT10A	I/O	3		True_of_IOT10B	NONE	NONE	84	84		140
IOT10B	I/O	3		Comp_of_IOT10A	NONE	NONE	83	83		139
IOT11A	I/O	3		True_of_IOT11B	NONE	x16	82	82	C4	
IOT11B	I/O	3		Comp_of_IOT11A	NONE	NONE	81	81	B4	
IOT12A	I/O	3		True_of_IOT12B	NONE	NONE	80	80		138
IOT12B	I/O	3		Comp_of_IOT12A	NONE	NONE	79	79		137
IOT13A	I/O	0		True_of_IOT13B	NONE	x16			D5	
IOT13B	I/O	0		Comp_of_IOT13A	NONE	NONE			D6	
IOT14A	I/O	0		True_of_IOT14B	NONE	NONE				
IOT14B	I/O	0		Comp_of_IOT14A	NONE	NONE				
IOT15A	I/O	0		True_of_IOT15B	NONE	x16				136
IOT15B	I/O	0		Comp_of_IOT15A	NONE	NONE				135
IOT16A	I/O	0		True_of_IOT16B	NONE	NONE				
IOT16B	I/O	0		Comp_of_IOT16A	NONE	NONE				
IOT17A	I/O	0		True_of_IOT17B	NONE	x16			C5	134
IOT17B	I/O	0		Comp_of_IOT17A	NONE	NONE			B5	133

Note!
[1]SDRAM embedded.
[2]PSRAM embedded.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	QN88[1]	QN88[2]	MG100[2]	LQ144[2]
IOT18A	I/O	0		True_of_IOT18B	NONE	NONE				
IOT18B	I/O	0		Comp_of_IOT18A	NONE	NONE				
IOT19A	I/O	0		True_of_IOT19B	NONE	NONE				
IOT19B	I/O	0		Comp_of_IOT19A	NONE	NONE				
IOT20A	I/O	0		True_of_IOT20B	NONE	NONE				132
IOT20B	I/O	0		Comp_of_IOT20A	NONE	NONE				131
IOT21A	I/O	0		True_of_IOT21B	NONE	x16			C6	
IOT21B	I/O	0		Comp_of_IOT21A	NONE	NONE			B6	
IOT22A	I/O	0		True_of_IOT22B	NONE	NONE				130
IOT22B	I/O	0		Comp_of_IOT22A	NONE	NONE				129
IOT23A	I/O	0		True_of_IOT23B	NONE	x16				
IOT23B	I/O	0		Comp_of_IOT23A	NONE	NONE				
IOT24A	I/O	0		True_of_IOT24B	NONE	NONE				128
IOT24B	I/O	0		Comp_of_IOT24A	NONE	NONE				126
IOT25A	I/O	0		True_of_IOT25B	NONE	x16				
IOT25B	I/O	0		Comp_of_IOT25A	NONE	NONE				
IOT26A	I/O	0		True_of_IOT26B	NONE	NONE				
IOT26B	I/O	0		Comp_of_IOT26A	NONE	NONE				
IOT27A	I/O	0		True_of_IOT27B	NONE	x16			A6	125
IOT27B	I/O	0		Comp_of_IOT27A	NONE	NONE			A7	124
IOT28A/GCLKT_0	I/O	0	GCLKT_0	True_of_IOT28B	NONE	NONE				
IOT28B/GCLKC_0	I/O	0	GCLKC_0	Comp_of_IOT28A	NONE	NONE				
IOT29A/GCLKT_1	I/O	0	GCLKT_1	True_of_IOT29B	NONE	x16			E6	123
IOT29B/GCLKC_1	I/O	0	GCLKC_1	Comp_of_IOT29A	NONE	NONE			E7	122
IOT2A	I/O	3		True_of_IOT2B	NONE	x16		3		3
IOT2B	I/O	3		Comp_of_IOT2A	NONE	NONE				4
IOT30A	I/O	0		True_of_IOT30B	NONE	NONE				
IOT30B	I/O	0		Comp_of_IOT30A	NONE	NONE				
IOT31A	I/O	0		True_of_IOT31B	NONE	x16				

Note!
[1]SDRAM embedded.
[2]PSRAM embedded.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	QN88[1]	QN88[2]	MG100[2]	LQ144[2]
IOT31B	I/O	0		Comp_of_IOT31A	NONE	NONE				
IOT32A	I/O	0		True_of_IOT32B	NONE	NONE				121
IOT32B	I/O	0		Comp_of_IOT32A	NONE	NONE				120
IOT33A	I/O	0		True_of_IOT33B	NONE	x16			C7	
IOT33B	I/O	0		Comp_of_IOT33A	NONE	NONE			B7	
IOT34A	I/O	0		True_of_IOT34B	NONE	NONE				119
IOT34B	I/O	0		Comp_of_IOT34A	NONE	NONE				118
IOT35A	I/O	0		True_of_IOT35B	NONE	x16				
IOT35B	I/O	0		Comp_of_IOT35A	NONE	NONE				
IOT36A	I/O	1		True_of_IOT36B	NONE	NONE				
IOT36B	I/O	1		Comp_of_IOT36A	NONE	NONE				
IOT37A	I/O	1		True_of_IOT37B	NONE	NONE	77	77		117
IOT37B	I/O	1		Comp_of_IOT37A	NONE	NONE	76	76		116
IOT38A	I/O	1		True_of_IOT38B	NONE	NONE	75	75		
IOT38B	I/O	1		Comp_of_IOT38A	NONE	NONE	74	74		
IOT39A	I/O	1		True_of_IOT39B	NONE	x16	73	73	B8	115
IOT39B	I/O	1		Comp_of_IOT39A	NONE	NONE	72	72	C8	114
IOT3A	I/O	3		True_of_IOT3B	NONE	NONE				
IOT3B	I/O	3		Comp_of_IOT3A	NONE	NONE				
IOT40A	I/O	1		True_of_IOT40B	NONE	NONE				
IOT40B	I/O	1		Comp_of_IOT40A	NONE	NONE				
IOT41A	I/O	1		True_of_IOT41B	NONE	x16	71	71	D7	113
IOT41B	I/O	1		Comp_of_IOT41A	NONE	NONE	70	70	D8	112
IOT42A	I/O	1		True_of_IOT42B	NONE	NONE	69	69		111
IOT42B	I/O	1		Comp_of_IOT42A	NONE	NONE	68	68		110
IOT43A	I/O	1		True_of_IOT43B	NONE	x16				
IOT43B	I/O	1		Comp_of_IOT43A	NONE	NONE				
IOT44A	I/O	1		True_of_IOT44B	NONE	NONE				
IOT44B	I/O	1		Comp_of_IOT44A	NONE	NONE				

Note!
[1]SDRAM embedded.
[2]PSRAM embedded.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	QN88[1]	QN88[2]	MG100[2]	LQ144[2]
IOT45A	I/O	1		True_of_IOT45B	NONE	x16			B9	
IOT45B	I/O	1		Comp_of_IOT45A	NONE	NONE			A10	
IOT46A	I/O	1		True_of_IOT46B	NONE	NONE				
IOT46B	I/O	1		Comp_of_IOT46A	NONE	NONE				
IOT4A	I/O	3		True_of_IOT4B	NONE	x16				
IOT4B	I/O	3		Comp_of_IOT4A	NONE	NONE				
IOT5A/MODE0	I/O	3	MODE0	True_of_IOT5B	NONE	NONE	88	88		144
IOT5B/MODE2	I/O	3	MODE2	Comp_of_IOT5A	NONE	NONE				
IOT6A	I/O	3		True_of_IOT6B	NONE	x16				
IOT6B/MODE1	I/O	3	MODE1	Comp_of_IOT6A	NONE	NONE	87	87	D4	143
IOT7A	I/O	3		True_of_IOT7B	NONE	NONE				
IOT7B	I/O	3		Comp_of_IOT7A	NONE	NONE				
IOT8A	I/O	3		True_of_IOT8B	NONE	x16	86	86	A3	142
IOT8B	I/O	3		Comp_of_IOT8A	NONE	NONE	85	85	A4	141
IOT9A	I/O	3		True_of_IOT9B	NONE	NONE				
IOT9B	I/O	3		Comp_of_IOT9A	NONE	NONE				
VCC	Power	N/A				NONE	1	1	A2	1
VCC	Power	N/A				NONE	22	22	J2	36
VCC	Power	N/A				NONE	45	45		73
VCC	Power	N/A				NONE	66	66	A8	108
VCCO0	Power	N/A				NONE			A5	109
VCCO0	Power	N/A				NONE				127
VCCO1	Power	N/A				NONE	58	58		91
VCCO1	Power	N/A				NONE			E9	
VCCO1	Power	N/A				NONE				103
VCCO2	Power	N/A				NONE		23	J5	37
VCCO2	Power	N/A				NONE		44		
VCCO2	Power	N/A				NONE				55
VCCO3	Power	N/A				NONE	12	12		

Note!
[1]SDRAM embedded.
[2]PSRAM embedded.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	QN88[1]	QN88[2]	MG100[2]	LQ144[2]
VCCO3	Power	N/A				NONE			E1	19
VCCO3	Power	N/A				NONE				9
VCCX	Power	N/A				NONE			J8	
VCCX	Power	N/A				NONE				31
VCCX	Power	N/A				NONE				77
VCCX/VCCO0	Power	N/A				NONE		64		
VCCX/VCCO0	Power	N/A				NONE		67		
VCCX/VCCO0	Power	N/A				NONE		78		
VCCX/VCCO0/VCCO2	Power	N/A				NONE	23			
VCCX/VCCO0/VCCO2	Power	N/A				NONE	44			
VCCX/VCCO0/VCCO2	Power	N/A				NONE	64			
VCCX/VCCO0/VCCO2	Power	N/A				NONE	67			
VCCX/VCCO0/VCCO2	Power	N/A				NONE	78			
VSS	Ground	N/A				NONE	2	2		
VSS	Ground	N/A				NONE	21	21		33
VSS	Ground	N/A				NONE	24	24		
VSS	Ground	N/A				NONE	43	43		
VSS	Ground	N/A				NONE	46	46		74
VSS	Ground	N/A				NONE	65	65		
VSS	Ground	N/A				NONE			A1	2
VSS	Ground	N/A				NONE			A9	17
VSS	Ground	N/A				NONE			J1	107
VSS	Ground	N/A				NONE			J9	
VSS	Ground	N/A				NONE				35
VSS	Ground	N/A				NONE				53
VSS	Ground	N/A				NONE				89
VSS	Ground	N/A				NONE				105

Note!
[1]SDRAM embedded.
[2]PSRAM embedded.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	QN88[1]	QN88[2]	MG100[2]	LQ144[2]
BANK3 True LVDS Pair										
IOL11A/TMS	I/O	3	TMS	True_of_IOL11B	TRUE	NONE	5	5	E2	13
IOL11B/TCK	I/O	3	TCK	Comp_of_IOL11A	TRUE	NONE	6	6	E3	14
IOL13A/TDO	I/O	3	TDO	True_of_IOL13B	TRUE	NONE	8	8	F2	18
IOL13B/RECONFIG_N	I/O	3	RECONFIG_N	Comp_of_IOL13A	TRUE	NONE	9	9	D3	20
IOL15A/GCLKT_6	I/O	3	GCLKT_6	True_of_IOL15B	TRUE	NONE				
IOL15B/GCLKC_6	I/O	3	GCLKC_6	Comp_of_IOL15A	TRUE	NONE				
IOL17A	I/O	3		True_of_IOL17B	TRUE	NONE				
IOL17B	I/O	3		Comp_of_IOL17A	TRUE	NONE				
IOL20A	I/O	3		True_of_IOL20B	TRUE	NONE				
IOL20B	I/O	3		Comp_of_IOL20A	TRUE	NONE				
IOL22A	I/O	3		True_of_IOL22B	TRUE	NONE	13			
IOL22B	I/O	3		Comp_of_IOL22A	TRUE	NONE	14			
IOL24A	I/O	3		True_of_IOL24B	TRUE	NONE				
IOL24B	I/O	3		Comp_of_IOL24A	TRUE	NONE				
IOL26A	I/O	3		True_of_IOL26B	TRUE	NONE	15			
IOL26B	I/O	3		Comp_of_IOL26A	TRUE	NONE	16			
IOL2A	I/O	3		True_of_IOL2B	TRUE	NONE				
IOL2B	I/O	3		Comp_of_IOL2A	TRUE	NONE				
IOL4A	I/O	3		True_of_IOL4B	TRUE	NONE				
IOL4B	I/O	3		Comp_of_IOL4A	TRUE	NONE				
IOL6A/LPLL_T_fb	I/O	3	LPLL_T_fb	True_of_IOL6B	TRUE	NONE				
IOL6B/LPLL_C_fb	I/O	3	LPLL_C_fb	Comp_of_IOL6A	TRUE	NONE				
IOL8A	I/O	3		True_of_IOL8B	TRUE	NONE				
IOL8B	I/O	3		Comp_of_IOL8A	TRUE	NONE				
BANK2 True LVDS Pair										
IOB11A	I/O	2		True_of_IOB11B	TRUE	x16	27	27	J3	42
IOB11B	I/O	2		Comp_of_IOB11A	TRUE	NONE	28	28	H3	43
IOB13A	I/O	2		True_of_IOB13B	TRUE	x16	29	29	E4	46

Note!
[1]SDRAM embedded.
[2]PSRAM embedded.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	QN88[1]	QN88[2]	MG100[2]	LQ144[2]
IOB13B	I/O	2		Comp_of_IOB13A	TRUE	NONE	30	30	F4	47
IOB15A	I/O	2		True_of_IOB15B	TRUE	x16	31	31	K3	48
IOB15B	I/O	2		Comp_of_IOB15A	TRUE	NONE	32	32	K4	49
IOB17A	I/O	2		True_of_IOB17B	TRUE	x16			J4	50
IOB17B	I/O	2		Comp_of_IOB17A	TRUE	NONE			H4	51
IOB21A	I/O	2		True_of_IOB21B	TRUE	x16			K5	
IOB21B	I/O	2		Comp_of_IOB21A	TRUE	NONE			K6	
IOB23A	I/O	2		True_of_IOB23B	TRUE	x16	33	33	H5	52
IOB23B	I/O	2		Comp_of_IOB23A	TRUE	NONE	34	34	G5	54
IOB25A	I/O	2		True_of_IOB25B	TRUE	x16				
IOB25B	I/O	2		Comp_of_IOB25A	TRUE	NONE				
IOB27A	I/O	2		True_of_IOB27B	TRUE	x16				
IOB27B	I/O	2		Comp_of_IOB27A	TRUE	NONE				
IOB29A/GCLKT_4	I/O	2	GCLKT_4	True_of_IOB29B	TRUE	x16	35	35	J6	58
IOB29B/GCLKC_4	I/O	2	GCLKC_4	Comp_of_IOB29A	TRUE	NONE	36	36	H6	59
IOB2A	I/O	2		True_of_IOB2B	TRUE	x16	17	17		
IOB2B	I/O	2		Comp_of_IOB2A	TRUE	NONE	18	18		
IOB31A	I/O	2		True_of_IOB31B	TRUE	x16	37	37	K7	62
IOB31B	I/O	2		Comp_of_IOB31A	TRUE	NONE	38	38	K8	63
IOB33A	I/O	2		True_of_IOB33B	TRUE	x16	39	39	J7	64
IOB33B	I/O	2		Comp_of_IOB33A	TRUE	NONE	40	40	H7	65
IOB35A	I/O	2		True_of_IOB35B	TRUE	x16			F6	66
IOB35B	I/O	2		Comp_of_IOB35A	TRUE	NONE			G6	67
IOB39A	I/O	2		True_of_IOB39B	TRUE	x16			F7	70
IOB39B	I/O	2		Comp_of_IOB39A	TRUE	NONE			G7	71
IOB41A	I/O	2		True_of_IOB41B	TRUE	x16	41	41	K10	
IOB41B	I/O	2		Comp_of_IOB41A	TRUE	NONE	42	42	K9	
IOB43A	I/O	2		True_of_IOB43B	TRUE	x16				78
IOB43B	I/O	2		Comp_of_IOB43A	TRUE	NONE				76

Note!
[1]SDRAM embedded.
[2]PSRAM embedded.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	QN88[1]	QN88[2]	MG100[2]	LQ144[2]
IOB45A	I/O	2		True_of_IOB45B	TRUE	x16				
IOB45B	I/O	2		Comp_of_IOB45A	TRUE	NONE				
IOB4A	I/O	2		True_of_IOB4B	TRUE	x16	19	19	K1	29
IOB4B	I/O	2		Comp_of_IOB4A	TRUE	NONE	20	20	K2	30
IOB6A	I/O	2		True_of_IOB6B	TRUE	x16				32
IOB6B	I/O	2		Comp_of_IOB6A	TRUE	NONE				34
IOB8A	I/O	2		True_of_IOB8B	TRUE	x16	25	25	G4	38
IOB8B	I/O	2		Comp_of_IOB8A	TRUE	NONE	26	26	G3	39
BANK1 True LVDS Pair										
IOR11A/MI/D7	I/O	1	MI/D7	True_of_IOR11B	TRUE	NONE	62	62		96
IOR11B/MO/D6	I/O	1	MO/D6	Comp_of_IOR11A	TRUE	NONE	61	61		95
IOR13A/FASTRD_N/D3	I/O	1	FASTRD_N/D3	True_of_IOR13B	TRUE	NONE				92
IOR13B/SI/D2	I/O	1	SI/D2	Comp_of_IOR13A	TRUE	NONE				90
IOR15A/DIN/CLKHOLD_N	I/O	1	DIN/CLKHOLD_N	True_of_IOR15B	TRUE	NONE	54	54		86
IOR15B/DOUT/WE_N	I/O	1	DOUT/WE_N	Comp_of_IOR15A	TRUE	NONE	53	53		85
IOR17A/GCLKT_3	I/O	1	GCLKT_3	True_of_IOR17B	TRUE	NONE	52	52	F8	
IOR17B/GCLKC_3	I/O	1	GCLKC_3	Comp_of_IOR17A	TRUE	NONE	51	51	G8	
IOR20A	I/O	1		True_of_IOR20B	TRUE	NONE				
IOR20B	I/O	1		Comp_of_IOR20A	TRUE	NONE				
IOR22A	I/O	1		True_of_IOR22B	TRUE	NONE				
IOR22B	I/O	1		Comp_of_IOR22A	TRUE	NONE				
IOR24A	I/O	1		True_of_IOR24B	TRUE	NONE	49	49		
IOR24B	I/O	1		Comp_of_IOR24A	TRUE	NONE	48	48		
IOR26A	I/O	1		True_of_IOR26B	TRUE	NONE				
IOR26B	I/O	1		Comp_of_IOR26A	TRUE	NONE				
IOR2A	I/O	1		True_of_IOR2B	TRUE	NONE				
IOR2B	I/O	1		Comp_of_IOR2A	TRUE	NONE				
IOR4A	I/O	1		True_of_IOR4B	TRUE	NONE				
IOR4B	I/O	1		Comp_of_IOR4A	TRUE	NONE				

Note!
[1]SDRAM embedded.
[2]PSRAM embedded.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	QN88[1]	QN88[2]	MG100[2]	LQ144[2]
IOR6A/RPLL_T_fb	I/O	1	RPLL_T_fb	True_of_IOR6B	TRUE	NONE				102
IOR6B/RPLL_C_fb	I/O	1	RPLL_C_fb	Comp_of_IOR6A	TRUE	NONE				101
IOR8A	I/O	1		True_of_IOR8B	TRUE	NONE				
IOR8B	I/O	1		Comp_of_IOR8A	TRUE	NONE				

Recommended Operating Conditions for GW1NR-9 QN88, embedded with SDR SDRAM			
Name	Description	Min.	Max.
VCC	LV: Core Power	1.14V	1.26V
	UV:Core Power	3.135V	3.465V
VCCO0, VCCO1 VCCO2, VCCO3	I/O bank power, connected to SDR SDRAM interface	3.135V	3.465V
VCCX/VCCO0/VCCO2	VCCX and VCCO2 provide power for SDRAM; VCCX, VCCO0, and VCCO2 are internal connected.	3.135V	3.465V
Recommended Operating Conditions for GW1NR-9 MG100			
Name	Description	Min.	Max.
VCC	LV: Core Power	1.14V	1.26V
	UV:Core Power	1.71V	3.465V
VCCO1, VCCO2	I/O Bank Power for LV	1.14V	3.465V
	I/O Bank Power for UV	1.71V	3.465V
VCCO1, VCCO3	I/O Bank power, connected to PSRAM and providing power for PSRAM	1.71V	1.89V
VCCX	Auxiliary volatage	2.375V	3.465V
Recommended Operating Conditions for GW1NR-9 QN88, embedded with PSRAM			
Name	Description	Min.	Max.
VCC	LV: Core Power	1.14V	1.26V
	UV:Core Power	1.71V	3.465V
VCCO1, VCCO2	I/O Bank Power for LV	1.14V	3.465V
	I/O Bank Power for UV	1.71V	3.465V
VCCO3	I/O Bank power, connected to PSRAM and providing power for PSRAM	1.71V	1.89V
VCCX/VCCO0	Auxiliary volatage,VCCX and VCCO0 are internal connected.	2.375V	3.465V
Recommended Operating Conditions for GW1NR-9 LQ144, embedded with PSRAM			
Name	Description	Min.	Max.
VCC	LV: Core Power	1.14V	1.26V
	UV:Core Power	1.71V	3.465V
VCCO0, VCCO1 VCCO2	I/O Bank Power for LV	1.14V	3.465V
	I/O Bank Power for UV	1.71V	3.465V
VCCO3	I/O Bank power, connected to PSRAM; VCCO3 provides power for PSRAM	1.71V	1.89V
VCCX	Auxiliary volatage	2.375V	3.465V