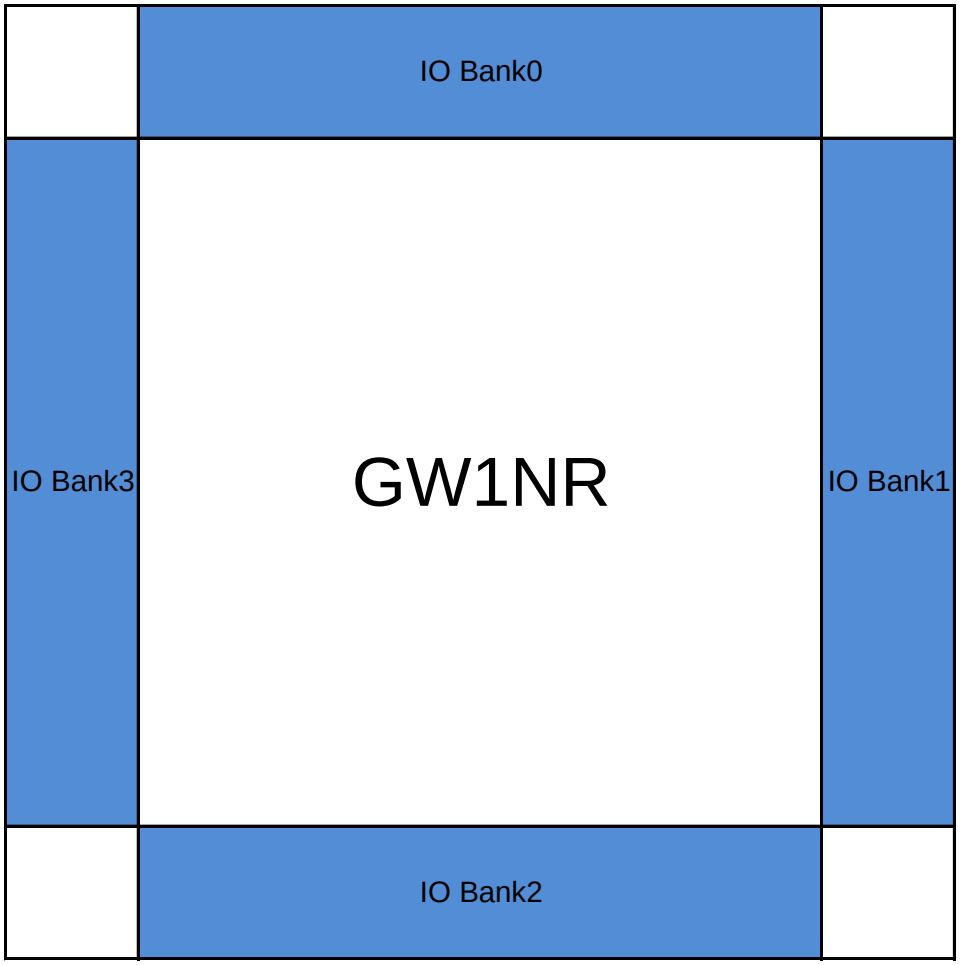
Version History

Date	Version	Description
06/30/2020	1.0E	Initial version published. FN32G package supported.
10/29/2021	1.1E	The info. Of EQ144G and QN48G packages embedded with Flash added. Pin Definitions updated.
01/20/2022	1.2E	The info. of QN32X, QN48X, and LQ100G packages added. The info. of QN48G package removed.
10/20/2022	1.2.1E	The note in Pin Definitions sheet updated.
05/04/2023	1.2.2E	The notes of FN32G/EQ144G/QN32X/QN48X in Power sheet added. The description of CLKHOLD_N pin in Pin Definitions sheet updated.
06/30/2023	1.2.3E	The descriptions of pin definitions and info. for MODE0, MODE1, MODE2 pins optimized.

Pin Name	Direction	Description
User I/O Pins		
IO [End] [Row/Column Number] [A/B]	I/O	[End] indicates the pin location, including L(left), R(right), B(bottom), and T(top).
		[Row/Column Number] indicates the pin row/column number. If [End] is T(top) or B(bottom), the pin indicates the column number of the corresponding CFU. If [End] is L(left) or R(right), the pin indicates the row number of the corresponding CFU.
		[A/B] indicates differential signal pair information.
Multi-Function Pins		
IO [End] [Row/Column Number] [A/B]/MMM		/MMM indicates one or more additional functions in addition to being general purpose user I/O. When not used for the additional functions, these pins can be user I/O.
D0	I/O	Data port D0 in CPU mode
D1	I/O	Data port D1 in CPU mode
D2	I/O	Data port D2 in CPU mode
D3	I/O	Data port D3 in CPU mode
D4	I/O	Data port D4 in CPU mode
D5	I/O	Data port D5 in CPU mode
D6	I/O	Data port D6 in CPU mode
D7	I/O	Data port D7 in CPU mode
WE_N	I	Select data input/output of D[7:0] in CPU mode.0: Write;1: Read.
DOUT	O	Data output in SERIAL mode
DIN	I, internal weak pull-up	Data input in SERIAL mode
TMS	I, internal weak pull-up	Serial mode input in JTAG mode
TCK	I	Serial clock input in JTAG mode
TDO	O	Serial data output in JTAG mode
TDI	I, internal weak pull-up	Serial data input in JTAG mode
JTAGSEL_N	I, internal weak pull-up	Reconfigure JTAG download function signal
RECONFIG_N	I, internal weak pull-up	Global reset GowinCONFIG logic signal, active low
FASTRD_N	I	Access SPI FLASH to select signal. Low, Fast Read mode; High, Read mode.
DONE[1]	O	High, the programming configuration has been completed successfully; Low, the programming configuration has not been completed or failed.
	I	When the DONE signal is low, delay the chip to activate. Activate the chip until the DONE signal is high.
READY[1]	I/O	High, the device can currently be programmed and configured; Low, the device cannot be programmed and configured.
MI	I	MI in MSPI mode

Pin Name	Direction	Description
MO	O	MO in MSPI mode
MCS_N	O	Enable signal MCS_N in MSPI mode, active-low
MCLK	O	Clock output MCLK in MSPI mode, with default frequency of 2.5Mhz
SCLK	I	Clock input in SSPI, SERIAL, and CPU modes
SO	O	SO in SSPI mode
SI	I/O	SI in SSPI mode
SSPI_CS_N	I/O	Enable signal SSPI_CS_N in SSPI mode, active-low, and internal weak pull-up
CLKHOLD_N	I, internal weak pull-up	Active-high in SSPI mode; Active-low in CPU mode.
GCLKC_[x]	I	Differential input pin of GCLKT_[x], C(Comp), [x]: global clock No.[2]
GCLKT_[x]	I	Global clock input pin, T(True), [x]: global clock No.
LPLL_C_fb/RPLL_C_fb	I	Left/right PLL feedback input pin, C(Comp)
LPLL_T_fb/RPLL_T_fb	I	Left/right PLL feedback input pin, T(True)
LPLL_C_in/RPLL_C_in	I	Left/right PLL clock input pin, C(Comp)
LPLL_T_in/RPLL_T_in	I	Left/right PLL clock input pin, T(True)
MODE2	I, internal weak pull-up	GowinCONFIG modes selection pin; if this pin is marked as “VCCIO”, it's internally powered; if this pin is marked as "GND", it's internally grounded.
MODE1	I, internal weak pull-up	GowinCONFIG modes selection pin; if this pin is marked as “VCCIO”, it's internally powered; if this pin is marked as "GND", it's internally grounded.
MODE0	I, internal weak pull-up	GowinCONFIG modes selection pin; if this pin is marked as “VCCIO”, it's internally powered; if this pin is marked as "GND", it's internally grounded.
Other Pins		
NC	NA	Reserved
VSS	NA	Ground
VCC	NA	Power supply pin of core voltage
VCCIO#	NA	Power supply pin of I/O voltage for I/O BANK#
VCCX	NA	Power supply pin of auxiliary voltage

Note!
[1] The default state of READY/DONE is open-drain output, internal weak pull-up. DONE outputs 0 during configuration.
[2] When the input is single-ended, GCLKC_[x] pin is not a global clock pin.



Note!

[1] Each Bank has independent reference voltage (VREF).

[2] You can select to use IOB internal VREF (equals to 0.5 x VCCIO).

[3] You can also select to use external VREF input (use any IO pins as external VREF input).

Note!
[1] The pin is internally grounded.
[2] The pin in internally short-circuited to VCCIO.

Pin Name	Function	BANK	Configuration Function	Differential Pair	FN32G	EQ144G	LQ100G	QN32X	QN48X
IOB10A	I/O	2	GCLKT_5	True_of_IOB10B		56	39		4
IOB10B	I/O	2	GCLKC_5	Comp_of_IOB10A		57	40		5
IOB11A	I/O	2	GCLKT_4	True_of_IOB11B	7	58	41	4	9
IOB11B	I/O	2	GCLKC_4	Comp_of_IOB11A	8	59	42	5	10
IOB12A	I/O	2		True_of_IOB12B		60			7
IOB12B	I/O	2		Comp_of_IOB12A		61	43		8
IOB13A	I/O	2		True_of_IOB13B		62			
IOB13B	I/O	2		Comp_of_IOB13A		63			
IOB14A	I/O	2		True_of_IOB14B		64	44		
IOB14B	I/O	2		Comp_of_IOB14A		65	45		
IOB15A	I/O	2		True_of_IOB15B		66			
IOB15B	I/O	2		Comp_of_IOB15A		67			
IOB16A	I/O	2		True_of_IOB16B		68	46		
IOB16B	I/O	2		Comp_of_IOB16A		69	47		
IOB17A	I/O	2		True_of_IOB17B		70	48		
IOB17B	I/O	2		Comp_of_IOB17A		71	49		
IOB18A	I/O	2		True_of_IOB18B					11
IOB18B	I/O	2		Comp_of_IOB18A					12
IOB19A	I/O	2		True_of_IOB19B		72	50		
IOB19B	I/O	2		Comp_of_IOB19A		75			
IOB2A	I/O	2		True_of_IOB2B	1	38	27		
IOB2B	I/O	2		Comp_of_IOB2A	2	39	28		
IOB3A	I/O	2		True_of_IOB3B	3	40	29		2
IOB3B	I/O	2		Comp_of_IOB3A		41	30		3
IOB4A	I/O	2		True_of_IOB4B		42			

Note!
[1] The pin is internally grounded.
[2] The pin in internally short-circuited to VCCIO.

Pin Name	Function	BANK	Configuration Function	Differential Pair	FN32G	EQ144G	LQ100G	QN32X	QN48X
IOB4B	I/O	2		Comp_of_IOB4A		43			
IOB5A	I/O	2		True_of_IOB5B		44	31		
IOB5B	I/O	2		Comp_of_IOB5A		45	32		
IOB6A	I/O	2		True_of_IOB6B		46			
IOB6B	I/O	2		Comp_of_IOB6A		47	33		
IOB7A	I/O	2		True_of_IOB7B		48	34		
IOB7B	I/O	2		Comp_of_IOB7A		49			
IOB8A	I/O	2		True_of_IOB8B		50	35		
IOB8B	I/O	2		Comp_of_IOB8A	6	51	36		
IOB9A	I/O	2		True_of_IOB9B		52			
IOB9B	I/O	2		Comp_of_IOB9A		54			
IOL10A	I/O	3		True_of_IOL10B		32	22		
IOL10B	I/O	3		Comp_of_IOL10A		34	23		
IOL2A	I/O	3	JTAGSEL_N	True_of_IOL2B		4	3	26	38
IOL2B	I/O	3		Comp_of_IOL2A		6	5	25	37
IOL3A	I/O	3		True_of_IOL3B		7			41
IOL3B	I/O	3		Comp_of_IOL3A		8		23	40
IOL4A	I/O	3		True_of_IOL4B		9			
IOL4B	I/O	3		Comp_of_IOL4A		10			
IOL5A	I/O	3	GCLKT_7	True_of_IOL5B	26	11	6	28	43
IOL5B	I/O	3	GCLKC_7	Comp_of_IOL5A	25	12	7	27	42
IOL6A	I/O	3	TMS	True_of_IOL6B	27	13	8	29	44
IOL6B	I/O	3	TCK	Comp_of_IOL6A	28	14	9	30	45
IOL6C	I/O	3	SCLK	True_of_IOL6D		15	10		
IOL6D	I/O	3	TDI	Comp_of_IOL6C	29	16	11	32	47

Note!
[1] The pin is internally grounded.
[2] The pin in internally short-circuited to VCCIO.

Pin Name	Function	BANK	Configuration Function	Differential Pair	FN32G	EQ144G	LQ100G	QN32X	QN48X
IOL6E	I/O	3	TDO	True_of_IOL6F	30	18	12	1	48
IOL6F	I/O	3	RECONFIG_N	Comp_of_IOL6E		20	14		
IOL6G	I/O	3	DONE	True_of_IOL6H		21	15		
IOL6H	I/O	3	READY	Comp_of_IOL6G		22	16		
IOL6I	I/O	3		True_of_IOL6J		23			
IOL6J	I/O	3		Comp_of_IOL6I		24			
IOL7A	I/O	3	GCLKT_6	True_of_IOL7B	31	25	17		
IOL7B	I/O	3	GCLKC_6	Comp_of_IOL7A	32	26	18		
IOL8A	I/O	3		True_of_IOL8B		27	19		
IOL8B	I/O	3		Comp_of_IOL8A		28	20		
IOL9A	I/O	3		True_of_IOL9B		29			
IOL9B	I/O	3		Comp_of_IOL9A		30			
IOR10A	I/O	1		True_of_IOR10B		78	55	8	
IOR10B	I/O	1		Comp_of_IOR10A		76	53		
IOR2A	I/O	1		True_of_IOR2B	16	106	73	16	23
IOR2B	I/O	1		Comp_of_IOR2A	15	104	72	17	24
IOR3A	I/O	1		True_of_IOR3B	14	102	70		
IOR3B	I/O	1		Comp_of_IOR3A		101	69		
IOR4A	I/O	1	RPLL_T_fb	True_of_IOR4B		100	68		
IOR4B	I/O	1	RPLL_C_fb	Comp_of_IOR4A		99	67		
IOR5A	I/O	1	GCLKT_2/RPLL_T_in	True_of_IOR5B		98	66	13	20
IOR5B	I/O	1	GCLKC_2/RPLL_C_in	Comp_of_IOR5A		97	65	14	21
IOR6A	I/O	1	MI/D7	True_of_IOR6B					
IOR6B	I/O	1	MO/D6	Comp_of_IOR6A					
IOR6C	I/O	1	MCS_N/D5	True_of_IOR6D					

Note!
[1] The pin is internally grounded.
[2] The pin in internally short-circuited to VCCIO.

Pin Name	Function	BANK	Configuration Function	Differential Pair	FN32G	EQ144G	LQ100G	QN32X	QN48X
IOR6D	I/O	1	MCLK/D4	Comp_of_IOR6C					
IOR6E	I/O	1	FASTRD_N/D3	True_of_IOR6F		92	64		
IOR6F	I/O	1	SI/D2	Comp_of_IOR6E		90	62		
IOR6G	I/O	1	SO/D1	True_of_IOR6H		88	61		
IOR6H	I/O	1	SSPI_CS_N/D0	Comp_of_IOR6G		87	60		
IOR6I	I/O	1	DIN/CLKHOLD_N	True_of_IOR6J		86	59		
IOR6J	I/O	1	DOUT/WE_N	Comp_of_IOR6I		85	58		
IOR7A	I/O	1	GCLKT_3	True_of_IOR7B	12	84	57	11	18
IOR7B	I/O	1	GCLKC_3	Comp_of_IOR7A	11	83	56	12	19
IOR8A	I/O	1		True_of_IOR8B		82		9	16
IOR8B	I/O	1		Comp_of_IOR8A		81		10	17
IOR9A	I/O	1		True_of_IOR9B		80			14
IOR9B	I/O	1		Comp_of_IOR9A		79			15
IOT10A	I/O	0		True_of_IOT10B		130	91		
IOT10B	I/O	0		Comp_of_IOT10A		129	90		
IOT11A	I/O	0		True_of_IOT11B		128	89		
IOT11B	I/O	0		Comp_of_IOT11A		126			
IOT12A	I/O	0		True_of_IOT12B		124	86		
IOT12B	I/O	0		Comp_of_IOT12A		123	85		
IOT13A	I/O	0		True_of_IOT13B		122			
IOT13B	I/O	0		Comp_of_IOT13A		121			
IOT14A	I/O	0		True_of_IOT14B	20	120	84	21	
IOT14B	I/O	0		Comp_of_IOT14A	19	119	83	20	
IOT15A	I/O	0		True_of_IOT15B		118	82		29
IOT15B	I/O	0		Comp_of_IOT15A		117	81		28

Note!
[1] The pin is internally grounded.
[2] The pin in internally short-circuited to VCCIO.

Pin Name	Function	BANK	Configuration Function	Differential Pair	FN32G	EQ144G	LQ100G	QN32X	QN48X
IOT16A	I/O	0		True_of_IOT16B	18	116	80		
IOT16B	I/O	0		Comp_of_IOT16A	17	115	79		
IOT17A	I/O	0		True_of_IOT17B		114	78		27
IOT17B	I/O	0		Comp_of_IOT17A		113	77		26
IOT2A	I/O	0		True_of_IOT2B		3			
IOT2B	I/O	0	MODE0	Comp_of_IOT2A	GND[1]	144	GND[1]	GND[1]	GND[1]
IOT3A	I/O	0	MODE2	True_of_IOT3B	GND[1]	GND[1]	GND[1]	GND[1]	GND[1]
IOT3B	I/O	0	MODE1	Comp_of_IOT3A	GND[1]	143	100	VCCIO[2]	GND[1]
IOT4A	I/O	0		True_of_IOT4B	24	142	99		36
IOT4B	I/O	0		Comp_of_IOT4A	23	141	98		35
IOT5A	I/O	0		True_of_IOT5B		140	97		
IOT5B	I/O	0		Comp_of_IOT5A		139	96		
IOT6A	I/O	0		True_of_IOT6B		138			34
IOT6B	I/O	0		Comp_of_IOT6A		137			33
IOT7A	I/O	0		True_of_IOT7B		136	95		
IOT7B	I/O	0		Comp_of_IOT7A		135	94		
IOT8A	I/O	0		True_of_IOT8B		134			
IOT8B	I/O	0		Comp_of_IOT8A		133			
IOT9A	I/O	0		True_of_IOT9B	22	132	93		32
IOT9B	I/O	0		Comp_of_IOT9A	21	131	92		31
VCC	Power	N/A			9	1	25	2	1
VCC	Power	N/A				36	75	18	25
VCC	Power	N/A				73	1		
VCC	Power	N/A				108	51		
VCCIO0	Power	N/A				109	76	19	30

Note!
[1] The pin is internally grounded.
[2] The pin in internally short-circuited to VCCIO.

Pin Name	Function	BANK	Configuration Function	Differential Pair	FN32G	EQ144G	LQ100G	QN32X	QN48X
VCCIO0	Power	N/A				127	88		
VCCIO0/VCCIO1	Power	N/A			13				
VCCIO0/VCCIO3	Power	N/A							
VCCIO1	Power	N/A				77	54	7	13
VCCIO1	Power	N/A				91	71	15	22
VCCIO1	Power	N/A				103	63		
VCCIO2	Power	N/A			5	37	26	6	6
VCCIO2	Power	N/A				55	38		
VCCIO3	Power	N/A			4	5	4	24	39
VCCIO3	Power	N/A				19	21	31	46
VCCIO3	Power	N/A				31	13		
VSS	Ground	N/A			10	2	2	3	
VSS	Ground	N/A				35	24	22	
VSS	Ground	N/A				74	52		
VSS	Ground	N/A				107	74		
VSS	Ground	N/A				125	87		
VSS	Ground	N/A				89	37		
VSS	Ground	N/A				105			
VSS	Ground	N/A				53			
VSS	Ground	N/A				17			
VSS	Ground	N/A				33			
NC	N/A	N/A				93			
NC	N/A	N/A				94			
NC	N/A	N/A				95			
NC	N/A	N/A				96			

Note!
[1] The pin is internally grounded.
[2] The pin in internally short-circuited to VCCIO.

Pin Name	Function	BANK	Configuration Function	Differential Pair	FN32G	EQ144G	LQ100G	QN32X	QN48X
NC	N/A	N/A				110			
NC	N/A	N/A				111			
NC	N/A	N/A				112			

Recommended Operating Conditions of FN32G Package in GW1NR-1			
Name	**Description**	**Min.**	**Max.**
VCC	Core voltage	1.14V	1.26V
VCCIO2, VCCIO3	I/O Bank power supply voltage	1.14V	3.6V
	When Flash is used, VCCIO3 provides voltage for Flash	1.71V	3.6V
VCCIO0/VCCIO1	I/O Bank power supply voltage, VCCIO0 and VCCIO1 are internally short-circuited.	1.14V	3.6V
Note! It is highly recommended that the epad connect to GND, but not a requirement.			
Recommended Operating Conditions of EQ144G/QN32X/QN48X Packages in GW1NR-1			
Name	**Description**	**Min.**	**Max.**
VCC	Core voltage	1.14V	1.26V
VCCIO0, VCCIO1, VCCIO2, VCCIO3	I/O Bank power supply voltage	1.14V	3.6V
	When Flash is used, VCCIO3 provides voltage for Flash	1.71V	3.6V
Note! It is highly recommended that the epad connect to GND, but not a requirement.			
Recommended Operating Conditions of LQ100G Package in GW1NR-1			
Name	**Description**	**Min.**	**Max.**
VCC	Core voltage	1.14V	1.26V
VCCIO0, VCCIO1, VCCIO2, VCCIO3	I/O Bank power supply voltage	1.14V	3.6V
	When Flash is used, VCCIO3 provides voltage for Flash	1.71V	3.6V