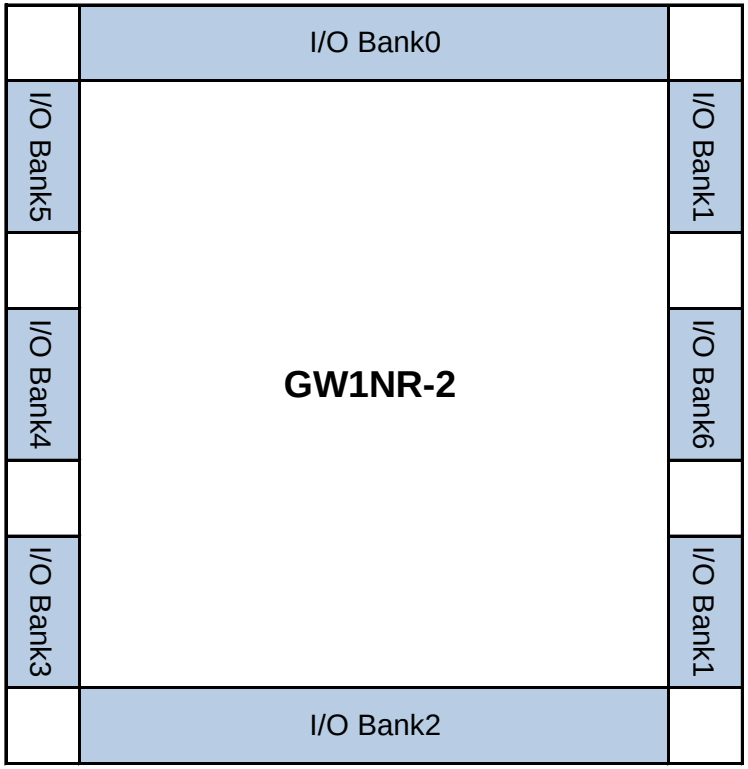
Date	Version	Description
02/02/2021	1.0E	Initial version published. Package MG49P, MG49G, and MG49PG supported.
02/23/2021	1.01E	Recommended operating conditions of core voltage for UV version added.
05/18/2021	1.02E	The descriptions of pin MODE0, MODE1, and MODE2 added.
10/20/2022	1.1E	Pin definitions updated. The note in Power sheet updated.
05/04/2023	1.1.1E	The descriptions of CLKHOLD_N pin and DIO pins in Pin Definitions sheet updated.
12/07/2023	1.1.2E	The descriptions of VCCD and VCCIOD pins in Pin Definitions sheet updated.
02/22/2024	1.1.3E	The note of VCCD and VCCIOD pins in Power sheet added.

Pin Name	I/O	Description
User I/O		
IO[End][Row/Column Number][A/B]	I/O	[End] indicates the pin location, including L(left), R(right), B(bottom), and T(top).
		[Row/Column Number] indicates the pin row/column number. If [End] is T(top) or B(bottom), the pin indicates the column number of the corresponding CFU. If [End] is L(left) or R(right), the pin indicates the row number of the corresponding CFU.
		[A/B] indicates differential signal pair information.
Multi-Function Pins		
IO[End][Row/Column Number][A/B]/MMM		/MMM represents one or more of the other functions in addition to being general purpose user I/O. When these functions are not in use, these pins can be used as user I/O.
D0	I/O	Data port D0 in CPU mode
D1	I/O	Data port D1 in CPU mode
D2	I/O	Data port D2 in CPU mode
D3	I/O	Data port D3 in CPU mode
D4	I/O	Data port D4 in CPU mode
D5	I/O	Data port D5 in CPU mode
D6	I/O	Data port D6 in CPU mode
D7	I/O	Data port D7 in CPU mode
WE_N	I	Select data input/output of D[7:0] in CPU mode.0: Write;1: Read.
DOUT	O	Data output in SERIAL mode
DIN	I, internal weak pull-up	Data input in SERIAL mode
TMS	I, internal weak pull-up	Serial mode input in JTAG mode
TCK	I	Serial clock input in JTAG mode
TDO	O	Serial data output in JTAG mode
TDI	I, internal weak pull-up	Serial data input in JTAG mode
JTAGSEL_N	I, internal weak pull-up	Reconfigure JTAG download function signal
RECONFIG_N	I, internal weak pull-up	Global reset GowinCONFIG logic signal, active low
FASTRD_N	I	Access SPI FLASH to select signal. Low, Fast Read mode; High, Read mode.
DONE[1]	O, internal weak pull-up	High, the programming configuration has been completed successfully; Low, the programming configuration has not been completed or failed.
	I, internal weak pull-up	When the DONE signal is low, delay the chip to activate. Activate the chip until the DONE signal is high.
READY[1]	I/O, internal weak pull-up	High, the device can be programmed and configured currently; Low, the device cannot be programmed and configured currently.
MI	I	MI in MSPI mode

Pin Name	I/O	Description
MO	O	MO in MSPI mode
MCS_N	O	Enable signal MCS_N in MSPI mode, active-low
MCLK	O	Clock output MCLK in MSPI mode, with default frequency of 2.5Mhz
SCLK	I	Clock input in SSPI, SERIAL, and CPU modes
SO	O	SO in SSPI mode
SI	I/O	SI in SSPI mode
SSPI_CS_N	I/O	Enable signal SSPI_CS_N in SSPI mode, active-low, and internal weak pull-up
CLKHOLD_N	I, internal weak pull-up	Active-high in SSPI mode; Active-low in CPU mode.
SDA	I/O	I2C serial data line: When I2C is supported in GowinCONFIG mode, external pull-up is required.
SCL	I	I2C serial clock line: When I2C is supported in GowinCONFIG mode, external pull-up is required.
GCLKC_[x]	I	Differential input pin of GCLKT_[x], C(Comp), [x]: global clock No.[2]
GCLKT_[x]	I	Global clock input pin, T(True), [x]: global clock No.
LPLL_C_fb/RPLL_C_fb	I	Left/Right PLL feedback input pin, C(Comp)
LPLL_T_fb/RPLL_T_fb	I	Left/Right PLL feedback input pin, T(True)
LPLL_C_in/RPLL_C_in	I	Left/Right PLL clock input pin, C(Comp)
LPLL_T_in/RPLL_T_in	I	Left/Right PLL clock input pin, T(True)
MODE2	I, internal weak pull-up	GowinCONFIG modes selection pin; if this pin is marked as “VCCIO”, it's internally powered; if this pin is marked as "GND", it's internally grounded.
MODE1	I, internal weak pull-up	GowinCONFIG modes selection pin; if this pin is marked as “VCCIO”, it's internally powered; if this pin is marked as "GND", it's internally grounded.
MODE0	I, internal weak pull-up	GowinCONFIG modes selection pin; if this pin is marked as “VCCIO”, it's internally powered; if this pin is marked as "GND", it's internally grounded.
Other Pins		
CKP	DIO[3]	The clock channel input pin of MIPI_DPHY_RX
CKN	DIO[3]	The clock channel differential pin of MIPI_DPHY_RX
RX0P	DIO[3]	The data channel 0 input pin of MIPI_DPHY_RX
RX0N	DIO[3]	The data channel 0 differential pin of MIPI_DPHY_RX
RX1P	DIO[3]	The data channel 1 input pin of MIPI_DPHY_RX
RX1N	DIO[3]	The data channel 1 differential pin of MIPI_DPHY_RX
RX2P	DIO[3]	The data channel 2 input pin of MIPI_DPHY_RX
RX2N	DIO[3]	The data channel 2 differential pin of MIPI_DPHY_RX

Pin Name	I/O	Description
RX3P	DIO[3]	The data channel 3 input pin of MIPI_DPHY_RX
RX3N	DIO[3]	The data channel 3 differential pin of MIPI_DPHY_RX
NC	NA	Reserved
VSS	NA	Ground
VCC	NA	Power supply pin of core voltage
VCCD	NA	Power supply pin of MIPI
VCCIOD	NA	Power supply pin of MIPI
VCCIO#	NA	Power supply pin of I/O voltage for I/O BANK#
VCCX	NA	Power supply pin of auxiliary voltage

Note!
[1] The default state of READY/DONE is open-drain output, internal weak pull-up. DONE outputs 0 during configuration.
[2] When the input is single-ended, GCLKC_[x] pin is not a global clock pin.
[3] DIO indicates a dedicated pin.



Note!

[1] Each Bank has independent reference voltage (VREF).

[2] You can select to use IOB internal VREF (equals to 0.5 * VCCIO).

[3] You can also select to use external VREF input (use any I/O pins as external VREF input).

Note!
[1] The pin is internally grounded.
[2] The pin is internal-circuited to VCCIO.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	MG49P	MG49PG	MG49G
IOB11A	I/O	2		True_of_IOB11B	True	x16			
IOB11B	I/O	2		Comp_of_IOB11A	True	none			
IOB12A/FASTRD_N	I/O	2	FASTRD_N	True_of_IOB12B	none	none			
IOB12B	I/O	2		Comp_of_IOB12A	none	none			
IOB13A	I/O	2		True_of_IOB13B	True	x16	G5	G5	G5
IOB13B	I/O	2		Comp_of_IOB13A	True	none	F5	F5	F5
IOB14A	I/O	2		True_of_IOB14B	none	none			
IOB14B	I/O	2		Comp_of_IOB14A	none	none			
IOB15A	I/O	2		True_of_IOB15B	True	x16			
IOB15B	I/O	2		Comp_of_IOB15A	True	none			
IOB16A	I/O	2		True_of_IOB16B	none	none			
IOB16B/DOUT/WE_N	I/O	2	DOUT/WE_N	Comp_of_IOB16A	none	none			
IOB17A	I/O	2		True_of_IOB17B	True	x16			
IOB17B	I/O	2		Comp_of_IOB17A	True	none			
IOB18A/SSPI_CS_N	I/O	2	SSPI_CS_N	True_of_IOB18B	none	none			
IOB18B/SI	I/O	2	SI	Comp_of_IOB18A	none	none			
IOB2A	I/O	2		True_of_IOB2B	True	x16			
IOB2B	I/O	2		Comp_of_IOB2A	True	none			
IOB3A/DIN/CLKHOLD_N	I/O	2	DIN/CLKHOLD_N	True_of_IOB3B	none	none			
IOB3B	I/O	2		Comp_of_IOB3A	none	none			
IOB4A	I/O	2		True_of_IOB4B	True	x16	G1	G1	G1
IOB4B	I/O	2		Comp_of_IOB4A	True	none	G2	G2	G2
IOB5A/SCLK	I/O	2	SCLK	True_of_IOB5B	none	none			
IOB5B/SO	I/O	2	SO	Comp_of_IOB5A	none	none			
IOB6A	I/O	2		True_of_IOB6B	True	x16			
IOB6B	I/O	2		Comp_of_IOB6A	True	none			
IOB7A/GCLKT_4	I/O	2	GCLKT_4	True_of_IOB7B	none	none	G3	G3	G3
IOB7B/GCLKC_4	I/O	2	GCLKC_4	Comp_of_IOB7A	none	none	F3	F3	F3
IOB8A	I/O	2		True_of_IOB8B	True	x16			
IOB8B	I/O	2		Comp_of_IOB8A	True	none			

Note!
[1] The pin is internally grounded.
[2] The pin is internal-circuited to VCCIO.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	MG49P	MG49PG	MG49G
IOB9A/GCLKT_3	I/O	2	GCLKT_3	True_of_IOB9B	none	none	G4	G4	G4
IOB9B/GCLKC_3	I/O	2	GCLKC_3	Comp_of_IOB9A	none	none	F4	F4	F4
IOL11A	I/O	4		True_of_IOL11B	True	x16			
IOL11B	I/O	4		Comp_of_IOL11A	True	none			
IOL12A/GCLKT_6	I/O	4	GCLKT_6	True_of_IOL12B	none	none	C1	C1	C1
IOL12B/GCLKC_6	I/O	4	GCLKC_6	Comp_of_IOL12A	none	none	C2	C2	C2
IOL13A	I/O	4		True_of_IOL13B	True	x16	D1	D1	D1
IOL13B	I/O	4		Comp_of_IOL13A	True	none	D2	D2	D2
IOL14A	I/O	4		True_of_IOL14B	none	none			
IOL14B	I/O	4		Comp_of_IOL14A	none	none			
IOL15A	I/O	3		True_of_IOL15B	True	x16			
IOL15B	I/O	3		Comp_of_IOL15A	True	none			
IOL16A/GCLKT_5	I/O	3	GCLKT_5	True_of_IOL16B	none	none	E1	E1	E1
IOL16B/GCLKC_5	I/O	3	GCLKC_5	Comp_of_IOL16A	none	none	E2	E2	E2
IOL17A	I/O	3		True_of_IOL17B	True	x16	F1	F1	F1
IOL17B	I/O	3		Comp_of_IOL17A	True	none	F2	F2	F2
IOL18A	I/O	3		True_of_IOL18B	none	none			
IOL18B	I/O	3		Comp_of_IOL18A	none	none			
IOL19A	I/O	3		True_of_IOL19B	none	none			
IOL19B	I/O	3		Comp_of_IOL19A	none	none			
IOL4A/LPLL_T_fb	I/O	5	LPLL_T_fb	True_of_IOL4B	True	x16			
IOL4B/LPLL_C_fb	I/O	5	LPLL_C_fb	Comp_of_IOL4A	True	none			
IOL5A/LPLL_T_in	I/O	5	LPLL_T_in	True_of_IOL5B	none	none			
IOL5B/LPLL_C_in	I/O	5	LPLL_C_in	Comp_of_IOL5A	none	none			
IOL6A/GCLKT_7	I/O	5	GCLKT_7	True_of_IOL6B	True	x16			
IOL6B/GCLKC_7	I/O	5	GCLKC_7	Comp_of_IOL6A	True	none			
IOL7A	I/O	5		True_of_IOL7B	none	none			
IOL7B	I/O	5		Comp_of_IOL7A	none	none			
IOL8A	I/O	5		True_of_IOL8B	True	x16			
IOL8B	I/O	5		Comp_of_IOL8A	True	none			

Note!
[1] The pin is internally grounded.
[2] The pin is internal-circuited to VCCIO.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	MG49P	MG49PG	MG49G
IOL9A	I/O	4		True_of_IOL9B	none	none			
IOL9B	I/O	4		Comp_of_IOL9A	none	none			
IOR11A/GCLKT_2	I/O	1	GCLKT_2	True_of_IOR11B	True	none			
IOR11B/GCLKC_2	I/O	1	GCLKC_2	Comp_of_IOR11A	True	none			
IOR12A	I/O	1		True_of_IOR12B	none	none			
IOR12B	I/O	1		Comp_of_IOR12A	none	none			
IOR13A	I/O	1		True_of_IOR13B	True	none			
IOR13B	I/O	1		Comp_of_IOR13A	True	none			
IOR14A	I/O	1		True_of_IOR14B	none	none			
IOR14B	I/O	1		Comp_of_IOR14A	none	none			
IOR15A	I/O	1		True_of_IOR15B	True	none			
IOR15B	I/O	1		Comp_of_IOR15A	True	none			
IOR16A	I/O	1		True_of_IOR16B	none	none			
IOR16B	I/O	1		Comp_of_IOR16A	none	none			
IOR17A	I/O	1		True_of_IOR17B	True	none			
IOR17B	I/O	1		Comp_of_IOR17A	True	none			
IOR18A	I/O	1		True_of_IOR18B	none	none			
IOR18B	I/O	1		Comp_of_IOR18A	none	none			
IOR19A	I/O	1		True_of_IOR19B	none	none			
IOR19B	I/O	1		Comp_of_IOR19A	none	none			
IOR1A	I/O	1		True_of_IOR1B	True	none			
IOR1B	I/O	1		Comp_of_IOR1A	True	none			
IOR2A	I/O	1		True_of_IOR2B	none	none			
IOR2B	I/O	1		Comp_of_IOR2A	none	none			
IOR3A/D2	I/O	1	D2	True_of_IOR3B	True	none			
IOR3B/D3	I/O	1	D3	Comp_of_IOR3A	True	none			
IOR4A/D0	I/O	1	D0	True_of_IOR4B	none	none			
IOR4B/D1	I/O	1	D1	Comp_of_IOR4A	none	none			
IOR5A/MI/D7	I/O	1	MI/D7	True_of_IOR5B	True	none			
IOR5B/MO/D6	I/O	1	MO/D6	Comp_of_IOR5A	True	none			

Note!
[1] The pin is internally grounded.
[2] The pin is internal-circuited to VCCIO.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	MG49P	MG49PG	MG49G
IOR6A/MCS_N/D5	I/O	1	MCS_N/D5	True_of_IOR6B	none	none			
IOR6B/MCLK/D4	I/O	1	MCLK/D4	Comp_of_IOR6A	none	none			
IOT11A/GCLKT_0	I/O	0	GCLKT_0	True_of_IOT11B	True	x16			
IOT11B/GCLKC_0	I/O	0	GCLKC_0	Comp_of_IOT11A	True	none			
IOT12A	I/O	0		True_of_IOT12B	none	none			
IOT12B	I/O	0		Comp_of_IOT12A	none	none			
IOT13A	I/O	0		True_of_IOT13B	True	x16	A5	A5	A5
IOT13B	I/O	0		Comp_of_IOT13A	True	none	B5	B5	B5
IOT14A/GCLKT_1/SCL	I/O	0	GCLKT_1/SCL	True_of_IOT14B	none	none	A4	A4	A4
IOT14B/GCLKC_1/SDA	I/O	0	GCLKC_1/SDA	Comp_of_IOT14A	none	none	B4	B4	B4
IOT15A	I/O	0		True_of_IOT15B	True	x16	A6	A6	A6
IOT15B	I/O	0		Comp_of_IOT15A	True	none	B6	B6	B6
IOT16A/JTAGSEL_N	I/O	0	JTAGSEL_N	True_of_IOT16B	none	none			
IOT16B/RECONFIG_N	I/O	0	RECONFIG_N	Comp_of_IOT16A	none	none			
IOT17A	I/O	0		True_of_IOT17B	True	x16	A7	A7	A7
IOT17B	I/O	0		Comp_of_IOT17A	True	none	B7	B7	B7
IOT18A/READY	I/O	0	READY	True_of_IOT18B	none	none			
IOT18B/DONE	I/O	0	DONE	Comp_of_IOT18A	none	none			
IOT19A	I/O	0		True_of_IOT19B	none	none			
IOT19B	I/O	0		Comp_of_IOT19A	none	none			
IOT2A/MODE0	I/O	0	MODE0	True_of_IOT2B	none	none	GND[1]	GND[1]	GND[1]
IOT2B/MODE1	I/O	0	MODE1	Comp_of_IOT2A	none	none	GND[1]	GND[1]	GND[1]
IOT3A/MODE2	I/O	0	MODE2	True_of_IOT3B	none	none	VCCIO[2]	VCCIO[2]	VCCIO[2]
IOT4A	I/O	0		True_of_IOT4B	True	x16			
IOT4B	I/O	0		Comp_of_IOT4A	True	none			
IOT5A	I/O	0		True_of_IOT5B	none	none			
IOT5B	I/O	0		Comp_of_IOT5A	none	none			
IOT6A	I/O	0		True_of_IOT6B	True	x16			
IOT6B	I/O	0		Comp_of_IOT6A	True	none			

Note!
[1] The pin is internally grounded.
[2] The pin is internal-circuited to VCCIO.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	MG49P	MG49PG	MG49G
IOT7A/TDO	I/O	0	TDO	True_of_IOT7B	none	none	A1	A1	A1
IOT7B/TDI	I/O	0	TDI	Comp_of_IOT7A	none	none	B1	B1	B1
IOT8A	I/O	0		True_of_IOT8B	True	x16	A3	A3	A3
IOT8B	I/O	0		Comp_of_IOT8A	True	none	B3	B3	B3
IOT9A/TCK	I/O	0	TCK	True_of_IOT9B	none	none	A2	A2	A2
IOT9B/TMS	I/O	0	TMS	Comp_of_IOT9A	none	none	B2	B2	B2
CKN	DIO	6		Comp_of_CKP	none	none	E6	E6	E6
CKP	DIO	6		True_of_CKN	none	none	E7	E7	E7
RX0N	DIO	6		Comp_of_RX0P	none	none	G6	G6	G6
RX0P	DIO	6		True_of_RX0N	none	none	G7	G7	G7
RX1N	DIO	6		Comp_of_RX1P	none	none	F6	F6	F6
RX1P	DIO	6		True_of_RX1N	none	none	F7	F7	F7
RX2N	DIO	6		Comp_of_RX2P	none	none	D6	D6	D6
RX2P	DIO	6		True_of_RX2N	none	none	D7	D7	D7
RX3N	DIO	6		Comp_of_RX3P	none	none	C6	C6	C6
RX3P	DIO	6		True_of_RX3N	none	none	C7	C7	C7
VCC	Power	N/A					C3	C3	C3
VCCD	Power	N/A					E4	E4	E4
VCCIO0	Power	N/A					C5	C5	C5
VCCIO1	Power	N/A					D5	D5	D5
VCCIO2/VCCIO3/VCCIO4/VCCIO5	Power	N/A					D3	D3	D3
VCCIOD	Power	N/A					E5	E5	E5
VCCX	Power	N/A					E3	E3	E3
VSS	Ground	N/A					C4	C4	C4
VSS	Ground	N/A					D4	D4	D4

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	MG49P	MG49PG	MG49G
BANK5 True LVDS Pair									
IOL4A/LPLL_T_fb	I/O	5	LPLL_T_fb	True_of_IOL4B	True	x16			
IOL4B/LPLL_C_fb	I/O	5	LPLL_C_fb	Comp_of_IOL4A	True	none			
IOL6A/GCLKT_7	I/O	5	GCLKT_7	True_of_IOL6B	True	x16			
IOL6B/GCLKC_7	I/O	5	GCLKC_7	Comp_of_IOL6A	True	none			
IOL8A	I/O	5		True_of_IOL8B	True	x16			
IOL8B	I/O	5		Comp_of_IOL8A	True	none			
BANK4 True LVDS Pair									
IOL11A	I/O	4		True_of_IOL11B	True	x16			
IOL11B	I/O	4		Comp_of_IOL11A	True	none			
IOL13A	I/O	4		True_of_IOL13B	True	x16	D1	D1	D1
IOL13B	I/O	4		Comp_of_IOL13A	True	none	D2	D2	D2
BANK3 True LVDS Pair									
IOL15A	I/O	3		True_of_IOL15B	True	x16			
IOL15B	I/O	3		Comp_of_IOL15A	True	none			
IOL17A	I/O	3		True_of_IOL17B	True	x16	F1	F1	F1
IOL17B	I/O	3		Comp_of_IOL17A	True	none	F2	F2	F2
BANK2 True LVDS Pair									
IOB11A	I/O	2		True_of_IOB11B	True	x16			
IOB11B	I/O	2		Comp_of_IOB11A	True	none			
IOB13A	I/O	2		True_of_IOB13B	True	x16	G5	G5	G5
IOB13B	I/O	2		Comp_of_IOB13A	True	none	F5	F5	F5
IOB15A	I/O	2		True_of_IOB15B	True	x16			
IOB15B	I/O	2		Comp_of_IOB15A	True	none			
IOB17A	I/O	2		True_of_IOB17B	True	x16			
IOB17B	I/O	2		Comp_of_IOB17A	True	none			
IOB2A	I/O	2		True_of_IOB2B	True	x16			
IOB2B	I/O	2		Comp_of_IOB2A	True	none			
IOB4A	I/O	2		True_of_IOB4B	True	x16	G1	G1	G1
IOB4B	I/O	2		Comp_of_IOB4A	True	none	G2	G2	G2
IOB6A	I/O	2		True_of_IOB6B	True	x16			
IOB6B	I/O	2		Comp_of_IOB6A	True	none			

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	MG49P	MG49PG	MG49G
IOB8A	I/O	2		True_of_IOB8B	True	x16			
IOB8B	I/O	2		Comp_of_IOB8A	True	none			
BANK1 True LVDS Pair									
IOR11A/GCLKT_2	I/O	1	GCLKT_2	True_of_IOR11B	True	none			
IOR11B/GCLKC_2	I/O	1	GCLKC_2	Comp_of_IOR11A	True	none			
IOR13A	I/O	1		True_of_IOR13B	True	none			
IOR13B	I/O	1		Comp_of_IOR13A	True	none			
IOR15A	I/O	1		True_of_IOR15B	True	none			
IOR15B	I/O	1		Comp_of_IOR15A	True	none			
IOR17A	I/O	1		True_of_IOR17B	True	none			
IOR17B	I/O	1		Comp_of_IOR17A	True	none			
IOR1A	I/O	1		True_of_IOR1B	True	none			
IOR1B	I/O	1		Comp_of_IOR1A	True	none			
IOR3A/D2	I/O	1	D2	True_of_IOR3B	True	none			
IOR3B/D3	I/O	1	D3	Comp_of_IOR3A	True	none			
IOR5A/MI/D7	I/O	1	MI/D7	True_of_IOR5B	True	none			
IOR5B/MO/D6	I/O	1	MO/D6	Comp_of_IOR5A	True	none			
BANK0 True LVDS Pair									
IOT11A/GCLKT_0	I/O	0	GCLKT_0	True_of_IOT11B	True	x16			
IOT11B/GCLKC_0	I/O	0	GCLKC_0	Comp_of_IOT11A	True	none			
IOT13A	I/O	0		True_of_IOT13B	True	x16	A5	A5	A5
IOT13B	I/O	0		Comp_of_IOT13A	True	none	B5	B5	B5
IOT15A	I/O	0		True_of_IOT15B	True	x16	A6	A6	A6
IOT15B	I/O	0		Comp_of_IOT15A	True	none	B6	B6	B6
IOT17A	I/O	0		True_of_IOT17B	True	x16	A7	A7	A7
IOT17B	I/O	0		Comp_of_IOT17A	True	none	B7	B7	B7
IOT4A	I/O	0		True_of_IOT4B	True	x16			
IOT4B	I/O	0		Comp_of_IOT4A	True	none			
IOT6A	I/O	0		True_of_IOT6B	True	x16			
IOT6B	I/O	0		Comp_of_IOT6A	True	none			
IOT8A	I/O	0		True_of_IOT8B	True	x16	A3	A3	A3
IOT8B	I/O	0		Comp_of_IOT8A	True	none	B3	B3	B3

Note!
VCCX should be greater than or equal to VCCIO.
[1] When MIPI HARD Core is not used, users can either leave VCCD and VCCIOD floating or connect them to 1.2V power.

Recommended Operating Conditions of Package MG49P in GW1NR-2				
Name	**Description**		**Min.**	**Max.**
VCC	Core voltage	LV version	1.14V	1.26V
		UV version	1.71V	3.6V
VCCIO1	VCCIO1 is connected to PSRAM and provides power for PSRAM.		1.71V	1.89V
VCCIO0	I/O Bank voltage		1.14V	3.6V
VCCIO2/VCCIO3/VCCIO4/VCCIO5	I/O Bank voltage, VCCIO2, VCCIO3, VCCIO4, and VCCIO5 are internally short-circuited.		1.14V	3.6V
VCCD[1]	Core voltage power supply pin of MIPI_DPHY_RX		1.14V	1.26V
VCCIOD[1]	I/O voltage power supply pin of DIO BANK6		1.14V	1.26V
VCCX	Auxiliary voltage		1.71V	3.6V

Recommended Operating Conditions of Package MG49PG in GW1NR-2				
Name	**Description**		**Min.**	**Max.**
VCC	Core voltage	LV version	1.14V	1.26V
		UV version	1.71V	3.6V
VCCIO1	VCCIO1 is connected to PSRAM and FLASH, and provides power for them.		1.71V	1.89V
VCCIO0	I/O Bank voltage		1.14V	3.6V
VCCIO2/VCCIO3/VCCIO4/VCCIO5	I/O Bank voltage, VCCIO2, VCCIO3, VCCIO4, and VCCIO5 are internally short-circuited.		1.14V	3.6V
VCCD[1]	Core voltage power supply pin of MIPI_DPHY_RX		1.14V	1.26V
VCCIOD[1]	I/O voltage power supply pin of DIO BANK6		1.14V	1.26V
VCCX	Auxiliary voltage		1.71V	3.6V

Recommended Operating Conditions of Package MG49G in GW1NR-2				
Name	**Description**		**Min.**	**Max.**
VCC	Core voltage	LV version	1.14V	1.26V
		UV version	1.71V	3.6V
VCCIO1	VCCIO1 is connected to FLASH and provides power for FLASH.		1.71V	3.6V
VCCIO0	I/O Bank voltage		1.14V	3.6V
VCCIO2/VCCIO3/VCCIO4/VCCIO5	I/O Bank voltage, VCCIO2, VCCIO3, VCCIO4, and VCCIO5 are internally short-circuited.		1.14V	3.6V
VCCD[1]	Core voltage power supply pin of MIPI_DPHY_RX		1.14V	1.26V
VCCIOD[1]	I/O voltage power supply pin of DIO BANK6		1.14V	1.26V
VCCX	Auxiliary voltage		1.71V	3.6V