GW1NS series of FPGA Products

Package & Pinout User Guide

UG823-1.8.2E, 08/09/2024

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Revision History

Date	Version	Description
09/10/2018	1.0E	Initial version published (Preliminary).
11/22/2018	1.1E	Pins distribution view for different packages added.
01/10/2019	1.2E	● Quantity of GW1NS-2/GW1NS-2C Pins updated; ● Introduction to the I/O BANK updated.
04/03/2019	1.3E	CS36 package outline updated.
10/12/2019	1.4E	GW1NS-4 / GW1NS-4C added.
11/12/2019	1.5E	CS49 package info. added and CS49 POD added.
03/30/2020	1.6E	GW1NS-2/GW1NS-2C CS36U package info. added.
04/16/2020	1.6.1E	● GW1NS-2C CS36U package info. removed; ● The pins distribution view and pin number of GW1NS-4/GW1NS-4C QN48 updated.
07/28/2020	1.7E	GW1NS-4/4C MG64 package info. added.
11/25/2020	1.7.1E	CS49 package outline updated.
06/30/2021	1.7.2E	Section 2.4.1 and 3.1 updated.
10/18/2022	1.8E	● The unit in the package outline unified to millimeter. ● GW1NS-2 and GW1NS-2C removed. ● Pin definitions updated.
06/30/2023	1.8.1E	GW1NS-4 QN32 package info. and outline added.
08/09/2024	1.8.2E	● The information of LQ144 package for GW1NS-4C devices added. ● The description of “2.5 Introduction to the I/O BANK” optimized. ● The note of “Figure 4-7 Package Outline” added.

Contents

Contents i
List of Figures ii
List of Tables iii
1 About This Guide 1
1.1 Purpose 1
1.2 Related Documents 1
1.3 Abbreviations and Terminology 1
1.4 Support and Feedback 2
2 Overview 3
2.1 PB-Free Package 3
2.2 Package and Max. User I/O Information 4
2.3 Power Pins 4
2.4 Pin Quantity 4
2.4.1 Quantity of GW1NS-4/GW1NS-4C Pins 4
2.5 Introduction to the I/O BANK 6
3 View of Pin Distribution 7
3.1 View of GW1NS-4/GW1NS-4C Pin Distribution 7
3.1.1 View of CS49 Pin Distribution 7
3.1.2 View of QN48 Pin Distribution 8
3.1.3 View of MG64 Pin Distribution 9
3.1.4 View of QN32 Pin Distribution 10
3.1.5 View of LQ144 Pin Distribution 11
4 Package Diagrams 12
4.1 CS49 Package Outline (2.9mm x 2.9mm, GW1NS-4/4C) 12
4.2 QN48 Package Outline (6mm x 6mm, GW1NS-4/4C) 14
4.3 MG64 Package Outline (4.2mm x 4.2mm, GW1NS-4/4C) 16
4.4 QN32 Package Outline (5mm x 5mm, GW1NS-4) 18
4.5 LQ144 Package Outline (20mm x 20mm, GW1NS-4C) 20

List of Figures

Figure 3-1 View of GW1NS-4/GW1NS-4C CS49 Pins Distribution (Top View) 7
Figure 3-2 View of GW1NS-4/GW1NS-4C QN48 Pins Distribution (Top View)..... 8
Figure 3-3 View of GW1NS-4/GW1NS-4C MG64 Pins Distribution (Top View) 9
Figure 3-4 View of GW1NS-4 QN32 Pins Distribution (Top View)..... 10
Figure 3-5 View of GW1NS-4C LQ144 Pins Distribution (Top View)..... 11
Figure 4-1 Package Outline CS49 (GW1NS-4/4C)..... 12
Figure 4-2 Recommended PCB Layout CS49 (GW1NS-4/4C) 13
Figure 4-3 Package Outline QN48 (GW1NS-4/4C) 14
Figure 4-4 Recommended PCB Layout QN48 (GW1NS-4/4C)..... 15
Figure 4-5 Package Outline MG64 (GW1NS-4/4C)..... 16
Figure 4-6 Recommended PCB Layout MG64 (GW1NS-4/4C) 17
Figure 4-7 Package Outline QN32 (GW1NS-4)..... 18
Figure 4-8 Recommended PCB Layout QN32 (GW1NS-4) 19
Figure 4-9 Package Outline LQ144 (GW1NS-4C)..... 20
Figure 4-10 Recommended PCB Layout LQ144 (GW1NS-4C) 21

List of Tables

Table 1-1 Abbreviations and Terminology 1
Table 2-1 Package and Max. User I/O Information 4
Table 2-2 GW1NS Power Pins 4
Table 2-3 Quantity of GW1NS-4/GW1NS-4C Pins 4
Table 3-1 Other pins in GW1NS-4/GW1NS-4C CS49 7
Table 3-2 Other pins in GW1NS-4/GW1NS-4C QN48 8
Table 3-3 Other pins in GW1NS-4/GW1NS-4C MG64 9
Table 3-4 Other pins in GW1NS-4 QN32 10
Table 3-5 Other pins in GW1NS-4C LQ144 11

1 About This Guide

1.1 Purpose

This manual contains an introduction to the GW1NS series of FPGA products together with a definition of the pins, list of pin numbers, distribution of pins, and package diagrams.

1.2 Related Documents

The latest user guides are available on GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

1. DS821, GW1NS series of FPGA Products Data Sheet
2. UG290, Gowin FPGA Products Programming and Configuration User Guide
3. UG823, GW1NS series of FPGA Products Package and Pinout
4. UG824, GW1NS-4&4C Pinout

1.3 Abbreviations and Terminology

The abbreviations and terminologies used in this manual are set out in Table 1-1 below.

Table 1-1 Abbreviations and Terminology

Abbreviations and Terminology	Meaning
CS	WLCSP package
FPGA	Field Programmable Gate Array
LQ	LQFP package
MG	MBGA package
QN	QFN package

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

The GW1NS series of FPGA products are the first-generation products in the LittleBee family and include SoC FPGA devices and non-SoC FPGA devices. SoC FPFA is embedded with an ARM Cortex-M3 hard core processor, while no ARM Cortex-M3 hard core processor is included in the non-SoC FPGA devices. When the ARM Cortex-M3 hard-core processor is employed as the core, the needs of the Min. memory can be met. FPGA logic resources and other embedded resources can flexibly facilitate the peripheral control functions, which provide excellent calculation functions and exceptional system response interrupts. They also offer high performance, low power consumption, a small number of pins, flexible usage, instant start-up, affordability, nonvolatile, high security, and abundant package types, among other benefits. The GW1NS series of SoC FPFA products achieve seamless connection between programmable logic devices and embedded processors. They are compatible with multiple peripheral device standards and can, therefore, reduce costs of operation and be widely deployed in industrial control, communication, Internet of Things, servo drive, consumption fields, etc.

2.1 PB-Free Package

The GW1NS series of FPGA products are PB free in line with the EU ROHS environmental directives. The substances used in the GW1NS series of FPGA products are in full compliance with the IPC-1752 standards.

2.2 Package and Max. User I/O Information

Table 2-1 Package and Max. User I/O Information

Package	Pitch (mm)	Size (mm)	GW1NS-4	GW1NS-4C	GW1NS-4/GW1NS-4C
QN48	0.4	6 x 6	-	-	38 (4)
CS49	0.4	2.9 x 2.9	-	-	42 (8)
MG64	0.5	4.2 x 4.2	-	-	55 (8)
QN32	0.5	5 x 5	23 (1)	-	-
LQ144	0.5	20 x 20	-	82 (5)	-

Note!

- In this manual, abbreviations are employed to refer to the package types. See 1.3 Abbreviations and Terminology for details.
- The JTAGSEL_N and JTAG pins are exclusive. The JTAGSEL_N pin and the four pins of JTAG (TCK, TDI, TDO, and TMS) cannot be simultaneously used as I/O. When mode [2:0] = 001, JTAGSEL_N and the four JTAG pins (TCK, TDI, TDO, and TMS) can be used as GPIO simultaneously.

2.3 Power Pins

Table 2-2 GW1NS Power Pins

VCC	VCCIO0	VCCIO1	VCCIO2
VCCIO3	VCCX	VSS	NC
VCCPLL	VCCP	–	–

2.4 Pin Quantity

2.4.1 Quantity of GW1NS-4/GW1NS-4C Pins

Table 2-3 Quantity of GW1NS-4/GW1NS-4C Pins

Pin Type		GW1NS-4	GW1NS-4C	GW1NS-4/GW1NS-4C		
		QN32	LQ144	CS49	QN48	MG64
I/O Single end/ Differential pair /LVDS [1]	Bank0	9/3/0	18/8/0	8/3/0	8/3/0	10/3/0
	Bank1	4/2/0	13/6/0	18/9/0	10/5/0	28/14/0
	Bank2	6/2/1	25/12/0	16/8/8	9/4/4	18/9/8
	Bank3	4/2/0	26/13/0	0/0/0	11/5/0	0/0/0
Max. User I/O [2]		23	82	42	38	55
Differential Pair		9	39	20	17	26
True LVDS output		1	5	8	4	8
VCC		3	5	1	2	1
VCCX		1	0	1	1	1
VCCIO0		1	1	0	1	1
VCCIO1		1	2	1	1	1
VCCIO2		1	0	1	1	1
VCCIO3		1	0	0	2	1
VCCIO0/VCCIO3[3]		0	0	1	0	0

Pin Type	GW1NS-4	GW1NS-4C	GW1NS-4/GW1NS-4C		
	QN32	LQ144	CS49	QN48	MG64
VCCIO2/VCCIO3/VCCX	0	7	0	0	0
VSS	1	36	2	1	2
MODE0	0	1	0	0	0
MODE1	1	1	0	1	0
MODE2	0	1	0	0	0
JTAGSEL_N	0	1	0	1	1
NC	0	11	0	0	0

Note!

- [1] Single end/ Differential I/O quantity include CLK pins, and download pins;
- [2] The JTAGSEL_N and JTAG pins are exclusive. The JTAGSEL_N pin and the four pins of JTAG (TCK, TDI, TDO, and TMS) cannot be simultaneously used as I/O.
- [3] Pin multiplexing.

2.5 Introduction to the I/O BANK

There are four I/O Banks in the GW1NS series of FPGA products.

Please refer to DS821, GW1NS series of FPGA Products Data Sheet > 2.3 Input/Output Blocks for detailed Bank distribution schematic.

This manual provides an overview of the distribution view of the pins in the GW1NS series of FPGA products. Please refer to 3 View of Pin Distribution for further details. Different I/O Banks of the GW1NS series of FPGA products are marked with different colors.

User I/O, power, and ground are also marked with different symbols and colors. The various symbols and colors used for the various pins are defined as follows:

- "  " denotes I/Os in BANK0.
- "  " denotes I/Os in BANK1.
- "  " denotes I/Os in BANK2.
- "  " denotes I/Os in BANK3.
- "  " denotes VCC, VCCX, and VCCIO.
- "  " denotes VCC. The filling color does not change.
- "  " denotes VSS. The filling color does not change.
- "  " denotes NC.

3 View of Pin Distribution

3.1 View of GW1NS-4/GW1NS-4C Pin Distribution

3.1.1 View of CS49 Pin Distribution

Figure 3-1 View of GW1NS-4/GW1NS-4C CS49 Pins Distribution (Top View)

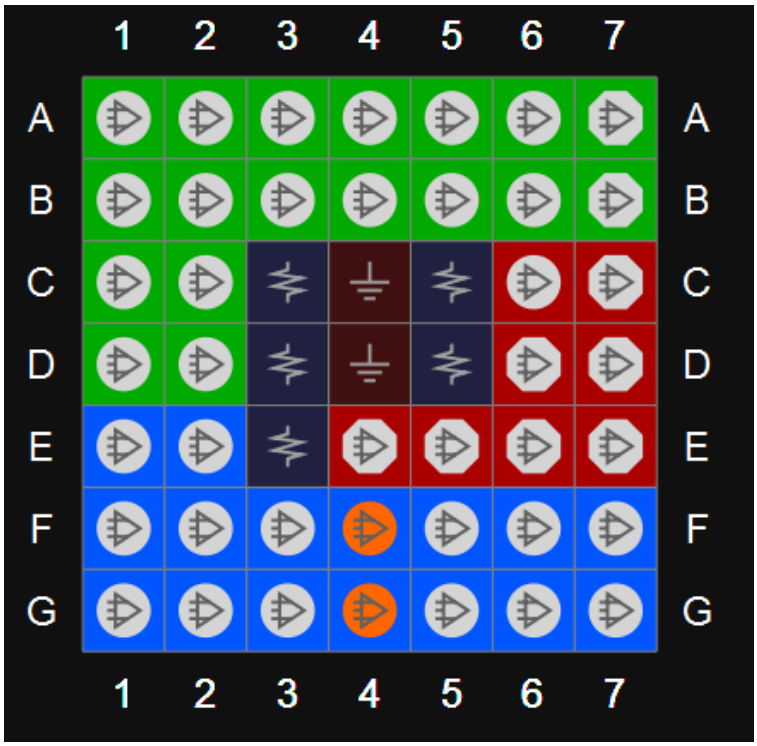


Table 3-1 Other pins in GW1NS-4/GW1NS-4C CS49

VCC	D5
VCCIO1	C3
VCCIO2	E3
VCCX	D3
VCCIO0/VCCIO3	C5
VSS	D4,C4

3.1.2 View of QN48 Pin Distribution

Figure 3-2 View of GW1NS-4/GW1NS-4C QN48 Pins Distribution (Top View)

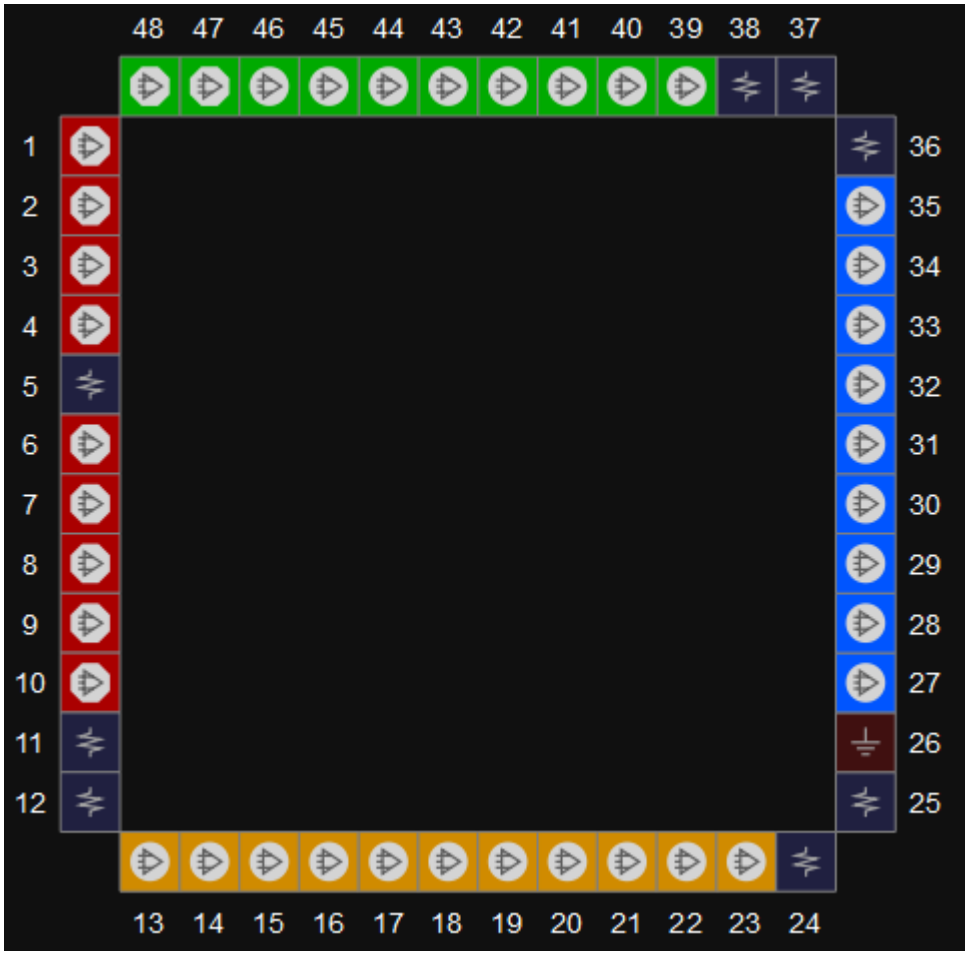


Table 3-2 Other pins in GW1NS-4/GW1NS-4C QN48

VCC	11,37
VCCIO0	5
VCCIO1	38
VCCIO2	36
VCCIO3	12,24
VCCX	25
VSS	26

3.1.3 View of MG64 Pin Distribution

Figure 3-3 View of GW1NS-4/GW1NS-4C MG64 Pins Distribution (Top View)

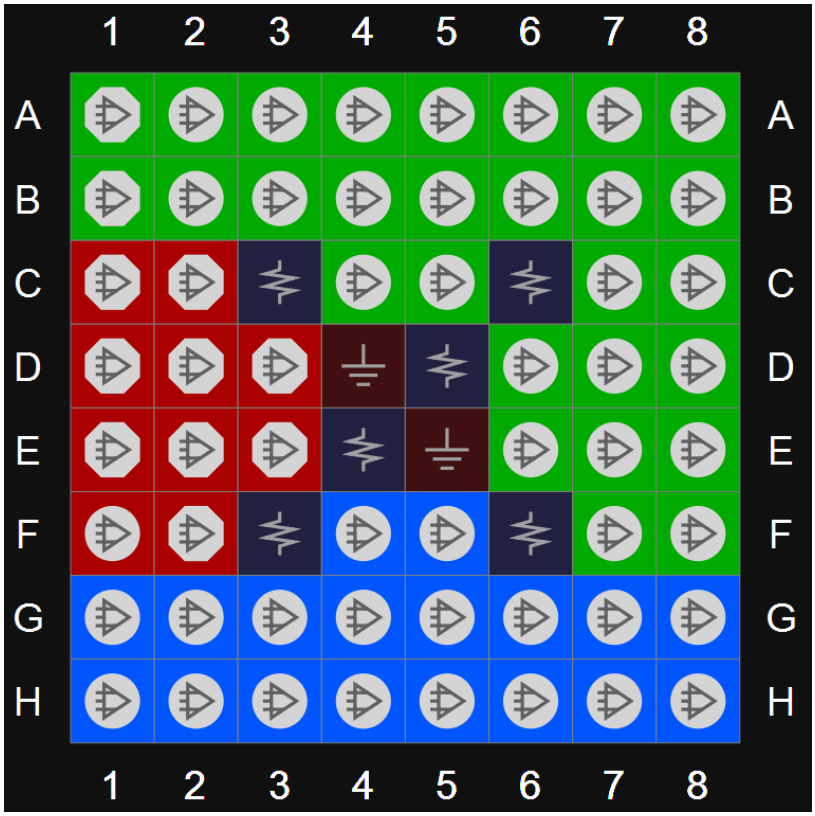


Table 3-3 Other pins in GW1NS-4/GW1NS-4C MG64

VCC	D5
VCCIO0	C3
VCCIO1	C6
VCCIO2	F6
VCCIO3	F3
VCCX	E4
VSS	D4,E5

3.1.4 View of QN32 Pin Distribution

Figure 3-4 View of GW1NS-4 QN32 Pins Distribution (Top View)

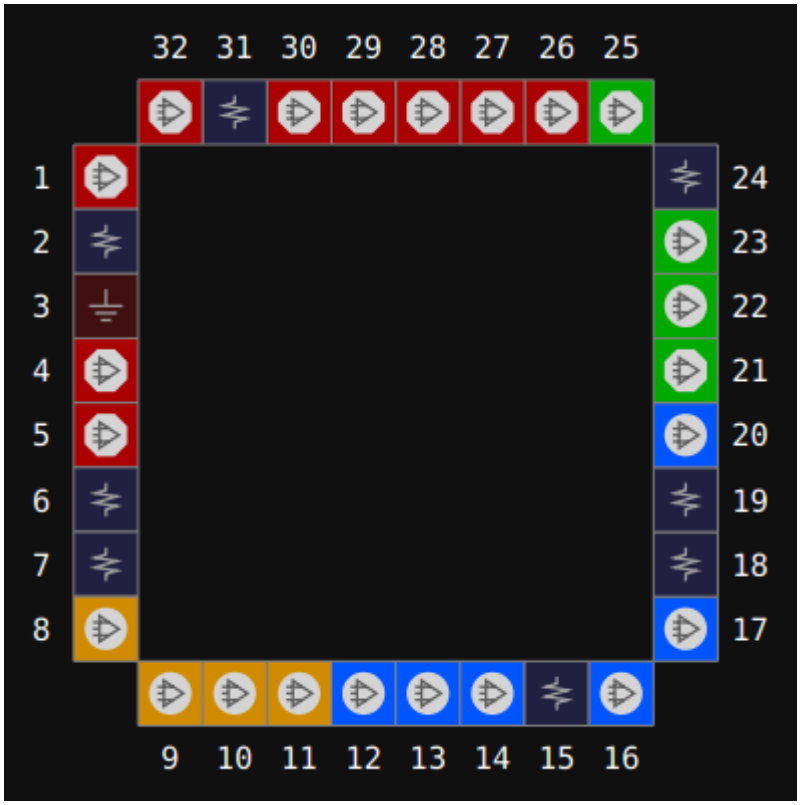


Table 3-4 Other pins in GW1NS-4 QN32

VCC	2,18,6
VCCIO0	31
VCCIO1	24
VCCIO2	19
VCCIO3	15
VCCX	7
VSS	3

3.1.5 View of LQ144 Pin Distribution

Figure 3-5 View of GW1NS-4C LQ144 Pins Distribution (Top View)

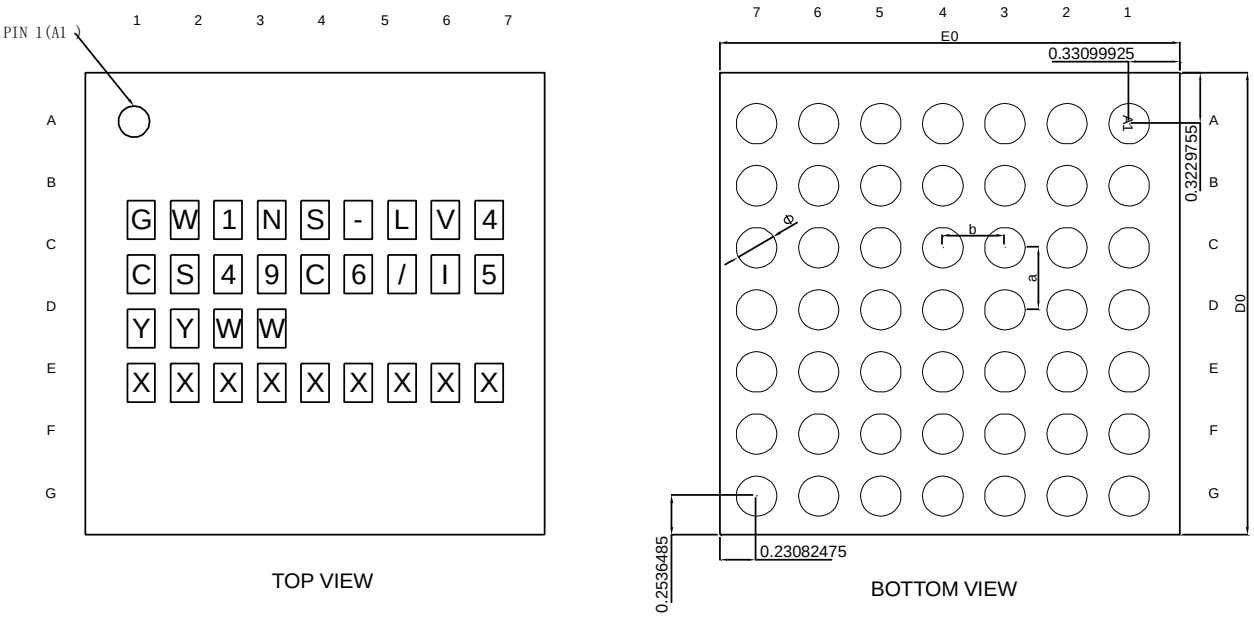
Table 3-5 Other pins in GW1NS-4C LQ144

VCC	48,36,108,104,132
VCCIO0	77
VCCIO1	37,55
VCCIO2/VCCIO3/VCCX	47,19,5,127,35,91,109
VSS	2,17,53,133,144,74,75,76,78,79,80,82,83,84,85,86,87,88,89,92,93,94,95,96,97,98,99,100,105,106,107,122,123,124,125,126

4 Package Diagrams

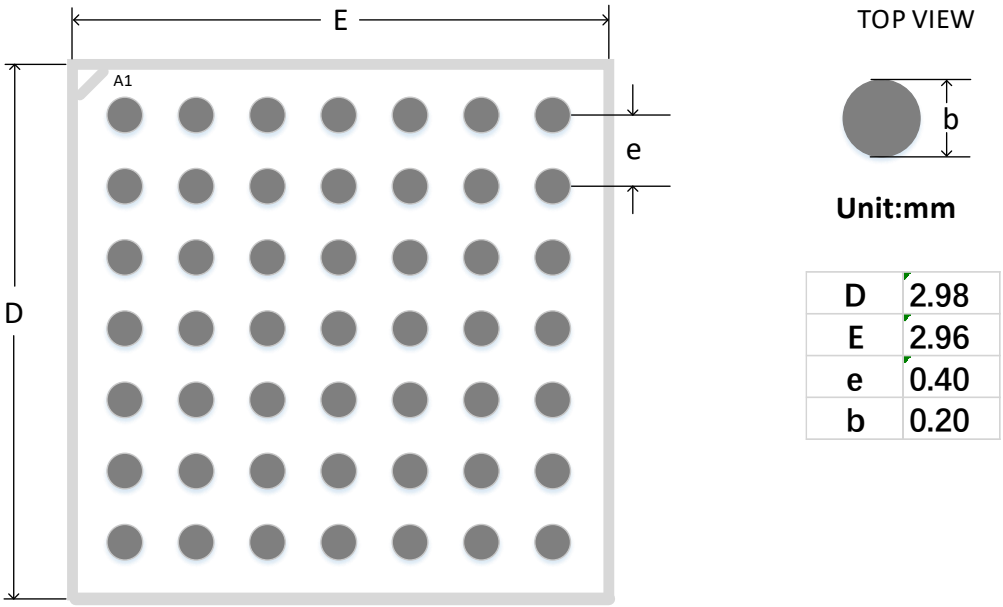
4.1 CS49 Package Outline (2.9mm x 2.9mm, GW1NS-4/4C)

Figure 4-1 Package Outline CS49 (GW1NS-4/4C)



SYMBOL	ITEM	DATA(mm)
D0*E0	PACKAGE SIZE X*Y	2.9766*2.9618±0.025
Φ	BALL DIAMETER	0.26±0.03
a/b	BALL PITCH X/Y	0.4/0.4
N	BALL COUNT	49
H	PACKAGE HEIGHT	0.54±0.05
H1	BALL HEIGHT	0.2±0.025
H2	SI THICKNESS+PI	0.315±0.015
H3	BACK COATING	0.025±0.01

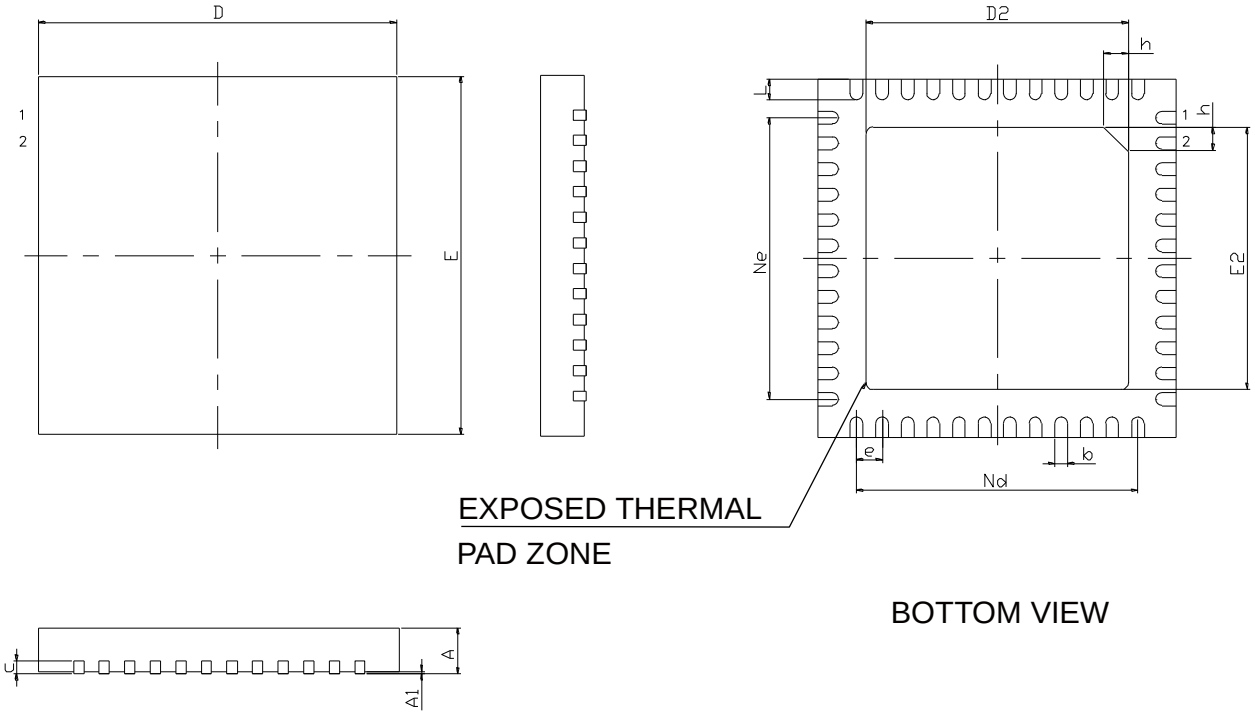
Figure 4-2 Recommended PCB Layout CS49 (GW1NS-4/4C)



D	2.98
E	2.96
e	0.40
b	0.20

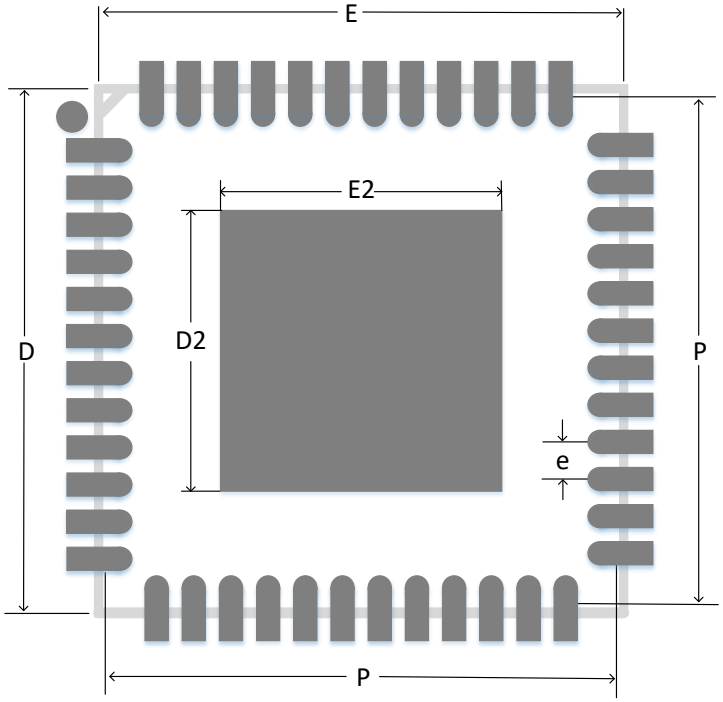
4.2 QN48 Package Outline (6mm x 6mm, GW1NS-4/4C)

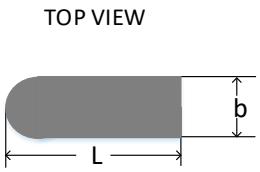
Figure 4-3 Package Outline QN48 (GW1NS-4/4C)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.75	0.85	0.85
A1	—	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.23
D	5.90	6.00	6.10
D2	4.10	4.20	4.30
e	0.40BSC		
Ne	4.40BSC		
Nd	4.40BSC		
E	5.90	6.00	6.10
E2	4.10	4.20	4.30
L	0.35	0.40	0.45
h	0.30	0.35	0.40

Figure 4-4 Recommended PCB Layout QN48 (GW1NS-4/4C)



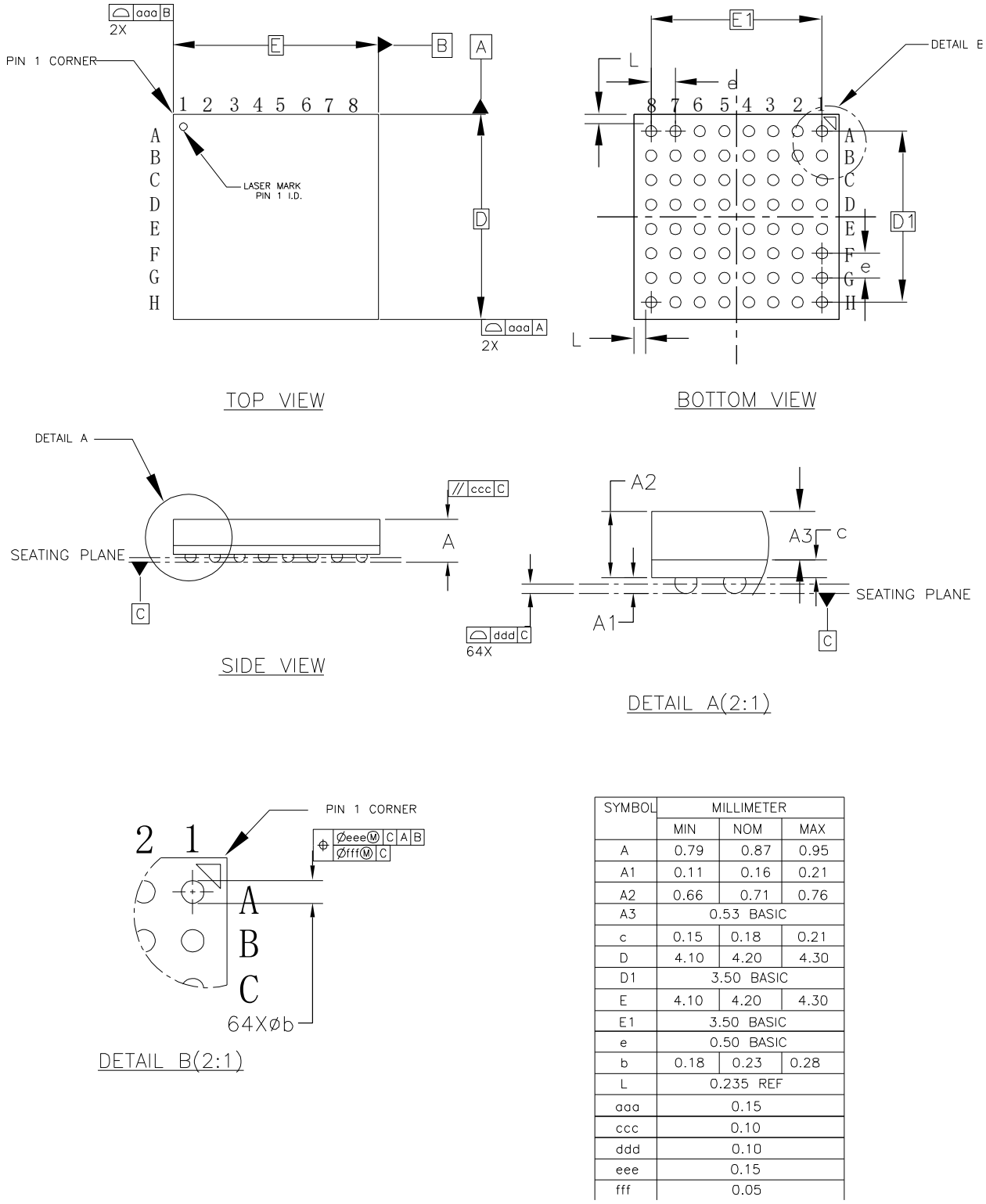


Unit:mm

D	6.00
E	6.00
D2	2.70
E2	2.70
P	5.90
e	0.40
L	0.85
b	0.20

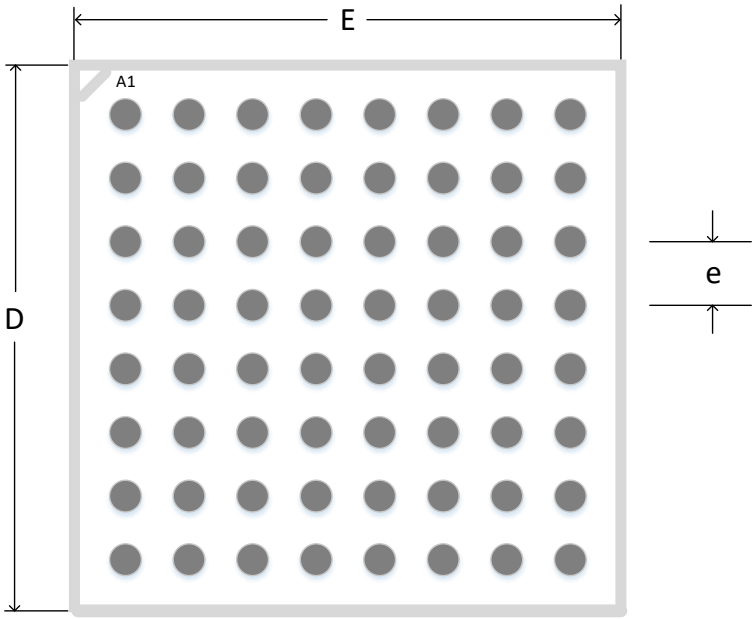
4.3 MG64 Package Outline (4.2mm x 4.2mm, GW1NS-4/4C)

Figure 4-5 Package Outline MG64 (GW1NS-4/4C)

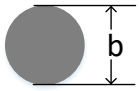


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.79	0.87	0.95
A1	0.11	0.16	0.21
A2	0.66	0.71	0.76
A3		0.53 BASIC	
c	0.15	0.18	0.21
D	4.10	4.20	4.30
D1		3.50 BASIC	
E	4.10	4.20	4.30
E1		3.50 BASIC	
e		0.50 BASIC	
b	0.18	0.23	0.28
L		0.235 REF	
aaa		0.15	
ccc		0.10	
ddd		0.10	
eee		0.15	
fff		0.05	

Figure 4-6 Recommended PCB Layout MG64 (GW1NS-4/4C)



TOP VIEW

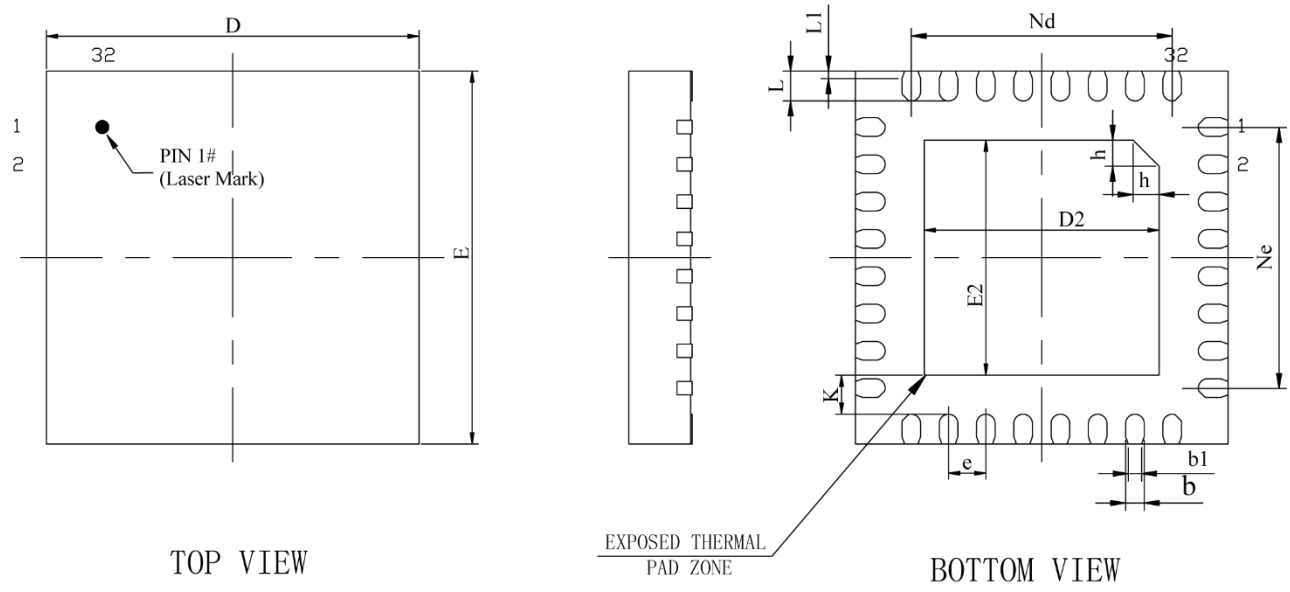


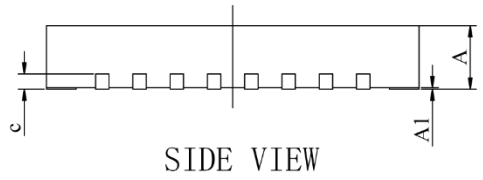
Unit:mm

D	4.20
E	4.20
e	0.50
b	0.23

4.4 QN32 Package Outline (5mm x 5mm, GW1NS-4)

Figure 4-7 Package Outline QN32 (GW1NS-4)



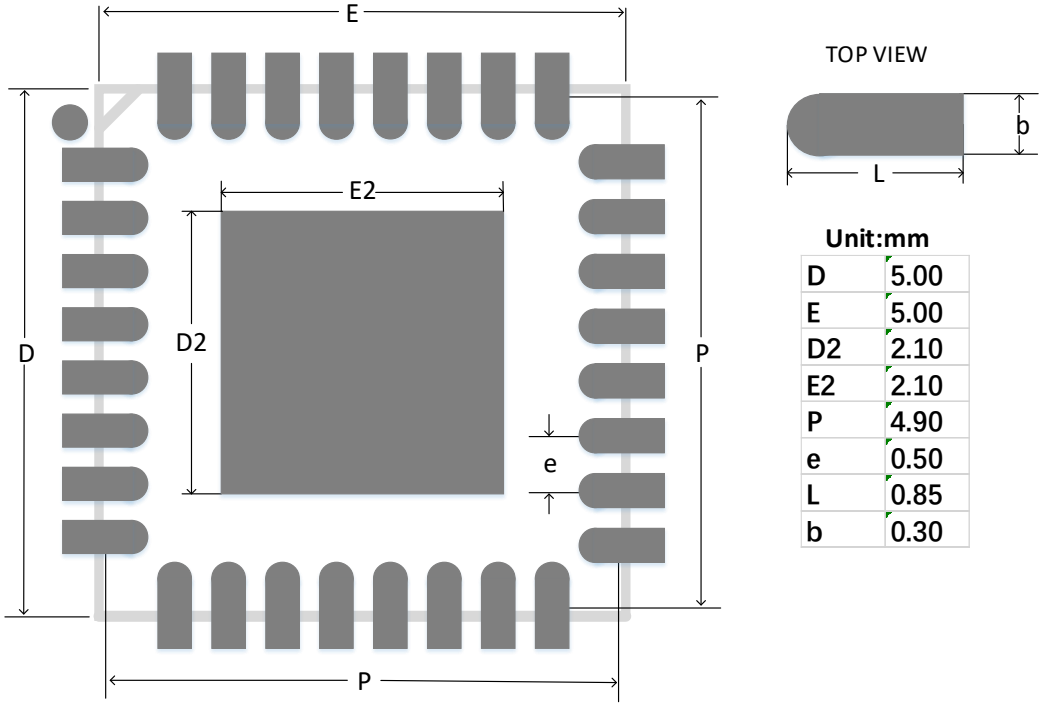


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
	0.85	0.90	0.95
	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.20	0.25	0.30
b1	0.18REF		
c	0.203REF		
D	4.90	5.00	5.10
D2	3.05	3.15	3.25
e	0.50BSC		
Nd	3.50BSC		
Ne	3.50BSC		
E	4.90	5.00	5.10
E2	3.05	3.15	3.25
L	0.35	0.40	0.45
L1	0.10REF		
h	0.30	0.35	0.40
K	0.525REF		

Note!

For GW1NS-LV4QN32, the value of A(NOM) is 0.75mm.

Figure 4-8 Recommended PCB Layout QN32 (GW1NS-4)

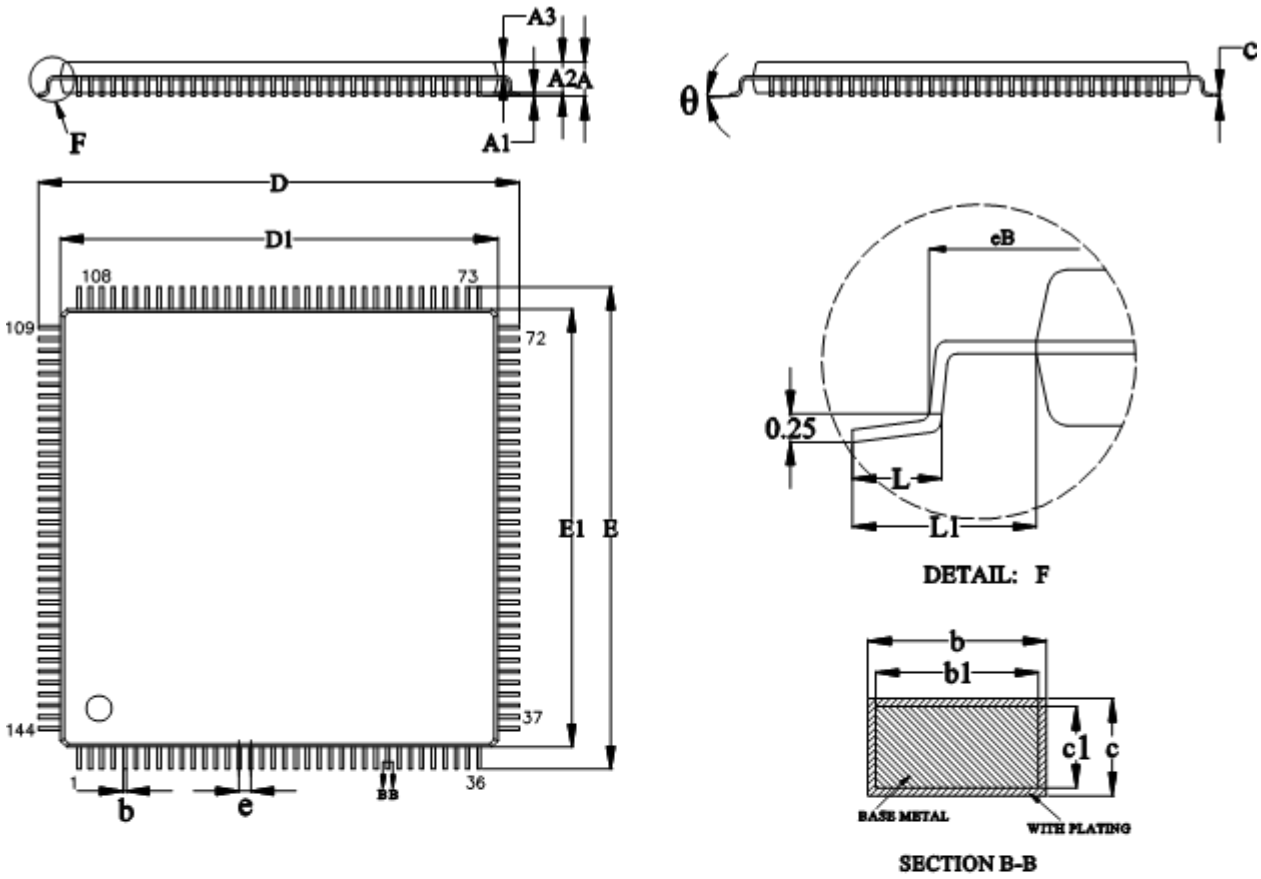


Unit:mm

D	5.00
E	5.00
D2	2.10
E2	2.10
P	4.90
e	0.50
L	0.85
b	0.30

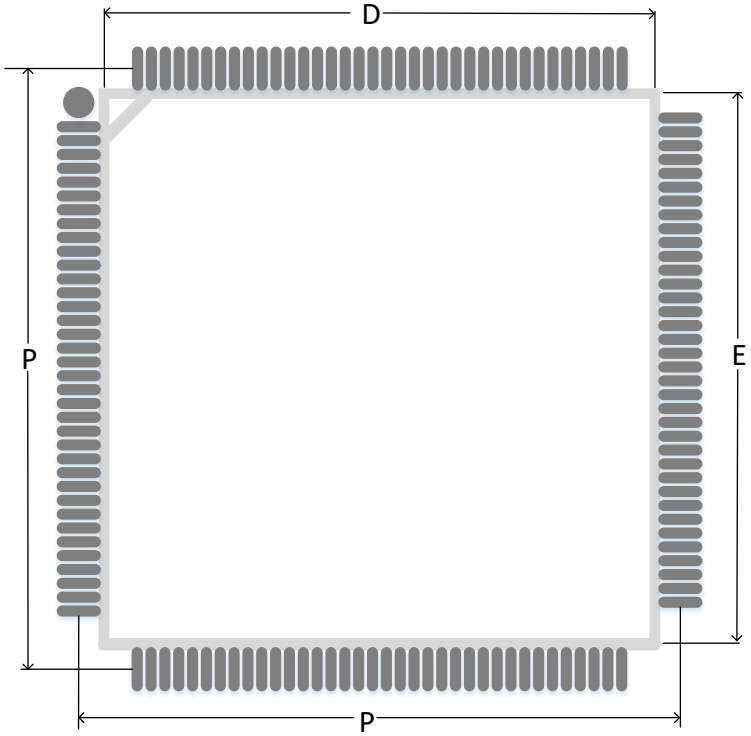
4.5 LQ144 Package Outline (20mm x 20mm, GW1NS-4C)

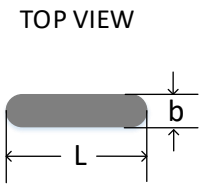
Figure 4-9 Package Outline LQ144 (GW1NS-4C)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	21.80	22.00	22.20
D1	19.90	20.00	20.10
E	21.80	22.00	22.20
E1	19.90	20.00	20.10
e	0.50BSC		
L	0.45	—	0.75
L1	1.00REF		
θ	0	—	7°

Figure 4-10 Recommended PCB Layout LQ144 (GW1NS-4C)





Unit:mm

D	20.00
E	20.00
P	21.40
e	0.50
L	1.55
b	0.30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