Date	Version	Description
09/26/2019	1.0E	Initial version published. CS49 and QN48 packages supported.
11/12/2019	1.1E	Notes added: In QN48 package, IOT7A and IOT7B share pin 10.
04/16/2020	1.1.1E	The location of pin 25 in QN48 package modified.
05/29/2020	1.1.2E	Recommended operating conditions of VCCX in QN48 added.
07/28/2020	1.2E	The info. of MG64 package added.
12/03/2021	1.3E	Pin definitions updated. The max value of VCCO power when output with MIPI updated.
08/12/2022	1.3.1E	The USB signal pins in pin definitions removed.
10/20/2022	1.3.2E	The note in Power sheet updated. The note in Pin Definitions sheet updated.
05/04/2023	1.3.3E	The description of CLKHOLD_N pin in Pin Definitions sheet updated. The note of QN48 package in Power sheet added.
06/30/2023	1.4E	QN32 package for GW1NS-4 devices added. The descriptions of pin definitions and info. for MODE0, MODE1, MODE2 pins optimized.
08/10/2023	1.4.1E	The info. of IOT7B/MODE2 pin for QN48 package in Pin List sheet updated.
08/09/2024	1.5E	The LQ144 package for GW1NS-4C devices added. The I/O descriptions of Ready and Done pins in Pin Definitions sheet optimized.
11/15/2024	1.5.1E	The description of EPAD pin in Pin Definitions sheet added.

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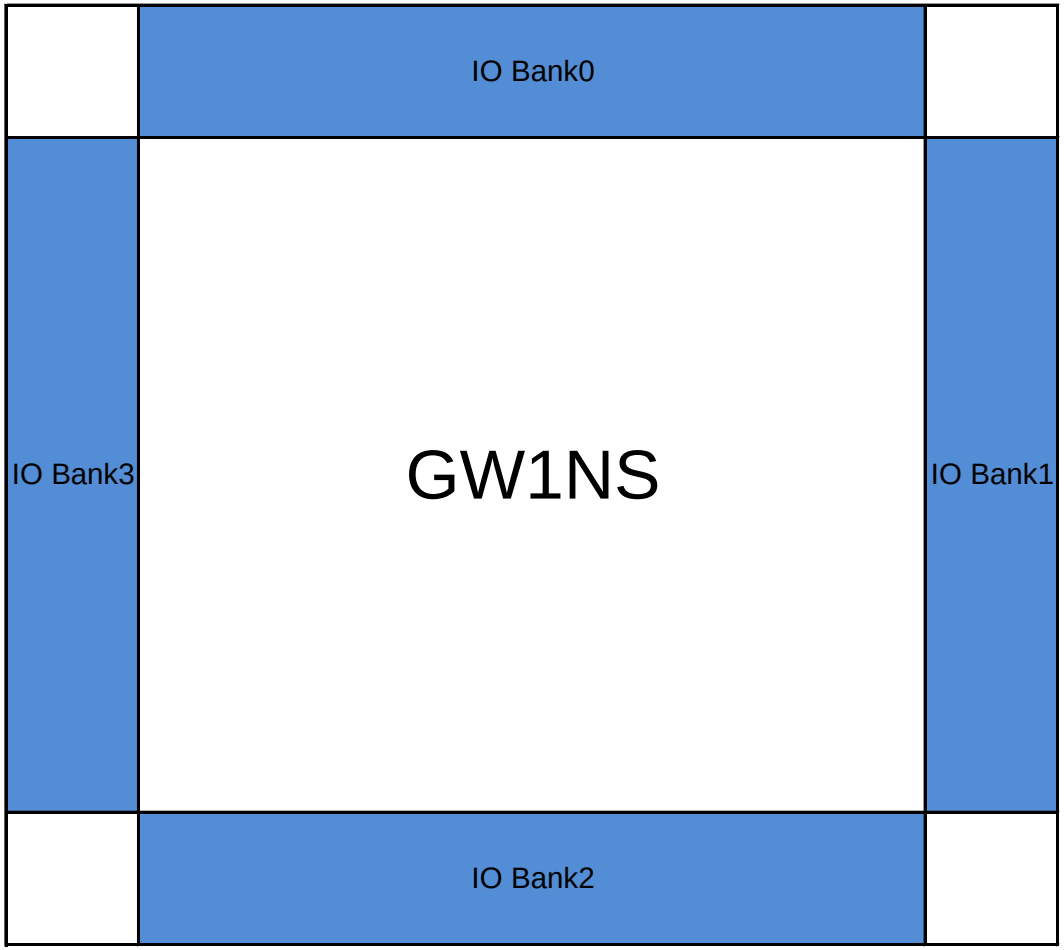
Pin Name	I/O	Description
User I/O		
IO[End][Row/Column Number][A/B]	I/O	[End] indicates the pin location, including L(left), R(right), B(bottom), and T(top).
		[Row/Column Number] indicates the pin row/column number. If [End] is T(top) or B(bottom), the pin indicates the column number of the corresponding CFU. If [End] is L(left) or R(right), the pin indicates the row number of the corresponding CFU.
		[A/B] indicates differential signal pair information.
Multi-Function Pins		
IO[End][Row/Column Number][A/B]/MMM		/MMM represents one or more of the other functions in addition to being general purpose user I/O. When these functions are not in use, these pins can be used as user I/O.
D0	I/O	Data port D0 in CPU mode
D1	I/O	Data port D1 in CPU mode
D2	I/O	Data port D2 in CPU mode
D3	I/O	Data port D3 in CPU mode
D4	I/O	Data port D4 in CPU mode
D5	I/O	Data port D5 in CPU mode
D6	I/O	Data port D6 in CPU mode
D7	I/O	Data port D7 in CPU mode
WE_N	I	Select data input/output of D[7:0] in CPU mode.0: Write;1: Read.
DOUT	O	Data output in SERIAL mode
DIN	I, internal weak pull-up	Data input in SERIAL mode
TMS	I, internal weak pull-up	Serial mode input in JTAG mode
TCK	I	Serial clock input in JTAG mode
TDO	O	Serial data output in JTAG mode
TDI	I, internal weak pull-up	Serial data input in JTAG mode
JTAGSEL_N	I, internal weak pull-up	Reconfigure JTAG download function signal
RECONFIG_N	I, internal weak pull-up	Global reset GowinCONFIG logic signal, active low
FASTRD_N	I	Access SPI FLASH to select signal. Low, Fast Read mode; High, Read mode.
DONE[1]	O, internal weak pull-up	High, the programming configuration has been completed successfully; Low, the programming configuration has not been completed or failed.
	I, internal weak pull-up	When the DONE signal is low, delay the chip to activate. Activate the chip until the DONE signal is high.
READY[1]	I/O, internal weak pull-up	High, the device can be programmed and configured currently; Low, the device cannot be programmed and configured currently.
MI	I	MI in MSPI mode
MO	O	MO in MSPI mode

Pin Name	I/O	Description
MCS_N	O	Enable signal MCS_N in MSPI mode, active-low
MCLK	O	Clock output MCLK in MSPI mode, with default frequency of 2.5Mhz
SCLK	I	Clock input in SSPI, SERIAL, and CPU modes
SO	O	SO in SSPI mode
SI	I/O	SI in SSPI mode
SSPI_CS_N	I/O	Enable signal SSPI_CS_N in SSPI mode, active-low, and internal weak pull-up
CLKHOLD_N	I, internal weak pull-up	Active-high in SSPI mode; Active-low in CPU mode.
GCLKC_[x]	I	Differential input pin of GCLKT_[x], C(Comp), [x] is global clock number[2]
GCLKT_[x]	I	Global clock input pin, T(True), [x] is global clock number
LPLL_C_fb/RPLL_C_fb	I	Left/Right PLL feedback input pin, C(Comp)
LPLL_T_fb/RPLL_T_fb	I	Left/Right PLL feedback input pin, T(True)
LPLL_C_in/RPLL_C_in	I	Left/Right PLL clock input pin, C(Comp)
LPLL_T_in/RPLL_T_in	I	Left/Right PLL clock input pin, T(True)
CH[7:0]	I	Eight-channel analog input
MODE2	I, internal weak pull-up	GowinCONFIG modes selection pin; If this pin is marked as “VCCIO”, it's internally powered; If this pin is marked as "GND", it's internally grounded.
MODE1	I, internal weak pull-up	GowinCONFIG modes selection pin; If this pin is marked as “VCCIO”, it's internally powered; If this pin is marked as "GND", it's internally grounded.
MODE0	I, internal weak pull-up	GowinCONFIG modes selection pin; If this pin is marked as “VCCIO”, it's internally powered; If this pin is marked as "GND", it's internally grounded.
Other Pins		
NC	NA	Reserved
VSS	NA	Ground
VCC	NA	Power supply pin of core voltage
VCCIO#	NA	Power supply pin of I/O voltage for I/O BANK#
VCCX	NA	Power supply pin of auxiliary voltage
VCCP	NA	Power supply pin of FLASH(1.8V)
VCCPLL	NA	Power supply pin of PLL voltage
EPAD	NA	Exposed pad. Connect to ground.

Note!

[1] The default state of READY/DONE is open-drain output, internal weak pull-up. DONE outputs 0 during configuration.

[2] When the input is single-ended, GCLKC_[x] pin is not a global clock pin.



Note!

[1] Each Bank has independent reference voltage (VREF).

[2] You can select to use IOB internal VREF (equals to 0.5 * VCCIO).

[3] You can also select to use external VREF input (use any I/O pins as external VREF input).

Note!
VCCX should be greater than or equal to VCCIO.

Recommended Operating Conditions of CS49 Package in GW1NS-4/GW1NS-4C				
Name	**Description**		**Min.**	**Max.**
VCC	Core voltage		1.14V	1.26V
VCCIO1, VCCIO2	I/O Bank voltage	When MIPI input is used in BANK1, VCCIO1 should provide 1.2V voltage.	1.14V	3.6V
		When MIPI output is used in BANK2, VCCIO2 should provide 1.2V voltage.		
VCCIO0/VCCIO3	I/O Bank voltage, VCCIO0/VCCIO3 are internally connected.		1.14V	3.6V
	When MIPI input is used in BANK0, VCCIO0 should provide 1.2V voltage.		1.14V	3.6V
VCCX	Auxiliary voltage		1.71V	3.6V

Recommended Operating Conditions of QN48 Package in GW1NS-4/GW1NS-4C				
Name	**Description**		**Min.**	**Max.**
VCC	Core voltage		1.14V	1.26V
VCCIO0, VCCIO1, VCCIO2, VCCIO3	I/O Bank voltage	When MIPI input is used in BANK0 and BANK1, VCCIO0 and VCCIO1 should provide 1.2V	1.14V	3.6V
		When MIPI output is used in BANK2, VCCIO2 should provide 1.2V voltage.		
VCCX	Auxiliary voltage		1.71V	3.6V

Note!
It is highly recommended that the EPAD connect to GND, but not a requirement.

Recommended Operating Conditions of MG64 Package in GW1NS-4/GW1NS-4C				
Name	**Description**		**Min.**	**Max.**
VCC	Core voltage		1.14V	1.26V
VCCIO0, VCCIO1, VCCIO2, VCCIO3	I/O Bank voltage	When MIPI input is used in BANK0 and BANK1, VCCIO0 and VCCIO1 should provide 1.2V	1.14V	3.6V
		When MIPI output is used in BANK2, VCCIO2 should provide 1.2V voltage.		
VCCX	Auxiliary voltage		1.71V	3.6V

Recommended Operating Conditions of QN32 Package in GW1NS-4				
Name	**Description**		**Min.**	**Max.**
VCC	Core voltage		1.14V	1.26V
VCCIO0, VCCIO1, VCCIO2, VCCIO3	I/O Bank voltage	When MIPI input is used in BANK0 and BANK1, VCCIO0 and VCCIO1 should provide 1.2V	1.14V	3.6V
		When MIPI output is used in BANK2, VCCIO2 should provide 1.2V voltage.		
VCCX	Auxiliary voltage		1.71V	3.6V

Note!
It is highly recommended that the EPAD connect to GND, but not a requirement.

Recommended Operating Conditions of LQ144 Package in GW1NS-4C			
Name	**Description**	**Min.**	**Max.**
VCC	Core voltage	1.14V	1.26V
VCCIO0, VCCIO1	I/O Bank voltage When MIPI input is used in BANK0 and BANK1, VCCIO0 and VCCIO1 should provide 1.2V voltage.	1.14V	3.6V
VCCIO2/VCCIO3/ VCCX	I/O Bank voltage VCCIO2/VCCIO3 and auxiliary voltage VCCX are internally connected. When MIPI output is used in BANK2, VCCIO2 should provide 1.2V voltage.	1.71V	3.6V

Note!

[1] IOT7A and IOT7B share pin 10 in package QN48.

[2] QN32 package is for GW1NS-4 devices.

[3] The pin is internally grounded.

[4] LQ144 package is for GW1NS-4C devices.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	CS49	QN48[1]	MG64	QN32[2]	LQ144[4]
IOB13A	I/O	3		True_of_IOB13B	NONE	NONE		18			118
IOB13B	I/O	3		Comp_of_IOB13A	NONE	NONE		19			119
IOB14A	I/O	3		True_of_IOB14B	NONE	NONE					120
IOB14B	I/O	3		Comp_of_IOB14A	NONE	NONE					121
IOB15A	I/O	3		True_of_IOB15B	NONE	NONE					128
IOB15B	I/O	3		Comp_of_IOB15A	NONE	NONE					129
IOB16A/GCLKT_5	I/O	3	GCLKT_5	True_of_IOB16B	NONE	NONE		20		10	130
IOB16B/GCLKC_5	I/O	3	GCLKC_5	Comp_of_IOB16A	NONE	NONE		21		11	131
IOB22A/GCLKT_4	I/O	3	GCLKT_4	True_of_IOB22B	NONE	NONE		22			134
IOB22B/GCLKC_4	I/O	3	GCLKC_4	Comp_of_IOB22A	NONE	NONE		23			135
IOB23A	I/O	3		True_of_IOB23B	NONE	NONE					136
IOB23B	I/O	3		Comp_of_IOB23A	NONE	NONE					137
IOB24A	I/O	3		True_of_IOB24B	NONE	NONE					138
IOB24B	I/O	3		Comp_of_IOB24A	NONE	NONE					139
IOB25A	I/O	3		True_of_IOB25B	NONE	NONE					140
IOB25B	I/O	3		Comp_of_IOB25A	NONE	NONE					141
IOB29A	I/O	3		True_of_IOB29B	NONE	NONE					142
IOB29B	I/O	3		Comp_of_IOB29A	NONE	NONE					143
IOB4A	I/O	3		True_of_IOB4B	NONE	NONE		13			110
IOB4B	I/O	3		Comp_of_IOB4A	NONE	NONE		14			111
IOB5A	I/O	3		True_of_IOB5B	NONE	NONE		15		8	112
IOB5B	I/O	3		Comp_of_IOB5A	NONE	NONE				9	113
IOB6A	I/O	3		True_of_IOB6B	NONE	NONE		16			114
IOB6B	I/O	3		Comp_of_IOB6A	NONE	NONE		17			115
IOB7A	I/O	3		True_of_IOB7B	NONE	NONE					116
IOB7B	I/O	3		Comp_of_IOB7A	NONE	NONE					117

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Note!

[1] IOT7A and IOT7B share pin 10 in package QN48.

[2] QN32 package is for GW1NS-4 devices.

[3] The pin is internally grounded.

[4] LQ144 package is for GW1NS-4C devices.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	CS49	QN48[1]	MG64	QN32[2]	LQ144[4]
IOR11A/GCLKT_3	I/O	2	GCLKT_3	True_of_IOR11B	TRUE	x16	G4	32	G5	13	18
IOR11B/GCLKC_3	I/O	2	GCLKC_3	Comp_of_IOR11A	TRUE	NONE	F4	31	H5	14	16
IOR12A	I/O	2		True_of_IOR12B	NONE	NONE					15
IOR12B	I/O	2		Comp_of_IOR12A	NONE	NONE					14
IOR13A	I/O	2		True_of_IOR13B	TRUE	x16	G5		G6		13
IOR13B	I/O	2		Comp_of_IOR13A	TRUE	NONE	F5		H6		12
IOR14A	I/O	2		True_of_IOR14B	NONE	NONE					11
IOR14B	I/O	2		Comp_of_IOR14A	NONE	NONE					10
IOR15A	I/O	2		True_of_IOR15B	TRUE	x16	G6	30	G7		9
IOR15B	I/O	2		Comp_of_IOR15A	TRUE	NONE	F6	29	H7		
IOR16A	I/O	2		True_of_IOR16B	NONE	NONE					7
IOR16B	I/O	2		Comp_of_IOR16A	NONE	NONE					6
IOR17A	I/O	2		True_of_IOR17B	TRUE	x16	G7	28	G8		
IOR17B	I/O	2		Comp_of_IOR17A	TRUE	NONE	F7	27	H8		
IOR18A	I/O	2		True_of_IOR18B	NONE	NONE				17	
IOR18B	I/O	2		Comp_of_IOR18A	NONE	NONE				16	
IOR2A/RPLL_T_in	I/O	2	RPLL_T_in	True_of_IOR2B	TRUE	x16	E1	35	G1		34
IOR2B/RPLL_C_in	I/O	2	RPLL_C_in	Comp_of_IOR2A	TRUE	NONE	E2	34	H1		33
IOR3A/RPLL_T_fb	I/O	2	RPLL_T_fb	True_of_IOR3B	NONE	NONE					30
IOR3B/RPLL_C_fb	I/O	2	RPLL_C_fb	Comp_of_IOR3A	NONE	NONE					32
IOR4A	I/O	2		True_of_IOR4B	TRUE	x16	G1		G2		
IOR4B	I/O	2		Comp_of_IOR4A	TRUE	NONE	F1		H2	20	
IOR5A	I/O	2		True_of_IOR5B	NONE	NONE					28
IOR5B	I/O	2		Comp_of_IOR5A	NONE	NONE					29
IOR6A	I/O	2		True_of_IOR6B	TRUE	x16	G2		G3		27
IOR6B	I/O	2		Comp_of_IOR6A	TRUE	NONE	F2		H3		26

Note!

[1] IOT7A and IOT7B share pin 10 in package QN48.

[2] QN32 package is for GW1NS-4 devices.

[3] The pin is internally grounded.

[4] LQ144 package is for GW1NS-4C devices.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	CS49	QN48[1]	MG64	QN32[2]	LQ144[4]
IOR7A	I/O	2		True_of_IOR7B	NONE	NONE					25
IOR7B	I/O	2		Comp_of_IOR7A	NONE	NONE					24
IOR8A	I/O	2		True_of_IOR8B	TRUE	x16	G3		G4		23
IOR8B	I/O	2		Comp_of_IOR8A	TRUE	NONE	F3		H4		22
IOR9A/GCLKT_2	I/O	2	GCLKT_2	True_of_IOR9B	NONE	NONE			F5		21
IOR9B/GCLKC_2	I/O	2	GCLKC_2	Comp_of_IOR9A	NONE	NONE		33	F4	12	20
IOT10A/MCLK/D4	I/O	0	MCLK/D4	True_of_IOT10B	NONE	NONE		1		27	56
IOT10B/MCS_N/D5	I/O	0	MCS_N/D5	Comp_of_IOT10A	NONE	NONE		2		26	54
IOT11A/MO/D6	I/O	1	MO/D6	True_of_IOT11B	NONE	x16	A7	48	A1	25	52
IOT11B/MI/D7	I/O	1	MI/D7	Comp_of_IOT11A	NONE	NONE	B7	47	B1	21	51
IOT12A/DIN/CLKHOLD_N	I/O	1	DIN/CLKHOLD_N	True_of_IOT12B	NONE	NONE			A2		50
IOT12B/DOUT/WE_N	I/O	1	DOUT/WE_N	Comp_of_IOT12A	NONE	NONE			B2		49
IOT13A/LPLL_T_in	I/O	1	LPLL_T_in	True_of_IOT13B	NONE	x16	B6	45	B3		46
IOT13B/LPLL_C_in	I/O	1	LPLL_C_in	Comp_of_IOT13A	NONE	NONE	A6	46	A3		45
IOT15A/LPLL_T_fb	I/O	1	LPLL_T_fb	True_of_IOT15B	NONE	x16	B5		B4		44
IOT15B/LPLL_C_fb	I/O	1	LPLL_C_fb	Comp_of_IOT15A	NONE	NONE	A5		A4		43
IOT17A/GCLKT_0	I/O	1	GCLKT_0	True_of_IOT17B	NONE	x16	B4	43	B5	23	42
IOT17B/GCLKC_0	I/O	1	GCLKC_0	Comp_of_IOT17A	NONE	NONE	A4	44	A5	22	41
IOT20A/GCLKT_1	I/O	1	GCLKT_1	True_of_IOT20B	NONE	x16	B3	41	C5		40
IOT20B/GCLKC_1	I/O	1	GCLKC_1	Comp_of_IOT20A	NONE	NONE	A3	42	C4		39
IOT21A	I/O	1		True_of_IOT21B	NONE	NONE			B6		38
IOT21B	I/O	1		Comp_of_IOT21A	NONE	NONE			A6		
IOT22A	I/O	1		True_of_IOT22B	NONE	x16	B2		B7		
IOT22B	I/O	1		Comp_of_IOT22A	NONE	NONE	A2		A7		
IOT24A	I/O	1		True_of_IOT24B	NONE	x16			A8		
IOT24B	I/O	1		Comp_of_IOT24A	NONE	NONE			B8		

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Note!

[1] IOT7A and IOT7B share pin 10 in package QN48.

[2] QN32 package is for GW1NS-4 devices.

[3] The pin is internally grounded.

[4] LQ144 package is for GW1NS-4C devices.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	CS49	QN48[1]	MG64	QN32[2]	LQ144[4]
IOT26A	I/O	1		True_of_IOT26B	NONE	x16	D2	39	C7		
IOT26B	I/O	1		Comp_of_IOT26A	NONE	NONE	C2	40	C8		
IOT29A	I/O	1		True_of_IOT29B	NONE	x16			E6		
IOT29B	I/O	1		Comp_of_IOT29A	NONE	NONE			D6		
IOT2A/TDI	I/O	0	TDI	True_of_IOT2B	NONE	x16	E7	3	E2	1	72
IOT2B/TDO	I/O	0	TDO	Comp_of_IOT2A	NONE	NONE	E6	4	E3	32	71
IOT31A	I/O	1		True_of_IOT31B	NONE	x16	B1		D7		
IOT31B	I/O	1		Comp_of_IOT31A	NONE	NONE	A1		D8		
IOT33A	I/O	1		True_of_IOT33B	NONE	x16			E7		
IOT33B	I/O	1		Comp_of_IOT33A	NONE	NONE			E8		
IOT35A	I/O	1		True_of_IOT35B	NONE	x16	D1		F7		
IOT35B	I/O	1		Comp_of_IOT35A	NONE	NONE	C1		F8		
IOT3A/TMS	I/O	0	TMS	True_of_IOT3B	NONE	NONE	E5	6	D2	4	70
IOT3B/TCK	I/O	0	TCK	Comp_of_IOT3A	NONE	NONE	E4	7	D3	5	69
IOT4A/SCLK	I/O	0	SCLK	True_of_IOT4B	NONE	x16	C6		F1		67
IOT4B/JTAGSEL_N	I/O	0	JTAGSEL_N	Comp_of_IOT4A	NONE	NONE		8	F2		68
IOT5A/READY	I/O	0	READY	True_of_IOT5B	NONE	NONE	D6		D1		66
IOT5B/DONE	I/O	0	DONE	Comp_of_IOT5A	NONE	NONE		9		30	65
IOT6A/RECONFIG_N	I/O	0	RECONFIG_N	True_of_IOT6B	NONE	x16			E1	29	64
IOT6B/MODE0	I/O	0	MODE0	Comp_of_IOT6A	NONE	NONE	GND[3]	GND[3]	GND[3]	GND[3]	63
IOT7A/MODE1	I/O	0	MODE1	True_of_IOT7B	NONE	NONE	GND[3]	10	GND[3]	28	62
IOT7B/MODE2	I/O	0	MODE2	Comp_of_IOT7A	NONE	NONE	GND[3]	10	GND[3]	GND[3]	61
IOT8A/SSPI_CS_N/D0	I/O	0	SSPI_CS_N/D0	True_of_IOT8B	NONE	x16	C7		C1		60
IOT8B/SO/D1	I/O	0	SO/D1	Comp_of_IOT8A	NONE	NONE	D7		C2		59
IOT9A/SI/D2	I/O	0	SI/D2	True_of_IOT9B	NONE	NONE					58

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Note!

[1] IOT7A and IOT7B share pin 10 in package QN48.

[2] QN32 package is for GW1NS-4 devices.

[3] The pin is internally grounded.

[4] LQ144 package is for GW1NS-4C devices.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	CS49	QN48[1]	MG64	QN32[2]	LQ144[4]
IOT9B/FASTRD_N/D3	I/O	0	FASTRD_N/D3	Comp_of_IOT9A	NONE	NONE					57
VCC	Power	N/A					D5	11	D5	2	48
VCC	Power	N/A						37		18	36
VCC	Power	N/A								6	108
VCC	Power	N/A									104
VCC	Power	N/A									132
VCCIO0	Power	N/A						5	C3	31	77
VCCIO0/VCCIO3	Power	N/A					C5				
VCCIO1	Power	N/A									37
VCCIO1	Power	N/A					C3	38	C6	24	55
VCCIO2	Power	N/A					E3			19	
VCCIO2	Power	N/A						36	F6		
VCCIO3	Power	N/A						12	F3	15	
VCCIO3	Power	N/A						24			
VCCIO2/VCCIO3/VCCX	Power	N/A									47
VCCIO2/VCCIO3/VCCX	Power	N/A									19
VCCIO2/VCCIO3/VCCX	Power	N/A									5
VCCIO2/VCCIO3/VCCX	Power	N/A									127
VCCIO2/VCCIO3/VCCX	Power	N/A									35
VCCIO2/VCCIO3/VCCX	Power	N/A									91
VCCIO2/VCCIO3/VCCX	Power	N/A									109
VCCX	Power	N/A					D3	25	E4	7	
VSS	Ground	N/A					C4		D4	3	2
VSS	Ground	N/A					D4	26	E5		17
VSS	Ground	N/A									53
VSS	Ground	N/A									133

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Note!

[1] IOT7A and IOT7B share pin 10 in package QN48.

[2] QN32 package is for GW1NS-4 devices.

[3] The pin is internally grounded.

[4] LQ144 package is for GW1NS-4C devices.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	CS49	QN48[1]	MG64	QN32[2]	LQ144[4]
VSS	Ground	N/A									144
VSS	Ground	N/A									74
VSS	Ground	N/A									75
VSS	Ground	N/A									76
VSS	Ground	N/A									78
VSS	Ground	N/A									79
VSS	Ground	N/A									80
VSS	Ground	N/A									82
VSS	Ground	N/A									83
VSS	Ground	N/A									84
VSS	Ground	N/A									85
VSS	Ground	N/A									86
VSS	Ground	N/A									87
VSS	Ground	N/A									88
VSS	Ground	N/A									89
VSS	Ground	N/A									92
VSS	Ground	N/A									93
VSS	Ground	N/A									94
VSS	Ground	N/A									95
VSS	Ground	N/A									96
VSS	Ground	N/A									97
VSS	Ground	N/A									98
VSS	Ground	N/A									99
VSS	Ground	N/A									100
VSS	Ground	N/A									105
VSS	Ground	N/A									106

Note!

[1] IOT7A and IOT7B share pin 10 in package QN48.

[2] QN32 package is for GW1NS-4 devices.

[3] The pin is internally grounded.

[4] LQ144 package is for GW1NS-4C devices.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	CS49	QN48[1]	MG64	QN32[2]	LQ144[4]
VSS	Ground	N/A									107
VSS	Ground	N/A									122
VSS	Ground	N/A									123
VSS	Ground	N/A									124
VSS	Ground	N/A									125
VSS	Ground	N/A									126
NC	N/A	N/A									1
NC	N/A	N/A									3
NC	N/A	N/A									4
NC	N/A	N/A									8
NC	N/A	N/A									31
NC	N/A	N/A									73
NC	N/A	N/A									81
NC	N/A	N/A									90
NC	N/A	N/A									101
NC	N/A	N/A									102
NC	N/A	N/A									103

Note!
[1] QN32 package is for GW1NS-4 devices.
[2] LQ144 package is for GW1NS-4C devices.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	CS49	QN48	MG64	QN32[1]	LQ144[2]
BANK2 True LVDS Pair											
IOR11A/GCLKT_3	I/O	2	GCLKT_3	True_of_IOR11B	TRUE	x16	G4	32	G5	13	18
IOR11B/GCLKC_3	I/O	2	GCLKC_3	Comp_of_IOR11A	TRUE	NONE	F4	31	H5	14	16
IOR13A	I/O	2		True_of_IOR13B	TRUE	x16	G5		G6		13
IOR13B	I/O	2		Comp_of_IOR13A	TRUE	NONE	F5		H6		12
IOR15A	I/O	2		True_of_IOR15B	TRUE	x16	G6	30	G7		9
IOR15B	I/O	2		Comp_of_IOR15A	TRUE	NONE	F6	29	H7		
IOR17A	I/O	2		True_of_IOR17B	TRUE	x16	G7	28	G8		
IOR17B	I/O	2		Comp_of_IOR17A	TRUE	NONE	F7	27	H8		
IOR2A/RPLL_T_in	I/O	2	RPLL_T_in	True_of_IOR2B	TRUE	x16	E1	35	G1		34
IOR2B/RPLL_C_in	I/O	2	RPLL_C_in	Comp_of_IOR2A	TRUE	NONE	E2	34	H1		33
IOR4A	I/O	2		True_of_IOR4B	TRUE	x16	G1		G2		
IOR4B	I/O	2		Comp_of_IOR4A	TRUE	NONE	F1		H2	20	
IOR6A	I/O	2		True_of_IOR6B	TRUE	x16	G2		G3		27
IOR6B	I/O	2		Comp_of_IOR6A	TRUE	NONE	F2		H3		26
IOR8A	I/O	2		True_of_IOR8B	TRUE	x16	G3		G4		23
IOR8B	I/O	2		Comp_of_IOR8A	TRUE	NONE	F3		H4		22

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