Date	Version	Description
08/24/2018	1.0E	Initial version published.
11/16/2018	1.1E	Recommended operating conditions added.
03/24/2020	1.2E	The descriptions of pin MODE0/MODE1/MODE2 updated.
09/16/2020	1.2.1E	The info. of Power updated.
07/16/2021	1.2.2E	The info. of pins related to Power updated.
08/12/2021	1.2.3E	The info. of VBUSPAD power removed.
12/03/2021	1.3E	Pin definitions updated. The max value of VCCO power when output with MIPI updated.

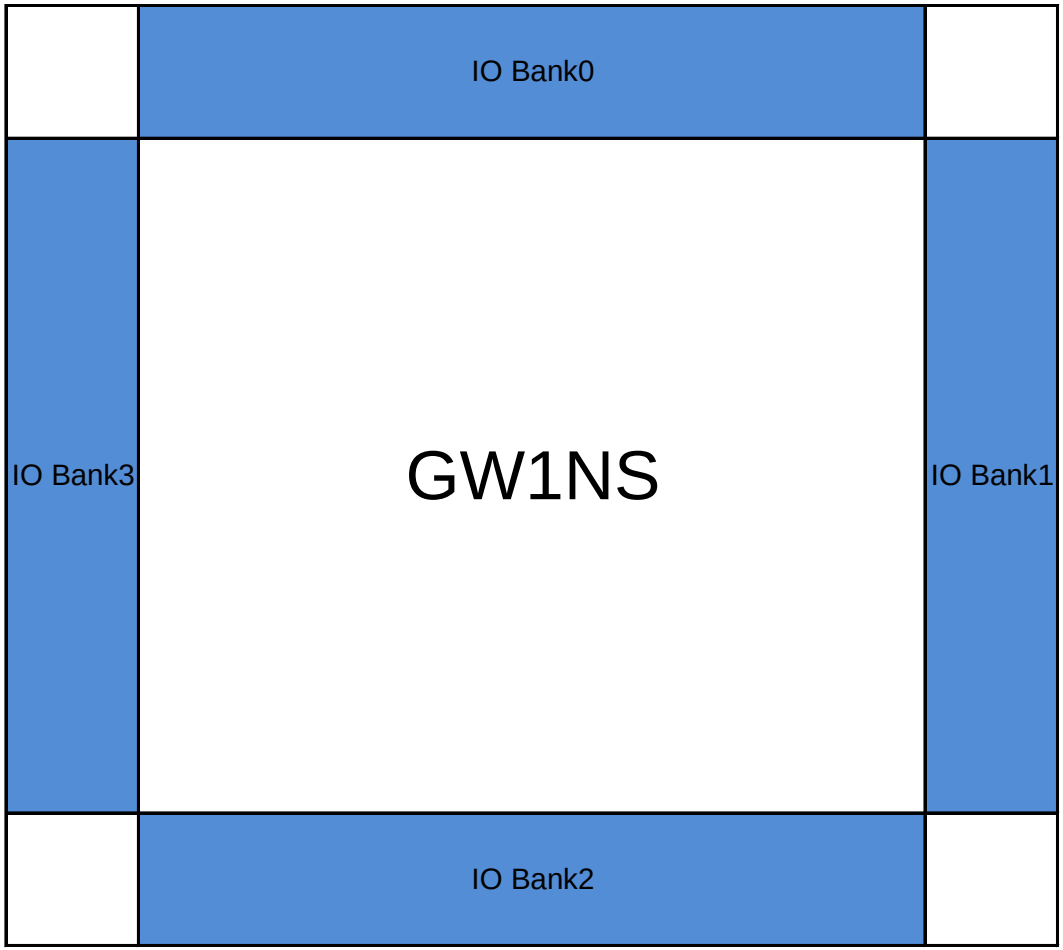
Pin Name	I/O	Description
User I/O		
IO[End][Row/Column Number][A/B]	I/O	[End] indicates the pin location, including L(left), R(right), B(bottom), and T(top).
		[Row/Column Number] indicates the pin row/column number. If [End] is T(top) or B(bottom), the pin indicates the column number of the corresponding CFU. If [End] is L(left) or R(right), the pin indicates the row number of the corresponding CFU.
		[A/B] indicates differential signal pair information.
Multi-Function Pins		
IO[End][Row/Column Number][A/B]/MMM		/MMM represents one or more of the other functions in addition to being general purpose user I/O. When these functions are not in use, these pins can be used as user I/O.
D0	I/O	Data port D0 in CPU mode
D1	I/O	Data port D1 in CPU mode
D2	I/O	Data port D2 in CPU mode
D3	I/O	Data port D3 in CPU mode
D4	I/O	Data port D4 in CPU mode
D5	I/O	Data port D5 in CPU mode
D6	I/O	Data port D6 in CPU mode
D7	I/O	Data port D7 in CPU mode
WE_N	I	Select data input/output of D[7:0] in CPU mode.0: Write;1: Read.
DOUT	O	Data output in SERIAL mode
DIN	I, internal weak pull-up	Data input in SERIAL mode
TMS	I, internal weak pull-up	Serial mode input in JTAG mode
TCK	I	Serial clock input in JTAG mode
TDO	O	Serial data output in JTAG mode
TDI	I, internal weak pull-up	Serial data input in JTAG mode
JTAGSEL_N	I, internal weak pull-up	Reconfigure JTAG download function signal
RECONFIG_N	I	Global reset GowinCONFIG logic signal, active low
FASTRD_N	I	Access SPI FLASH to select signal. Low, Fast Read mode; High, Read mode.
DONE[1]	O	High, the programming configuration has been completed successfully; Low, the programming configuration has not been completed or failed.
	I	When the DONE signal is low, delay the chip to activate. Activate the chip until the DONE signal is high.
READY[1]	I/O	High, the device can be programmed and configured currently; Low, the device cannot be programmed and configured currently.
MI	O	MI in MSPI mode

Pin Name	I/O	Description
MO	I	MO in MSPI mode
MCS_N	O	Enable signal MCS_N in MSPI mode, active-low
MCLK	O	Clock output MCLK in MSPI mode, with default frequency of 2.5Mhz
SCLK	I	Clock input in SSPI, SERIAL, and CPU modes
SO	O	SO in SSPI mode
SI	I/O	SI in SSPI mode
SSPI_CS_N	I/O	Enable signal SSPI_CS_N in SSPI mode, active-low, and internal weak pull-up
CLKHOLD_N	I, internal weak pull-up	High, the operation is efficient in SSPI mode or CPU mode; Low, the operation is inefficient in SSPI mode or CPU mode.
GCLKC_[x]	I	Differential input pin of GCLKT_[x], C(Comp), [x]: global clock No.[2]
GCLKT_[x]	I	Global clock input pin, T(True), [x]: global clock No.
LPLL_C_fb/RPLL_C_fb	I	Left/Right PLL feedback input pin, C(Comp)
LPLL_T_fb/RPLL_T_fb	I	Left/Right PLL feedback input pin, T(True)
LPLL_C_in/RPLL_C_in	I	Left/Right PLL clock input pin, C(Comp)
LPLL_T_in/RPLL_T_in	I	Left/Right PLL clock input pin, T(True)
CH[7:0]	I	Eight-channel analog input
MODE2	I, internal weak pull-up	Selection signal port in GowinCONFIG mode If this pin is not bonded, it's internally grounded.
MODE1	I, internal weak pull-up	Selection signal port in GowinCONFIG mode If this pin is not bonded, it's internally grounded.
MODE0	I, internal weak pull-up	Selection signal port in GowinCONFIG mode If this pin is not bonded, it's internally grounded.
Other Pins		
NC	NA	Reserved
VSS	NA	Ground
VCC	NA	Power supply pin of core voltage
VCCO#	NA	Power supply pin of I/O voltage for I/O BANK#
VCCX	NA	Power supply pin of auxiliary voltage
VCCP	NA	Power supply pin of FLASH(1.8V)
VCCPLL	NA	Power supply pin of PLL voltage
USB signal pin		
DM	NA	USB data pin Data-
DP	NA	USB data pin Data+

Pin Name	I/O	Description
REXT	NA	12.7K high-accuracy resistance
XIN	NA	Crystal oscillator input signal
XOUT	NA	Crystal oscillator output signal
IDPAD	NA	ID signal
VBUSPAD	NA	VBUS signal
VDDA	NA	ADC analog power supply voltage, VDDA=3.3V
VDDAUSB	NA	Analog power supply pin (3.3V)
VDDDUSB	NA	Analog power supply pin (3.3V)
VDDPL	NA	Power supply pin of HS driver (1.2V)
X16	NA	IO supports 16:1 function
VREF	NA	ADC external reference voltage input pin

Note!
[1] Ready and Done can not be driven to low before and during configuration.
[2] When the input is single-ended, GCLKC_[x] pin is not a global clock pin.

Bank



Note!

[1] Each Bank has independent reference voltage (VREF);

[2] You can select to use IOB internal VREF (equals to 0.5 X VCCO);

[3] You can also select to use external VREF input (use any I/O pins as external VREF input).

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	QN32	QN32U	CS36	QN48	LQ144
IOB10A/GCLKT_5	I/O	2	GCLKT_5	True_of_IOB10B	NONE	NONE				17	44
IOB10B/GCLKC_5	I/O	2	GCLKC_5	Comp_of_IOB10A	NONE	NONE				18	45
IOB11A/GCLKT_4	I/O	2	GCLKT_4	True_of_IOB11B	TRUE	x16	4	4	F4	19	46
IOB11B/GCLKC_4	I/O	2	GCLKC_4	Comp_of_IOB11A	TRUE	NONE	5	5	E4	20	47
IOB12A	I/O	2		True_of_IOB12B	NONE	NONE					54
IOB12B	I/O	2		Comp_of_IOB12A	NONE	NONE					58
IOB13A	I/O	2		True_of_IOB13B	TRUE	x16				21	59
IOB13B	I/O	2		Comp_of_IOB13A	TRUE	NONE				22	60
IOB14A	I/O	2		True_of_IOB14B	NONE	NONE					61
IOB14B	I/O	2		Comp_of_IOB14A	NONE	NONE					62
IOB15A	I/O	2		True_of_IOB15B	TRUE	x16	7		F3	23	63
IOB15B	I/O	2		Comp_of_IOB15A	TRUE	NONE			E3	24	64
IOB16A	I/O	2		True_of_IOB16B	NONE	NONE					65
IOB16B	I/O	2		Comp_of_IOB16A	NONE	NONE					66
IOB17A	I/O	2		True_of_IOB17B	TRUE	x16			F2		67
IOB17B	I/O	2		Comp_of_IOB17A	TRUE	NONE			E2		68
IOB18A	I/O	2		True_of_IOB18B	NONE	NONE					69
IOB18B	I/O	2		Comp_of_IOB18A	NONE	NONE					70
IOB19A	I/O	2		True_of_IOB19B	NONE	NONE					71
IOB19B	I/O	2		Comp_of_IOB19A	NONE	NONE					72
IOB7A	I/O	2		True_of_IOB7B	TRUE	x16			F6		38
IOB7B	I/O	2		Comp_of_IOB7A	TRUE	NONE			E6	14	39
IOB8A	I/O	2		True_of_IOB8B	NONE	NONE					40
IOB8B	I/O	2		Comp_of_IOB8A	NONE	NONE					41
IOB9A	I/O	2		True_of_IOB9B	TRUE	x16			F5	15	42
IOB9B	I/O	2		Comp_of_IOB9A	TRUE	NONE			E5	16	43
IOL2A/JTAGSEL_N/VREF	I/O	3	JTAGSEL_N/VREF	True_of_IOL2B	TRUE	NONE			B6	3	3
IOL2B	I/O	3		Comp_of_IOL2A	TRUE	NONE					4
IOL3A	I/O	3		True_of_IOL3B	NONE	NONE					
IOL3B	I/O	3		Comp_of_IOL3A	NONE	NONE					7
IOL4A	I/O	3		True_of_IOL4B	TRUE	NONE					8
IOL4B	I/O	3		Comp_of_IOL4A	TRUE	NONE					9

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	QN32	QN32U	CS36	QN48	LQ144
IOL5A/GCLKT_7	I/O	3	GCLKT_7	True_of_IOL5B	NONE	NONE					11
IOL5B/GCLKC_7	I/O	3	GCLKC_7	Comp_of_IOL5A	NONE	NONE					12
IOL6A/TMS	I/O	3	TMS	True_of_IOL6B	NONE	NONE	24	24	C5	4	13
IOL6B/TCK	I/O	3	TCK	Comp_of_IOL6A	NONE	NONE	25	25	C6	5	14
IOL6C/SCLK	I/O	3	SCLK	True_of_IOL6D	NONE	NONE	26	26			15
IOL6D/TDI	I/O	3	TDI	Comp_of_IOL6C	NONE	NONE	27	27	D5	6	16
IOL6E/TDO	I/O	3	TDO	True_of_IOL6F	NONE	NONE	28	28	D6	7	18
IOL6F/RECONFIG_N	I/O	3	RECONFIG_N	Comp_of_IOL6E	NONE	NONE					20
IOL6G/DONE	I/O	3	DONE	True_of_IOL6H	NONE	NONE				9	21
IOL6H/READY	I/O	3	READY	Comp_of_IOL6G	NONE	NONE					22
IOL6I	I/O	3		True_of_IOL6J	NONE	NONE					23
IOL6J	I/O	3		Comp_of_IOL6I	NONE	NONE					24
IOL7A/GCLKT_6	I/O	3	GCLKT_6	True_of_IOL7B	TRUE	NONE	29	29		10	25
IOL7B/GCLKC_6	I/O	3	GCLKC_6	Comp_of_IOL7A	TRUE	NONE	30	30		11	27
IOL8A	I/O	3		True_of_IOL8B	NONE	NONE	32				
IOL8B	I/O	3		Comp_of_IOL8A	NONE	NONE	1	32			28
IOL9A	I/O	3		True_of_IOL9B	NONE	NONE		1			29
IOL9B	I/O	3		Comp_of_IOL9A	NONE	NONE					30
IOR2A/RPLL_T_fb	I/O	1	RPLL_T_fb	True_of_IOR2B	TRUE	NONE	17				106
IOR2B/RPLL_C_fb	I/O	1	RPLL_C_fb	Comp_of_IOR2A	TRUE	NONE	16				104
IOR3A/GCLKT_2/RPLL_T_in	I/O	1	GCLKT_2/RPLL_T_in	True_of_IOR3B	NONE	NONE	13	16	D1	35	101
IOR3B/GCLKC_2/RPLL_C_in	I/O	1	GCLKC_2/RPLL_C_in	Comp_of_IOR3A	NONE	NONE	14	17	E1		102
IOR4A/MI/D7	I/O	1	MI/D7	True_of_IOR4B	TRUE	NONE				33	99
IOR4B/MO/D6	I/O	1	MO/D6	Comp_of_IOR4A	TRUE	NONE				34	100
IOR5A/MCS_N/D5	I/O	1	MCS_N/D5	True_of_IOR5B	NONE	NONE					97
IOR5B/MCLK/D4	I/O	1	MCLK/D4	Comp_of_IOR5A	NONE	NONE					98
IOR6A/FASTRD_N/D3	I/O	1	FASTRD_N /D3	True_of_IOR6B	NONE	NONE					96
IOR6B/SI/D2	I/O	1	SI/D2	Comp_of_IOR6A	NONE	NONE	12				95
IOR7A/SO/D1	I/O	1	SO/D1	True_of_IOR7B	TRUE	NONE	11		C1	32	90
IOR7B/SSPI_CS_N/D0	I/O	1	SSPI_CS_N/D0	Comp_of_IOR7A	TRUE	NONE	10		C2	31	88
IOR8A/DIN/CLKHOLD_N	I/O	1	DIN/CLKHOLD_N	True_of_IOR8B	NONE	NONE				29	86
IOR8B/DOUT/WE_N	I/O	1	DOUT/WE_N	Comp_of_IOR8A	NONE	NONE				30	87

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	QN32	QN32U	CS36	QN48	LQ144
IOR9A/GCLKT_3	I/O	1	GCLKT_3	True_of_IOR9B	NONE	NONE	9		D2	28	84
IOR9B/GCLKC_3	I/O	1	GCLKC_3	Comp_of_IOR9A	NONE	NONE	8			27	83
IOT10A/GCLKT_0	I/O	0	GCLKT_0	True_of_IOT10B	NONE	NONE					130
IOT10B/GCLKC_0	I/O	0	GCLKC_0	Comp_of_IOT10A	NONE	NONE					129
IOT11A/GCLKT_1	I/O	0	GCLKT_1	True_of_IOT11B	NONE	x16	20	20	A3		128
IOT11B/GCLKC_1	I/O	0	GCLKC_1	Comp_of_IOT11A	NONE	NONE			B3		126
IOT12A	I/O	0		True_of_IOT12B	NONE	NONE					124
IOT12B	I/O	0		Comp_of_IOT12A	NONE	NONE					123
IOT13A	I/O	0		True_of_IOT13B	NONE	x16				39	122
IOT13B	I/O	0		Comp_of_IOT13A	NONE	NONE				38	121
IOT14A	I/O	0		True_of_IOT14B	NONE	NONE					120
IOT14B	I/O	0		Comp_of_IOT14A	NONE	NONE					119
IOT15A	I/O	0		True_of_IOT15B	NONE	x16			A4		118
IOT15B	I/O	0		Comp_of_IOT15A	NONE	NONE			B4		117
IOT16A	I/O	0		True_of_IOT16B	NONE	NONE					116
IOT16B	I/O	0		Comp_of_IOT16A	NONE	NONE					115
IOT17A	I/O	0		True_of_IOT17B	NONE	x16			A5		114
IOT17B	I/O	0		Comp_of_IOT17A	NONE	NONE			B5		113
IOT18A	I/O	0		True_of_IOT18B	NONE	NONE					112
IOT18B	I/O	0		Comp_of_IOT18A	NONE	NONE					111
IOT19A	I/O	0		True_of_IOT19B	NONE	NONE					110
IOT19B	I/O	0		Comp_of_IOT19A	NONE	NONE					
IOT2A	I/O	0		True_of_IOT2B	NONE	x16					
IOT2B/MODE0	I/O	0	MODE0	Comp_of_IOT2A	NONE	NONE	23				143
IOT3A/MODE2	I/O	0	MODE2	True_of_IOT3B	NONE	NONE				48	142
IOT3B/MODE1	I/O	0	MODE1	Comp_of_IOT3A	NONE	NONE					141
IOT4A/CH0	I/O	0	CH0	True_of_IOT4B	NONE	x16		22	A1	47	140
IOT4B/CH1	I/O	0	CH1	Comp_of_IOT4A	NONE	NONE			B1	46	139
IOT5A/CH2	I/O	0	CH2	True_of_IOT5B	NONE	NONE				45	138
IOT5B/CH3	I/O	0	CH3	Comp_of_IOT5A	NONE	NONE				44	137
IOT6A/CH4	I/O	0	CH4	True_of_IOT6B	NONE	x16	22	21	A2	43	136
IOT6B/CH5	I/O	0	CH5	Comp_of_IOT6A	NONE	NONE	21		B2	42	135

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	QN32	QN32U	CS36	QN48	LQ144
IOT7A/CH6	I/O	0	CH6	True_of_IOT7B	NONE	NONE				41	134
IOT7B/CH7	I/O	0	CH7	Comp_of_IOT7A	NONE	NONE				40	133
IOT8A	I/O	0		True_of_IOT8B	NONE	x16					
IOT8B	I/O	0		Comp_of_IOT8A	NONE	NONE					
IOT9A	I/O	0		True_of_IOT9B	NONE	NONE					132
IOT9B	I/O	0		Comp_of_IOT9A	NONE	NONE					131
VCCO0	Power	N/A					19				
VCCO1	Power	N/A								25	91
VCCO2	Power	N/A					6	6	F1	13	37
VCCO2	Power	N/A									55
VCCO3	Power	N/A						31			5
VCCO3	Power	N/A									26
VCC/VCCPLL	Power	N/A					2		D4	12	
VCC/VCCPLL	Power	N/A					18			37	
VCCO1/VCCO3/VCCP/VCCX	Power	N/A					15				
VCCO1/VCCO3/VCCP/VCCX	Power	N/A					31				
VBUSPAD/VCCO1/VCCX/VDDAUSB/VDDDUSB	Power	N/A						15			
VBUSPAD/VCCO1/VCCX/VDDAUSB/VDDDUSB	Power	N/A						11			
VCC/VCCPLL/VDDPL	Power	N/A						2			1
VCC/VCCPLL/VDDPL	Power	N/A						7			36
VCC/VCCPLL/VDDPL	Power	N/A						18			73
VCC/VCCPLL/VDDPL	Power	N/A									108
VCCO0/VDDA	Power	N/A						19	A6		109
VCCO0/VDDA	Power	N/A						23			127
VCCO0/VDDA	Power	N/A									144
VCCO1/VCCO3	Power	N/A							C4		
VCCP/VCCX	Power	N/A							D3	8	
VCCP/VCCX	Power	N/A								36	
VCCO0/VCCO3/VDDA	Power	N/A								1	
VCCX/VDDAUSB	Power	N/A									31

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	QN32	QN32U	CS36	QN48	LQ144
VCCX/VDDAUSB	Power	N/A									78
VCCX/VDDAUSB	Power	N/A									103
DP	Power	N/A						8			75
IDPAD	Power	N/A						13			80
DM	Power	N/A						9			76
XIN	Power	N/A						10			77
XOUT	Power	N/A						12			79
REXT	Power	N/A						14			81
VBUSPAD	Power	N/A									82
VDDDUSB	Power	N/A									85
VSS	Ground	N/A					3	3	C3	2	2
VSS	Ground	N/A								26	33
VSS	Ground	N/A									105
VSS	Ground	N/A									125
VSS	Ground	N/A									89
VSS	Ground	N/A									53
VSS	Ground	N/A									17
VSS	Ground	N/A									35
VSS	Ground	N/A									107
VSS	Ground	N/A									74
NC	Ground	N/A									6
NC	Ground	N/A									10
NC	Ground	N/A									19
NC	Ground	N/A									32
NC	Ground	N/A									34
NC	Ground	N/A									48
NC	Ground	N/A									49
NC	Ground	N/A									50
NC	Ground	N/A									51
NC	Ground	N/A									52
NC	Ground	N/A									56
NC	Ground	N/A									57

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	QN32	QN32U	CS36	QN48	LQ144
NC	Ground	N/A									92
NC	Ground	N/A									93
NC	Ground	N/A									94

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	QN32	QN32U	CS36	QN48	LQ144
BANK3 True LVDS Pair										
IOL2A/JTAGSEL_N/VREF	I/O	3	JTAGSEL_N/VREF	True_of_IOL2B	TRUE					3
IOL2B	I/O	3		Comp_of_IOL2A	TRUE					4
IOL4A	I/O	3		True_of_IOL4B	TRUE					8
IOL4B	I/O	3		Comp_of_IOL4A	TRUE					9
IOL7A/GCLKT_6	I/O	3	GCLKT_6	True_of_IOL7B	TRUE	29	29		10	25
IOL7B/GCLKC_6	I/O	3	GCLKC_6	Comp_of_IOL7A	TRUE	30	30		11	27
BANK2 True LVDS Pair										
IOB11A/GCLKT_4	I/O	2	GCLKT_4	True_of_IOB11B	TRUE	4	4	F4	19	46
IOB11B/GCLKC_4	I/O	2	GCLKC_4	Comp_of_IOB11A	TRUE	5	5	E4	20	47
IOB13A	I/O	2		True_of_IOB13B	TRUE				21	59
IOB13B	I/O	2		Comp_of_IOB13A	TRUE				22	60
IOB15A	I/O	2		True_of_IOB15B	TRUE			F3	23	63
IOB15B	I/O	2		Comp_of_IOB15A	TRUE			E3	24	64
IOB17A	I/O	2		True_of_IOB17B	TRUE			F2		67
IOB17B	I/O	2		Comp_of_IOB17A	TRUE			E2		68
IOB7A	I/O	2		True_of_IOB7B	TRUE			F6		38
IOB7B	I/O	2		Comp_of_IOB7A	TRUE			E6		39
IOB9A	I/O	2		True_of_IOB9B	TRUE			F5	15	42
IOB9B	I/O	2		Comp_of_IOB9A	TRUE			E5	16	43
BANK1 True LVDS Pair										
IOR2A/RPLL_T_fb	I/O	1	RPLL_T_fb	True_of_IOR2B	TRUE	17				106
IOR2B/RPLL_C_fb	I/O	1	RPLL_C_fb	Comp_of_IOR2A	TRUE	16				104
IOR4A/MI/D7	I/O	1	MI/D7	True_of_IOR4B	TRUE				33	99
IOR4B/MO/D6	I/O	1	MO/D6	Comp_of_IOR4A	TRUE				34	100
IOR7A/SO/D1	I/O	1	SO/D1	True_of_IOR7B	TRUE	11		C1	32	90
IOR7B/SSPI_CS_N/D0	I/O	1	SSPI_CS_N/D0	Comp_of_IOR7A	TRUE	10		C2	31	88

Note!
VCCX should be greater than or equal to VCCO. It is recommended to connect VCCX with the maximum VCCO in the system.

Recommended Operating Conditions of Package QN32 in GW1NS-2C				
Name	**Description**		**Min.**	**Max.**
VCC/VCCPLL	VCC/VCCPLL are internally connected.		1.14V	1.26V
VCCO0, VCCO2	I/O Bank voltage	LX: I/O Bank voltage	1.14V	1.89V
		UX: I/O Bank voltage, the VCCX for the UX version of the device needs to be greater than or equal to the I/O Bank voltage.	1.14V	3.6V
VCCX/VCCO1/VCCO3	VCCX/VCCO1/VCCO3 are internally connected.	LX: Auxiliary voltage	1.71V	1.89V
		UX: Auxiliary voltage	2.375V	3.6V

Recommended Operating Conditions of Package QN32U in GW1NS-2C				
Name	**Description**		**Min.**	**Max.**
VCC/VCCPLL	VCC/VCCPLL are internally connected.		1.14V	1.26V
VCCO0, VCCO2, VCCO3	I/O Bank voltage	LX: I/O Bank voltage	1.14V	1.89V
		UX: I/O Bank voltage, the VCCX for the UX version of the device needs to be greater than or equal to the I/O Bank voltage.	1.14V	3.6V
		When output with the MIPI in BANK2, VCCO2 need provide 1.2V voltage.	1.14V	3.6V
		When ADC is used, VCCO0 should provide 3.3V voltage.	3.135V	3.6V
VCCX/VCCO1/VBUSPAD /VDDDUSB	VCCX/VCCO1/VBUSPAD/ VDDDUSB are internally connected.	LX: Auxiliary voltage (USB 2.0 PHY is not supported)	1.71V	1.89V
		UX: Auxiliary voltage（USB 2.0 PHY is supported）	2.375V	3.6V
		When USB 2.0 PHY is used, VCCX should provide 3.3V voltage.	3.135V	3.6V

Recommended Operating Conditions of Package CS36 in GW1NS-2C				
Name	**Description**		**Min.**	**Max.**
VCC/VCCPLL	VCC/VCCPLL are internally connected.		1.14V	1.26V
VCCO1/VCCO3	I/O Bank voltage, VCCO1/VCCO3 are internally connected.	LX: I/O Bank voltage	1.14V	1.89V
		UX: I/O Bank voltage, the VCCX for the UX version of the device needs to be greater than or equal to the I/O Bank voltage.	1.14V	3.6V
VCCO2, VCCO0	I/O Bank voltage	LX: I/O Bank voltage	1.14V	1.89V
		UX: I/O Bank voltage, the VCCX for the UX version of the device needs to be greater than or equal to the I/O Bank voltage.	1.14V	3.6V
		When ADC is used, VCCO0 should provide 3.3V voltage.	3.135V	3.6V
VCCX	LX: Auxiliary voltage		1.71V	1.89V
	UX: Auxiliary voltage		2.375V	3.6V

Recommended Operating Conditions of Package QN48 in GW1NS-2C				
Name	**Description**		**Min.**	**Max.**
VCC/VCCPLL	VCC/VCCPLL are internally connected.		1.14V	1.26V
VCCO1, VCCO2	I/O Bank voltage	LX: I/O Bank voltage	1.14V	1.89V
		UX: I/O Bank voltage, the VCCX for the UX version of the device needs to be greater than or equal to the I/O Bank voltage.	1.14V	3.6V
VCCX	LX: Auxiliary voltage		1.71V	1.89V
	UX: Auxiliary voltage		2.375V	3.6V
VCCO0/VCCO3	VCCO0/VCCO3 are internally connected.	LX: I/O Bank voltage	1.14V	1.89V
		UX: I/O Bank voltage, the VCCX for the UX version of the device needs to be greater than or equal to the I/O Bank voltage.	1.14V	3.6V
		When ADC is used, VCCO0 should provide 3.3V voltage.	3.135V	3.6V
Recommended Operating Conditions of Package LQ144 in GW1NS-2C				
Name	**Description**		**Min.**	**Max.**
VCC/VCCPLL	VCC/VCCPLL are internally connected.		1.14V	1.26V
VCCO0, VCCO1, VCCO2, VCCO3	I/O Bank voltage	LX: I/O Bank voltage	1.14V	1.89V
		UX: I/O Bank voltage, the VCCX for the UX version of the device needs to be greater than or equal to the I/O Bank voltage.	1.14V	3.6V
		When ADC is used, VCCO0 should provide 3.3V voltage.	3.135V	3.6V
VCCX/VDDAUSB	VCCX/VDDAUSB are internally connected.	LX: Auxiliary voltage (USB 2.0 PHY is not supported)	1.71V	1.89V
		UX: Auxiliary voltage（USB 2.0 PHY is supported）	2.375V	3.6V
		When USB 2.0 PHY is used, VCCX should provide 3.3V voltage.	3.135V	3.6V
VDDDUSB	Analog power supply pin (3.3V)		3.135V	3.6V