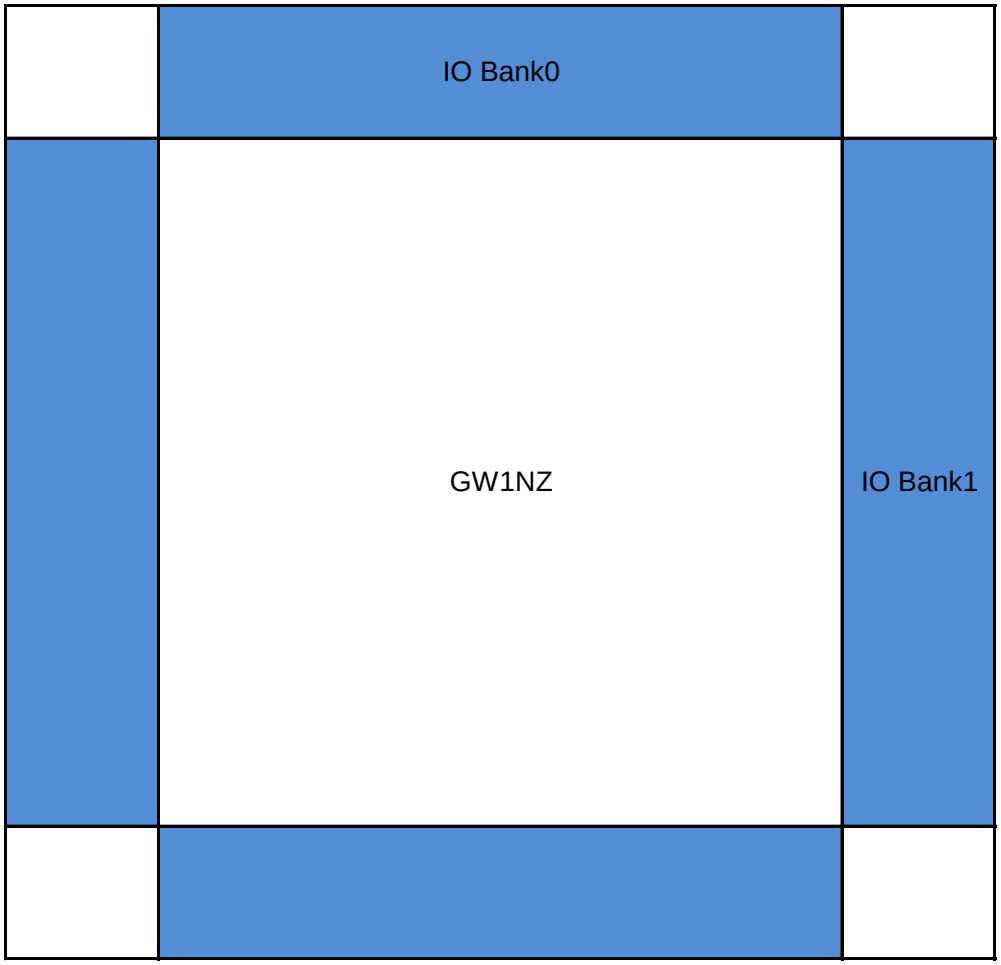
Date	Version	Description
09/27/2018	1.0E	Initial version published.
01/14/2019	1.1E	Recommended operating conditions added.
01/23/2019	1.2E	Core voltage of ZV version modified.
04/03/2019	1.3E	IO Bank View modified.
12/10/2019	1.4E	QN48 package added.
06/19/2020	1.5E	FN32F package added.
01/27/2021	1.5.1E	QN48 package (ZV Version) and core voltage info added.
10/29/2021	1.6E	The location of pin 9 in QN48 package modified. Pin definitions updated.
11/25/2021	1.6.1E	The location of pin 9 in QN49 package modified.
10/20/2022	1.6.2E	The note in Power sheet updated. The note in Pin Definitions sheet updated.
05/04/2023	1.6.3E	The description of CLKHOLD_N pin in Pin Definitions sheet updated. The note of FN32/FN32F/QN48 in Power sheet updated.
06/30/2023	1.6.4E	The descriptions of pin definitions and info. for MODE0, MODE1, MODE2 pins optimized.
09/08/2023	1.6.5E	CG25 and FN24 packages added.

Pin Name	I/O	Description
User I/O		
IO[End][Row/Column Number][A/B]	I/O	[End] indicates the pin location, including L(left), R(right), B(bottom), and T(top).
		[Row/Column Number] indicates the pin row/column number. If [End] is T(top) or B(bottom), the pin indicates the column number of the corresponding CFU. If [End] is L(left) or R(right), the pin indicates the row number of the corresponding CFU.
		[A/B] indicates differential signal pair information.
Multi-Function Pins		
IO [End][Row/Column Number][A/B]/MMM		/MMM represents one or more of the other functions in addition to being general purpose user I/O. When these functions are not in use, these pins can be used as user I/O.
D0	I/O	Data port D0 in CPU mode
D1	I/O	Data port D1 in CPU mode
D2	I/O	Data port D2 in CPU mode
D3	I/O	Data port D3 in CPU mode
D4	I/O	Data port D4 in CPU mode
D5	I/O	Data port D5 in CPU mode
D6	I/O	Data port D6 in CPU mode
D7	I/O	Data port D7 in CPU mode
WE_N	I	Select data input/output of D[7:0] in CPU mode.0: Write;1: Read.
DOUT	O	Data output in SERIAL mode
DIN	I, internal weak pull-up	Data input in SERIAL mode
TMS	I, internal weak pull-up	Serial mode input in JTAG mode
TCK	I	Serial clock input in JTAG mode
TDO	O	Serial data output in JTAG mode
TDI	I, internal weak pull-up	Serial data input in JTAG mode
JTAGSEL_N	I, internal weak pull-up	Reconfigure JTAG download function signal
RECONFIG_N	I, internal weak pull-up	Global reset GowinCONFIG logic signal, active low
FASTRD_N	I	Access SPI FLASH to select signal. Low, Fast Read mode; High, Read mode.
DONE[1]	O, internal weak pull-up	High, the programming configuration has been completed successfully; Low, the programming configuration has not been completed or failed.
	I, internal weak pull-up	When the DONE signal is low, delay the chip to activate. Activate the chip until the DONE signal is high.
READY[1]	I/O, internal weak pull-up	High, the device can be programmed and configured currently; Low, the device cannot be programmed and configured currently.
MI	I	MI in MSPI mode
MO	O	MO in MSPI mode

Pin Name	I/O	Description
MCS_N	O	Enable signal MCS_N in MSPI mode, active-low
MCLK	O	Clock output MCLK in MSPI mode, with default frequency of 2.5Mhz
SCLK	I	Clock input in SSPI, SERIAL, and CPU modes
SO	O	SO in SSPI mode
SI	I/O	SI in SSPI mode
SSPI_CS_N	I/O	Enable signal SSPI_CS_N in SSPI mode, active-low, and internal weak pull-up
CLKHOLD_N	I, internal weak pull-up	Active-high in SSPI mode; Active-low in CPU mode.
GCLKC_[x]	I	Differential input pin of GCLKT_[x], C(Comp), [x]: global clock No.[2]
GCLKT_[x]	I	Global clock input pin, T(True), [x]: global clock No.
LPLL_C_fb/RPLL_C_fb	I	Left/Right PLL feedback input pin, C(Comp)
LPLL_T_fb/RPLL_T_fb	I	Left/Right PLL feedback input pin, T(True)
LPLL_C_in/RPLL_C_in	I	Left/Right PLL clock input pin, C(Comp)
LPLL_T_in/RPLL_T_in	I	Left/Right PLL clock input pin, T(True)
MODE2	I, internal weak pull-up	GowinCONFIG modes selection pin; if this pin is marked as “VCCIO”, it's internally powered; if this pin is marked as "GND", it's internally grounded.
MODE1	I, internal weak pull-up	GowinCONFIG modes selection pin; if this pin is marked as “VCCIO”, it's internally powered; if this pin is marked as "GND", it's internally grounded.
MODE0	I, internal weak pull-up	GowinCONFIG modes selection pin; if this pin is marked as “VCCIO”, it's internally powered; if this pin is marked as "GND", it's internally grounded.
SPMI_SDATA	I/O	The communication bus in SPMI (System Power Management Interface) mode
SPMI_EN/VCCEN	I	The sleep control and enable in SPMI (System Power Management Interface) mode
SPMI_SCLK	I/O	The communication bus in SPMI (System Power Management Interface) mode
SPMI_CLK	I	The external low-speed clock in SPMI (System Power Management Interface) mode
Other Pins		
NC	NA	Reserved
VSS	NA	Ground
VCC	NA	Power supply pin of core voltage
VCCIO#	NA	Power supply pin of I/O voltage for I/O BANK#
VCCX	NA	Power supply pin of auxiliary voltage

Note!
[1] The default state of READY/DONE is open-drain output, internal weak pull-up. DONE outputs 0 during configuration.
[2] When the input is single-ended, GCLKC_[x] pin is not a global clock.



Note!

[1] Each Bank has independent reference voltage (VREF).
[2] You can select to use IOB internal VREF (equals to 0.5 * VCCIO).
[3] You can also select to use external VREF input (use any IO pins as external VREF input).

Note!
[1] The pin is internally grounded.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	CS16	FN32	FN32F	QN48	CG25	FN24
IOR10A	I/O	1		True_of_IOR10B	NONE		12	12	20	D3	8
IOR10B	I/O	1		Comp_of_IOR10A	NONE		11	11	13	E4	7
IOR2A	I/O	1		True_of_IOR2B	NONE		24		9		
IOR2B	I/O	1		Comp_of_IOR2A	NONE			24	10		
IOR3A	I/O	1		True_of_IOR3B	NONE		23	23	11	B1	1
IOR3B	I/O	1		Comp_of_IOR3A	NONE		22	22	34	C1	3
IOR4A/RPLL_T_fb	I/O	1	RPLL_T_fb	True_of_IOR4B	NONE		21	21			
IOR4B/RPLL_C_fb	I/O	1	RPLL_C_fb	Comp_of_IOR4A	NONE		20	20			
IOR5A/GCLKT_2/RPLL_T_in	I/O	1	GCLKT_2/RPLL_T_in	True_of_IOR5B	NONE	D3	19	19	33	C2	16
IOR5B/GCLKC_2/RPLL_C_in	I/O	1	GCLKC_2/RPLL_C_in	Comp_of_IOR5A	NONE		18	18	32	D2	15
IOR6A/MI/D7	I/O	1	MI/D7	True_of_IOR6B	NONE				31		
IOR6B/MO/D6	I/O	1	MO/D6	Comp_of_IOR6A	NONE				14		
IOR6C/MCS_N/D5	I/O	1	MCS_N/D5	True_of_IOR6D	NONE				30		
IOR6D/MCLK/D4	I/O	1	MCLK/D4	Comp_of_IOR6C	NONE				15		
IOR6E/FASTRD_N/D3	I/O	1	FASTRD_N/D3	True_of_IOR6F	NONE				29	B4	
IOR6F	I/O	1		Comp_of_IOR6E	NONE				16	C4	
IOR6G	I/O	1		True_of_IOR6H	NONE				17		
IOR6H	I/O	1		Comp_of_IOR6G	NONE				18		
IOR6I/DIN/CLKHOLD_N	I/O	1	DIN/CLKHOLD_N	True_of_IOR6J	NONE				28	D1	14
IOR6J/DOUT/WE_N	I/O	1	DOUT/WE_N	Comp_of_IOR6I	NONE				19	E1	13
IOR7A/GCLKT_3/SSPI_CS_N/D0	I/O	1	GCLKT_3/SSPI_CS_N/D0	True_of_IOR7B	NONE	D1	17	17	27	E2	5
IOR7B/GCLKC_3	I/O	1	GCLKC_3	Comp_of_IOR7A	NONE				21	E3	4
IOR8A/SO/D1	I/O	1	SO/D1	True_of_IOR8B	NONE	D2			24		
IOR8B	I/O	1		Comp_of_IOR8A	NONE		14	14	23		
IOR9A/SI/D2	I/O	1	SI/D2	True_of_IOR9B	NONE	C1	15	15	22		11
IOR9B	I/O	1		Comp_of_IOR9A	NONE		16	16			10
IOT10A/GCLKT_0	I/O	0	GCLKT_0	True_of_IOT10B	NONE		32	32	47		
IOT10B/GCLKC_0	I/O	0	GCLKC_0	Comp_of_IOT10A	NONE		31	31	8		
IOT11A/GCLKT_1	I/O	0	GCLKT_1	True_of_IOT11B	NONE		30	30			
IOT11B/GCLKC_1	I/O	0	GCLKC_1	Comp_of_IOT11A	NONE		29	29			
IOT12A/DONE	I/O	0	DONE	True_of_IOT12B	NONE		28	28	46	B5	23
IOT12B/READY	I/O	0	READY	Comp_of_IOT12A	NONE		27	27	45		
IOT13A/JTAGSEL_N	I/O	0	JTAGSEL_N	True_of_IOT13B	NONE		26	26	44		
IOT13B	I/O	0		Comp_of_IOT13A	NONE						
IOT14A/MODE0	I/O	0	MODE0	True_of_IOT14B	NONE	B3	GND[1]	GND[1]	43	C5	22

Note!
[1] The pin is internally grounded.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	CS16	FN32	FN32F	QN48	CG25	FN24
IOT14B/MODE1	I/O	0	MODE1	Comp_of_IOT14A	NONE	GND[1]	GND[1]	GND[1]	42	GND[1]	GND[1]
IOT15A/MODE2	I/O	0	MODE2	True_of_IOT15B	NONE	GND[1]	GND[1]	GND[1]	GND[1]	C5	22
IOT15B	I/O	0		Comp_of_IOT15A	NONE	A2	25	25	41	D5	
IOT16A	I/O	0		True_of_IOT16B	NONE				40	A4	21
IOT16B	I/O	0		Comp_of_IOT16A	NONE				39	B3	
IOT17A	I/O	0		True_of_IOT17B	NONE				38	A3	20
IOT17B	I/O	0		Comp_of_IOT17A	NONE				35	A2	19
IOT7A/TMS/SPMI_SDATA	I/O	0	TMS/SPMI_SDATA	True_of_IOT7B	NONE	C4	7	7	4		
IOT7B/TCK/SPMI_EN/VCCEN	I/O	0	TCK/SPMI_EN/VCCEN	Comp_of_IOT7A	NONE	B4	6	6	3		
IOT8A/TDI/SPMI_SCLK	I/O	0	TDI/SPMI_SCLK	True_of_IOT8B	NONE	A4	3	3	5		
IOT8B/TDO	I/O	0	TDO	Comp_of_IOT8A	NONE	A3	1	1	7		
IOT9A/SCLK/SPMI_CLK	I/O	0	SCLK/SPMI_CLK	True_of_IOT9B	NONE	B1			6	A5	24
IOT9B/RECONFIG_N	I/O	0	RECONFIG_N	Comp_of_IOT9A	NONE		2	2	48		
VCC	Power	N/A				D4	9	9	12	E5	6
VCC	Power	N/A							37		
VCCIO0	Power	N/A				B2	5	5	1	D4	18
VCCIO1	Power	N/A				C3	13	13	25	B2	9
VCCX	Power	N/A				A1	4	4	36	A1	2
VSS	Ground	N/A				C2	10	8	2	C3	12
VSS	Ground	N/A					8	10	26		17

Note!
VCCX should be greater than or equal to VCCIO.

Recommended Operating Conditions of CS16 Package in GW1NZ-1			
Name	**Description**	**Min.**	**Max.**
VCC	LV: Core voltage	1.14V	1.26V
	ZV: Core voltage	0.88V	1V
VCCIO0, VCCIO1	I/O Bank voltage	1.14V	3.6V
VCCX	Auxiliary voltage	1.71V	3.6V

Recommended Operating Conditions of FN32/FN32F/QN48 Package in GW1NZ-1			
Name	**Description**	**Min.**	**Max.**
VCC	LV: Core voltage	1.14V	1.26V
	ZV: Core voltage	0.88V	1V
VCCIO0, VCCIO1	I/O Bank voltage	1.14V	3.6V
VCCX	Auxiliary voltage	1.71V	3.6V

Note!
It is highly recommended that the epad connect to GND, but not a requirement.

Recommended Operating Conditions of CG25 Package in GW1NZ-1			
Name	**Description**	**Min.**	**Max.**
VCC	LV: Core voltage	1.14V	1.26V
VCCIO0, VCCIO1	I/O Bank voltage	1.14V	3.6V
VCCX	Auxiliary voltage	1.71V	3.6V

Recommended Operating Conditions of FN24 Package in GW1NZ-1			
Name	**Description**	**Min.**	**Max.**
VCC	LV: Core voltage	1.14V	1.26V
VCCIO0, VCCIO1	I/O Bank voltage	1.14V	3.6V
VCCX	Auxiliary voltage	1.71V	3.6V

Note!
It is highly recommended that the epad connect to GND, but not a requirement.