| Data | Version | Description |
|---|---|---|
| 08/18/2023 | 1.0E | Initial version, QN48 and CS100H packages supported. |
| 11/30/2023 | 1.1E | The info. of CS42 package added.<br>The description of the directions for Ready and Done pins in Pin Definitions sheet optimized.<br>The Max. value of VCC for QN48 and CS100H packages in Power sheet updated. |
| 12/07/2023 | 1.1.1E | The description of VCCD and VCCIOD pins in Pin Definitions sheet updated. |
| 12/28/2023 | 1.1.2E | The voltage value range of VCC in Power sheet updated. |
| 02/22/2024 | 1.1.3E | The bank diagram of CS100H package in Bank sheet added.<br>The note of VCCD and VCCIOD pins in Power sheet added. |
| 07/05/2024 | 1.1.4E | The Min. value of VCC voltage in Power sheet updated. |
| 11/15/2024 | 1.1.5E | The description of EPAD pin in Pin Definitions sheet added. |
| 02/28/2025 | 1.2E | The information of CG56 package added. |

| Pins Name | Direction | Description |
|---|---|---|
| **User I/O Pins** | | |
| IO [End][Row/Column Number][A/B] | I/O | [End] indicates the pin location, including L(left), R(right), B(bottom), and T(top) |
| | | [Row/Column Number] indicates the pin Row/Column number.<br>If [End] is T(top) or B(bottom), the pin indicates the column number of the corresponding CFU.<br>If [End] is L(left) or R(right), the pin indicates the row number of the corresponding CFU. |
| | | [A/B] indicaties differential signal pair information. |
| **Multi-Function Pins** | | |
| IO [End][Row/Column Number][A/B]/MMM | | /MMM represents one or more of the other functions in addition to being general purpose user I/O.<br>When not used for the specical functions, these pins can be user I/O. |
| D0 | I/O | Data port D0 in CPU mode |
| D1 | I/O | Data port D1 in CPU mode |
| D2 | I/O | Data port D2 in CPU mode |
| D3 | I/O | Data port D3 in CPU mode |
| D4 | I/O | Data port D4 in CPU mode |
| D5 | I/O | Data port D5 in CPU mode |
| D6 | I/O | Data port D6 in CPU mode |
| D7 | I/O | Data port D7 in CPU mode |
| WE_N | I | Select data input/output of D[7:0] in CPU mode |
| MODE2 | I, Internal Weak Pull Up | GowinCONFIG modes selection pin; if this pin is marked as “VCCIO”, it's internally powered; if this pin is marked as "GND", it's internally grounded. |
| MODE1 | I, Internal Weak Pull Up | GowinCONFIG modes selection pin; if this pin is marked as “VCCIO”, it's internally powered; if this pin is marked as "GND", it's internally grounded. |
| MODE0 | I, Internal Weak Pull Up | GowinCONFIG modes selection pin; if this pin is marked as “VCCIO”, it's internally powered; if this pin is marked as "GND", it's internally grounded. |
| TMS | I, Internal Weak Pull Up | Serial mode input in JTAG mode |
| TCK | I | Serial clock input in JTAG mode, which needs to be connected with 4.7 K drop-down resistance on |
| TDO | O | Serial data output in JTAG mode |
| TDI | I, Internal Weak Pull Up | Serial data input in JTAG mode |
| JTAGSEL_N | I, Internal Weak Pull Up | JTAG mode selection, active-low |
| FASTRD_N | I/O | Flash access speed selection port FASTRD_N in MSPI mode.<br>Low indicates high-speed Flash access mode; high indicates regular Flash access mode. |
| MI | I/O | MISO in MSPI mode: Master data input/Slave data output |

| Pins Name | Direction | Description |
|---|---|---|
| MO | I/O | MOSI in MSPI mode:Master data output/Slave data input |
| MCS_N | I/O | Enable signal MCS_N in MSPI mode, active-low |
| MCLK | I/O | Clock output MCLK in MSPI mode, and the frequency is 2.1 Mhz by default, the accuracy is +/-5%. |
| DOUT | O | Data output in SERIAL mode |
| DIN | I, Internal Weak Pull Up | Data input in SERIAL mode |
| SCLK | I | Clock input in SSPI, SERIAL, and CPU modes |
| SO | I/O | MISO in SSPI mode:Master data input/Slave data output |
| SI | I/O | MOSI in SSPI mode:Master data output/Slave data input |
| SSPI_CS_N | I/O | Enable signal SSPI_CS_N in SSPI mode, active-low, Internal weak pull up |
| CLKHOLD_N | I, Internal Weak Pull Up | High, SSPI and CPU modes are valid<br>Low, SSPI and CPU modes are invalid |
| SDA | I/O | Serial data line |
| SCL | I | Serial clock line |
| RECONFIG_N | I, Internal Weak Pull Up | Start new GowinCONFIG mode when low pulse |
| DONE[3] | I/O, Internal Weak Pull Up | High indicates successful completion of programming and configuration<br>Low indicates incomplete or failed programming and configuration |
| READY[3] | I/O, Internal Weak Pull Up | When high, device can be programmed and configured<br>When low, device cannot be programmed and configured |
| GCLKT_[x] | I | Pins for Global clock input,T(True), [x] is global clock number |
| GCLKC_[x] | I | Differential input pin for GCLKT_[x], C(Comp), [x] is global clock number[1] |
| LPLL_T_fb/RPLL_T_fb | I | Left/Right PLL feedback input pin, T(True) |
| LPLL_C_fb/RPLL_C_fb | I | Left/Right PLL feedback input pin, C(Comp) |
| LPLL_T_in/RPLL_T_in | I | Left/Right PLL clock input pin,T(True) |
| LPLL_C_in/RPLL_C_in | I | Left/Right PLL clock input pin, C(Comp) |
| **Other Pins** | | |
| CKP | DIO[2] | Clock channel input pin for MIPI_DPHY_RX, T(True) |
| CKN | DIO[2] | Differential input pin of clock channel for MIPI_DPHY_RX, C(Comp) |
| RX0P | DIO[2] | Data channel 0 input pin for MIPI_DPHY_RX, T(True) |
| RX0N | DIO[2] | Differential input pin of data channel 0 for MIPI_DPHY_RX, C(Comp) |
| RX1P | DIO[2] | Data channel 1 input pin for MIPI_DPHY_RX,T(True) |
| RX1N | DIO[2] | Differential input pin of data channel 1 for MIPI_DPHY_RX, C(Comp) |

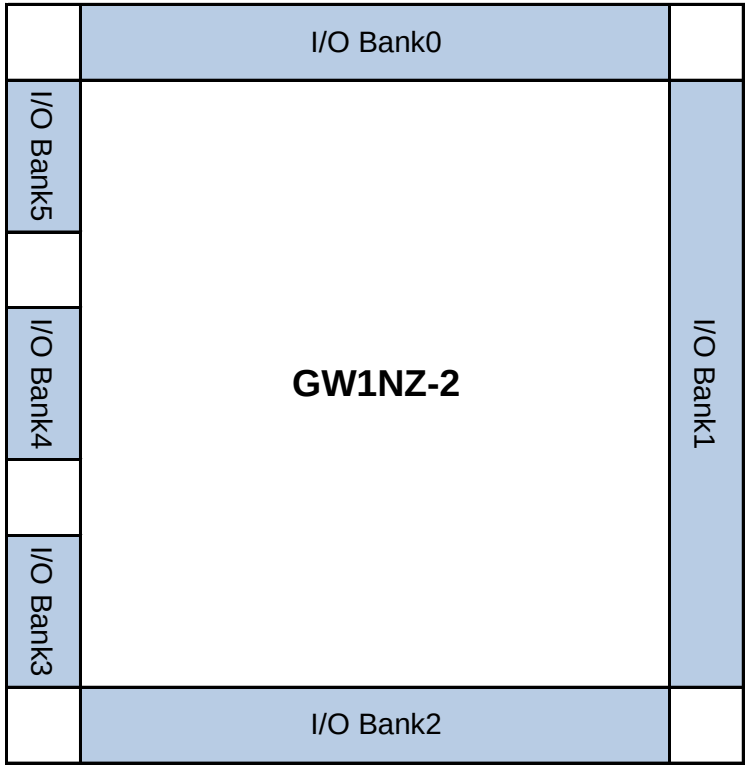
| Pins Name | Direction | Description |
|---|---|---|
| RX2P | DIO[2] | Data channel 2 input pin for MIPI_DPHY_RX, T(True) |
| RX2N | DIO[2] | Differential input pin of data channel 2 for MIPI_DPHY_RX, C(Comp) |
| RX3P | DIO[2] | Data channel 3 input pin for MIPI_DPHY_RX, T(True) |
| RX3N | DIO[2] | Differential input pin of data channel 3 for MIPI_DPHY_RX, C(Comp) |
| NC | NA | Reserved |
| VSS | NA | Ground pin |
| VCCD | NA | Power supply pin for MIPI |
| VCCIOD | NA | Power supply pin for MIPI |
| VCC | NA | Power supply pin for internal core logic |
| VCCIO# | NA | Power supply pin for I/O voltage of I/O BANK# |
| VCCX | NA | Power supply pin for auxiliary voltage |
| EPAD | NA | Exposed pad. Connect to ground. |

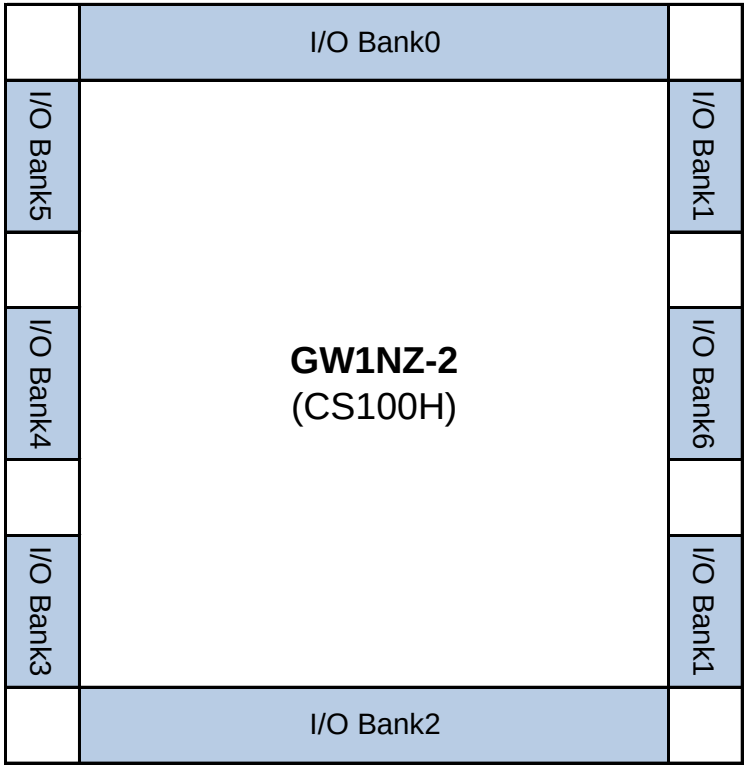
**Note!**

[1] When the input is single-ended, the GCLKC_[x] pin is not a global clock pin.

[2] DIO is a dedicated pin.

[3] The default state of READY/DONE is open-drain output, internal weak pull-up. DONE outputs 0 during configuration.




**Note!**

[1] Each Bank has independent reference volatge (VREF).

[2] You can select to use IOB internal VREF (equals to 0.5*VCCIO).

[3] You can also select to use external VREF input (use any IO pins as external VREF input).

**Note!**
VCCX should be greater than or equal to VCCIO.
[1] When MIPI HARD Core is not used, users can either leave VCCD and VCCIOD floating or connect them to 1.2V power.

| Recommended Operating Conditions of QN48 Package for GW1NZ-2 | | | |
|---|---|---|---|
| **Name** | **Description** | **Min.** | **Max.** |
| VCC/VCCPLL | Core voltage for ZV version, VCC and VCCPLL are internally short-circuited. | 0.88V | 1.05V |
| VCCIO0, VCCIO1 | I/O Bank voltage | 1.14V | 3.6V |
| VCCIO3/VCCIO4/VCCIO5 | I/O Bank voltage，VCCIO3, VCCIO4, and VCCIO5 are internally short-circuited. | 1.14V | 3.6V |
| VCCX/VCCIO2 | Auxiliary voltage VCCX and VCCIO2 are internally short-circuited. | 1.71V | 2.75V |

**Note！**
It is highly recommended that the EPAD connect to GND, but not a requirement.

| Recommended Operating Conditions of CS100H Package for GW1NZ-2 | | | |
|---|---|---|---|
| **Name** | **Description** | **Min.** | **Max.** |
| VCC/VCCPLL | Core voltage for ZV version, VCC and VCCPLL are internally short-circuited. | 0.88V | 1.05V |
| VCCIO0, VCCIO1, VCCIO2, VCCIO3, VCCIO4, VCCIO5 | I/O Bank voltage | 1.14V | 3.6V |
| VCCX | Auxiliary voltage | 1.71V | 2.75V |
| VCCD/VCCIOD[1] | VCCD and VCCIOD are internally short-circuited. | 1.14V | 1.26V |

| Recommended Operating Conditions of CS42 Package for GW1NZ-2 | | | |
|---|---|---|---|
| **Name** | **Description** | **Min.** | **Max.** |
| VCC | Core voltage for LV version | 1.07V | 1.26V |
| VCCIO0 | I/O Bank voltage | 1.14V | 3.6V |
| VCCIO1/VCCIO2 | I/O Bank voltage, VCCIO1 and VCCIO2 are internally short-circuited. | 1.14V | 3.6V |
| VCCIO3/VCCIO4/VCCIO5 | I/O Bank voltage, VCCIO3, VCCIO4, and VCCIO5 are internally short-circuited. | 1.14V | 3.6V |
| VCCX | Auxiliary voltage | 1.71V | 3.6V |

| Recommended Operating Conditions of CG56 Package for GW1NZ-2 | | | |
|---|---|---|---|
| **Name** | **Description** | **Min.** | **Max.** |
| VCC | Core voltage for LV version | 1.07V | 1.26V |
| VCCIO0、VCCIO2 | I/O Bank voltage | 1.14V | 3.6V |
| VCCIO1/VCCX | Auxiliary voltage VCCX and VCCIO1 are internally short-circuited. | 1.71V | 3.6V |
| VCCIO3/VCCIO4/VCCIO5 | I/O Bank voltage, VCCIO3, VCCIO4, and VCCIO5 are internally short-circuited. | 1.14V | 3.6V |

**Note!**

[1] You can ignore the short-circuited pins.

[2] The pin is internally grounded.

| Pin Name | Function | BANK | Configuration Function | Differential Pair | LVDS | X16 | QN48 | CS100H | CS42 | CG56 |
|---|---|---|---|---|---|---|---|---|---|---|
| IOB11A | I/O | 2 | | True_of_IOB11B | True | x16 | | K5 | E1 | F1 |
| IOB11B | I/O | 2 | | Comp_of_IOB11A | True | none | | J5 | E2 | F2 |
| IOB12A/FASTRD_N | I/O | 2 | FASTRD_N | True_of_IOB12B | none | none | | | | |
| IOB12B | I/O | 2 | | Comp_of_IOB12A | none | none | | | | |
| IOB13A | I/O | 2 | | True_of_IOB13B | True | x16 | 33 | H5 | F1 | H3 |
| IOB13B | I/O | 2 | | Comp_of_IOB13A | True | none | 32 | G5 | F2 | G3 |
| IOB14A | I/O | 2 | | True_of_IOB14B | none | none | | | | |
| IOB14B | I/O | 2 | | Comp_of_IOB14A | none | none | | | | |
| IOB15A | I/O | 2 | | True_of_IOB15B | True | x16 | | K4 | G1 | G1 |
| IOB15B | I/O | 2 | | Comp_of_IOB15A | True | none | | J4 | G2 | G2 |
| IOB16A | I/O | 2 | | True_of_IOB16B | none | none | | | | |
| IOB16B/DOUT/WE_N | I/O | 2 | DOUT/WE_N | Comp_of_IOB16A | none | none | | | | |
| IOB17A | I/O | 2 | | True_of_IOB17B | True | x16 | | H4 | | |
| IOB17B | I/O | 2 | | Comp_of_IOB17A | True | none | | G4 | | |
| IOB18A/SSPI_CS_N | I/O | 2 | SSPI_CS_N | True_of_IOB18B | none | none | 34 | K3 | F3 | H2 |
| IOB18B/SI | I/O | 2 | SI | Comp_of_IOB18A | none | none | 35 | J3 | G3 | H1 |
| IOB2A | I/O | 2 | | True_of_IOB2B | True | x16 | | K10 | | G5 |
| IOB2B | I/O | 2 | | Comp_of_IOB2A | True | none | | J10 | | F5 |
| IOB3A/DIN/CLKHOLD_N | I/O | 2 | DIN/CLKHOLD_N | True_of_IOB3B | none | none | | | | H5 |
| IOB3B | I/O | 2 | | Comp_of_IOB3A | none | none | | | | |
| IOB4A | I/O | 2 | | True_of_IOB4B | True | x16 | | | | |
| IOB4B | I/O | 2 | | Comp_of_IOB4A | True | none | | H8 | | |
| IOB5A/SCLK | I/O | 2 | SCLK | True_of_IOB5B | none | none | 29 | K9 | F4 | F4 |
| IOB5B/SO | I/O | 2 | SO | Comp_of_IOB5A | none | none | 28 | J9 | G4 | F3 |
| IOB6A | I/O | 2 | | True_of_IOB6B | True | x16 | | K8 | C1 | H4 |
| IOB6B | I/O | 2 | | Comp_of_IOB6A | True | none | | J8 | C2 | G4 |
| IOB7A/GCLKT_4 | I/O | 2 | GCLKT_4 | True_of_IOB7B | none | none | 31 | K7 | | |
| IOB7B/GCLKC_4 | I/O | 2 | GCLKC_4 | Comp_of_IOB7A | none | none | 30 | J7 | | |
| IOB8A | I/O | 2 | | True_of_IOB8B | True | x16 | | H7 | | |
| IOB8B | I/O | 2 | | Comp_of_IOB8A | True | none | | H6 | | |
| IOB9A/GCLKT_3 | I/O | 2 | GCLKT_3 | True_of_IOB9B | none | none | | K6 | D1 | E2 |

**Note!**

[1] You can ignore the short-circuited pins.

[2] The pin is internally grounded.

| Pin Name | Function | BANK | Configuration Function | Differential Pair | LVDS | X16 | QN48 | CS100H | CS42 | CG56 |
|---|---|---|---|---|---|---|---|---|---|---|
| IOB9B/GCLKC_3 | I/O | 2 | GCLKC_3 | Comp_of_IOB9A | none | none | | J6 | D2 | E1 |
| IOL11A | I/O | 4 | | True_of_IOL11B | True | x16 | 20 | E10_L11A[1] | | E6 |
| IOL11B | I/O | 4 | | Comp_of_IOL11A | True | none | 21 | D10_L11B[1] | | E7 |
| IOL12A/GCLKT_6 | I/O | 4 | GCLKT_6 | True_of_IOL12B | none | none | | F10 | | |
| IOL12B/GCLKC_6 | I/O | 4 | GCLKC_6 | Comp_of_IOL12A | none | none | | F9 | | |
| IOL13A | I/O | 4 | | True_of_IOL13B | True | x16 | | G9 | E5 | F7 |
| IOL13B | I/O | 4 | | Comp_of_IOL13A | True | none | | G10 | E6 | F6 |
| IOL14A | I/O | 4 | | True_of_IOL14B | none | none | | F8 | | |
| IOL14B | I/O | 4 | | Comp_of_IOL14A | none | none | | E8 | | |
| IOL15A | I/O | 3 | | True_of_IOL15B | True | x16 | 23 | G10_L15A[1] | F5 | G7 |
| IOL15B | I/O | 3 | | Comp_of_IOL15A | True | none | 22 | E9 | F6 | G6 |
| IOL16A/GCLKT_5 | I/O | 3 | GCLKT_5 | True_of_IOL16B | none | none | | H10 | | |
| IOL16B/GCLKC_5 | I/O | 3 | GCLKC_5 | Comp_of_IOL16A | none | none | | H9 | | |
| IOL17A | I/O | 3 | | True_of_IOL17B | True | x16 | 27 | E9_L17A[1] | G5 | H7 |
| IOL17B | I/O | 3 | | Comp_of_IOL17A | True | none | 24 | G9_L17B[1] | G6 | H6 |
| IOL18A | I/O | 3 | | True_of_IOL18B | none | none | | G8 | | |
| IOL18B | I/O | 3 | | Comp_of_IOL18A | none | none | | | | |
| IOL19A | I/O | 3 | | True_of_IOL19B | none | none | | | | |
| IOL19B | I/O | 3 | | Comp_of_IOL19A | none | none | | | | |
| IOL4A/LPLL_T_fb | I/O | 5 | LPLL_T_fb | True_of_IOL4B | True | x16 | 15 | C10 | | B7 |
| IOL4B/LPLL_C_fb | I/O | 5 | LPLL_C_fb | Comp_of_IOL4A | True | none | 14 | C9 | | A7 |
| IOL5A/LPLL_T_in | I/O | 5 | LPLL_T_in | True_of_IOL5B | none | none | 16 | | | |
| IOL5B/LPLL_C_in | I/O | 5 | LPLL_C_in | Comp_of_IOL5A | none | none | 17 | | | |
| IOL6A/GCLKT_7 | I/O | 5 | GCLKT_7 | True_of_IOL6B | True | x16 | 18 | D10 | D5 | C7 |
| IOL6B/GCLKC_7 | I/O | 5 | GCLKC_7 | Comp_of_IOL6A | True | none | 19 | D9 | D6 | C6 |
| IOL7A | I/O | 5 | | True_of_IOL7B | none | none | | | | |
| IOL7B | I/O | 5 | | Comp_of_IOL7A | none | none | | | | |
| IOL8A | I/O | 5 | | True_of_IOL8B | True | x16 | | D9_L8A[1] | C5 | D7 |
| IOL8B | I/O | 5 | | Comp_of_IOL8A | True | none | | E10 | C6 | D6 |
| IOL9A | I/O | 4 | | True_of_IOL9B | none | none | | | | |
| IOL9B | I/O | 4 | | Comp_of_IOL9A | none | none | | | | |

**Note!**

[1] You can ignore the short-circuited pins.

[2] The pin is internally grounded.

| Pin Name | Function | BANK | Configuration Function | Differential Pair | LVDS | X16 | QN48 | CS100H | CS42 | CG56 |
|---|---|---|---|---|---|---|---|---|---|---|
| IOR11A/GCLKT_2 | I/O | 1 | GCLKT_2 | True_of_IOR11B | True | none | 41 | G3 | | |
| IOR11B/GCLKC_2 | I/O | 1 | GCLKC_2 | Comp_of_IOR11A | True | none | 40 | F3 | | |
| IOR12A | I/O | 1 | | True_of_IOR12B | none | none | | | | |
| IOR12B | I/O | 1 | | Comp_of_IOR12A | none | none | | | | |
| IOR13A | I/O | 1 | | True_of_IOR13B | True | none | 38 | H1 | | |
| IOR13B | I/O | 1 | | Comp_of_IOR13A | True | none | 39 | H2 | | |
| IOR14A | I/O | 1 | | True_of_IOR14B | none | none | | H3 | | |
| IOR14B | I/O | 1 | | Comp_of_IOR14A | none | none | | | | |
| IOR15A | I/O | 1 | | True_of_IOR15B | True | none | | J1 | | |
| IOR15B | I/O | 1 | | Comp_of_IOR15A | True | none | | J2 | | |
| IOR16A | I/O | 1 | | True_of_IOR16B | none | none | | | | |
| IOR16B | I/O | 1 | | Comp_of_IOR16A | none | none | | | | |
| IOR17A | I/O | 1 | | True_of_IOR17B | True | none | | K1 | | |
| IOR17B | I/O | 1 | | Comp_of_IOR17A | True | none | | K2 | | |
| IOR18A | I/O | 1 | | True_of_IOR18B | none | none | | | | |
| IOR18B | I/O | 1 | | Comp_of_IOR18A | none | none | | | | |
| IOR19A | I/O | 1 | | True_of_IOR19B | none | none | | | | |
| IOR19B | I/O | 1 | | Comp_of_IOR19A | none | none | | | | |
| IOR1A | I/O | 1 | | True_of_IOR1B | True | none | 47 | A1 | | |
| IOR1B | I/O | 1 | | Comp_of_IOR1A | True | none | 46 | A2 | | |
| IOR2A | I/O | 1 | | True_of_IOR2B | none | none | | | | |
| IOR2B | I/O | 1 | | Comp_of_IOR2A | none | none | | | | |
| IOR3A/D2 | I/O | 1 | D2 | True_of_IOR3B | True | none | 45 | B1 | | |
| IOR3B/D3 | I/O | 1 | D3 | Comp_of_IOR3A | True | none | 44 | B2 | | |
| IOR4A/D0 | I/O | 1 | D0 | True_of_IOR4B | none | none | | | | |
| IOR4B/D1 | I/O | 1 | D1 | Comp_of_IOR4A | none | none | | | | |
| IOR5A/MI/D7 | I/O | 1 | MI/D7 | True_of_IOR5B | True | none | 43 | C3 | | |
| IOR5B/MO/D6 | I/O | 1 | MO/D6 | Comp_of_IOR5A | True | none | 42 | D4 | | |
| IOR6A/MCS_N/D5 | I/O | 1 | MCS_N/D5 | True_of_IOR6B | none | none | | D3 | | |
| IOR6B/MCLK/D4 | I/O | 1 | MCLK/D4 | Comp_of_IOR6A | none | none | | E3 | | |
| IOT11A/GCLKT_0 | I/O | 0 | GCLKT_0 | True_of_IOT11B | True | x16 | 6 | D7 | A3 | C1 |

**Note!**

[1] You can ignore the short-circuited pins.

[2] The pin is internally grounded.

| Pin Name | Function | BANK | Configuration Function | Differential Pair | LVDS | X16 | QN48 | CS100H | CS42 | CG56 |
|---|---|---|---|---|---|---|---|---|---|---|
| IOT11B/GCLKC_0 | I/O | 0 | GCLKC_0 | Comp_of_IOT11A | True | none | 7 | B6 | B3 | D1 |
| IOT12A | I/O | 0 | | True_of_IOT12B | none | none | | C7 | | |
| IOT12B | I/O | 0 | | Comp_of_IOT12A | none | none | | | | |
| IOT13A | I/O | 0 | | True_of_IOT13B | True | x16 | | A6 | B2 | |
| IOT13B | I/O | 0 | | Comp_of_IOT13A | True | none | | A4 | B1 | |
| IOT14A/GCLKT_1/SCL | I/O | 0 | GCLKT_1/SCL | True_of_IOT14B | none | none | 5 | A5 | | B3 |
| IOT14B/GCLKC_1/SDA | I/O | 0 | GCLKC_1/SDA | Comp_of_IOT14A | none | none | 4 | B5 | | A3 |
| IOT15A | I/O | 0 | | True_of_IOT15B | True | x16 | | B4 | | |
| IOT15B | I/O | 0 | | Comp_of_IOT15A | True | none | | A6_T15B[1] | | |
| IOT16A/JTAGSEL_N | I/O | 0 | JTAGSEL_N | True_of_IOT16B | none | none | 3 | C6 | A2 | A2 |
| IOT16B/RECONFIG_N | I/O | 0 | RECONFIG_N | Comp_of_IOT16A | none | none | 48 | D5 | | B2 |
| IOT17A | I/O | 0 | | True_of_IOT17B | True | x16 | | A4_T17A[1] | | |
| IOT17B | I/O | 0 | | Comp_of_IOT17A | True | none | | B4_T17B[1] | | |
| IOT18A/READY | I/O | 0 | READY | True_of_IOT18B | none | none | | A3 | | A1 |
| IOT18B/DONE | I/O | 0 | DONE | Comp_of_IOT18A | none | none | | B3 | | B1 |
| IOT19A | I/O | 0 | | True_of_IOT19B | none | none | | C5 | | |
| IOT19B | I/O | 0 | | Comp_of_IOT19A | none | none | | C4 | | |
| IOT2A/MODE0 | I/O | 0 | MODE0 | True_of_IOT2B | none | none | 13 | A10 | B6 | B6 |
| IOT2B/MODE1 | I/O | 0 | MODE1 | Comp_of_IOT2A | none | none | GND[2] | GND[2] | GND[2] | GND[2] |
| IOT3A/MODE2 | I/O | 0 | MODE2 | True_of_IOT3B | none | none | GND[2] | B10 | GND[2] | GND[2] |
| IOT4A | I/O | 0 | | True_of_IOT4B | True | x16 | | | B5 | A5 |
| IOT4B | I/O | 0 | | Comp_of_IOT4A | True | none | | | | A6 |
| IOT5A | I/O | 0 | | True_of_IOT5B | none | none | | | | |
| IOT5B | I/O | 0 | | Comp_of_IOT5A | none | none | | | | |
| IOT6A | I/O | 0 | | True_of_IOT6B | True | x16 | | A9 | | |
| IOT6B | I/O | 0 | | Comp_of_IOT6A | True | none | | B9 | | B5 |
| IOT7A/TDO | I/O | 0 | TDO | True_of_IOT7B | none | none | 11 | A8 | A6 | A4 |
| IOT7B/TDI | I/O | 0 | TDI | Comp_of_IOT7A | none | none | 10 | B8 | A5 | B4 |
| IOT8A | I/O | 0 | | True_of_IOT8B | True | x16 | | C8 | | |
| IOT8B | I/O | 0 | | Comp_of_IOT8A | True | none | | D8 | | |

**Note!**

[1] You can ignore the short-circuited pins.

[2] The pin is internally grounded.

| Pin Name | Function | BANK | Configuration Function | Differential Pair | LVDS | X16 | QN48 | CS100H | CS42 | CG56 |
|---|---|---|---|---|---|---|---|---|---|---|
| IOT9A/TCK | I/O | 0 | TCK | True_of_IOT9B | none | none | 9 | A7 | A4 | D2 |
| IOT9B/TMS | I/O | 0 | TMS | Comp_of_IOT9A | none | none | 8 | B7 | B4 | C2 |
| CKN | DIO | 6 | | Comp_of_CKP | none | none | | E2 | | |
| CKP | DIO | 6 | | True_of_CKN | none | none | | E1 | | |
| RX0N | DIO | 6 | | Comp_of_RX0P | none | none | | G2 | | |
| RX0P | DIO | 6 | | True_of_RX0N | none | none | | G1 | | |
| RX1N | DIO | 6 | | Comp_of_RX1P | none | none | | F2 | | |
| RX1P | DIO | 6 | | True_of_RX1N | none | none | | F1 | | |
| RX2N | DIO | 6 | | Comp_of_RX2P | none | none | | D2 | | |
| RX2P | DIO | 6 | | True_of_RX2N | none | none | | D1 | | |
| RX3N | DIO | 6 | | Comp_of_RX3P | none | none | | C2 | | |
| RX3P | DIO | 6 | | True_of_RX3N | none | none | | C1 | | |
| TXN | DIO | 6 | | Comp_of_TXP | none | none | | | | |
| TXP | DIO | 6 | | True_of_TXN | none | none | | | | |
| VCC | Power | N/A | | | | | 12 | | D4 | E5 |
| VCC | Power | N/A | | | | | | | | C3 |
| VCC | Power | N/A | | | | | | | | |
| VCC | Power | N/A | | | | | | | | |
| VCC/VCCIO1 | Power | N/A | | | | | | | | |
| VCC/VCCPLL | Power | N/A | | | | | | E5 | | |
| VCCD/VCCIO1/VCCIOD | Power | N/A | | | | | | | | |
| VCCD/VCCIOD | Power | N/A | | | | | | F4 | | |
| VCCIO0 | Power | N/A | | | | | 1 | D6 | A1 | C4 |
| VCCIO0 | Power | N/A | | | | | | | | |
| VCCIO0 | Power | N/A | | | | | | | | |
| VCCIO0/VCCIO2 | Power | N/A | | | | | | | | |
| VCCIO1/VCCIO2 | Power | N/A | | | | | | | D3 | |
| VCCIO1 | Power | N/A | | | | | 37 | E4 | | |
| VCCIO1/VCCX | Power | N/A | | | | | | | | C5 |
| VCCIO1/VCCX | Power | N/A | | | | | | | | E3 |
| VCCIO1/VCCX | Power | N/A | | | | | | | | |

**Note!**

[1] You can ignore the short-circuited pins.

[2] The pin is internally grounded.

| Pin Name | Function | BANK | Configuration Function | Differential Pair | LVDS | X16 | QN48 | CS100H | CS42 | CG56 |
|---|---|---|---|---|---|---|---|---|---|---|
| VCCIO2 | Power | N/A | | | | | | G6 | | E4 |
| VCCIO2 | Power | N/A | | | | | | | | |
| VCCIO2 | Power | N/A | | | | | | | | |
| VCCIO2/VCCX | Power | N/A | | | | | 36 | | | |
| VCCIO3 | Power | N/A | | | | | | G7 | | |
| VCCIO3/VCCIO4/VCCIO5 | Power | N/A | | | | | 25 | | C4 | D5 |
| VCCIO4 | Power | N/A | | | | | | F7 | | |
| VCCIO5 | Power | N/A | | | | | | E7 | | |
| VCCX | Power | N/A | | | | | | F5 | E3 | |
| VSS | Ground | N/A | | | | | 26 | E6 | E4 | D4 |
| VSS | Ground | N/A | | | | | 2 | F6 | C3 | D3 |
| VSS | Ground | N/A | | | | | | | | |
| VSS | Ground | N/A | | | | | | | | |
| VSS | Ground | N/A | | | | | | | | |
| VSS | Ground | N/A | | | | | | | | |
| VSS | Ground | N/A | | | | | | | | |
| VSS | Ground | N/A | | | | | | | | |
| VSS | Ground | N/A | | | | | | | | |
| VSS | Ground | N/A | | | | | | | | |
| VSS | Ground | N/A | | | | | | | | |
| VSS | Ground | N/A | | | | | | | | |
| VSS | Ground | N/A | | | | | | | | |
| VSS | Ground | N/A | | | | | | | | |
| NC | N/A | N/A | | | | | | | | |
| NC | N/A | N/A | | | | | | | | |

**Note!**

[1] You can ignore the short-circuited pins.

| Pin Name | Function | BANK | Configuration Function | Differential Pair | LVDS | X16 | QN48 | CS100H | CS42 | CG56 |
|---|---|---|---|---|---|---|---|---|---|---|
| **BANK5 True LVDS Pair** | | | | | | | | | | |
| IOL4A/LPLL_T_fb | I/O | 5 | LPLL_T_fb | True_of_IOL4B | True | x16 | 15 | D9_L8A[1] | | B7 |
| IOL4B/LPLL_C_fb | I/O | 5 | LPLL_C_fb | Comp_of_IOL4A | True | none | 14 | E10 | | A7 |
| IOL6A/GCLKT_7 | I/O | 5 | GCLKT_7 | True_of_IOL6B | True | x16 | 18 | C10 | D5 | C7 |
| IOL6B/GCLKC_7 | I/O | 5 | GCLKC_7 | Comp_of_IOL6A | True | none | 19 | C9 | D6 | C6 |
| IOL8A | I/O | 5 | | True_of_IOL8B | True | x16 | | D10 | C5 | D7 |
| IOL8B | I/O | 5 | | Comp_of_IOL8A | True | none | | D9 | C6 | D6 |
| **BANK4 True LVDS Pair** | | | | | | | | | | |
| IOL11A | I/O | 4 | | True_of_IOL11B | True | x16 | 20 | G9 | | E6 |
| IOL11B | I/O | 4 | | Comp_of_IOL11A | True | none | 21 | G10 | | E7 |
| IOL13A | I/O | 4 | | True_of_IOL13B | True | x16 | | E10_L11A[1] | E5 | F7 |
| IOL13B | I/O | 4 | | Comp_of_IOL13A | True | none | | D10_L11B[1] | E6 | F6 |
| **BANK3 True LVDS Pair** | | | | | | | | | | |
| IOL15A | I/O | 3 | | True_of_IOL15B | True | x16 | 23 | G10_L15A[1] | F5 | G7 |
| IOL15B | I/O | 3 | | Comp_of_IOL15A | True | none | 22 | E9 | F6 | G6 |
| IOL17A | I/O | 3 | | True_of_IOL17B | True | x16 | 27 | E9_L17A[1] | G5 | H7 |
| IOL17B | I/O | 3 | | Comp_of_IOL17A | True | none | 24 | G9_L17B[1] | G6 | H6 |
| **BANK2 True LVDS Pair** | | | | | | | | | | |
| IOB11A | I/O | 2 | | True_of_IOB11B | True | x16 | | K5 | E1 | F1 |
| IOB11B | I/O | 2 | | Comp_of_IOB11A | True | none | | J5 | E2 | F2 |
| IOB13A | I/O | 2 | | True_of_IOB13B | True | x16 | 33 | K4 | F1 | H3 |
| IOB13B | I/O | 2 | | Comp_of_IOB13A | True | none | 32 | J4 | F2 | G3 |
| IOB15A | I/O | 2 | | True_of_IOB15B | True | x16 | | H4 | G1 | G1 |
| IOB15B | I/O | 2 | | Comp_of_IOB15A | True | none | | G4 | G2 | G2 |
| IOB17A | I/O | 2 | | True_of_IOB17B | True | x16 | | K10 | | |
| IOB17B | I/O | 2 | | Comp_of_IOB17A | True | none | | J10 | | |
| IOB2A | I/O | 2 | | True_of_IOB2B | True | x16 | | | | G5 |
| IOB2B | I/O | 2 | | Comp_of_IOB2A | True | none | | H8 | | F5 |
| IOB4A | I/O | 2 | | True_of_IOB4B | True | x16 | | K8 | | |
| IOB4B | I/O | 2 | | Comp_of_IOB4A | True | none | | J8 | | |
| IOB6A | I/O | 2 | | True_of_IOB6B | True | x16 | | H7 | C1 | H4 |

**Note!**

[1] You can ignore the short-circuited pins.

| Pin Name | Function | BANK | Configuration Function | Differential Pair | LVDS | X16 | QN48 | CS100H | CS42 | CG56 |
|---|---|---|---|---|---|---|---|---|---|---|
| IOB6B | I/O | 2 | | Comp_of_IOB6A | True | none | | H6 | C2 | G4 |
| IOB8A | I/O | 2 | | True_of_IOB8B | True | x16 | | H5 | | |
| IOB8B | I/O | 2 | | Comp_of_IOB8A | True | none | | G5 | | |
| **BANK1 True LVDS Pair** | | | | | | | | | | |
| IOR11A/GCLKT_2 | I/O | 1 | GCLKT_2 | True_of_IOR11B | True | none | 41 | G3 | | |
| IOR11B/GCLKC_2 | I/O | 1 | GCLKC_2 | Comp_of_IOR11A | True | none | 40 | F3 | | |
| IOR13A | I/O | 1 | | True_of_IOR13B | True | none | 38 | H1 | | |
| IOR13B | I/O | 1 | | Comp_of_IOR13A | True | none | 39 | H2 | | |
| IOR15A | I/O | 1 | | True_of_IOR15B | True | none | | J1 | | |
| IOR15B | I/O | 1 | | Comp_of_IOR15A | True | none | | J2 | | |
| IOR17A | I/O | 1 | | True_of_IOR17B | True | none | | K1 | | |
| IOR17B | I/O | 1 | | Comp_of_IOR17A | True | none | | K2 | | |
| IOR1A | I/O | 1 | | True_of_IOR1B | True | none | 47 | A1 | | |
| IOR1B | I/O | 1 | | Comp_of_IOR1A | True | none | 46 | A2 | | |
| IOR3A/D2 | I/O | 1 | D2 | True_of_IOR3B | True | none | 45 | B1 | | |
| IOR3B/D3 | I/O | 1 | D3 | Comp_of_IOR3A | True | none | 44 | B2 | | |
| IOR5A/MI/D7 | I/O | 1 | MI/D7 | True_of_IOR5B | True | none | 43 | C3 | | |
| IOR5B/MO/D6 | I/O | 1 | MO/D6 | Comp_of_IOR5A | True | none | 42 | D4 | | |
| **BANK0 True LVDS Pair** | | | | | | | | | | |
| IOT11A/GCLKT_0 | I/O | 0 | GCLKT_0 | True_of_IOT11B | True | x16 | 6 | D7 | A3 | C1 |
| IOT11B/GCLKC_0 | I/O | 0 | GCLKC_0 | Comp_of_IOT11A | True | none | 7 | B6 | B3 | D1 |
| IOT13A | I/O | 0 | | True_of_IOT13B | True | x16 | | A6 | B2 | |
| IOT13B | I/O | 0 | | Comp_of_IOT13A | True | none | | A4 | B1 | |
| IOT15A | I/O | 0 | | True_of_IOT15B | True | x16 | | B4 | | |
| IOT15B | I/O | 0 | | Comp_of_IOT15A | True | none | | A6_T15B[1] | | |
| IOT17A | I/O | 0 | | True_of_IOT17B | True | x16 | | A4_T17A[1] | | |
| IOT17B | I/O | 0 | | Comp_of_IOT17A | True | none | | B4_T17B[1] | | |
| IOT4A | I/O | 0 | | True_of_IOT4B | True | x16 | | | B5 | A5 |
| IOT4B | I/O | 0 | | Comp_of_IOT4A | True | none | | | | A6 |
| IOT6A | I/O | 0 | | True_of_IOT6B | True | x16 | | A9 | | |
| IOT6B | I/O | 0 | | Comp_of_IOT6A | True | none | | B9 | | |

**Note!**
[1] You can ignore the short-circuited pins.

| Pin Name | Function | BANK | Configuration Function | Differential Pair | LVDS | X16 | QN48 | CS100H | CS42 | CG56 |
|---|---|---|---|---|---|---|---|---|---|---|
| IOT8A | I/O | 0 | | True_of_IOT8B | True | x16 | | C8 | | |
| IOT8B | I/O | 0 | | Comp_of_IOT8A | True | none | | D8 | | |