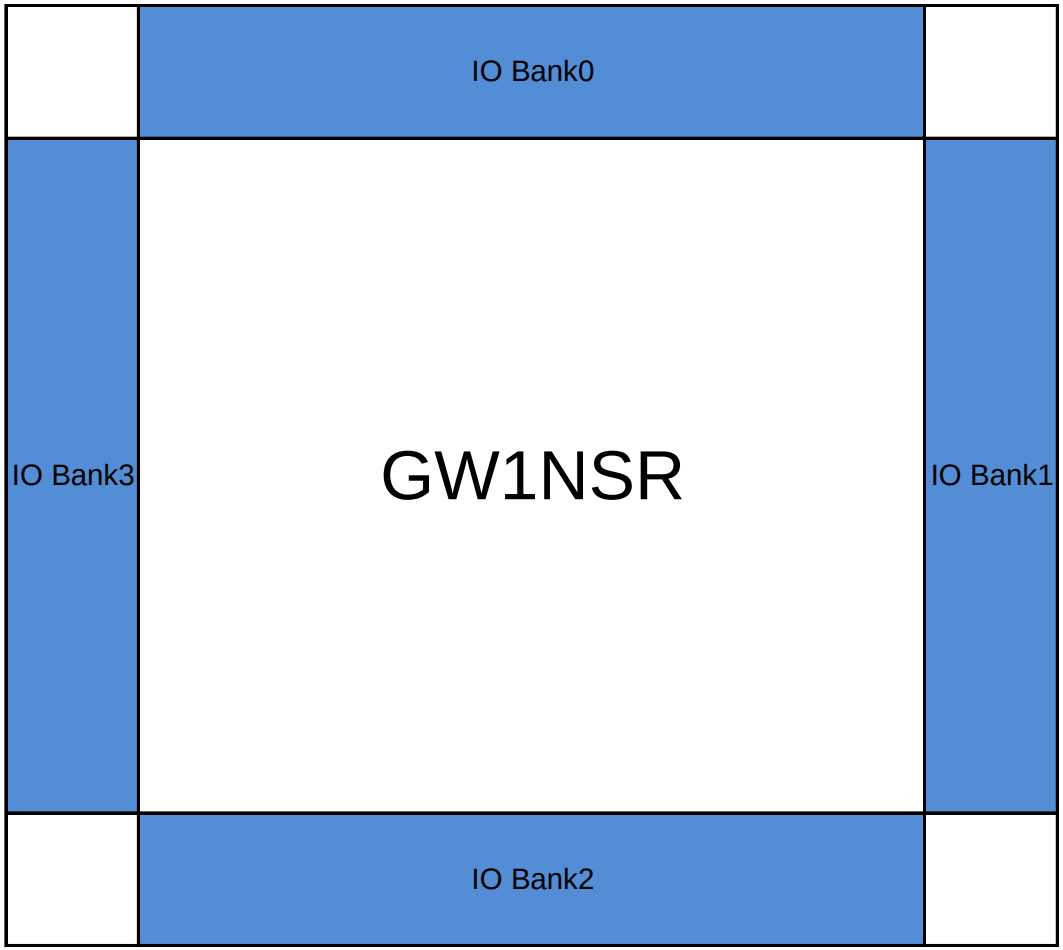
Data	Version	Description
01/03/2019	1.0E	Initial version published.
06/30/2020	1.01E	The package name of "QN48" corrected as "QN48P".

Pins Name	Direction	Description
User I/O Pins		
IO [End][Row/Column Number][A/B]	I/O	[End] indicates the pin location, including L(left) R(right) B(bottom), and T(top)
		[Row/Column Number] indicates the pin Row/Column number. If [End] is T(top) or B(bottom), the pin indicates the Column number of the corresponding CFU. If [End] is L(left) or R(right), the pin indicates the Row number of the corresponding CFU.
		[A/B] indicaties differential signal pair information.
Multi-Function Pins		
IO [End][Row/Column Number][A/B]/MMM		/MMM represents one or more of the other functions in addition to being general purpose user I/O. When not used for the specical functions, these pins can be user I/O.
RECONFIG_N	I,Internal Weak Pull Up	Starat new GowinCONFIG mode when low pulse
READY	I/O	When high, device can be programmed and configured
		When low, device cannot be programmed and configured
DONE	I/O	High indicates successful completion of programming and configuration
		Low indicates unfinished or failure of programming and configuration
FASTRD_N/D3	I/O	In MSPI mode, FASTRD_N is used as Flash access speed port.
		Data port D3 in CPU mode
MCLK/D4	I/O	Clock output MCLK in MSPI mode
		Data port D4 in CPU mode
MCS_N/D5	I/O	Enable signal MCS_N in MSPI mode, active-low
		Data port D5 in CPU mode
MO/D6	I/O	MOSI in MSPI mode:Master data output/Slave data input
		Data port D6 in CPU mode
MI/D7	I/O	MISO in MSPI mode:Master data input/Slave data output
		Data port D7 in CPU mode
SSPI_CS_N/D0	I/O	Enable signal SSPI_CS_N in SSPI mode, active-low
		Data port D0 in CPU mode
SO/D1	I/O	MISO in MSPI mode:Master data input/Slave data output
		Data port D1 in CPU mode
SI/D2	I/O	MOSI in SSPI mode:Master data output/Slave data input
		Data port D2 in CPU mode
TMS	I	Serial mode input in JTAG mode

Pins Name	Direction	Description
TCK	I	Serial clock input in JTAG mode
TDI	I	Serial data input in JTAG mode
TDO	O	Serial data output in JTAG mode
JTAGSEL_N	I, Internal Weak Pull Up	JTAG mode selection, active-low
SCLK	I	Clock input in SSPI, SERIAL, and CPU modes
DIN	I, Internal Weak Pull Up	Data input in SERIAL mode
DOUT	O	Data output in SERIAL mode
CLKHOLD_N	I, Internal Weak Pull Up	High, SCLK will be connected internally in SSPI mode or CPU mode
		Low, SCLK will be disconnected from SSPI mode or CPU mode
WE_N	I	Select data input/output of D[7:0] in CPU mode
GCLKT_[x]	I	Pins for Global clock input, T(True), [x]:global clock number.
GCLKC_[x]	I	Differential comparation input pin of GCLKT_[x], C(Comp), [x]: global clock No.[1].
LPLL_T_fb/RPLL_T_fb	I	L/R PLL feedback the input pins, T(True)
LPLL_C_fb/RPLL_C_fb	I	L/R PLL feedback the input pins, C(Comp)
LPLL_T_in/RPLL_T_in	I	L/R PLL clock input pins,T(True)
LPLL_C_in/RPLL_C_in	I	L/R PLL clock input pins, C(Comp)
CH[7:0]	I	Eight-channel analog input
MODE2	I,Internal Weak Pull Up	GowinCONFIG modes selection pin; if this pin is not bonded, it's internal grounded.
MODE1	I,Internal Weak Pull Up	GowinCONFIG modes selection pin; if this pin is not bonded, it's internal grounded.
MODE0	I,Internal Weak Pull Up	GowinCONFIG modes selection pin; if this pin is not bonded, it's internal grounded.
Other Pins		
NC	NA	Reserved.
VSS	NA	Ground.
VCC	NA	Power supply pins for the internal core logic.
VCCO#	NA	Power supply pins for I/O voltage of I/O BANK#.
VCCX	NA	Power supply pins for auxiliary voltage.
VCCP	NA	Power supply pins for FLASH (1.8V).

Pins Name	Direction	Description
VCCPLL	NA	Power supply pins for PLL.
VDDA	NA	ADC Analog power supply voltage, VDDA=3.3V
X16	NA	I/O supports 16:1.
VREF	NA	The input pin of ADC external reference voltage.
Note! [1]When the input is not single-ended, the GLKC_[x] pin is not a global clock pin.		



Note！

1.Each Bank has independent reference volatge (VREF);

2.Users can select to use internal VREF of IOB (equals to 0.5*VCCO) or external VREF input (use any IO pins as external VREF input).

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	QN48P
IOB10A/GCLKT_5	I/O	2	GCLKT_5	True_of_IOB10B	NONE	NONE	17
IOB10B/GCLKC_5	I/O	2	GCLKC_5	Comp_of_IOB10A	NONE	NONE	18
IOB11A/GCLKT_4	I/O	2	GCLKT_4	True_of_IOB11B	TRUE	x16	19
IOB11B/GCLKC_4	I/O	2	GCLKC_4	Comp_of_IOB11A	TRUE	NONE	20
IOB12A	I/O	2		True_of_IOB12B	NONE	NONE	
IOB12B	I/O	2		Comp_of_IOB12A	NONE	NONE	
IOB13A	I/O	2		True_of_IOB13B	TRUE	x16	21
IOB13B	I/O	2		Comp_of_IOB13A	TRUE	NONE	22
IOB14A	I/O	2		True_of_IOB14B	NONE	NONE	
IOB14B	I/O	2		Comp_of_IOB14A	NONE	NONE	
IOB15A	I/O	2		True_of_IOB15B	TRUE	x16	23
IOB15B	I/O	2		Comp_of_IOB15A	TRUE	NONE	24
IOB16A	I/O	2		True_of_IOB16B	NONE	NONE	
IOB16B	I/O	2		Comp_of_IOB16A	NONE	NONE	
IOB17A	I/O	2		True_of_IOB17B	TRUE	x16	
IOB17B	I/O	2		Comp_of_IOB17A	TRUE	NONE	
IOB18A	I/O	2		True_of_IOB18B	NONE	NONE	
IOB18B	I/O	2		Comp_of_IOB18A	NONE	NONE	
IOB19A	I/O	2		True_of_IOB19B	NONE	NONE	
IOB19B	I/O	2		Comp_of_IOB19A	NONE	NONE	
IOB7A	I/O	2		True_of_IOB7B	TRUE	x16	
IOB7B	I/O	2		Comp_of_IOB7A	TRUE	NONE	14
IOB8A	I/O	2		True_of_IOB8B	NONE	NONE	
IOB8B	I/O	2		Comp_of_IOB8A	NONE	NONE	
IOB9A	I/O	2		True_of_IOB9B	TRUE	x16	15
IOB9B	I/O	2		Comp_of_IOB9A	TRUE	NONE	16
IOL2A/JTAGSEL_N/VREF	I/O	3	JTAGSEL_N/VREF	True_of_IOL2B	TRUE	NONE	3
IOL2B	I/O	3		Comp_of_IOL2A	TRUE	NONE	
IOL3A	I/O	3		True_of_IOL3B	NONE	NONE	
IOL3B	I/O	3		Comp_of_IOL3A	NONE	NONE	
IOL4A	I/O	3		True_of_IOL4B	TRUE	NONE	
IOL4B	I/O	3		Comp_of_IOL4A	TRUE	NONE	
IOL5A/GCLKT_7	I/O	3	GCLKT_7	True_of_IOL5B	NONE	NONE	

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	QN48P
IOL5B/GCLKC_7	I/O	3	GCLKC_7	Comp_of_IOL5A	NONE	NONE	
IOL6A/TMS	I/O	3	TMS	True_of_IOL6B	NONE	NONE	4
IOL6B/TCK	I/O	3	TCK	Comp_of_IOL6A	NONE	NONE	5
IOL6C/SCLK	I/O	3	SCLK	True_of_IOL6D	NONE	NONE	
IOL6D/TDI	I/O	3	TDI	Comp_of_IOL6C	NONE	NONE	6
IOL6E/TDO	I/O	3	TDO	True_of_IOL6F	NONE	NONE	7
IOL6F/RECONFIG_N	I/O	3	RECONFIG_N	Comp_of_IOL6E	NONE	NONE	
IOL6G/DONE	I/O	3	DONE	True_of_IOL6H	NONE	NONE	9
IOL6H/READY	I/O	3	READY	Comp_of_IOL6G	NONE	NONE	
IOL6I	I/O	3		True_of_IOL6J	NONE	NONE	
IOL6J	I/O	3		Comp_of_IOL6I	NONE	NONE	
IOL7A/GCLKT_6	I/O	3	GCLKT_6	True_of_IOL7B	TRUE	NONE	10
IOL7B/GCLKC_6	I/O	3	GCLKC_6	Comp_of_IOL7A	TRUE	NONE	11
IOL8A	I/O	3		True_of_IOL8B	NONE	NONE	
IOL8B	I/O	3		Comp_of_IOL8A	NONE	NONE	
IOL9A	I/O	3		True_of_IOL9B	NONE	NONE	
IOL9B	I/O	3		Comp_of_IOL9A	NONE	NONE	
IOR2A/RPLL_T_fb	I/O	1	RPLL_T_fb	True_of_IOR2B	TRUE	NONE	
IOR2B/RPLL_C_fb	I/O	1	RPLL_C_fb	Comp_of_IOR2A	TRUE	NONE	
IOR3A/GCLKT_2/RPLL_T_in	I/O	1	GCLKT_2/RPLL_T_in	True_of_IOR3B	NONE	NONE	35
IOR3B/GCLKC_2/RPLL_C_in	I/O	1	GCLKC_2/RPLL_C_in	Comp_of_IOR3A	NONE	NONE	
IOR4A/MI/D7	I/O	1	MI/D7	True_of_IOR4B	TRUE	NONE	33
IOR4B/MO/D6	I/O	1	MO/D6	Comp_of_IOR4A	TRUE	NONE	34
IOR5A/MCS_N/D5	I/O	1	MCS_N/D5	True_of_IOR5B	NONE	NONE	
IOR5B/MCLK/D4	I/O	1	MCLK/D4	Comp_of_IOR5A	NONE	NONE	
IOR6A/FASTRD_N/D3	I/O	1	FASTRD_N/D3	True_of_IOR6B	NONE	NONE	
IOR6B/SI/D2	I/O	1	SI/D2	Comp_of_IOR6A	NONE	NONE	
IOR7A/SO/D1	I/O	1	SO/D1	True_of_IOR7B	TRUE	NONE	32
IOR7B/SSPI_CS_N/D0	I/O	1	SSPI_CS_N/D0	Comp_of_IOR7A	TRUE	NONE	31
IOR8A/DIN/CLKHOLD_N	I/O	1	DIN/CLKHOLD_N	True_of_IOR8B	NONE	NONE	29
IOR8B/DOUT/WE_N	I/O	1	DOUT/WE_N	Comp_of_IOR8A	NONE	NONE	30
IOR9A/GCLKT_3	I/O	1	GCLKT_3	True_of_IOR9B	NONE	NONE	28
IOR9B/GCLKC_3	I/O	1	GCLKC_3	Comp_of_IOR9A	NONE	NONE	27

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	QN48P
IOT10A/GCLKT_0	I/O	0	GCLKT_0	True_of_IOT10B	NONE	NONE	
IOT10B/GCLKC_0	I/O	0	GCLKC_0	Comp_of_IOT10A	NONE	NONE	
IOT11A/GCLKT_1	I/O	0	GCLKT_1	True_of_IOT11B	NONE	x16	
IOT11B/GCLKC_1	I/O	0	GCLKC_1	Comp_of_IOT11A	NONE	NONE	
IOT12A	I/O	0		True_of_IOT12B	NONE	NONE	
IOT12B	I/O	0		Comp_of_IOT12A	NONE	NONE	
IOT13A	I/O	0		True_of_IOT13B	NONE	x16	39
IOT13B	I/O	0		Comp_of_IOT13A	NONE	NONE	38
IOT14A	I/O	0		True_of_IOT14B	NONE	NONE	
IOT14B	I/O	0		Comp_of_IOT14A	NONE	NONE	
IOT15A	I/O	0		True_of_IOT15B	NONE	x16	
IOT15B	I/O	0		Comp_of_IOT15A	NONE	NONE	
IOT16A	I/O	0		True_of_IOT16B	NONE	NONE	
IOT16B	I/O	0		Comp_of_IOT16A	NONE	NONE	
IOT17A	I/O	0		True_of_IOT17B	NONE	x16	
IOT17B	I/O	0		Comp_of_IOT17A	NONE	NONE	
IOT18A	I/O	0		True_of_IOT18B	NONE	NONE	
IOT18B	I/O	0		Comp_of_IOT18A	NONE	NONE	
IOT19A	I/O	0		True_of_IOT19B	NONE	NONE	
IOT19B	I/O	0		Comp_of_IOT19A	NONE	NONE	
IOT2A	I/O	0		True_of_IOT2B	NONE	x16	
IOT2B/MODE0	I/O	0	MODE0	Comp_of_IOT2A	NONE	NONE	
IOT3A/MODE2	I/O	0	MODE2	True_of_IOT3B	NONE	NONE	48
IOT3B/MODE1	I/O	0	MODE1	Comp_of_IOT3A	NONE	NONE	
IOT4A/CH0	I/O	0	CH0	True_of_IOT4B	NONE	x16	47
IOT4B/CH1	I/O	0	CH1	Comp_of_IOT4A	NONE	NONE	46
IOT5A/CH2	I/O	0	CH2	True_of_IOT5B	NONE	NONE	45
IOT5B/CH3	I/O	0	CH3	Comp_of_IOT5A	NONE	NONE	44
IOT6A/CH4	I/O	0	CH4	True_of_IOT6B	NONE	x16	43
IOT6B/CH5	I/O	0	CH5	Comp_of_IOT6A	NONE	NONE	42
IOT7A/CH6	I/O	0	CH6	True_of_IOT7B	NONE	NONE	41
IOT7B/CH7	I/O	0	CH7	Comp_of_IOT7A	NONE	NONE	40
IOT8A	I/O	0		True_of_IOT8B	NONE	x16	

Pin List

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	QN48P
IOT8B	I/O	0		Comp_of_IOT8A	NONE	NONE	
IOT9A	I/O	0		True_of_IOT9B	NONE	NONE	
IOT9B	I/O	0		Comp_of_IOT9A	NONE	NONE	
VCC/VCCPLL	Power	N/A				NONE	12
VCC/VCCPLL	Power	N/A				NONE	37
VCCO1	Power	N/A				NONE	25
VCCO2	Power	N/A				NONE	13
VCCX	Power	N/A				NONE	8
VCCX	Power	N/A				NONE	36
VCCO0/VCCO3	Power	N/A				NONE	1
VSS	Ground	N/A				NONE	2
VSS	Ground	N/A				NONE	26

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	QN48P
BANK3 True LVDS Pair							
IOL7A/GCLKT_6	I/O	3	GCLKT_6	True_of_IOL7B	TRUE	NONE	10
IOL7B/GCLKC_6	I/O	3	GCLKC_6	Comp_of_IOL7A	TRUE	NONE	11
BANK2 True LVDS Pair							
IOB9A	I/O	2		True_of_IOB9B	TRUE	x16	15
IOB9B	I/O	2		Comp_of_IOB9A	TRUE	NONE	16
IOB11A/GCLKT_4	I/O	2	GCLKT_4	True_of_IOB11B	TRUE	x16	19
IOB11B/GCLKC_4	I/O	2	GCLKC_4	Comp_of_IOB11A	TRUE	NONE	20
IOB13A	I/O	2		True_of_IOB13B	TRUE	x16	21
IOB13B	I/O	2		Comp_of_IOB13A	TRUE	NONE	22
IOB15A	I/O	2		True_of_IOB15B	TRUE	x16	23
IOB15B	I/O	2		Comp_of_IOB15A	TRUE	NONE	24
BANK1 True LVDS Pair							
IOR7B/SSPI_CS_N/D0	I/O	1	SSPI_CS_N/D0	Comp_of_IOR7A	TRUE	NONE	31
IOR7A/SO/D1	I/O	1	SO/D1	True_of_IOR7B	TRUE	NONE	32
IOR4A/MI/D7	I/O	1	MI/D7	True_of_IOR4B	TRUE	NONE	33
IOR4B/MO/D6	I/O	1	MO/D6	Comp_of_IOR4A	TRUE	NONE	34

Note!
It is recommended to connect VCCX to the VCCO with the Max. voltage.

Recommended Operating Conditions for GW1NSR-2/GW1NSR-2C QN48P Packages			
Name	**Description**	**Min.**	**Max.**
VCC	Core volatge	1.14V	1.26V
VCCO1, VCCO2	I/O Bank volatge	1.14V	3.465V
	VCCO2 needs to be supplied with 1.2V when BANK2 MIPI output is employed.	1.14V	1.26V
VCCO0/VCCO3	VCCO0/VCCO3 are internal short circuited, when ADC is employed.	3.135V	3.465V
	VCCO0/VCCO3 are internal short circuited. When PSRAM is employed, VCCO0 provides power to PSRAM.	1.71V	1.89V
VCCX	LX auxiliary voltage	1.71V	1.89V
	UX auxiliary voltage	2.375V	3.465V
	When USB2.0 PHY is employed, VCCX needs to be supplied with 3.3V. LX version devices do not support USB2.0 PHY.	3.135V	3.465V