GW1NSR series of FPGA Products

Package & Pinout User Guide

UG823-1.5E, 10/18/2022

Disclaimer

GOWINSEMI assumes no liability and provides no warranty (either expressed or implied) and is not responsible for any damage incurred to your hardware, software, data, or property resulting from usage of the materials or intellectual property except as outlined in the GOWINSEMI Terms and Conditions of Sale. GOWINSEMI may make changes to this document at any time without prior notice. Anyone relying on this documentation should contact GOWINSEMI for the current documentation and errata.

Revision History

Date	Version	Description
10/29/2018	1.0E	Initial version published.
12/24/2018	1.1 E	IO bank description updated.
10/15/2019	1.2E	Devices of GW1NSR-4/GW1NSR-4C added.
03/11/2020	1.3E	MG64P package outline updated.
04/16/2020	1.4E	The pin distribution view and pin number of GW1NSR-4/GW1NSR-4C QN48P updated.
06/30/2020	1.4.1E	The package name of GW1NS-2/2C QN48 (PSRAM embedded) corrected as QN48P.
10/18/2022	1.5E	• GW1NSR-2 and GW1NSR-2C removed. • Pin definitions updated.

Contents

List of Figures

List of Tables

1 About This Guide

1.1 Purpose

This manual contains an introduction to the GW1NSR series of FPGA products together with a definition of the pins, list of pin numbers, distribution of pins, and package diagrams.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

1. DS861, GW1NSR series of FPGA Products Data Sheet
2. UG290, Gowin FPGA Products Programming and Configuration User Guide
3. UG864, GW1NSR-4 Pinout
4. UG865, GW1NSR-4C Pinout

1.3 Abbreviations and Terminology

The abbreviations and terminology used in this manual are as shown in Table 1-1 below.

Table 1-1 Abbreviations and Terminology

Abbreviations and Terminology	Full Name
FPGA	Field Programmable Gate Array
MG64P	MBGA64P
QN48G	QFN48G
QN48P	QFN48P

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

GW1NSR series of FPGA products are the first-generation products in the LittleBee family. They integrate with PSRAM based on the GW1NS series. When the ARM Cortex-M3 hard-core processor is employed as the core, the needs of the Min. memory can be met. FPGA logic resources and other embedded resources can flexibly facilitate the peripheral control functions, which provide excellent calculation functions and exceptional system response interrupts. They also offer high performance, low power consumption, a small number of pins, flexible usage, instant start-up, affordability, nonvolatile, high security, and abundant package types, among other benefits. GW1NSR series of SoC FPFA products achieve seamless connection between programmable logic devices and embedded processors. They are compatible with multiple peripheral device standards and can, therefore, reduce costs of operation and be widely deployed in industrial control, communication, Internet of Things, servo drive, consumption fields, etc.

2.1 PB-Free Package

The GW1NSR series of FPGA products are PB free in line with the EU ROHS environmental directives. The substances used in the GW1NSR series of FPGA products are in full compliance with the IPC-1752 standards.

2.2 Package and Max. User I/O Information

Table 2-1 Package, Max. User I/O Information, and LVDS Paris

Package	Pitch(mm)	Size (mm)	GW1NSR-4	GW1NSR-4C
QN48P	0.4	6 x 6	-	39(4)
MG64P	0.5	4.2 x 4.2	55(8)	55(8)
QN48G	0.4	6 x 6	-	39(4)

Note!

- In this manual, abbreviations are employed to refer to the package types. See 1.3 Abbreviations and Terminology.
- The JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The data in this table is when the loaded four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O; When mode [2:0] = 001, JTAGSEL_N and the four JTAG pins (TCK, TDI, TDO, and TMS) can be used as GPIO simultaneously, and the Max. user I/O plus one.

2.3 Power Pin

Table 2-2 GW1NSR Power Pins

VCC	VCCO0	VCCO1	VCCO2
VCCO3	VCCX	VSS	NC
VCCPLL	VCCP	VDDA	–

2.4 Pin Quantity

2.4.1 Quantity of GW1NSR-4/GW1NSR-4C Pins

Table 2-3 Quantity of GW1NSR-4/GW1NSR-4C Pins

Pin Type		GW1NSR-4/GW1NSR-4C		
		QN48P (GW1NSR-4C)	QN48G (GW1NSR-4C)	MG64P
I/O Single end/ Differential pair/LVDS[1]	BANK0	8/3/0	8/3/0	9/4/0
	BANK1	10/5/0	10/5/0	28/14/0
	BANK2	9/4/4	9/4/4	18/9/8
	BANK3	11/5/0	11/5/0	0/0/0
Max. User I/O[2]		38	38	55
Differential Pair		17	17	37
True LVDS Output		4	4	8
VCC		2	2	1
VCCX		1	1	1
VCCO0		1	1	1
VCCO1		1	1	1
VCCO2		1	1	1
VCCO3		2	2	1
VSS		1	1	2
MODE0		0	0	0
MODE1		0	0	0
MODE2		0	0	0
MODE1/MODE2[3]		1	1	0
JTAGSEL_N		1	1	1

Note!

- [1] Single end/ Differential I/O quantity include CLK pins, and download pins;
- [2] The JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The data in this table is when the loaded four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O;
- [3] Pin multiplexing.

2.5 Pin Definitions

The location of the pins in the GW1NSR series of FPGA products varies according to the different packages.

Table 2-4 provides a detailed overview of user I/O, multi-function pins, dedicated pins, and other pins.

Table 2-4 Definition of the Pins in the GW1NSR series of FPGA products

Pin Name	I/O	Description
Max. User I/O		
IO[End][Row/Column Number][A/B]	I/O	[End] indicates the pin location, including L(left) R(right) B(bottom), and T(top). [Row/Column Number] indicates the pin Row/Column number.If [End] is T(top) or B(bottom), the pin indicates the column number of the corresponding CFU. If [End] is L(left) or R(right), the pin indicates the Row number of the corresponding CFU. [A/B] indicates differential signal pair information.
Multi-Function Pins		
IO[End][Row/Column Number][A/B]/MMM		/MMM represents one or more of the other functions in addition to being general purpose user I/O. These pins can be used as user I/O when the functions are not used.
D0	I/O	Data port D0 in CPU mode
D1	I/O	Data port D1 in CPU mode
D2	I/O	Data port D2 in CPU mode
D3	I/O	Data port D3 in CPU mode
D4	I/O	Data port D4 in CPU mode
D5	I/O	Data port D5 in CPU mode
D6	I/O	Data port D6 in CPU mode
D7	I/O	Data port D7 in CPU mode
WE_N	I	Select data input/output of D[7:0] in CPU mode.0: Write;1: Read.
DOUT	O	Data output in SERIAL mode
DIN	I, internal weak pull-up	Data input in SERIAL mode
TMS	I, internal weak pull-up	Serial mode input in JTAG mode
TCK	I	Serial clock input in JTAG mode
TDO	O	Serial data output in JTAG mode
TDI	I, internal weak pull-up	Serial data input in JTAG mode
JTAGSEL_N	I, internal weak pull-up	Reconfigure JTAG download function signal
FASTRD_N	I	Access SPI FLASH to select signal. Low, Fast Read mode; High, Read mode.
READY[1]	I/O	High, the device can be programmed and configured

Pin Name	I/O	Description
		currently; Low, the device cannot be programmed and configured currently.
DONE[1]	O	High, the programming configuration has been completed successfully; Low, the programming configuration has not been completed or failed.
	I	When the DONE signal is low, delay the chip to activate. Activate the chip until the DONE signal is high.
MI	O	MI in MSPI mode
MO	I	MO in MSPI mode
MCS_N	O	Enable signal MCS_N in MSPI mode, active-low.
MCLK	O	Clock output MCLK in MSPI mode, with default frequency of 2.5MHz.
SCLK	I	Clock input in SSPI, SERIAL, and CPU modes.
SO	O	SO in SSPI mode
SI	I/O	SI in SSPI mode
SSPI_CS_N	I/O	Enable signal SSPI_CS_N in SSPI mode, active-low, and internal weak pull-up
CLKHOLD_N	I, internal weak pull-up	High, the operation is efficient in SSPI mode or CPU mode; Low, the operation is inefficient in SSPI mode or CPU mode.
GCLKT_[x]	I	Pins in global clock input, T(True), [x]: global clock No.
GCLKC_[x]	I	Differential comparation input pin of GCLKT_[x], C(Comp), [x]: global clock No.[2].
LPLL_T_fb/RPLL_T_fb	I	L/R PLL feedback input pin, T(True).
LPLL_C_fb/RPLL_C_fb	I	L/R PLL feedback input pin, C(Comp).
LPLL_T_in/RPLL_T_in	I	L/R PLL clock input pin, T(True).
LPLL_C_in/RPLL_C_in	I	L/R PLL clock input pin, C(Comp).
CH[7:0]	I	Eight-channel analog input
MODE2	I, internal weak pull-up	GowinCONFIG modes selection pin; if this pin is not bonded, it's internal grounded.
MODE1	I, internal weak pull-up	GowinCONFIG modes selection pin; if this pin is not bonded, it's internal grounded.
MODE0	I, internal weak pull-up	GowinCONFIG modes selection pin; if this pin is not bonded, it's internal grounded.
Other Pins		
NC	NA	Reserved
VSS	NA	Ground pins
VCC	NA	Power supply pins for internal core logic.
VCCO#	NA	Power supply pins for the I/O voltage of I/O BANK#
VCCX	NA	Power supply pins for auxiliary voltage
VCCP	NA	FLASH Power supply pin (1.8V)

Pin Name	I/O	Description
VCCPLL	NA	Power supply pins in PLL
VDDA	NA	Analog power supply voltage, VDDA=3.3V.
X16	NA	Indicates IO supports 16:1 function
VREF	NA	ADC external reference voltage input pin

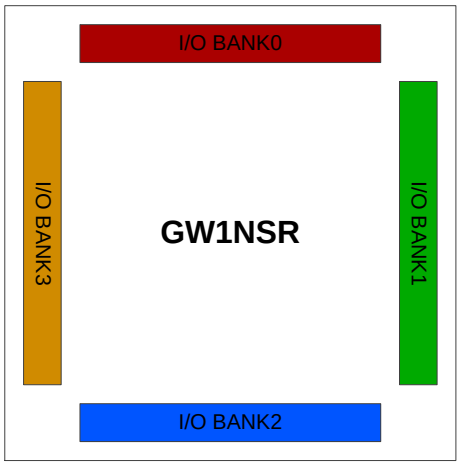
Note!

- [1] The default state of READY/DONE is open-drain output, internal weak pull-up. DONE outputs 0 during configuration.
- [2] When the input is not single-ended, the GLKC_[x] pin is not a global clock pin.

2.6 I/O BANK Introduction

There are two I/O Banks in the GW1NSR series of FPGA products. The I/O BANK Distribution of the GW1NSR series of FPGA products is as shown in Figure 2-1.

Figure 2-1 GW1NSR series I/O Bank Distribution



This manual provides an overview of the distribution view of the pins in the GW1NSR series of FPGA products. The eight I/O Banks that form the GW1NSR series of FPGA products are marked with eight different colors.

Various symbols are used for the user I/O, power, and ground. The various symbols and colors used for the various pins are defined as follows:

- "  " denotes the I/O in BANK0. The filling color changes with the BANK;
- "  " denotes the I/O in BANK1. The filling color changes with the BANK;
- "  " denotes the I/O in BANK2. The filling color changes with the BANK;
- "  " denotes the I/O in BANK3. The filling color changes with the BANK;

- "  " denotes VCC, VCCX, and VCCO. The filling color does not change;
- "  " denotes VSS, the filling color does not change;
- "  " denotes NC.

3 View of Pin Distribution

3.1 View of GW1NSR-4/GW1NSR-4C Pins Distribution

3.1.1 View of QN48P Pins Distribution

Figure 3-1 View of GW1NSR-4C QN48P Pins Distribution (Top View)

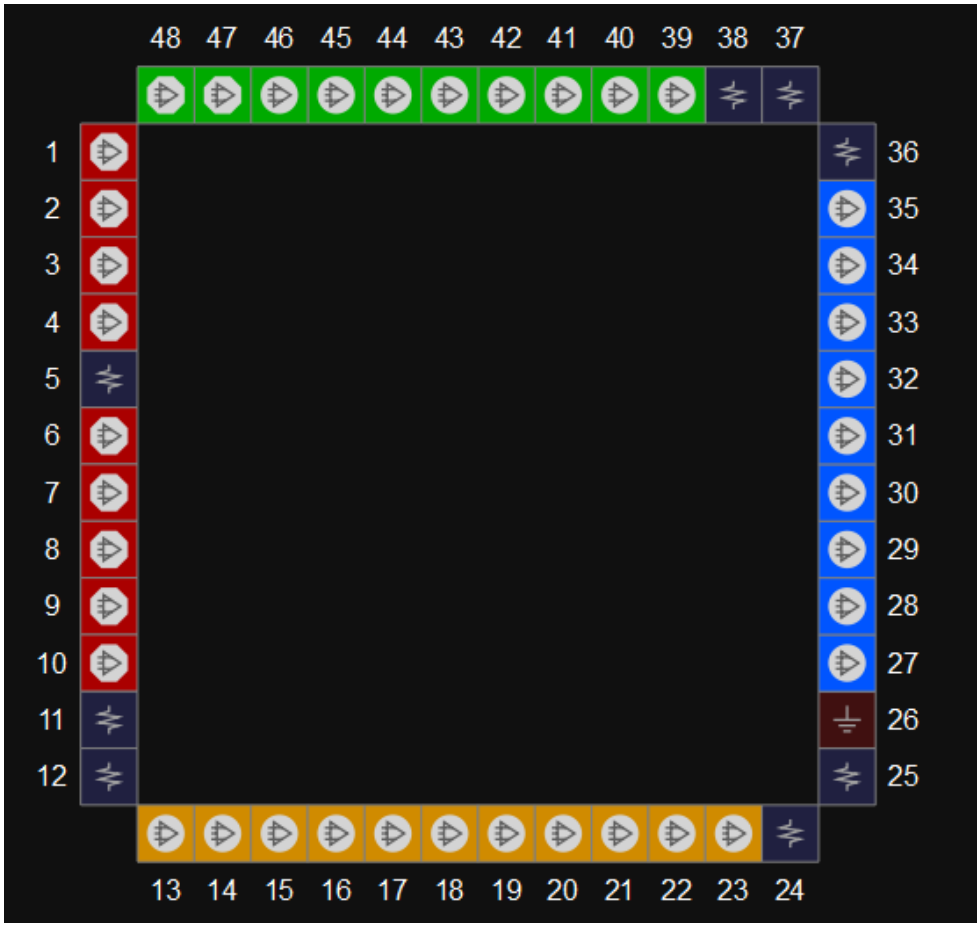


Table 3-1 Other Pins in GW1NSR-4C QN48P

VCC	11,37
VCCO0	5
VCCO1	38
VCCO2	36
VCCO3	12,24
VCCX	25
VSS	26

3.1.2 View of QN48G Pins Distribution

Figure 3-2 View of GW1NSR-4C QN48G Pins Distribution (Top View)

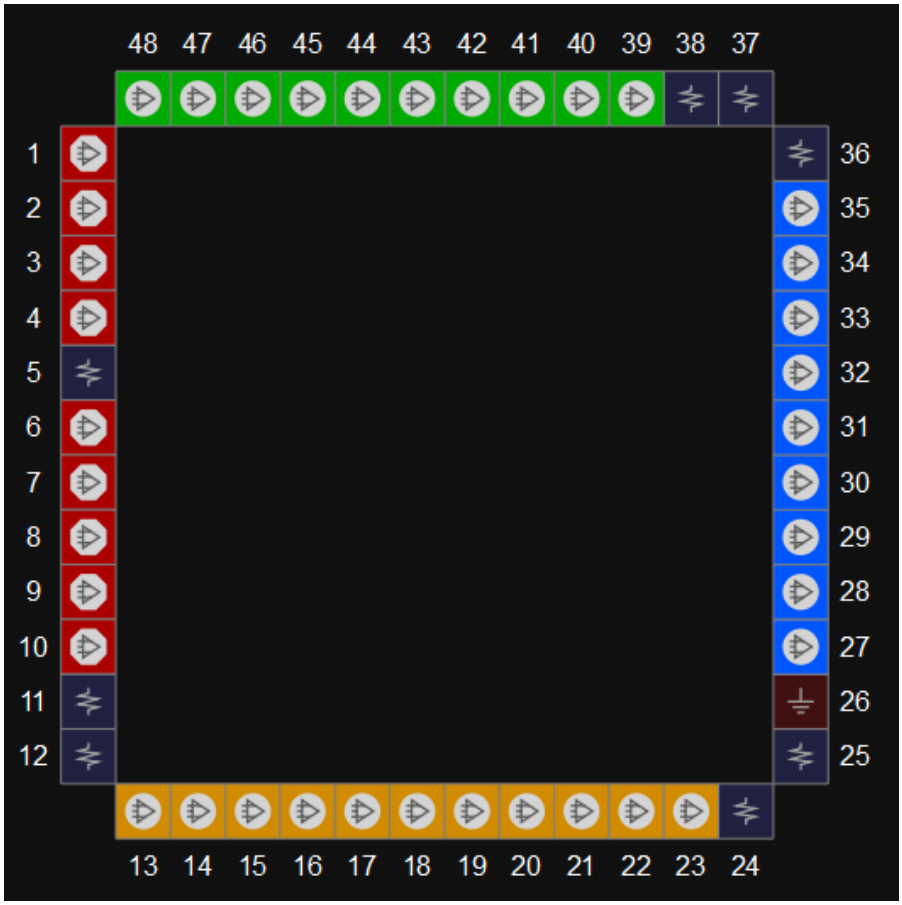


Table 3-2 Other Pins in GW1NSR-4C QN48G

VCC	11,37
VCCO0	5
VCCO1	38
VCCO2	36
VCCO3	12,24
VCCX	25
VSS	26

3.1.3 View of GW1NSR-4/GW1NSR-4C MG64P Pins Distribution

Figure 3-3 View of GW1NSR-4/GW1NSR-4C MG64P Pins Distribution (Top View)

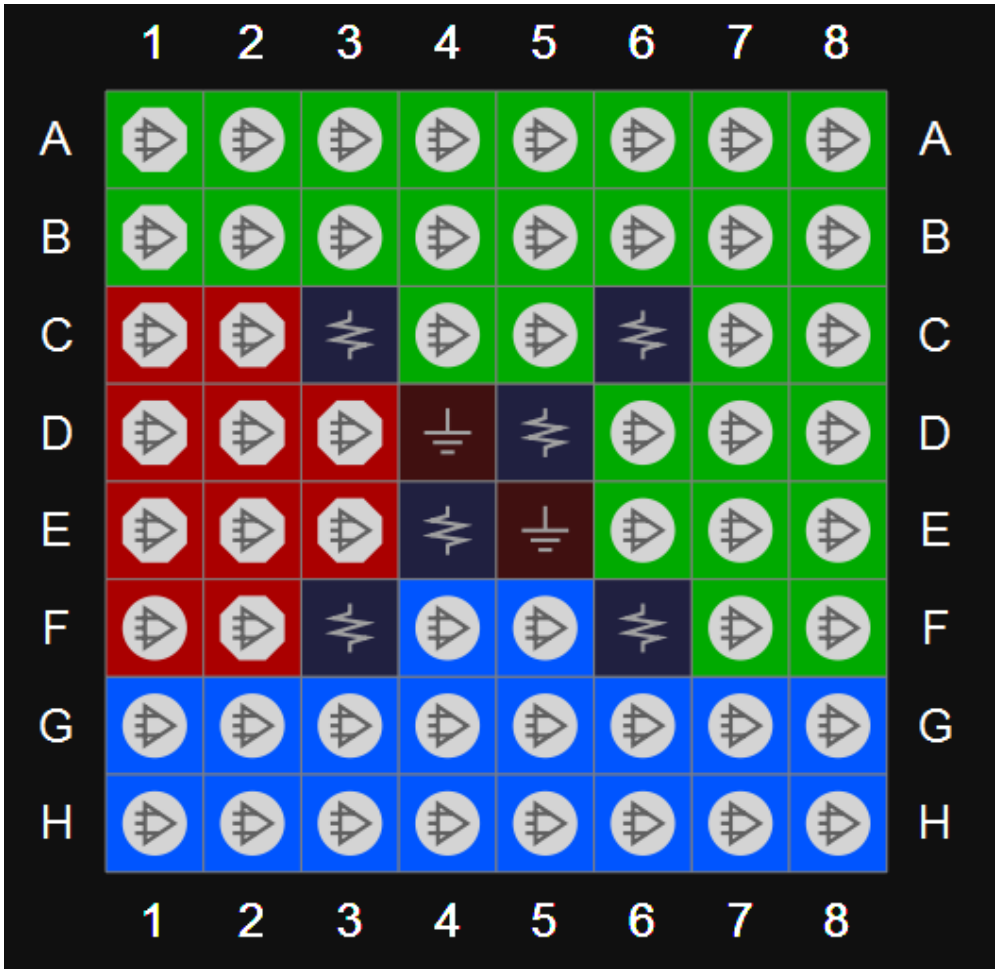


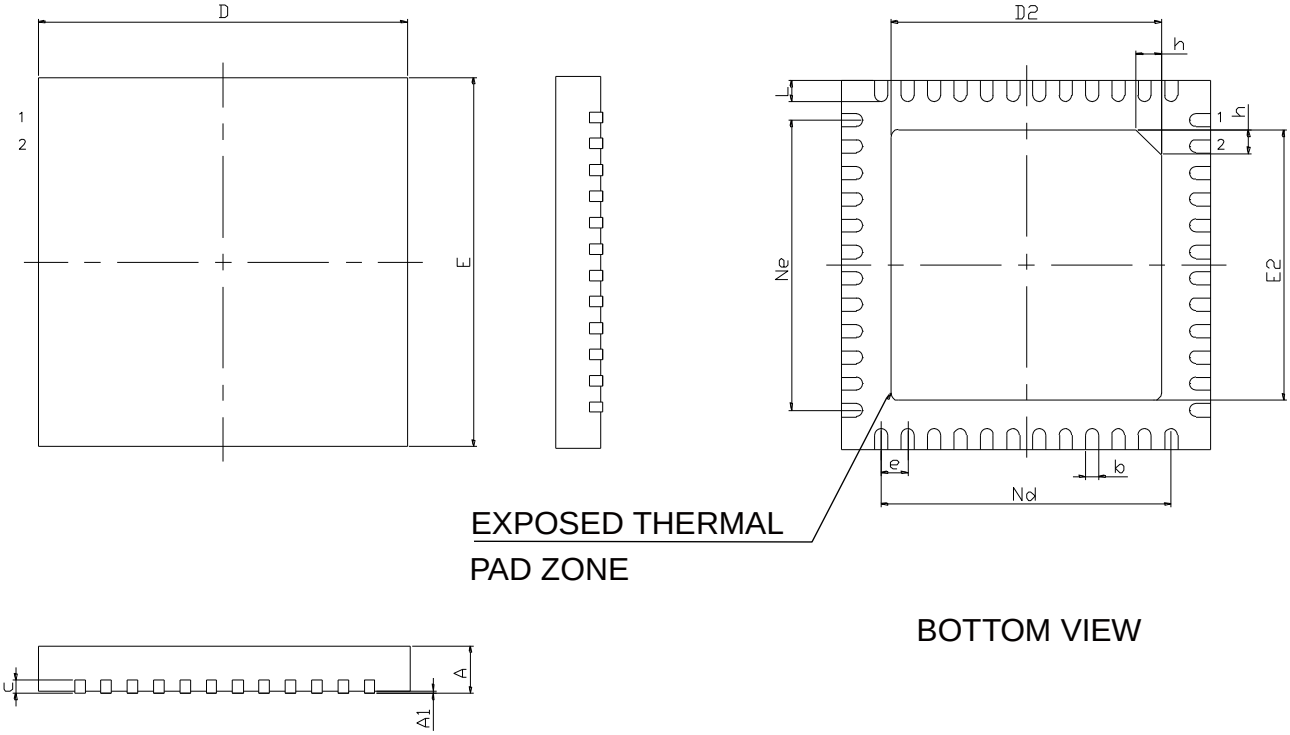
Table 3-3 Other Pins in GW1NSR-4/GW1NSR-4C MG64P

VCC	D5
VCCX	E4
VCCO0	C3
VCCO1	C6
VCCO2	F6
VCCO3	F3
VSS	D4,E5

4 Package Diagrams

4.1 GW1NSR-4C QN48P/QN48G Package Outline (6mm x 6mm)

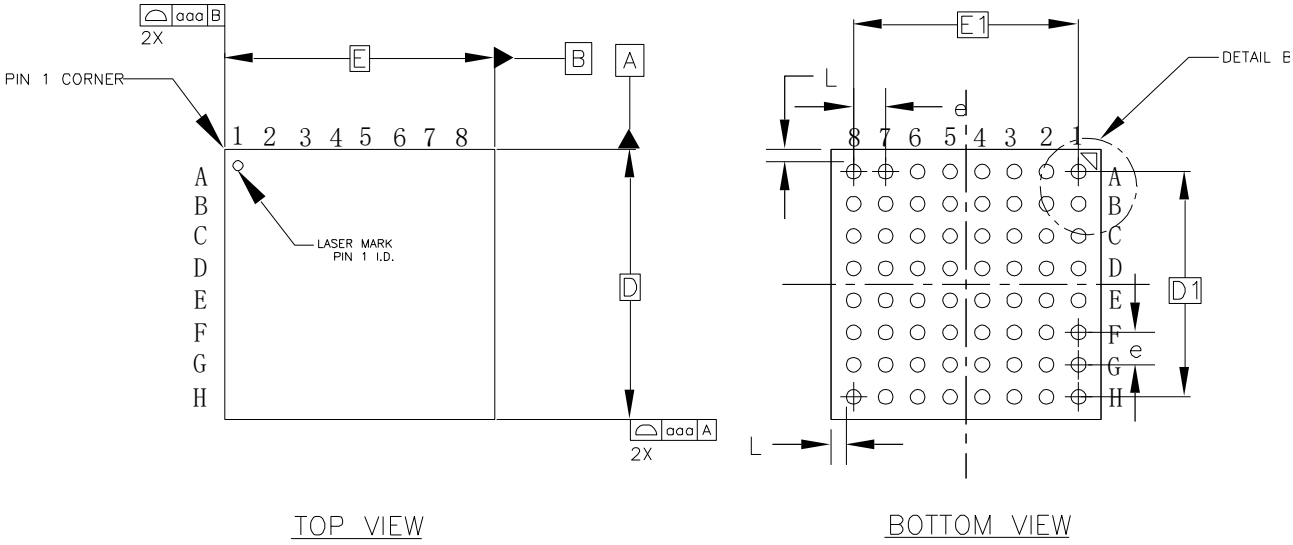
Figure 4-1 Package Outline QN48P/QN48G

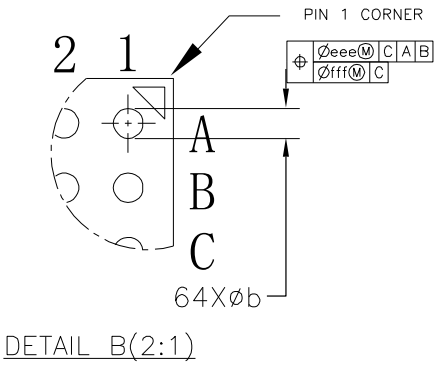


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.75	0.85	0.85
A1	—	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.23
D	5.90	6.00	6.10
D2	4.10	4.20	4.30
e	0.40BSC		
Ne	4.40BSC		
Nd	4.40BSC		
E	5.90	6.00	6.10
E2	4.10	4.20	4.30
L	0.35	0.40	0.45
h	0.30	0.35	0.40

4.2 GW1NSR-4/GW1NSR-4C MG64P Package Outline (4.2mm x 4.2mm)

Figure 4-2 Package Outline MG64P





SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.79	0.87	0.95
A1	0.11	0.16	0.21
A2	0.66	0.71	0.76
A3		0.53 BASIC	
c	0.15	0.18	0.21
D	4.10	4.20	4.30
D1		3.50 BASIC	
E	4.10	4.20	4.30
E1		3.50 BASIC	
e		0.50 BASIC	
b	0.18	0.23	0.28
L		0.235 REF	
aaa		0.15	
ccc		0.10	
ddd		0.10	
eee		0.15	
fff		0.05	


GOWIN
PROGRAMMING FOR THE FUTURE