Date	Version	Description
06/21/2019	1.0E	Initial version published.
11/19/2021	1.1E	Pin definitions updated. Power updated.

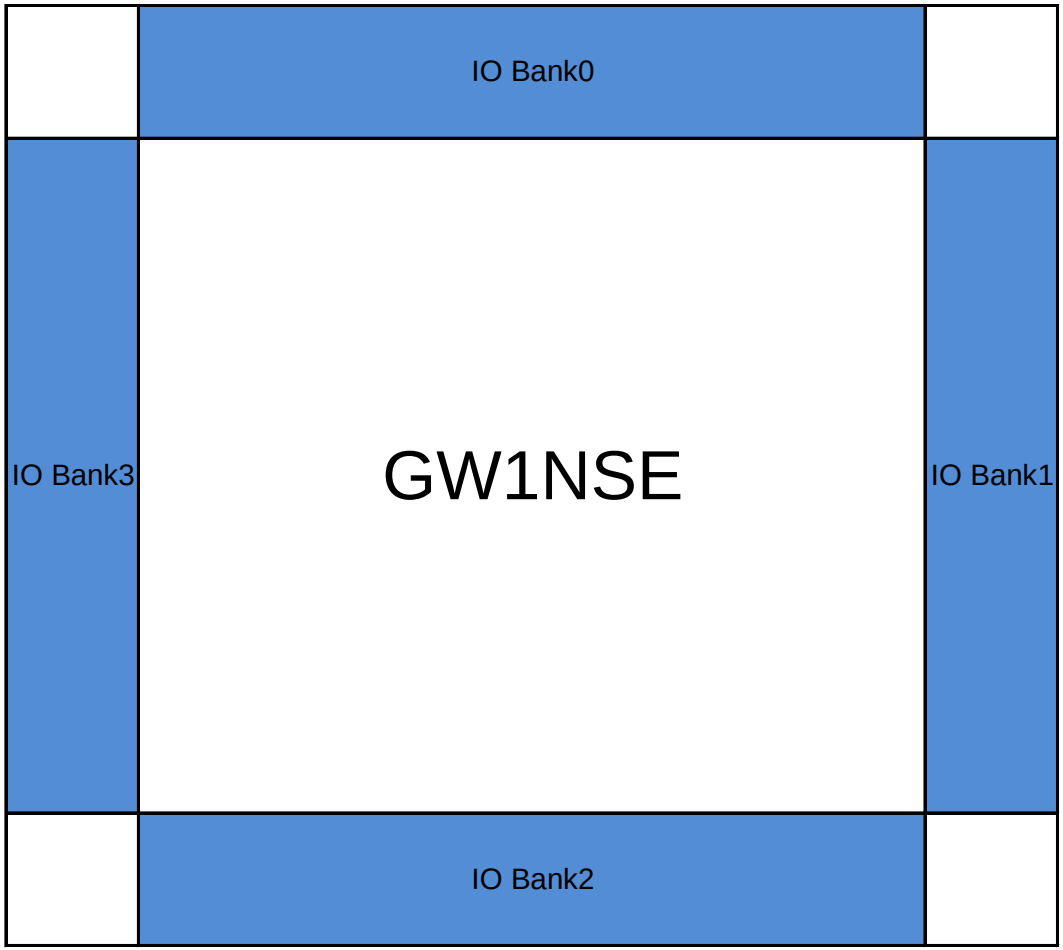
Pin Name	I/O	Description
User I/O		
IO[End][Row/Column Number][A/B]	I/O	[End] indicates the pin location, including L(left), R(right), B(bottom), and T(top).
		[Row/Column Number] indicates the pin row/column number. If [End] is T(top) or B(bottom), the pin indicates the column number of the corresponding CFU. If [End] is L(left) or R(right), the pin indicates the row number of the corresponding CFU.
		[A/B] indicates differential signal pair information.
Multi-Function Pins		
IO[End][Row/Column Number][A/B]/MMM		/MMM represents one or more of the other functions in addition to being general purpose user I/O. When these functions are not in use, these pins can be used as user I/O.
D0	I/O	Data port D0 in CPU mode
D1	I/O	Data port D1 in CPU mode
D2	I/O	Data port D2 in CPU mode
D3	I/O	Data port D3 in CPU mode
D4	I/O	Data port D4 in CPU mode
D5	I/O	Data port D5 in CPU mode
D6	I/O	Data port D6 in CPU mode
D7	I/O	Data port D7 in CPU mode
WE_N	I	Select data input/output of D[7:0] in CPU mode.0: Write;1: Read.
DOUT	O	Data output in SERIAL mode
DIN	I, internal weak pull-up	Data input in SERIAL mode
TMS	I, internal weak pull-up	Serial mode input in JTAG mode
TCK	I	Serial clock input in JTAG mode
TDO	O	Serial data output in JTAG mode
TDI	I, internal weak pull-up	Serial data input in JTAG mode
JTAGSEL_N	I, internal weak pull-up	Reconfigure JTAG download function signal
RECONFIG_N	I	Global reset GowinCONFIG logic signal, active low
FASTRD_N	I	Access SPI FLASH to select signal. Low, Fast Read mode; High, Read mode.
DONE[1]	O	High, the programming configuration has been completed successfully; Low, the programming configuration has not been completed or failed.
	I	When the DONE signal is low, delay the chip to activate. Activate the chip until the DONE signal is high.
READY[1]	I/O	High, the device can be programmed and configured currently; Low, the device cannot be programmed and configured currently.
MI	O	MI in MSPI mode

Pin Name	I/O	Description
MO	I	MO in MSPI mode
MCS_N	O	Enable signal MCS_N in MSPI mode, active-low
MCLK	O	Clock output MCLK in MSPI mode, with default frequency of 2.5Mhz
SCLK	I	Clock input in SSPI, SERIAL, and CPU modes
SO	O	SO in SSPI mode
SI	I/O	SI in SSPI mode
SSPI_CS_N	I/O	Enable signal SSPI_CS_N in SSPI mode, active-low, and internal weak pull-up
CLKHOLD_N	I, internal weak pull-up	High, the operation is efficient in SSPI mode or CPU mode; Low, the operation is inefficient in SSPI mode or CPU mode.
GCLKC_[x]	I	Differential input pin of GCLKT_[x], C(Comp), [x]: global clock No.[2]
GCLKT_[x]	I	Global clock input pin, T(True), [x]: global clock No.
LPLL_C_fb/RPLL_C_fb	I	Left/Right PLL feedback input pin, C(Comp)
LPLL_T_fb/RPLL_T_fb	I	Left/Right PLL feedback input pin, T(True)
LPLL_C_in/RPLL_C_in	I	Left/Right PLL clock input pin, C(Comp)
LPLL_T_in/RPLL_T_in	I	Left/Right PLL clock input pin, T(True)
CH[7:0]	I	Eight-channel analog input
MODE2	I, internal weak pull-up	Selection signal port in GowinCONFIG mode If this pin is not bonded, it's internally grounded.
MODE1	I, internal weak pull-up	Selection signal port in GowinCONFIG mode If this pin is not bonded, it's internally grounded.
MODE0	I, internal weak pull-up	Selection signal port in GowinCONFIG mode If this pin is not bonded, it's internally grounded.
Other Pins		
NC	NA	Reserved
VSS	NA	Ground
VCC	NA	Power supply pin of core voltage
VCCO#	NA	Power supply pin of I/O voltage for I/O BANK#
VCCX	NA	Power supply pin of auxiliary voltage
VCCP	NA	Power supply pin of FLASH(1.8V)
VCCPLL	NA	Power supply pin of PLL voltage
USB Signal Pin		
DM	NA	USB data pin Data-
DP	NA	USB data pin Data+

Pin Name	I/O	Description
REXT	NA	12.7K high-accuracy resistance
XIN	NA	Crystal oscillator input signal
XOUT	NA	Crystal oscillator output signal
IDPAD	NA	ID signal
VBUSPAD	NA	VBUS signal
VDDA	NA	ADC analog power supply voltage, VDDA=3.3V
VDDAUSB	NA	Analog power supply pin (3.3V)
VDDDUSB	NA	Analog power supply pin (3.3V)
VDDPL	NA	Power supply pin of HS driver (1.2V)
X16	NA	Indicates IO supports 16:1 function
VREF	NA	ADC external reference voltage input pin

Note!
[1] Ready and Done can not be driven to low before and during configuration.
[2] When the input is single-ended, GCLKC_[x] pin is not a global clock.

Bank



Note!

[1] Each Bank has independent reference voltage (VREF);

[2] You can select to use IOB internal VREF (equals to 0.5 X VCCO);

[3] You can also select to use external VREF input (use any I/O pins as external VREF input).

Note!
[1] IOL2A shares pin 1 with VCCO0 and VCCO3 in package QN48.
[2] IOL2A shares pin 144 with VCCO0 in package LQ144.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	QN48	LQ144
DM	Power	N/A						76
DP	Power	N/A						75
IDPAD	Power	N/A						80
IOB10A	I/O	2	GCLKT_5	True_of_IOB10B	NONE	NONE	17	44
IOB10B	I/O	2	GCLKC_5	Comp_of_IOB10A	NONE	NONE	18	45
IOB11A	I/O	2	GCLKT_4	True_of_IOB11B	TRUE	x16	19	46
IOB11B	I/O	2	GCLKC_4	Comp_of_IOB11A	TRUE	NONE	20	47
IOB12A	I/O	2		True_of_IOB12B	NONE	NONE		54
IOB12B	I/O	2		Comp_of_IOB12A	NONE	NONE		58
IOB13A	I/O	2		True_of_IOB13B	TRUE	x16	21	59
IOB13B	I/O	2		Comp_of_IOB13A	TRUE	NONE	22	60
IOB14A	I/O	2		True_of_IOB14B	NONE	NONE		61
IOB14B	I/O	2		Comp_of_IOB14A	NONE	NONE		62
IOB15A	I/O	2		True_of_IOB15B	TRUE	x16	23	63
IOB15B	I/O	2		Comp_of_IOB15A	TRUE	NONE	24	64
IOB16A	I/O	2		True_of_IOB16B	NONE	NONE		65
IOB16B	I/O	2		Comp_of_IOB16A	NONE	NONE		66
IOB17A	I/O	2		True_of_IOB17B	TRUE	x16		67
IOB17B	I/O	2		Comp_of_IOB17A	TRUE	NONE		68
IOB18A	I/O	2		True_of_IOB18B	NONE	NONE		69
IOB18B	I/O	2		Comp_of_IOB18A	NONE	NONE		70
IOB19A	I/O	2		True_of_IOB19B	NONE	NONE		71
IOB19B	I/O	2		Comp_of_IOB19A	NONE	NONE		72
IOB7A	I/O	2		True_of_IOB7B	TRUE	x16		38
IOB7B	I/O	2		Comp_of_IOB7A	TRUE	NONE	14	39
IOB8A	I/O	2		True_of_IOB8B	NONE	NONE		40
IOB8B	I/O	2		Comp_of_IOB8A	NONE	NONE		41
IOB9A	I/O	2		True_of_IOB9B	TRUE	x16	15	42
IOB9B	I/O	2		Comp_of_IOB9A	TRUE	NONE	16	43
IOL2A	I/O	3	JTAGSEL_N/VREF	True_of_IOL2B	TRUE	NONE	1	144

Note!
[1] IOL2A shares pin 1 with VCCO0 and VCCO3 in package QN48.
[2] IOL2A shares pin 144 with VCCO0 in package LQ144.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	QN48	LQ144
IOL2B	I/O	3		Comp_of_IOL2A	TRUE	NONE		
IOL3A	I/O	3		True_of_IOL3B	NONE	NONE		
IOL3B	I/O	3		Comp_of_IOL3A	NONE	NONE		7
IOL4A	I/O	3		True_of_IOL4B	TRUE	NONE		8
IOL4B	I/O	3		Comp_of_IOL4A	TRUE	NONE		9
IOL5A	I/O	3	GCLKT_7	True_of_IOL5B	NONE	NONE	3	11
IOL5B	I/O	3	GCLKC_7	Comp_of_IOL5A	NONE	NONE		12
IOL6A	I/O	3	TMS	True_of_IOL6B	NONE	NONE	4	13
IOL6B	I/O	3	TCK	Comp_of_IOL6A	NONE	NONE	5	14
IOL6C	I/O	3	SCLK	True_of_IOL6D	NONE	NONE		15
IOL6D	I/O	3	TDI	Comp_of_IOL6C	NONE	NONE	6	16
IOL6E	I/O	3	TDO	True_of_IOL6F	NONE	NONE	7	18
IOL6F	I/O	3	RECONFIG_N	Comp_of_IOL6E	NONE	NONE		20
IOL6G	I/O	3	DONE	True_of_IOL6H	NONE	NONE	9	21
IOL6H	I/O	3	READY	Comp_of_IOL6G	NONE	NONE		22
IOL6I	I/O	3		True_of_IOL6J	NONE	NONE		23
IOL6J	I/O	3		Comp_of_IOL6I	NONE	NONE		24
IOL7A	I/O	3	GCLKT_6	True_of_IOL7B	TRUE	NONE	10	25
IOL7B	I/O	3	GCLKC_6	Comp_of_IOL7A	TRUE	NONE	11	27
IOL8A	I/O	3		True_of_IOL8B	NONE	NONE		
IOL8B	I/O	3		Comp_of_IOL8A	NONE	NONE		28
IOL9A	I/O	3		True_of_IOL9B	NONE	NONE		29
IOL9B	I/O	3		Comp_of_IOL9A	NONE	NONE		30
IOR2A	I/O	1	RPLL_T_fb	True_of_IOR2B	TRUE	NONE		106
IOR2B	I/O	1	RPLL_C_fb	Comp_of_IOR2A	TRUE	NONE		104
IOR3A	I/O	1	GCLKT_2/RPLL_T_in	True_of_IOR3B	NONE	NONE	35	101
IOR3B	I/O	1	GCLKC_2/RPLL_C_in	Comp_of_IOR3A	NONE	NONE		102
IOR4A	I/O	1	MI/D7	True_of_IOR4B	TRUE	NONE	33	99
IOR4B	I/O	1	MO/D6	Comp_of_IOR4A	TRUE	NONE	34	100
IOR5A	I/O	1	MCS_N/D5	True_of_IOR5B	NONE	NONE		97

Note!
[1] IOL2A shares pin 1 with VCCO0 and VCCO3 in package QN48.
[2] IOL2A shares pin 144 with VCCO0 in package LQ144.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	QN48	LQ144
IOR5B	I/O	1	MCLK/D4	Comp_of_IOR5A	NONE	NONE		98
IOR6A	I/O	1	FASTRD_N /D3	True_of_IOR6B	NONE	NONE		96
IOR6B	I/O	1	SI/D2	Comp_of_IOR6A	NONE	NONE		95
IOR7A	I/O	1	SO/D1	True_of_IOR7B	TRUE	NONE	32	90
IOR7B	I/O	1	SSPI_CS_N/D0	Comp_of_IOR7A	TRUE	NONE	31	88
IOR8A	I/O	1	DIN/CLKHOLD_N	True_of_IOR8B	NONE	NONE	29	86
IOR8B	I/O	1	DOUT/WE_N	Comp_of_IOR8A	NONE	NONE	30	87
IOR9A	I/O	1	GCLKT_3	True_of_IOR9B	NONE	NONE	28	84
IOR9B	I/O	1	GCLKC_3	Comp_of_IOR9A	NONE	NONE	27	83
IOT10A	I/O	0	GCLKT_0	True_of_IOT10B	NONE	NONE		130
IOT10B	I/O	0	GCLKC_0	Comp_of_IOT10A	NONE	NONE		129
IOT11A	I/O	0	GCLKT_1	True_of_IOT11B	NONE	x16		128
IOT11B	I/O	0	GCLKC_1	Comp_of_IOT11A	NONE	NONE		126
IOT12A	I/O	0		True_of_IOT12B	NONE	NONE		124
IOT12B	I/O	0		Comp_of_IOT12A	NONE	NONE		123
IOT13A	I/O	0		True_of_IOT13B	NONE	x16	39	122
IOT13B	I/O	0		Comp_of_IOT13A	NONE	NONE	38	121
IOT14A	I/O	0		True_of_IOT14B	NONE	NONE		120
IOT14B	I/O	0		Comp_of_IOT14A	NONE	NONE		119
IOT15A	I/O	0		True_of_IOT15B	NONE	x16		118
IOT15B	I/O	0		Comp_of_IOT15A	NONE	NONE		117
IOT16A	I/O	0		True_of_IOT16B	NONE	NONE		116
IOT16B	I/O	0		Comp_of_IOT16A	NONE	NONE		115
IOT17A	I/O	0		True_of_IOT17B	NONE	x16		114
IOT17B	I/O	0		Comp_of_IOT17A	NONE	NONE		113
IOT18A	I/O	0		True_of_IOT18B	NONE	NONE		112
IOT18B	I/O	0		Comp_of_IOT18A	NONE	NONE		111
IOT19A	I/O	0		True_of_IOT19B	NONE	NONE		110
IOT19B	I/O	0		Comp_of_IOT19A	NONE	NONE		
IOT2A	I/O	0		True_of_IOT2B	NONE	x16	48	

Note!
[1] IOL2A shares pin 1 with VCCO0 and VCCO3 in package QN48.
[2] IOL2A shares pin 144 with VCCO0 in package LQ144.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	QN48	LQ144
IOT2B	I/O	0	MODE0	Comp_of_IOT2A	NONE	NONE		
IOT3A	I/O	0	MODE2	True_of_IOT3B	NONE	NONE		
IOT3B	I/O	0	MODE1	Comp_of_IOT3A	NONE	NONE		
IOT4A	I/O	0	CH0	True_of_IOT4B	NONE	x16	47	140
IOT4B	I/O	0	CH1	Comp_of_IOT4A	NONE	NONE	46	139
IOT5A	I/O	0	CH2	True_of_IOT5B	NONE	NONE	45	138
IOT5B	I/O	0	CH3	Comp_of_IOT5A	NONE	NONE	44	137
IOT6A	I/O	0	CH4	True_of_IOT6B	NONE	x16	43	136
IOT6B	I/O	0	CH5	Comp_of_IOT6A	NONE	NONE	42	135
IOT7A	I/O	0	CH6	True_of_IOT7B	NONE	NONE	41	134
IOT7B	I/O	0	CH7	Comp_of_IOT7A	NONE	NONE	40	133
IOT8A	I/O	0		True_of_IOT8B	NONE	x16		
IOT8B	I/O	0		Comp_of_IOT8A	NONE	NONE		
IOT9A	I/O	0		True_of_IOT9B	NONE	NONE		132
IOT9B	I/O	0		Comp_of_IOT9A	NONE	NONE		131
NC	N/A	N/A						1
NC	N/A	N/A						3
NC	N/A	N/A						4
NC	N/A	N/A						6
NC	N/A	N/A						10
NC	N/A	N/A						19
NC	N/A	N/A						32
NC	N/A	N/A						34
NC	N/A	N/A						48
NC	N/A	N/A						49
NC	N/A	N/A						50
NC	N/A	N/A						51
NC	N/A	N/A						52
NC	N/A	N/A						56
NC	N/A	N/A						57

Note!
[1] IOL2A shares pin 1 with VCCO0 and VCCO3 in package QN48.
[2] IOL2A shares pin 144 with VCCO0 in package LQ144.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	QN48	LQ144
NC	N/A	N/A						92
NC	N/A	N/A						93
NC	N/A	N/A						94
NC	N/A	N/A						141
NC	N/A	N/A						142
NC	N/A	N/A						143
REXT	Power	N/A						81
VBUSPAD	Power	N/A						82
VCC/VCCPLL	Power	N/A					37	
VCC/VCCPLL	Power	N/A					12	
VCC/VCCPLL/VDDPL	Power	N/A						36
VCC/VCCPLL/VDDPL	Power	N/A						73
VCC/VCCPLL/VDDPL	Power	N/A						108
VCCO0/VCCO3	Power	N/A					1	
VCCO0	Power	N/A						109
VCCO0	Power	N/A						127
VCCO0	Power	N/A						144
VCCO1	Power	N/A					25	91
VCCO2	Power	N/A					13	37
VCCO2	Power	N/A						55
VCCO3	Power	N/A						5
VCCO3	Power	N/A						26
VCCP/VCCX	Power	N/A					8	
VCCP/VCCX	Power	N/A					36	
VCCX/VDDAUSB	Power	N/A						78
VCCX/VDDAUSB	Power	N/A						31
VCCX/VDDAUSB	Power	N/A						103
VDDDUSB	Power	N/A						85
VSS	Ground	N/A						105
VSS	Ground	N/A						107

Note!
[1] IOL2A shares pin 1 with VCCO0 and VCCO3 in package QN48.
[2] IOL2A shares pin 144 with VCCO0 in package LQ144.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	QN48	LQ144
VSS	Ground	N/A						74
VSS	Ground	N/A					26	17
VSS	Ground	N/A					2	2
VSS	Ground	N/A						33
VSS	Ground	N/A						35
VSS	Ground	N/A						125
VSS	Ground	N/A						89
VSS	Ground	N/A						53
XIN	Power	N/A						77
XOUT	Power	N/A						79

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	QN48	LQ144
BANK2 True LVDS Pair								
IOB11A	I/O	2	GCLKT_4	True_of_IOB11B	TRUE	x16	19	46
IOB11B	I/O	2	GCLKC_4	Comp_of_IOB11A	TRUE	NONE	20	47
IOB13A	I/O	2		True_of_IOB13B	TRUE	x16	21	59
IOB13B	I/O	2		Comp_of_IOB13A	TRUE	NONE	22	60
IOB15A	I/O	2		True_of_IOB15B	TRUE	x16	23	63
IOB15B	I/O	2		Comp_of_IOB15A	TRUE	NONE	24	64
IOB17A	I/O	2		True_of_IOB17B	TRUE	x16		67
IOB17B	I/O	2		Comp_of_IOB17A	TRUE	NONE		68
IOB7A	I/O	2		True_of_IOB7B	TRUE	x16		38
IOB7B	I/O	2		Comp_of_IOB7A	TRUE	NONE	14	39
IOB9A	I/O	2		True_of_IOB9B	TRUE	x16	15	42
IOB9B	I/O	2		Comp_of_IOB9A	TRUE	NONE	16	43
IOL2A	I/O	3	JTAGSEL_N/VREF	True_of_IOL2B	TRUE	NONE	1	144
IOL2B	I/O	3		Comp_of_IOL2A	TRUE	NONE		
IOL4A	I/O	3		True_of_IOL4B	TRUE	NONE		8
IOL4B	I/O	3		Comp_of_IOL4A	TRUE	NONE		9
IOL7A	I/O	3	GCLKT_6	True_of_IOL7B	TRUE	NONE	10	25
IOL7B	I/O	3	GCLKC_6	Comp_of_IOL7A	TRUE	NONE	11	27
IOR2A	I/O	1	RPLL_T_fb	True_of_IOR2B	TRUE	NONE		106
IOR2B	I/O	1	RPLL_C_fb	Comp_of_IOR2A	TRUE	NONE		104
IOR4A	I/O	1	MI/D7	True_of_IOR4B	TRUE	NONE	33	99
IOR4B	I/O	1	MO/D6	Comp_of_IOR4A	TRUE	NONE	34	100
IOR7A	I/O	1	SO/D1	True_of_IOR7B	TRUE	NONE	32	90
IOR7B	I/O	1	SSPI_CS_N/D0	Comp_of_IOR7A	TRUE	NONE	31	88

Note! It is recommended to connect VCCX to the VCCO with the Max. voltage				
Recommended Operating Conditions of Package QN48 in GW1NSE-2C				
Name	**Description**		**Min.**	**Max.**
VCCO1, VCCO2	LX: I/O Bank power supply voltage		1.14V	1.89V
	UX: I/O Bank power supply voltage; VCCX must be greater than or equal to VCCO		1.14V	3.6V
VCCP/VCCX	VCCP/ VCCX are internally connected.	LX: Auxiliary voltage	1.71V	1.89V
		UX: Auxiliary voltage	2.375V	3.6V
VCC/VCCPLL	VCC/VCCPLL are internally connected.		1.14V	1.26V
IOL2A/VCCO0/ VCCO3	IOL2A/VCCO0/VCCO3 are internally connected.	LX: I/O Bank power supply voltage	1.14V	1.89V
		UX: I/O Bank power supply voltage; VCCX must be greater than or equal to VCCO	1.14V	3.6V
		When ADC is used, IOL2A/VCCO0/VCCO3 need provide 3.3V voltage.	3.135V	3.6V
Recommended Operating Conditions of Package LQ144 in GW1NSE-2C				
Name	**Description**		**Min.**	**Max.**
VCCO1, VCCO2, VCCO3	LX: I/O Bank power supply voltage		1.14V	1.89V
	UX: I/O Bank power supply voltage; VCCX must be greater than or equal to VCCO		1.14V	3.6V
VCCX/VDDAUSB	VCCX/VDDAUSB are internally connected.	LX: Auxiliary voltage	1.71V	1.89V
		UX: Auxiliary voltage	2.375V	3.6V
IOL2A/VCCO0	LX: I/O Bank power supply voltage		1.14V	1.89V
	UX: I/O Bank power supply voltage; VCCX must be greater than or equal to VCCO		1.14V	3.6V
	When ADC is used, IOL2A/VCCO0 need provide 3.3V voltage.		3.135V	3.6V
VCC/VCCPLL/VDDPL	VCC/VCCPLL/VDDPL are internally connected.		1.14V	1.26V