GW1NSER series of SecureFPGA

Package & Pinout User Guide

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Revision History

Date	Version	Description
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1 About This Guide

1.1 Purpose

This manual contains an introduction to the GW1NSER series of SecureFPGA products together with a definition of the pins, list of pin numbers, distribution of pins, and package diagrams.

1.2 Related Documents

The user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

1. DS881, GW1NSER series of SecureFPGA products Data Sheet
2. UG290, Gowin FPGA Products Programming and Configuration User Guide
3. UG884, GW1NSER series of SecureFPGA products Package and Pinout
4. UG883, GW1NSER-4C Pinout

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Full Name
FPGA	Field Programmable Gate Array
GPIO	Gowin Programmable IO
QN48P	QFN48P
QN48G	QFN48G

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail:support@gowinsemi.com

2 Overview

GW1NSER series of SecureFPGA products provide a Root of Trust based on SRAM PUF technology. Each device is factory provisioned with a unique key pair that is never exposed outside of the device or to the internal development space. The Intrinsic ID BroadKey-Pro security library is provided with GOWIN SecureFPGA devices allowing easy integration of common security features into user applications. The GOWIN SecureFPGA feature set is widely applicable and can used for a variety of consumer, industrial IoT, edge, and server management applications.

2.1 PB-Free Package

The GW1NSER series of SecureFPGA products are PB free in line with the EU ROHS environmental directives. The substances used in the GW1NSER series of SecureFPGA products are in full compliance with the IPC-1752 standards.

2.2 Package and Max. User I/O Information

Table 2-1 Package, Max. User I/O Information, and LVDS Paris

Package	Pitch (mm)	Size (mm)	GW1NSER-4C
QN48P	0.4	6 x 6	38(4)
QN48G	0.4	6 x 6	38(4)

Note!

- In this manual, abbreviations are employed to refer to the package types. See 1.3Terminology and Abbreviations.
- The JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The data in this table is when the loaded four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O. When mode [2:0] = 001, JTAGSEL_N and the four JTAG pins (TCK, TDI, TDO, and TMS) can be used as GPIO simultaneously, and the Max. user I/O plus one.

2.3 Power Pin

Table 2-2 GW1NSER Power Pins

VCC	VCCO0	VCCO1	VCCO2
VCCO3	VSS		

2.4 Pin Quantity

2.4.1 Quantity of GW1NSER-4C Pins

Table 2-3 Quantity of GW1NSER-4CPins

Pin Type		GW1NSER-4C	
		QN48P	QN48G
I/O Single end / Differential pair[1]	BANK0	8/4/0	8/4/0
	BANK1	10/5/0	10/5/0
	BANK2	9/4/4	9/4/4
	BANK3	11/5/0	11/5/0
Max. User I/O [2]		38	38
Differential Pair		18	18
True LVDS output		4	4
VCC		2	2
VCCO0		1	1
VCCO1		1	1
VCCO2		1	1
VCCO3		2	2
VCCX		1	1
VSS		1	1
MODE0		0	0
MODE1		0	0
MODE2		0	0
JTAGSEL_N		1	1

Note!

- Single end/ Differential I/O quantity include CLK pins, and download pins;
- [2]The JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The data in this table is when the loaded four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O;

2.5 Pin Definitions

The location of the pins in the GW1NSER series of SecureFPGA products varies according to the different packages.

Table 2-4 provides a detailed overview of user I/O, multi-function pins, dedicated pins, and other pins.

Table 2-4 Definition of the Pins in the GW1NSER series of SecureFPGA products

Pin Name	I/O	Description
Max. User I/O		
IO[End][Row/Column Number][A/B]	I/O	[End] indicates the pin location, including L(left) R(right) B(bottom), and T(top) [Row/Column Number] indicates the pin Row/Column number.If [End] is T(top) or B(bottom), the pin indicates the column number of the corresponding CFU. If [End] is L(left) or R(right), the pin indicates the Row number of the corresponding CFU. [A/B] indicates differential signal pair information.
Multi-Function Pins		
IO[End][Row/Column Number][A/B]/MMM		/MMM represents one or more of the other functions in addition to being general purpose user I/O. These pins can be used as user I/O when the functions are not used.
RECONFIG_N	I, internal weak pull-up	Start new GowinCONFIG mode when low pulse
READY	I/O	When high level, the device can be programmed and configured When low level, the device cannot be programmed and configured
DONE	I/O	High level indicates successful program and configure Low level indicates incomplete or failed to program and configure
FASTRD_N /D3	I/O	In MSPI mode, FASTRD_N is used as Flash access speed port. Low indicates high-speed Flash access mode; high indicates regular Flash access mode. Data port D3 in CPU mode
MCLK /D4	I/O	Clock output MCLK in MSPI mode Data port D4 in CPU mode
MCS_N /D5	I/O	Enable signal MCS_N in MSPI mode, active-low Data port D5 in CPU mode
MI /D7	I/O	MISO in MSPI mode: Master data input/Slave data output Data port D7 in CPU mode
MO /D6	I/O	MISO in MSPI mode: Master data output/Slave data input Data port D6 in CPU mode
SSPI_CS_N/D0	I/O	Enable signal SSPI_CS_N in SSPI mod, active-low, Internal Weak Pull Up Data port D0 in CPU mode
SO /D1	I/O	MISO in MSPI mode: Master data input/Slave data output Data port D1 in CPU mode

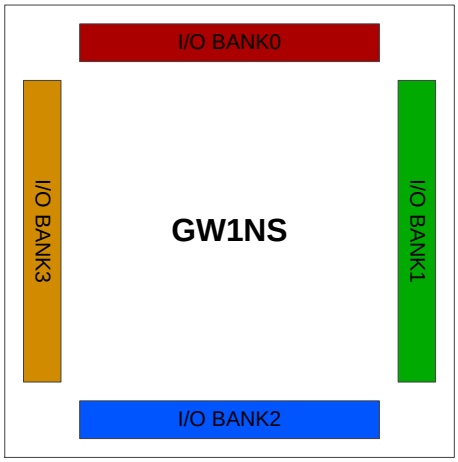
Pin Name	I/O	Description
SI /D2	I/O	MISO in MSPI mode: Master data output/Slave data input Data port D2 in CPU mode
TMS	I, internal weak pull-up	Serial mode input in JTAG mode
TCK	I	Serial clock input in JTAG mode, which needs to be connected with 4.7 K drop-down resistance on PCB
TDI	I, internal weak pull-up	Serial data input in JTAG mode
TDO	O	Serial data output in JTAG mode
JTAGSEL_N	I, internal weak pull-up	Select signal in JTAG mode, active-low
SCLK	I	Clock input in SSPI, SERIAL, and CPU mode
DIN	I, internal weak pull-up	Input data in SERIAL mode
DOUT	O	Output data in SERIAL mode
CLKHOLD_N	I, internal weak pull-up	High level, SCLK will be connected internally in SSPI mode or CPU mode Low level, SCLK will be disconnected from SSPI mode or CPU mode
WE_N	I	Select data input/output of D[7:0] in CPU mode
GCLKT_[x]	I	Pins in global clock input, T(True), [x]: global clock No.
GCLKC_[x]	I	Pins for Global clock input, C(Comp), [x]: global clock No.
LPLL_T_fb/RPLL_T_fb	I	L/R PLL feedback input pin, T(True)
LPLL_C_fb/RPLL_C_fb	I	L/R PLL feedback input pin, C(Comp)
LPLL_T_in/RPLL_T_in	I	L/R PLL clock input pin, T(True)
LPLL_C_in/RPLL_C_in	I	L/R PLL clock input pin, C(Comp)
CH[7:0]	I	Eight-channel analog input
MODE2	I, internal weak pull-up	GowinCONFIG modes selection pin; if this pin is not bonded, it's internal grounded.
MODE1	I, internal weak pull-up	GowinCONFIG modes selection pin; if this pin is not bonded, it's internal grounded.
MODE0	I, internal weak pull-up	GowinCONFIG modes selection pin; if this pin is not bonded, it's internal grounded.
Other Pins		
NC	NA	Reserved.
VSS	NA	Ground pins
VCC	NA	Power supply pins for internal core logic.
VCCO#	NA	Power supply pins for the I/O voltage of I/O BANK#.
VCCX	NA	Power supply pins for auxiliary voltage.
VCCP	NA	FLASH Power supply pin (1.8V)
VCCPLL	NA	Power supply pins in PLL
USB Power supply pin		
DM	NA	USB data pin Data-
DP	NA	USB data pin Data+

Pin Name	I/O	Description
REXT	NA	12.7K high-accuracy resistance
XIN	NA	Crystal input signals
XOUT	NA	Crystal oscillator signals
IDPAD	NA	ID signal
VBUSPAD	NA	VBUS signal
VDDA	NA	Analog power supply voltage, VDDA=3.3V
VDDAUSB	NA	Analog power supply pin (3.3V)
VDDDUSB	NA	Analog power supply pin (3.3V)
VDDPL	NA	Power supply pin for driver (1.2V)

2.6 I/O BANK Introduction

There are four I/O Banks in the GW1NSER series of SecureFPGA products. The I/O BANK Distribution of the GW1NSER series of SecureFPGA products is as shown in Figure 2-1.

Figure 2-1 GW1NSER series of SecureFPGA products I/O Bank Distribution



This manual provides an overview of the distribution view of the pins in the GW1NSER series of SecureFPGA products. The four I/O Banks in the GW1NSER series of SecureFPGA products are marked with four different colors.

Various symbols are used for the user I/O, power, and ground. The various symbols and colors used for the various pins are defined as follows:

- "  " denotes the I/O in BANK0. The filling color changes with the BANK;
- "  " denotes the I/O in BANK1. The filling color changes with the BANK;
- "  " denotes the I/O in BANK2. The filling color changes with the BANK;
- "  " denotes the I/O in BANK3. The filling color changes with the BANK;
- "  " denotes VCC, VCCX, and VCCO. The filling color does not change;
- "  " denotes VSS, the filling color does not change;
- "  " denotes NC.

3 View of Pin Distribution

3.1 View of GW1NSER-4C Pins Distribution

3.1.1 View of QN48P Pins Distribution

Figure 3-1 View of GW1NSER-4C QN48P Pins Distribution (Top View)

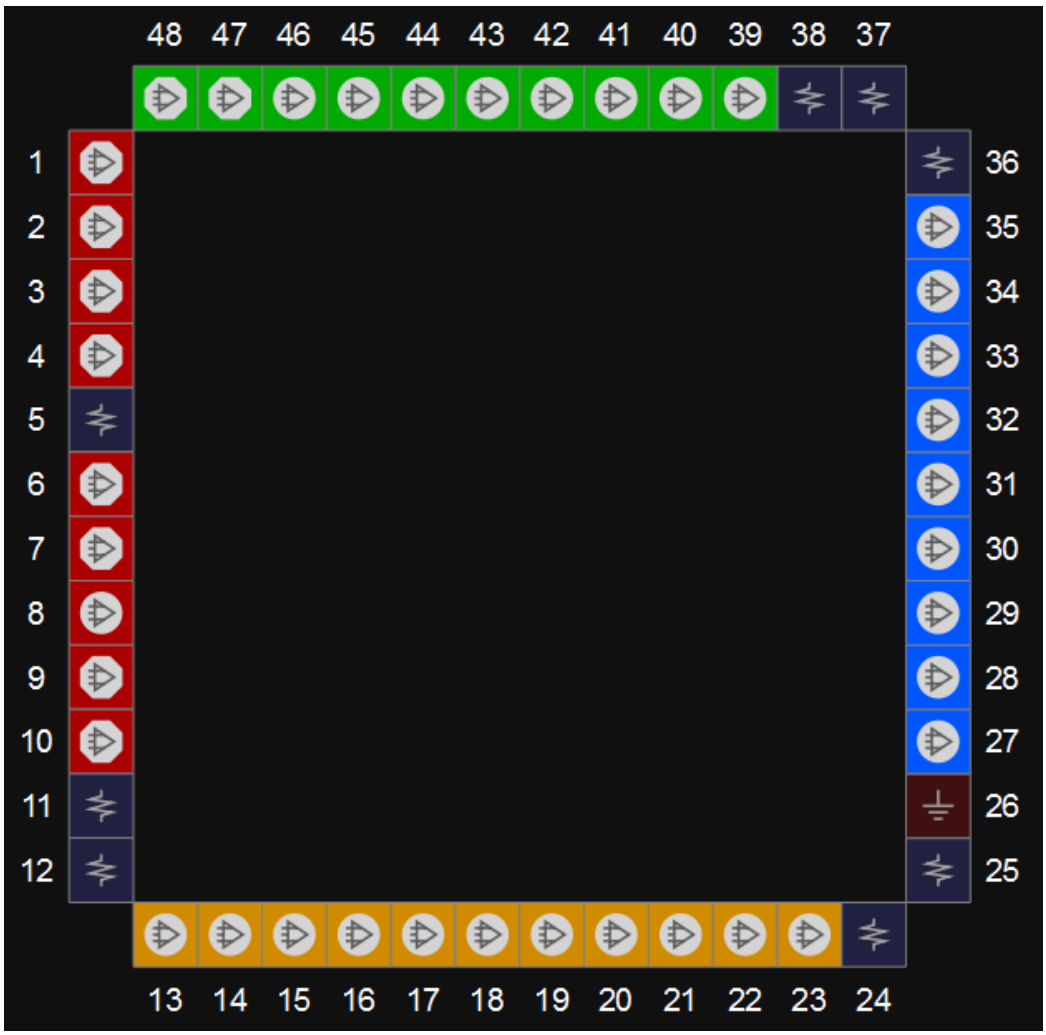


Table 3-1 Other pins in GW1NSER-4C QN48P

VCC	11,37
VCCO0	5
VCCO1	38
VCCO2	36
VCCO3	12,24
VCCX	25
VSS	26

3.1.2 View of QN48G Pins Distribution

Figure 3-2 View of GW1N-4 QN48G Pins Distribution (Top View)

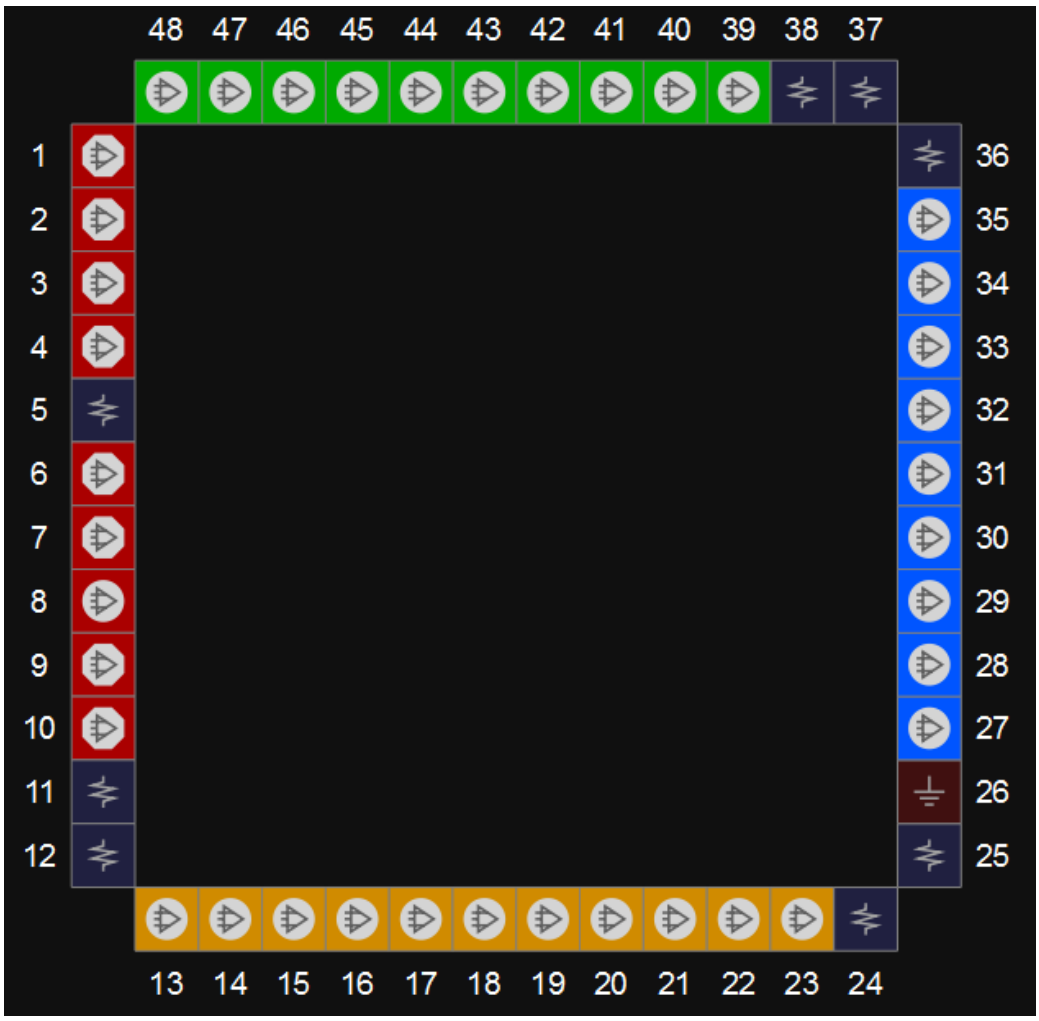


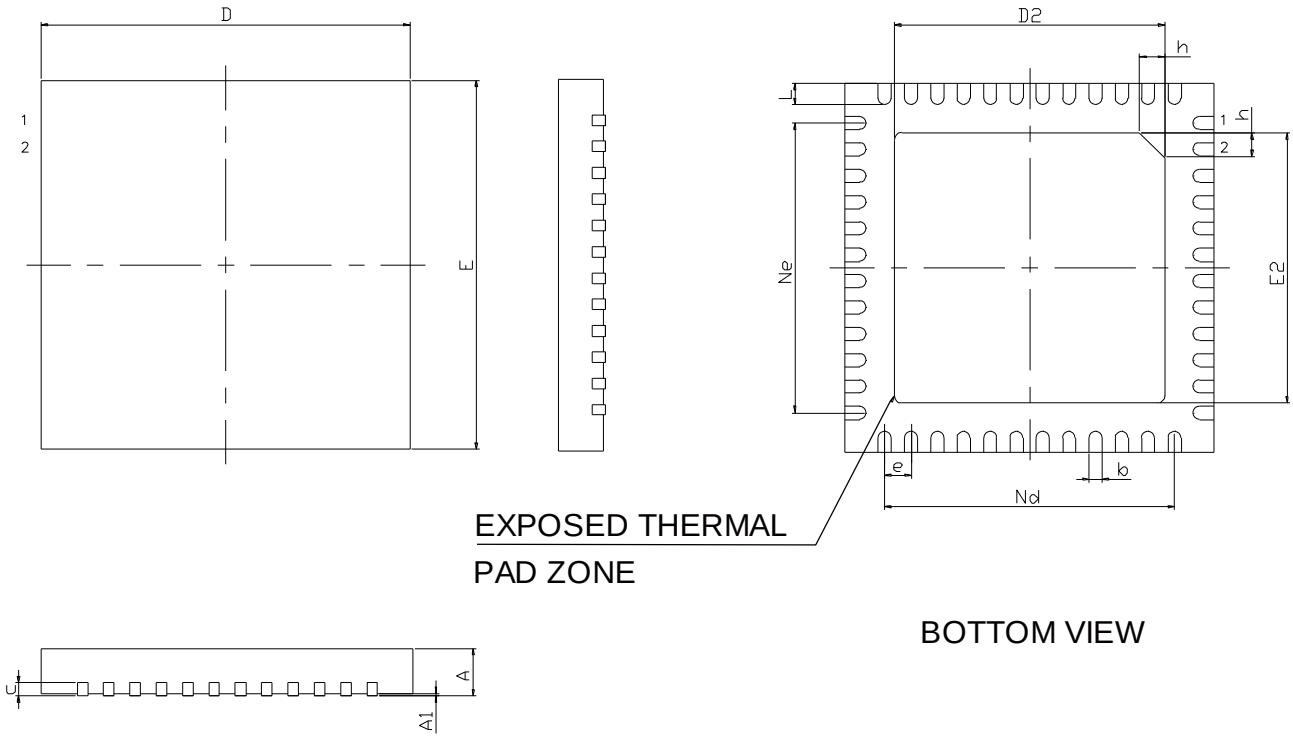
Table 3-2 Other pins in GW1NSER-4C QN48G

VCC	11,37
VCCO0	5
VCCO1	38
VCCO2	36
VCCO3	12,24
VCCX	25
VSS	26

4 Package Diagrams

4.1 QN48P / QN48G Package Outline (6mm x 6mm)

Figure 4-1 Package Outline of QN48P / QN48G



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.75	0.85	0.85
A1	—	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.23
D	5.90	6.00	6.10
D2	4.10	4.20	4.30
e	0.40BSC		
Ne	4.40BSC		
Nd	4.40BSC		
E	5.90	6.00	6.10
E2	4.10	4.20	4.30
L	0.35	0.40	0.45
h	0.30	0.35	0.40
L/F载体尺寸（MIL）	177*177		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