Date	Version	Description
01/27/2021	1.0E	Initial version published. UG484, UG400, UG256, PG256, UG332, UG324, and PG484 packages supported.
05/19/2021	1.1E	The location of pin IOB15A, IOB15B, IOB17A, and IOB17B in UG484 package modified.
07/21/2021	1.2E	The descriptions of pin DED and MODE removed.
08/12/2021	1.3E	Power info modified; The description of mode pin improved.
10/21/2021	1.4E	Pin definitions updated.
08/19/2022	1.4.1E	The Min.voltage of VCCX in Power updated.
10/20/2022	1.4.2E	The note in Power sheet updated; The note in Pin Definitions sheet updated; The description of MODE0 and MODE1 pins in Pin Definitions sheet updated.
11/11/2022	1.4.3E	Power info. updated; The description of pin CLKHOLD_N in Pin Definitions sheet updated.
05/04/2023	1.4.4E	The direction of pin MO in Pin Definitions updated.

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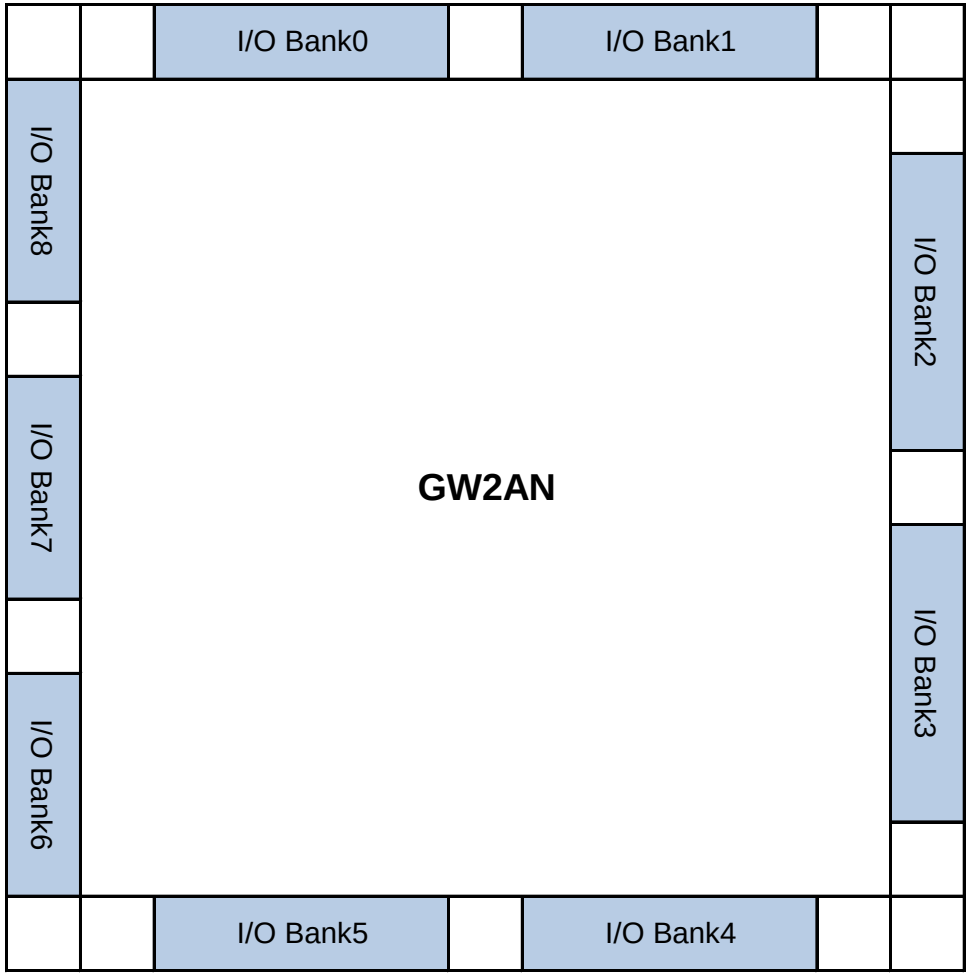
Pin Name	I/O	Description
User I/O		
IO[End][Row/Column Number][A/B]	I/O/LVDS	[End] indicates the pin location, including L(left), R(right), B(bottom), and T(top).
		[Row/Column Number] indicates the pin row/column number. If [End] is T(top) or B(bottom), the pin indicates the column number of the corresponding CFU. If [End] is L(left) or R(right), the pin indicates the row number of the corresponding CFU.
		[A/B] indicates differential signal pair information.
		LVDS indicates that the pin only supports LVDS output.
Multi-Function Pins		
IO[End][Row/Column Number][A/B]/MMM		/MMM represents one or more of the other functions in addition to being general purpose user I/O. When these functions are not in use, these pins can be used as user I/O.
D0	I/O	Data port D0 in CPU mode
D1	I/O	Data port D1 in CPU mode
D2	I/O	Data port D2 in CPU mode
D3	I/O	Data port D3 in CPU mode
D4	I/O	Data port D4 in CPU mode
D5	I/O	Data port D5 in CPU mode
D6	I/O	Data port D6 in CPU mode
D7	I/O	Data port D7 in CPU mode
WE_N	I	Select data input/output of D[7:0] in CPU mode.0: Write;1: Read.
DOUT	O	Data output in SERIAL mode
DIN	I, internal weak pull-down	Data input in SERIAL mode
TMS	I, internal weak pull-up	Serial mode input in JTAG mode
TCK	I	Serial clock input in JTAG mode
TDO	O	Serial data output in JTAG mode
TDI	I, internal weak pull-up	Serial data input in JTAG mode
JTAGSEL_N	I, internal weak pull-up	Reconfigure JTAG download function signal
RECONFIG_N	I, internal weak pull-up	Global reset GowinCONFIG logic signal, active low
FASTRD_N	I	Access SPI FLASH to select signal. Low, Fast Read mode; High, Read mode.
DONE[1]	O	High, the programming configuration has been completed successfully; Low, the programming configuration has not been completed or failed.
	I	When the DONE signal is low, delay the chip to activate. Activate the chip until the DONE signal is high.

Pin Name	I/O	Description
READY[1]	O	High, the device can be programmed and configured currently; Low, the device cannot be programmed and configured currently.
MI-1	I/O	MI in MSPI mode
MI-2	I/O	WPN in MSPI mode; data lane 2 in QMSPI mode
MI-3	I/O	HOLDN in MSPI mode; data lane 3 in QMSPI mode
MO	O	MO in MSPI mode
MCS_N	O	Enable signal MCS_N in MSPI mode, active-low
MCLK	O	Clock output MCLK in MSPI mode, with default frequency of 2.5Mhz
SCLK	I	Clock input in SSPI, SERIAL, and CPU modes
SO	I/O	SO in SSPI mode
SI	I/O	SI in SSPI mode
SSPI_CS_N	I/O	Enable signal SSPI_CS_N in SSPI mode, active-low, and internal weak pull-up
QSSPI_WPN	I	WPN in QSSPI mode; data lane 2 in QSSPI mode
CLKHOLD_N	I, internal weak pull-down	Active-high in SSPI mode; Active-low in CPU mode.
GCLKC_[x]	I	Differential input pin of GCLKT_[x], C(Comp), [x]: global clock No.[2]
GCLKT_[x]	I	Global clock input pin, T(True), [x]: global clock No.
LPLL_C_fb/RPLL_C_fb	I	Left/Right PLL feedback input pin, C(Comp)
LPLL_T_fb/RPLL_T_fb	I	Left/Right PLL feedback input pin, T(True)
LPLL_C_in/RPLL_C_in	I	Left/Right PLL clock input pin, C(Comp)
LPLL_T_in/RPLL_T_in	I	Left/Right PLL clock input pin, T(True)
MODE1	I, internal weak pull-down	Selection signal port in GowinCONFIG mode
MODE0	I, internal weak pull-down	Selection signal port in GowinCONFIG mode
Other Pins		
EXTR	NA	External 10K 1% resistor to ground
VSS	NA	Ground
VCC	NA	Power supply pin of core voltage
VCCIO#	NA	Power supply pin of I/O voltage for I/O BANK#
VCCX	NA	Power supply pin of auxiliary voltage

Note!
[1] The default state of READY/DONE is open-drain output, internal weak pull-up. DONE outputs 0 during configuration.
[2] When the input is single-ended, GCLKC_[x] pin is not a global clock pin.



Note!

[1] Each Bank has independent reference voltage (VREF).

[2] You can select to use IOB internal VREF (equals to 0.5 * VCCIO).

[3] You can also select to use external VREF input (use any IO pins as external VREF input).

Note!
[1] UV Version; The unpackaged MODE[1:0] is internally connected to 01.
[2] LV Version; The unpackaged MODE[1:0] is internally connected to 01.
[3] EV Version; The unpackaged MODE[1:0] is internally connected to 01.
[4] "Tie to VSS by 10K Resisitor" indicates the pin is connected to the ground with 10K resistance.

Pin Name	Function	BANK	DQS	Configuration Function	Differential Pair	LVDS	UG484[1]	UG484[2]	UG484[3]	UG400[1]	UG400[2]	UG400[3]	UG256[1]	UG256[2]	UG256[3]	PG256[1]	PG256[2]	PG256[3]	UG332[1]	UG332[2]	UG332[3]	UG324[1]	UG324[2]	UG324[3]	PG484[1]	PG484[2]	PG484[3]
EXTR	Ground	N/A					Tie to VSS by 10K Resisitor	Tie to VSS by 10K Resisitor	Tie to VSS by 10K Resisitor	Tie to VSS by 10K Resisitor	Tie to VSS by 10K Resisitor	Tie to VSS by 10K Resisitor	Tie to VSS by 10K Resisitor	Tie to VSS by 10K Resisitor	Tie to VSS by 10K Resisitor	Tie to VSS by 10K Resisitor	Tie to VSS by 10K Resisitor	Tie to VSS by 10K Resisitor	Tie to VSS by 10K Resisitor	Tie to VSS by 10K Resisitor	Tie to VSS by 10K Resisitor	Tie to VSS by 10K Resisitor	Tie to VSS by 10K Resisitor	Tie to VSS by 10K Resisitor	Tie to VSS by 10K Resisitor	Tie to VSS by 10K Resisitor	Tie to VSS by 10K Resisitor
IOB12A	I/O	5	DQ2		True_of_IOB12B	True	AA6	AA6	AA6	T7	T7	T7	T5	T5	T5	T5	T5	T5	U4	U4	U4	N7	N7	N7	W6	W6	W6
IOB12B	I/O	5	DQ2		Comp_of_IOB12A	True	AB6	AB6	AB6	T8	T8	T8	R6	R6	R6	R6	R6	R6	T7	T7	T7	P7	P7	P7	W7	W7	W7
IOB13A	I/O	5	DQ2		True_of_IOB13B	none	W6	W6	W6																AB5	AB5	AB5
IOB13B	I/O	5	DQ2		Comp_of_IOB13A	none	V7	V7	V7																Y6	Y6	Y6
IOB14A	I/O	5	DQ2		True_of_IOB14B	True	V8	V8	V8	W5	W5	W5	N6	N6	N6	N6	N6	N6	U6	U6	U6	N8	N8	N8	V8	V8	V8
IOB14B	I/O	5	DQ2		Comp_of_IOB14A	True	U8	U8	U8	Y5	Y5	Y5	L7	L7	L7	L7	L7	L7	T8	T8	T8	R7	R7	R7	W8	W8	W8
IOB15A	I/O	5	DQ2		True_of_IOB15B	none	AA8	AA7	AA7																V9	V9	V9
IOB15B	I/O	5	DQ2		Comp_of_IOB15A	none	AB8	AB7	AB7																W9	W9	W9
IOB16A	I/O	5	DQ2		True_of_IOB16B	True	V9	V9	V9	P9	P9	P9	R7	R7	R7	R7	R7	R7	Y7	Y7	Y7	V5	V5	V5	AB8	AB8	AB8
IOB16B	I/O	5	DQ2		Comp_of_IOB16A	True	W8	W8	W8	R9	R9	R9	P7	P7	P7	P7	P7	P7	V8	V8	V8	V6	V6	V6	Y9	Y9	Y9
IOB17A	I/O	5	DQ2		True_of_IOB17B	none	AA7	AA8	AA8													T7	T7	T7	AA7	AA7	AA7
IOB17B	I/O	5	DQ2		Comp_of_IOB17A	none	AB7	AB8	AB8													P8	P8	P8	AB7	AB7	AB7
IOB18A	I/O	5	DQ2		True_of_IOB18B	True	Y8	Y8	Y8	W7	W7	W7	M7	M7	M7	M7	M7	M7	U7	U7	U7	V7	V7	V7	U10	U10	U10
IOB18B	I/O	5	DQ2		Comp_of_IOB18A	True	W9	W9	W9	Y7	Y7	Y7	N7	N7	N7	N7	N7	N7	T9	T9	T9	U8	U8	U8	T10	T10	T10
IOB19A	I/O	5	DQ2		True_of_IOB19B	none	AA9	AA9	AA9	V8	V8	V8							U8	U8	U8	U7	U7	U7	Y8	Y8	Y8
IOB19B	I/O	5	DQ2		Comp_of_IOB19A	none	AB9	AB9	AB9	U9	U9	U9							U9	U9	U9	R8	R8	R8	AA8	AA8	AA8
IOB20A	I/O	5	DQ2		True_of_IOB20B	True	T10	T10	T10	V9	V9	V9	M6	M6	M6	M6	M6	M6	W8	W8	W8	R9	R9	R9	V10	V10	V10
IOB20B	I/O	5	DQ2		Comp_of_IOB20A	True	U10	U10	U10	T9	T9	T9	L8	L8	L8	L8	L8	L8	Y8	Y8	Y8	P9	P9	P9	Y11	Y11	Y11
IOB21A	I/O	5	DQS2		True_of_IOB21B	none	Y9	Y9	Y9	W8	W8	W8													U11	U11	U11
IOB21B	I/O	5	DQS2		Comp_of_IOB21A	none	Y10	Y10	Y10	Y8	Y8	Y8													T11	T11	T11
IOB22A	I/O	5	DQ2		True_of_IOB22B	True	V10	V10	V10	P10	P10	P10	P8	P8	P8	P8	P8	P8							U9	U9	U9
IOB22B	I/O	5	DQ2		Comp_of_IOB22A	True	W10	W10	W10	R10	R10	R10	T8	T8	T8	T8	T8	T8							T9	T9	T9
IOB23A/GCLKT_5	I/O	5	DQ2	GCLKT_5	True_of_IOB23B	none	AA10	AA10	AA10	W9	W9	W9	T7	T7	T7	T7	T7	T7	V9	V9	V9	T8	T8	T8	AA9	AA9	AA9
IOB23B/GCLKC_5	I/O	5	DQ2	GCLKC_5	Comp_of_IOB23A	none	AB10	AB10	AB10	Y9	Y9	Y9	R8	R8	R8	R8	R8	R8	W9	W9	W9	T9	T9	T9	Y10	Y10	Y10
IOB24A	I/O	5	DQ2		True_of_IOB24B	True	T11	T11	T11	Y10	Y10	Y10	N8	N8	N8	N8	N8	N8							AA10	AA10	AA10
IOB24B	I/O	5	DQ2		Comp_of_IOB24A	True	U11	U11	U11	W10	W10	W10	L9	L9	L9	L9	L9	L9							AB10	AB10	AB10
IOB25A	I/O	5	DQ2		True_of_IOB25B	none	AA11	AA11	AA11	U10	U10	U10							Y9	Y9	Y9	V8	V8	V8	AA11	AA11	AA11
IOB25B	I/O	5	DQ2		Comp_of_IOB25A	none	AB11	AB11	AB11	V10	V10	V10							V10	V10	V10	U9	U9	U9	AB11	AB11	AB11
IOB26A	I/O	5	DQ2		True_of_IOB26B	True	V11	V11	V11	U11	U11	U11	M8	M8	M8	M8	M8	M8	W10	W10	W10	N9	N9	N9	V11	V11	V11
IOB26B	I/O	5	DQ2		Comp_of_IOB26A	True	Y11	Y11	Y11	T10	T10	T10	N9	N9	N9	N9	N9	N9	Y10	Y10	Y10	N10	N10	N10	W11	W11	W11
IOB27A	I/O	5	DQ2		True_of_IOB27B	none	U12	U12	U12	Y11	Y11	Y11							W11	W11	W11	V9	V9	V9	AB12	AB12	AB12
IOB27B	I/O	5	DQ2		Comp_of_IOB27A	none	V12	V12	V12	W11	W11	W11							V11	V11	V11	U10	U10	U10	AA12	AA12	AA12
IOB2A	I/O	5	DQ1		True_of_IOB2B	True	AA2	AA2	AA2	W1	W1	W1	P4	P4	P4	P4	P4	P4	W4	W4	W4	V2	V2	V2	Y3	Y3	Y3
IOB2B	I/O	5	DQ1		Comp_of_IOB2A	True	AB2	AB2	AB2	Y1	Y1	Y1	T4	T4	T4	T4	T4	T4	Y4	Y4	Y4	U3	U3	U3	AA3	AA3	AA3
IOB30A/GCLKT_4	I/O	4	DQ3	GCLKT_4	True_of_IOB30B	True	AB12	AB12	AB12	Y12	Y12	Y12	T9	T9	T9	T9	T9	T9	Y12	Y12	Y12	V10	V10	V10	Y13	Y13	Y13
IOB30B/GCLKC_4	I/O	4	DQ3	GCLKC_4	Comp_of_IOB30A	True	AA12	AA12	AA12	W12	W12	W12	P9	P9	P9	P9	P9	P9	W12	W12	W12	U11	U11	U11	AA14	AA14	AA14
IOB31A	I/O	4	DQ3		True_of_IOB31B	none	Y12	Y12	Y12													T10	T10	T10	AB13	AB13	AB13
IOB31B	I/O	4	DQ3		Comp_of_IOB31A	none	T12	T12	T12													R10	R10	R10	AA13	AA13	AA13
IOB32A	I/O	4	DQ3		True_of_IOB32B	True	V13	V13	V13	P11	P11	P11	R9	R9	R9	R9	R9	R9	U10	U10	U10				Y14	Y14	Y14
IOB32B	I/O	4	DQ3		Comp_of_IOB32A	True	U13	U13	U13	R11	R11	R11	T10	T10	T10	T10	T10	T10	U11	U11	U11				AB15	AB15	AB15
IOB33A	I/O	4	DQ3		True_of_IOB33B	none	AB13	AB13	AB13	Y13	Y13	Y13							T11	T11	T11	P10	P10	P10	W12	W12	W12
IOB33B	I/O	4	DQ3		Comp_of_IOB33A	none	AA13	AA13	AA13	W13	W13	W13							U12	U12	U12	T11	T11	T11	V12	V12	V12
IOB34A	I/O	4	DQ3		True_of_IOB34B	True	Y13	Y13	Y13	V12	V12	V12	M9	M9	M9	M9	M9	M9				V11	V11	V11	AA15	AA15	AA15
IOB34B	I/O	4	DQ3		Comp_of_IOB34A	True	W13	W13	W13	V13	V13	V13	L10	L10	L10	L10	L10	L10				V12	V12	V12	Y15	Y15	Y15
IOB35A	I/O	4	DQ3		True_of_IOB35B	none	U14	U14	U14	U12	U12	U12							V12	V12	V12	N11	N11	N11	AA18	AA18	AA18
IOB35B	I/O	4	DQ3		Comp_of_IOB35A	none	V14	V14	V14	T11	T11	T11							Y13	Y13	Y13	R11	R11	R11	AB19	AB19	AB19
IOB36A	I/O	4	DQ3		True_of_IOB36B	True	T13	T13	T13	Y14	Y14	Y14	P10	P10	P10	P10	P10	P10	T12	T12	T12				Y12	Y12	Y12
IOB36B	I/O	4	DQ3		Comp_of_IOB36A	True	T14	T14	T14	W14	W14	W14	R10	R10	R10	R10	R10	R10	U13	U13	U13				V13	V13	V13
IOB37A	I/O	4	DQS3		True_of_IOB37B	none	AB14	AB14	AB14													U12	U12	U12	AB16	AB16	AB16
IOB37B	I/O	4	DQS3		Comp_of_IOB37A	none	AA14	AA14	AA14													V13	V13	V13	AA16	AA16	AA16
IOB38A	I/O	4	DQ3		True_of_IOB38B	True	Y14	Y14	Y14	Y15	Y15	Y15	N10	N10	N10	N10	N10	N10	W13	W13	W13	P11	P11	P11	T13	T13	T13
IOB38B	I/O	4	DQ3		Comp_of_IOB38A	True	W14	W14	W14	W15	W15	W15	M11	M11	M11	M11	M11	M11	Y14	Y14	Y14	T12	T12	T12	U13	U13	U13
IOB39A	I/O	4	DQ3		True_of_IOB39B	none	AB15	AB15	AB15	P12	P12	P12							V13	V13	V13	U13	U13	U13	Y16	Y16	Y16
IOB39B	I/O	4	DQ3		Comp_of_IOB39A	none	AA15	AA15	AA15	R12	R12	R12							T13	T13	T13	V14	V14	V14	AB17	AB17	AB17
IOB3A	I/O	5	DQ1		True_of_IOB3B	none	V6	V6	V6	R6	R6	R6							V4	V4	V4	R4	R4	R4	U6	U6	U6
IOB3B	I/O	5	DQ1		Comp_of_IOB3A	none	U6	U6	U6	T6	T6	T6							Y3	Y3	Y3	P6	P6	P6	V6	V6	V6
IOB40A	I/O	4	DQ3		True_of_IOB40B	True	Y15	Y15	Y15	Y16	Y16	Y16	T11	T11	T11	T11	T11	T11	W14	W14	W14				W14	W14	W14
IOB40B	I/O	4	DQ3		Comp_of_IOB40A	True	W15	W15	W15	W16	W16	W16	P11	P11	P11	P11	P11	P11	V14	V14	V14				V14	V14	V14
IOB41A	I/O	4	DQ3		True_of_IOB41B	none	AB16	AB16	AB16	T12	T12	T12										R12	R12	R12	U14	U14	U14
IOB41B	I/O	4	DQ3		Comp_of_IOB41A	none	AA16	AA16	AA16	T13	T13	T13										T13	T13	T13	T14	T14	T14
IOB42A	I/O	4	DQ3		True_of_IOB42B	True	V15	V15	V15	Y17	Y17	Y17	M10	M10	M10	M10	M10	M10	U14	U14	U14	U14	U14	U14	Y17	Y17	Y17
IOB42B	I/O	4	DQ3		Comp_of_IOB42A	True	U15	U15	U15	W17	W17	W17	N11	N11	N11	N11	N11	N11	V15	V15	V15	V15	V15	V15	AB18	AB18	AB18
IOB43A	I/O	4	DQ3		True_of_IOB43B	none	AB17	AB17	AB17													T14	T14	T14	W15	W15	W15
IOB43B	I/O	4	DQ3		Comp_of_IOB43A	none	AA17	AA17	AA17													N12	N12	N12	V15	V15	V15
IOB44A	I/O	4	DQ3		True_of_IOB44B	True	Y17	Y17	Y17	P13	P13	P13	R13	R13	R13	R13	R13	R13	U15	U15	U15				Y18	Y18	Y18
IOB44B	I/O	4	DQ3		Comp_of_IOB44A	True	V16	V16	V16	R13	R13	R13	T14	T14	T14	T14	T14	T14	T14	T14	T14				AA19	AA19	AA19
IOB45A	I/O	4	DQ3		True_of_IOB45B	none	Y18	Y18	Y18	V15	V15	V15							Y15	Y15	Y15	U15	U15	U15	W16	W16	W16
IOB45B	I/O	4	DQ3		Comp_of_IOB45A	none	W17	W17	W17	V16	V16	V16							W15	W15	W15	V16	V16	V16	W17	W17	W17

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IOB48A	I/O	4	DQS4		True_of_IOB48B	True	AB18	AB18	AB18	V14	V14	V14	R11	R11	R11	R11	R11	R11	Y16	Y16	Y16	P12	P12	P12	AB20	AB20	AB20
IOB48B	I/O	4	DQS4		Comp_of_IOB48A	True	AA18	AA18	AA18	U14	U14	U14	T12	T12	T12	T12	T12	T12	W16	W16	W16	R14	R14	R14	AB21	AB21	AB21
IOB49A	I/O	4	DQ4		True_of_IOB49B	none	AB19	AB19	AB19	Y18	Y18	Y18							U16	U16	U16	T15	T15	T15	T12	T12	T12
IOB49B	I/O	4	DQ4		Comp_of_IOB49A	none	AA19	AA19	AA19	W18	W18	W18							T15	T15	T15	T16	T16	T16	U12	U12	U12
IOB4A	I/O	5	DQ1		True_of_IOB4B	True	AA3	AA3	AA3	W2	W2	W2	T2	T2	T2	T2	T2	T2	V5	V5	V5	T3	T3	T3	W5	W5	W5
IOB4B	I/O	5	DQ1		Comp_of_IOB4A	True	AB3	AB3	AB3	Y2	Y2	Y2	R3	R3	R3	R3	R3	R3	W5	W5	W5	U4	U4	U4	Y4	Y4	Y4
IOB50A/SCLK	I/O	4	DQ4	SCLK	True_of_IOB50B	True	T9	T9	T9	W6	W6	W6	P6	P6	P6	P6	P6	P6	V7	V7	V7	T6	T6	T6	AB6	AB6	AB6
IOB50B/D1/SO	I/O	4	DQ4	D1/SO	Comp_of_IOB50A	True	U9	U9	U9	Y6	Y6	Y6	T6	T6	T6	T6	T6	T6	W7	W7	W7	U6	U6	U6	Y7	Y7	Y7
IOB51A/DIN/CLKHOLD_N	I/O	4	DQ4	DIN/CLKHOLD_N	True_of_IOB51B	none	T15	T15	T15	T14	T14	T14							V16	V16	V16				V16	V16	V16
IOB51B/DOUT/WE_N	I/O	4	DQ4	DOUT/WE_N	Comp_of_IOB51A	none	U16	U16	U16	U15	U15	U15							Y17	Y17	Y17				U15	U15	U15
IOB52A/FASTRD_N/D3	I/O	4	DQ4	FASTRD_N /D3	True_of_IOB52B	True	AB20	AB20	AB20	Y19	Y19	Y19	P12	P12	P12	P12	P12	P12							Y19	Y19	Y19
IOB52B/QSSPI_WPN	I/O	4	DQ4	QSSPI_WPN	Comp_of_IOB52A	True	AA20	AA20	AA20	W19	W19	W19	T13	T13	T13	T13	T13	T13							W18	W18	W18
IOB53A/D7	I/O	4	DQ4	D7	True_of_IOB53B	none	Y19	Y19	Y19	P14	P14	P14							W19	W19	W19	R13	R13	R13	T15	T15	T15
IOB53B/D6	I/O	4	DQ4	D6	Comp_of_IOB53A	none	W18	W18	W18	R14	R14	R14							Y19	Y19	Y19	R15	R15	R15	U16	U16	U16
IOB54A/SSPI_CS_N/D0	I/O	4	DQ4	SSPI_CS_N/D0	True_of_IOB54B	True	AB21	AB21	AB21	Y20	Y20	Y20	R12	R12	R12	R12	R12	R12	W17	W17	W17	U16	U16	U16	AA20	AA20	AA20
IOB54B/SI/D2	I/O	4	DQ4	SI/D2	Comp_of_IOB54A	True	AA21	AA21	AA21	W20	W20	W20	P13	P13	P13	P13	P13	P13	V17	V17	V17	V17	V17	V17	W19	W19	W19
IOB55A/D5	I/O	4	DQ4	D5	True_of_IOB55B	none	V17	V17	V17	T16	T16	T16	T15	T15	T15	T15	T15	T15	W18	W18	W18	P13	P13	P13	V17	V17	V17
IOB55B/D4	I/O	4	DQ4	D4	Comp_of_IOB55A	none	T16	T16	T16	R15	R15	R15	R14	R14	R14	R14	R14	R14	Y18	Y18	Y18	P14	P14	P14	T16	T16	T16
IOB5A	I/O	5	DQ1		True_of_IOB5B	none	Y4	Y4	Y4	P7	P7	P7							W3	W3	W3	P5	P5	P5	U7	U7	U7
IOB5B	I/O	5	DQ1		Comp_of_IOB5A	none	W5	W5	W5	R7	R7	R7							Y2	Y2	Y2	R6	R6	R6	T8	T8	T8
IOB6A	I/O	5	DQ1		True_of_IOB6B	True	U7	U7	U7	V6	V6	V6	R5	R5	R5	R5	R5	R5							AB2	AB2	AB2
IOB6B	I/O	5	DQ1		Comp_of_IOB6A	True	T8	T8	T8	U6	U6	U6	P5	P5	P5	P5	P5	P5							AB3	AB3	AB3
IOB7A	I/O	5	DQ1		True_of_IOB7B	none	AA4	AA4	AA4	W3	W3	W3							T6	T6	T6	V3	V3	V3	AB4	AB4	AB4
IOB7B	I/O	5	DQ1		Comp_of_IOB7A	none	AB4	AB4	AB4	Y3	Y3	Y3							U5	U5	U5	V4	V4	V4	AA5	AA5	AA5
IOB8A	I/O	5	DQ1		True_of_IOB8B	True	AA5	AA5	AA5	W4	W4	W4	T3	T3	T3	T3	T3	T3	Y5	Y5	Y5	R5	R5	R5	U8	U8	U8
IOB8B	I/O	5	DQ1		Comp_of_IOB8A	True	AB5	AB5	AB5	Y4	Y4	Y4	R4	R4	R4	R4	R4	R4	V6	V6	V6	T4	T4	T4	V7	V7	V7
IOB9A	I/O	5	DQS1		True_of_IOB9B	none	Y5	Y5	Y5	P8	P8	P8							W6	W6	W6	T5	T5	T5	AA4	AA4	AA4
IOB9B	I/O	5	DQS1		Comp_of_IOB9A	none	Y6	Y6	Y6	R8	R8	R8							Y6	Y6	Y6	U5	U5	U5	Y5	Y5	Y5
IOL11A	I/O	8	none		True_of_IOL11B	True	E1	E1	E1	H6	H6	H6							F2	F2	F2	E2	E2	E2	F4	F4	F4
IOL11B	I/O	8	none		Comp_of_IOL11A	True	F1	F1	F1	H7	H7	H7							F1	F1	F1	E1	E1	E1	G4	G4	G4
IOL12A	I/O	8	none		True_of_IOL12B	none	G3	G3	G3																F1	F1	F1
IOL12B	I/O	8	none		Comp_of_IOL12A	none	G4	G4	G4																G3	G3	G3
IOL13A	I/O	8	none		True_of_IOL13B	True	H4	H4	H4	F2	F2	F2							F5	F5	F5	F2	F2	F2	H5	H5	H5
IOL13B	I/O	8	none		Comp_of_IOL13A	True	H3	H3	H3	F1	F1	F1							G5	G5	G5	H5	H5	H5	H4	H4	H4
IOL14A/GCLKT_8	I/O	8	none	GCLKT_8	True_of_IOL14B	none	G2	G2	G2	E2	E2	E2	E1	E1	E1	E1	E1	E1	G3	G3	G3	G4	G4	G4	E1	E1	E1
IOL14B/GCLKC_8	I/O	8	none	GCLKC_8	Comp_of_IOL14A	none	G1	G1	G1	E1	E1	E1	F2	F2	F2	F2	F2	F2	G2	G2	G2	G3	G3	G3	F3	F3	F3
IOL15A	I/O	8	none		True_of_IOL15B	True	H2	H2	H2	G4	G4	G4	F4	F4	F4	F4	F4	F4				F1	F1	F1	D2	D2	D2
IOL15B	I/O	8	none		Comp_of_IOL15A	True	H1	H1	H1	G3	G3	G3	G6	G6	G6	G6	G6	G6				G6	G6	G6	E3	E3	E3
IOL16A	I/O	8	none		True_of_IOL16B	none	J7	J7	J7	H3	H3	H3	F3	F3	F3	F3	F3	F3	F4	F4	F4				J5	J5	J5
IOL16B	I/O	8	none		Comp_of_IOL16A	none	J6	J6	J6	H4	H4	H4	F1	F1	F1	F1	F1	F1	H5	H5	H5				J4	J4	J4
IOL17A	I/O	8	none		True_of_IOL17B	True	H5	H5	H5	G2	G2	G2	G5	G5	G5	G5	G5	G5	H2	H2	H2	G2	G2	G2	G2	G2	G2
IOL17B	I/O	8	none		Comp_of_IOL17A	True	J5	J5	J5	G1	G1	G1	G4	G4	G4	G4	G4	G4	H1	H1	H1	G1	G1	G1	G1	G1	G1
IOL18A	I/O	8	none		True_of_IOL18B	none	J4	J4	J4	J6	J6	J6							G4	G4	G4	H3	H3	H3	K6	K6	K6
IOL18B	I/O	8	none		Comp_of_IOL18A	none	J3	J3	J3	J5	J5	J5							J5	J5	J5	H4	H4	H4	K7	K7	K7
IOL19A	I/O	8	none		True_of_IOL19B	True	J2	J2	J2	H2	H2	H2	G2	G2	G2	G2	G2	G2	J3	J3	J3	H2	H2	H2	H3	H3	H3
IOL19B	I/O	8	none		Comp_of_IOL19A	True	J1	J1	J1	H1	H1	H1	G3	G3	G3	G3	G3	G3	J2	J2	J2	H1	H1	H1	H2	H2	H2
IOL20A	I/O	8	none		True_of_IOL20B	none	K7	K7	K7	J4	J4	J4	F5	F5	F5	F5	F5	F5	H4	H4	H4	H6	H6	H6	K5	K5	K5
IOL20B	I/O	8	none		Comp_of_IOL20A	none	K6	K6	K6	J3	J3	J3	H6	H6	H6	H6	H6	H6	J4	J4	J4	J1	J1	J1	L3	L3	L3
IOL21A	I/O	7	none		True_of_IOL21B	True	L7	L7	L7	J2	J2	J2	G1	G1	G1	G1	G1	G1	J1	J1	J1	J2	J2	J2	H1	H1	H1
IOL21B	I/O	7	none		Comp_of_IOL21A	True	K5	K5	K5	J1	J1	J1	H2	H2	H2	H2	H2	H2	K3	K3	K3	J5	J5	J5	J3	J3	J3
IOL22A	I/O	7	none		True_of_IOL22B	none	K4	K4	K4	K5	K5	K5	H4	H4	H4	H4	H4	H4	K2	K2	K2	J3	J3	J3	L5	L5	L5
IOL22B	I/O	7	none		Comp_of_IOL22A	none	K3	K3	K3	K4	K4	K4	J6	J6	J6	J6	J6	J6	K1	K1	K1	J7	J7	J7	L4	L4	L4
IOL23A	I/O	7	none		True_of_IOL23B	True	K2	K2	K2	K2	K2	K2													J2	J2	J2
IOL23B	I/O	7	none		Comp_of_IOL23A	True	K1	K1	K1	K1	K1	K1													K3	K3	K3
IOL24A	I/O	7	none		True_of_IOL24B	none	L6	L6	L6	K6	K6	K6	H3	H3	H3	H3	H3	H3	K4	K4	K4	J4	J4	J4	L6	L6	L6
IOL24B	I/O	7	none		Comp_of_IOL24A	none	L5	L5	L5	K7	K7	K7	H1	H1	H1	H1	H1	H1	L4	L4	L4	K3	K3	K3	L7	L7	L7
IOL25A/GCLKT_7	I/O	7	none	GCLKT_7	True_of_IOL25B	True	L1	L1	L1	L1	L1	L1	J1	J1	J1	J1	J1	J1	M1	M1	M1	K2	K2	K2	K2	K2	K2
IOL25B/GCLKC_7	I/O	7	none	GCLKC_7	Comp_of_IOL25A	True	M2	M2	M2	L2	L2	L2	J3	J3	J3	J3	J3	J3	M2	M2	M2	J6	J6	J6	K1	K1	K1
IOL26A	I/O	7	none		True_of_IOL26B	none	L3	L3	L3	L3	L3	L3													L2	L2	L2
IOL26B	I/O	7	none		Comp_of_IOL26A	none	L4	L4	L4	L4	L4	L4													L1	L1	L1
IOL27A/MO	I/O	9	none	MO	True_of_IOL27B	none																					
IOL27B/MI-1	I/O	9	none	MI-1	Comp_of_IOL27A	none																					
IOL27C/MI-2	I/O	9	none	MI-2	True_of_IOL27D	none																					
IOL27D/MI-3	I/O	9	none	MI-3	Comp_of_IOL27C	none																					
IOL27E/MCLK	I/O	9	none	MCLK	True_of_IOL27F	none																					
IOL27F/MCS_N	I/O	9	none	MCS_N	Comp_of_IOL27E	none																					
IOL28A	I/O	7	none		True_of_IOL28B	True	M1	M1	M1	M1	M1	M1	J2	J2	J2	J2	J2	J2	M3	M3	M3	K1	K1	K1	N1	N1	N1

Note!
[1] UV Version; The unpackaged MODE[1:0] is internally connected to 01.
[2] LV Version; The unpackaged MODE[1:0] is internally connected to 01.
[3] EV Version; The unpackaged MODE[1:0] is internally connected to 01.
[4] "Tie to VSS by 10K Resisitor" indicates the pin is connected to the ground with 10K resistance.

Pin Name	Function	BANK	DQS	Configuration Function	Differential Pair	LVDS	UG484[1]	UG484[2]	UG484[3]	UG400[1]	UG400[2]	UG400[3]	UG256[1]	UG256[2]	UG256[3]	PG256[1]	PG256[2]	PG256[3]	UG332[1]	UG332[2]	UG332[3]	UG324[1]	UG324[2]	UG324[3]	PG484[1]	PG484[2]	PG484[3]
IOL28B	I/O	7	none		Comp_of_IOL28A	True	N1	N1	N1	M2	M2	M2	K1	K1	K1	K1	K1	K1	N1	N1	N1	L1	L1	L1	N2	N2	N2
IOL29A	I/O	7	none		True_of_IOL29B	none	M6	M6	M6	M3	M3	M3							L2	L2	L2	K7	K7	K7	M1	M1	M1
IOL29B	I/O	7	none		Comp_of_IOL29A	none	M5	M5	M5	M4	M4	M4							L3	L3	L3	K5	K5	K5	M2	M2	M2
IOL2A	I/O	8	DQ0		True_of_IOL2B	True	D3	D3	D3	C4	C4	C4	B1	B1	B1	B1	B1	B1	D2	D2	D2	B1	B1	B1	C3	C3	C3
IOL2B	I/O	8	DQ0		Comp_of_IOL2A	True	D4	D4	D4	C3	C3	C3	C2	C2	C2	C2	C2	C2	D1	D1	D1	C2	C2	C2	C2	C2	C2
IOL30A	I/O	7	none		True_of_IOL30B	True	N2	N2	N2	L5	L5	L5	H5	H5	H5	H5	H5	H5							N3	N3	N3
IOL30B	I/O	7	none		Comp_of_IOL30A	True	P1	P1	P1	M5	M5	M5	J4	J4	J4	J4	J4	J4							P2	P2	P2
IOL31A	I/O	7	none		True_of_IOL31B	none	N3	N3	N3	L6	L6	L6													M7	M7	M7
IOL31B	I/O	7	none		Comp_of_IOL31A	none	N4	N4	N4	L7	L7	L7													M6	M6	M6
IOL32A	I/O	7	none		True_of_IOL32B	True	P2	P2	P2	N1	N1	N1	K3	K3	K3	K3	K3	K3	N2	N2	N2	K4	K4	K4	P3	P3	P3
IOL32B	I/O	7	none		Comp_of_IOL32A	True	R1	R1	R1	N2	N2	N2	K2	K2	K2	K2	K2	K2	N3	N3	N3	L2	L2	L2	R1	R1	R1
IOL33A	I/O	7	none		True_of_IOL33B	none	P3	P3	P3	P1	P1	P1	J5	J5	J5	J5	J5	J5	L1	L1	L1	K6	K6	K6	M4	M4	M4
IOL33B	I/O	7	none		Comp_of_IOL33A	none	M7	M7	M7	P2	P2	P2	K6	K6	K6	K6	K6	K6	M4	M4	M4	L3	L3	L3	M5	M5	M5
IOL34A	I/O	6	none		True_of_IOL34B	True	P4	P4	P4	N3	N3	N3							P1	P1	P1	L4	L4	L4	R2	R2	R2
IOL34B	I/O	6	none		Comp_of_IOL34A	True	N5	N5	N5	N4	N4	N4							P2	P2	P2	M2	M2	M2	R3	R3	R3
IOL35A	I/O	6	none		True_of_IOL35B	none	N6	N6	N6													M1	M1	M1	M3	M3	M3
IOL35B	I/O	6	none		Comp_of_IOL35A	none	N7	N7	N7													L6	L6	L6	N5	N5	N5
IOL36A	I/O	6	none		True_of_IOL36B	True	R2	R2	R2	M6	M6	M6	L1	L1	L1	L1	L1	L1	M5	M5	M5				U3	U3	U3
IOL36B	I/O	6	none		Comp_of_IOL36A	True	T1	T1	T1	M7	M7	M7	L3	L3	L3	L3	L3	L3	N4	N4	N4				V1	V1	V1
IOL37A	I/O	6	none		True_of_IOL37B	none	P5	P5	P5													N1	N1	N1	N7	N7	N7
IOL37B	I/O	6	none		Comp_of_IOL37A	none	P6	P6	P6													N2	N2	N2	N6	N6	N6
IOL38A	I/O	6	none		True_of_IOL38B	True	R3	R3	R3	P3	P3	P3							P3	P3	P3	M3	M3	M3	R5	R5	R5
IOL38B	I/O	6	none		Comp_of_IOL38A	True	R4	R4	R4	P4	P4	P4							R1	R1	R1	L5	L5	L5	P5	P5	P5
IOL39A	I/O	6	none		True_of_IOL39B	none	R5	R5	R5																W1	W1	W1
IOL39B	I/O	6	none		Comp_of_IOL39A	none	P7	P7	P7																V2	V2	V2
IOL3A	I/O	8	DQ0		True_of_IOL3B	none	F6	F6	F6	F6	F6	F6							D3	D3	D3				F6	F6	F6
IOL3B	I/O	8	DQ0		Comp_of_IOL3A	none	G7	G7	G7	G6	G6	G6							C1	C1	C1				F5	F5	F5
IOL40A	I/O	6	none		True_of_IOL40B	True	T2	T2	T2	R1	R1	R1	K4	K4	K4	K4	K4	K4	N5	N5	N5	M5	M5	M5	P7	P7	P7
IOL40B	I/O	6	none		Comp_of_IOL40A	True	U1	U1	U1	R2	R2	R2	L5	L5	L5	L5	L5	L5	P4	P4	P4	N3	N3	N3	P6	P6	P6
IOL41A	I/O	6	none		True_of_IOL41B	none	R6	R6	R6													R1	R1	R1	T4	T4	T4
IOL41B	I/O	6	none		Comp_of_IOL41A	none	R7	R7	R7													P3	P3	P3	U4	U4	U4
IOL42A	I/O	6	none		True_of_IOL42B	True	T3	T3	T3	T1	T1	T1							P5	P5	P5				R4	R4	R4
IOL42B	I/O	6	none		Comp_of_IOL42A	True	T4	T4	T4	T2	T2	T2							R4	R4	R4				P4	P4	P4
IOL43A	I/O	6	none		True_of_IOL43B	none	T5	T5	T5	N5	N5	N5										P2	P2	P2	Y1	Y1	Y1
IOL43B	I/O	6	none		Comp_of_IOL43A	none	T6	T6	T6	N6	N6	N6										M6	M6	M6	AA1	AA1	AA1
IOL44A/GCLKT_6	I/O	6	none	GCLKT_6	True_of_IOL44B	True	U2	U2	U2	U1	U1	U1	L2	L2	L2	L2	L2	L2	R2	R2	R2	P1	P1	P1	V3	V3	V3
IOL44B/GCLKC_6	I/O	6	none	GCLKC_6	Comp_of_IOL44A	True	V1	V1	V1	U2	U2	U2	M1	M1	M1	M1	M1	M1	R3	R3	R3	M4	M4	M4	W2	W2	W2
IOL45A	I/O	6	none		True_of_IOL45B	none	U3	U3	U3	R3	R3	R3							T1	T1	T1				T5	T5	T5
IOL45B	I/O	6	none		Comp_of_IOL45A	none	U4	U4	U4	R4	R4	R4							T2	T2	T2				R6	R6	R6
IOL46A	I/O	6	none		True_of_IOL46B	True	W1	W1	W1	T3	T3	T3	K5	K5	K5	K5	K5	K5	R5	R5	R5	N4	N4	N4	T2	T2	T2
IOL46B	I/O	6	none		Comp_of_IOL46A	True	W2	W2	W2	T4	T4	T4	L4	L4	L4	L4	L4	L4	T4	T4	T4	T1	T1	T1	T3	T3	T3
IOL47A	I/O	6	none		True_of_IOL47B	none	V4	V4	V4	V1	V1	V1	N2	N2	N2	N2	N2	N2				R2	R2	R2	W3	W3	W3
IOL47B	I/O	6	none		Comp_of_IOL47A	none	U5	U5	U5	V2	V2	V2	P1	P1	P1	P1	P1	P1				U1	U1	U1	V4	V4	V4
IOL48A	I/O	6	none		True_of_IOL48B	True	Y1	Y1	Y1	V3	V3	V3	M3	M3	M3	M3	M3	M3	T3	T3	T3				R7	R7	R7
IOL48B	I/O	6	none		Comp_of_IOL48A	True	AA1	AA1	AA1	V4	V4	V4	N1	N1	N1	N1	N1	N1	U1	U1	U1				T6	T6	T6
IOL49A	I/O	6	none		True_of_IOL49B	none	W3	W3	W3	P5	P5	P5							W2	W2	W2	T2	T2	T2	U1	U1	U1
IOL49B	I/O	6	none		Comp_of_IOL49A	none	Y2	Y2	Y2	P6	P6	P6							W1	W1	W1	N5	N5	N5	T1	T1	T1
IOL4A/LPLL1_T_fb	I/O	8	DQ0	LPLL1_T_fb	True_of_IOL4B	True	E4	E4	E4	C2	C2	C2	D3	D3	D3	D3	D3	D3	E3	E3	E3	E4	E4	E4	E4	E4	E4
IOL4B/LPLL1_C_fb	I/O	8	DQ0	LPLL1_C_fb	Comp_of_IOL4A	True	F5	F5	F5	C1	C1	C1	D1	D1	D1	D1	D1	D1	E2	E2	E2	F4	F4	F4	D3	D3	D3
IOL50A	I/O	6	none		True_of_IOL50B	True	Y3	Y3	Y3	T5	T5	T5	M2	M2	M2	M2	M2	M2	U2	U2	U2	P4	P4	P4	Y2	Y2	Y2
IOL50B	I/O	6	none		Comp_of_IOL50A	True	W4	W4	W4	R5	R5	R5	N3	N3	N3	N3	N3	N3	U3	U3	U3	R3	R3	R3	W4	W4	W4
IOL51A	I/O	6	none		True_of_IOL51B	none	V5	V5	V5	U4	U4	U4	R1	R1	R1	R1	R1	R1	V2	V2	V2				U5	U5	U5
IOL51B	I/O	6	none		Comp_of_IOL51A	none	T7	T7	T7	U5	U5	U5	P2	P2	P2	P2	P2	P2	V1	V1	V1				T7	T7	T7
IOL5A/LPLL1_T_in	I/O	8	DQ0	LPLL1_T_in	True_of_IOL5B	none	C1	C1	C1	D2	D2	D2	E2	E2	E2	E2	E2	E2	E1	E1	E1	D2	D2	D2	B1	B1	B1
IOL5B/LPLL1_C_in	I/O	8	DQ0	LPLL1_C_in	Comp_of_IOL5A	none	D2	D2	D2	D1	D1	D1	E3	E3	E3	E3	E3	E3	F3	F3	F3	G5	G5	G5	C1	C1	C1
IOL6A	I/O	8	DQS0		True_of_IOL6B	True	G6	G6	G6	E4	E4	E4										D3	D3	D3	G6	G6	G6
IOL6B	I/O	8	DQS0		Comp_of_IOL6A	True	H7	H7	H7	E3	E3	E3										C1	C1	C1	H7	H7	H7
IOL7A	I/O	8	DQ0		True_of_IOL7B	none	G5	G5	G5	F5	F5	F5							C2	C2	C2				H6	H6	H6
IOL7B	I/O	8	DQ0		Comp_of_IOL7A	none	H6	H6	H6	G5	G5	G5							B1	B1	B1				G5	G5	G5
IOL8A	I/O	8	DQ0		True_of_IOL8B	True	D1	D1	D1				C1	C1	C1	C1	C1	C1	G1	G1	G1	E3	E3	E3	J6	J6	J6
IOL8B	I/O	8	DQ0		Comp_of_IOL8A	True	E2	E2	E2				D2	D2	D2	D2	D2	D2	H3	H3	H3	F5	F5	F5	J7	J7	J7
IOL9A	I/O	8	DQ0		True_of_IOL9B	none	E3	E3	E3	F4	F4	F4							E4	E4	E4	F3	F3	F3	E2	E2	E2
IOL9B	I/O	8	DQ0		Comp_of_IOL9A	none	F4	F4	F4	F3	F3	F3							D4	D4	D4	D1	D1	D1	D1	D1	D1
IOR11A	I/O	2	none		True_of_IOR11B	True	G21	G21	G21	G16	G16	G16	E16	E16	E16	E16	E16	E16	F17	F17	F17				F19	F19	F19
IOR11B	I/O	2	none		Comp_of_IOR11A	True	G20	G20	G20	F18	F18	F18	F15	F15	F15	F15	F15	F15	G16	G16	G16				G19	G19	G19
IOR12A	I/O	2	none		True_of_IOR12B	none	G19	G19	G19	G17	G17	G17							F20	F20	F20	E17	E17	E17	E21	E21	E21
IOR12B	I/O	2	none		Comp_of_IOR12A	none	G18	G18	G18	E20	E20	E20							G18	G18	G18	D18	D18	D18	D22	D22	D22
IOR13A	I/O	2	none		True_of_IOR13B	True	H22	H22	H22	F19	F19	F19	F13	F13	F13	F13	F13	F13	G17	G17	G17	G16	G16	G16	J17	J17	J17
IOR13B	I/O	2	none		Comp_of_IOR13A	True	H21	H21	H21	F20	F20	F20	G12	G12	G12	G12	G12	G12	H16	H16	H16	H15	H15	H15	J16	J16	J16
IOR14A	I/O	2	none		True_of_IOR14B	none	G17	G17	G17													H14	H14	H14	E22	E22	E22
IOR14B	I/O	2	none		Comp_of_IOR14A	none	H20	H20	H20													F17	F17	F17	F20	F20	F20
IOR15A	I/O	2	none		True_of_IOR15B	True	H19	H19	H19	J14	J14	J14	F14	F14	F14	F14	F14	F14				E18	E18	E18	J20	J20	J20

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Note!
[1] UV Version; The unpackaged MODE[1:0] is internally connected to 01.
[2] LV Version; The unpackaged MODE[1:0] is internally connected to 01.
[3] EV Version; The unpackaged MODE[1:0] is internally connected to 01.
[4] "Tie to VSS by 10K Resisitor" indicates the pin is connected to the ground with 10K resistance.

Pin Name	Function	BANK	DQS	Configuration Function	Differential Pair	LVDS	UG484[1]	UG484[2]	UG484[3]	UG400[1]	UG400[2]	UG400[3]	UG256[1]	UG256[2]	UG256[3]	PG256[1]	PG256[2]	PG256[3]	UG332[1]	UG332[2]	UG332[3]	UG324[1]	UG324[2]	UG324[3]	PG484[1]	PG484[2]	PG484[3]
IOR15B	I/O	2	none		Comp_of_IOR15A	True	H18	H18	H18	J15	J15	J15	F16	F16	F16	F16	F16	F16				G17	G17	G17	G20	G20	G20
IOR16A	I/O	2	none		True_of_IOR16B	none	H17	H17	H17	G19	G19	G19							G19	G19	G19				G21	G21	G21
IOR16B	I/O	2	none		Comp_of_IOR16A	none	H16	H16	H16	H17	H17	H17							G20	G20	G20				G22	G22	G22
IOR17A	I/O	2	none		True_of_IOR17B	True	J18	J18	J18	H18	H18	H18	F12	F12	F12	F12	F12	F12	H17	H17	H17	H16	H16	H16	J18	J18	J18
IOR17B	I/O	2	none		Comp_of_IOR17A	True	J19	J19	J19	H19	H19	H19	G13	G13	G13	G13	G13	G13	J16	J16	J16	F18	F18	F18	J19	J19	J19
IOR18A	I/O	2	none		True_of_IOR18B	none	J16	J16	J16	H16	H16	H16							H18	H18	H18	J15	J15	J15	K17	K17	K17
IOR18B	I/O	2	none		Comp_of_IOR18A	none	J17	J17	J17	G20	G20	G20							H19	H19	H19	H17	H17	H17	K16	K16	K16
IOR19A	I/O	2	none		True_of_IOR19B	True	J21	J21	J21	J17	J17	J17	G15	G15	G15	G15	G15	G15							H20	H20	H20
IOR19B	I/O	2	none		Comp_of_IOR19A	True	J22	J22	J22	H20	H20	H20	G14	G14	G14	G14	G14	G14							H21	H21	H21
IOR20A	I/O	2	none		True_of_IOR20B	none	J20	J20	J20	J18	J18	J18							J17	J17	J17	J13	J13	J13	K18	K18	K18
IOR20B	I/O	2	none		Comp_of_IOR20A	none	K20	K20	K20	J16	J16	J16							K16	K16	K16	G18	G18	G18	L20	L20	L20
IOR21A	I/O	2	none		True_of_IOR21B	True	K19	K19	K19	K14	K14	K14	G11	G11	G11	G11	G11	G11	H20	H20	H20	J16	J16	J16	H22	H22	H22
IOR21B	I/O	2	none		Comp_of_IOR21A	True	K18	K18	K18	K15	K15	K15	H12	H12	H12	H12	H12	H12	J18	J18	J18	J17	J17	J17	F22	F22	F22
IOR22A	I/O	2	none		True_of_IOR22B	none	K17	K17	K17																J21	J21	J21
IOR22B	I/O	2	none		Comp_of_IOR22A	none	K16	K16	K16																K20	K20	K20
IOR23A	I/O	2	none		True_of_IOR23B	True	L17	L17	L17	J19	J19	J19	G16	G16	G16	G16	G16	G16							L17	L17	L17
IOR23B	I/O	2	none		Comp_of_IOR23A	True	L16	L16	L16	J20	J20	J20	H15	H15	H15	H15	H15	H15							L16	L16	L16
IOR24A	I/O	2	none		True_of_IOR24B	none	L19	L19	L19													J14	J14	J14	K21	K21	K21
IOR24B	I/O	2	none		Comp_of_IOR24A	none	L20	L20	L20													J12	J12	J12	K22	K22	K22
IOR25A	I/O	2	none		True_of_IOR25B	True	K22	K22	K22	K17	K17	K17	H13	H13	H13	H13	H13	H13	K17	K17	K17				L21	L21	L21
IOR25B	I/O	2	none		Comp_of_IOR25A	True	L21	L21	L21	K18	K18	K18	J12	J12	J12	J12	J12	J12	L17	L17	L17				L22	L22	L22
IOR26A	I/O	2	none		True_of_IOR26B	none	L22	L22	L22																M22	M22	M22
IOR26B	I/O	2	none		Comp_of_IOR26A	none	M17	M17	M17																M21	M21	M21
IOR28A/GCLKT_3	I/O	3	none	GCLKT_3	True_of_IOR28B	True	M22	M22	M22	K19	K19	K19	H14	H14	H14	H14	H14	H14	J19	J19	J19	H18	H18	H18	N22	N22	N22
IOR28B/GCLKC_3	I/O	3	none	GCLKC_3	Comp_of_IOR28A	True	M21	M21	M21	K20	K20	K20	H16	H16	H16	H16	H16	H16	J20	J20	J20	K15	K15	K15	N21	N21	N21
IOR29A	I/O	3	none		True_of_IOR29B	none	M20	M20	M20	K16	K16	K16	J16	J16	J16	J16	J16	J16	L18	L18	L18	K16	K16	K16	N20	N20	N20
IOR29B	I/O	3	none		Comp_of_IOR29A	none	M19	M19	M19	L17	L17	L17	J14	J14	J14	J14	J14	J14	M20	M20	M20	K17	K17	K17	P21	P21	P21
IOR2A/RPLL1_T_fb	I/O	2	DQ5	RPLL1_T_fb	True_of_IOR2B	True	C21	C21	C21	D17	D17	D17	D14	D14	D14	D14	D14	D14	D18	D18	D18	B18	B18	B18	D19	D19	D19
IOR2B/RPLL1_C_fb	I/O	2	DQ5	RPLL1_C_fb	Comp_of_IOR2A	True	C22	C22	C22	C18	C18	C18	E15	E15	E15	E15	E15	E15	D19	D19	D19	C17	C17	C17	C21	C21	C21
IOR30A	I/O	3	none		True_of_IOR30B	True	M16	M16	M16	L19	L19	L19	J15	J15	J15	J15	J15	J15	L20	L20	L20	K12	K12	K12	M16	M16	M16
IOR30B	I/O	3	none		Comp_of_IOR30A	True	N16	N16	N16	L20	L20	L20	K16	K16	K16	K16	K16	K16	L19	L19	L19	K13	K13	K13	M17	M17	M17
IOR31A	I/O	3	none		True_of_IOR31B	none	N17	N17	N17	L14	L14	L14	H11	H11	H11	H11	H11	H11	M19	M19	M19				P20	P20	P20
IOR31B	I/O	3	none		Comp_of_IOR31A	none	N18	N18	N18	L15	L15	L15	J13	J13	J13	J13	J13	J13	M18	M18	M18				R22	R22	R22
IOR32A	I/O	3	none		True_of_IOR32B	True	N22	N22	N22	M20	M20	M20	K14	K14	K14	K14	K14	K14	K18	K18	K18	K18	K18	K18	M19	M19	M19
IOR32B	I/O	3	none		Comp_of_IOR32A	True	P21	P21	P21	M19	M19	M19	K15	K15	K15	K15	K15	K15	K19	K19	K19	L16	L16	L16	M18	M18	M18
IOR33A	I/O	3	none		True_of_IOR33B	none	N20	N20	N20	L16	L16	L16							M17	M17	M17	L15	L15	L15	R21	R21	R21
IOR33B	I/O	3	none		Comp_of_IOR33A	none	N19	N19	N19	M18	M18	M18							N17	N17	N17	L13	L13	L13	R20	R20	R20
IOR34A	I/O	3	none		True_of_IOR34B	True	R22	R22	R22	M17	M17	M17	J11	J11	J11	J11	J11	J11	N20	N20	N20				V20	V20	V20
IOR34B	I/O	3	none		Comp_of_IOR34A	True	R21	R21	R21	N20	N20	N20	L12	L12	L12	L12	L12	L12	N19	N19	N19				W21	W21	W21
IOR35A	I/O	3	none		True_of_IOR35B	none	P22	P22	P22													L17	L17	L17	M20	M20	M20
IOR35B	I/O	3	none		Comp_of_IOR35A	none	P20	P20	P20													M16	M16	M16	N18	N18	N18
IOR36A	I/O	3	none		True_of_IOR36B	True	T22	T22	T22	M16	M16	M16	L16	L16	L16	L16	L16	L16	M16	M16	M16	L18	L18	L18	T22	T22	T22
IOR36B	I/O	3	none		Comp_of_IOR36A	True	T21	T21	T21	N19	N19	N19	L14	L14	L14	L14	L14	L14	P17	P17	P17	M18	M18	M18	T21	T21	T21
IOR37A	I/O	3	none		True_of_IOR37B	none	P19	P19	P19													M17	M17	M17	N16	N16	N16
IOR37B	I/O	3	none		Comp_of_IOR37A	none	P18	P18	P18													N18	N18	N18	N17	N17	N17
IOR38A	I/O	3	none		True_of_IOR38B	True	P17	P17	P17	N18	N18	N18	K13	K13	K13	K13	K13	K13	P19	P19	P19	L14	L14	L14	T20	T20	T20
IOR38B	I/O	3	none		Comp_of_IOR38A	True	P16	P16	P16	N17	N17	N17	K12	K12	K12	K12	K12	K12	P18	P18	P18	N17	N17	N17	U22	U22	U22
IOR39A	I/O	3	none		True_of_IOR39B	none	U22	U22	U22	P20	P20	P20							N16	N16	N16				P19	P19	P19
IOR39B	I/O	3	none		Comp_of_IOR39A	none	U21	U21	U21	P19	P19	P19							R17	R17	R17				P18	P18	P18
IOR3A	I/O	2	DQ5		True_of_IOR3B	none	F17	F17	F17	F15	F15	F15							C20	C20	C20	F14	F14	F14	G16	G16	G16
IOR3B	I/O	2	DQ5		Comp_of_IOR3A	none	G16	G16	G16	G15	G15	G15							C19	C19	C19	D16	D16	D16	F18	F18	F18
IOR40A	I/O	3	none		True_of_IOR40B	True	V22	V22	V22	P18	P18	P18	L15	L15	L15	L15	L15	L15	R20	R20	R20	K14	K14	K14	P16	P16	P16
IOR40B	I/O	3	none		Comp_of_IOR40A	True	W22	W22	W22	R20	R20	R20	M16	M16	M16	M16	M16	M16	R19	R19	R19	J18	J18	J18	P17	P17	P17
IOR41A	I/O	3	none		True_of_IOR41B	none	R20	R20	R20	M15	M15	M15							P16	P16	P16	M15	M15	M15	U20	U20	U20
IOR41B	I/O	3	none		Comp_of_IOR41A	none	R19	R19	R19	M14	M14	M14							R16	R16	R16	P18	P18	P18	V22	V22	V22
IOR42A	I/O	3	none		True_of_IOR42B	True	R18	R18	R18	N16	N16	N16	K11	K11	K11	K11	K11	K11	R18	R18	R18	M14	M14	M14	R19	R19	R19
IOR42B	I/O	3	none		Comp_of_IOR42A	True	R17	R17	R17	R19	R19	R19	L13	L13	L13	L13	L13	L13	T20	T20	T20	N16	N16	N16	R18	R18	R18
IOR43A	I/O	3	none		True_of_IOR43B	none	R16	R16	R16	T20	T20	T20										P17	P17	P17	W22	W22	W22
IOR43B	I/O	3	none		Comp_of_IOR43A	none	T20	T20	T20	T19	T19	T19										N15	N15	N15	V21	V21	V21
IOR44A	I/O	3	none		True_of_IOR44B	True	T19	T19	T19	U20	U20	U20	M14	M14	M14	M14	M14	M14	U17	U17	U17				T19	T19	T19
IOR44B	I/O	3	none		Comp_of_IOR44A	True	T18	T18	T18	P17	P17	P17	M15	M15	M15	M15	M15	M15	T17	T17	T17				U19	U19	U19
IOR45A	I/O	3	none		True_of_IOR45B	none	T17	T17	T17	T18	T18	T18							T19	T19	T19	R18	R18	R18	L18	L18	L18
IOR45B	I/O	3	none		Comp_of_IOR45A	none	U20	U20	U20	U19	U19	U19							T18	T18	T18	M13	M13	M13	L19	L19	L19
IOR46A	I/O	3	none		True_of_IOR46B	True	Y22	Y22	Y22	V20	V20	V20	N15	N15	N15	N15	N15	N15	W20	W20	W20	P16	P16	P16	Y22	Y22	Y22
IOR46B	I/O	3	none		Comp_of_IOR46A	True	W21	W21	W21	P16	P16	P16	P16	P16	P16	P16	P16	P16	V19	V19	V19	T18	T18	T18	AA22	AA22	AA22
IOR47A	I/O	3	none		True_of_IOR47B	none	U19	U19	U19	N15	N15	N15										R17	R17	R17	T18	T18	T18
IOR47B	I/O	3	none		Comp_of_IOR47A	none	U18	U18	U18	N14	N14	N14										N14	N14	N14	R17	R17	R17
IOR48A	I/O	3	none		True_of_IOR48B	True	AA22	AA22	AA22	R17	R17	R17	N16	N16	N16	N16	N16	N16	N18	N18	N18				W20	W20	W20
IOR48B	I/O	3	none		Comp_of_IOR48A	True	Y21	Y21	Y21	U18	U18	U18	N14	N14	N14	N14	N14	N14	P20	P20	P20				V19	V19	V19
IOR49A	I/O	3	none		True_of_IOR49B	none	U17	U17	U17	P15	P15	P15							U20	U20	U20	P15	P15	P15	R16	R16	R16
IOR49B	I/O	3	none		Comp_of_IOR49A	none	V19	V19	V19	R16	R16	R16							U19	U19	U19	U18	U18	U18	T17	T17	T17
IOR4A/RPLL1_T_in	I/O	2	DQ5	RPLL1_T_in	True_of_IOR4B	True	D22	D22	D22	C19	C19	C19	D16	D16	D16	D16	D16	D16	D20	D20	D20	E15	E15	E15	E19	E19	E19

Note!
[1] UV Version; The unpackaged MODE[1:0] is internally connected to 01.
[2] LV Version; The unpackaged MODE[1:0] is internally connected to 01.
[3] EV Version; The unpackaged MODE[1:0] is internally connected to 01.
[4] "Tie to VSS by 10K Resisitor" indicates the pin is connected to the ground with 10K resistance.

Pin Name	Function	BANK	DQS	Configuration Function	Differential Pair	LVDS	UG484[1]	UG484[2]	UG484[3]	UG400[1]	UG400[2]	UG400[3]	UG256[1]	UG256[2]	UG256[3]	PG256[1]	PG256[2]	PG256[3]	UG332[1]	UG332[2]	UG332[3]	UG324[1]	UG324[2]	UG324[3]	PG484[1]	PG484[2]	PG484[3]
IOR4B/RPLL1_C_in	I/O	2	DQ5	RPLL1_C_in	Comp_of_IOR4A	True	D21	D21	D21	E17	E17	E17	E14	E14	E14	E14	E14	E14	E18	E18	E18	C18	C18	C18	D20	D20	D20
IOR50A	I/O	3	none		True_of_IOR50B	True	V18	V18	V18	V19	V19	V19	P15	P15	P15	P15	P15	P15	V20	V20	V20	R16	R16	R16	Y21	Y21	Y21
IOR50B	I/O	3	none		Comp_of_IOR50A	True	W20	W20	W20	T17	T17	T17	R16	R16	R16	R16	R16	R16	U18	U18	U18	T17	T17	T17	Y20	Y20	Y20
IOR51A	I/O	3	none		True_of_IOR51B	none	W19	W19	W19	U17	U17	U17													U18	U18	U18
IOR51B	I/O	3	none		Comp_of_IOR51A	none	Y20	Y20	Y20	V17	V17	V17													U17	U17	U17
IOR5A	I/O	2	DQ5		True_of_IOR5B	none	D19	D19	D19	F16	F16	F16							B20	B20	B20	G13	G13	G13	G17	G17	G17
IOR5B	I/O	2	DQ5		Comp_of_IOR5A	none	D20	D20	D20	D18	D18	D18							B19	B19	B19	G14	G14	G14	H16	H16	H16
IOR6A	I/O	2	DQS5		True_of_IOR6B	True	E22	E22	E22	B20	B20	B20	C15	C15	C15	C15	C15	C15							B22	B22	B22
IOR6B	I/O	2	DQS5		Comp_of_IOR6A	True	E21	E21	E21	C20	C20	C20	B16	B16	B16	B16	B16	B16							C22	C22	C22
IOR7A	I/O	2	DQ5		True_of_IOR7B	none	E19	E19	E19	H14	H14	H14							E19	E19	E19	F15	F15	F15	H17	H17	H17
IOR7B	I/O	2	DQ5		Comp_of_IOR7A	none	E20	E20	E20	H15	H15	H15							E20	E20	E20	D17	D17	D17	G18	G18	G18
IOR8A	I/O	2	DQ5		True_of_IOR8B	True	F22	F22	F22	D19	D19	D19	C16	C16	C16	C16	C16	C16	E17	E17	E17	E16	E16	E16	H18	H18	H18
IOR8B	I/O	2	DQ5		Comp_of_IOR8A	True	G22	G22	G22	F17	F17	F17	D15	D15	D15	D15	D15	D15	F16	F16	F16	H13	H13	H13	H19	H19	H19
IOR9A	I/O	2	DQ5		True_of_IOR9B	none	F18	F18	F18	D20	D20	D20							F18	F18	F18	G15	G15	G15	D21	D21	D21
IOR9B	I/O	2	DQ5		Comp_of_IOR9A	none	F19	F19	F19	E19	E19	E19							F19	F19	F19	F16	F16	F16	E20	E20	E20
IOT12A	I/O	0	DQ8		True_of_IOT12B	True	B5	B5	B5	B4	B4	B4	A3	A3	A3	A3	A3	A3	C6	C6	C6	A4	A4	A4	A5	A5	A5
IOT12B	I/O	0	DQ8		Comp_of_IOT12A	True	A6	A6	A6	A4	A4	A4	B4	B4	B4	B4	B4	B4	D7	D7	D7	A5	A5	A5	C6	C6	C6
IOT13A	I/O	0	DQ8		True_of_IOT13B	none	D6	D6	D6	C6	C6	C6													B4	B4	B4
IOT13B	I/O	0	DQ8		Comp_of_IOT13A	none	E7	E7	E7	D7	D7	D7													C5	C5	C5
IOT14A	I/O	0	DQ8		True_of_IOT14B	True	B6	B6	B6	B5	B5	B5	D6	D6	D6	D6	D6	D6	A7	A7	A7	B6	B6	B6	E9	E9	E9
IOT14B	I/O	0	DQ8		Comp_of_IOT14A	True	A7	A7	A7	A5	A5	A5	E7	E7	E7	E7	E7	E7	B8	B8	B8	A6	A6	A6	D9	D9	D9
IOT15A	I/O	0	DQ8		True_of_IOT15B	none	C6	C6	C6	G8	G8	G8													F10	F10	F10
IOT15B	I/O	0	DQ8		Comp_of_IOT15A	none	D7	D7	D7	F8	F8	F8													G10	G10	G10
IOT16A	I/O	0	DQ8		True_of_IOT16B	True	C8	C8	C8	B6	B6	B6							D8	D8	D8	D8	D8	D8	B7	B7	B7
IOT16B	I/O	0	DQ8		Comp_of_IOT16A	True	D8	D8	D8	A6	A6	A6							E9	E9	E9	E7	E7	E7	A7	A7	A7
IOT17A/TDO	I/O	0	DQ8	TDO	True_of_IOT17B	none	E8	E8	E8	E8	E8	E8	C6	C6	C6	C6	C6	C6	C7	C7	C7	D7	D7	D7	A6	A6	A6
IOT17B/TDI	I/O	0	DQ8	TDI	Comp_of_IOT17A	none	E9	E9	E9	C7	C7	C7	A6	A6	A6	A6	A6	A6	B7	B7	B7	C6	C6	C6	C7	C7	C7
IOT18A	I/O	0	DQ8		True_of_IOT18B	True	B8	B8	B8	B7	B7	B7	B7	B7	B7	B7	B7	B7	B6	B6	B6	A7	A7	A7	E8	E8	E8
IOT18B	I/O	0	DQ8		Comp_of_IOT18A	True	A8	A8	A8	A7	A7	A7	C7	C7	C7	C7	C7	C7	A6	A6	A6	B7	B7	B7	D8	D8	D8
IOT19A	I/O	0	DQ8		True_of_IOT19B	none	C9	C9	C9	G9	G9	G9							E8	E8	E8	E8	E8	E8	B10	B10	B10
IOT19B	I/O	0	DQ8		Comp_of_IOT19A	none	D9	D9	D9	F9	F9	F9							C8	C8	C8	F8	F8	F8	A10	A10	A10
IOT20A	I/O	0	DQ8		True_of_IOT20B	True	B9	B9	B9	B8	B8	B8	E6	E6	E6	E6	E6	E6	D9	D9	D9	B8	B8	B8	E10	E10	E10
IOT20B	I/O	0	DQ8		Comp_of_IOT20A	True	A9	A9	A9	A8	A8	A8	D7	D7	D7	D7	D7	D7	E10	E10	E10	A8	A8	A8	C11	C11	C11
IOT21A	I/O	0	DQS8		True_of_IOT21B	none	F9	F9	F9	D8	D8	D8							D10	D10	D10	C9	C9	C9			
IOT21B	I/O	0	DQS8		Comp_of_IOT21A	none	G9	G9	G9	C8	C8	C8							D11	D11	D11	D9	D9	D9			
IOT22A	I/O	0	DQ8		True_of_IOT22B	True	F10	F10	F10	B9	B9	B9	F7	F7	F7	F7	F7	F7							E11	E11	E11
IOT22B	I/O	0	DQ8		Comp_of_IOT22A	True	E10	E10	E10	A9	A9	A9	E8	E8	E8	E8	E8	E8							D11	D11	D11
IOT23A/TCK	I/O	0	DQ8	TCK	True_of_IOT23B	none	D10	D10	D10	C9	C9	C9	A7	A7	A7	A7	A7	A7	A8	A8	A8	C7	C7	C7	A8	A8	A8
IOT23B/TMS	I/O	0	DQ8	TMS	Comp_of_IOT23A	none	C10	C10	C10	D9	D9	D9	B8	B8	B8	B8	B8	B8	C9	C9	C9	C8	C8	C8	C9	C9	C9
IOT24A/GCLKT_0	I/O	0	DQ8	GCLKT_0	True_of_IOT24B	True	B10	B10	B10	B10	B10	B10	C8	C8	C8	C8	C8	C8	B9	B9	B9	A9	A9	A9	B9	B9	B9
IOT24B/GCLKC_0	I/O	0	DQ8	GCLKC_0	Comp_of_IOT24A	True	A10	A10	A10	A10	A10	A10	A8	A8	A8	A8	A8	A8	A9	A9	A9	B9	B9	B9	C10	C10	C10
IOT25A	I/O	0	DQ8		True_of_IOT25B	none	G11	G11	G11	G10	G10	G10													C8	C8	C8
IOT25B	I/O	0	DQ8		Comp_of_IOT25A	none	F11	F11	F11	F10	F10	F10													B8	B8	B8
IOT26A	I/O	0	DQ8		True_of_IOT26B	True	B11	B11	B11	B11	B11	B11	D8	D8	D8	D8	D8	D8	C10	C10	C10	A10	A10	A10	B11	B11	B11
IOT26B	I/O	0	DQ8		Comp_of_IOT26A	True	A11	A11	A11	A11	A11	A11	E9	E9	E9	E9	E9	E9	B10	B10	B10	B10	B10	B10	A11	A11	A11
IOT27A	I/O	0	DQ8		True_of_IOT27B	none	E11	E11	E11	D10	D10	D10													C12	C12	C12
IOT27B	I/O	0	DQ8		Comp_of_IOT27A	none	D11	D11	D11	C10	C10	C10													E13	E13	E13
IOT2A	I/O	0	DQ9		True_of_IOT2B	True	B1	B1	B1	B1	B1	B1	C4	C4	C4	C4	C4	C4	C4	C4	C4	A2	A2	A2	D4	D4	D4
IOT2B	I/O	0	DQ9		Comp_of_IOT2A	True	A2	A2	A2	A1	A1	A1	B5	B5	B5	B5	B5	B5	B4	B4	B4	B3	B3	B3	B3	B3	B3
IOT30A	I/O	1	DQ7		True_of_IOT30B	True	D12	D12	D12	A12	A12	A12							A11	A11	A11	C10	C10	C10	D12	D12	D12
IOT30B	I/O	1	DQ7		Comp_of_IOT30A	True	E12	E12	E12	B12	B12	B12							B11	B11	B11	B11	B11	B11	E12	E12	E12
IOT31A/SCL/GCLKT_1	I/O	1	DQ7	SCL/GCLKT_1	True_of_IOT31B	none	B12	B12	B12	C11	C11	C11	A9	A9	A9	A9	A9	A9	C11	C11	C11	E9	E9	E9	A13	A13	A13
IOT31B/SDA/GCLKC_1	I/O	1	DQ7	SDA/GCLKC_1	Comp_of_IOT31A	none	A12	A12	A12	D11	D11	D11	C9	C9	C9	C9	C9	C9	A12	A12	A12	D10	D10	D10	B13	B13	B13
IOT32A	I/O	1	DQ7		True_of_IOT32B	True	G12	G12	G12	A13	A13	A13							B12	B12	B12	B12	B12	B12	A12	A12	A12
IOT32B	I/O	1	DQ7		Comp_of_IOT32A	True	F12	F12	F12	B13	B13	B13							C12	C12	C12	C11	C11	C11	B12	B12	B12
IOT33A	I/O	1	DQ7		True_of_IOT33B	none	E13	E13	E13																C14	C14	C14
IOT33B	I/O	1	DQ7		Comp_of_IOT33A	none	F13	F13	F13																A15	A15	A15
IOT34A	I/O	1	DQ7		True_of_IOT34B	True	A13	A13	A13	G11	G11	G11	F8	F8	F8	F8	F8	F8	D12	D12	D12	A11	A11	A11	C13	C13	C13
IOT34B	I/O	1	DQ7		Comp_of_IOT34A	True	B13	B13	B13	F11	F11	F11	D9	D9	D9	D9	D9	D9	D13	D13	D13	A12	A12	A12	B14	B14	B14
IOT35A	I/O	1	DQ7		True_of_IOT35B	none	C13	C13	C13																G12	G12	G12
IOT35B	I/O	1	DQ7		Comp_of_IOT35A	none	D13	D13	D13																F12	F12	F12
IOT36A	I/O	1	DQ7		True_of_IOT36B	True	A14	A14	A14	D12	D12	D12	B9	B9	B9	B9	B9	B9	E12	E12	E12	F9	F9	F9	F11	F11	F11
IOT36B	I/O	1	DQ7		Comp_of_IOT36A	True	B14	B14	B14	C12	C12	C12	A10	A10	A10	A10	A10	A10	D14	D14	D14	F10	F10	F10	G11	G11	G11
IOT37A	I/O	1	DQS7		True_of_IOT37B	none	C14	C14	C14																G14	G14	G14
IOT37B	I/O	1	DQS7		Comp_of_IOT37A	none	D14	D14	D14																F14	F14	F14
IOT38A	I/O	1	DQ7		True_of_IOT38B	True	G14	G14	G14	A14	A14	A14	F9	F9	F9	F9	F9	F9	B14	B14	B14	C12	C12	C12	B15	B15	B15
IOT38B	I/O	1	DQ7		Comp_of_IOT38A	True	F14	F14	F14	B14	B14	B14	E11	E11	E11	E11	E11	E11	C14	C14	C14	B13	B13	B13	C15	C15	C15
IOT39A/JTAGSEL_N	I/O	1	DQ7	JTAGSEL_N	True_of_IOT39B	none	E14	E14	E14	C13	C13	C13	C10	C10	C10	C10	C10	C10	C13	C13	C13	D11	D11	D11	A16	A16	A16
IOT39B/RECONFIG_N	I/O	1	DQ7	RECONFIG_N	Comp_of_IOT39A	none	E15	E15	E15	D13	D13	D13	B10	B10	B10	B10	B10	B10	A14	A14	A14	D12	D12	D12	B16	B16	B16

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[1] UV Version; The unpackaged MODE[1:0] is internally connected to 01.
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[4] "Tie to VSS by 10K Resisitor" indicates the pin is connected to the ground with 10K resistance.

Pin Name	Function	BANK	DQS	Configuration Function	Differential Pair	LVDS	UG484[1]	UG484[2]	UG484[3]	UG400[1]	UG400[2]	UG400[3]	UG256[1]	UG256[2]	UG256[3]	PG256[1]	PG256[2]	PG256[3]	UG332[1]	UG332[2]	UG332[3]	UG324[1]	UG324[2]	UG324[3]	PG484[1]	PG484[2]	PG484[3]
IOT3A	I/O	0	DQ9		True_of_IOT3B	none	E6	E6	E6										A3	A3	A3	D4	D4	D4	G7	G7	G7
IOT3B	I/O	0	DQ9		Comp_of_IOT3A	none	F7	F7	F7										B3	B3	B3	E5	E5	E5	E6	E6	E6
IOT40A	I/O	1	DQ7		True_of_IOT40B	True	A15	A15	A15	A15	A15	A15	D10	D10	D10	D10	D10	D10	A13	A13	A13	A13	A13	A13	G13	G13	G13
IOT40B	I/O	1	DQ7		Comp_of_IOT40A	True	B15	B15	B15	B15	B15	B15	E10	E10	E10	E10	E10	E10	B13	B13	B13	A14	A14	A14	F13	F13	F13
IOT41A	I/O	1	DQ7		True_of_IOT41B	none	C15	C15	C15										E13	E13	E13	E10	E10	E10	D14	D14	D14
IOT41B	I/O	1	DQ7		Comp_of_IOT41A	none	D15	D15	D15										D15	D15	D15	E11	E11	E11	E14	E14	E14
IOT42A	I/O	1	DQ7		True_of_IOT42B	True	A16	A16	A16	A16	A16	A16	A11	A11	A11	A11	A11	A11	E14	E14	E14	B14	B14	B14	C16	C16	C16
IOT42B	I/O	1	DQ7		Comp_of_IOT42A	True	B17	B17	B17	B16	B16	B16	C11	C11	C11	C11	C11	C11	E15	E15	E15	B15	B15	B15	A17	A17	A17
IOT43A	I/O	1	DQ7		True_of_IOT43B	none	C17	C17	C17	G12	G12	G12													C17	C17	C17
IOT43B	I/O	1	DQ7		Comp_of_IOT43A	none	D16	D16	D16	F12	F12	F12													A18	A18	A18
IOT44A	I/O	1	DQ7		True_of_IOT44B	True	A17	A17	A17	A17	A17	A17	F10	F10	F10	F10	F10	F10	A15	A15	A15	F11	F11	F11	D15	D15	D15
IOT44B	I/O	1	DQ7		Comp_of_IOT44A	True	B18	B18	B18	B17	B17	B17	D11	D11	D11	D11	D11	D11	B15	B15	B15	C13	C13	C13	E15	E15	E15
IOT45A	I/O	1	DQ7		True_of_IOT45B	none	E16	E16	E16	C14	C14	C14													B18	B18	B18
IOT45B	I/O	1	DQ7		Comp_of_IOT45A	none	D17	D17	D17	D14	D14	D14													A19	A19	A19
IOT48A	I/O	1	DQS6		True_of_IOT48B	True	A18	A18	A18	C15	C15	C15	B11	B11	B11	B11	B11	B11	D17	D17	D17	C14	C14	C14	C18	C18	C18
IOT48B	I/O	1	DQS6		Comp_of_IOT48A	True	B19	B19	B19	C16	C16	C16	A12	A12	A12	A12	A12	A12	D16	D16	D16	C15	C15	C15	B19	B19	B19
IOT49A	I/O	1	DQ6		True_of_IOT49B	none	C18	C18	C18	G13	G13	G13							C15	C15	C15	E12	E12	E12	D16	D16	D16
IOT49B	I/O	1	DQ6		Comp_of_IOT49A	none	D18	D18	D18	F13	F13	F13							A16	A16	A16	F12	F12	F12	D17	D17	D17
IOT4A	I/O	0	DQ9		True_of_IOT4B	True	B2	B2	B2	G7	G7	G7	B3	B3	B3	B3	B3	B3	A4	A4	A4	C3	C3	C3	D5	D5	D5
IOT4B	I/O	0	DQ9		Comp_of_IOT4A	True	A3	A3	A3	F7	F7	F7	A2	A2	A2	A2	A2	A2	C5	C5	C5	C4	C4	C4	C4	C4	C4
IOT50A	I/O	1	DQ6		True_of_IOT50B	True	A19	A19	A19	A18	A18	A18	B13	B13	B13	B13	B13	B13	A19	A19	A19	A15	A15	A15	E16	E16	E16
IOT50B	I/O	1	DQ6		Comp_of_IOT50A	True	B20	B20	B20	B18	B18	B18	A14	A14	A14	A14	A14	A14	B18	B18	B18	A16	A16	A16	F15	F15	F15
IOT51A	I/O	1	DQ6		True_of_IOT51B	none	F15	F15	F15	E14	E14	E14													A20	A20	A20
IOT51B	I/O	1	DQ6		Comp_of_IOT51A	none	G15	G15	G15	D15	D15	D15													A21	A21	A21
IOT52A	I/O	1	DQ6		True_of_IOT52B	True	A20	A20	A20	E15	E15	E15	C12	C12	C12	C12	C12	C12	B16	B16	B16	B16	B16	B16	C19	C19	C19
IOT52B	I/O	1	DQ6		Comp_of_IOT52A	True	B21	B21	B21	D16	D16	D16	B12	B12	B12	B12	B12	B12	C16	C16	C16	A17	A17	A17	D18	D18	D18
IOT53A	I/O	1	DQ6		True_of_IOT53B	none	C19	C19	C19	G14	G14	G14										D13	D13	D13	G15	G15	G15
IOT53B	I/O	1	DQ6		Comp_of_IOT53A	none	C20	C20	C20	F14	F14	F14										E13	E13	E13	F16	F16	F16
IOT54A	I/O	1	DQ6		True_of_IOT54B	True	A21	A21	A21	B19	B19	B19	B14	B14	B14	B14	B14	B14	A18	A18	A18	D14	D14	D14	E17	E17	E17
IOT54B	I/O	1	DQ6		Comp_of_IOT54A	True	B22	B22	B22	A20	A20	A20	A15	A15	A15	A15	A15	A15	C17	C17	C17	D15	D15	D15	F17	F17	F17
IOT55A/READY	I/O	1	DQ6	READY	True_of_IOT55B	none	F16	F16	F16	C17	C17	C17	A13	A13	A13	A13	A13	A13	A17	A17	A17	C16	C16	C16	B20	B20	B20
IOT55B/DONE	I/O	1	DQ6	DONE	Comp_of_IOT55A	none	E17	E17	E17	A19	A19	A19	C13	C13	C13	C13	C13	C13	B17	B17	B17	E14	E14	E14	C20	C20	C20
IOT5A	I/O	0	DQ9		True_of_IOT5B	none	C3	C3	C3	E6	E6	E6							A2	A2	A2	F7	F7	F7	F7	F7	F7
IOT5B	I/O	0	DQ9		Comp_of_IOT5A	none	C4	C4	C4	D5	D5	D5							B2	B2	B2	E6	E6	E6	G8	G8	G8
IOT6A	I/O	0	DQ9		True_of_IOT6B	True	B3	B3	B3	B2	B2	B2	A4	A4	A4	A4	A4	A4	B5	B5	B5	D5	D5	D5	A2	A2	A2
IOT6B	I/O	0	DQ9		Comp_of_IOT6A	True	A4	A4	A4	A2	A2	A2	C5	C5	C5	C5	C5	C5	A5	A5	A5	B5	B5	B5	A3	A3	A3
IOT7A	I/O	0	DQ9		True_of_IOT7B	none	F8	F8	F8																A4	A4	A4
IOT7B	I/O	0	DQ9		Comp_of_IOT7A	none	G8	G8	G8																B5	B5	B5
IOT8A	I/O	0	DQ9		True_of_IOT8B	True	B4	B4	B4	B3	B3	B3	A5	A5	A5	A5	A5	A5	E7	E7	E7	A3	A3	A3	D6	D6	D6
IOT8B	I/O	0	DQ9		Comp_of_IOT8A	True	A5	A5	A5	A3	A3	A3	B6	B6	B6	B6	B6	B6	D6	D6	D6	B4	B4	B4	D7	D7	D7
IOT9A	I/O	0	DQS9		True_of_IOT9B	none	D5	D5	D5	D6	D6	D6							E6	E6	E6	C5	C5	C5	F8	F8	F8
IOT9B	I/O	0	DQS9		Comp_of_IOT9A	none	C5	C5	C5	E7	E7	E7							D5	D5	D5	D6	D6	D6	E7	E7	E7
VCC	Power	N/A						K10	K10		L9	L9		T16	T16		T16	T16		M11	M11		L10	L10		N13	N13
VCC	Power	N/A						K11	K11		J9	J9		G7	G7		G7	G7		K12	K12		H10	H10		M13	M13
VCC	Power	N/A						K12	K12		H12	H12		A16	A16		A16	A16		J11	J11		H8	H8		K13	K13
VCC	Power	N/A						K13	K13		L12	L12		K10	K10		K10	K10		L9	L9		L11	L11		K11	K11
VCC	Power	N/A						L11	L11		J10	J10		K7	K7		K7	K7		L12	L12		H11	H11		N10	N10
VCC	Power	N/A						L12	L12		M10	M10		T1	T1		T1	T1		M10	M10		M12	M12		L10	L10
VCC	Power	N/A						M11	M11		J11	J11		G10	G10		G10	G10		K9	K9		L8	L8		N11	N11
VCC	Power	N/A						M12	M12		M12	M12		A1	A1		A1	A1		J10	J10		L9	L9		L13	L13
VCC	Power	N/A						N10	N10		K12	K12											H9	H9		N12	N12
VCC	Power	N/A						N11	N11		H13	H13											G12	G12		M10	M10
VCC	Power	N/A						N12	N12																	K12	K12
VCC	Power	N/A						N13	N13																	K10	K10
VCC/VCCX	Power	N/A					K10			L9			T16			T16			M11			L10			N13		
VCC/VCCX	Power	N/A					K11			J9			G7			G7			K12			H10			M13		
VCC/VCCX	Power	N/A					K12			H12			A16			A16			J11			H8			K13		
VCC/VCCX	Power	N/A					K13			L12			K10			K10			L9			L11			K11		
VCC/VCCX	Power	N/A					L11			J10			K7			K7			L12			H11			N10		
VCC/VCCX	Power	N/A					L12			M10			T1			T1			M10			M12			L10		
VCC/VCCX	Power	N/A					M11			J11			G10			G10			K9			L8			N11		
VCC/VCCX	Power	N/A					M12			M12			A1			A1			J10			L9			L13		
VCC/VCCX	Power	N/A					N10			K12												H9			N12		
VCC/VCCX	Power	N/A					N11			H13												G12			M10		
VCC/VCCX	Power	N/A					N12																		K12		
VCC/VCCX	Power	N/A					N13																		K10		
VCCIO0	Power	N/A					C7			H8			G8			G8			H9			G8			F9		
VCCIO0	Power	N/A					G10			H10			D5			D5			H10			G9			B6		
VCCIO0	Power	N/A					H11			H9															D10		
VCCIO0	Power	N/A					H9																		H10		
VCCIO0	Power	N/A																							H9		
VCCIO0	Power	N/A																							H11		

Note!
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[3] EV Version; The unpackaged MODE[1:0] is internally connected to 01.
[4] "Tie to VSS by 10K Resisitor" indicates the pin is connected to the ground with 10K resistance.

Pin Name	Function	BANK	DQS	Configuration Function	Differential Pair	LVDS	UG484[1]	UG484[2]	UG484[3]	UG400[1]	UG400[2]	UG400[3]	UG256[1]	UG256[2]	UG256[3]	PG256[1]	PG256[2]	PG256[3]	UG332[1]	UG332[2]	UG332[3]	UG324[1]	UG324[2]	UG324[3]	PG484[1]	PG484[2]	PG484[3]
VCCIO0/VCCX	Power	N/A						C7	C7		H8	H8		G8	G8		G8	G8		H9	H9		G8	G8		F9	F9
VCCIO0/VCCX	Power	N/A						G10	G10		H10	H10		D5	D5		D5	D5		H10	H10		G9	G9		B6	B6
VCCIO0/VCCX	Power	N/A						H11	H11		H9	H9														D10	D10
VCCIO0/VCCX	Power	N/A						H9	H9																	H10	H10
VCCIO0/VCCX	Power	N/A																								H9	H9
VCCIO0/VCCX	Power	N/A																								H11	H11
VCCIO1	Power	N/A					C12	C12	C12	H11	H11	H11	D12	D12	D12	D12	D12	D12	H11	H11	H11	G10	G10	G10	B17	B17	B17
VCCIO1	Power	N/A					C16	C16	C16	J12	J12	J12	G9	G9	G9	G9	G9	G9	H12	H12	H12	G11	G11	G11	H14	H14	H14
VCCIO1	Power	N/A					G13	G13	G13																H12	H12	H12
VCCIO1	Power	N/A					H12	H12	H12																D13	D13	D13
VCCIO1	Power	N/A					H14	H14	H14																H13	H13	H13
VCCIO2	Power	N/A					F20	F20	F20	J13	J13	J13	E13	E13	E13	E13	E13	E13	J13	J13	J13	H12	H12	H12	J15	J15	J15
VCCIO2	Power	N/A					J15	J15	J15	K13	K13	K13	H10	H10	H10	H10	H10	H10	K13	K13	K13	J11	J11	J11	K15	K15	K15
VCCIO2	Power	N/A					K15	K15	K15																L15	L15	L15
VCCIO2	Power	N/A					L15	L15	L15																F21	F21	F21
VCCIO2	Power	N/A																							K19	K19	K19
VCCIO3	Power	N/A					M15	M15	M15	L13	L13	L13	M13	M13	M13	M13	M13	M13	L13	L13	L13	K11	K11	K11	M15	M15	M15
VCCIO3	Power	N/A					M18	M18	M18	M13	M13	M13	J10	J10	J10	J10	J10	J10	M13	M13	M13	L12	L12	L12	P15	P15	P15
VCCIO3	Power	N/A					N15	N15	N15	N13	N13	N13													N15	N15	N15
VCCIO3	Power	N/A					P15	P15	P15																N19	N19	N19
VCCIO3	Power	N/A					V20	V20	V20																U21	U21	U21
VCCIO4	Power	N/A					R12	R12	R12	N11	N11	N11	N12	N12	N12	N12	N12	N12	N12	N12	N12	M11	M11	M11	R14	R14	R14
VCCIO4	Power	N/A					R13	R13	R13	N12	N12	N12	K9	K9	K9	K9	K9	K9	N11	N11	N11	M10	M10	M10	R13	R13	R13
VCCIO4	Power	N/A					R14	R14	R14																R12	R12	R12
VCCIO4	Power	N/A					W16	W16	W16																AA17	AA17	AA17
VCCIO4	Power	N/A																							W13	W13	W13
VCCIO5	Power	N/A					R10	R10	R10	N9	N9	N9	N5	N5	N5	N5	N5	N5	N9	N9	N9	M8	M8	M8	R11	R11	R11
VCCIO5	Power	N/A					R11	R11	R11	N10	N10	N10	K8	K8	K8	K8	K8	K8	N10	N10	N10	M9	M9	M9	AA6	AA6	AA6
VCCIO5	Power	N/A					R9	R9	R9	N8	N8	N8													R9	R9	R9
VCCIO5	Power	N/A					W11	W11	W11																R10	R10	R10
VCCIO5	Power	N/A					W7	W7	W7																W10	W10	W10
VCCIO6	Power	N/A					N8	N8	N8	M8	M8	M8	M4	M4	M4	M4	M4	M4	L8	L8	L8	L7	L7	L7	N8	N8	N8
VCCIO6	Power	N/A					P8	P8	P8	M9	M9	M9							M8	M8	M8	M7	M7	M7	P8	P8	P8
VCCIO6	Power	N/A					V3	V3	V3																U2	U2	U2
VCCIO7	Power	N/A					L8	L8	L8	K8	K8	K8	H7	H7	H7	H7	H7	H7	K5	K5	K5	J8	J8	J8	K4	K4	K4
VCCIO7	Power	N/A					M3	M3	M3	K9	K9	K9	J7	J7	J7	J7	J7	J7				K8	K8	K8	M8	M8	M8
VCCIO7	Power	N/A					M8	M8	M8																L8	L8	L8
VCCIO7	Power	N/A																							N4	N4	N4
VCCIO8	Power	N/A					F3	F3	F3	J7	J7	J7	E4	E4	E4	E4	E4	E4	J8	J8	J8	G7	G7	G7	K8	K8	K8
VCCIO8	Power	N/A					J8	J8	J8	J8	J8	J8							K8	K8	K8	H7	H7	H7	F2	F2	F2
VCCIO8	Power	N/A					K8	K8	K8																J8	J8	J8
VSS	Ground	N/A					A1	A1	A1																		
VSS	Ground	N/A					A22	A22	A22	C5	C5	C5	M12	M12	M12	M12	M12	M12	A1	A1	A1	A1	A1	A1	A1	A1	A1
VSS	Ground	N/A					AB1	AB1	AB1																		
VSS	Ground	N/A					AB22	AB22	AB22	D3	D3	D3	M5	M5	M5	M5	M5	M5	A10	A10	A10	A18	A18	A18	A14	A14	A14
VSS	Ground	N/A					B16	B16	B16	E13	E13	E13	B2	B2	B2	B2	B2	B2	J9	J9	J9	K9	K9	K9	AB22	AB22	AB22
VSS	Ground	N/A					B7	B7	B7																P22	P22	P22
VSS	Ground	N/A					C11	C11	C11	U8	U8	U8							Y20	Y20	Y20				L11	L11	L11
VSS	Ground	N/A					C2	C2	C2																V18	V18	V18
VSS	Ground	N/A					E18	E18	E18	E11	E11	E11	R15	R15	R15	R15	R15	R15	H8	H8	H8	J9	J9	J9	AB1	AB1	AB1
VSS	Ground	N/A					E5	E5	E5																R15	R15	R15
VSS	Ground	N/A					F2	F2	F2																V5	V5	V5
VSS	Ground	N/A					F21	F21	F21	D4	D4	D4	N13	N13	N13	N13	N13	N13	A20	A20	A20	B2	B2	B2	A22	A22	A22
VSS	Ground	N/A					H10	H10	H10	V5	V5	V5													L9	L9	L9
VSS	Ground	N/A					H13	H13	H13	K11	K11	K11	H8	H8	H8	H8	H8	H8	M12	M12	M12				J11	J11	J11
VSS	Ground	N/A					H15	H15	H15	E18	E18	E18	C3	C3	C3	C3	C3	C3	K10	K10	K10	N6	N6	N6	B2	B2	B2
VSS	Ground	N/A					H8	H8	H8																P13	P13	P13
VSS	Ground	N/A					J10	J10	J10	V7	V7	V7													M11	M11	M11
VSS	Ground	N/A					J11	J11	J11	U13	U13	U13													L12	L12	L12
VSS	Ground	N/A					J12	J12	J12	T15	T15	T15	L11	L11	L11	L11	L11	L11	V18	V18	V18				J9	J9	J9
VSS	Ground	N/A					J13	J13	J13	L18	L18	L18	H9	H9	H9	H9	H9	H9	N8	N8	N8				J12	J12	J12
VSS	Ground	N/A					J14	J14	J14	H5	H5	H5	D4	D4	D4	D4	D4	D4	K20	K20	K20	U2	U2	U2	E18	E18	E18
VSS	Ground	N/A					J9	J9	J9																N14	N14	N14
VSS	Ground	N/A					K14	K14	K14	K3	K3	K3	D13	D13	D13	D13	D13	D13	L5	L5	L5	U17	U17	U17	E5	E5	E5
VSS	Ground	N/A					K21	K21	K21	E5	E5	E5	N4	N4	N4	N4	N4	N4	C3	C3	C3	B17	B17	B17	A9	A9	A9
VSS	Ground	N/A					K9	K9	K9																N9	N9	N9
VSS	Ground	N/A					L10	L10	L10	V11	V11	V11													M12	M12	M12
VSS	Ground	N/A					L13	L13	L13	M11	M11	M11	J8	J8	J8	J8	J8	J8	N13	N13	N13				J13	J13	J13
VSS	Ground	N/A					L14	L14	L14	K10	K10	K10	E5	E5	E5	E5	E5	E5	L10	L10	L10	V1	V1	V1	H15	H15	H15
VSS	Ground	N/A					L18	L18	L18	E12	E12	E12	R2	R2	R2	R2	R2	R2	H13	H13	H13	J10	J10	J10	AB14	AB14	AB14
VSS	Ground	N/A					L2	L2	L2																		
VSS	Ground	N/A					L9	L9	L9																P1	P1	P1

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Pin Name	Function	BANK	DQS	Configuration Function	Differential Pair	LVDS	UG484[1]	UG484[2]	UG484[3]	UG400[1]	UG400[2]	UG400[3]	UG256[1]	UG256[2]	UG256[3]	PG256[1]	PG256[2]	PG256[3]	UG332[1]	UG332[2]	UG332[3]	UG324[1]	UG324[2]	UG324[3]	PG484[1]	PG484[2]	PG484[3]
VSS	Ground	N/A					M10	M10	M10	V18	V18	V18													M14	M14	M14
VSS	Ground	N/A					M13	M13	M13	N7	N7	N7	J9	J9	J9	J9	J9	J9	T10	T10	T10				J14	J14	J14
VSS	Ground	N/A					M14	M14	M14	L8	L8	L8	E12	E12	E12	E12	E12	E12	L11	L11	L11	V18	V18	V18	H8	H8	H8
VSS	Ground	N/A					M4	M4	M4																R8	R8	R8
VSS	Ground	N/A					M9	M9	M9																P10	P10	P10
VSS	Ground	N/A					N14	N14	N14	L10	L10	L10	F6	F6	F6	F6	F6	F6	L16	L16	L16				J1	J1	J1
VSS	Ground	N/A					N21	N21	N21	E9	E9	E9	P14	P14	P14	P14	P14	P14	C18	C18	C18	F6	F6	F6	AA2	AA2	AA2
VSS	Ground	N/A					N9	N9	N9																P11	P11	P11
VSS	Ground	N/A					P10	P10	P10																M9	M9	M9
VSS	Ground	N/A					P11	P11	P11	U16	U16	U16													L14	L14	L14
VSS	Ground	N/A					P12	P12	P12	U3	U3	U3							Y1	Y1	Y1				K14	K14	K14
VSS	Ground	N/A					P13	P13	P13	R18	R18	R18	L6	L6	L6	L6	L6	L6	V3	V3	V3				J22	J22	J22
VSS	Ground	N/A					P14	P14	P14	L11	L11	L11	F11	F11	F11	F11	F11	F11	M9	M9	M9				J10	J10	J10
VSS	Ground	N/A					P9	P9	P9																P12	P12	P12
VSS	Ground	N/A					R15	R15	R15	G18	G18	G18	C14	C14	C14	C14	C14	C14	K11	K11	K11	N13	N13	N13	B21	B21	B21
VSS	Ground	N/A					R8	R8	R8																P14	P14	P14
VSS	Ground	N/A					V2	V2	V2																G9	G9	G9
VSS	Ground	N/A					V21	V21	V21	E10	E10	E10	P3	P3	P3	P3	P3	P3	E11	E11	E11	F13	F13	F13	AA21	AA21	AA21
VSS	Ground	N/A					W12	W12	W12	U7	U7	U7							Y11	Y11	Y11				K9	K9	K9
VSS	Ground	N/A					Y16	Y16	Y16	E16	E16	E16	B15	B15	B15	B15	B15	B15	J12	J12	J12	K10	K10	K10	AB9	AB9	AB9
VSS	Ground	N/A					Y7	Y7	Y7																P9	P9	P9

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Note!
[1] UV version.
[2] LV version.
[3] EV version.

Pin Name	Function	BANK	DQS	Configuration Function	Differential Pair	LVDS	UG484[1]	UG484[2]	UG484[3]	UG400[1]	UG400[2]	UG400[3]	UG256[1]	UG256[2]	UG256[3]	PG256[1]	PG256[2]	PG256[3]	UG332[1]	UG332[2]	UG332[3]	UG324[1]	UG324[2]	UG324[3]	PG484[1]	PG484[2]	PG484[3]
BANK8 True LVDS Pair																											
IOL11A	I/O	8	none		True_of_IOL11B	True	E1	E1	E1	H6	H6	H6							F2	F2	F2	E2	E2	E2	F4	F4	F4
IOL11B	I/O	8	none		Comp_of_IOL11A	True	F1	F1	F1	H7	H7	H7							F1	F1	F1	E1	E1	E1	G4	G4	G4
IOL13A	I/O	8	none		True_of_IOL13B	True	H4	H4	H4	F2	F2	F2							F5	F5	F5	F2	F2	F2	H5	H5	H5
IOL13B	I/O	8	none		Comp_of_IOL13A	True	H3	H3	H3	F1	F1	F1							G5	G5	G5	H5	H5	H5	H4	H4	H4
IOL15A	I/O	8	none		True_of_IOL15B	True	H2	H2	H2	G4	G4	G4	F4	F4	F4	F4	F4	F4				F1	F1	F1	D2	D2	D2
IOL15B	I/O	8	none		Comp_of_IOL15A	True	H1	H1	H1	G3	G3	G3	G6	G6	G6	G6	G6	G6				G6	G6	G6	E3	E3	E3
IOL17A	I/O	8	none		True_of_IOL17B	True	H5	H5	H5	G2	G2	G2	G5	G5	G5	G5	G5	G5	H2	H2	H2	G2	G2	G2	G2	G2	G2
IOL17B	I/O	8	none		Comp_of_IOL17A	True	J5	J5	J5	G1	G1	G1	G4	G4	G4	G4	G4	G4	H1	H1	H1	G1	G1	G1	G1	G1	G1
IOL19A	I/O	8	none		True_of_IOL19B	True	J2	J2	J2	H2	H2	H2	G2	G2	G2	G2	G2	G2	J3	J3	J3	H2	H2	H2	H3	H3	H3
IOL19B	I/O	8	none		Comp_of_IOL19A	True	J1	J1	J1	H1	H1	H1	G3	G3	G3	G3	G3	G3	J2	J2	J2	H1	H1	H1	H2	H2	H2
IOL2A	I/O	8	DQ0		True_of_IOL2B	True	D3	D3	D3	C4	C4	C4	B1	B1	B1	B1	B1	B1	D2	D2	D2	B1	B1	B1	C3	C3	C3
IOL2B	I/O	8	DQ0		Comp_of_IOL2A	True	D4	D4	D4	C3	C3	C3	C2	C2	C2	C2	C2	C2	D1	D1	D1	C2	C2	C2	C2	C2	C2
IOL4A/LPLL1_T_fb	I/O	8	DQ0	LPLL1_T_fb	True_of_IOL4B	True	E4	E4	E4	C2	C2	C2	D3	D3	D3	D3	D3	D3	E3	E3	E3	E4	E4	E4	E4	E4	E4
IOL4B/LPLL1_C_fb	I/O	8	DQ0	LPLL1_C_fb	Comp_of_IOL4A	True	F5	F5	F5	C1	C1	C1	D1	D1	D1	D1	D1	D1	E2	E2	E2	F4	F4	F4	D3	D3	D3
IOL6A	I/O	8	DQS0		True_of_IOL6B	True	G6	G6	G6	E4	E4	E4										D3	D3	D3	G6	G6	G6
IOL6B	I/O	8	DQS0		Comp_of_IOL6A	True	H7	H7	H7	E3	E3	E3										C1	C1	C1	H7	H7	H7
IOL8A	I/O	8	DQ0		True_of_IOL8B	True	D1	D1	D1				C1	C1	C1	C1	C1	C1	G1	G1	G1	E3	E3	E3	J6	J6	J6
IOL8B	I/O	8	DQ0		Comp_of_IOL8A	True	E2	E2	E2				D2	D2	D2	D2	D2	D2	H3	H3	H3	F5	F5	F5	J7	J7	J7
BANK7 True LVDS Pair																											
IOL21A	I/O	7	none		True_of_IOL21B	True	L7	L7	L7	J2	J2	J2	G1	G1	G1	G1	G1	G1	J1	J1	J1	J2	J2	J2	H1	H1	H1
IOL21B	I/O	7	none		Comp_of_IOL21A	True	K5	K5	K5	J1	J1	J1	H2	H2	H2	H2	H2	H2	K3	K3	K3	J5	J5	J5	J3	J3	J3
IOL23A	I/O	7	none		True_of_IOL23B	True	K2	K2	K2	K2	K2	K2													J2	J2	J2
IOL23B	I/O	7	none		Comp_of_IOL23A	True	K1	K1	K1	K1	K1	K1													K3	K3	K3
IOL25A/GCLKT_7	I/O	7	none	GCLKT_7	True_of_IOL25B	True	L1	L1	L1	L1	L1	L1	J1	J1	J1	J1	J1	J1	M1	M1	M1	K2	K2	K2	K2	K2	K2
IOL25B/GCLKC_7	I/O	7	none	GCLKC_7	Comp_of_IOL25A	True	M2	M2	M2	L2	L2	L2	J3	J3	J3	J3	J3	J3	M2	M2	M2	J6	J6	J6	K1	K1	K1
IOL28A	I/O	7	none		True_of_IOL28B	True	M1	M1	M1	M1	M1	M1	J2	J2	J2	J2	J2	J2	M3	M3	M3	K1	K1	K1	N1	N1	N1
IOL28B	I/O	7	none		Comp_of_IOL28A	True	N1	N1	N1	M2	M2	M2	K1	K1	K1	K1	K1	K1	N1	N1	N1	L1	L1	L1	N2	N2	N2
IOL30A	I/O	7	none		True_of_IOL30B	True	N2	N2	N2	L5	L5	L5	H5	H5	H5	H5	H5	H5							N3	N3	N3
IOL30B	I/O	7	none		Comp_of_IOL30A	True	P1	P1	P1	M5	M5	M5	J4	J4	J4	J4	J4	J4							P2	P2	P2
IOL32A	I/O	7	none		True_of_IOL32B	True	P2	P2	P2	N1	N1	N1	K3	K3	K3	K3	K3	K3	N2	N2	N2	K4	K4	K4	P3	P3	P3
IOL32B	I/O	7	none		Comp_of_IOL32A	True	R1	R1	R1	N2	N2	N2	K2	K2	K2	K2	K2	K2	N3	N3	N3	L2	L2	L2	R1	R1	R1
BANK6 True LVDS Pair																											
IOL34A	I/O	6	none		True_of_IOL34B	True	P4	P4	P4	N3	N3	N3							P1	P1	P1	L4	L4	L4	R2	R2	R2
IOL34B	I/O	6	none		Comp_of_IOL34A	True	N5	N5	N5	N4	N4	N4							P2	P2	P2	M2	M2	M2	R3	R3	R3
IOL36A	I/O	6	none		True_of_IOL36B	True	R2	R2	R2	M6	M6	M6	L1	L1	L1	L1	L1	L1	M5	M5	M5				U3	U3	U3
IOL36B	I/O	6	none		Comp_of_IOL36A	True	T1	T1	T1	M7	M7	M7	L3	L3	L3	L3	L3	L3	N4	N4	N4				V1	V1	V1
IOL38A	I/O	6	none		True_of_IOL38B	True	R3	R3	R3	P3	P3	P3							P3	P3	P3	M3	M3	M3	R5	R5	R5
IOL38B	I/O	6	none		Comp_of_IOL38A	True	R4	R4	R4	P4	P4	P4							R1	R1	R1	L5	L5	L5	P5	P5	P5
IOL40A	I/O	6	none		True_of_IOL40B	True	T2	T2	T2	R1	R1	R1	K4	K4	K4	K4	K4	K4	N5	N5	N5	M5	M5	M5	P7	P7	P7
IOL40B	I/O	6	none		Comp_of_IOL40A	True	U1	U1	U1	R2	R2	R2	L5	L5	L5	L5	L5	L5	P4	P4	P4	N3	N3	N3	P6	P6	P6
IOL42A	I/O	6	none		True_of_IOL42B	True	T3	T3	T3	T1	T1	T1							P5	P5	P5				R4	R4	R4
IOL42B	I/O	6	none		Comp_of_IOL42A	True	T4	T4	T4	T2	T2	T2							R4	R4	R4				P4	P4	P4
IOL44A/GCLKT_6	I/O	6	none	GCLKT_6	True_of_IOL44B	True	U2	U2	U2	U1	U1	U1	L2	L2	L2	L2	L2	L2	R2	R2	R2	P1	P1	P1	V3	V3	V3
IOL44B/GCLKC_6	I/O	6	none	GCLKC_6	Comp_of_IOL44A	True	V1	V1	V1	U2	U2	U2	M1	M1	M1	M1	M1	M1	R3	R3	R3	M4	M4	M4	W2	W2	W2
IOL46A	I/O	6	none		True_of_IOL46B	True	W1	W1	W1	T3	T3	T3	K5	K5	K5	K5	K5	K5	R5	R5	R5	N4	N4	N4	T2	T2	T2
IOL46B	I/O	6	none		Comp_of_IOL46A	True	W2	W2	W2	T4	T4	T4	L4	L4	L4	L4	L4	L4	T4	T4	T4	T1	T1	T1	T3	T3	T3
IOL48A	I/O	6	none		True_of_IOL48B	True	Y1	Y1	Y1	V3	V3	V3	M3	M3	M3	M3	M3	M3	T3	T3	T3				R7	R7	R7
IOL48B	I/O	6	none		Comp_of_IOL48A	True	AA1	AA1	AA1	V4	V4	V4	N1	N1	N1	N1	N1	N1	U1	U1	U1				T6	T6	T6
IOL50A	I/O	6	none		True_of_IOL50B	True	Y3	Y3	Y3	T5	T5	T5	M2	M2	M2	M2	M2	M2	U2	U2	U2	P4	P4	P4	Y2	Y2	Y2
IOL50B	I/O	6	none		Comp_of_IOL50A	True	W4	W4	W4	R5	R5	R5	N3	N3	N3	N3	N3	N3	U3	U3	U3	R3	R3	R3	W4	W4	W4
BANK5 True LVDS Pair																											
IOB12A	I/O	5	DQ2		True_of_IOB12B	True	AA6	AA6	AA6	T7	T7	T7	T5	T5	T5	T5	T5	T5	U4	U4	U4	N7	N7	N7	W6	W6	W6
IOB12B	I/O	5	DQ2		Comp_of_IOB12A	True	AB6	AB6	AB6	T8	T8	T8	R6	R6	R6	R6	R6	R6	T7	T7	T7	P7	P7	P7	W7	W7	W7
IOB14A	I/O	5	DQ2		True_of_IOB14B	True	V8	V8	V8	W5	W5	W5	N6	N6	N6	N6	N6	N6	U6	U6	U6	N8	N8	N8	V8	V8	V8
IOB14B	I/O	5	DQ2		Comp_of_IOB14A	True	U8	U8	U8	Y5	Y5	Y5	L7	L7	L7	L7	L7	L7	T8	T8	T8	R7	R7	R7	W8	W8	W8
IOB16A	I/O	5	DQ2		True_of_IOB16B	True	V9	V9	V9	P9	P9	P9	R7	R7	R7	R7	R7	R7	Y7	Y7	Y7	V5	V5	V5	AB8	AB8	AB8
IOB16B	I/O	5	DQ2		Comp_of_IOB16A	True	W8	W8	W8	R9	R9	R9	P7	P7	P7	P7	P7	P7	V8	V8	V8	V6	V6	V6	Y9	Y9	Y9
IOB18A	I/O	5	DQ2		True_of_IOB18B	True	Y8	Y8	Y8	W7	W7	W7	M7	M7	M7	M7	M7	M7	U7	U7	U7	V7	V7	V7	U10	U10	U10
IOB18B	I/O	5	DQ2		Comp_of_IOB18A	True	W9	W9	W9	Y7	Y7	Y7	N7	N7	N7	N7	N7	N7	T9	T9	T9	U8	U8	U8	T10	T10	T10
IOB20A	I/O	5	DQ2		True_of_IOB20B	True	T10	T10	T10	V9	V9	V9	M6	M6	M6	M6	M6	M6	W8	W8	W8	R9	R9	R9	V10	V10	V10

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Note!
[1] UV version.
[2] LV version.
[3] EV version.

Pin Name	Function	BANK	DQS	Configuration Function	Differential Pair	LVDS	UG484[1]	UG484[2]	UG484[3]	UG400[1]	UG400[2]	UG400[3]	UG256[1]	UG256[2]	UG256[3]	PG256[1]	PG256[2]	PG256[3]	UG332[1]	UG332[2]	UG332[3]	UG324[1]	UG324[2]	UG324[3]	PG484[1]	PG484[2]	PG484[3]
IOB20B	I/O	5	DQ2		Comp_of_IOB20A	True	U10	U10	U10	T9	T9	T9	L8	L8	L8	L8	L8	L8	Y8	Y8	Y8	P9	P9	P9	Y11	Y11	Y11
IOB22A	I/O	5	DQ2		True_of_IOB22B	True	V10	V10	V10	P10	P10	P10	P8	P8	P8	P8	P8	P8							U9	U9	U9
IOB22B	I/O	5	DQ2		Comp_of_IOB22A	True	W10	W10	W10	R10	R10	R10	T8	T8	T8	T8	T8	T8							T9	T9	T9
IOB24A	I/O	5	DQ2		True_of_IOB24B	True	T11	T11	T11	Y10	Y10	Y10	N8	N8	N8	N8	N8	N8							AA10	AA10	AA10
IOB24B	I/O	5	DQ2		Comp_of_IOB24A	True	U11	U11	U11	W10	W10	W10	L9	L9	L9	L9	L9	L9							AB10	AB10	AB10
IOB26A	I/O	5	DQ2		True_of_IOB26B	True	V11	V11	V11	U11	U11	U11	M8	M8	M8	M8	M8	M8	W10	W10	W10	N9	N9	N9	V11	V11	V11
IOB26B	I/O	5	DQ2		Comp_of_IOB26A	True	Y11	Y11	Y11	T10	T10	T10	N9	N9	N9	N9	N9	N9	Y10	Y10	Y10	N10	N10	N10	W11	W11	W11
IOB2A	I/O	5	DQ1		True_of_IOB2B	True	AA2	AA2	AA2	W1	W1	W1	P4	P4	P4	P4	P4	P4	W4	W4	W4	V2	V2	V2	Y3	Y3	Y3
IOB2B	I/O	5	DQ1		Comp_of_IOB2A	True	AB2	AB2	AB2	Y1	Y1	Y1	T4	T4	T4	T4	T4	T4	Y4	Y4	Y4	U3	U3	U3	AA3	AA3	AA3
IOB4A	I/O	5	DQ1		True_of_IOB4B	True	AA3	AA3	AA3	W2	W2	W2	T2	T2	T2	T2	T2	T2	V5	V5	V5	T3	T3	T3	W5	W5	W5
IOB4B	I/O	5	DQ1		Comp_of_IOB4A	True	AB3	AB3	AB3	Y2	Y2	Y2	R3	R3	R3	R3	R3	R3	W5	W5	W5	U4	U4	U4	Y4	Y4	Y4
IOB6A	I/O	5	DQ1		True_of_IOB6B	True	U7	U7	U7	V6	V6	V6	R5	R5	R5	R5	R5	R5							AB2	AB2	AB2
IOB6B	I/O	5	DQ1		Comp_of_IOB6A	True	T8	T8	T8	U6	U6	U6	P5	P5	P5	P5	P5	P5							AB3	AB3	AB3
IOB8A	I/O	5	DQ1		True_of_IOB8B	True	AA5	AA5	AA5	W4	W4	W4	T3	T3	T3	T3	T3	T3	Y5	Y5	Y5	R5	R5	R5	U8	U8	U8
IOB8B	I/O	5	DQ1		Comp_of_IOB8A	True	AB5	AB5	AB5	Y4	Y4	Y4	R4	R4	R4	R4	R4	R4	V6	V6	V6	T4	T4	T4	V7	V7	V7
BANK4 True LVDS Pair																											
IOB30A/GCLKT_4	I/O	4	DQ3	GCLKT_4	True_of_IOB30B	True	AB12	AB12	AB12	Y12	Y12	Y12	T9	T9	T9	T9	T9	T9	Y12	Y12	Y12	V10	V10	V10	Y13	Y13	Y13
IOB30B/GCLKC_4	I/O	4	DQ3	GCLKC_4	Comp_of_IOB30A	True	AA12	AA12	AA12	W12	W12	W12	P9	P9	P9	P9	P9	P9	W12	W12	W12	U11	U11	U11	AA14	AA14	AA14
IOB32A	I/O	4	DQ3		True_of_IOB32B	True	V13	V13	V13	P11	P11	P11	R9	R9	R9	R9	R9	R9	U10	U10	U10				Y14	Y14	Y14
IOB32B	I/O	4	DQ3		Comp_of_IOB32A	True	U13	U13	U13	R11	R11	R11	T10	T10	T10	T10	T10	T10	U11	U11	U11				AB15	AB15	AB15
IOB34A	I/O	4	DQ3		True_of_IOB34B	True	Y13	Y13	Y13	V12	V12	V12	M9	M9	M9	M9	M9	M9				V11	V11	V11	AA15	AA15	AA15
IOB34B	I/O	4	DQ3		Comp_of_IOB34A	True	W13	W13	W13	V13	V13	V13	L10	L10	L10	L10	L10	L10				V12	V12	V12	Y15	Y15	Y15
IOB36A	I/O	4	DQ3		True_of_IOB36B	True	T13	T13	T13	Y14	Y14	Y14	P10	P10	P10	P10	P10	P10	T12	T12	T12				Y12	Y12	Y12
IOB36B	I/O	4	DQ3		Comp_of_IOB36A	True	T14	T14	T14	W14	W14	W14	R10	R10	R10	R10	R10	R10	U13	U13	U13				V13	V13	V13
IOB38A	I/O	4	DQ3		True_of_IOB38B	True	Y14	Y14	Y14	Y15	Y15	Y15	N10	N10	N10	N10	N10	N10	W13	W13	W13	P11	P11	P11	T13	T13	T13
IOB38B	I/O	4	DQ3		Comp_of_IOB38A	True	W14	W14	W14	W15	W15	W15	M11	M11	M11	M11	M11	M11	Y14	Y14	Y14	T12	T12	T12	U13	U13	U13
IOB40A	I/O	4	DQ3		True_of_IOB40B	True	Y15	Y15	Y15	Y16	Y16	Y16	T11	T11	T11	T11	T11	T11	W14	W14	W14				W14	W14	W14
IOB40B	I/O	4	DQ3		Comp_of_IOB40A	True	W15	W15	W15	W16	W16	W16	P11	P11	P11	P11	P11	P11	V14	V14	V14				V14	V14	V14
IOB42A	I/O	4	DQ3		True_of_IOB42B	True	V15	V15	V15	Y17	Y17	Y17	M10	M10	M10	M10	M10	M10	U14	U14	U14	U14	U14	U14	Y17	Y17	Y17
IOB42B	I/O	4	DQ3		Comp_of_IOB42A	True	U15	U15	U15	W17	W17	W17	N11	N11	N11	N11	N11	N11	V15	V15	V15	V15	V15	V15	AB18	AB18	AB18
IOB44A	I/O	4	DQ3		True_of_IOB44B	True	Y17	Y17	Y17	P13	P13	P13	R13	R13	R13	R13	R13	R13	U15	U15	U15				Y18	Y18	Y18
IOB44B	I/O	4	DQ3		Comp_of_IOB44A	True	V16	V16	V16	R13	R13	R13	T14	T14	T14	T14	T14	T14	T14	T14	T14				AA19	AA19	AA19
IOB48A	I/O	4	DQS4		True_of_IOB48B	True	AB18	AB18	AB18	V14	V14	V14	R11	R11	R11	R11	R11	R11	Y16	Y16	Y16	P12	P12	P12	AB20	AB20	AB20
IOB48B	I/O	4	DQS4		Comp_of_IOB48A	True	AA18	AA18	AA18	U14	U14	U14	T12	T12	T12	T12	T12	T12	W16	W16	W16	R14	R14	R14	AB21	AB21	AB21
IOB50A/SCLK	I/O	4	DQ4	SCLK	True_of_IOB50B	True	T9	T9	T9	W6	W6	W6	P6	P6	P6	P6	P6	P6	V7	V7	V7	T6	T6	T6	AB6	AB6	AB6
IOB50B/D1/SO	I/O	4	DQ4	D1/SO	Comp_of_IOB50A	True	U9	U9	U9	Y6	Y6	Y6	T6	T6	T6	T6	T6	T6	W7	W7	W7	U6	U6	U6	Y7	Y7	Y7
IOB52A/FASTRD_N/D3	I/O	4	DQ4	FASTRD_N /D3	True_of_IOB52B	True	AB20	AB20	AB20	Y19	Y19	Y19	P12	P12	P12	P12	P12	P12							Y19	Y19	Y19
IOB52B/QSSPI_WPN	I/O	4	DQ4	QSSPI_WPN	Comp_of_IOB52A	True	AA20	AA20	AA20	W19	W19	W19	T13	T13	T13	T13	T13	T13							W18	W18	W18
IOB54A/SSPI_CS_N/D0	I/O	4	DQ4	SSPI_CS_N/D0	True_of_IOB54B	True	AB21	AB21	AB21	Y20	Y20	Y20	R12	R12	R12	R12	R12	R12	W17	W17	W17	U16	U16	U16	AA20	AA20	AA20
IOB54B/SI/D2	I/O	4	DQ4	SI/D2	Comp_of_IOB54A	True	AA21	AA21	AA21	W20	W20	W20	P13	P13	P13	P13	P13	P13	V17	V17	V17	V17	V17	V17	W19	W19	W19
BANK3 True LVDS Pair																											
IOR28A/GCLKT_3	I/O	3	none	GCLKT_3	True_of_IOR28B	True	M22	M22	M22	K19	K19	K19	H14	H14	H14	H14	H14	H14	J19	J19	J19	H18	H18	H18	N22	N22	N22
IOR28B/GCLKC_3	I/O	3	none	GCLKC_3	Comp_of_IOR28A	True	M21	M21	M21	K20	K20	K20	H16	H16	H16	H16	H16	H16	J20	J20	J20	K15	K15	K15	N21	N21	N21
IOR30A	I/O	3	none		True_of_IOR30B	True	M16	M16	M16	L19	L19	L19	J15	J15	J15	J15	J15	J15	L20	L20	L20	K12	K12	K12	M16	M16	M16
IOR30B	I/O	3	none		Comp_of_IOR30A	True	N16	N16	N16	L20	L20	L20	K16	K16	K16	K16	K16	K16	L19	L19	L19	K13	K13	K13	M17	M17	M17
IOR32A	I/O	3	none		True_of_IOR32B	True	N22	N22	N22	M20	M20	M20	K14	K14	K14	K14	K14	K14	K18	K18	K18	K18	K18	K18	M19	M19	M19
IOR32B	I/O	3	none		Comp_of_IOR32A	True	P21	P21	P21	M19	M19	M19	K15	K15	K15	K15	K15	K15	K19	K19	K19	L16	L16	L16	M18	M18	M18
IOR34A	I/O	3	none		True_of_IOR34B	True	R22	R22	R22	M17	M17	M17	J11	J11	J11	J11	J11	J11	N20	N20	N20				V20	V20	V20
IOR34B	I/O	3	none		Comp_of_IOR34A	True	R21	R21	R21	N20	N20	N20	L12	L12	L12	L12	L12	L12	N19	N19	N19				W21	W21	W21
IOR36A	I/O	3	none		True_of_IOR36B	True	T22	T22	T22	M16	M16	M16	L16	L16	L16	L16	L16	L16	M16	M16	M16	L18	L18	L18	T22	T22	T22
IOR36B	I/O	3	none		Comp_of_IOR36A	True	T21	T21	T21	N19	N19	N19	L14	L14	L14	L14	L14	L14	P17	P17	P17	M18	M18	M18	T21	T21	T21
IOR38A	I/O	3	none		True_of_IOR38B	True	P17	P17	P17	N18	N18	N18	K13	K13	K13	K13	K13	K13	P19	P19	P19	L14	L14	L14	T20	T20	T20
IOR38B	I/O	3	none		Comp_of_IOR38A	True	P16	P16	P16	N17	N17	N17	K12	K12	K12	K12	K12	K12	P18	P18	P18	N17	N17	N17	U22	U22	U22
IOR40A	I/O	3	none		True_of_IOR40B	True	V22	V22	V22	P18	P18	P18	L15	L15	L15	L15	L15	L15	R20	R20	R20	K14	K14	K14	P16	P16	P16
IOR40B	I/O	3	none		Comp_of_IOR40A	True	W22	W22	W22	R20	R20	R20	M16	M16	M16	M16	M16	M16	R19	R19	R19	J18	J18	J18	P17	P17	P17
IOR42A	I/O	3	none		True_of_IOR42B	True	R18	R18	R18	N16	N16	N16	K11	K11	K11	K11	K11	K11	R18	R18	R18	M14	M14	M14	R19	R19	R19
IOR42B	I/O	3	none		Comp_of_IOR42A	True	R17	R17	R17	R19	R19	R19	L13	L13	L13	L13	L13	L13	T20	T20	T20	N16	N16	N16	R18	R18	R18
IOR44A	I/O	3	none		True_of_IOR44B	True	T19	T19	T19	U20	U20	U20	M14	M14	M14	M14	M14	M14	U17	U17	U17				T19	T19	T19
IOR44B	I/O	3	none		Comp_of_IOR44A	True	T18	T18	T18	P17	P17	P17	M15	M15	M15	M15	M15	M15	T17	T17	T17				U19	U19	U19
IOR46A	I/O	3	none		True_of_IOR46B	True	Y22	Y22	Y22	V20	V20	V20	N15	N15	N15	N15	N15	N15	W20	W20	W20	P16	P16	P16	Y22	Y22	Y22
IOR46B	I/O	3	none		Comp_of_IOR46A	True	W21	W21	W21	P16	P16	P16	P16	P16	P16	P16	P16	P16	V19	V19	V19	T18	T18	T18	AA22	AA22	AA22
IOR48A	I/O	3	none		True_of_IOR48B	True	AA22	AA22	AA22	R17	R17	R17	N16	N16	N16	N16	N16	N16	N18	N18	N18				W20	W20	W20
IOR48B	I/O	3	none		Comp_of_IOR48A	True	Y21	Y21	Y21	U18	U18	U18	N14	N14	N14	N14	N14	N14	P20	P20	P20				V19	V19	V19
IOR50A	I/O	3	none		True_of_IOR50B	True	V18	V18	V18	V19	V19	V19	P15	P15	P15	P15	P15	P15	V20	V20	V20	R16	R16	R16	Y21	Y21	Y21

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Note!
[1] UV version.
[2] LV version.
[3] EV version.

Pin Name	Function	BANK	DQS	Configuration Function	Differential Pair	LVDS	UG484[1]	UG484[2]	UG484[3]	UG400[1]	UG400[2]	UG400[3]	UG256[1]	UG256[2]	UG256[3]	PG256[1]	PG256[2]	PG256[3]	UG332[1]	UG332[2]	UG332[3]	UG324[1]	UG324[2]	UG324[3]	PG484[1]	PG484[2]	PG484[3]
IOR50B	I/O	3	none		Comp_of_IOR50A	True	W20	W20	W20	T17	T17	T17	R16	R16	R16	R16	R16	R16	U18	U18	U18	T17	T17	T17	Y20	Y20	Y20
BANK2 True LVDS Pair																											
IOR11A	I/O	2	none		True_of_IOR11B	True	G21	G21	G21	G16	G16	G16	E16	E16	E16	E16	E16	E16	F17	F17	F17				F19	F19	F19
IOR11B	I/O	2	none		Comp_of_IOR11A	True	G20	G20	G20	F18	F18	F18	F15	F15	F15	F15	F15	F15	G16	G16	G16				G19	G19	G19
IOR13A	I/O	2	none		True_of_IOR13B	True	H22	H22	H22	F19	F19	F19	F13	F13	F13	F13	F13	F13	G17	G17	G17	G16	G16	G16	J17	J17	J17
IOR13B	I/O	2	none		Comp_of_IOR13A	True	H21	H21	H21	F20	F20	F20	G12	G12	G12	G12	G12	G12	H16	H16	H16	H15	H15	H15	J16	J16	J16
IOR15A	I/O	2	none		True_of_IOR15B	True	H19	H19	H19	J14	J14	J14	F14	F14	F14	F14	F14	F14				E18	E18	E18	J20	J20	J20
IOR15B	I/O	2	none		Comp_of_IOR15A	True	H18	H18	H18	J15	J15	J15	F16	F16	F16	F16	F16	F16				G17	G17	G17	G20	G20	G20
IOR17A	I/O	2	none		True_of_IOR17B	True	J18	J18	J18	H18	H18	H18	F12	F12	F12	F12	F12	F12	H17	H17	H17	H16	H16	H16	J18	J18	J18
IOR17B	I/O	2	none		Comp_of_IOR17A	True	J19	J19	J19	H19	H19	H19	G13	G13	G13	G13	G13	G13	J16	J16	J16	F18	F18	F18	J19	J19	J19
IOR19A	I/O	2	none		True_of_IOR19B	True	J21	J21	J21	J17	J17	J17	G15	G15	G15	G15	G15	G15							H20	H20	H20
IOR19B	I/O	2	none		Comp_of_IOR19A	True	J22	J22	J22	H20	H20	H20	G14	G14	G14	G14	G14	G14							H21	H21	H21
IOR21A	I/O	2	none		True_of_IOR21B	True	K19	K19	K19	K14	K14	K14	G11	G11	G11	G11	G11	G11	H20	H20	H20	J16	J16	J16	H22	H22	H22
IOR21B	I/O	2	none		Comp_of_IOR21A	True	K18	K18	K18	K15	K15	K15	H12	H12	H12	H12	H12	H12	J18	J18	J18	J17	J17	J17	F22	F22	F22
IOR23A	I/O	2	none		True_of_IOR23B	True	L17	L17	L17	J19	J19	J19	G16	G16	G16	G16	G16	G16							L17	L17	L17
IOR23B	I/O	2	none		Comp_of_IOR23A	True	L16	L16	L16	J20	J20	J20	H15	H15	H15	H15	H15	H15							L16	L16	L16
IOR25A	I/O	2	none		True_of_IOR25B	True	K22	K22	K22	K17	K17	K17	H13	H13	H13	H13	H13	H13	K17	K17	K17				L21	L21	L21
IOR25B	I/O	2	none		Comp_of_IOR25A	True	L21	L21	L21	K18	K18	K18	J12	J12	J12	J12	J12	J12	L17	L17	L17				L22	L22	L22
IOR2A/RPLL1_T_fb	I/O	2	DQ5	RPLL1_T_fb	True_of_IOR2B	True	C21	C21	C21	D17	D17	D17	D14	D14	D14	D14	D14	D14	D18	D18	D18	B18	B18	B18	D19	D19	D19
IOR2B/RPLL1_C_fb	I/O	2	DQ5	RPLL1_C_fb	Comp_of_IOR2A	True	C22	C22	C22	C18	C18	C18	E15	E15	E15	E15	E15	E15	D19	D19	D19	C17	C17	C17	C21	C21	C21
IOR4A/RPLL1_T_in	I/O	2	DQ5	RPLL1_T_in	True_of_IOR4B	True	D22	D22	D22	C19	C19	C19	D16	D16	D16	D16	D16	D16	D20	D20	D20	E15	E15	E15	E19	E19	E19
IOR4B/RPLL1_C_in	I/O	2	DQ5	RPLL1_C_in	Comp_of_IOR4A	True	D21	D21	D21	E17	E17	E17	E14	E14	E14	E14	E14	E14	E18	E18	E18	C18	C18	C18	D20	D20	D20
IOR6A	I/O	2	DQS5		True_of_IOR6B	True	E22	E22	E22	B20	B20	B20	C15	C15	C15	C15	C15	C15							B22	B22	B22
IOR6B	I/O	2	DQS5		Comp_of_IOR6A	True	E21	E21	E21	C20	C20	C20	B16	B16	B16	B16	B16	B16							C22	C22	C22
IOR8A	I/O	2	DQ5		True_of_IOR8B	True	F22	F22	F22	D19	D19	D19	C16	C16	C16	C16	C16	C16	E17	E17	E17	E16	E16	E16	H18	H18	H18
IOR8B	I/O	2	DQ5		Comp_of_IOR8A	True	G22	G22	G22	F17	F17	F17	D15	D15	D15	D15	D15	D15	F16	F16	F16	H13	H13	H13	H19	H19	H19
BANK1 True LVDS Pair																											
IOT30A	I/O	1	DQ7		True_of_IOT30B	True	D12	D12	D12	A12	A12	A12							A11	A11	A11	C10	C10	C10	D12	D12	D12
IOT30B	I/O	1	DQ7		Comp_of_IOT30A	True	E12	E12	E12	B12	B12	B12							B11	B11	B11	B11	B11	B11	E12	E12	E12
IOT32A	I/O	1	DQ7		True_of_IOT32B	True	G12	G12	G12	A13	A13	A13							B12	B12	B12	B12	B12	B12	A12	A12	A12
IOT32B	I/O	1	DQ7		Comp_of_IOT32A	True	F12	F12	F12	B13	B13	B13							C12	C12	C12	C11	C11	C11	B12	B12	B12
IOT34A	I/O	1	DQ7		True_of_IOT34B	True	A13	A13	A13	G11	G11	G11	F8	F8	F8	F8	F8	F8	D12	D12	D12	A11	A11	A11	C13	C13	C13
IOT34B	I/O	1	DQ7		Comp_of_IOT34A	True	B13	B13	B13	F11	F11	F11	D9	D9	D9	D9	D9	D9	D13	D13	D13	A12	A12	A12	B14	B14	B14
IOT36A	I/O	1	DQ7		True_of_IOT36B	True	A14	A14	A14	D12	D12	D12	B9	B9	B9	B9	B9	B9	E12	E12	E12	F9	F9	F9	F11	F11	F11
IOT36B	I/O	1	DQ7		Comp_of_IOT36A	True	B14	B14	B14	C12	C12	C12	A10	A10	A10	A10	A10	A10	D14	D14	D14	F10	F10	F10	G11	G11	G11
IOT38A	I/O	1	DQ7		True_of_IOT38B	True	G14	G14	G14	A14	A14	A14	F9	F9	F9	F9	F9	F9	B14	B14	B14	C12	C12	C12	B15	B15	B15
IOT38B	I/O	1	DQ7		Comp_of_IOT38A	True	F14	F14	F14	B14	B14	B14	E11	E11	E11	E11	E11	E11	C14	C14	C14	B13	B13	B13	C15	C15	C15
IOT40A	I/O	1	DQ7		True_of_IOT40B	True	A15	A15	A15	A15	A15	A15	D10	D10	D10	D10	D10	D10	A13	A13	A13	A13	A13	A13	G13	G13	G13
IOT40B	I/O	1	DQ7		Comp_of_IOT40A	True	B15	B15	B15	B15	B15	B15	E10	E10	E10	E10	E10	E10	B13	B13	B13	A14	A14	A14	F13	F13	F13
IOT42A	I/O	1	DQ7		True_of_IOT42B	True	A16	A16	A16	A16	A16	A16	A11	A11	A11	A11	A11	A11	E14	E14	E14	B14	B14	B14	C16	C16	C16
IOT42B	I/O	1	DQ7		Comp_of_IOT42A	True	B17	B17	B17	B16	B16	B16	C11	C11	C11	C11	C11	C11	E15	E15	E15	B15	B15	B15	A17	A17	A17
IOT44A	I/O	1	DQ7		True_of_IOT44B	True	A17	A17	A17	A17	A17	A17	F10	F10	F10	F10	F10	F10	A15	A15	A15	F11	F11	F11	D15	D15	D15
IOT44B	I/O	1	DQ7		Comp_of_IOT44A	True	B18	B18	B18	B17	B17	B17	D11	D11	D11	D11	D11	D11	B15	B15	B15	C13	C13	C13	E15	E15	E15
IOT48A	I/O	1	DQS6		True_of_IOT48B	True	A18	A18	A18	C15	C15	C15	B11	B11	B11	B11	B11	B11	D17	D17	D17	C14	C14	C14	C18	C18	C18
IOT48B	I/O	1	DQS6		Comp_of_IOT48A	True	B19	B19	B19	C16	C16	C16	A12	A12	A12	A12	A12	A12	D16	D16	D16	C15	C15	C15	B19	B19	B19
IOT50A	I/O	1	DQ6		True_of_IOT50B	True	A19	A19	A19	A18	A18	A18	B13	B13	B13	B13	B13	B13	A19	A19	A19	A15	A15	A15	E16	E16	E16
IOT50B	I/O	1	DQ6		Comp_of_IOT50A	True	B20	B20	B20	B18	B18	B18	A14	A14	A14	A14	A14	A14	B18	B18	B18	A16	A16	A16	F15	F15	F15
IOT52A	I/O	1	DQ6		True_of_IOT52B	True	A20	A20	A20	E15	E15	E15	C12	C12	C12	C12	C12	C12	B16	B16	B16	B16	B16	B16	C19	C19	C19
IOT52B	I/O	1	DQ6		Comp_of_IOT52A	True	B21	B21	B21	D16	D16	D16	B12	B12	B12	B12	B12	B12	C16	C16	C16	A17	A17	A17	D18	D18	D18
IOT54A	I/O	1	DQ6		True_of_IOT54B	True	A21	A21	A21	B19	B19	B19	B14	B14	B14	B14	B14	B14	A18	A18	A18	D14	D14	D14	E17	E17	E17
IOT54B	I/O	1	DQ6		Comp_of_IOT54A	True	B22	B22	B22	A20	A20	A20	A15	A15	A15	A15	A15	A15	C17	C17	C17	D15	D15	D15	F17	F17	F17
BANK0 True LVDS Pair																											
IOT12A	I/O	0	DQ8		True_of_IOT12B	True	B5	B5	B5	B4	B4	B4	A3	A3	A3	A3	A3	A3	C6	C6	C6	A4	A4	A4	A5	A5	A5
IOT12B	I/O	0	DQ8		Comp_of_IOT12A	True	A6	A6	A6	A4	A4	A4	B4	B4	B4	B4	B4	B4	D7	D7	D7	A5	A5	A5	C6	C6	C6
IOT14A	I/O	0	DQ8		True_of_IOT14B	True	B6	B6	B6	B5	B5	B5	D6	D6	D6	D6	D6	D6	A7	A7	A7	B6	B6	B6	E9	E9	E9
IOT14B	I/O	0	DQ8		Comp_of_IOT14A	True	A7	A7	A7	A5	A5	A5	E7	E7	E7	E7	E7	E7	B8	B8	B8	A6	A6	A6	D9	D9	D9
IOT16A	I/O	0	DQ8		True_of_IOT16B	True	C8	C8	C8	B6	B6	B6							D8	D8	D8	D8	D8	D8	B7	B7	B7
IOT16B	I/O	0	DQ8		Comp_of_IOT16A	True	D8	D8	D8	A6	A6	A6							E9	E9	E9	E7	E7	E7	A7	A7	A7
IOT18A	I/O	0	DQ8		True_of_IOT18B	True	B8	B8	B8	B7	B7	B7	B7	B7	B7	B7	B7	B7	B6	B6	B6	A7	A7	A7	E8	E8	E8
IOT18B	I/O	0	DQ8		Comp_of_IOT18A	True	A8	A8	A8	A7	A7	A7	C7	C7	C7	C7	C7	C7	A6	A6	A6	B7	B7	B7	D8	D8	D8
IOT20A	I/O	0	DQ8		True_of_IOT20B	True	B9	B9	B9	B8	B8	B8	E6	E6	E6	E6	E6	E6	D9	D9	D9	B8	B8	B8	E10	E10	E10
IOT20B	I/O	0	DQ8		Comp_of_IOT20A	True	A9	A9	A9	A8	A8	A8	D7	D7	D7	D7	D7	D7	E10	E10	E10	A8	A8	A8	C11	C11	C11
IOT22A	I/O	0	DQ8		True_of_IOT22B	True	F10	F10	F10	B9	B9	B9	F7	F7	F7	F7	F7	F7							E11	E11	E11
IOT22B	I/O	0	DQ8		Comp_of_IOT22A	True	E10	E10	E10	A9	A9	A9	E8	E8	E8	E8	E8	E8							D11	D11	D11
IOT24A/GCLKT_0	I/O	0	DQ8	GCLKT_0	True_of_IOT24B	True	B10	B10	B10	B10	B10	B10	C8	C8	C8	C8	C8	C8	B9	B9	B9	A9	A9	A9	B9	B9	B9

Note!
[1] UV version.
[2] LV version.
[3] EV version.

Pin Name	Function	BANK	DQS	Configuration Function	Differential Pair	LVDS	UG484[1]	UG484[2]	UG484[3]	UG400[1]	UG400[2]	UG400[3]	UG256[1]	UG256[2]	UG256[3]	PG256[1]	PG256[2]	PG256[3]	UG332[1]	UG332[2]	UG332[3]	UG324[1]	UG324[2]	UG324[3]	PG484[1]	PG484[2]	PG484[3]
IOT24B/GCLKC_0	I/O	0	DQ8	GCLKC_0	Comp_of_IOT24A	True	A10	A10	A10	A10	A10	A10	A8	A8	A8	A8	A8	A8	A9	A9	A9	B9	B9	B9	C10	C10	C10
IOT26A	I/O	0	DQ8		True_of_IOT26B	True	B11	B11	B11	B11	B11	B11	D8	D8	D8	D8	D8	D8	C10	C10	C10	A10	A10	A10	B11	B11	B11
IOT26B	I/O	0	DQ8		Comp_of_IOT26A	True	A11	A11	A11	A11	A11	A11	E9	E9	E9	E9	E9	E9	B10	B10	B10	B10	B10	B10	A11	A11	A11
IOT2A	I/O	0	DQ9		True_of_IOT2B	True	B1	B1	B1	B1	B1	B1	C4	C4	C4	C4	C4	C4	C4	C4	C4	A2	A2	A2	D4	D4	D4
IOT2B	I/O	0	DQ9		Comp_of_IOT2A	True	A2	A2	A2	A1	A1	A1	B5	B5	B5	B5	B5	B5	B4	B4	B4	B3	B3	B3	B3	B3	B3
IOT4A	I/O	0	DQ9		True_of_IOT4B	True	B2	B2	B2	G7	G7	G7	B3	B3	B3	B3	B3	B3	A4	A4	A4	C3	C3	C3	D5	D5	D5
IOT4B	I/O	0	DQ9		Comp_of_IOT4A	True	A3	A3	A3	F7	F7	F7	A2	A2	A2	A2	A2	A2	C5	C5	C5	C4	C4	C4	C4	C4	C4
IOT6A	I/O	0	DQ9		True_of_IOT6B	True	B3	B3	B3	B2	B2	B2	A4	A4	A4	A4	A4	A4	B5	B5	B5	D5	D5	D5	A2	A2	A2
IOT6B	I/O	0	DQ9		Comp_of_IOT6A	True	A4	A4	A4	A2	A2	A2	C5	C5	C5	C5	C5	C5	A5	A5	A5	B5	B5	B5	A3	A3	A3
IOT8A	I/O	0	DQ9		True_of_IOT8B	True	B4	B4	B4	B3	B3	B3	A5	A5	A5	A5	A5	A5	E7	E7	E7	A3	A3	A3	D6	D6	D6
IOT8B	I/O	0	DQ9		Comp_of_IOT8A	True	A5	A5	A5	A3	A3	A3	B6	B6	B6	B6	B6	B6	D6	D6	D6	B4	B4	B4	D7	D7	D7

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Note!
[1] It is recommended to set Bank VCCIO of True LVDS to 2.5V.
[2] VCCX should be greater than or equal to VCCIO.

Recommended Operating Conditions of UG484/UG400/UG256/PG256/UG332/UG324/PG484 Package in GW2AN-18X (UV Version)			
Name	**Description**	**Min.**	**Max.**
VCC/VCCX	Core voltage and auxiliary voltage are internally short-circuited.	2.7V	3.6V
VCCIO0, VCCIO1, VCCIO2, VCCIO3, VCCIO4, VCCIO6, VCCIO7, VCCIO8, VCCIO9	I/O Bank voltage	1.14V	3.6V
VCCIO5	I/O Bank5 voltage When the voltage is less than 2.0V, VCCIO5 will add about 20mA quiescent current.	1.14V	3.6V

Recommended Operating Conditions of UG484/UG400/UG256/PG256/UG332/UG324/PG484 Package in GW2AN-18X (LV Version)			
Name	**Description**	**Min.**	**Max.**
VCC	Core voltage	0.95V	1.05V
VCCIO1, VCCIO2, VCCIO3, VCCIO4, VCCIO6, VCCIO7, VCCIO8, VCCIO9	I/O Bank voltage	1.14V	3.6V
VCCX/VCCIO0	Core voltage and I/O Bank0 voltage are internally short-circuited.	2.7V	3.6V
VCCIO5	I/O Bank5 voltage When the voltage is less than 2.0V, VCCIO5 will add about 20mA quiescent current.	1.14V	3.6V

Recommended Operating Conditions of UG484/UG400/UG256/PG256/UG332/UG324/PG484 Package in GW2AN-18X (EV Version)			
Name	**Description**	**Min.**	**Max.**
VCC	Core voltage	1.14V	1.26V
VCCIO1, VCCIO2, VCCIO3, VCCIO4, VCCIO6, VCCIO7, VCCIO8, VCCIO9	I/O Bank voltage	1.14V	3.6V
VCCX/VCCIO0	Core voltage and I/O Bank0 voltage are internally short-circuited.	2.7V	3.6V
VCCIO5	I/O Bank5 voltage When the voltage is less than 2.0V, VCCIO5 will add about 20mA quiescent current.	1.14V	3.6V

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