GW2A-55

Package & Pinout User Guide

Revision History

Date	Version	Description
01/28/2021	1.0E	Initial version.
10/20/2022	1.1E	• Four pins of IOR50[A/B] and IOR51[A/B] of UG676 package updated. • NC pins removed. • Pin definitions updated.

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1 About This Guide

1.1 Purpose

This manual mainly contains an introduction to GW2AN-55 together with a definition of the pins, list of pin numbers, distribution of pin, and package diagram.

1.2 Related Documents

The latest user guides are available on GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- DS976, GW2AN-55 Data Sheet
- UG974, GW2AN-55 Pinout
- UG290, Gowin FPGA Products Programming and Configuration User Guide

1.3 Abbreviations and Terminology

The abbreviations and terminologies used in this manual are set out in Table 1-1 below.

Table 1-1 Abbreviations and Terminology

Abbreviations and Terminology	Name
FPGA	Field Programmable Gate Array
LVDS	Low-Voltage Differential Signaling
UG676	UBGA676

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

GW2AN-55 is the first-generation products of Arora family. They are available in various forms that offer high I/O compatibility and flexible usage.

2.1 PB-Free Package

GW2AN-55 is PB free, in line with the EU ROHS environmental directives. The substances used in GW2AN-55 are in full compliance with the IPC-1752 standards.

2.2 Package Information, Max. User I/O, and LVDS Pairs

Table 2-1 Package Information, Max. User I/O, and LVDS Pairs

Package	Pitch(mm)	Size(mm)	GW2AN-55
UG676	0.8	21 x 21	525 (111)

Note!

- The package types in this manual are written with abbreviations. See 1.3 Abbreviations and Terminology.
- The JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The data in this table is when the loaded four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O.

2.3 Power Pin

Table 2-2 GW2AN-55 Power Pin

VCC	VCCO0	VCCO1	VCCO2
VCCO3	VCCO4	VCCO5	VCCO6
VCCO7	VCCX	VSS	VCCPLLL0
VCCPLLL1	VCCPLLR0	VCCPLLR1	VCCPLLL
VCCPLLR	–	–	–

2.4 Pin Quantity

2.4.1 Quantity of GW2AN-55 Pins

Table 2-3 Quantity of GW2AN-55 Pins

Pin Type		GW2AN-55
		UG676
I/O Single end/Differential pair/LVDS/LVDS output[1]	BANK0	68/34/14/0
	BANK1	71/35/16/0
	BANK2	66/33/13/3
	BANK3	58/29/13/4
	BANK4	72/36/16/0
	BANK5	68/34/14/0
	BANK6	56/28/12/4
	BANK7	66/33/13/3
Max. User I/O [2]		525
Differential Pair		262
True LVDS Output		111
Only True LVDS Output[3]		14
VCC		19
VCCX		14
VCCO0		5
VCCO1		4
VCCO2		5
VCCO3		4
VCCO4		5
VCCO5		4
VCCO6		5
VCCO7		4
VCCPLLL		2
VCCPLLR		2
VSS		77
MODE0		1
MODE1		1
MODE2		1
EXTR		0
NC		0
JTAGSEL_N		1

Note!

- [1] I/O Single end/ Differential pair/LVDS/ LVDS output quantity include CLK pins and download pins; The EXTR No. is excluded;

- [2] The JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The data in this table is when the loaded four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O;
- [3] Support true LVDS output only, do not support input.

2.5 Pin Definitions

The location of the Pins in GW2AN-55 varies according to the different packages.

Table 2-4 provides a detailed overview of user I/O, multi-function pins, dedicated pins, and other pins.

Table 2-4 Definition of the Pins in GW2AN-55

Pin Name	I/O	Description
User I/O Pins		
IO[End][Row/Column Number][A/B]	I/O/LVDS	[End] indicates the pin location, including L (left) R(right) B(bottom), and T(top). [Row/Column Number] indicates the pin Row/Column number. If [End] is T (top) or B (bottom), the pin indicates the column number of the corresponding CFU. If [End] is L (left) or R (right), the pin indicates the Row number of the corresponding CFU. [A/B] indicates differential signal pair information. LVDS in the I/O column indicates that the pin support LVDS output only.
Multi-Function Pins		
IO[End][Row/Column Number][A/B]/MMM		/MMM represents one or more of the other functions in addition to being general purpose user I/O. These pins can be used as user I/O when the functions are not used.
RECONFIG_N	I, internal weak pull-up	Start new GowinCONFIG mode when low pulse
READY[2]	I/O	When high level, the device can be programmed and configured. When low level, the device cannot be programmed and configured.
DONE[2]	I/O	High level indicates successful program and configure Low level indicates incomplete or failed to program and configure.
FASTRD_N/D3	I/O	In MSPI mode, FASTRD_N is used as Flash access speed port. Low indicates high-speed Flash access mode; high indicates regular Flash access mode. Data port D3 in CPU mode
MCLK/D4	I/O	Clock output MCLK in MSPI mode Data port D4 in CPU mode
MCS_N/D5	I/O	Enable signal MCS_N in MSPI mode, active-low. Data port D5 in CPU mode
MI/D7	I/O	MISO in MSPI mode: Master data input/Slave data output Data port D7 in CPU mode
MO/D6	I/O	MISO in MSPI mode: Master data output/Slave data input Data port D6 in CPU mode
SSPI_CS_N/D0	I/O	Enable signal SSPI_CS_N in SSPI mod, active-low, Internal

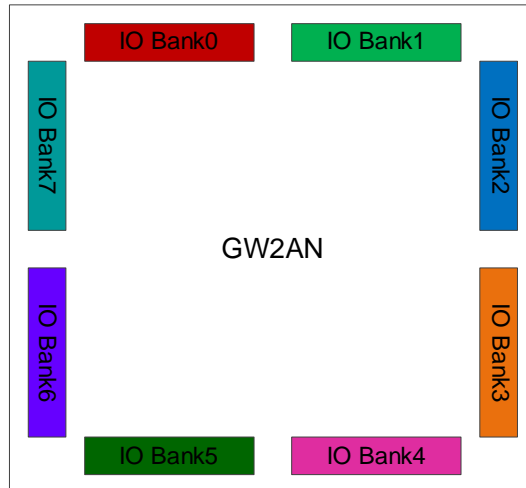| Pin Name	I/O	Description
		Weak Pull Up. Data port D0 in CPU mode
SO/D1	I/O	MISO in MSPI mode: Master data input/Slave data output Data port D1 in CPU mode
SI/D2	I/O	MISO in MSPI mode: Master data output/Slave data input Data port D2 in CPU mode
TMS	I, internal weak pull-up	Serial mode input in JTAG mode
TCK	I	Serial clock input in JTAG mode, which needs to be connected with 4.7 K drop-down resistance on PCB.
TDI	I, internal weak pull-up	Serial data input in JTAG mode
TDO	O	Serial data output in JTAG mode
JTAGSEL_N	I, internal weak pull-up	Select signal in JTAG mode, active-low.
SCLK	I	Clock input in SSPI, SERIAL, and CPU mode.
DIN	I, internal weak pull-up	Input data in SERIAL mode
DOUT	O	Output data in SERIAL mode
GCLKT_[x]	I	Pins for global clock input, T(True), [x]: global clock No.
GCLKC_[x]	I	Differential comparation input pin of GCLKT_[x], C(Comp), [x]: global clock No.[1].
LPLL_T_fb/RPLL_T_fb	I	L/R PLL feedback input pin, T(True).
LPLL_C_fb/RPLL_C_fb	I	L/R PLL feedback input pin, C(Comp).
LPLL_T_in/RPLL_T_in	I	L/R PLL clock input pin, T(True).
LPLL_C_in/RPLL_C_in	I	L/R PLL clock input pin, C(Comp).
MODE2	I, internal weak pull-up	GowinCONFIG modes selection pin; if this pin is not bonded, it's internal grounded.
MODE1	I, internal weak pull-up	GowinCONFIG modes selection pin; if this pin is not bonded, it's internal grounded.
MODE0	I, internal weak pull-up	GowinCONFIG modes selection pin; if this pin is not bonded, it's internal grounded.
EXTR	NA	External 10K 1% resister grounding
The Other Pins		
NC	NA	Reserved
VSS	NA	Ground pins
VCC	NA	Power supply pins for internal core logic
VCCO#	NA	Power supply pins for the I/O voltage of I/O BANK#
VCCX	NA	Power supply pins for auxiliary voltage
VCCPLLL	NA	PBGA: Power supply pins for left PLL0/1
VCCPLLR	NA	PBGA: Power supply pins for right PLL0/1

Note！

- [1] When the input is single-ended, the GLKC_[x] pin is not a global clock pin.

- [2] The default state of READY/DONE is open-drain output, internal weak pull-up. DONE outputs 0 during configuration.

2.6 Introduction to the I/O BANK

There are eight I/O Banks in GW2AN-55, as shown in Figure 2-1.

Figure 2-1 GW2AN-55 I/O Bank Distribution

This manual provides an overview of the distribution view of the pins in GW2AN-55. The eight I/O Banks that form GW2AN-55 is marked with eight different colors.

User I/O, power, and ground are marked with different symbols and colors. The various symbols and colors used for the various pins are defined as follows:

- " ⬦ " denotes I/Os in BANK0. The filling color changes with the BANK.

- " ⬦ " denotes I/Os in BANK1. The filling color changes with the BANK.

- " ⬦ " denotes I/Os in BANK2. The filling color changes with the BANK.

- " ⬦ " denotes I/Os in BANK3. The filling color changes with the BANK.

- " ⬦ " denotes I/Os in BANK4. The filling color changes with the BANK.

- " ⬦ " denotes I/Os in BANK5. The filling color changes with the BANK.

- " ⬦ " denotes I/Os in BANK6. The filling color changes with the BANK.

- " ⬦ " denotes I/Os in BANK7. The filling color changes with the BANK.

- " ⚡ " denotes VCC, VCCX, and VCCO. The filling color does not change.

- " ⏚ " denotes VSS. The filling color does not change.

- " ⬦ " denotes NC.

● " E " denotes dedicated pins EXTR.

3 View of Pin Distribution

3.1 View of GW2AN-55 Pin Distribution

3.1.1 View of UG676 Pin Distribution
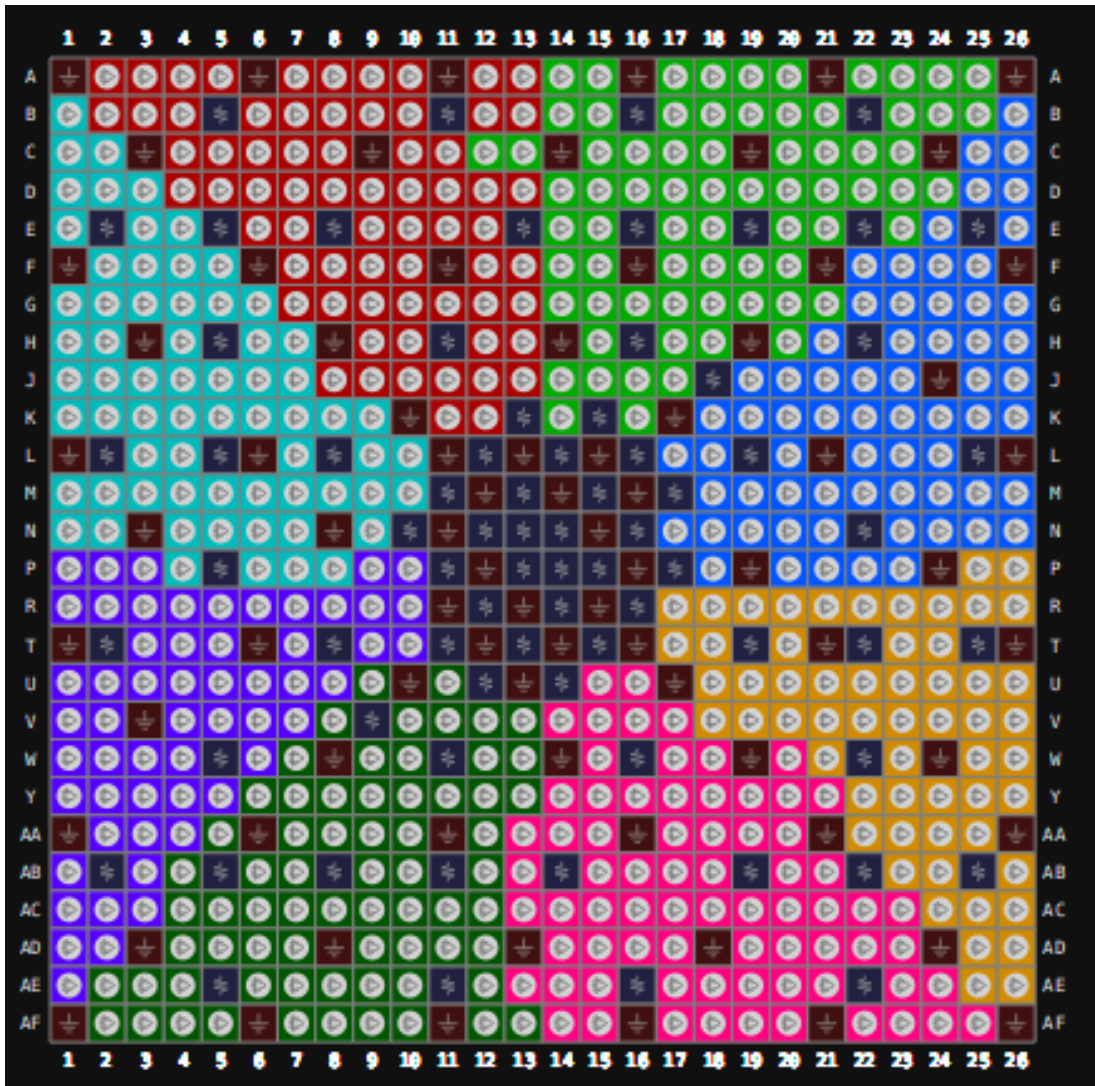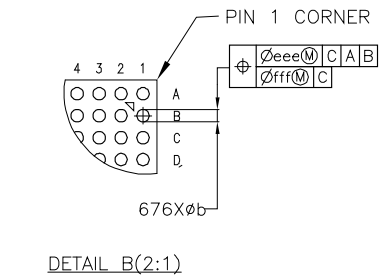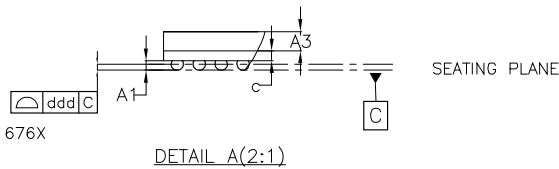
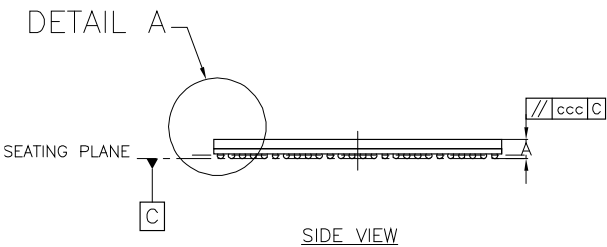**Figure 3-1 View of GW2AN-55 UG676 Pin Distribution (Top View)**

Table 3-1 Other Pins in GW2AN-55 UG676

VCC	K15,L12,L14,L16,M13,M17,N12,N13,N14,N16,P11,P13,P14,P15,R12,F 14,R16,T13,U12
VCCO0	B11,B5,E13,E8,H11
VCCO1	B16,B22,E19,H16
VCCO2	E25,H22,L19,L25,N22
VCCO3	AB25,T19,T25,W22
VCCO4	AB14,AB19,AE16,AE22,W16
VCCO5	AB8,AE11,AE5,W11
VCCO6	AB2,P5,T2,T8,W5
VCCO7	E2,H5,L2,L8
VCCX	AB11,AB22,AB5,E16,E22,E5,J18,K13,L5,N10,P17,T22,U14,V9
VCCPLLL	M11,M15
VCCPLLR	T11,T15
VSS	A1,A11,,A16,A21,A26,A6,AA1,AA11,AA16,,AA21,AA26,AA6,AD13,AD1 8,AD24,AD3,AD8,AF1,AF11,AF16,AF21,AF26,AF6,C14,C19,C24,C3,C 9,F1,F11,F16,F21,F26,F6,H14,H19,H3,H8,J24,K10,K17,L1,L11,L13,L1 ,L21,L26,L6,M12,M14,M16,N11,N15,N3,N8,P12,P16,P19,P24,R11,R13 R15,T1,T12,T14,T16,T21,T26,T6,U10,U13,U17,V3,W14,W19,W24,W8
MODE	P26,R26,R23
JTAGSEL_N	D24

4 Package Diagram

4.1 UG676 Package Outline (21mm x 21mm)

Figure 4-1 Package Outline UG676

TOP VIEW

BOTTOM VIEW

DETAIL A

SIDE VIEW

DETAIL A(2:1)

DETAIL B(2:1)

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.33	1.41	1.49
A1	0.30	0.35	0.40
A2	0.98	1.06	1.14
A3	0.70 BASIC		
c	0.32	0.36	0.40
D	20.90	21.00	21.10
D1	20.00 BASIC		
E	20.90	21.00	21.10
E1	20.000 BASIC		
e	0.800 BASIC		
L	0.275 BASIC		
b	0.40	0.45	0.50
aaa	0.15		
ccc	0.17		
ddd	0.15		
eee	0.15		
fff	0.08		