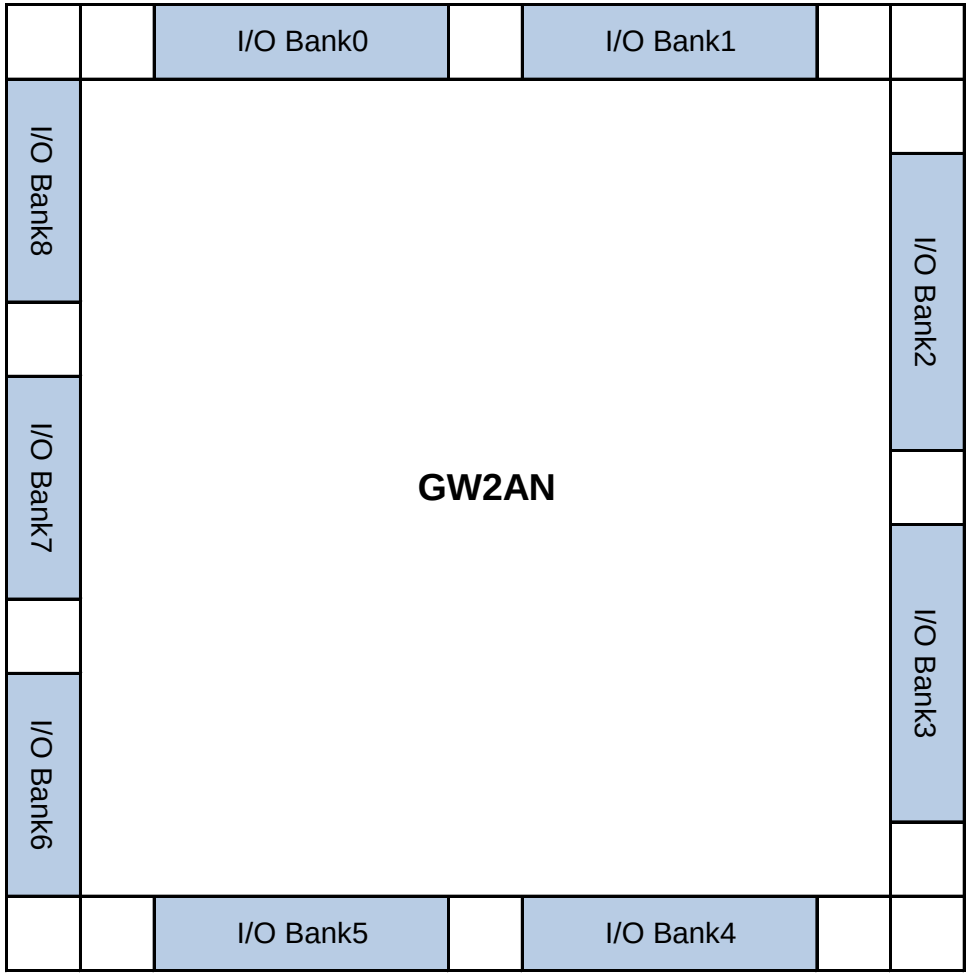
Date	Version	Description
07/21/2021	1.0E	Initial version published. UG400, UG484 packages supported.
08/12/2021	1.1E	Power info modified; The description of mode pin improved.
10/29/2021	1.2E	UG256, PG256, UG324 packages added; Pin definitions updated.
08/19/2022	1.2.1E	The Min. voltage of VCCX in Power updated.
10/20/2022	1.2.2E	The note in Power sheet updated; The note in Pin Definitions sheet updated; The description of MODE0 and MODE1 pins in Pin Definitions sheet updated.
11/11/2022	1.2.3E	Power info. updated; The description of pin CLKHOLD_N in Pin Definitions sheet updated.
05/04/2023	1.2.4E	The direction of pin MO in Pin Definitions sheet updated.

Pin Name	I/O	Description
User I/O		
IO [End][Row/Column Number][A/B]	I/O/LVDS	[End] indicates the pin location, including L(left), R(right), B(bottom), and T(top).
		[Row/Column Number] indicates the pin row/column number. If [End] is T(top) or B(bottom), the pin indicates the column number of the corresponding CFU. If [End] is L(left) or R(right), the pin indicates the row number of the corresponding CFU.
		[A/B] indicates differential signal pair information.
		LVDS indicates that the pin only supports LVDS output.
Multi-Function Pins		
IO [End][Row/Column Number][A/B]/MMM		/MMM represents one or more of the other functions in addition to being general purpose user I/O. When these functions are not in use, these pins can be used as user I/O.
D0	I/O	Data port D0 in CPU mode
D1	I/O	Data port D1 in CPU mode
D2	I/O	Data port D2 in CPU mode
D3	I/O	Data port D3 in CPU mode
D4	I/O	Data port D4 in CPU mode
D5	I/O	Data port D5 in CPU mode
D6	I/O	Data port D6 in CPU mode
D7	I/O	Data port D7 in CPU mode
WE_N	I	Select data input/output of D[7:0] in CPU mode.0: Write;1: Read.
DOUT	O	Data output in SERIAL mode
DIN	I, internal weak pull-down	Data input in SERIAL mode
TMS	I, internal weak pull-up	Serial mode input in JTAG mode
TCK	I	Serial clock input in JTAG mode
TDO	O	Serial data output in JTAG mode
TDI	I, internal weak pull-up	Serial data input in JTAG mode
JTAGSEL_N	I, internal weak pull-up	Reconfigure JTAG download function signal
RECONFIG_N	I, internal weak pull-up	Global reset GowinCONFIG logic signal, active low
FASTRD_N	I	Access SPI FLASH to select signal. Low, Fast Read mode; High, Read mode.
DONE[1]	O	High, the programming configuration has been completed successfully; Low, the programming configuration has not been completed or failed.
	I	When the DONE signal is low, delay the chip to activate. Activate the chip until the DONE signal is high.

Pin Name	I/O	Description
READY[1]	O	High, the device can be programmed and configured currently; Low, the device cannot be programmed and configured currently.
MI-1	I/O	MI in MSPI mode
MI-2	I/O	WPN in MSPI mode; data lane 2 in QMSPI mode
MI-3	I/O	HOLDN in MSPI mode; data lane 3 in QMSPI mode
MO	O	MO in MSPI mode
MCS_N	O	Enable signal MCS_N in MSPI mode, active-low
MCLK	O	Clock output MCLK in MSPI mode, with default frequency of 2.5Mhz
SCLK	I	Clock input in SSPI, SERIAL, and CPU modes
SO	I/O	SO in SSPI mode
SI	I/O	SI in SSPI mode
SSPI_CS_N	I/O	Enable signal SSPI_CS_N in SSPI mode, active-low, and internal weak pull-up
QSSPI_WPN	I	WPN in QSSPI mode; data lane 2 in QSSPI mode
CLKHOLD_N	I, internal weak pull-down	Active-high in SSPI mode; Active-low in CPU mode.
GCLKC_[x]	I	Differential input pin of GCLKT_[x], C(Comp), [x]: global clock No.[2]
GCLKT_[x]	I	Global clock input pin, T(True), [x]: global clock No.
LPLL_C_fb/RPLL_C_fb	I	Left/Right PLL feedback input pin, C(Comp)
LPLL_T_fb/RPLL_T_fb	I	Left/Right PLL feedback input pin, T(True)
LPLL_C_in/RPLL_C_in	I	Left/Right PLL clock input pin, C(Comp)
LPLL_T_in/RPLL_T_in	I	Left/Right PLL clock input pin, T(True)
MODE1	I, internal weak pull-down	Selection signal port in GowinCONFIG mode
MODE0	I, internal weak pull-down	Selection signal port in GowinCONFIG mode
Other Pins		
EXTR	NA	External 10K 1% resistor to ground
VSS	NA	Ground
VCC	NA	Power supply pin of core voltage
VCCIO#	NA	Power supply pin of I/O voltage for I/O BANK#
VCCX	NA	Power supply pin of auxiliary voltage

Note!
[1] The default state of READY/DONE is open-drain output, internal weak pull-up. DONE outputs 0 during configuration.
[2] When the input is single-ended, GCLKC_[x] pin is not a global clock pin.



Note!

[1] Each Bank has independent reference voltage (VREF).

[2] You can select to use IOB internal VREF (equals to 0.5 * VCCIO).

[3] You can also select to use external VREF input (use any IO pins as external VREF input).

Note!
[1] UV Version; The unpackaged MODE[1:0] is internally connected to 01.
[2] LV Version; The unpackaged MODE[1:0] is internally connected to 01.
[3] EV Version; The unpackaged MODE[1:0] is internally connected to 01.

Pin Name	Function	BANK	DQS	Configuration Function	Differential Pair	LVDS	UG484[1]	UG484[2]	UG484[3]	UG400[1]	UG400[2]	UG400[3]	UG256[1]	UG256[2]	UG256[3]	PG256[1]	PG256[2]	PG256[3]	UG324[1]	UG324[2]	UG324[3]
EXTR	Ground	N/A																			
IOB12A	I/O	5	DQ2		True_of_IOB12B	True	AA6	AA6	AA6	T7	T7	T7	T5	T5	T5	T5	T5	T5	N7	N7	N7
IOB12B	I/O	5	DQ2		Comp_of_IOB12A	True	AB6	AB6	AB6	T8	T8	T8	R6	R6	R6	R6	R6	R6	P7	P7	P7
IOB13A	I/O	5	DQ2		True_of_IOB13B	none	W6	W6	W6												
IOB13B	I/O	5	DQ2		Comp_of_IOB13A	none	V7	V7	V7												
IOB14A	I/O	5	DQ2		True_of_IOB14B	True	V8	V8	V8	W5	W5	W5	N6	N6	N6	N6	N6	N6	N8	N8	N8
IOB14B	I/O	5	DQ2		Comp_of_IOB14A	True	U8	U8	U8	Y5	Y5	Y5	L7	L7	L7	L7	L7	L7	R7	R7	R7
IOB15A	I/O	5	DQ2		True_of_IOB15B	none	AA8	AA7	AA7												
IOB15B	I/O	5	DQ2		Comp_of_IOB15A	none	AB8	AB7	AB7												
IOB16A	I/O	5	DQ2		True_of_IOB16B	True	V9	V9	V9	P9	P9	P9	R7	R7	R7	R7	R7	R7	V5	V5	V5
IOB16B	I/O	5	DQ2		Comp_of_IOB16A	True	W8	W8	W8	R9	R9	R9	P7	P7	P7	P7	P7	P7	V6	V6	V6
IOB17A	I/O	5	DQ2		True_of_IOB17B	none	AA7	AA8	AA8										T7	T7	T7
IOB17B	I/O	5	DQ2		Comp_of_IOB17A	none	AB7	AB8	AB8										P8	P8	P8
IOB18A	I/O	5	DQ2		True_of_IOB18B	True	Y8	Y8	Y8	W7	W7	W7	M7	M7	M7	M7	M7	M7	V7	V7	V7
IOB18B	I/O	5	DQ2		Comp_of_IOB18A	True	W9	W9	W9	Y7	Y7	Y7	N7	N7	N7	N7	N7	N7	U8	U8	U8
IOB19A	I/O	5	DQ2		True_of_IOB19B	none	AA9	AA9	AA9	V8	V8	V8							U7	U7	U7
IOB19B	I/O	5	DQ2		Comp_of_IOB19A	none	AB9	AB9	AB9	U9	U9	U9							R8	R8	R8
IOB20A	I/O	5	DQ2		True_of_IOB20B	True	T10	T10	T10	V9	V9	V9	M6	M6	M6	M6	M6	M6	R9	R9	R9
IOB20B	I/O	5	DQ2		Comp_of_IOB20A	True	U10	U10	U10	T9	T9	T9	L8	L8	L8	L8	L8	L8	P9	P9	P9
IOB21A	I/O	5	DQS2		True_of_IOB21B	none	Y9	Y9	Y9	W8	W8	W8									
IOB21B	I/O	5	DQS2		Comp_of_IOB21A	none	Y10	Y10	Y10	Y8	Y8	Y8									
IOB22A	I/O	5	DQ2		True_of_IOB22B	True	V10	V10	V10	P10	P10	P10	P8	P8	P8	P8	P8	P8			
IOB22B	I/O	5	DQ2		Comp_of_IOB22A	True	W10	W10	W10	R10	R10	R10	T8	T8	T8	T8	T8	T8			
IOB23A/GCLKT_5	I/O	5	DQ2	GCLKT_5	True_of_IOB23B	none	AA10	AA10	AA10	W9	W9	W9	T7	T7	T7	T7	T7	T7	T8	T8	T8
IOB23B/GCLKC_5	I/O	5	DQ2	GCLKC_5	Comp_of_IOB23A	none	AB10	AB10	AB10	Y9	Y9	Y9	R8	R8	R8	R8	R8	R8	T9	T9	T9
IOB24A	I/O	5	DQ2		True_of_IOB24B	True	T11	T11	T11	Y10	Y10	Y10	N8	N8	N8	N8	N8	N8			
IOB24B	I/O	5	DQ2		Comp_of_IOB24A	True	U11	U11	U11	W10	W10	W10	L9	L9	L9	L9	L9	L9			
IOB25A	I/O	5	DQ2		True_of_IOB25B	none	AA11	AA11	AA11	U10	U10	U10							V8	V8	V8
IOB25B	I/O	5	DQ2		Comp_of_IOB25A	none	AB11	AB11	AB11	V10	V10	V10							U9	U9	U9
IOB26A	I/O	5	DQ2		True_of_IOB26B	True	V11	V11	V11	U11	U11	U11	M8	M8	M8	M8	M8	M8	N9	N9	N9
IOB26B	I/O	5	DQ2		Comp_of_IOB26A	True	Y11	Y11	Y11	T10	T10	T10	N9	N9	N9	N9	N9	N9	N10	N10	N10
IOB27A	I/O	5	DQ2		True_of_IOB27B	none	U12	U12	U12	Y11	Y11	Y11							V9	V9	V9
IOB27B	I/O	5	DQ2		Comp_of_IOB27A	none	V12	V12	V12	W11	W11	W11							U10	U10	U10
IOB2A	I/O	5	DQ1		True_of_IOB2B	True	AA2	AA2	AA2	W1	W1	W1	P4	P4	P4	P4	P4	P4	V2	V2	V2
IOB2B	I/O	5	DQ1		Comp_of_IOB2A	True	AB2	AB2	AB2	Y1	Y1	Y1	T4	T4	T4	T4	T4	T4	U3	U3	U3
IOB30A/GCLKT_4	I/O	4	DQ3	GCLKT_4	True_of_IOB30B	True	AB12	AB12	AB12	Y12	Y12	Y12	T9	T9	T9	T9	T9	T9	V10	V10	V10
IOB30B/GCLKC_4	I/O	4	DQ3	GCLKC_4	Comp_of_IOB30A	True	AA12	AA12	AA12	W12	W12	W12	P9	P9	P9	P9	P9	P9	U11	U11	U11
IOB31A	I/O	4	DQ3		True_of_IOB31B	none	Y12	Y12	Y12										T10	T10	T10
IOB31B	I/O	4	DQ3		Comp_of_IOB31A	none	T12	T12	T12										R10	R10	R10
IOB32A	I/O	4	DQ3		True_of_IOB32B	True	V13	V13	V13	P11	P11	P11	R9	R9	R9	R9	R9	R9			
IOB32B	I/O	4	DQ3		Comp_of_IOB32A	True	U13	U13	U13	R11	R11	R11	T10	T10	T10	T10	T10	T10			
IOB33A	I/O	4	DQ3		True_of_IOB33B	none	AB13	AB13	AB13	Y13	Y13	Y13							P10	P10	P10
IOB33B	I/O	4	DQ3		Comp_of_IOB33A	none	AA13	AA13	AA13	W13	W13	W13							T11	T11	T11
IOB34A	I/O	4	DQ3		True_of_IOB34B	True	Y13	Y13	Y13	V12	V12	V12	M9	M9	M9	M9	M9	M9	V11	V11	V11
IOB34B	I/O	4	DQ3		Comp_of_IOB34A	True	W13	W13	W13	V13	V13	V13	L10	L10	L10	L10	L10	L10	V12	V12	V12
IOB35A	I/O	4	DQ3		True_of_IOB35B	none	U14	U14	U14	U12	U12	U12							N11	N11	N11
IOB35B	I/O	4	DQ3		Comp_of_IOB35A	none	V14	V14	V14	T11	T11	T11							R11	R11	R11
IOB36A	I/O	4	DQ3		True_of_IOB36B	True	T13	T13	T13	Y14	Y14	Y14	P10	P10	P10	P10	P10	P10			
IOB36B	I/O	4	DQ3		Comp_of_IOB36A	True	T14	T14	T14	W14	W14	W14	R10	R10	R10	R10	R10	R10			
IOB37A	I/O	4	DQS3		True_of_IOB37B	none	AB14	AB14	AB14										U12	U12	U12
IOB37B	I/O	4	DQS3		Comp_of_IOB37A	none	AA14	AA14	AA14										V13	V13	V13
IOB38A	I/O	4	DQ3		True_of_IOB38B	True	Y14	Y14	Y14	Y15	Y15	Y15	N10	N10	N10	N10	N10	N10	P11	P11	P11
IOB38B	I/O	4	DQ3		Comp_of_IOB38A	True	W14	W14	W14	W15	W15	W15	M11	M11	M11	M11	M11	M11	T12	T12	T12
IOB39A	I/O	4	DQ3		True_of_IOB39B	none	AB15	AB15	AB15	P12	P12	P12							U13	U13	U13
IOB39B	I/O	4	DQ3		Comp_of_IOB39A	none	AA15	AA15	AA15	R12	R12	R12							V14	V14	V14
IOB3A	I/O	5	DQ1		True_of_IOB3B	none	V6	V6	V6	R6	R6	R6							R4	R4	R4
IOB3B	I/O	5	DQ1		Comp_of_IOB3A	none	U6	U6	U6	T6	T6	T6							P6	P6	P6

Note!
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[2] LV Version; The unpackaged MODE[1:0] is internally connected to 01.
[3] EV Version; The unpackaged MODE[1:0] is internally connected to 01.

Pin Name	Function	BANK	DQS	Configuration Function	Differential Pair	LVDS	UG484[1]	UG484[2]	UG484[3]	UG400[1]	UG400[2]	UG400[3]	UG256[1]	UG256[2]	UG256[3]	PG256[1]	PG256[2]	PG256[3]	UG324[1]	UG324[2]	UG324[3]
IOB40A	I/O	4	DQ3		True_of_IOB40B	True	Y15	Y15	Y15	Y16	Y16	Y16	T11	T11	T11	T11	T11	T11			
IOB40B	I/O	4	DQ3		Comp_of_IOB40A	True	W15	W15	W15	W16	W16	W16	P11	P11	P11	P11	P11	P11			
IOB41A	I/O	4	DQ3		True_of_IOB41B	none	AB16	AB16	AB16	T12	T12	T12							R12	R12	R12
IOB41B	I/O	4	DQ3		Comp_of_IOB41A	none	AA16	AA16	AA16	T13	T13	T13							T13	T13	T13
IOB42A	I/O	4	DQ3		True_of_IOB42B	True	V15	V15	V15	Y17	Y17	Y17	M10	M10	M10	M10	M10	M10	U14	U14	U14
IOB42B	I/O	4	DQ3		Comp_of_IOB42A	True	U15	U15	U15	W17	W17	W17	N11	N11	N11	N11	N11	N11	V15	V15	V15
IOB43A	I/O	4	DQ3		True_of_IOB43B	none	AB17	AB17	AB17										T14	T14	T14
IOB43B	I/O	4	DQ3		Comp_of_IOB43A	none	AA17	AA17	AA17										N12	N12	N12
IOB44A	I/O	4	DQ3		True_of_IOB44B	True	Y17	Y17	Y17	P13	P13	P13	R13	R13	R13	R13	R13	R13			
IOB44B	I/O	4	DQ3		Comp_of_IOB44A	True	V16	V16	V16	R13	R13	R13	T14	T14	T14	T14	T14	T14			
IOB45A	I/O	4	DQ3		True_of_IOB45B	none	Y18	Y18	Y18	V15	V15	V15							U15	U15	U15
IOB45B	I/O	4	DQ3		Comp_of_IOB45A	none	W17	W17	W17	V16	V16	V16							V16	V16	V16
IOB48A	I/O	4	DQS4		True_of_IOB48B	True	AB18	AB18	AB18	V14	V14	V14	R11	R11	R11	R11	R11	R11	P12	P12	P12
IOB48B	I/O	4	DQS4		Comp_of_IOB48A	True	AA18	AA18	AA18	U14	U14	U14	T12	T12	T12	T12	T12	T12	R14	R14	R14
IOB49A	I/O	4	DQ4		True_of_IOB49B	none	AB19	AB19	AB19	Y18	Y18	Y18							T15	T15	T15
IOB49B	I/O	4	DQ4		Comp_of_IOB49A	none	AA19	AA19	AA19	W18	W18	W18							T16	T16	T16
IOB4A	I/O	5	DQ1		True_of_IOB4B	True	AA3	AA3	AA3	W2	W2	W2	T2	T2	T2	T2	T2	T2	T3	T3	T3
IOB4B	I/O	5	DQ1		Comp_of_IOB4A	True	AB3	AB3	AB3	Y2	Y2	Y2	R3	R3	R3	R3	R3	R3	U4	U4	U4
IOB50A/SCLK	I/O	4	DQ4	SCLK	True_of_IOB50B	True	T9	T9	T9	W6	W6	W6	P6	P6	P6	P6	P6	P6	T6	T6	T6
IOB50B/D1/SO	I/O	4	DQ4	D1/SO	Comp_of_IOB50A	True	U9	U9	U9	Y6	Y6	Y6	T6	T6	T6	T6	T6	T6	U6	U6	U6
IOB51A/DIN/CLKHOLD_N	I/O	4	DQ4	DIN/CLKHOLD_N	True_of_IOB51B	none	T15	T15	T15	T14	T14	T14									
IOB51B/DOUT/WE_N	I/O	4	DQ4	DOUT/WE_N	Comp_of_IOB51A	none	U16	U16	U16	U15	U15	U15									
IOB52A/FASTRD_N/D3	I/O	4	DQ4	FASTRD_N/D3	True_of_IOB52B	True	AB20	AB20	AB20	Y19	Y19	Y19	P12	P12	P12	P12	P12	P12			
IOB52B/QSSPI_WPN	I/O	4	DQ4	QSSPI_WPN	Comp_of_IOB52A	True	AA20	AA20	AA20	W19	W19	W19	T13	T13	T13	T13	T13	T13			
IOB53A/D7	I/O	4	DQ4	D7	True_of_IOB53B	none	Y19	Y19	Y19	P14	P14	P14							R13	R13	R13
IOB53B/D6	I/O	4	DQ4	D6	Comp_of_IOB53A	none	W18	W18	W18	R14	R14	R14							R15	R15	R15
IOB54A/SSPI_CS_N/D0	I/O	4	DQ4	SSPI_CS_N/D0	True_of_IOB54B	True	AB21	AB21	AB21	Y20	Y20	Y20	R12	R12	R12	R12	R12	R12	U16	U16	U16
IOB54B/SI/D2	I/O	4	DQ4	SI/D2	Comp_of_IOB54A	True	AA21	AA21	AA21	W20	W20	W20	P13	P13	P13	P13	P13	P13	V17	V17	V17
IOB55A/D5	I/O	4	DQ4	D5	True_of_IOB55B	none	V17	V17	V17	T16	T16	T16	T15	T15	T15	T15	T15	T15	P13	P13	P13
IOB55B/D4	I/O	4	DQ4	D4	Comp_of_IOB55A	none	T16	T16	T16	R15	R15	R15	R14	R14	R14	R14	R14	R14	P14	P14	P14
IOB5A	I/O	5	DQ1		True_of_IOB5B	none	Y4	Y4	Y4	P7	P7	P7							P5	P5	P5
IOB5B	I/O	5	DQ1		Comp_of_IOB5A	none	W5	W5	W5	R7	R7	R7							R6	R6	R6
IOB6A	I/O	5	DQ1		True_of_IOB6B	True	U7	U7	U7	V6	V6	V6	R5	R5	R5	R5	R5	R5			
IOB6B	I/O	5	DQ1		Comp_of_IOB6A	True	T8	T8	T8	U6	U6	U6	P5	P5	P5	P5	P5	P5			
IOB7A	I/O	5	DQ1		True_of_IOB7B	none	AA4	AA4	AA4	W3	W3	W3							V3	V3	V3
IOB7B	I/O	5	DQ1		Comp_of_IOB7A	none	AB4	AB4	AB4	Y3	Y3	Y3							V4	V4	V4
IOB8A	I/O	5	DQ1		True_of_IOB8B	True	AA5	AA5	AA5	W4	W4	W4	T3	T3	T3	T3	T3	T3	R5	R5	R5
IOB8B	I/O	5	DQ1		Comp_of_IOB8A	True	AB5	AB5	AB5	Y4	Y4	Y4	R4	R4	R4	R4	R4	R4	T4	T4	T4
IOB9A	I/O	5	DQS1		True_of_IOB9B	none	Y5	Y5	Y5	P8	P8	P8							T5	T5	T5
IOB9B	I/O	5	DQS1		Comp_of_IOB9A	none	Y6	Y6	Y6	R8	R8	R8							U5	U5	U5
IOL11A	I/O	8	none		True_of_IOL11B	True	E1	E1	E1	H6	H6	H6							E2	E2	E2
IOL11B	I/O	8	none		Comp_of_IOL11A	True	F1	F1	F1	H7	H7	H7							E1	E1	E1
IOL12A	I/O	8	none		True_of_IOL12B	none	G3	G3	G3												
IOL12B	I/O	8	none		Comp_of_IOL12A	none	G4	G4	G4												
IOL13A	I/O	8	none		True_of_IOL13B	True	H4	H4	H4	F2	F2	F2							F2	F2	F2
IOL13B	I/O	8	none		Comp_of_IOL13A	True	H3	H3	H3	F1	F1	F1							H5	H5	H5
IOL14A/GCLKT_8	I/O	8	none	GCLKT_8	True_of_IOL14B	none	G2	G2	G2	E2	E2	E2	E1	E1	E1	E1	E1	E1	G4	G4	G4
IOL14B/GCLKC_8	I/O	8	none	GCLKC_8	Comp_of_IOL14A	none	G1	G1	G1	E1	E1	E1	F2	F2	F2	F2	F2	F2	G3	G3	G3
IOL15A	I/O	8	none		True_of_IOL15B	True	H2	H2	H2	G4	G4	G4	F4	F4	F4	F4	F4	F4	F1	F1	F1
IOL15B	I/O	8	none		Comp_of_IOL15A	True	H1	H1	H1	G3	G3	G3	G6	G6	G6	G6	G6	G6	G6	G6	G6
IOL16A	I/O	8	none		True_of_IOL16B	none	J7	J7	J7	H3	H3	H3	F3	F3	F3	F3	F3	F3			

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Pin Name	Function	BANK	DQS	Configuration Function	Differential Pair	LVDS	UG484[1]	UG484[2]	UG484[3]	UG400[1]	UG400[2]	UG400[3]	UG256[1]	UG256[2]	UG256[3]	PG256[1]	PG256[2]	PG256[3]	UG324[1]	UG324[2]	UG324[3]
IOL16B	I/O	8	none		Comp_of_IOL16A	none	J6	J6	J6	H4	H4	H4	F1	F1	F1	F1	F1	F1			
IOL17A	I/O	8	none		True_of_IOL17B	True	H5	H5	H5	G2	G2	G2	G5	G5	G5	G5	G5	G5	G2	G2	G2
IOL17B	I/O	8	none		Comp_of_IOL17A	True	J5	J5	J5	G1	G1	G1	G4	G4	G4	G4	G4	G4	G1	G1	G1
IOL18A	I/O	8	none		True_of_IOL18B	none	J4	J4	J4	J6	J6	J6							H3	H3	H3
IOL18B	I/O	8	none		Comp_of_IOL18A	none	J3	J3	J3	J5	J5	J5							H4	H4	H4
IOL19A	I/O	8	none		True_of_IOL19B	True	J2	J2	J2	H2	H2	H2	G2	G2	G2	G2	G2	G2	H2	H2	H2
IOL19B	I/O	8	none		Comp_of_IOL19A	True	J1	J1	J1	H1	H1	H1	G3	G3	G3	G3	G3	G3	H1	H1	H1
IOL20A	I/O	8	none		True_of_IOL20B	none	K7	K7	K7	J4	J4	J4	F5	F5	F5	F5	F5	F5	H6	H6	H6
IOL20B	I/O	8	none		Comp_of_IOL20A	none	K6	K6	K6	J3	J3	J3	H6	H6	H6	H6	H6	H6	J1	J1	J1
IOL21A	I/O	7	none		True_of_IOL21B	True	L7	L7	L7	J2	J2	J2	G1	G1	G1	G1	G1	G1	J2	J2	J2
IOL21B	I/O	7	none		Comp_of_IOL21A	True	K5	K5	K5	J1	J1	J1	H2	H2	H2	H2	H2	H2	J5	J5	J5
IOL22A	I/O	7	none		True_of_IOL22B	none	K4	K4	K4	K5	K5	K5	H4	H4	H4	H4	H4	H4	J3	J3	J3
IOL22B	I/O	7	none		Comp_of_IOL22A	none	K3	K3	K3	K4	K4	K4	J6	J6	J6	J6	J6	J6	J7	J7	J7
IOL23A	I/O	7	none		True_of_IOL23B	True	K2	K2	K2	K2	K2	K2									
IOL23B	I/O	7	none		Comp_of_IOL23A	True	K1	K1	K1	K1	K1	K1									
IOL24A	I/O	7	none		True_of_IOL24B	none	L6	L6	L6	K6	K6	K6	H3	H3	H3	H3	H3	H3	J4	J4	J4
IOL24B	I/O	7	none		Comp_of_IOL24A	none	L5	L5	L5	K7	K7	K7	H1	H1	H1	H1	H1	H1	K3	K3	K3
IOL25A/GCLKT_7	I/O	7	none	GCLKT_7	True_of_IOL25B	True	L1	L1	L1	L1	L1	L1	J1	J1	J1	J1	J1	J1	K2	K2	K2
IOL25B/GCLKC_7	I/O	7	none	GCLKC_7	Comp_of_IOL25A	True	M2	M2	M2	L2	L2	L2	J3	J3	J3	J3	J3	J3	J6	J6	J6
IOL26A	I/O	7	none		True_of_IOL26B	none	L3	L3	L3	L3	L3	L3									
IOL26B	I/O	7	none		Comp_of_IOL26A	none	L4	L4	L4	L4	L4	L4									
IOL27A/MO	I/O	9	none	MO	True_of_IOL27B	none															
IOL27B/MI-1	I/O	9	none	MI-1	Comp_of_IOL27A	none															
IOL27C/MI-2	I/O	9	none	MI-2	True_of_IOL27D	none															
IOL27D/MI-3	I/O	9	none	MI-3	Comp_of_IOL27C	none															
IOL27E/MCLK	I/O	9	none	MCLK	True_of_IOL27F	none															
IOL27F/MCS_N	I/O	9	none	MCS_N	Comp_of_IOL27E	none															
IOL28A	I/O	7	none		True_of_IOL28B	True	M1	M1	M1	M1	M1	M1	J2	J2	J2	J2	J2	J2	K1	K1	K1
IOL28B	I/O	7	none		Comp_of_IOL28A	True	N1	N1	N1	M2	M2	M2	K1	K1	K1	K1	K1	K1	L1	L1	L1
IOL29A	I/O	7	none		True_of_IOL29B	none	M6	M6	M6	M3	M3	M3							K7	K7	K7
IOL29B	I/O	7	none		Comp_of_IOL29A	none	M5	M5	M5	M4	M4	M4							K5	K5	K5
IOL2A	I/O	8	DQ0		True_of_IOL2B	True	D3	D3	D3	C4	C4	C4	B1	B1	B1	B1	B1	B1	B1	B1	B1
IOL2B	I/O	8	DQ0		Comp_of_IOL2A	True	D4	D4	D4	C3	C3	C3	C2	C2	C2	C2	C2	C2	C2	C2	C2
IOL30A	I/O	7	none		True_of_IOL30B	True	N2	N2	N2	L5	L5	L5	H5	H5	H5	H5	H5	H5			
IOL30B	I/O	7	none		Comp_of_IOL30A	True	P1	P1	P1	M5	M5	M5	J4	J4	J4	J4	J4	J4			
IOL31A	I/O	7	none		True_of_IOL31B	none	N3	N3	N3	L6	L6	L6									
IOL31B	I/O	7	none		Comp_of_IOL31A	none	N4	N4	N4	L7	L7	L7									
IOL32A	I/O	7	none		True_of_IOL32B	True	P2	P2	P2	N1	N1	N1	K3	K3	K3	K3	K3	K3	K4	K4	K4
IOL32B	I/O	7	none		Comp_of_IOL32A	True	R1	R1	R1	N2	N2	N2	K2	K2	K2	K2	K2	K2	L2	L2	L2
IOL33A	I/O	7	none		True_of_IOL33B	none	P3	P3	P3	P1	P1	P1	J5	J5	J5	J5	J5	J5	K6	K6	K6
IOL33B	I/O	7	none		Comp_of_IOL33A	none	M7	M7	M7	P2	P2	P2	K6	K6	K6	K6	K6	K6	L3	L3	L3
IOL34A	I/O	6	none		True_of_IOL34B	True	P4	P4	P4	N3	N3	N3							L4	L4	L4
IOL34B	I/O	6	none		Comp_of_IOL34A	True	N5	N5	N5	N4	N4	N4							M2	M2	M2
IOL35A	I/O	6	none		True_of_IOL35B	none	N6	N6	N6										M1	M1	M1
IOL35B	I/O	6	none		Comp_of_IOL35A	none	N7	N7	N7										L6	L6	L6
IOL36A	I/O	6	none		True_of_IOL36B	True	R2	R2	R2	M6	M6	M6	L1	L1	L1	L1	L1	L1			
IOL36B	I/O	6	none		Comp_of_IOL36A	True	T1	T1	T1	M7	M7	M7	L3	L3	L3	L3	L3	L3			
IOL37A	I/O	6	none		True_of_IOL37B	none	P5	P5	P5										N1	N1	N1
IOL37B	I/O	6	none		Comp_of_IOL37A	none	P6	P6	P6										N2	N2	N2
IOL38A	I/O	6	none		True_of_IOL38B	True	R3	R3	R3	P3	P3	P3							M3	M3	M3
IOL38B	I/O	6	none		Comp_of_IOL38A	True	R4	R4	R4	P4	P4	P4							L5	L5	L5
IOL39A	I/O	6	none		True_of_IOL39B	none	R5	R5	R5												
IOL39B	I/O	6	none		Comp_of_IOL39A	none	P7	P7	P7												
IOL3A	I/O	8	DQ0		True_of_IOL3B	none	F6	F6	F6	F6	F6	F6									
IOL3B	I/O	8	DQ0		Comp_of_IOL3A	none	G7	G7	G7	G6	G6	G6									
IOL40A	I/O	6	none		True_of_IOL40B	True	T2	T2	T2	R1	R1	R1	K4	K4	K4	K4	K4	K4	M5	M5	M5
IOL40B	I/O	6	none		Comp_of_IOL40A	True	U1	U1	U1	R2	R2	R2	L5	L5	L5	L5	L5	L5	N3	N3	N3

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Pin Name	Function	BANK	DQS	Configuration Function	Differential Pair	LVDS	UG484[1]	UG484[2]	UG484[3]	UG400[1]	UG400[2]	UG400[3]	UG256[1]	UG256[2]	UG256[3]	PG256[1]	PG256[2]	PG256[3]	UG324[1]	UG324[2]	UG324[3]
IOL41A	I/O	6	none		True_of_IOL41B	none	R6	R6	R6										R1	R1	R1
IOL41B	I/O	6	none		Comp_of_IOL41A	none	R7	R7	R7										P3	P3	P3
IOL42A	I/O	6	none		True_of_IOL42B	True	T3	T3	T3	T1	T1	T1									
IOL42B	I/O	6	none		Comp_of_IOL42A	True	T4	T4	T4	T2	T2	T2									
IOL43A	I/O	6	none		True_of_IOL43B	none	T5	T5	T5	N5	N5	N5							P2	P2	P2
IOL43B	I/O	6	none		Comp_of_IOL43A	none	T6	T6	T6	N6	N6	N6							M6	M6	M6
IOL44A/GCLKT_6	I/O	6	none	GCLKT_6	True_of_IOL44B	True	U2	U2	U2	U1	U1	U1	L2	L2	L2	L2	L2	L2	P1	P1	P1
IOL44B/GCLKC_6	I/O	6	none	GCLKC_6	Comp_of_IOL44A	True	V1	V1	V1	U2	U2	U2	M1	M1	M1	M1	M1	M1	M4	M4	M4
IOL45A	I/O	6	none		True_of_IOL45B	none	U3	U3	U3	R3	R3	R3									
IOL45B	I/O	6	none		Comp_of_IOL45A	none	U4	U4	U4	R4	R4	R4									
IOL46A	I/O	6	none		True_of_IOL46B	True	W1	W1	W1	T3	T3	T3	K5	K5	K5	K5	K5	K5	N4	N4	N4
IOL46B	I/O	6	none		Comp_of_IOL46A	True	W2	W2	W2	T4	T4	T4	L4	L4	L4	L4	L4	L4	T1	T1	T1
IOL47A	I/O	6	none		True_of_IOL47B	none	V4	V4	V4	V1	V1	V1	N2	N2	N2	N2	N2	N2	R2	R2	R2
IOL47B	I/O	6	none		Comp_of_IOL47A	none	U5	U5	U5	V2	V2	V2	P1	P1	P1	P1	P1	P1	U1	U1	U1
IOL48A	I/O	6	none		True_of_IOL48B	True	Y1	Y1	Y1	V3	V3	V3	M3	M3	M3	M3	M3	M3			
IOL48B	I/O	6	none		Comp_of_IOL48A	True	AA1	AA1	AA1	V4	V4	V4	N1	N1	N1	N1	N1	N1			
IOL49A	I/O	6	none		True_of_IOL49B	none	W3	W3	W3	P5	P5	P5							T2	T2	T2
IOL49B	I/O	6	none		Comp_of_IOL49A	none	Y2	Y2	Y2	P6	P6	P6							N5	N5	N5
IOL4A/LPLL1_T_fb	I/O	8	DQ0	LPLL1_T_fb	True_of_IOL4B	True	E4	E4	E4	C2	C2	C2	D3	D3	D3	D3	D3	D3	E4	E4	E4
IOL4B/LPLL1_C_fb	I/O	8	DQ0	LPLL1_C_fb	Comp_of_IOL4A	True	F5	F5	F5	C1	C1	C1	D1	D1	D1	D1	D1	D1	F4	F4	F4
IOL50A	I/O	6	none		True_of_IOL50B	True	Y3	Y3	Y3	T5	T5	T5	M2	M2	M2	M2	M2	M2	P4	P4	P4
IOL50B	I/O	6	none		Comp_of_IOL50A	True	W4	W4	W4	R5	R5	R5	N3	N3	N3	N3	N3	N3	R3	R3	R3
IOL51A	I/O	6	none		True_of_IOL51B	none	V5	V5	V5	U4	U4	U4	R1	R1	R1	R1	R1	R1			
IOL51B	I/O	6	none		Comp_of_IOL51A	none	T7	T7	T7	U5	U5	U5	P2	P2	P2	P2	P2	P2			
IOL5A/LPLL1_T_in	I/O	8	DQ0	LPLL1_T_in	True_of_IOL5B	none	C1	C1	C1	D2	D2	D2	E2	E2	E2	E2	E2	E2	D2	D2	D2
IOL5B/LPLL1_C_in	I/O	8	DQ0	LPLL1_C_in	Comp_of_IOL5A	none	D2	D2	D2	D1	D1	D1	E3	E3	E3	E3	E3	E3	G5	G5	G5
IOL6A	I/O	8	DQS0		True_of_IOL6B	True	G6	G6	G6	E4	E4	E4							D3	D3	D3
IOL6B	I/O	8	DQS0		Comp_of_IOL6A	True	H7	H7	H7	E3	E3	E3							C1	C1	C1
IOL7A	I/O	8	DQ0		True_of_IOL7B	none	G5	G5	G5	F5	F5	F5									
IOL7B	I/O	8	DQ0		Comp_of_IOL7A	none	H6	H6	H6	G5	G5	G5									
IOL8A	I/O	8	DQ0		True_of_IOL8B	True	D1	D1	D1				C1	C1	C1	C1	C1	C1	E3	E3	E3
IOL8B	I/O	8	DQ0		Comp_of_IOL8A	True	E2	E2	E2				D2	D2	D2	D2	D2	D2	F5	F5	F5
IOL9A	I/O	8	DQ0		True_of_IOL9B	none	E3	E3	E3	F4	F4	F4							F3	F3	F3
IOL9B	I/O	8	DQ0		Comp_of_IOL9A	none	F4	F4	F4	F3	F3	F3							D1	D1	D1
IOR11A	I/O	2	none		True_of_IOR11B	True	G21	G21	G21	G16	G16	G16	E16	E16	E16	E16	E16	E16			
IOR11B	I/O	2	none		Comp_of_IOR11A	True	G20	G20	G20	F18	F18	F18	F15	F15	F15	F15	F15	F15			
IOR12A	I/O	2	none		True_of_IOR12B	none	G19	G19	G19	G17	G17	G17							E17	E17	E17
IOR12B	I/O	2	none		Comp_of_IOR12A	none	G18	G18	G18	E20	E20	E20							D18	D18	D18
IOR13A	I/O	2	none		True_of_IOR13B	True	H22	H22	H22	F19	F19	F19	F13	F13	F13	F13	F13	F13	G16	G16	G16
IOR13B	I/O	2	none		Comp_of_IOR13A	True	H21	H21	H21	F20	F20	F20	G12	G12	G12	G12	G12	G12	H15	H15	H15
IOR14A	I/O	2	none		True_of_IOR14B	none	G17	G17	G17										H14	H14	H14
IOR14B	I/O	2	none		Comp_of_IOR14A	none	H20	H20	H20										F17	F17	F17
IOR15A	I/O	2	none		True_of_IOR15B	True	H19	H19	H19	J14	J14	J14	F14	F14	F14	F14	F14	F14	E18	E18	E18
IOR15B	I/O	2	none		Comp_of_IOR15A	True	H18	H18	H18	J15	J15	J15	F16	F16	F16	F16	F16	F16	G17	G17	G17
IOR16A	I/O	2	none		True_of_IOR16B	none	H17	H17	H17	G19	G19	G19									
IOR16B	I/O	2	none		Comp_of_IOR16A	none	H16	H16	H16	H17	H17	H17									
IOR17A	I/O	2	none		True_of_IOR17B	True	J18	J18	J18	H18	H18	H18	F12	F12	F12	F12	F12	F12	H16	H16	H16
IOR17B	I/O	2	none		Comp_of_IOR17A	True	J19	J19	J19	H19	H19	H19	G13	G13	G13	G13	G13	G13	F18	F18	F18
IOR18A	I/O	2	none		True_of_IOR18B	none	J16	J16	J16	H16	H16	H16							J15	J15	J15
IOR18B	I/O	2	none		Comp_of_IOR18A	none	J17	J17	J17	G20	G20	G20							H17	H17	H17
IOR19A	I/O	2	none		True_of_IOR19B	True	J21	J21	J21	J17	J17	J17	G15	G15	G15	G15	G15	G15			
IOR19B	I/O	2	none		Comp_of_IOR19A	True	J22	J22	J22	H20	H20	H20	G14	G14	G14	G14	G14	G14			
IOR20A	I/O	2	none		True_of_IOR20B	none	J20	J20	J20	J18	J18	J18							J13	J13	J13
IOR20B	I/O	2	none		Comp_of_IOR20A	none	K20	K20	K20	J16	J16	J16							G18	G18	G18
IOR21A	I/O	2	none		True_of_IOR21B	True	K19	K19	K19	K14	K14	K14	G11	G11	G11	G11	G11	G11	J16	J16	J16
IOR21B	I/O	2	none		Comp_of_IOR21A	True	K18	K18	K18	K15	K15	K15	H12	H12	H12	H12	H12	H12	J17	J17	J17
IOR22A	I/O	2	none		True_of_IOR22B	none	K17	K17	K17												

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Pin Name	Function	BANK	DQS	Configuration Function	Differential Pair	LVDS	UG484[1]	UG484[2]	UG484[3]	UG400[1]	UG400[2]	UG400[3]	UG256[1]	UG256[2]	UG256[3]	PG256[1]	PG256[2]	PG256[3]	UG324[1]	UG324[2]	UG324[3]
IOR22B	I/O	2	none		Comp_of_IOR22A	none	K16	K16	K16												
IOR23A	I/O	2	none		True_of_IOR23B	True	L17	L17	L17	J19	J19	J19	G16	G16	G16	G16	G16	G16			
IOR23B	I/O	2	none		Comp_of_IOR23A	True	L16	L16	L16	J20	J20	J20	H15	H15	H15	H15	H15	H15			
IOR24A	I/O	2	none		True_of_IOR24B	none	L19	L19	L19										J14	J14	J14
IOR24B	I/O	2	none		Comp_of_IOR24A	none	L20	L20	L20										J12	J12	J12
IOR25A	I/O	2	none		True_of_IOR25B	True	K22	K22	K22	K17	K17	K17	H13	H13	H13	H13	H13	H13			
IOR25B	I/O	2	none		Comp_of_IOR25A	True	L21	L21	L21	K18	K18	K18	J12	J12	J12	J12	J12	J12			
IOR26A	I/O	2	none		True_of_IOR26B	none	L22	L22	L22												
IOR26B	I/O	2	none		Comp_of_IOR26A	none	M17	M17	M17												
IOR28A/GCLKT_3	I/O	3	none	GCLKT_3	True_of_IOR28B	True	M22	M22	M22	K19	K19	K19	H14	H14	H14	H14	H14	H14	H18	H18	H18
IOR28B/GCLKC_3	I/O	3	none	GCLKC_3	Comp_of_IOR28A	True	M21	M21	M21	K20	K20	K20	H16	H16	H16	H16	H16	H16	K15	K15	K15
IOR29A	I/O	3	none		True_of_IOR29B	none	M20	M20	M20	K16	K16	K16	J16	J16	J16	J16	J16	J16	K16	K16	K16
IOR29B	I/O	3	none		Comp_of_IOR29A	none	M19	M19	M19	L17	L17	L17	J14	J14	J14	J14	J14	J14	K17	K17	K17
IOR2A/RPLL1_T_fb	I/O	2	DQ5	RPLL1_T_fb	True_of_IOR2B	True	C21	C21	C21	D17	D17	D17	D14	D14	D14	D14	D14	D14	B18	B18	B18
IOR2B/RPLL1_C_fb	I/O	2	DQ5	RPLL1_C_fb	Comp_of_IOR2A	True	C22	C22	C22	C18	C18	C18	E15	E15	E15	E15	E15	E15	C17	C17	C17
IOR30A	I/O	3	none		True_of_IOR30B	True	M16	M16	M16	L19	L19	L19	J15	J15	J15	J15	J15	J15	K12	K12	K12
IOR30B	I/O	3	none		Comp_of_IOR30A	True	N16	N16	N16	L20	L20	L20	K16	K16	K16	K16	K16	K16	K13	K13	K13
IOR31A	I/O	3	none		True_of_IOR31B	none	N17	N17	N17	L14	L14	L14	H11	H11	H11	H11	H11	H11			
IOR31B	I/O	3	none		Comp_of_IOR31A	none	N18	N18	N18	L15	L15	L15	J13	J13	J13	J13	J13	J13			
IOR32A	I/O	3	none		True_of_IOR32B	True	N22	N22	N22	M20	M20	M20	K14	K14	K14	K14	K14	K14	K18	K18	K18
IOR32B	I/O	3	none		Comp_of_IOR32A	True	P21	P21	P21	M19	M19	M19	K15	K15	K15	K15	K15	K15	L16	L16	L16
IOR33A	I/O	3	none		True_of_IOR33B	none	N20	N20	N20	L16	L16	L16							L15	L15	L15
IOR33B	I/O	3	none		Comp_of_IOR33A	none	N19	N19	N19	M18	M18	M18							L13	L13	L13
IOR34A	I/O	3	none		True_of_IOR34B	True	R22	R22	R22	M17	M17	M17	J11	J11	J11	J11	J11	J11			
IOR34B	I/O	3	none		Comp_of_IOR34A	True	R21	R21	R21	N20	N20	N20	L12	L12	L12	L12	L12	L12			
IOR35A	I/O	3	none		True_of_IOR35B	none	P22	P22	P22										L17	L17	L17
IOR35B	I/O	3	none		Comp_of_IOR35A	none	P20	P20	P20										M16	M16	M16
IOR36A	I/O	3	none		True_of_IOR36B	True	T22	T22	T22	M16	M16	M16	L16	L16	L16	L16	L16	L16	L18	L18	L18
IOR36B	I/O	3	none		Comp_of_IOR36A	True	T21	T21	T21	N19	N19	N19	L14	L14	L14	L14	L14	L14	M18	M18	M18
IOR37A	I/O	3	none		True_of_IOR37B	none	P19	P19	P19										M17	M17	M17
IOR37B	I/O	3	none		Comp_of_IOR37A	none	P18	P18	P18										N18	N18	N18
IOR38A	I/O	3	none		True_of_IOR38B	True	P17	P17	P17	N18	N18	N18	K13	K13	K13	K13	K13	K13	L14	L14	L14
IOR38B	I/O	3	none		Comp_of_IOR38A	True	P16	P16	P16	N17	N17	N17	K12	K12	K12	K12	K12	K12	N17	N17	N17
IOR39A	I/O	3	none		True_of_IOR39B	none	U22	U22	U22	P20	P20	P20									
IOR39B	I/O	3	none		Comp_of_IOR39A	none	U21	U21	U21	P19	P19	P19									
IOR3A	I/O	2	DQ5		True_of_IOR3B	none	F17	F17	F17	F15	F15	F15							F14	F14	F14
IOR3B	I/O	2	DQ5		Comp_of_IOR3A	none	G16	G16	G16	G15	G15	G15							D16	D16	D16
IOR40A	I/O	3	none		True_of_IOR40B	True	V22	V22	V22	P18	P18	P18	L15	L15	L15	L15	L15	L15	K14	K14	K14
IOR40B	I/O	3	none		Comp_of_IOR40A	True	W22	W22	W22	R20	R20	R20	M16	M16	M16	M16	M16	M16	J18	J18	J18
IOR41A	I/O	3	none		True_of_IOR41B	none	R20	R20	R20	M15	M15	M15							M15	M15	M15
IOR41B	I/O	3	none		Comp_of_IOR41A	none	R19	R19	R19	M14	M14	M14							P18	P18	P18
IOR42A	I/O	3	none		True_of_IOR42B	True	R18	R18	R18	N16	N16	N16	K11	K11	K11	K11	K11	K11	M14	M14	M14
IOR42B	I/O	3	none		Comp_of_IOR42A	True	R17	R17	R17	R19	R19	R19	L13	L13	L13	L13	L13	L13	N16	N16	N16
IOR43A	I/O	3	none		True_of_IOR43B	none	R16	R16	R16	T20	T20	T20							P17	P17	P17
IOR43B	I/O	3	none		Comp_of_IOR43A	none	T20	T20	T20	T19	T19	T19							N15	N15	N15
IOR44A	I/O	3	none		True_of_IOR44B	True	T19	T19	T19	U20	U20	U20	M14	M14	M14	M14	M14	M14			
IOR44B	I/O	3	none		Comp_of_IOR44A	True	T18	T18	T18	P17	P17	P17	M15	M15	M15	M15	M15	M15			
IOR45A	I/O	3	none		True_of_IOR45B	none	T17	T17	T17	T18	T18	T18							R18	R18	R18
IOR45B	I/O	3	none		Comp_of_IOR45A	none	U20	U20	U20	U19	U19	U19							M13	M13	M13
IOR46A	I/O	3	none		True_of_IOR46B	True	Y22	Y22	Y22	V20	V20	V20	N15	N15	N15	N15	N15	N15	P16	P16	P16
IOR46B	I/O	3	none		Comp_of_IOR46A	True	W21	W21	W21	P16	P16	P16	P16	P16	P16	P16	P16	P16	T18	T18	T18
IOR47A	I/O	3	none		True_of_IOR47B	none	U19	U19	U19	N15	N15	N15							R17	R17	R17
IOR47B	I/O	3	none		Comp_of_IOR47A	none	U18	U18	U18	N14	N14	N14							N14	N14	N14
IOR48A	I/O	3	none		True_of_IOR48B	True	AA22	AA22	AA22	R17	R17	R17	N16	N16	N16	N16	N16	N16			
IOR48B	I/O	3	none		Comp_of_IOR48A	True	Y21	Y21	Y21	U18	U18	U18	N14	N14	N14	N14	N14	N14			
IOR49A	I/O	3	none		True_of_IOR49B	none	U17	U17	U17	P15	P15	P15							P15	P15	P15
IOR49B	I/O	3	none		Comp_of_IOR49A	none	V19	V19	V19	R16	R16	R16							U18	U18	U18

Note!
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Pin Name	Function	BANK	DQS	Configuration Function	Differential Pair	LVDS	UG484[1]	UG484[2]	UG484[3]	UG400[1]	UG400[2]	UG400[3]	UG256[1]	UG256[2]	UG256[3]	PG256[1]	PG256[2]	PG256[3]	UG324[1]	UG324[2]	UG324[3]
IOR4A/RPLL1_T_in	I/O	2	DQ5	RPLL1_T_in	True_of_IOR4B	True	D22	D22	D22	C19	C19	C19	D16	D16	D16	D16	D16	D16	E15	E15	E15
IOR4B/RPLL1_C_in	I/O	2	DQ5	RPLL1_C_in	Comp_of_IOR4A	True	D21	D21	D21	E17	E17	E17	E14	E14	E14	E14	E14	E14	C18	C18	C18
IOR50A	I/O	3	none		True_of_IOR50B	True	V18	V18	V18	V19	V19	V19	P15	P15	P15	P15	P15	P15	R16	R16	R16
IOR50B	I/O	3	none		Comp_of_IOR50A	True	W20	W20	W20	T17	T17	T17	R16	R16	R16	R16	R16	R16	T17	T17	T17
IOR51A	I/O	3	none		True_of_IOR51B	none	W19	W19	W19	U17	U17	U17									
IOR51B	I/O	3	none		Comp_of_IOR51A	none	Y20	Y20	Y20	V17	V17	V17									
IOR5A	I/O	2	DQ5		True_of_IOR5B	none	D19	D19	D19	F16	F16	F16							G13	G13	G13
IOR5B	I/O	2	DQ5		Comp_of_IOR5A	none	D20	D20	D20	D18	D18	D18							G14	G14	G14
IOR6A	I/O	2	DQS5		True_of_IOR6B	True	E22	E22	E22	B20	B20	B20	C15	C15	C15	C15	C15	C15			
IOR6B	I/O	2	DQS5		Comp_of_IOR6A	True	E21	E21	E21	C20	C20	C20	B16	B16	B16	B16	B16	B16			
IOR7A	I/O	2	DQ5		True_of_IOR7B	none	E19	E19	E19	H14	H14	H14							F15	F15	F15
IOR7B	I/O	2	DQ5		Comp_of_IOR7A	none	E20	E20	E20	H15	H15	H15							D17	D17	D17
IOR8A	I/O	2	DQ5		True_of_IOR8B	True	F22	F22	F22	D19	D19	D19	C16	C16	C16	C16	C16	C16	E16	E16	E16
IOR8B	I/O	2	DQ5		Comp_of_IOR8A	True	G22	G22	G22	F17	F17	F17	D15	D15	D15	D15	D15	D15	H13	H13	H13
IOR9A	I/O	2	DQ5		True_of_IOR9B	none	F18	F18	F18	D20	D20	D20							G15	G15	G15
IOR9B	I/O	2	DQ5		Comp_of_IOR9A	none	F19	F19	F19	E19	E19	E19							F16	F16	F16
IOT12A	I/O	0	DQ8		True_of_IOT12B	True	B5	B5	B5	B4	B4	B4	A3	A3	A3	A3	A3	A3	A4	A4	A4
IOT12B	I/O	0	DQ8		Comp_of_IOT12A	True	A6	A6	A6	A4	A4	A4	B4	B4	B4	B4	B4	B4	A5	A5	A5
IOT13A	I/O	0	DQ8		True_of_IOT13B	none	D6	D6	D6	C6	C6	C6									
IOT13B	I/O	0	DQ8		Comp_of_IOT13A	none	E7	E7	E7	D7	D7	D7									
IOT14A	I/O	0	DQ8		True_of_IOT14B	True	B6	B6	B6	B5	B5	B5	D6	D6	D6	D6	D6	D6	B6	B6	B6
IOT14B	I/O	0	DQ8		Comp_of_IOT14A	True	A7	A7	A7	A5	A5	A5	E7	E7	E7	E7	E7	E7	A6	A6	A6
IOT15A	I/O	0	DQ8		True_of_IOT15B	none	C6	C6	C6	G8	G8	G8									
IOT15B	I/O	0	DQ8		Comp_of_IOT15A	none	D7	D7	D7	F8	F8	F8									
IOT16A	I/O	0	DQ8		True_of_IOT16B	True	C8	C8	C8	B6	B6	B6							D8	D8	D8
IOT16B	I/O	0	DQ8		Comp_of_IOT16A	True	D8	D8	D8	A6	A6	A6							E7	E7	E7
IOT17A/TDO	I/O	0	DQ8	TDO	True_of_IOT17B	none	E8	E8	E8	E8	E8	E8	C6	C6	C6	C6	C6	C6	D7	D7	D7
IOT17B/TDI	I/O	0	DQ8	TDI	Comp_of_IOT17A	none	E9	E9	E9	C7	C7	C7	A6	A6	A6	A6	A6	A6	C6	C6	C6
IOT18A	I/O	0	DQ8		True_of_IOT18B	True	B8	B8	B8	B7	B7	B7	B7	B7	B7	B7	B7	B7	A7	A7	A7
IOT18B	I/O	0	DQ8		Comp_of_IOT18A	True	A8	A8	A8	A7	A7	A7	C7	C7	C7	C7	C7	C7	B7	B7	B7
IOT19A	I/O	0	DQ8		True_of_IOT19B	none	C9	C9	C9	G9	G9	G9							E8	E8	E8
IOT19B	I/O	0	DQ8		Comp_of_IOT19A	none	D9	D9	D9	F9	F9	F9							F8	F8	F8
IOT20A	I/O	0	DQ8		True_of_IOT20B	True	B9	B9	B9	B8	B8	B8	E6	E6	E6	E6	E6	E6	B8	B8	B8
IOT20B	I/O	0	DQ8		Comp_of_IOT20A	True	A9	A9	A9	A8	A8	A8	D7	D7	D7	D7	D7	D7	A8	A8	A8
IOT21A	I/O	0	DQS8		True_of_IOT21B	none	F9	F9	F9	D8	D8	D8							C9	C9	C9
IOT21B	I/O	0	DQS8		Comp_of_IOT21A	none	G9	G9	G9	C8	C8	C8							D9	D9	D9
IOT22A	I/O	0	DQ8		True_of_IOT22B	True	F10	F10	F10	B9	B9	B9	F7	F7	F7	F7	F7	F7			
IOT22B	I/O	0	DQ8		Comp_of_IOT22A	True	E10	E10	E10	A9	A9	A9	E8	E8	E8	E8	E8	E8			
IOT23A/TCK	I/O	0	DQ8	TCK	True_of_IOT23B	none	D10	D10	D10	C9	C9	C9	A7	A7	A7	A7	A7	A7	C7	C7	C7
IOT23B/TMS	I/O	0	DQ8	TMS	Comp_of_IOT23A	none	C10	C10	C10	D9	D9	D9	B8	B8	B8	B8	B8	B8	C8	C8	C8
IOT24A/GCLKT_0	I/O	0	DQ8	GCLKT_0	True_of_IOT24B	True	B10	B10	B10	B10	B10	B10	C8	C8	C8	C8	C8	C8	A9	A9	A9
IOT24B/GCLKC_0	I/O	0	DQ8	GCLKC_0	Comp_of_IOT24A	True	A10	A10	A10	A10	A10	A10	A8	A8	A8	A8	A8	A8	B9	B9	B9
IOT25A	I/O	0	DQ8		True_of_IOT25B	none	G11	G11	G11	G10	G10	G10									
IOT25B	I/O	0	DQ8		Comp_of_IOT25A	none	F11	F11	F11	F10	F10	F10									
IOT26A	I/O	0	DQ8		True_of_IOT26B	True	B11	B11	B11	B11	B11	B11	D8	D8	D8	D8	D8	D8	A10	A10	A10
IOT26B	I/O	0	DQ8		Comp_of_IOT26A	True	A11	A11	A11	A11	A11	A11	E9	E9	E9	E9	E9	E9	B10	B10	B10
IOT27A	I/O	0	DQ8		True_of_IOT27B	none	E11	E11	E11	D10	D10	D10									
IOT27B	I/O	0	DQ8		Comp_of_IOT27A	none	D11	D11	D11	C10	C10	C10									
IOT2A	I/O	0	DQ9		True_of_IOT2B	True	B1	B1	B1	B1	B1	B1	C4	C4	C4	C4	C4	C4	A2	A2	A2
IOT2B	I/O	0	DQ9		Comp_of_IOT2A	True	A2	A2	A2	A1	A1	A1	B5	B5	B5	B5	B5	B5	B3	B3	B3
IOT30A	I/O	1	DQ7		True_of_IOT30B	True	D12	D12	D12	A12	A12	A12							C10	C10	C10
IOT30B	I/O	1	DQ7		Comp_of_IOT30A	True	E12	E12	E12	B12	B12	B12							B11	B11	B11
IOT31A/SCL/GCLKT_1	I/O	1	DQ7	SCL/GCLKT_1	True_of_IOT31B	none	B12	B12	B12	C11	C11	C11	A9	A9	A9	A9	A9	A9	E9	E9	E9
IOT31B/SDA/GCLKC_1	I/O	1	DQ7	SDA/GCLKC_1	Comp_of_IOT31A	none	A12	A12	A12	D11	D11	D11	C9	C9	C9	C9	C9	C9	D10	D10	D10
IOT32A	I/O	1	DQ7		True_of_IOT32B	True	G12	G12	G12	A13	A13	A13							B12	B12	B12

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Pin Name	Function	BANK	DQS	Configuration Function	Differential Pair	LVDS	UG484[1]	UG484[2]	UG484[3]	UG400[1]	UG400[2]	UG400[3]	UG256[1]	UG256[2]	UG256[3]	PG256[1]	PG256[2]	PG256[3]	UG324[1]	UG324[2]	UG324[3]
IOT32B	I/O	1	DQ7		Comp_of_IOT32A	True	F12	F12	F12	B13	B13	B13							C11	C11	C11
IOT33A	I/O	1	DQ7		True_of_IOT33B	none	E13	E13	E13												
IOT33B	I/O	1	DQ7		Comp_of_IOT33A	none	F13	F13	F13												
IOT34A	I/O	1	DQ7		True_of_IOT34B	True	A13	A13	A13	G11	G11	G11	F8	F8	F8	F8	F8	F8	A11	A11	A11
IOT34B	I/O	1	DQ7		Comp_of_IOT34A	True	B13	B13	B13	F11	F11	F11	D9	D9	D9	D9	D9	D9	A12	A12	A12
IOT35A	I/O	1	DQ7		True_of_IOT35B	none	C13	C13	C13												
IOT35B	I/O	1	DQ7		Comp_of_IOT35A	none	D13	D13	D13												
IOT36A	I/O	1	DQ7		True_of_IOT36B	True	A14	A14	A14	D12	D12	D12	B9	B9	B9	B9	B9	B9	F9	F9	F9
IOT36B	I/O	1	DQ7		Comp_of_IOT36A	True	B14	B14	B14	C12	C12	C12	A10	A10	A10	A10	A10	A10	F10	F10	F10
IOT37A	I/O	1	DQS7		True_of_IOT37B	none	C14	C14	C14												
IOT37B	I/O	1	DQS7		Comp_of_IOT37A	none	D14	D14	D14												
IOT38A	I/O	1	DQ7		True_of_IOT38B	True	G14	G14	G14	A14	A14	A14	F9	F9	F9	F9	F9	F9	C12	C12	C12
IOT38B	I/O	1	DQ7		Comp_of_IOT38A	True	F14	F14	F14	B14	B14	B14	E11	E11	E11	E11	E11	E11	B13	B13	B13
IOT39A/JTAGSEL_N	I/O	1	DQ7	JTAGSEL_N	True_of_IOT39B	none	E14	E14	E14	C13	C13	C13	C10	C10	C10	C10	C10	C10	D11	D11	D11
IOT39B/RECONFIG_N	I/O	1	DQ7	RECONFIG_N	Comp_of_IOT39A	none	E15	E15	E15	D13	D13	D13	B10	B10	B10	B10	B10	B10	D12	D12	D12
IOT3A	I/O	0	DQ9		True_of_IOT3B	none	E6	E6	E6										D4	D4	D4
IOT3B	I/O	0	DQ9		Comp_of_IOT3A	none	F7	F7	F7										E5	E5	E5
IOT40A	I/O	1	DQ7		True_of_IOT40B	True	A15	A15	A15	A15	A15	A15	D10	D10	D10	D10	D10	D10	A13	A13	A13
IOT40B	I/O	1	DQ7		Comp_of_IOT40A	True	B15	B15	B15	B15	B15	B15	E10	E10	E10	E10	E10	E10	A14	A14	A14
IOT41A	I/O	1	DQ7		True_of_IOT41B	none	C15	C15	C15										E10	E10	E10
IOT41B	I/O	1	DQ7		Comp_of_IOT41A	none	D15	D15	D15										E11	E11	E11
IOT42A	I/O	1	DQ7		True_of_IOT42B	True	A16	A16	A16	A16	A16	A16	A11	A11	A11	A11	A11	A11	B14	B14	B14
IOT42B	I/O	1	DQ7		Comp_of_IOT42A	True	B17	B17	B17	B16	B16	B16	C11	C11	C11	C11	C11	C11	B15	B15	B15
IOT43A	I/O	1	DQ7		True_of_IOT43B	none	C17	C17	C17	G12	G12	G12									
IOT43B	I/O	1	DQ7		Comp_of_IOT43A	none	D16	D16	D16	F12	F12	F12									
IOT44A	I/O	1	DQ7		True_of_IOT44B	True	A17	A17	A17	A17	A17	A17	F10	F10	F10	F10	F10	F10	F11	F11	F11
IOT44B	I/O	1	DQ7		Comp_of_IOT44A	True	B18	B18	B18	B17	B17	B17	D11	D11	D11	D11	D11	D11	C13	C13	C13
IOT45A	I/O	1	DQ7		True_of_IOT45B	none	E16	E16	E16	C14	C14	C14									
IOT45B	I/O	1	DQ7		Comp_of_IOT45A	none	D17	D17	D17	D14	D14	D14									
IOT48A	I/O	1	DQS6		True_of_IOT48B	True	A18	A18	A18	C15	C15	C15	B11	B11	B11	B11	B11	B11	C14	C14	C14
IOT48B	I/O	1	DQS6		Comp_of_IOT48A	True	B19	B19	B19	C16	C16	C16	A12	A12	A12	A12	A12	A12	C15	C15	C15
IOT49A	I/O	1	DQ6		True_of_IOT49B	none	C18	C18	C18	G13	G13	G13							E12	E12	E12
IOT49B	I/O	1	DQ6		Comp_of_IOT49A	none	D18	D18	D18	F13	F13	F13							F12	F12	F12
IOT4A	I/O	0	DQ9		True_of_IOT4B	True	B2	B2	B2	G7	G7	G7	B3	B3	B3	B3	B3	B3	C3	C3	C3
IOT4B	I/O	0	DQ9		Comp_of_IOT4A	True	A3	A3	A3	F7	F7	F7	A2	A2	A2	A2	A2	A2	C4	C4	C4
IOT50A	I/O	1	DQ6		True_of_IOT50B	True	A19	A19	A19	A18	A18	A18	B13	B13	B13	B13	B13	B13	A15	A15	A15
IOT50B	I/O	1	DQ6		Comp_of_IOT50A	True	B20	B20	B20	B18	B18	B18	A14	A14	A14	A14	A14	A14	A16	A16	A16
IOT51A	I/O	1	DQ6		True_of_IOT51B	none	F15	F15	F15	E14	E14	E14									
IOT51B	I/O	1	DQ6		Comp_of_IOT51A	none	G15	G15	G15	D15	D15	D15									
IOT52A	I/O	1	DQ6		True_of_IOT52B	True	A20	A20	A20	E15	E15	E15	C12	C12	C12	C12	C12	C12	B16	B16	B16
IOT52B	I/O	1	DQ6		Comp_of_IOT52A	True	B21	B21	B21	D16	D16	D16	B12	B12	B12	B12	B12	B12	A17	A17	A17
IOT53A	I/O	1	DQ6		True_of_IOT53B	none	C19	C19	C19	G14	G14	G14							D13	D13	D13
IOT53B	I/O	1	DQ6		Comp_of_IOT53A	none	C20	C20	C20	F14	F14	F14							E13	E13	E13
IOT54A	I/O	1	DQ6		True_of_IOT54B	True	A21	A21	A21	B19	B19	B19	B14	B14	B14	B14	B14	B14	D14	D14	D14
IOT54B	I/O	1	DQ6		Comp_of_IOT54A	True	B22	B22	B22	A20	A20	A20	A15	A15	A15	A15	A15	A15	D15	D15	D15
IOT55A/READY	I/O	1	DQ6	READY	True_of_IOT55B	none	F16	F16	F16	C17	C17	C17	A13	A13	A13	A13	A13	A13	C16	C16	C16
IOT55B/DONE	I/O	1	DQ6	DONE	Comp_of_IOT55A	none	E17	E17	E17	A19	A19	A19	C13	C13	C13	C13	C13	C13	E14	E14	E14
IOT5A	I/O	0	DQ9		True_of_IOT5B	none	C3	C3	C3	E6	E6	E6							F7	F7	F7
IOT5B	I/O	0	DQ9		Comp_of_IOT5A	none	C4	C4	C4	D5	D5	D5							E6	E6	E6
IOT6A	I/O	0	DQ9		True_of_IOT6B	True	B3	B3	B3	B2	B2	B2	A4	A4	A4	A4	A4	A4	D5	D5	D5
IOT6B	I/O	0	DQ9		Comp_of_IOT6A	True	A4	A4	A4	A2	A2	A2	C5	C5	C5	C5	C5	C5	B5	B5	B5
IOT7A	I/O	0	DQ9		True_of_IOT7B	none	F8	F8	F8												
IOT7B	I/O	0	DQ9		Comp_of_IOT7A	none	G8	G8	G8												
IOT8A	I/O	0	DQ9		True_of_IOT8B	True	B4	B4	B4	B3	B3	B3	A5	A5	A5	A5	A5	A5	A3	A3	A3

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Pin Name	Function	BANK	DQS	Configuration Function	Differential Pair	LVDS	UG484[1]	UG484[2]	UG484[3]	UG400[1]	UG400[2]	UG400[3]	UG256[1]	UG256[2]	UG256[3]	PG256[1]	PG256[2]	PG256[3]	UG324[1]	UG324[2]	UG324[3]
IOT8B	I/O	0	DQ9		Comp_of_IOT8A	True	A5	A5	A5	A3	A3	A3	B6	B6	B6	B6	B6	B6	B4	B4	B4
IOT9A	I/O	0	DQS9		True_of_IOT9B	none	D5	D5	D5	D6	D6	D6							C5	C5	C5
IOT9B	I/O	0	DQS9		Comp_of_IOT9A	none	C5	C5	C5	E7	E7	E7							D6	D6	D6
VCC	Power	N/A						K10	K10		L9	L9		T16	T16		T16	T16		L10	L10
VCC	Power	N/A						K11	K11		J9	J9		G7	G7		G7	G7		H10	H10
VCC	Power	N/A						K12	K12		H12	H12		A16	A16		A16	A16		H8	H8
VCC	Power	N/A						K13	K13		L12	L12		K10	K10		K10	K10		L11	L11
VCC	Power	N/A						L11	L11		J10	J10		K7	K7		K7	K7		H11	H11
VCC	Power	N/A						L12	L12		M10	M10		T1	T1		T1	T1		M12	M12
VCC	Power	N/A						M11	M11		J11	J11		G10	G10		G10	G10		L8	L8
VCC	Power	N/A						M12	M12		M12	M12		A1	A1		A1	A1		L9	L9
VCC	Power	N/A						N10	N10		K12	K12								H9	H9
VCC	Power	N/A						N11	N11		H13	H13								G12	G12
VCC	Power	N/A						N12	N12												
VCC	Power	N/A						N13	N13												
VCC/VCCX	Power	N/A					K10			L9			T16			T16			L10		
VCC/VCCX	Power	N/A					K11			J9			G7			G7			H10		
VCC/VCCX	Power	N/A					K12			H12			A16			A16			H8		
VCC/VCCX	Power	N/A					K13			L12			K10			K10			L11		
VCC/VCCX	Power	N/A					L11			J10			K7			K7			H11		
VCC/VCCX	Power	N/A					L12			M10			T1			T1			M12		
VCC/VCCX	Power	N/A					M11			J11			G10			G10			L8		
VCC/VCCX	Power	N/A					M12			M12			A1			A1			L9		
VCC/VCCX	Power	N/A					N10			K12									H9		
VCC/VCCX	Power	N/A					N11			H13									G12		
VCC/VCCX	Power	N/A					N12														
VCC/VCCX	Power	N/A					N13														
VCCIO0	Power	N/A					C7			H8			G8			G8			G8		
VCCIO0	Power	N/A					G10			H10			D5			D5			G9		
VCCIO0	Power	N/A					H11			H9											
VCCIO0	Power	N/A					H9														
VCCIO0	Power	N/A																			
VCCIO0	Power	N/A																			
VCCIO0/VCCX	Power	N/A						C7	C7		H8	H8		G8	G8		G8	G8		G8	G8
VCCIO0/VCCX	Power	N/A						G10	G10		H10	H10		D5	D5		D5	D5		G9	G9
VCCIO0/VCCX	Power	N/A						H11	H11		H9	H9									
VCCIO0/VCCX	Power	N/A						H9	H9												
VCCIO0/VCCX	Power	N/A																			
VCCIO0/VCCX	Power	N/A																			
VCCIO1	Power	N/A					C12	C12	C12	H11	H11	H11	D12	D12	D12	D12	D12	D12	G10	G10	G10
VCCIO1	Power	N/A					C16	C16	C16	J12	J12	J12	G9	G9	G9	G9	G9	G9	G11	G11	G11
VCCIO1	Power	N/A					G13	G13	G13												
VCCIO1	Power	N/A					H12	H12	H12												
VCCIO1	Power	N/A					H14	H14	H14												
VCCIO2	Power	N/A					F20	F20	F20	J13	J13	J13	E13	E13	E13	E13	E13	E13	H12	H12	H12
VCCIO2	Power	N/A					J15	J15	J15	K13	K13	K13	H10	H10	H10	H10	H10	H10	J11	J11	J11
VCCIO2	Power	N/A					K15	K15	K15												
VCCIO2	Power	N/A					L15	L15	L15												
VCCIO2	Power	N/A																			
VCCIO3	Power	N/A					M15	M15	M15	L13	L13	L13	M13	M13	M13	M13	M13	M13	K11	K11	K11
VCCIO3	Power	N/A					M18	M18	M18	M13	M13	M13	J10	J10	J10	J10	J10	J10	L12	L12	L12
VCCIO3	Power	N/A					N15	N15	N15	N13	N13	N13									
VCCIO3	Power	N/A					P15	P15	P15												
VCCIO3	Power	N/A					V20	V20	V20												
VCCIO4	Power	N/A					R12	R12	R12	N11	N11	N11	N12	N12	N12	N12	N12	N12	M11	M11	M11
VCCIO4	Power	N/A					R13	R13	R13	N12	N12	N12	K9	K9	K9	K9	K9	K9	M10	M10	M10
VCCIO4	Power	N/A					R14	R14	R14												

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Pin Name	Function	BANK	DQS	Configuration Function	Differential Pair	LVDS	UG484[1]	UG484[2]	UG484[3]	UG400[1]	UG400[2]	UG400[3]	UG256[1]	UG256[2]	UG256[3]	PG256[1]	PG256[2]	PG256[3]	UG324[1]	UG324[2]	UG324[3]
VCCIO4	Power	N/A					W16	W16	W16												
VCCIO4	Power	N/A																			
VCCIO5	Power	N/A					R10	R10	R10	N9	N9	N9	N5	N5	N5	N5	N5	N5	M8	M8	M8
VCCIO5	Power	N/A					R11	R11	R11	N10	N10	N10	K8	K8	K8	K8	K8	K8	M9	M9	M9
VCCIO5	Power	N/A					R9	R9	R9	N8	N8	N8									
VCCIO5	Power	N/A					W11	W11	W11												
VCCIO5	Power	N/A					W7	W7	W7												
VCCIO6	Power	N/A					N8	N8	N8	M8	M8	M8	M4	M4	M4	M4	M4	M4	L7	L7	L7
VCCIO6	Power	N/A					P8	P8	P8	M9	M9	M9							M7	M7	M7
VCCIO6	Power	N/A					V3	V3	V3												
VCCIO7	Power	N/A					L8	L8	L8	K8	K8	K8	H7	H7	H7	H7	H7	H7	J8	J8	J8
VCCIO7	Power	N/A					M3	M3	M3	K9	K9	K9	J7	J7	J7	J7	J7	J7	K8	K8	K8
VCCIO7	Power	N/A					M8	M8	M8												
VCCIO7	Power	N/A																			
VCCIO8	Power	N/A					F3	F3	F3	J7	J7	J7	E4	E4	E4	E4	E4	E4	G7	G7	G7
VCCIO8	Power	N/A					J8	J8	J8	J8	J8	J8							H7	H7	H7
VCCIO8	Power	N/A					K8	K8	K8												
VSS	Ground	N/A					A1	A1	A1												
VSS	Ground	N/A					A22	A22	A22	C5	C5	C5	M12	M12	M12	M12	M12	M12	A1	A1	A1
VSS	Ground	N/A					AB1	AB1	AB1												
VSS	Ground	N/A					AB22	AB22	AB22	D3	D3	D3	M5	M5	M5	M5	M5	M5	A18	A18	A18
VSS	Ground	N/A					B16	B16	B16	E13	E13	E13	B2	B2	B2	B2	B2	B2	K9	K9	K9
VSS	Ground	N/A					B7	B7	B7												
VSS	Ground	N/A					C11	C11	C11	U8	U8	U8									
VSS	Ground	N/A					C2	C2	C2												
VSS	Ground	N/A					E18	E18	E18	E11	E11	E11	R15	R15	R15	R15	R15	R15	J9	J9	J9
VSS	Ground	N/A					E5	E5	E5												
VSS	Ground	N/A					F2	F2	F2												
VSS	Ground	N/A					F21	F21	F21	D4	D4	D4	N13	N13	N13	N13	N13	N13	B2	B2	B2
VSS	Ground	N/A					H10	H10	H10	V5	V5	V5									
VSS	Ground	N/A					H13	H13	H13	K11	K11	K11	H8	H8	H8	H8	H8	H8			
VSS	Ground	N/A					H15	H15	H15	E18	E18	E18	C3	C3	C3	C3	C3	C3	N6	N6	N6
VSS	Ground	N/A					H8	H8	H8												
VSS	Ground	N/A					J10	J10	J10	V7	V7	V7									
VSS	Ground	N/A					J11	J11	J11	U13	U13	U13									
VSS	Ground	N/A					J12	J12	J12	T15	T15	T15	L11	L11	L11	L11	L11	L11			
VSS	Ground	N/A					J13	J13	J13	L18	L18	L18	H9	H9	H9	H9	H9	H9			
VSS	Ground	N/A					J14	J14	J14	H5	H5	H5	D4	D4	D4	D4	D4	D4	U2	U2	U2
VSS	Ground	N/A					J9	J9	J9												
VSS	Ground	N/A					K14	K14	K14	K3	K3	K3	D13	D13	D13	D13	D13	D13	U17	U17	U17
VSS	Ground	N/A					K21	K21	K21	E5	E5	E5	N4	N4	N4	N4	N4	N4	B17	B17	B17
VSS	Ground	N/A					K9	K9	K9												
VSS	Ground	N/A					L10	L10	L10	V11	V11	V11									
VSS	Ground	N/A					L13	L13	L13	M11	M11	M11	J8	J8	J8	J8	J8	J8			
VSS	Ground	N/A					L14	L14	L14	K10	K10	K10	E5	E5	E5	E5	E5	E5	V1	V1	V1
VSS	Ground	N/A					L18	L18	L18	E12	E12	E12	R2	R2	R2	R2	R2	R2	J10	J10	J10
VSS	Ground	N/A					L2	L2	L2												
VSS	Ground	N/A					L9	L9	L9												
VSS	Ground	N/A					M10	M10	M10	V18	V18	V18									
VSS	Ground	N/A					M13	M13	M13	N7	N7	N7	J9	J9	J9	J9	J9	J9			
VSS	Ground	N/A					M14	M14	M14	L8	L8	L8	E12	E12	E12	E12	E12	E12	V18	V18	V18
VSS	Ground	N/A					M4	M4	M4												
VSS	Ground	N/A					M9	M9	M9												
VSS	Ground	N/A					N14	N14	N14	L10	L10	L10	F6	F6	F6	F6	F6	F6			
VSS	Ground	N/A					N21	N21	N21	E9	E9	E9	P14	P14	P14	P14	P14	P14	F6	F6	F6
VSS	Ground	N/A					N9	N9	N9												
VSS	Ground	N/A					P10	P10	P10												

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Pin Name	Function	BANK	DQS	Configuration Function	Differential Pair	LVDS	UG484[1]	UG484[2]	UG484[3]	UG400[1]	UG400[2]	UG400[3]	UG256[1]	UG256[2]	UG256[3]	PG256[1]	PG256[2]	PG256[3]	UG324[1]	UG324[2]	UG324[3]
VSS	Ground	N/A					P11	P11	P11	U16	U16	U16									
VSS	Ground	N/A					P12	P12	P12	U3	U3	U3									
VSS	Ground	N/A					P13	P13	P13	R18	R18	R18	L6	L6	L6	L6	L6	L6			
VSS	Ground	N/A					P14	P14	P14	L11	L11	L11	F11	F11	F11	F11	F11	F11			
VSS	Ground	N/A					P9	P9	P9												
VSS	Ground	N/A					R15	R15	R15	G18	G18	G18	C14	C14	C14	C14	C14	C14	N13	N13	N13
VSS	Ground	N/A					R8	R8	R8												
VSS	Ground	N/A					V2	V2	V2												
VSS	Ground	N/A					V21	V21	V21	E10	E10	E10	P3	P3	P3	P3	P3	P3	F13	F13	F13
VSS	Ground	N/A					W12	W12	W12	U7	U7	U7									
VSS	Ground	N/A					Y16	Y16	Y16	E16	E16	E16	B15	B15	B15	B15	B15	B15	K10	K10	K10
VSS	Ground	N/A					Y7	Y7	Y7												

Note!
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Pin Name	Function	BANK	DQS	Configuration Function	Differential Pair	LVDS	UG484[1]	UG484[2]	UG484[3]	UG400[1]	UG400[2]	UG400[3]	UG256[1]	UG256[2]	UG256[3]	PG256[1]	PG256[2]	PG256[3]	UG332[1]	UG332[2]	UG332[3]	UG324[1]	UG324[2]	UG324[3]
BANK8 True LVDS Pair																								
IOL11A	I/O	8	none		True_of_IOL11B	True	E1	E1	E1	H6	H6	H6							F2	F2	F2	E2	E2	E2
IOL11B	I/O	8	none		Comp_of_IOL11A	True	F1	F1	F1	H7	H7	H7							F1	F1	F1	E1	E1	E1
IOL13A	I/O	8	none		True_of_IOL13B	True	H4	H4	H4	F2	F2	F2							F5	F5	F5	F2	F2	F2
IOL13B	I/O	8	none		Comp_of_IOL13A	True	H3	H3	H3	F1	F1	F1							G5	G5	G5	H5	H5	H5
IOL15A	I/O	8	none		True_of_IOL15B	True	H2	H2	H2	G4	G4	G4	F4	F4	F4	F4	F4	F4				F1	F1	F1
IOL15B	I/O	8	none		Comp_of_IOL15A	True	H1	H1	H1	G3	G3	G3	G6	G6	G6	G6	G6	G6				G6	G6	G6
IOL17A	I/O	8	none		True_of_IOL17B	True	H5	H5	H5	G2	G2	G2	G5	G5	G5	G5	G5	G5	H2	H2	H2	G2	G2	G2
IOL17B	I/O	8	none		Comp_of_IOL17A	True	J5	J5	J5	G1	G1	G1	G4	G4	G4	G4	G4	G4	H1	H1	H1	G1	G1	G1
IOL19A	I/O	8	none		True_of_IOL19B	True	J2	J2	J2	H2	H2	H2	G2	G2	G2	G2	G2	G2	J3	J3	J3	H2	H2	H2
IOL19B	I/O	8	none		Comp_of_IOL19A	True	J1	J1	J1	H1	H1	H1	G3	G3	G3	G3	G3	G3	J2	J2	J2	H1	H1	H1
IOL2A	I/O	8	DQ0		True_of_IOL2B	True	D3	D3	D3	C4	C4	C4	B1	B1	B1	B1	B1	B1	D2	D2	D2	B1	B1	B1
IOL2B	I/O	8	DQ0		Comp_of_IOL2A	True	D4	D4	D4	C3	C3	C3	C2	C2	C2	C2	C2	C2	D1	D1	D1	C2	C2	C2
IOL4A/LPLL1_T_fb	I/O	8	DQ0	LPLL1_T_fb	True_of_IOL4B	True	E4	E4	E4	C2	C2	C2	D3	D3	D3	D3	D3	D3	E3	E3	E3	E4	E4	E4
IOL4B/LPLL1_C_fb	I/O	8	DQ0	LPLL1_C_fb	Comp_of_IOL4A	True	F5	F5	F5	C1	C1	C1	D1	D1	D1	D1	D1	D1	E2	E2	E2	F4	F4	F4
IOL6A	I/O	8	DQS0		True_of_IOL6B	True	G6	G6	G6	E4	E4	E4										D3	D3	D3
IOL6B	I/O	8	DQS0		Comp_of_IOL6A	True	H7	H7	H7	E3	E3	E3										C1	C1	C1
IOL8A	I/O	8	DQ0		True_of_IOL8B	True	D1	D1	D1				C1	C1	C1	C1	C1	C1	G1	G1	G1	E3	E3	E3
IOL8B	I/O	8	DQ0		Comp_of_IOL8A	True	E2	E2	E2				D2	D2	D2	D2	D2	D2	H3	H3	H3	F5	F5	F5
BANK7 True LVDS Pair																								
IOL21A	I/O	7	none		True_of_IOL21B	True	L7	L7	L7	J2	J2	J2	G1	G1	G1	G1	G1	G1	J1	J1	J1	J2	J2	J2
IOL21B	I/O	7	none		Comp_of_IOL21A	True	K5	K5	K5	J1	J1	J1	H2	H2	H2	H2	H2	H2	K3	K3	K3	J5	J5	J5
IOL23A	I/O	7	none		True_of_IOL23B	True	K2	K2	K2	K2	K2	K2												
IOL23B	I/O	7	none		Comp_of_IOL23A	True	K1	K1	K1	K1	K1	K1												
IOL25A/GCLKT_7	I/O	7	none	GCLKT_7	True_of_IOL25B	True	L1	L1	L1	L1	L1	L1	J1	J1	J1	J1	J1	J1	M1	M1	M1	K2	K2	K2
IOL25B/GCLKC_7	I/O	7	none	GCLKC_7	Comp_of_IOL25A	True	M2	M2	M2	L2	L2	L2	J3	J3	J3	J3	J3	J3	M2	M2	M2	J6	J6	J6
IOL28A	I/O	7	none		True_of_IOL28B	True	M1	M1	M1	M1	M1	M1	J2	J2	J2	J2	J2	J2	M3	M3	M3	K1	K1	K1
IOL28B	I/O	7	none		Comp_of_IOL28A	True	N1	N1	N1	M2	M2	M2	K1	K1	K1	K1	K1	K1	N1	N1	N1	L1	L1	L1
IOL30A	I/O	7	none		True_of_IOL30B	True	N2	N2	N2	L5	L5	L5	H5	H5	H5	H5	H5	H5						
IOL30B	I/O	7	none		Comp_of_IOL30A	True	P1	P1	P1	M5	M5	M5	J4	J4	J4	J4	J4	J4						
IOL32A	I/O	7	none		True_of_IOL32B	True	P2	P2	P2	N1	N1	N1	K3	K3	K3	K3	K3	K3	N2	N2	N2	K4	K4	K4
IOL32B	I/O	7	none		Comp_of_IOL32A	True	R1	R1	R1	N2	N2	N2	K2	K2	K2	K2	K2	K2	N3	N3	N3	L2	L2	L2
BANK6 True LVDS Pair																								
IOL34A	I/O	6	none		True_of_IOL34B	True	P4	P4	P4	N3	N3	N3							P1	P1	P1	L4	L4	L4
IOL34B	I/O	6	none		Comp_of_IOL34A	True	N5	N5	N5	N4	N4	N4							P2	P2	P2	M2	M2	M2
IOL36A	I/O	6	none		True_of_IOL36B	True	R2	R2	R2	M6	M6	M6	L1	L1	L1	L1	L1	L1	M5	M5	M5			
IOL36B	I/O	6	none		Comp_of_IOL36A	True	T1	T1	T1	M7	M7	M7	L3	L3	L3	L3	L3	L3	N4	N4	N4			
IOL38A	I/O	6	none		True_of_IOL38B	True	R3	R3	R3	P3	P3	P3							P3	P3	P3	M3	M3	M3
IOL38B	I/O	6	none		Comp_of_IOL38A	True	R4	R4	R4	P4	P4	P4							R1	R1	R1	L5	L5	L5
IOL40A	I/O	6	none		True_of_IOL40B	True	T2	T2	T2	R1	R1	R1	K4	K4	K4	K4	K4	K4	N5	N5	N5	M5	M5	M5
IOL40B	I/O	6	none		Comp_of_IOL40A	True	U1	U1	U1	R2	R2	R2	L5	L5	L5	L5	L5	L5	P4	P4	P4	N3	N3	N3
IOL42A	I/O	6	none		True_of_IOL42B	True	T3	T3	T3	T1	T1	T1							P5	P5	P5			
IOL42B	I/O	6	none		Comp_of_IOL42A	True	T4	T4	T4	T2	T2	T2							R4	R4	R4			
IOL44A/GCLKT_6	I/O	6	none	GCLKT_6	True_of_IOL44B	True	U2	U2	U2	U1	U1	U1	L2	L2	L2	L2	L2	L2	R2	R2	R2	P1	P1	P1
IOL44B/GCLKC_6	I/O	6	none	GCLKC_6	Comp_of_IOL44A	True	V1	V1	V1	U2	U2	U2	M1	M1	M1	M1	M1	M1	R3	R3	R3	M4	M4	M4
IOL46A	I/O	6	none		True_of_IOL46B	True	W1	W1	W1	T3	T3	T3	K5	K5	K5	K5	K5	K5	R5	R5	R5	N4	N4	N4
IOL46B	I/O	6	none		Comp_of_IOL46A	True	W2	W2	W2	T4	T4	T4	L4	L4	L4	L4	L4	L4	T4	T4	T4	T1	T1	T1
IOL48A	I/O	6	none		True_of_IOL48B	True	Y1	Y1	Y1	V3	V3	V3	M3	M3	M3	M3	M3	M3	T3	T3	T3			
IOL48B	I/O	6	none		Comp_of_IOL48A	True	AA1	AA1	AA1	V4	V4	V4	N1	N1	N1	N1	N1	N1	U1	U1	U1			
IOL50A	I/O	6	none		True_of_IOL50B	True	Y3	Y3	Y3	T5	T5	T5	M2	M2	M2	M2	M2	M2	U2	U2	U2	P4	P4	P4
IOL50B	I/O	6	none		Comp_of_IOL50A	True	W4	W4	W4	R5	R5	R5	N3	N3	N3	N3	N3	N3	U3	U3	U3	R3	R3	R3
BANK5 True LVDS Pair																								
IOB12A	I/O	5	DQ2		True_of_IOB12B	True	AA6	AA6	AA6	T7	T7	T7	T5	T5	T5	T5	T5	T5	U4	U4	U4	N7	N7	N7
IOB12B	I/O	5	DQ2		Comp_of_IOB12A	True	AB6	AB6	AB6	T8	T8	T8	R6	R6	R6	R6	R6	R6	T7	T7	T7	P7	P7	P7
IOB14A	I/O	5	DQ2		True_of_IOB14B	True	V8	V8	V8	W5	W5	W5	N6	N6	N6	N6	N6	N6	U6	U6	U6	N8	N8	N8
IOB14B	I/O	5	DQ2		Comp_of_IOB14A	True	U8	U8	U8	Y5	Y5	Y5	L7	L7	L7	L7	L7	L7	T8	T8	T8	R7	R7	R7
IOB16A	I/O	5	DQ2		True_of_IOB16B	True	V9	V9	V9	P9	P9	P9	R7	R7	R7	R7	R7	R7	Y7	Y7	Y7	V5	V5	V5

Note!
[1] UV version.
[2] LV version.
[3] EV version.

Pin Name	Function	BANK	DQS	Configuration Function	Differential Pair	LVDS	UG484[1]	UG484[2]	UG484[3]	UG400[1]	UG400[2]	UG400[3]	UG256[1]	UG256[2]	UG256[3]	PG256[1]	PG256[2]	PG256[3]	UG332[1]	UG332[2]	UG332[3]	UG324[1]	UG324[2]	UG324[3]
IOB16B	I/O	5	DQ2		Comp_of_IOB16A	True	W8	W8	W8	R9	R9	R9	P7	P7	P7	P7	P7	P7	V8	V8	V8	V6	V6	V6
IOB18A	I/O	5	DQ2		True_of_IOB18B	True	Y8	Y8	Y8	W7	W7	W7	M7	M7	M7	M7	M7	M7	U7	U7	U7	V7	V7	V7
IOB18B	I/O	5	DQ2		Comp_of_IOB18A	True	W9	W9	W9	Y7	Y7	Y7	N7	N7	N7	N7	N7	N7	T9	T9	T9	U8	U8	U8
IOB20A	I/O	5	DQ2		True_of_IOB20B	True	T10	T10	T10	V9	V9	V9	M6	M6	M6	M6	M6	M6	W8	W8	W8	R9	R9	R9
IOB20B	I/O	5	DQ2		Comp_of_IOB20A	True	U10	U10	U10	T9	T9	T9	L8	L8	L8	L8	L8	L8	Y8	Y8	Y8	P9	P9	P9
IOB22A	I/O	5	DQ2		True_of_IOB22B	True	V10	V10	V10	P10	P10	P10	P8	P8	P8	P8	P8	P8						
IOB22B	I/O	5	DQ2		Comp_of_IOB22A	True	W10	W10	W10	R10	R10	R10	T8	T8	T8	T8	T8	T8						
IOB24A	I/O	5	DQ2		True_of_IOB24B	True	T11	T11	T11	Y10	Y10	Y10	N8	N8	N8	N8	N8	N8						
IOB24B	I/O	5	DQ2		Comp_of_IOB24A	True	U11	U11	U11	W10	W10	W10	L9	L9	L9	L9	L9	L9						
IOB26A	I/O	5	DQ2		True_of_IOB26B	True	V11	V11	V11	U11	U11	U11	M8	M8	M8	M8	M8	M8	W10	W10	W10	N9	N9	N9
IOB26B	I/O	5	DQ2		Comp_of_IOB26A	True	Y11	Y11	Y11	T10	T10	T10	N9	N9	N9	N9	N9	N9	Y10	Y10	Y10	N10	N10	N10
IOB2A	I/O	5	DQ1		True_of_IOB2B	True	AA2	AA2	AA2	W1	W1	W1	P4	P4	P4	P4	P4	P4	W4	W4	W4	V2	V2	V2
IOB2B	I/O	5	DQ1		Comp_of_IOB2A	True	AB2	AB2	AB2	Y1	Y1	Y1	T4	T4	T4	T4	T4	T4	Y4	Y4	Y4	U3	U3	U3
IOB4A	I/O	5	DQ1		True_of_IOB4B	True	AA3	AA3	AA3	W2	W2	W2	T2	T2	T2	T2	T2	T2	V5	V5	V5	T3	T3	T3
IOB4B	I/O	5	DQ1		Comp_of_IOB4A	True	AB3	AB3	AB3	Y2	Y2	Y2	R3	R3	R3	R3	R3	R3	W5	W5	W5	U4	U4	U4
IOB6A	I/O	5	DQ1		True_of_IOB6B	True	U7	U7	U7	V6	V6	V6	R5	R5	R5	R5	R5	R5						
IOB6B	I/O	5	DQ1		Comp_of_IOB6A	True	T8	T8	T8	U6	U6	U6	P5	P5	P5	P5	P5	P5						
IOB8A	I/O	5	DQ1		True_of_IOB8B	True	AA5	AA5	AA5	W4	W4	W4	T3	T3	T3	T3	T3	T3	Y5	Y5	Y5	R5	R5	R5
IOB8B	I/O	5	DQ1		Comp_of_IOB8A	True	AB5	AB5	AB5	Y4	Y4	Y4	R4	R4	R4	R4	R4	R4	V6	V6	V6	T4	T4	T4
BANK4 True LVDS Pair																								
IOB30A/GCLKT_4	I/O	4	DQ3	GCLKT_4	True_of_IOB30B	True	AB12	AB12	AB12	Y12	Y12	Y12	T9	T9	T9	T9	T9	T9	Y12	Y12	Y12	V10	V10	V10
IOB30B/GCLKC_4	I/O	4	DQ3	GCLKC_4	Comp_of_IOB30A	True	AA12	AA12	AA12	W12	W12	W12	P9	P9	P9	P9	P9	P9	W12	W12	W12	U11	U11	U11
IOB32A	I/O	4	DQ3		True_of_IOB32B	True	V13	V13	V13	P11	P11	P11	R9	R9	R9	R9	R9	R9	U10	U10	U10			
IOB32B	I/O	4	DQ3		Comp_of_IOB32A	True	U13	U13	U13	R11	R11	R11	T10	T10	T10	T10	T10	T10	U11	U11	U11			
IOB34A	I/O	4	DQ3		True_of_IOB34B	True	Y13	Y13	Y13	V12	V12	V12	M9	M9	M9	M9	M9	M9				V11	V11	V11
IOB34B	I/O	4	DQ3		Comp_of_IOB34A	True	W13	W13	W13	V13	V13	V13	L10	L10	L10	L10	L10	L10				V12	V12	V12
IOB36A	I/O	4	DQ3		True_of_IOB36B	True	T13	T13	T13	Y14	Y14	Y14	P10	P10	P10	P10	P10	P10	T12	T12	T12			
IOB36B	I/O	4	DQ3		Comp_of_IOB36A	True	T14	T14	T14	W14	W14	W14	R10	R10	R10	R10	R10	R10	U13	U13	U13			
IOB38A	I/O	4	DQ3		True_of_IOB38B	True	Y14	Y14	Y14	Y15	Y15	Y15	N10	N10	N10	N10	N10	N10	W13	W13	W13	P11	P11	P11
IOB38B	I/O	4	DQ3		Comp_of_IOB38A	True	W14	W14	W14	W15	W15	W15	M11	M11	M11	M11	M11	M11	Y14	Y14	Y14	T12	T12	T12
IOB40A	I/O	4	DQ3		True_of_IOB40B	True	Y15	Y15	Y15	Y16	Y16	Y16	T11	T11	T11	T11	T11	T11	W14	W14	W14			
IOB40B	I/O	4	DQ3		Comp_of_IOB40A	True	W15	W15	W15	W16	W16	W16	P11	P11	P11	P11	P11	P11	V14	V14	V14			
IOB42A	I/O	4	DQ3		True_of_IOB42B	True	V15	V15	V15	Y17	Y17	Y17	M10	M10	M10	M10	M10	M10	U14	U14	U14	U14	U14	U14
IOB42B	I/O	4	DQ3		Comp_of_IOB42A	True	U15	U15	U15	W17	W17	W17	N11	N11	N11	N11	N11	N11	V15	V15	V15	V15	V15	V15
IOB44A	I/O	4	DQ3		True_of_IOB44B	True	Y17	Y17	Y17	P13	P13	P13	R13	R13	R13	R13	R13	R13	U15	U15	U15			
IOB44B	I/O	4	DQ3		Comp_of_IOB44A	True	V16	V16	V16	R13	R13	R13	T14	T14	T14	T14	T14	T14	T14	T14	T14			
IOB48A	I/O	4	DQS4		True_of_IOB48B	True	AB18	AB18	AB18	V14	V14	V14	R11	R11	R11	R11	R11	R11	Y16	Y16	Y16	P12	P12	P12
IOB48B	I/O	4	DQS4		Comp_of_IOB48A	True	AA18	AA18	AA18	U14	U14	U14	T12	T12	T12	T12	T12	T12	W16	W16	W16	R14	R14	R14
IOB50A/SCLK	I/O	4	DQ4	SCLK	True_of_IOB50B	True	T9	T9	T9	W6	W6	W6	P6	P6	P6	P6	P6	P6	V7	V7	V7	T6	T6	T6
IOB50B/D1/SO	I/O	4	DQ4	D1/SO	Comp_of_IOB50A	True	U9	U9	U9	Y6	Y6	Y6	T6	T6	T6	T6	T6	T6	W7	W7	W7	U6	U6	U6
IOB52A/FASTRD_N/D3	I/O	4	DQ4	FASTRD_N /D3	True_of_IOB52B	True	AB20	AB20	AB20	Y19	Y19	Y19	P12	P12	P12	P12	P12	P12						
IOB52B/QSSPI_WPN	I/O	4	DQ4	QSSPI_WPN	Comp_of_IOB52A	True	AA20	AA20	AA20	W19	W19	W19	T13	T13	T13	T13	T13	T13						
IOB54A/SSPI_CS_N/D0	I/O	4	DQ4	SSPI_CS_N/D0	True_of_IOB54B	True	AB21	AB21	AB21	Y20	Y20	Y20	R12	R12	R12	R12	R12	R12	W17	W17	W17	U16	U16	U16
IOB54B/SI/D2	I/O	4	DQ4	SI/D2	Comp_of_IOB54A	True	AA21	AA21	AA21	W20	W20	W20	P13	P13	P13	P13	P13	P13	V17	V17	V17	V17	V17	V17
BANK3 True LVDS Pair																								
IOR28A/GCLKT_3	I/O	3	none	GCLKT_3	True_of_IOR28B	True	M22	M22	M22	K19	K19	K19	H14	H14	H14	H14	H14	H14	J19	J19	J19	H18	H18	H18
IOR28B/GCLKC_3	I/O	3	none	GCLKC_3	Comp_of_IOR28A	True	M21	M21	M21	K20	K20	K20	H16	H16	H16	H16	H16	H16	J20	J20	J20	K15	K15	K15
IOR30A	I/O	3	none		True_of_IOR30B	True	M16	M16	M16	L19	L19	L19	J15	J15	J15	J15	J15	J15	L20	L20	L20	K12	K12	K12
IOR30B	I/O	3	none		Comp_of_IOR30A	True	N16	N16	N16	L20	L20	L20	K16	K16	K16	K16	K16	K16	L19	L19	L19	K13	K13	K13
IOR32A	I/O	3	none		True_of_IOR32B	True	N22	N22	N22	M20	M20	M20	K14	K14	K14	K14	K14	K14	K18	K18	K18	K18	K18	K18
IOR32B	I/O	3	none		Comp_of_IOR32A	True	P21	P21	P21	M19	M19	M19	K15	K15	K15	K15	K15	K15	K19	K19	K19	L16	L16	L16
IOR34A	I/O	3	none		True_of_IOR34B	True	R22	R22	R22	M17	M17	M17	J11	J11	J11	J11	J11	J11	N20	N20	N20			
IOR34B	I/O	3	none		Comp_of_IOR34A	True	R21	R21	R21	N20	N20	N20	L12	L12	L12	L12	L12	L12	N19	N19	N19			
IOR36A	I/O	3	none		True_of_IOR36B	True	T22	T22	T22	M16	M16	M16	L16	L16	L16	L16	L16	L16	M16	M16	M16	L18	L18	L18

Note!
[1] UV version.
[2] LV version.
[3] EV version.

Pin Name	Function	BANK	DQS	Configuration Function	Differential Pair	LVDS	UG484[1]	UG484[2]	UG484[3]	UG400[1]	UG400[2]	UG400[3]	UG256[1]	UG256[2]	UG256[3]	PG256[1]	PG256[2]	PG256[3]	UG332[1]	UG332[2]	UG332[3]	UG324[1]	UG324[2]	UG324[3]
IOR36B	I/O	3	none		Comp_of_IOR36A	True	T21	T21	T21	N19	N19	N19	L14	L14	L14	L14	L14	L14	P17	P17	P17	M18	M18	M18
IOR38A	I/O	3	none		True_of_IOR38B	True	P17	P17	P17	N18	N18	N18	K13	K13	K13	K13	K13	K13	P19	P19	P19	L14	L14	L14
IOR38B	I/O	3	none		Comp_of_IOR38A	True	P16	P16	P16	N17	N17	N17	K12	K12	K12	K12	K12	K12	P18	P18	P18	N17	N17	N17
IOR40A	I/O	3	none		True_of_IOR40B	True	V22	V22	V22	P18	P18	P18	L15	L15	L15	L15	L15	L15	R20	R20	R20	K14	K14	K14
IOR40B	I/O	3	none		Comp_of_IOR40A	True	W22	W22	W22	R20	R20	R20	M16	M16	M16	M16	M16	M16	R19	R19	R19	J18	J18	J18
IOR42A	I/O	3	none		True_of_IOR42B	True	R18	R18	R18	N16	N16	N16	K11	K11	K11	K11	K11	K11	R18	R18	R18	M14	M14	M14
IOR42B	I/O	3	none		Comp_of_IOR42A	True	R17	R17	R17	R19	R19	R19	L13	L13	L13	L13	L13	L13	T20	T20	T20	N16	N16	N16
IOR44A	I/O	3	none		True_of_IOR44B	True	T19	T19	T19	U20	U20	U20	M14	M14	M14	M14	M14	M14	U17	U17	U17			
IOR44B	I/O	3	none		Comp_of_IOR44A	True	T18	T18	T18	P17	P17	P17	M15	M15	M15	M15	M15	M15	T17	T17	T17			
IOR46A	I/O	3	none		True_of_IOR46B	True	Y22	Y22	Y22	V20	V20	V20	N15	N15	N15	N15	N15	N15	W20	W20	W20	P16	P16	P16
IOR46B	I/O	3	none		Comp_of_IOR46A	True	W21	W21	W21	P16	P16	P16	P16	P16	P16	P16	P16	P16	V19	V19	V19	T18	T18	T18
IOR48A	I/O	3	none		True_of_IOR48B	True	AA22	AA22	AA22	R17	R17	R17	N16	N16	N16	N16	N16	N16	N18	N18	N18			
IOR48B	I/O	3	none		Comp_of_IOR48A	True	Y21	Y21	Y21	U18	U18	U18	N14	N14	N14	N14	N14	N14	P20	P20	P20			
IOR50A	I/O	3	none		True_of_IOR50B	True	V18	V18	V18	V19	V19	V19	P15	P15	P15	P15	P15	P15	V20	V20	V20	R16	R16	R16
IOR50B	I/O	3	none		Comp_of_IOR50A	True	W20	W20	W20	T17	T17	T17	R16	R16	R16	R16	R16	R16	U18	U18	U18	T17	T17	T17
BANK2 True LVDS Pair																								
IOR11A	I/O	2	none		True_of_IOR11B	True	G21	G21	G21	G16	G16	G16	E16	E16	E16	E16	E16	E16	F17	F17	F17			
IOR11B	I/O	2	none		Comp_of_IOR11A	True	G20	G20	G20	F18	F18	F18	F15	F15	F15	F15	F15	F15	G16	G16	G16			
IOR13A	I/O	2	none		True_of_IOR13B	True	H22	H22	H22	F19	F19	F19	F13	F13	F13	F13	F13	F13	G17	G17	G17	G16	G16	G16
IOR13B	I/O	2	none		Comp_of_IOR13A	True	H21	H21	H21	F20	F20	F20	G12	G12	G12	G12	G12	G12	H16	H16	H16	H15	H15	H15
IOR15A	I/O	2	none		True_of_IOR15B	True	H19	H19	H19	J14	J14	J14	F14	F14	F14	F14	F14	F14				E18	E18	E18
IOR15B	I/O	2	none		Comp_of_IOR15A	True	H18	H18	H18	J15	J15	J15	F16	F16	F16	F16	F16	F16				G17	G17	G17
IOR17A	I/O	2	none		True_of_IOR17B	True	J18	J18	J18	H18	H18	H18	F12	F12	F12	F12	F12	F12	H17	H17	H17	H16	H16	H16
IOR17B	I/O	2	none		Comp_of_IOR17A	True	J19	J19	J19	H19	H19	H19	G13	G13	G13	G13	G13	G13	J16	J16	J16	F18	F18	F18
IOR19A	I/O	2	none		True_of_IOR19B	True	J21	J21	J21	J17	J17	J17	G15	G15	G15	G15	G15	G15						
IOR19B	I/O	2	none		Comp_of_IOR19A	True	J22	J22	J22	H20	H20	H20	G14	G14	G14	G14	G14	G14						
IOR21A	I/O	2	none		True_of_IOR21B	True	K19	K19	K19	K14	K14	K14	G11	G11	G11	G11	G11	G11	H20	H20	H20	J16	J16	J16
IOR21B	I/O	2	none		Comp_of_IOR21A	True	K18	K18	K18	K15	K15	K15	H12	H12	H12	H12	H12	H12	J18	J18	J18	J17	J17	J17
IOR23A	I/O	2	none		True_of_IOR23B	True	L17	L17	L17	J19	J19	J19	G16	G16	G16	G16	G16	G16						
IOR23B	I/O	2	none		Comp_of_IOR23A	True	L16	L16	L16	J20	J20	J20	H15	H15	H15	H15	H15	H15						
IOR25A	I/O	2	none		True_of_IOR25B	True	K22	K22	K22	K17	K17	K17	H13	H13	H13	H13	H13	H13	K17	K17	K17			
IOR25B	I/O	2	none		Comp_of_IOR25A	True	L21	L21	L21	K18	K18	K18	J12	J12	J12	J12	J12	J12	L17	L17	L17			
IOR2A/RPLL1_T_fb	I/O	2	DQ5	RPLL1_T_fb	True_of_IOR2B	True	C21	C21	C21	D17	D17	D17	D14	D14	D14	D14	D14	D14	D18	D18	D18	B18	B18	B18
IOR2B/RPLL1_C_fb	I/O	2	DQ5	RPLL1_C_fb	Comp_of_IOR2A	True	C22	C22	C22	C18	C18	C18	E15	E15	E15	E15	E15	E15	D19	D19	D19	C17	C17	C17
IOR4A/RPLL1_T_in	I/O	2	DQ5	RPLL1_T_in	True_of_IOR4B	True	D22	D22	D22	C19	C19	C19	D16	D16	D16	D16	D16	D16	D20	D20	D20	E15	E15	E15
IOR4B/RPLL1_C_in	I/O	2	DQ5	RPLL1_C_in	Comp_of_IOR4A	True	D21	D21	D21	E17	E17	E17	E14	E14	E14	E14	E14	E14	E18	E18	E18	C18	C18	C18
IOR6A	I/O	2	DQS5		True_of_IOR6B	True	E22	E22	E22	B20	B20	B20	C15	C15	C15	C15	C15	C15						
IOR6B	I/O	2	DQS5		Comp_of_IOR6A	True	E21	E21	E21	C20	C20	C20	B16	B16	B16	B16	B16	B16						
IOR8A	I/O	2	DQ5		True_of_IOR8B	True	F22	F22	F22	D19	D19	D19	C16	C16	C16	C16	C16	C16	E17	E17	E17	E16	E16	E16
IOR8B	I/O	2	DQ5		Comp_of_IOR8A	True	G22	G22	G22	F17	F17	F17	D15	D15	D15	D15	D15	D15	F16	F16	F16	H13	H13	H13
BANK1 True LVDS Pair																								
IOT30A	I/O	1	DQ7		True_of_IOT30B	True	D12	D12	D12	A12	A12	A12							A11	A11	A11	C10	C10	C10
IOT30B	I/O	1	DQ7		Comp_of_IOT30A	True	E12	E12	E12	B12	B12	B12							B11	B11	B11	B11	B11	B11
IOT32A	I/O	1	DQ7		True_of_IOT32B	True	G12	G12	G12	A13	A13	A13							B12	B12	B12	B12	B12	B12
IOT32B	I/O	1	DQ7		Comp_of_IOT32A	True	F12	F12	F12	B13	B13	B13							C12	C12	C12	C11	C11	C11
IOT34A	I/O	1	DQ7		True_of_IOT34B	True	A13	A13	A13	G11	G11	G11	F8	F8	F8	F8	F8	F8	D12	D12	D12	A11	A11	A11
IOT34B	I/O	1	DQ7		Comp_of_IOT34A	True	B13	B13	B13	F11	F11	F11	D9	D9	D9	D9	D9	D9	D13	D13	D13	A12	A12	A12
IOT36A	I/O	1	DQ7		True_of_IOT36B	True	A14	A14	A14	D12	D12	D12	B9	B9	B9	B9	B9	B9	E12	E12	E12	F9	F9	F9
IOT36B	I/O	1	DQ7		Comp_of_IOT36A	True	B14	B14	B14	C12	C12	C12	A10	A10	A10	A10	A10	A10	D14	D14	D14	F10	F10	F10
IOT38A	I/O	1	DQ7		True_of_IOT38B	True	G14	G14	G14	A14	A14	A14	F9	F9	F9	F9	F9	F9	B14	B14	B14	C12	C12	C12
IOT38B	I/O	1	DQ7		Comp_of_IOT38A	True	F14	F14	F14	B14	B14	B14	E11	E11	E11	E11	E11	E11	C14	C14	C14	B13	B13	B13
IOT40A	I/O	1	DQ7		True_of_IOT40B	True	A15	A15	A15	A15	A15	A15	D10	D10	D10	D10	D10	D10	A13	A13	A13	A13	A13	A13
IOT40B	I/O	1	DQ7		Comp_of_IOT40A	True	B15	B15	B15	B15	B15	B15	E10	E10	E10	E10	E10	E10	B13	B13	B13	A14	A14	A14
IOT42A	I/O	1	DQ7		True_of_IOT42B	True	A16	A16	A16	A16	A16	A16	A11	A11	A11	A11	A11	A11	E14	E14	E14	B14	B14	B14
IOT42B	I/O	1	DQ7		Comp_of_IOT42A	True	B17	B17	B17	B16	B16	B16	C11	C11	C11	C11	C11	C11	E15	E15	E15	B15	B15	B15
IOT44A	I/O	1	DQ7		True_of_IOT44B	True	A17	A17	A17	A17	A17	A17	F10	F10	F10	F10	F10	F10	A15	A15	A15	F11	F11	F11
IOT44B	I/O	1	DQ7		Comp_of_IOT44A	True	B18	B18	B18	B17	B17	B17	D11	D11	D11	D11	D11	D11	B15	B15	B15	C13	C13	C13

Note!
[1] UV version.
[2] LV version.
[3] EV version.

Pin Name	Function	BANK	DQS	Configuration Function	Differential Pair	LVDS	UG484[1]	UG484[2]	UG484[3]	UG400[1]	UG400[2]	UG400[3]	UG256[1]	UG256[2]	UG256[3]	PG256[1]	PG256[2]	PG256[3]	UG332[1]	UG332[2]	UG332[3]	UG324[1]	UG324[2]	UG324[3]
IOT48A	I/O	1	DQS6		True_of_IOT48B	True	A18	A18	A18	C15	C15	C15	B11	B11	B11	B11	B11	B11	D17	D17	D17	C14	C14	C14
IOT48B	I/O	1	DQS6		Comp_of_IOT48A	True	B19	B19	B19	C16	C16	C16	A12	A12	A12	A12	A12	A12	D16	D16	D16	C15	C15	C15
IOT50A	I/O	1	DQ6		True_of_IOT50B	True	A19	A19	A19	A18	A18	A18	B13	B13	B13	B13	B13	B13	A19	A19	A19	A15	A15	A15
IOT50B	I/O	1	DQ6		Comp_of_IOT50A	True	B20	B20	B20	B18	B18	B18	A14	A14	A14	A14	A14	A14	B18	B18	B18	A16	A16	A16
IOT52A	I/O	1	DQ6		True_of_IOT52B	True	A20	A20	A20	E15	E15	E15	C12	C12	C12	C12	C12	C12	B16	B16	B16	B16	B16	B16
IOT52B	I/O	1	DQ6		Comp_of_IOT52A	True	B21	B21	B21	D16	D16	D16	B12	B12	B12	B12	B12	B12	C16	C16	C16	A17	A17	A17
IOT54A	I/O	1	DQ6		True_of_IOT54B	True	A21	A21	A21	B19	B19	B19	B14	B14	B14	B14	B14	B14	A18	A18	A18	D14	D14	D14
IOT54B	I/O	1	DQ6		Comp_of_IOT54A	True	B22	B22	B22	A20	A20	A20	A15	A15	A15	A15	A15	A15	C17	C17	C17	D15	D15	D15
BANK0 True LVDS Pair																								
IOT12A	I/O	0	DQ8		True_of_IOT12B	True	B5	B5	B5	B4	B4	B4	A3	A3	A3	A3	A3	A3	C6	C6	C6	A4	A4	A4
IOT12B	I/O	0	DQ8		Comp_of_IOT12A	True	A6	A6	A6	A4	A4	A4	B4	B4	B4	B4	B4	B4	D7	D7	D7	A5	A5	A5
IOT14A	I/O	0	DQ8		True_of_IOT14B	True	B6	B6	B6	B5	B5	B5	D6	D6	D6	D6	D6	D6	A7	A7	A7	B6	B6	B6
IOT14B	I/O	0	DQ8		Comp_of_IOT14A	True	A7	A7	A7	A5	A5	A5	E7	E7	E7	E7	E7	E7	B8	B8	B8	A6	A6	A6
IOT16A	I/O	0	DQ8		True_of_IOT16B	True	C8	C8	C8	B6	B6	B6							D8	D8	D8	D8	D8	D8
IOT16B	I/O	0	DQ8		Comp_of_IOT16A	True	D8	D8	D8	A6	A6	A6							E9	E9	E9	E7	E7	E7
IOT18A	I/O	0	DQ8		True_of_IOT18B	True	B8	B8	B8	B7	B7	B7	B7	B7	B7	B7	B7	B7	B6	B6	B6	A7	A7	A7
IOT18B	I/O	0	DQ8		Comp_of_IOT18A	True	A8	A8	A8	A7	A7	A7	C7	C7	C7	C7	C7	C7	A6	A6	A6	B7	B7	B7
IOT20A	I/O	0	DQ8		True_of_IOT20B	True	B9	B9	B9	B8	B8	B8	E6	E6	E6	E6	E6	E6	D9	D9	D9	B8	B8	B8
IOT20B	I/O	0	DQ8		Comp_of_IOT20A	True	A9	A9	A9	A8	A8	A8	D7	D7	D7	D7	D7	D7	E10	E10	E10	A8	A8	A8
IOT22A	I/O	0	DQ8		True_of_IOT22B	True	F10	F10	F10	B9	B9	B9	F7	F7	F7	F7	F7	F7						
IOT22B	I/O	0	DQ8		Comp_of_IOT22A	True	E10	E10	E10	A9	A9	A9	E8	E8	E8	E8	E8	E8						
IOT24A/GCLKT_0	I/O	0	DQ8	GCLKT_0	True_of_IOT24B	True	B10	B10	B10	B10	B10	B10	C8	C8	C8	C8	C8	C8	B9	B9	B9	A9	A9	A9
IOT24B/GCLKC_0	I/O	0	DQ8	GCLKC_0	Comp_of_IOT24A	True	A10	A10	A10	A10	A10	A10	A8	A8	A8	A8	A8	A8	A9	A9	A9	B9	B9	B9
IOT26A	I/O	0	DQ8		True_of_IOT26B	True	B11	B11	B11	B11	B11	B11	D8	D8	D8	D8	D8	D8	C10	C10	C10	A10	A10	A10
IOT26B	I/O	0	DQ8		Comp_of_IOT26A	True	A11	A11	A11	A11	A11	A11	E9	E9	E9	E9	E9	E9	B10	B10	B10	B10	B10	B10
IOT2A	I/O	0	DQ9		True_of_IOT2B	True	B1	B1	B1	B1	B1	B1	C4	C4	C4	C4	C4	C4	C4	C4	C4	A2	A2	A2
IOT2B	I/O	0	DQ9		Comp_of_IOT2A	True	A2	A2	A2	A1	A1	A1	B5	B5	B5	B5	B5	B5	B4	B4	B4	B3	B3	B3
IOT4A	I/O	0	DQ9		True_of_IOT4B	True	B2	B2	B2	G7	G7	G7	B3	B3	B3	B3	B3	B3	A4	A4	A4	C3	C3	C3
IOT4B	I/O	0	DQ9		Comp_of_IOT4A	True	A3	A3	A3	F7	F7	F7	A2	A2	A2	A2	A2	A2	C5	C5	C5	C4	C4	C4
IOT6A	I/O	0	DQ9		True_of_IOT6B	True	B3	B3	B3	B2	B2	B2	A4	A4	A4	A4	A4	A4	B5	B5	B5	D5	D5	D5
IOT6B	I/O	0	DQ9		Comp_of_IOT6A	True	A4	A4	A4	A2	A2	A2	C5	C5	C5	C5	C5	C5	A5	A5	A5	B5	B5	B5
IOT8A	I/O	0	DQ9		True_of_IOT8B	True	B4	B4	B4	B3	B3	B3	A5	A5	A5	A5	A5	A5	E7	E7	E7	A3	A3	A3
IOT8B	I/O	0	DQ9		Comp_of_IOT8A	True	A5	A5	A5	A3	A3	A3	B6	B6	B6	B6	B6	B6	D6	D6	D6	B4	B4	B4

Note!
[1] It is recommended to set Bank VCCIO of True LVDS to 2.5V.
[2] VCCX should be greater than or equal to VCCIO.

Recommended Operating Conditions of UG400/UG484/UG256/PG256/UG324 Packages in GW2AN-9X (UV Version)			
Name	**Description**	**Min.**	**Max.**
VCC/VCCX	Core voltage and auxiliary voltage are internally short-circuited.	2.7V	3.6V
VCCIO0, VCCIO1, VCCIO2, VCCIO3, VCCIO4, VCCIO6, VCCIO7, VCCIO8, VCCIO9	I/O Bank voltage	1.14V	3.6V
VCCIO5	I/O Bank5 voltage When the voltage is less than 2.0V, VCCIO5 will add about 20mA quiescent current.	1.14V	3.6V

Recommended Operating Conditions of UG400/UG484/UG256/PG256/UG324 Packages in GW2AN-9X (LV Version)			
Name	**Description**	**Min.**	**Max.**
VCC	Core voltage	0.95V	1.05V
VCCIO1, VCCIO2, VCCIO3, VCCIO4, VCCIO6, VCCIO7, VCCIO8, VCCIO9	I/O Bank voltage	1.14V	3.6V
VCCX/VCCIO0	Core voltage and I/O Bank0 voltage are internally short-circuited.	2.7V	3.6V
VCCIO5	I/O Bank5 voltage When the voltage is less than 2.0V, VCCIO5 will add about 20mA quiescent current.	1.14V	3.6V

Recommended Operating Conditions of UG400/UG484/UG256/PG256/UG324 Packages in GW2AN-9X (EV Version)			
Name	**Description**	**Min.**	**Max.**
VCC	Core voltage	1.14V	1.26V
VCCIO1, VCCIO2, VCCIO3, VCCIO4, VCCIO6, VCCIO7, VCCIO8, VCCIO9	I/O Bank voltage	1.14V	3.6V
VCCX/VCCIO0	Core voltage and I/O Bank0 voltage are internally short-circuited.	2.7V	3.6V
VCCIO5	I/O Bank5 voltage When the voltage is less than 2.0V, VCCIO5 will add about 20mA quiescent current.	1.14V	3.6V