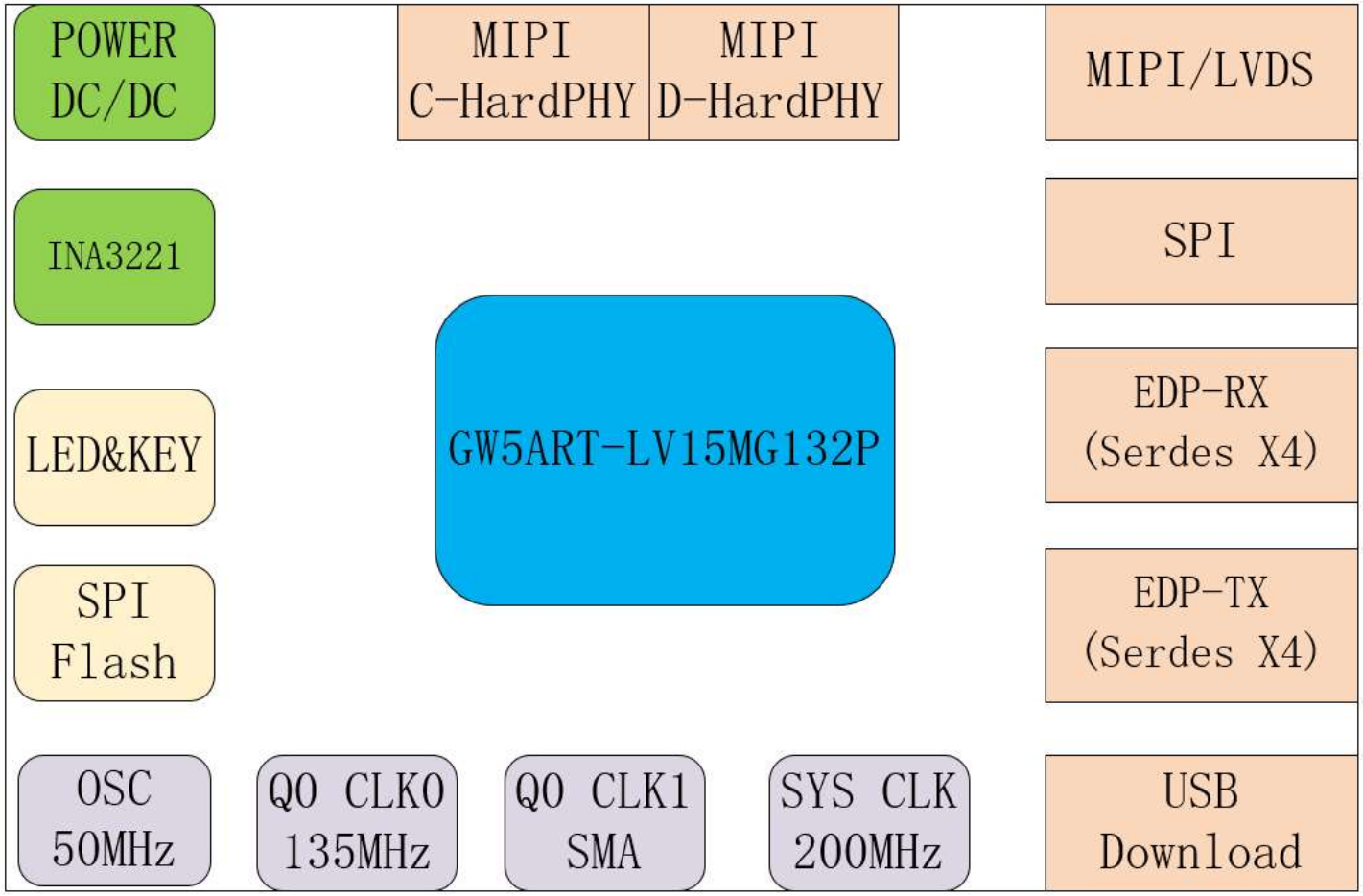
SCHEMATIC	CONTENT	PAGE
COVER PAGE	COVER PAGE	01
DIAGRAM	PCB DIAGRAM	02
POWER	VCC3P3,VCC2P8,VCC2P5,VCC1P8,VCC1P2,VCC0P9	03~05
FPGA-1	MIPI,SPI-FLASH,SPI,CLOCK,CONFIG	06
FPGA-2	EDP-TX,EDP-RX	07
FPGA-3	LVDS/MIPI,USB-JTAG,OSC,RST,LED	08
FPGA-4	FPGA POWER&GND	09

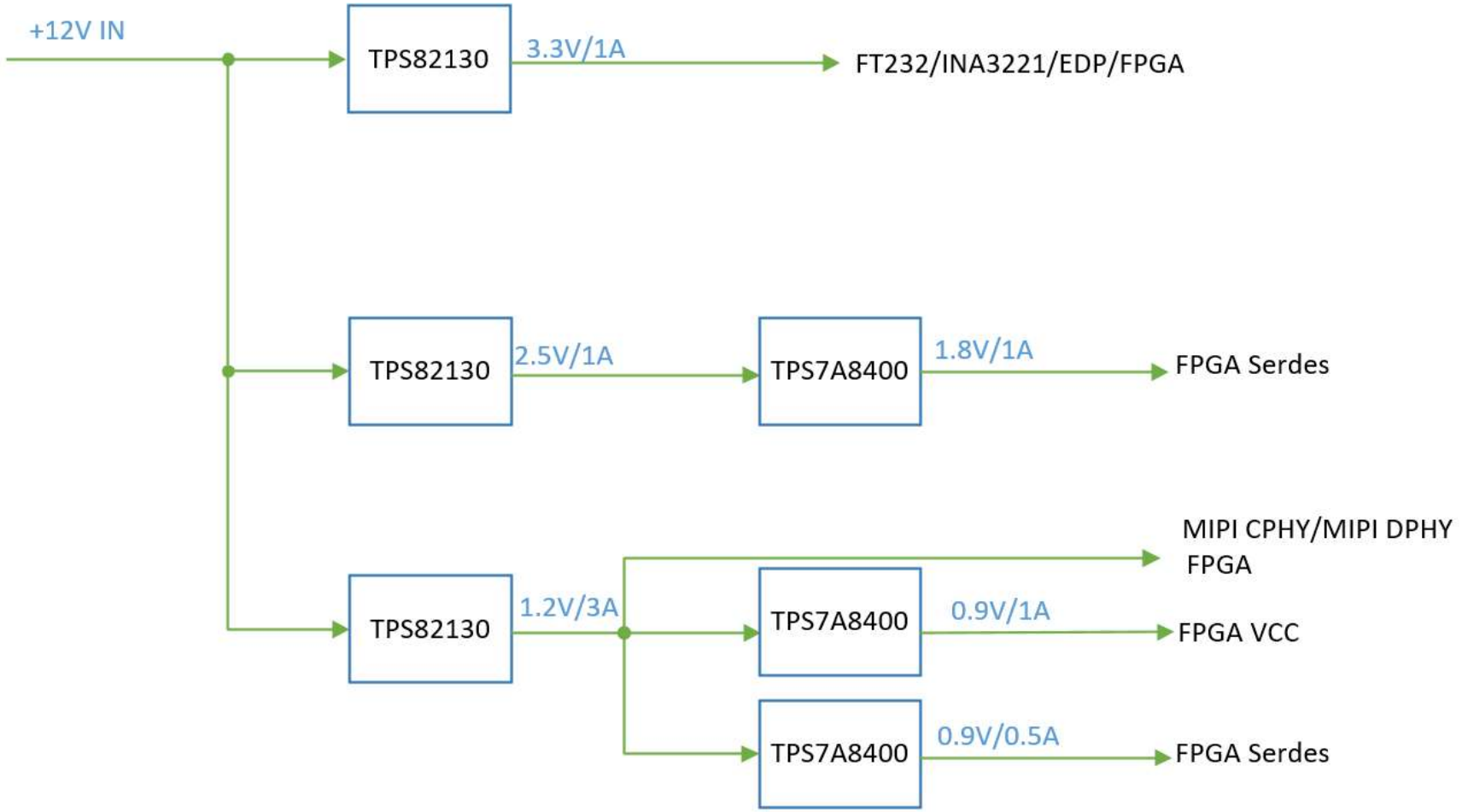
Title	DK_EDP_GW5ART-LV15MG132P_V1.0	
Size A3	Document Number COVER PAGE	Rev V1.0
Date: Wednesday, July 10, 2024	Sheet 1 of 9	

PCB DIAGRAM



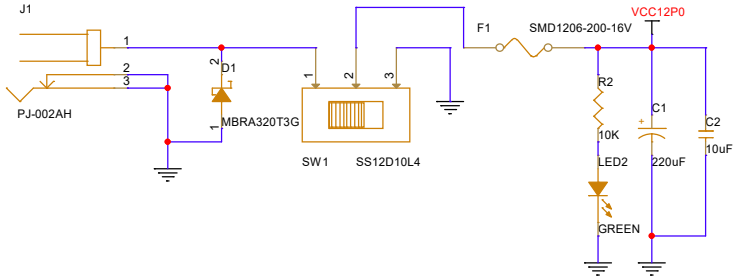
Title	DK_EDP_GW5ART-LV15MG132P_V1.0	
Size A3	Document Number DIAGRAM	Rev V1.0
Date: Thursday, August 08, 2024	Sheet 2 of 9	

POWER TREE

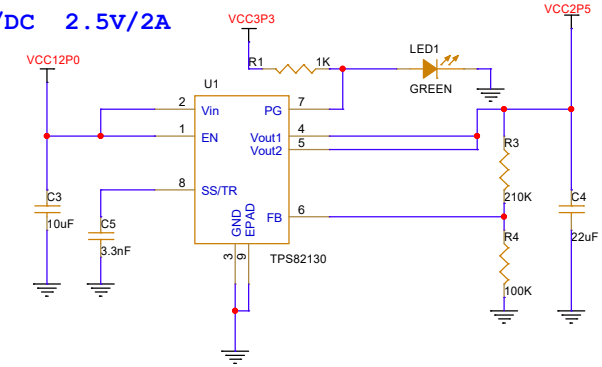


Title	DK_EDP_GW5ART-LV15MG132P_V1.0	
Size A3	Document Number POWER TREE	Rev V1.0
Date: Thursday, August 08, 2024	Sheet 3 of 9	

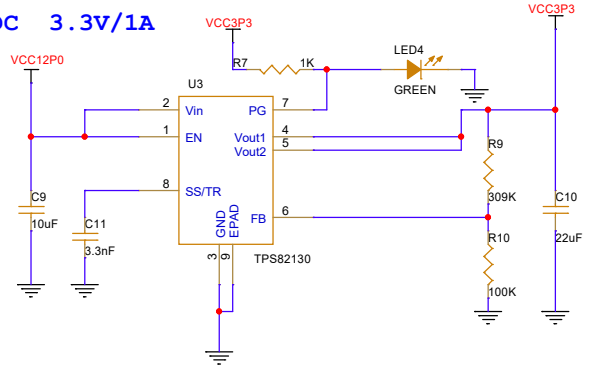
12V INPUT



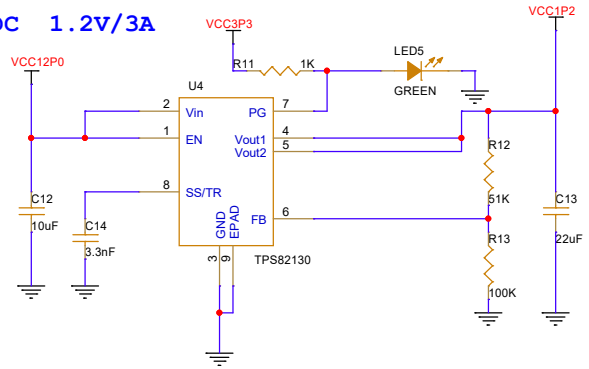
DC/DC 2.5V/2A



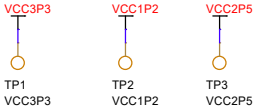
DC/DC 3.3V/1A



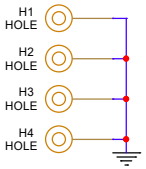
DC/DC 1.2V/3A



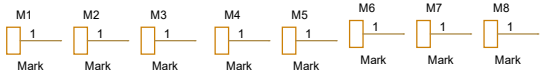
Power Test Hole



Mounting Hole

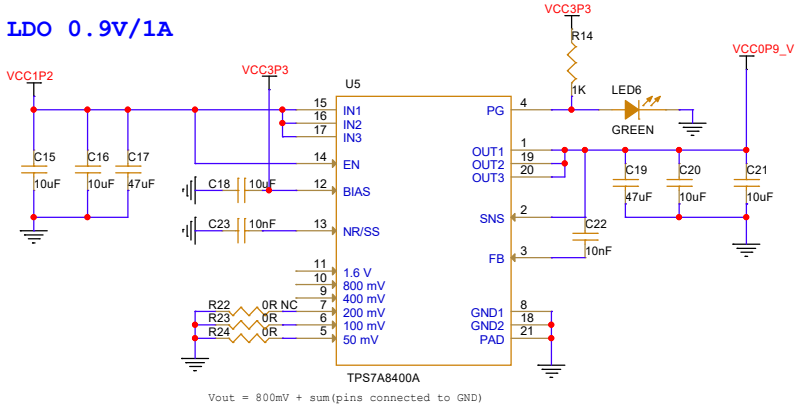


Mark

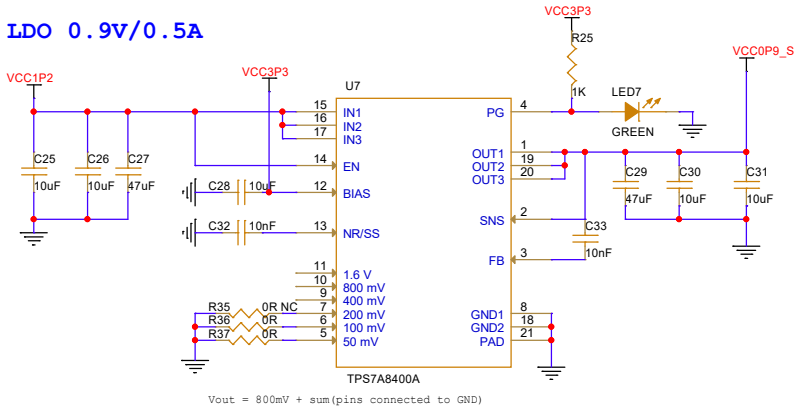


Title	DK_EDP_GW5ART-LV15MG132P_V1.0	
Size A3	Document Number POWER I	Rev V1.0
Date: Monday, August 12, 2024	Sheet 4 of 9	

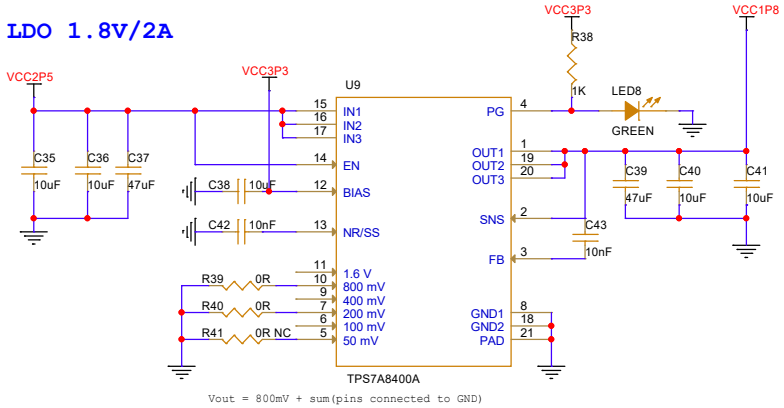
LDO 0.9V/1A



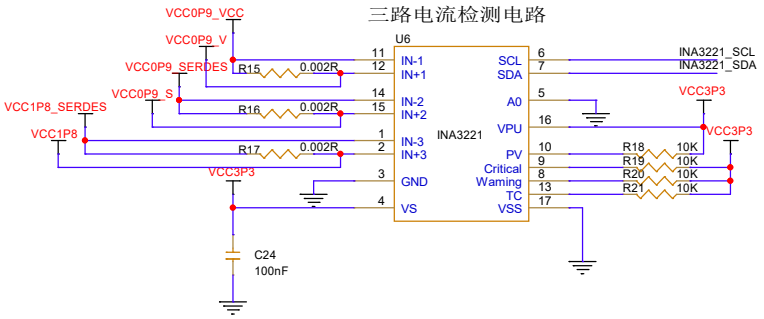
LDO 0.9V/0.5A



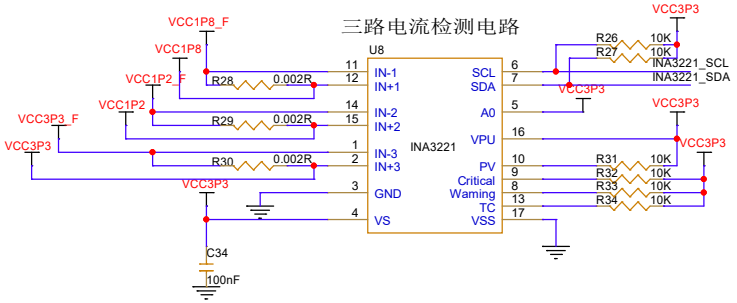
LDO 1.8V/2A

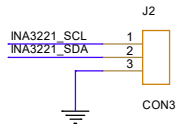


三路电流检测电路

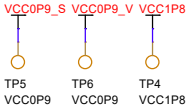


三路电流检测电路

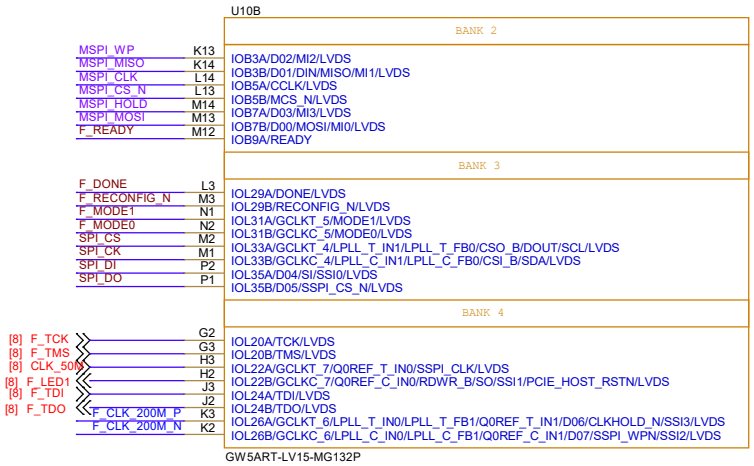


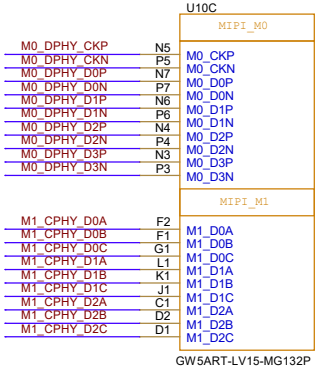


Power Test Hole

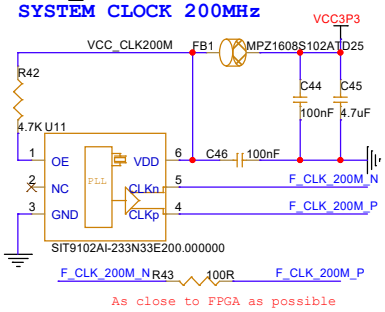


Title	DK_EDP_GW5ART-LV15MG132P_V1.0	
Size A3	Document Number POWER II	Rev V1.0
Date: Monday, August 12, 2024	Sheet 5 of 9	

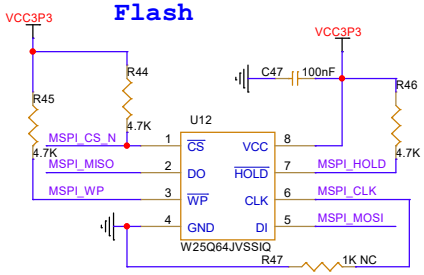




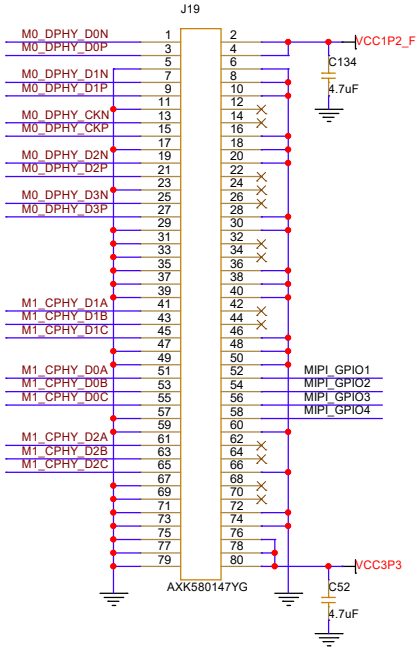
SYSTEM CLOCK 200MHz



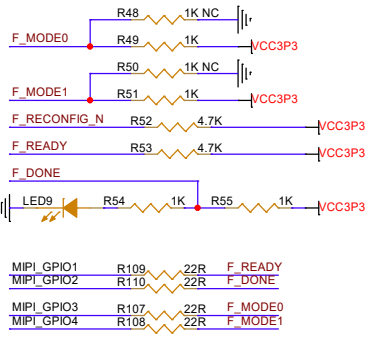
Flash



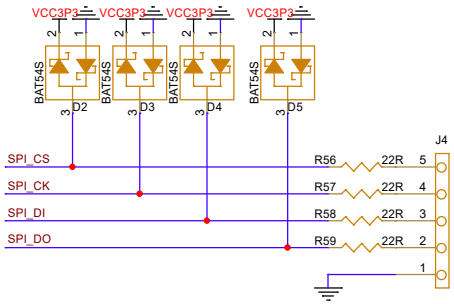
MIPI



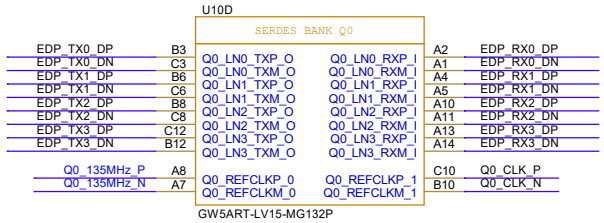
FPGA CONFIG PIN



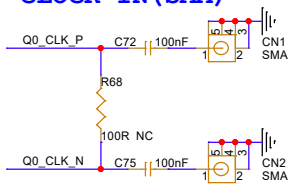
SPI(Remote upgrade)



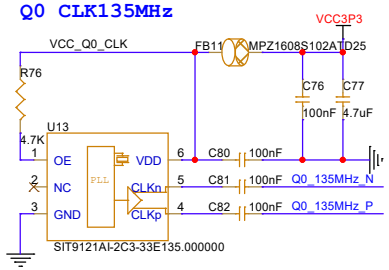
Title	DK_EDP_GW5ART-LV15MG132P_V1.0	
Size A3	Document Number MIPI/SPI/FLASH/CLOCK	Rev V1.0
Date: Monday, August 12, 2024	Sheet 6 of 9	



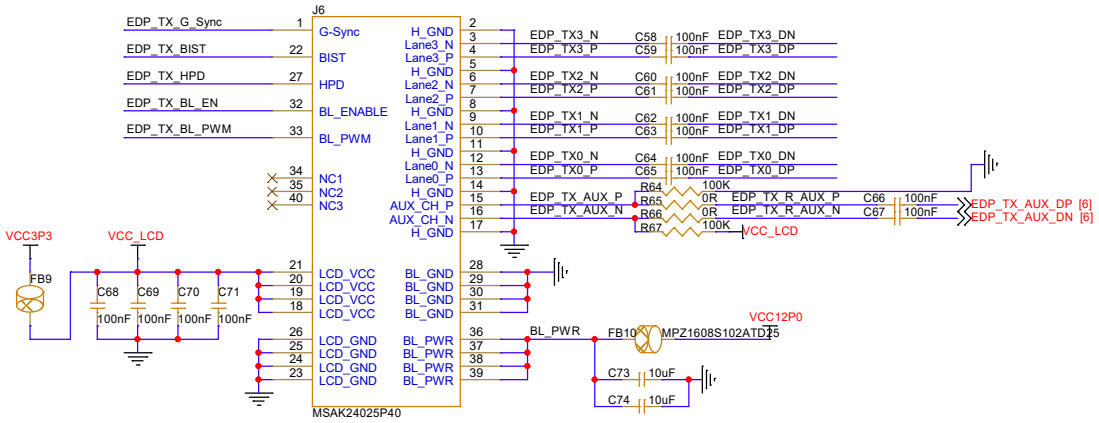
CLOCK IN(SMA)



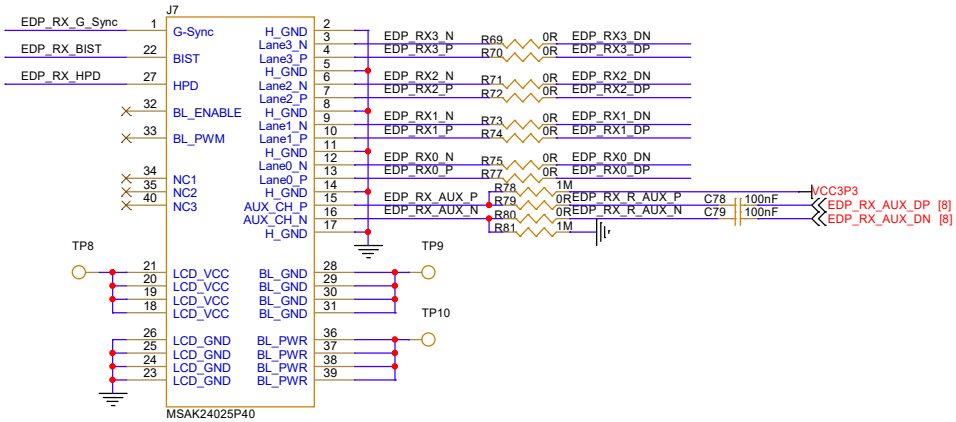
Q0 CLK135MHz

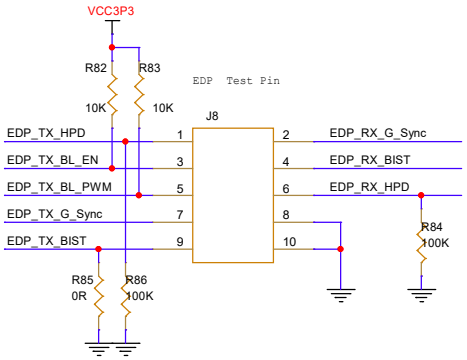


EDP-TX

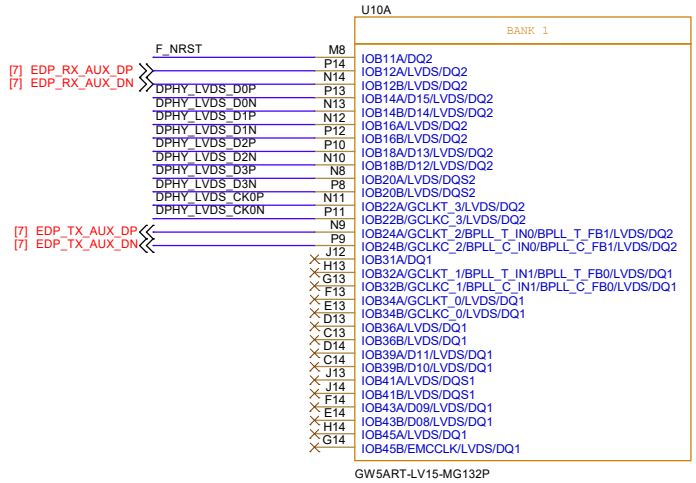


EDP-RX

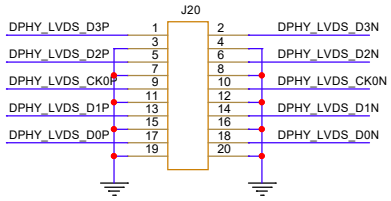


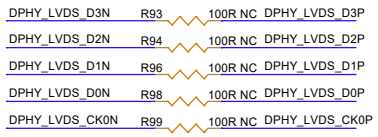


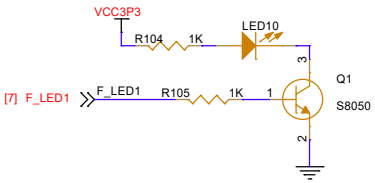
Title	DK_EDP_GW5ART-LV15MG132P_V1.0	
Size A3	Document Number EDP-RX/EDP-TX	Rev V1.0
Date: Friday, July 12, 2024	Sheet 7 of 9	



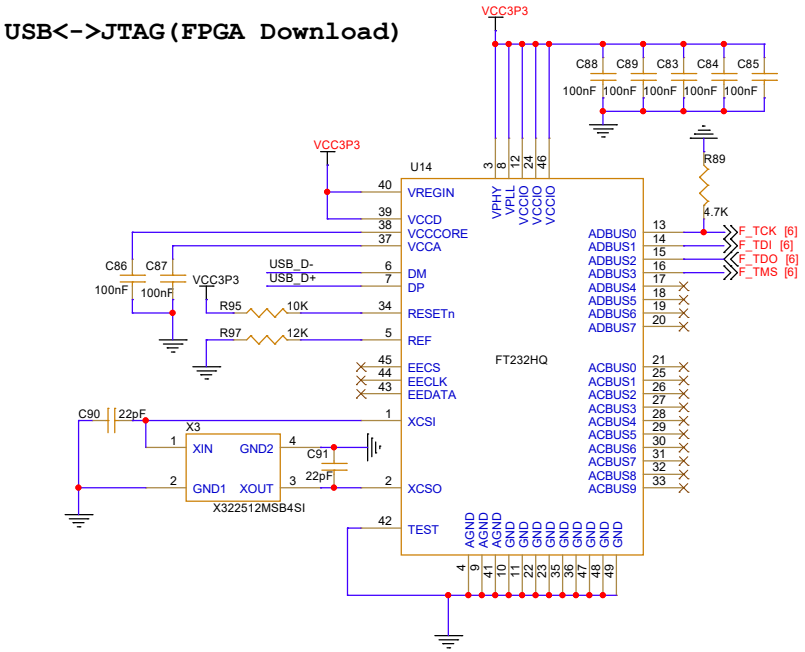
DPHY/LVDS

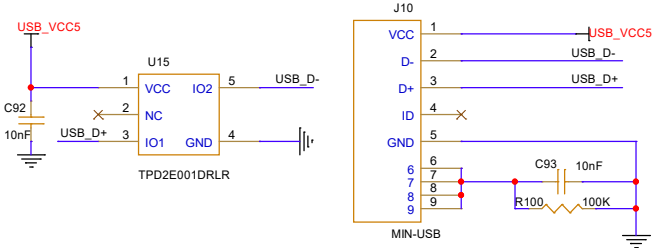


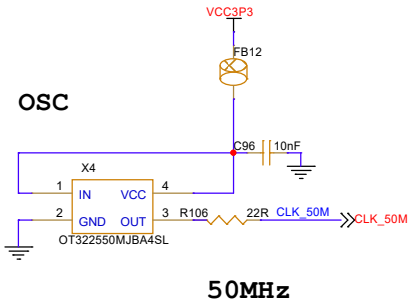


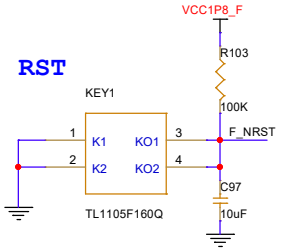


USB<->JTAG(FPGA Download)

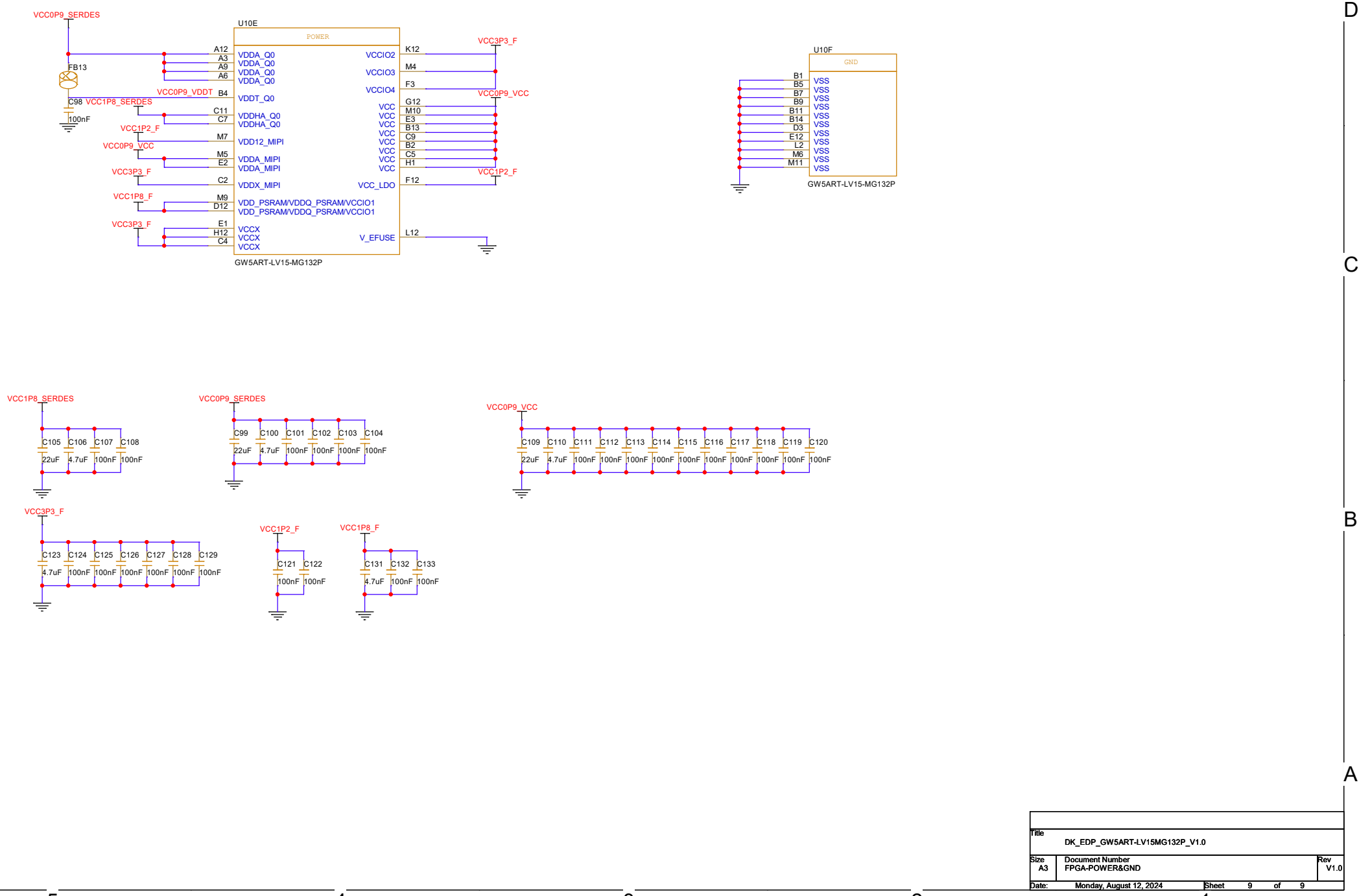








Title	DK_EDP_GW5ART-LV15MG132P_V1.0	
Size A3	Document Number LVDS/MIPI/USB-JTAG	Rev V1.0
Date: Thursday, August 08, 2024	Sheet 8 of 9	



Title	DK_EDP_GW5ART-LV15MG132P_V1.0	
Size A3	Document Number FPGA-POWER&GND	Rev V1.0
Date: Monday, August 12, 2024	Sheet 9 of 9	