

5

4

3

2

1

D

D

C

C

B

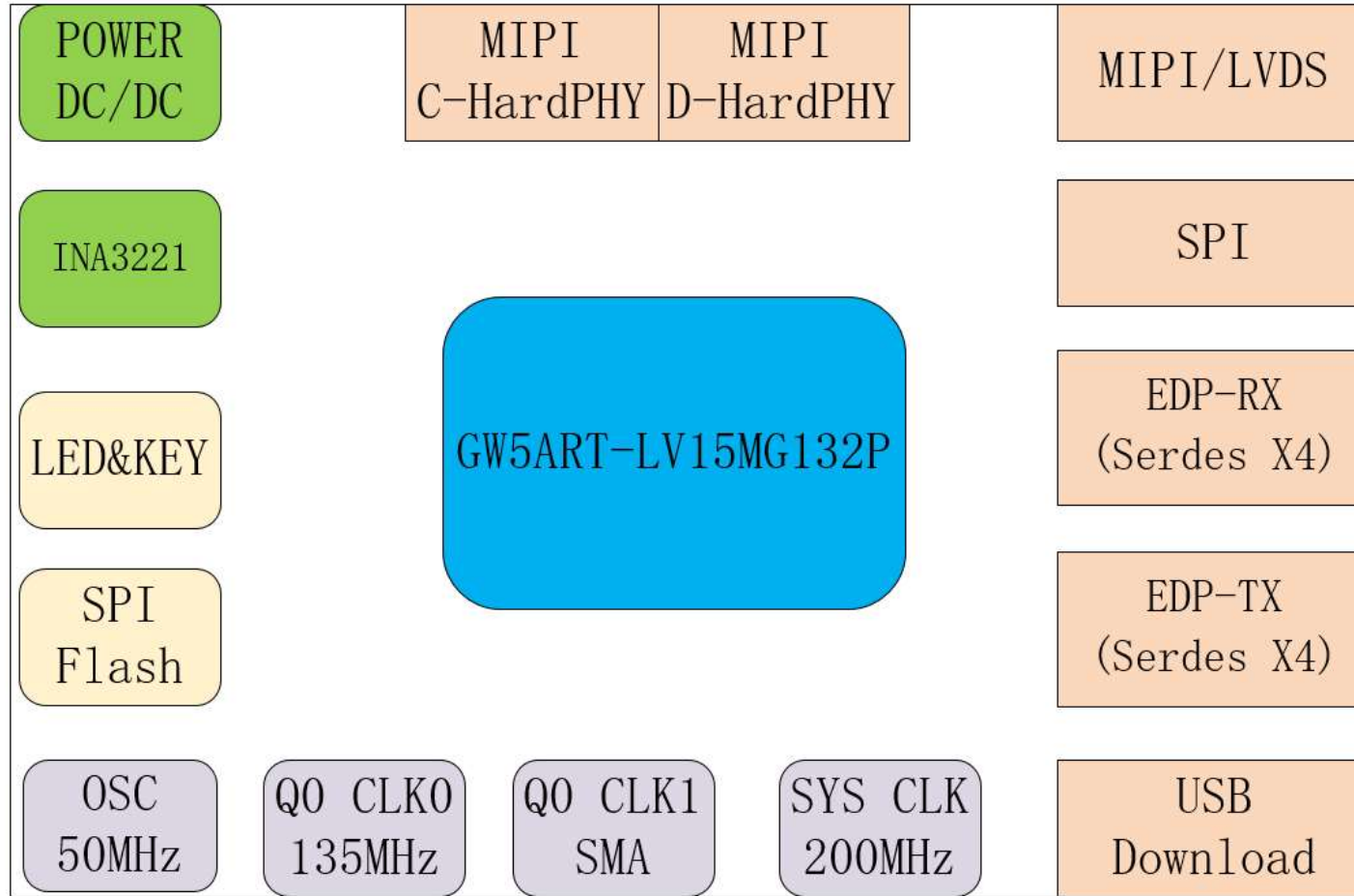
B

A

A

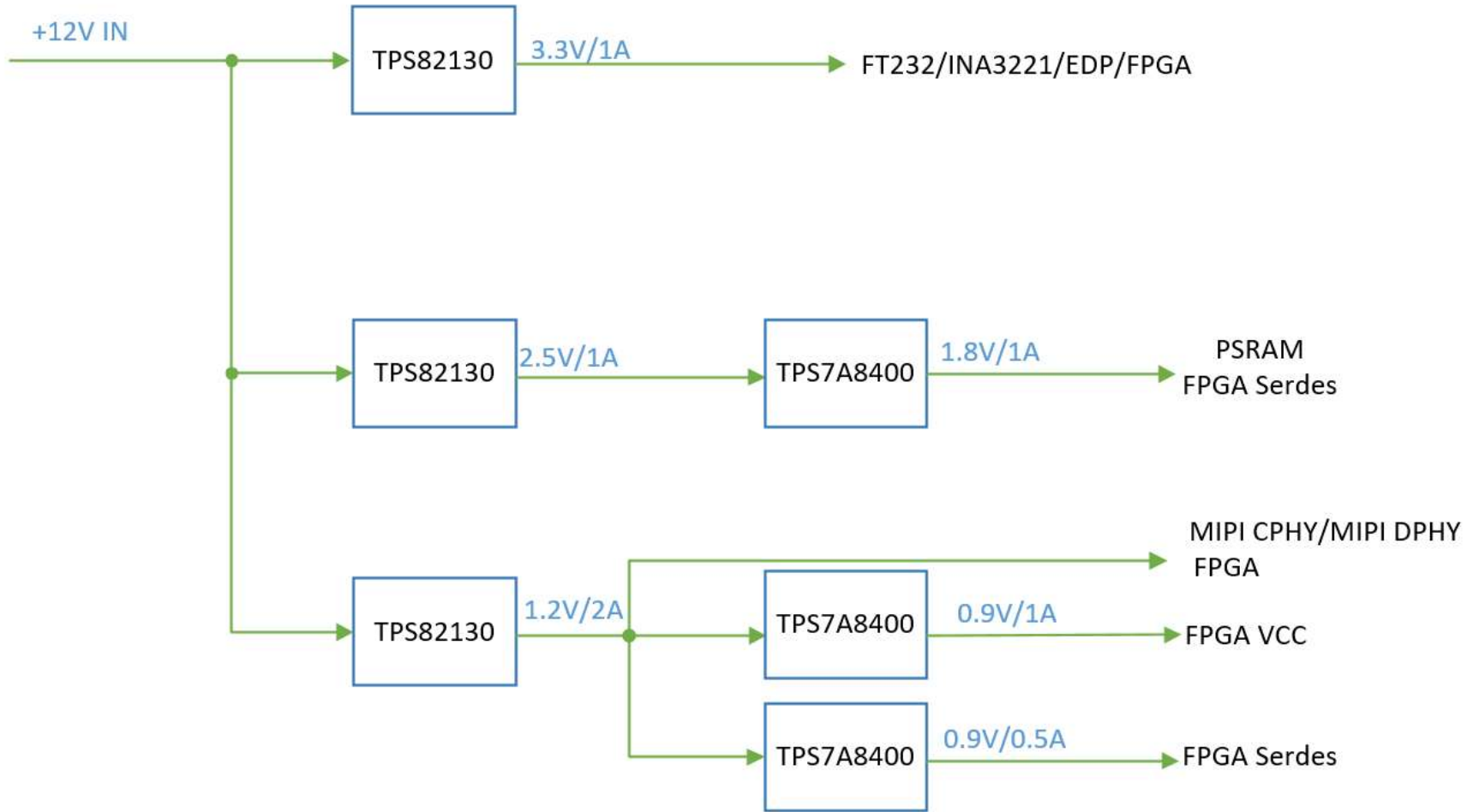
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# PCB DIAGRAM



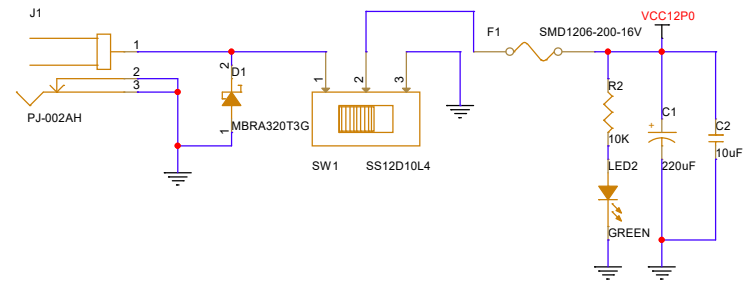
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# POWER TREE

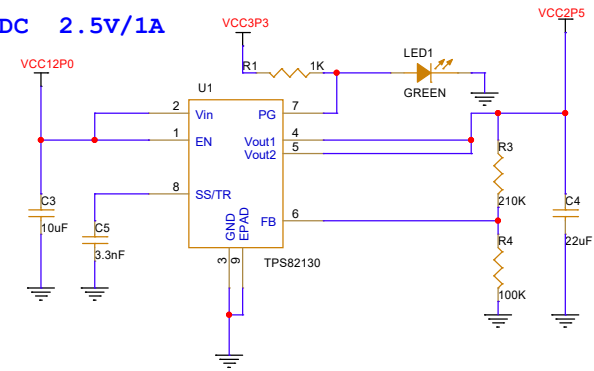


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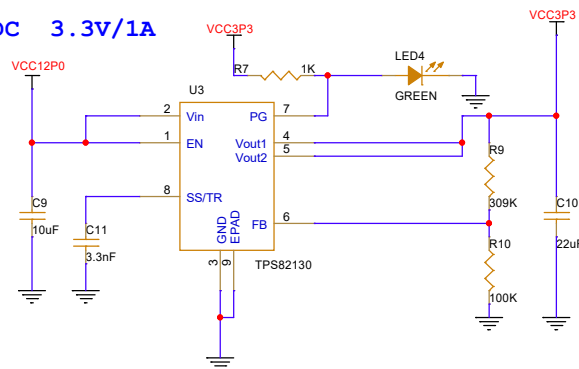
12V INPUT



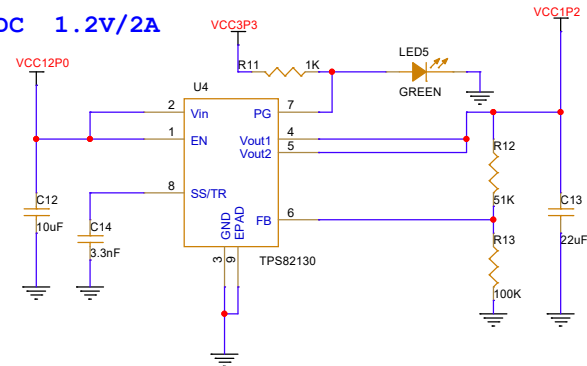
DC/DC 2.5V/1A



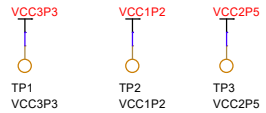
DC/DC 3.3V/1A



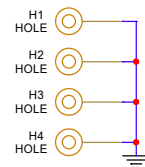
DC/DC 1.2V/2A



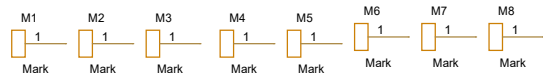
Power Test Hole



Mounting Hole

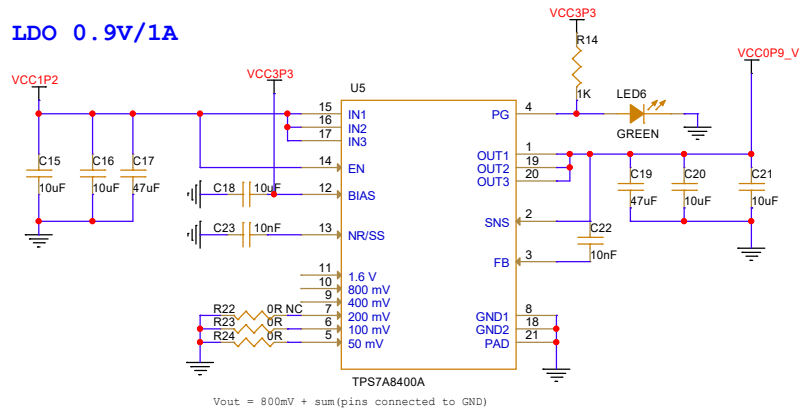


Mark



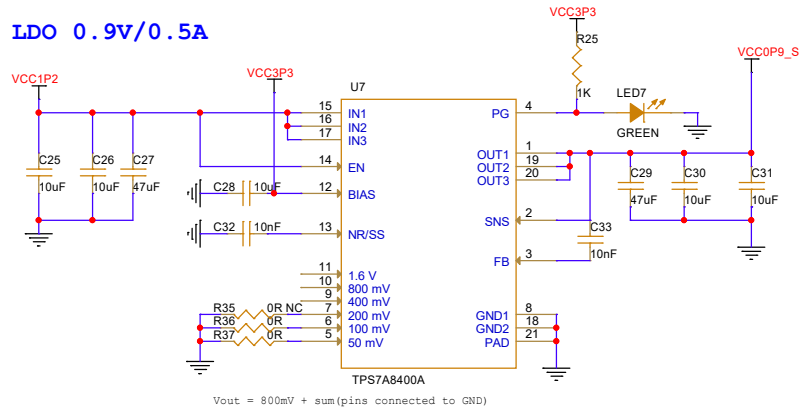
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Size	Document Number	Rev
A3	POWER I	V1.0
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**LDO 0.9V/1A**



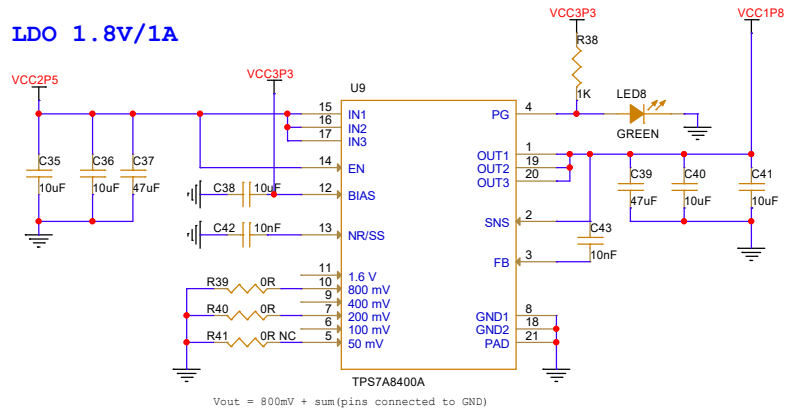
$V_{out} = 800mV + \text{sum}(\text{pins connected to GND})$

**LDO 0.9V/0.5A**



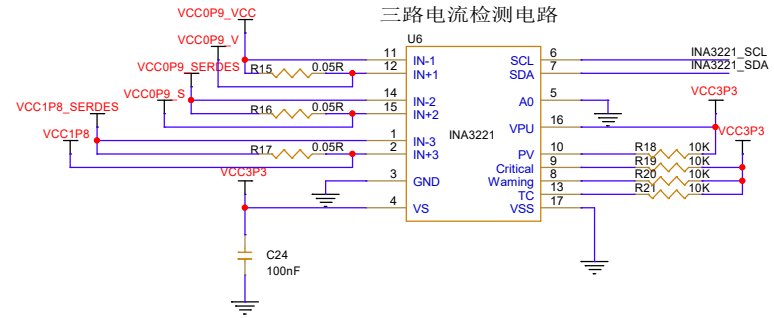
$V_{out} = 800mV + \text{sum}(\text{pins connected to GND})$

**LDO 1.8V/1A**

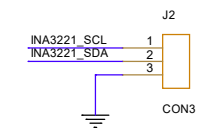
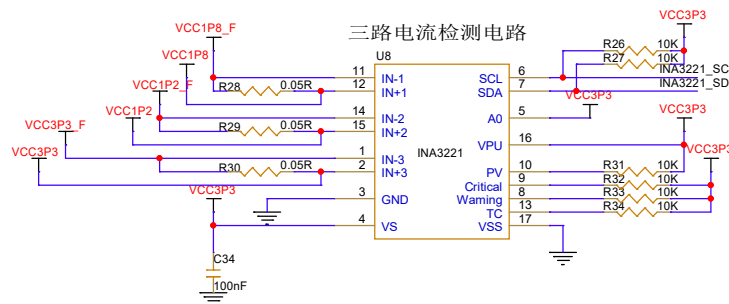


$V_{out} = 800mV + \text{sum}(\text{pins connected to GND})$

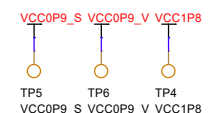
**三路电流检测电路**



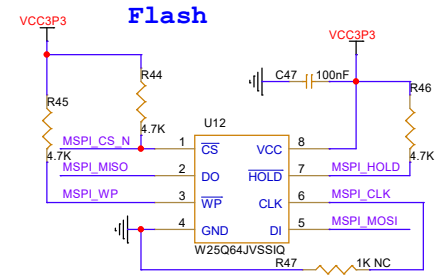
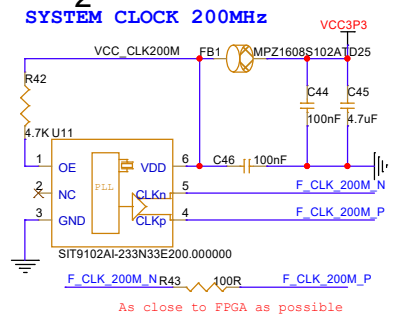
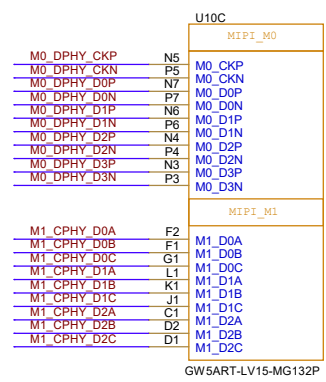
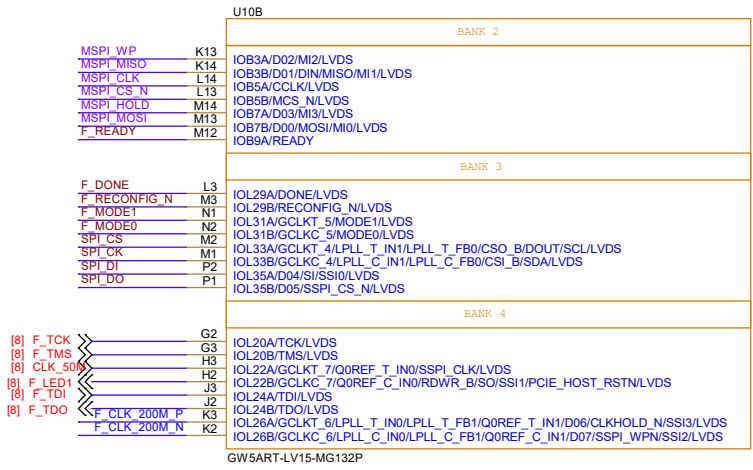
**三路电流检测电路**



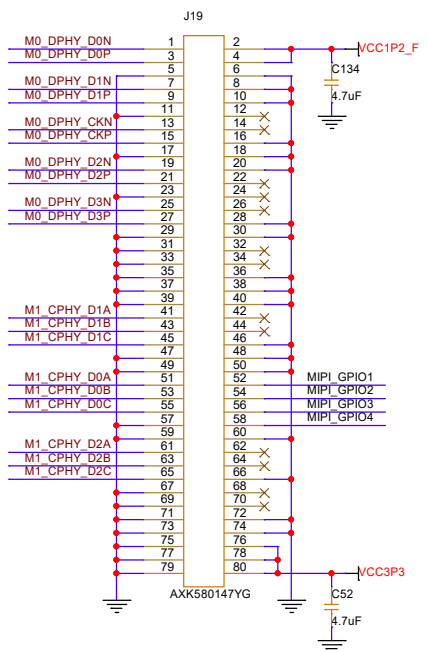
**Power Test Hole**



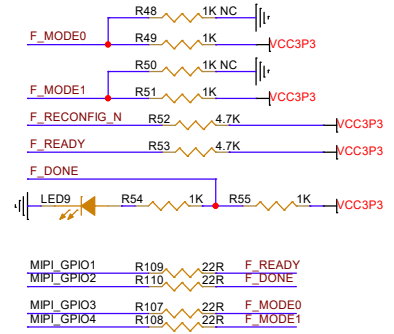
Title		
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A3	POWER II	V1.0
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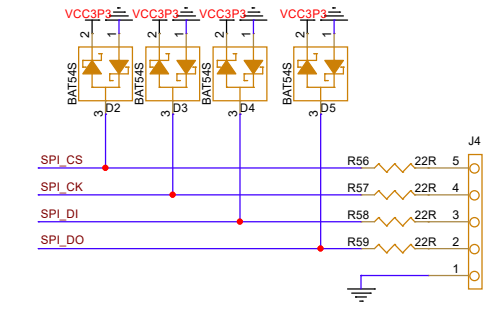
**MIPI**

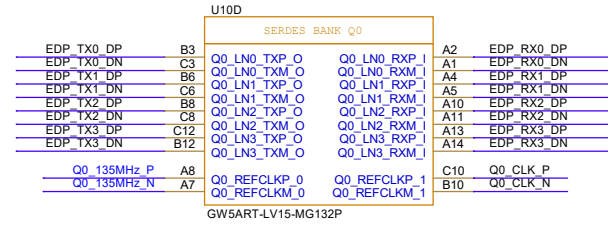


**FPGA CONFIG PIN**

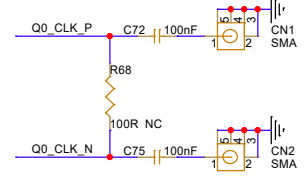


**SPI (Remote upgrade)**

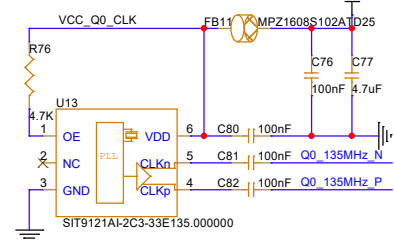




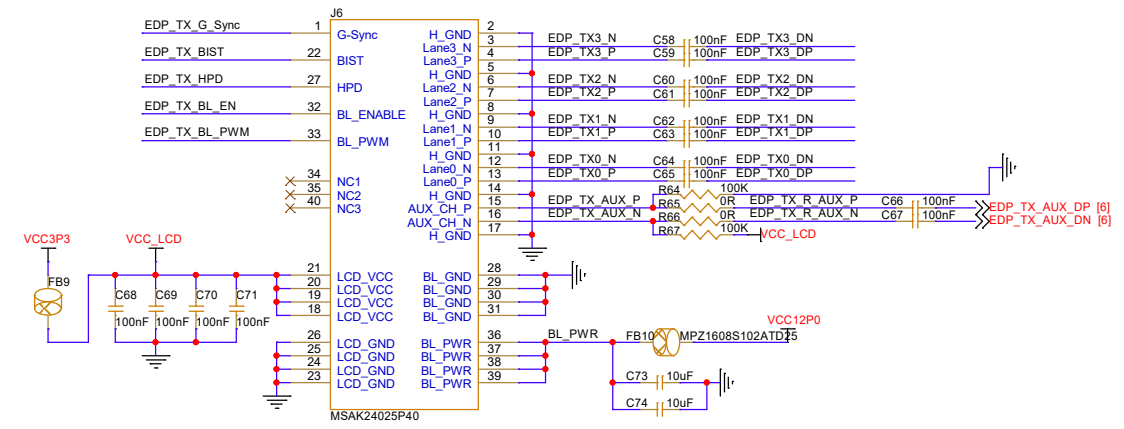
**CLOCK IN (SMA)**



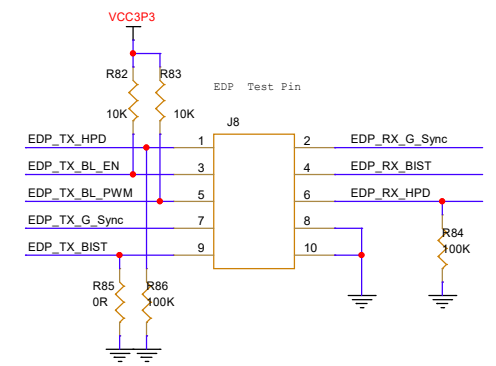
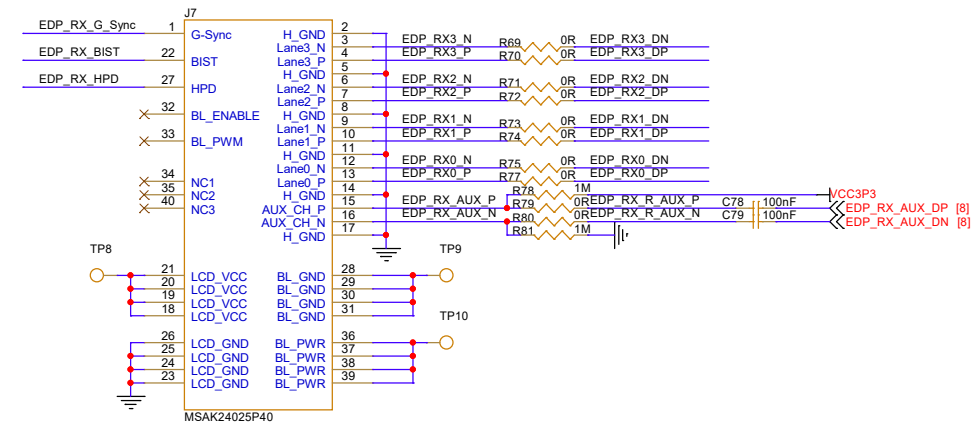
**Q0 CLK135MHz**



**EDP-TX**



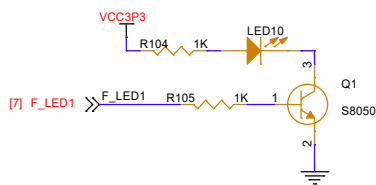
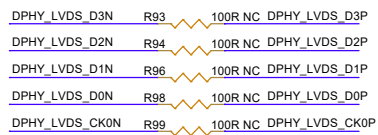
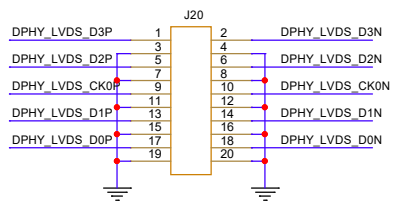
**EDP-RX**



File		
DK_EDP_GW5ART-LV15MG132P_V1.0		
Size	Document Number	Rev
A3	EDP-RX/EDP-TX	V1.0
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**DPHY/LVDS**



**USB<->JTAG (FPGA Download)**

