| SCHEMATIC | CONTENT | PAGE |
|---|---|---|
| COVER PAGE | COVER PAGE | 01 |
| DIAGRAM | PCB DIAGRAM | 02 |
| POWER | VCC3P3,VCC2P8,VCC2P5,VCC1P8,VCC1P2,VCC0P9 | 03~05 |
| FPGA-1 | MIPI,SPI-FLASH,SPI,CLOCK,CONFIG | 06 |
| FPGA-2 | EDP-TX,EDP-RX | 07 |
| FPGA-3 | LVDS/MIPI,USB-JTAG,OSC,RST,LED | 08 |
| FPGA-4 | FPGA POWER&GND | 09 |
| | | |
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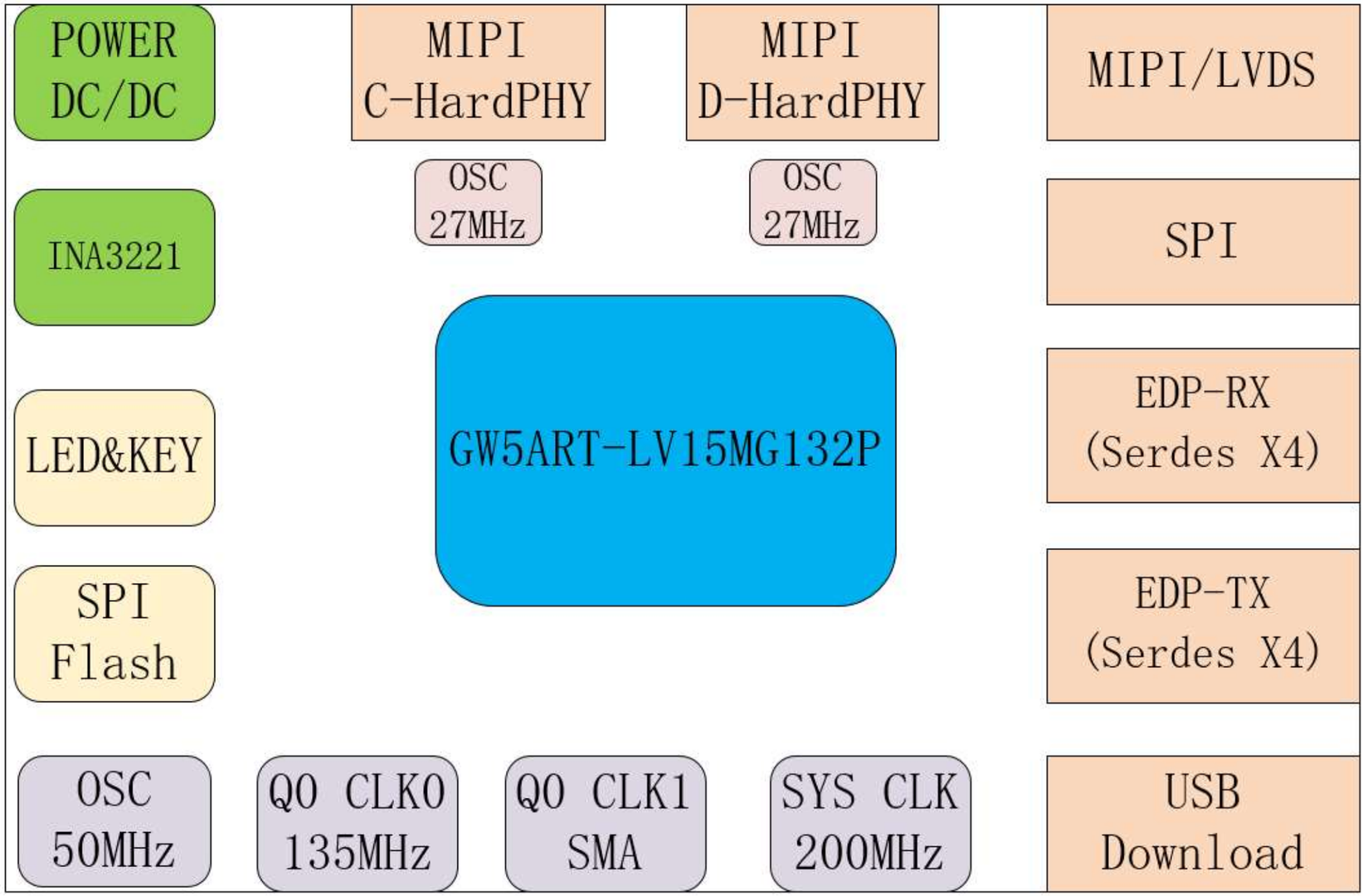
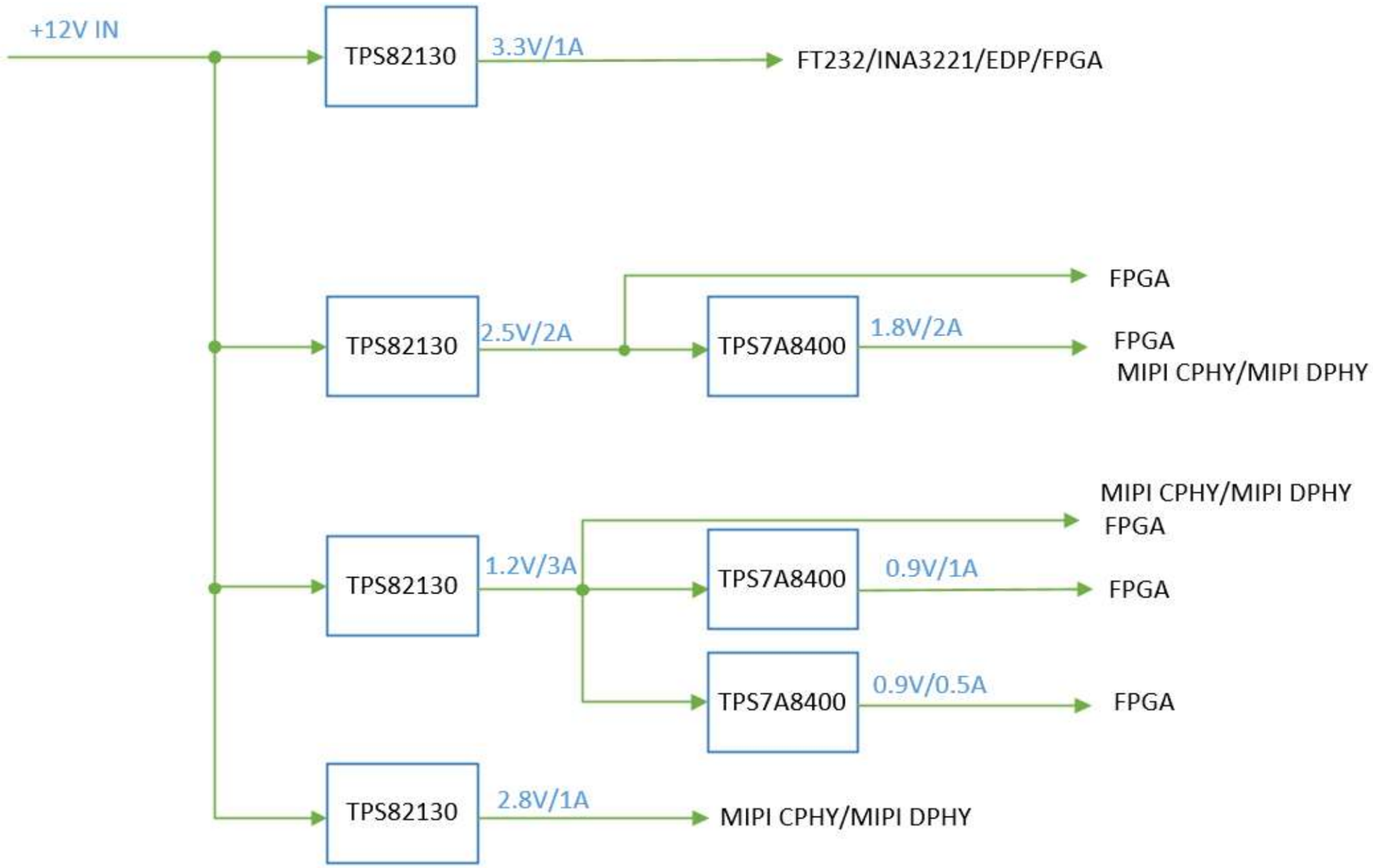
| | | |
|---|---|---|
| Title | DK_EDP_GW5ART-LV15MG132P_V1.0 | |
| Size A3 | Document Number COVER PAGE | Rev V1.0 |
| Date: Wednesday, July 10, 2024 | Sheet 1 of 9 | |

# PCB DIAGRAM



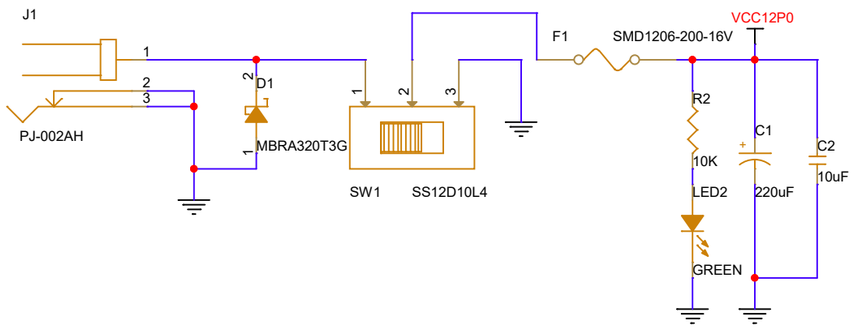

| | | |
|---|---|---|
| Title | DK_EDP_GW5ART-LV15MG132P_V1.0 | |
| Size A3 | Document Number DIAGRAM | Rev V1.0 |
| Date: Wednesday, July 10, 2024 | Sheet 2 of 9 | |

# POWER TREE

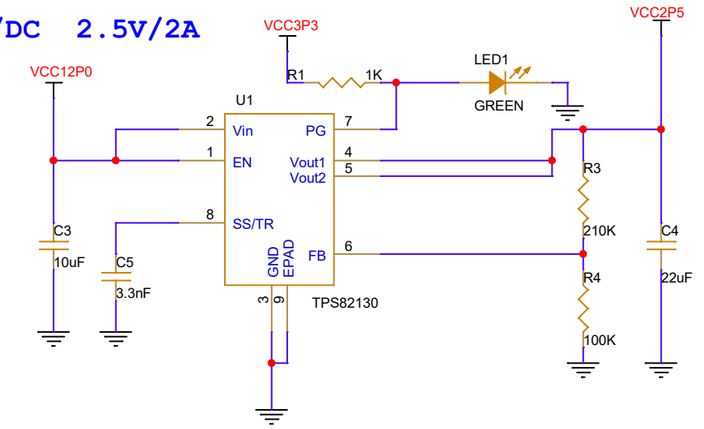



| | | |
|---|---|---|
| Title | DK_EDP_GW5ART-LV15MG132P_V1.0 | |
| Size A3 | Document Number POWER TREE | Rev V1.0 |
| Date: Wednesday, July 10, 2024 | Sheet 3 of 9 | |

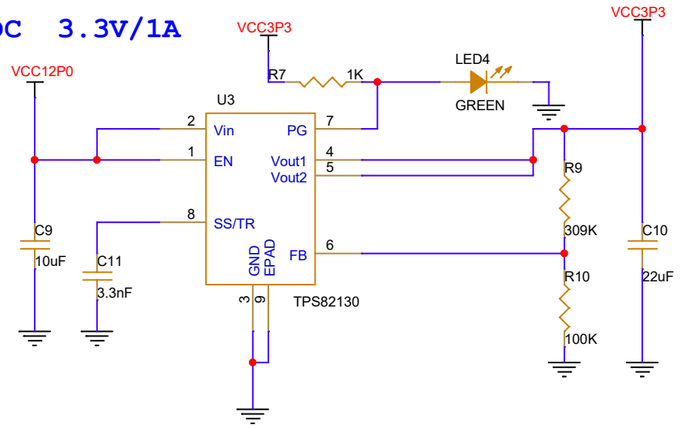
## 12V INPUT



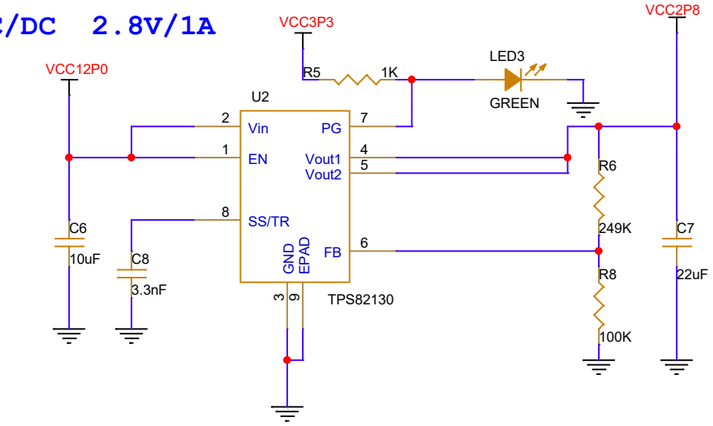

## DC/DC 2.5V/2A



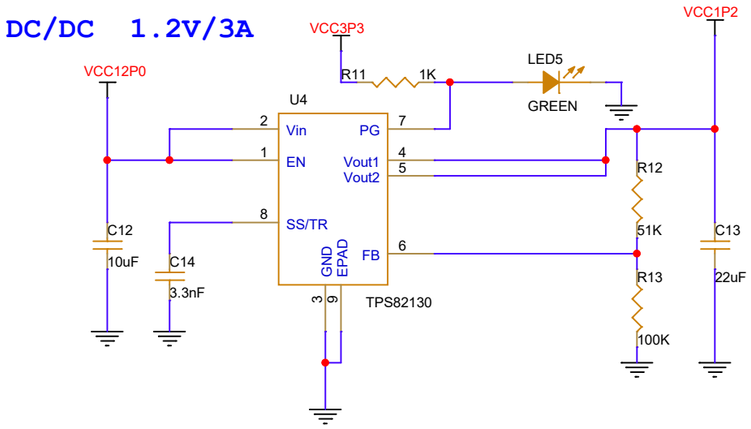

## DC/DC 3.3V/1A



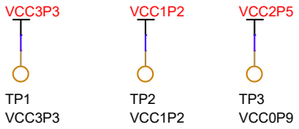

## DC/DC 2.8V/1A



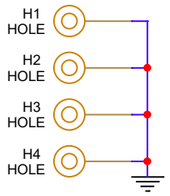

## DC/DC 1.2V/3A



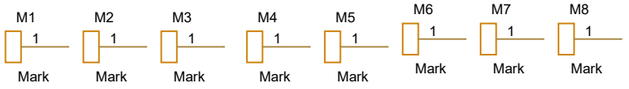

## Power Test Hole




## Mounting Hole

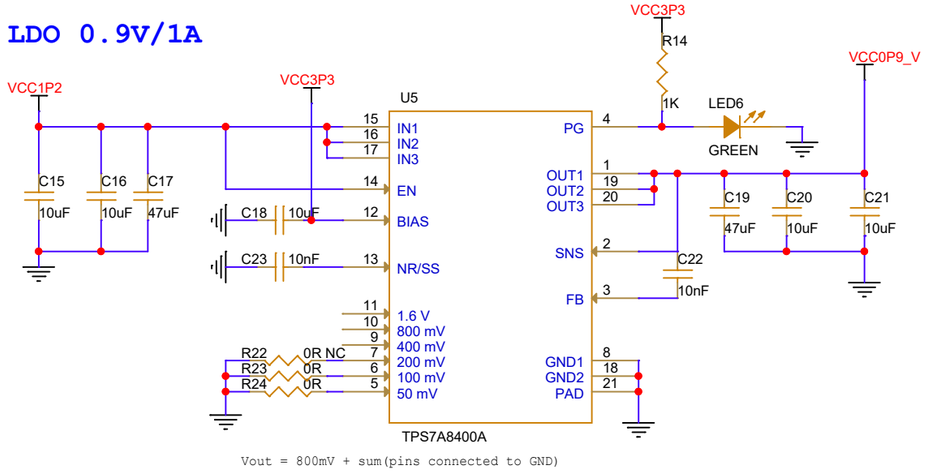



## Mark

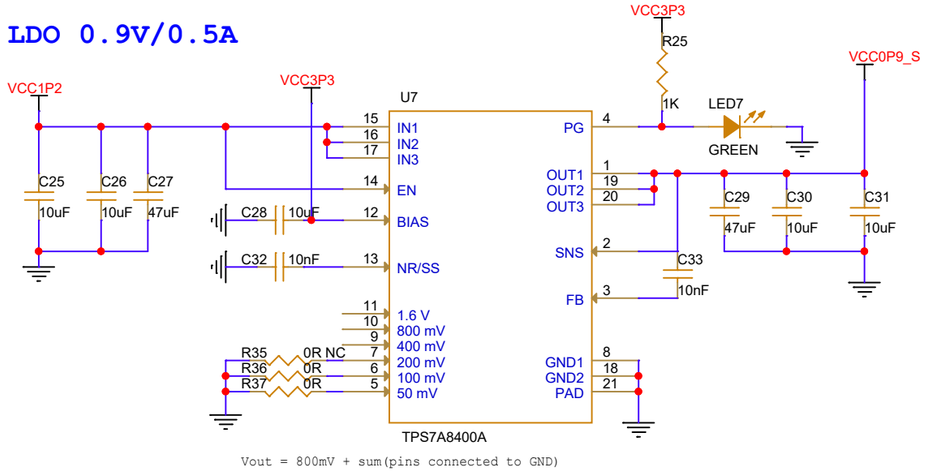



| | | |
|---|---|---|
| Title | DK_EDP_GW5ART-LV15MG132P_V1.0 | |
| Size A3 | Document Number POWER I | Rev V1.0 |
| Date: Wednesday, July 10, 2024 | Sheet 4 of 9 | |

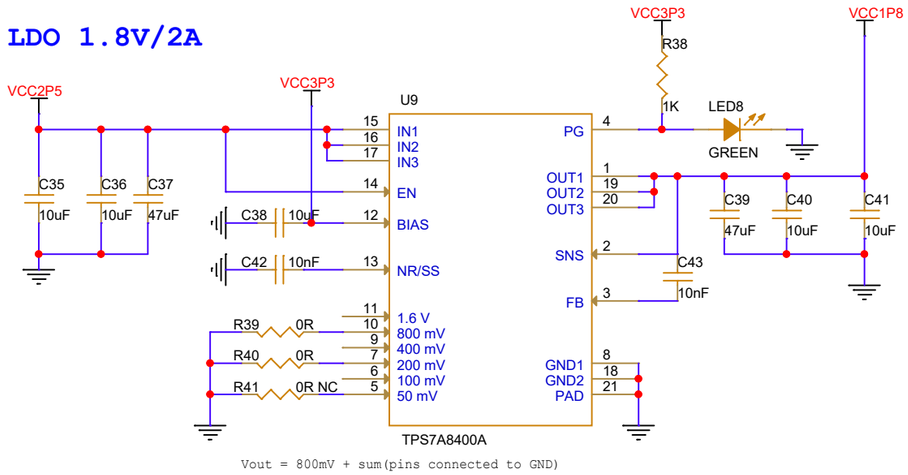
## LDO 0.9V/1A



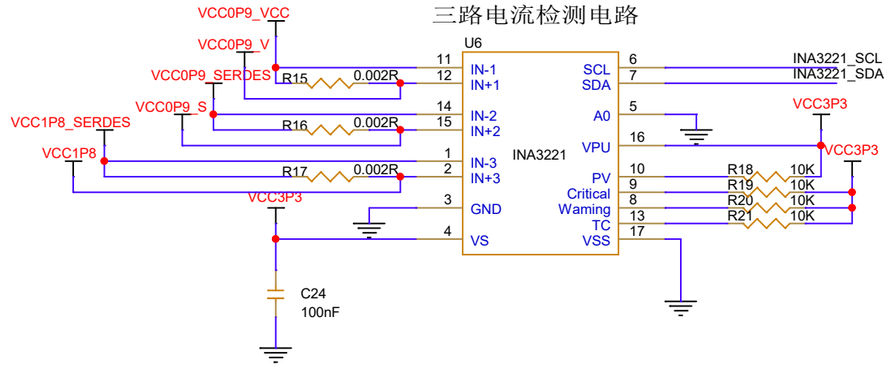

## LDO 0.9V/0.5A



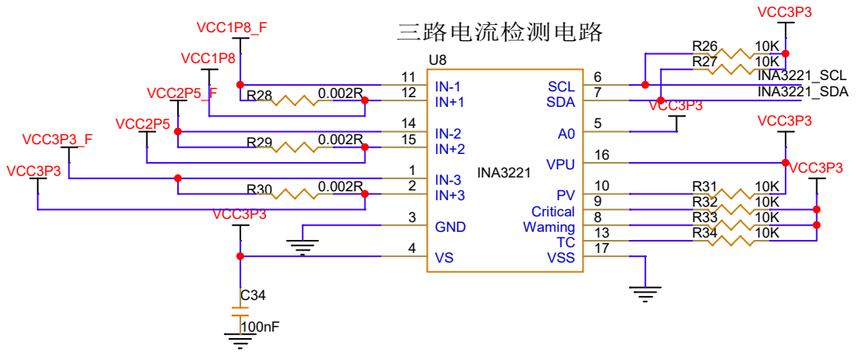

## LDO 1.8V/2A



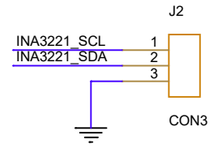

## 三路电流检测电路



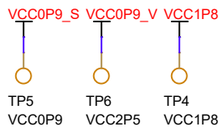

## 三路电流检测电路



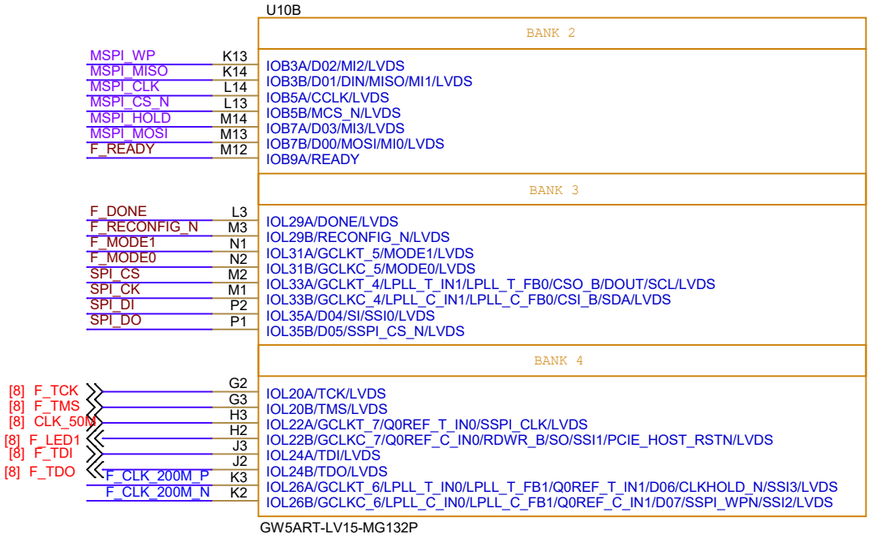

J2

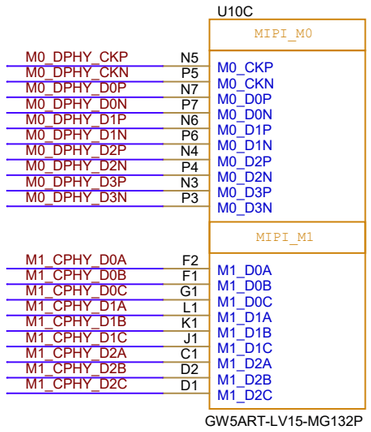



## Power Test Hole

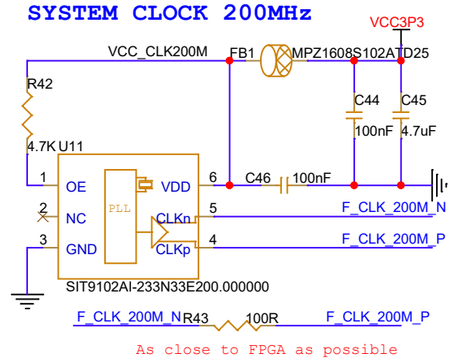



| | | | |
|---|---|---|---|
| Title | DK_EDP_GW5ART-LV15MG132P_V1.0 | | |
| Size A3 | Document Number POWER II | | Rev V1.0 |
| Date: Wednesday, July 10, 2024 | | Sheet 5 of 9 | |

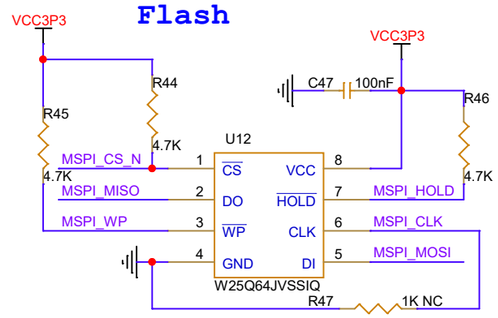


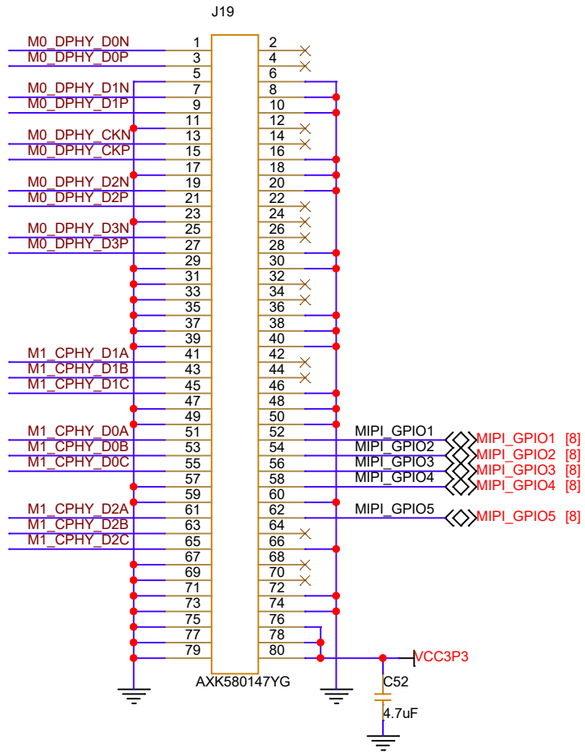

## SYSTEM CLOCK 200MHz



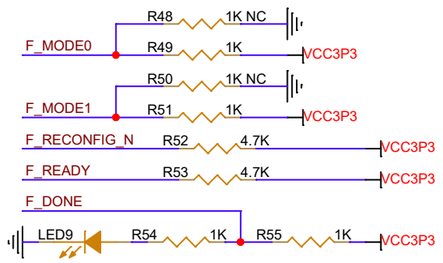

## Flash



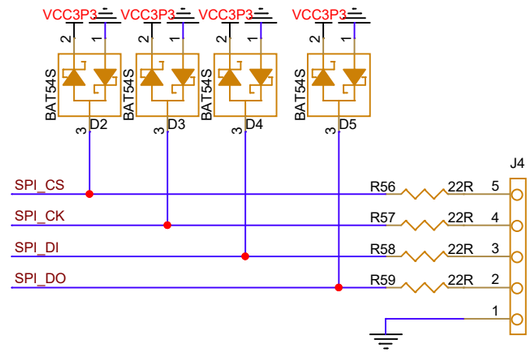

## MIPI



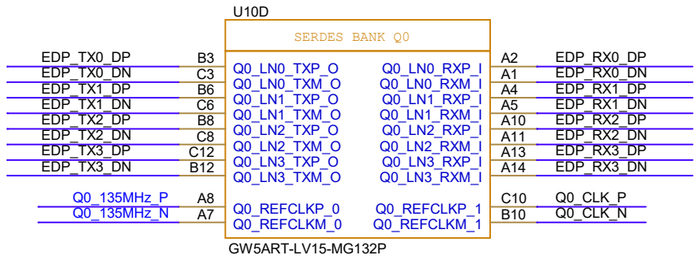

## FPGA CONFIG PIN



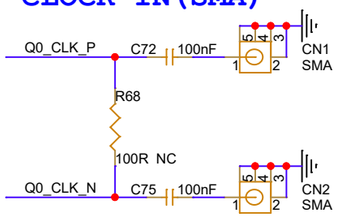

## SPI(Remote upgrade)



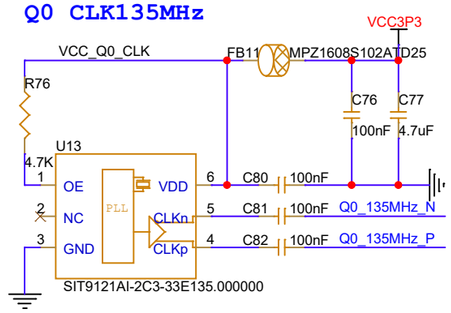

| | | |
|---|---|---|
| Title | DK_EDP_GW5ART-LV15MG132P_V1.0 | |
| Size A3 | Document Number MIPI/SPI/FLASH/CLOCK | Rev V1.0 |
| Date: Wednesday, July 24, 2024 | Sheet 6 of 9 | |



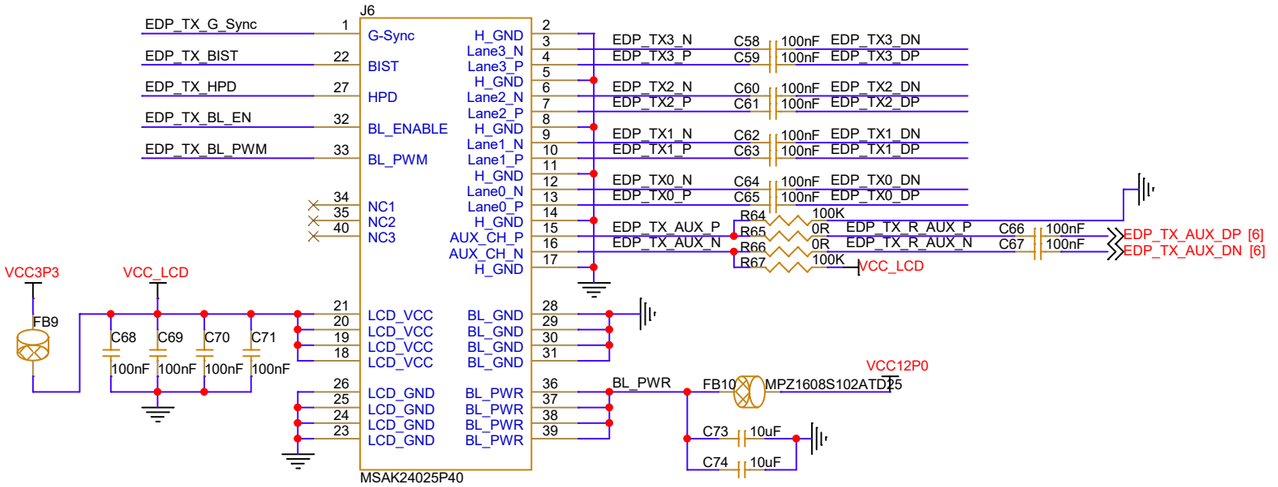

## CLOCK IN(SMA)



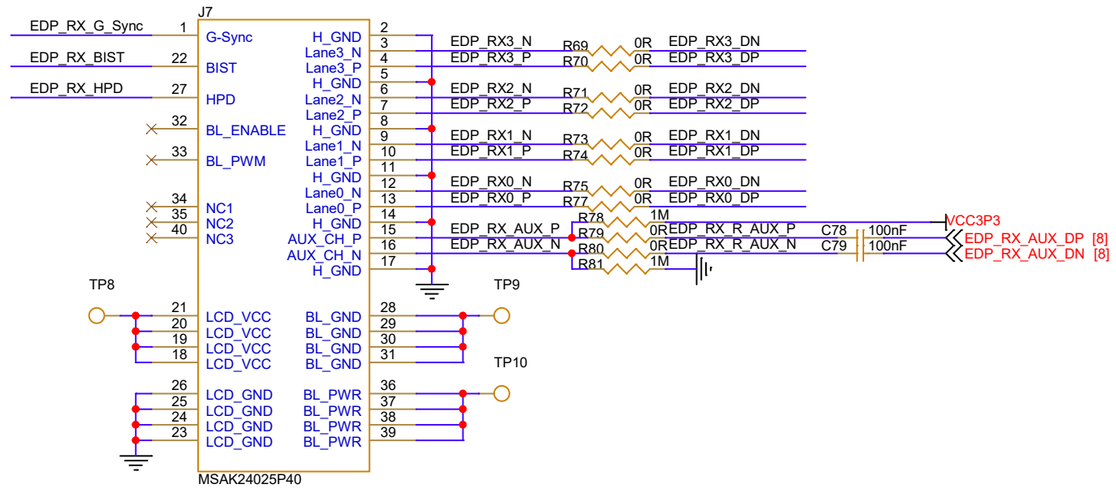

## Q0 CLK135MHz

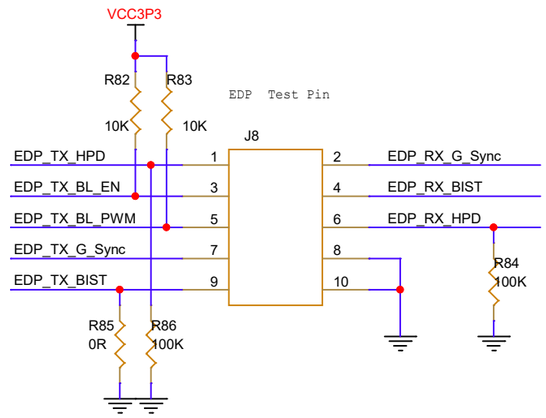



## EDP-TX




## EDP-RX




| | | |
|---|---|---|
| Title | DK_EDP_GW5ART-LV15MG132P_V1.0 | |
| Size A3 | Document Number EDP-RX/EDP-TX | Rev V1.0 |
| Date: Friday, July 12, 2024 | Sheet 7 of 9 | |

GW5ART:VCCIO1-> 1.8V (PSRAM)
GW5AT :VCCIO1 -> 2.5V/1.8V

U10A

BANK 1

| | | |
|---|---|---|
| MIPI_GPIO1 | M8 | IOB11A/DQ2 |
| MIPI_GPIO2 | P14 | IOB12A/LVDS/DQ2 |
| F_NRST | N14 | IOB12B/LVDS/DQ2 |
| DPHY_LVDS_D0P | P13 | IOB14A/D15/LVDS/DQ2 |
| DPHY_LVDS_D0N | N13 | IOB14B/D14/LVDS/DQ2 |
| DPHY_LVDS_D1P | N12 | IOB16A/LVDS/DQ2 |
| DPHY_LVDS_D1N | P12 | IOB16B/LVDS/DQ2 |
| DPHY_LVDS_D2P | P10 | IOB18A/D13/LVDS/DQ2 |
| DPHY_LVDS_D2N | N10 | IOB18B/D12/LVDS/DQ2 |
| DPHY_LVDS_D3P | N8 | IOB20A/LVDS/DQS2 |
| DPHY_LVDS_D3N | P8 | IOB20B/LVDS/DQS2 |
| DPHY_LVDS_CK0P | N11 | IOB22A/GCLKT_3/LVDS/DQ2 |
| DPHY_LVDS_CK0N | P11 | IOB22B/GCLKC_3/LVDS/DQ2 |
| [7] EDP_TX_AUX_DP | N9 | IOB24A/GCLKT_2/BPLL_T_IN0/BPLL_T_FB1/LVDS/DQ2 |
| [7] EDP_TX_AUX_DN | P9 | IOB24B/GCLKC_2/BPLL_C_IN0/BPLL_C_FB1/LVDS/DQ2 |
| MIPI_GPIO3 | J12 | IOB31A/DQ1 |
| MIPI_GPIO4 | H13 | IOB32A/GCLKT_1/BPLL_T_IN1/BPLL_T_FB0/LVDS/DQ1 |
| MIPI_GPIO5 | G13 | IOB32B/GCLKC_1/BPLL_C_IN1/BPLL_C_FB0/LVDS/DQ1 |
| DPHY_LVDS_CK1P | F13 | IOB34A/GCLKT_0/LVDS/DQ1 |
| DPHY_LVDS_CK1N | E13 | IOB34B/GCLKC_0/LVDS/DQ1 |
| DPHY_LVDS_D4P | D13 | IOB36A/LVDS/DQ1 |
| DPHY_LVDS_D4N | C13 | IOB36B/LVDS/DQ1 |
| DPHY_LVDS_D5P | D14 | IOB39A/D11/LVDS/DQ1 |
| DPHY_LVDS_D5N | C14 | IOB39B/D10/LVDS/DQ1 |
| DPHY_LVDS_D6P | J13 | IOB41A/LVDS/DQS1 |
| DPHY_LVDS_D6N | J14 | IOB41B/LVDS/DQS1 |
| DPHY_LVDS_D7P | F14 | IOB43A/D09/LVDS/DQ1 |
| DPHY_LVDS_D7N | E14 | IOB43B/D08/LVDS/DQ1 |
| [7] EDP_RX_AUX_DP | H14 | IOB45A/LVDS/DQ1 |
| [7] EDP_RX_AUX_DN | G14 | IOB45B/EMCCLK/LVDS/DQ1 |

GW5ART-LV15-MG132P

| | | | |
|---|---|---|---|
| DPHY_LVDS_D4N | R87 | 100R NC | DPHY_LVDS_D4P |
| DPHY_LVDS_D5N | R88 | 100R NC | DPHY_LVDS_D5P |
| DPHY_LVDS_D6N | R90 | 100R NC | DPHY_LVDS_D6P |
| DPHY_LVDS_D7N | R91 | 100R NC | DPHY_LVDS_D7P |
| DPHY_LVDS_CK1N | R92 | 100R NC | DPHY_LVDS_CK1P |
| DPHY_LVDS_D3N | R93 | 100R NC | DPHY_LVDS_D3P |
| DPHY_LVDS_D2N | R94 | 100R NC | DPHY_LVDS_D2P |
| DPHY_LVDS_D1N | R96 | 100R NC | DPHY_LVDS_D1P |
| DPHY_LVDS_D0N | R98 | 100R NC | DPHY_LVDS_D0P |
| DPHY_LVDS_CK0N | R99 | 100R NC | DPHY_LVDS_CK0P |

## USB<->JTAG(FPGA Download)

VCC3P3

C88 100nF, C89 100nF, C83 100nF, C84 100nF, C85 100nF

U14

| | | |
|---|---|---|
| 40 | VREGIN | |
| 39 | VCCD | |
| 38 | VCCCORE | |
| 37 | VCCA | |
| 6 | DM | USB_D- |
| 7 | DP | USB_D+ |
| 34 | RESETn | R95 10K |
| 5 | REF | R97 12K |
| 45 | EECS | |
| 44 | EECLK | |
| 43 | EEDATA | |
| 1 | XCSI | C90 22pF |
| 2 | XCSO | C91 22pF |
| 42 | TEST | |
| 3, 8, 12, 24, 46 | VPHY, VPLL, VCCIO, VCCIO, VCCIO | |
| 4, 9, 41, 10, 11, 22, 23, 35, 36, 47, 48, 49 | AGND, AGND, AGND, GND, GND, GND, GND, GND, GND, GND, GND, GND | |

FT232HQ

| | |
|---|---|
| 13 | ADBUS0 |
| 14 | ADBUS1 |
| 15 | ADBUS2 |
| 16 | ADBUS3 |
| 17 | ADBUS4 |
| 18 | ADBUS5 |
| 19 | ADBUS6 |
| 20 | ADBUS7 |
| 21 | ACBUS0 |
| 25 | ACBUS1 |
| 26 | ACBUS2 |
| 27 | ACBUS3 |
| 28 | ACBUS4 |
| 29 | ACBUS5 |
| 30 | ACBUS6 |
| 31 | ACBUS7 |
| 32 | ACBUS8 |
| 33 | ACBUS9 |

R89 4.7K

F_TCK [6], F_TDI [6], F_TDO [6], F_TMS [6]

C86 100nF, C87 100nF, VCC3P3

X3: XIN, GND2, GND1, XOUT — X322512MSB4SI

USB_VCC5

U15: VCC, IO2, NC, IO1, GND — TPD2E001DRLR

C92 10nF

J10: VCC, D-, D+, ID, GND — MIN-USB

C93 10nF, R100 100K

## DPHY/LVDS

J20

| | | | |
|---|---|---|---|
| DPHY_LVDS_D3P | 1 | 2 | DPHY_LVDS_D3N |
| DPHY_LVDS_D2P | 3 | 4 | DPHY_LVDS_D2N |
| DPHY_LVDS_CK0P | 5 | 6 | DPHY_LVDS_CK0N |
| DPHY_LVDS_D1P | 7 | 8 | DPHY_LVDS_D1N |
| DPHY_LVDS_D0P | 9 | 10 | DPHY_LVDS_D0N |
| | 11 | 12 | |
| | 13 | 14 | |
| | 15 | 16 | |
| | 17 | 18 | |
| | 19 | 20 | |

## DPHY/LVDS

J21

| | | | |
|---|---|---|---|
| DPHY_LVDS_D4P | 1 | 2 | DPHY_LVDS_D4N |
| DPHY_LVDS_D5P | 3 | 4 | DPHY_LVDS_D5N |
| DPHY_LVDS_CK1P | 5 | 6 | DPHY_LVDS_CK1N |
| DPHY_LVDS_D6P | 7 | 8 | DPHY_LVDS_D6N |
| DPHY_LVDS_D7P | 9 | 10 | DPHY_LVDS_D7N |
| | 11 | 12 | |
| | 13 | 14 | |
| | 15 | 16 | |
| | 17 | 18 | |
| | 19 | 20 | |

VCC3P3, R104 1K, LED10, Q1 S8050, [7] F_LED1, F_LED1, R105 1K

## OSC

VCC3P3, FB12, C96 10nF

X4: IN, VCC, GND, OUT — OT322550MJBA4SL

R106 22R CLK_50M → CLK_50M

50MHz

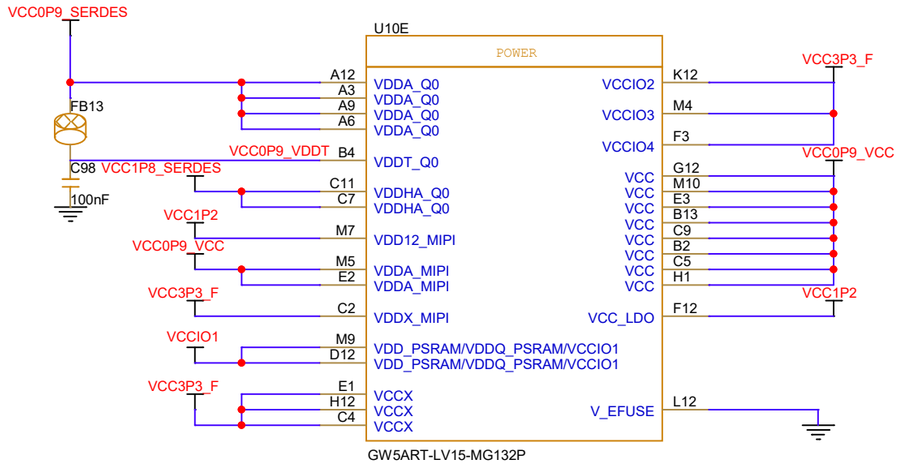
## RST

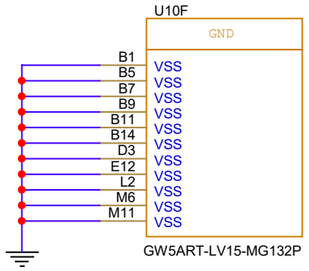
VCCIO1, R103 100K

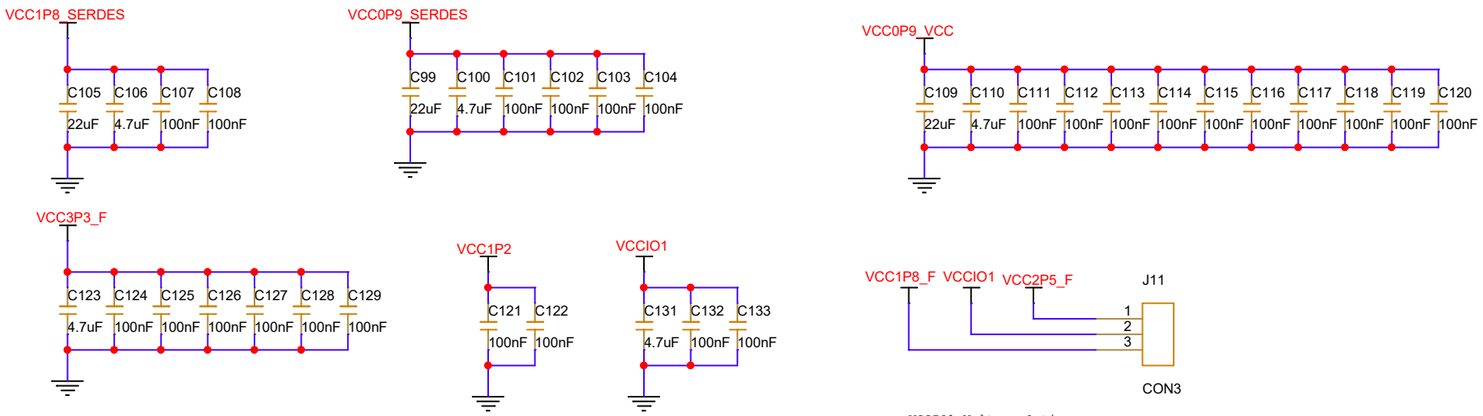
KEY1: K1, K2, KO1, KO2 — TL1105F160Q

F_NRST, C97 10uF

| | |
|---|---|
| Title | DK_EDP_GW5ART-LV15MG132P_V1.0 |
| Size A3 | Document Number LVDS/MIPI/USB-JTAG |
| Rev | V1.0 |
| Date: | Wednesday, July 24, 2024 |
| Sheet | 8 of 9 |




| | | |
|---|---|---|
| Title | DK_EDP_GW5ART-LV15MG132P_V1.0 | |
| Size A3 | Document Number FPGA-POWER&GND | Rev V1.0 |
| Date: Friday, July 12, 2024 | Sheet 9 of 9 | |