

5

4

3

2

1

D

D

C

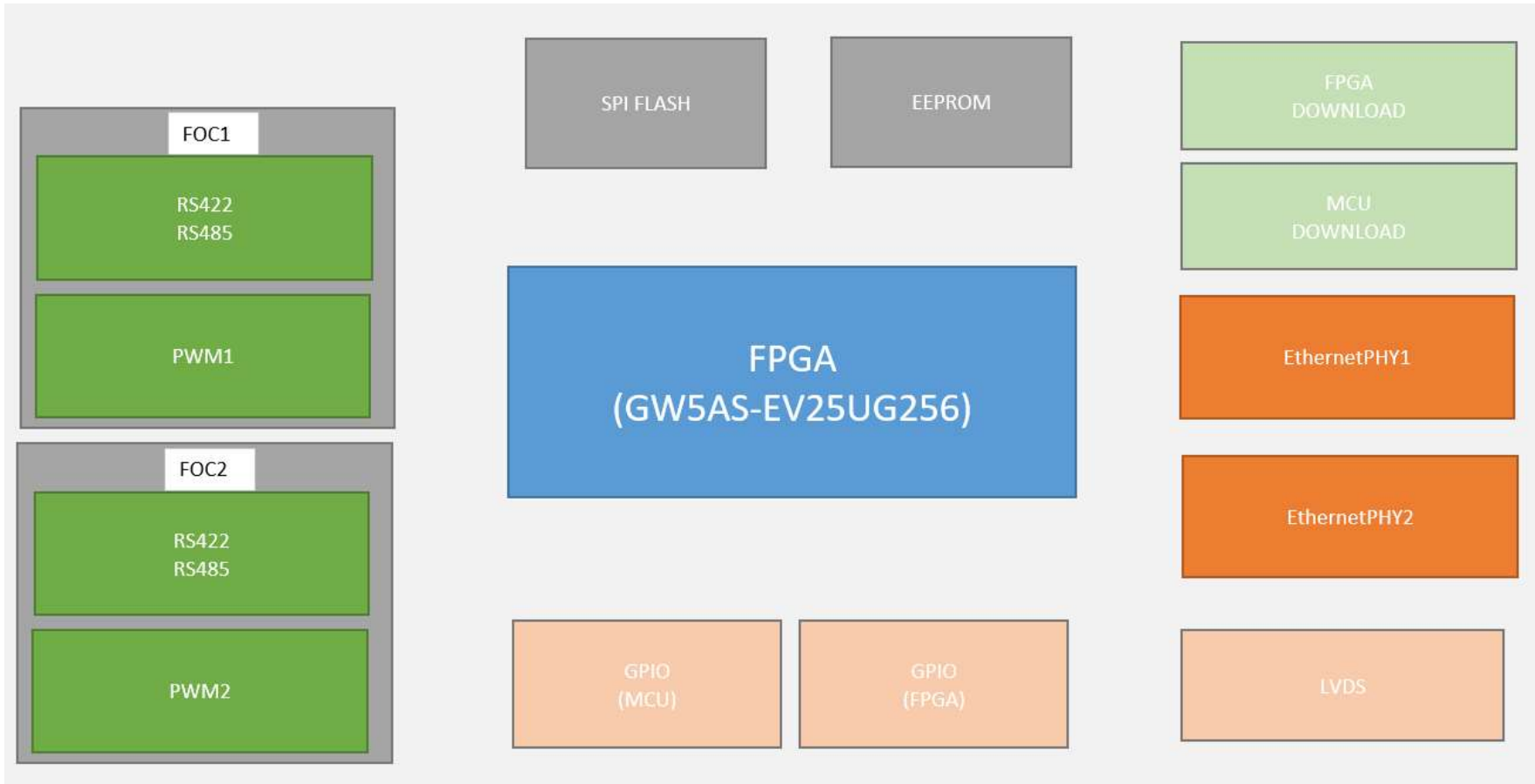
C

B

B

A

A



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A3	0	1.1
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D

D

C

C

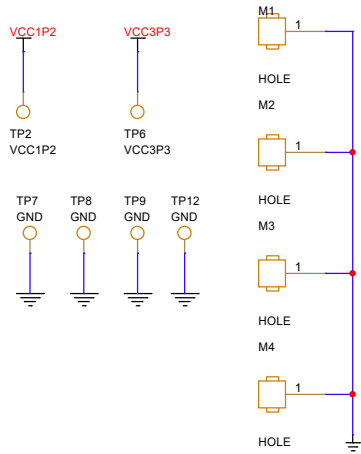
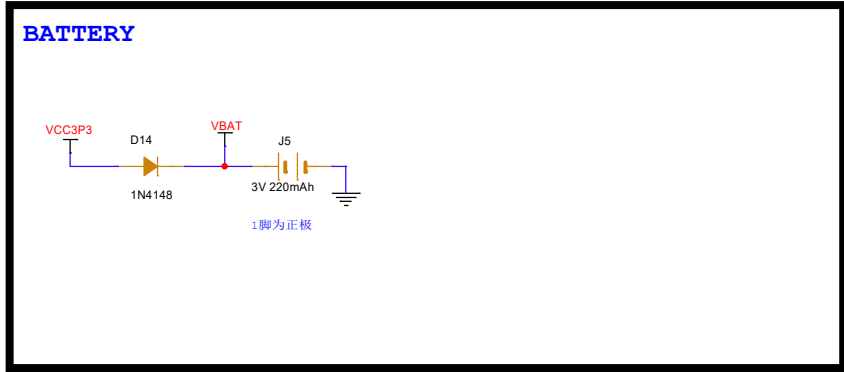
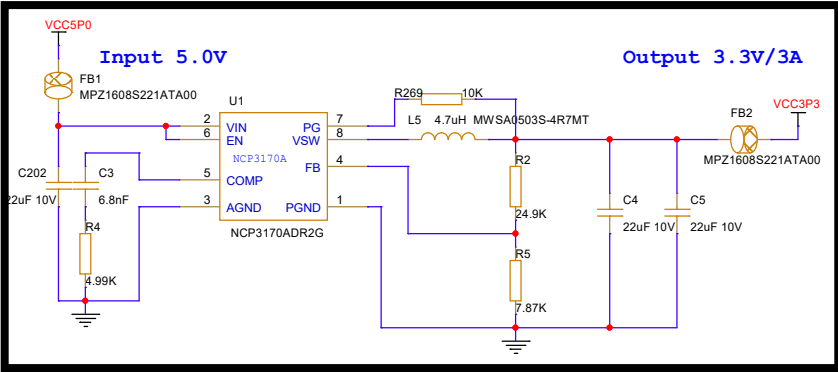
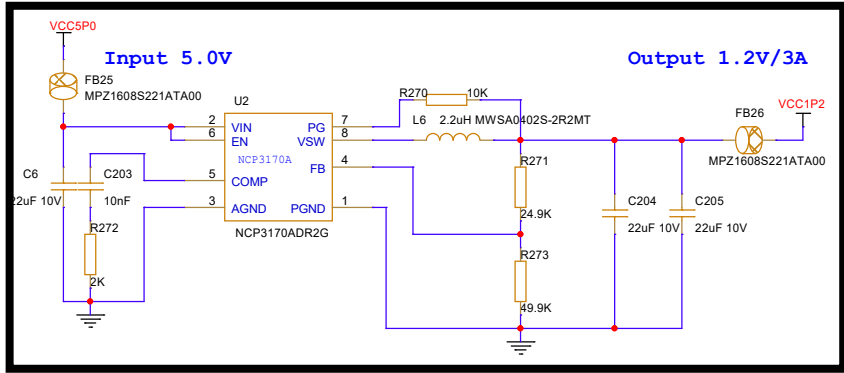
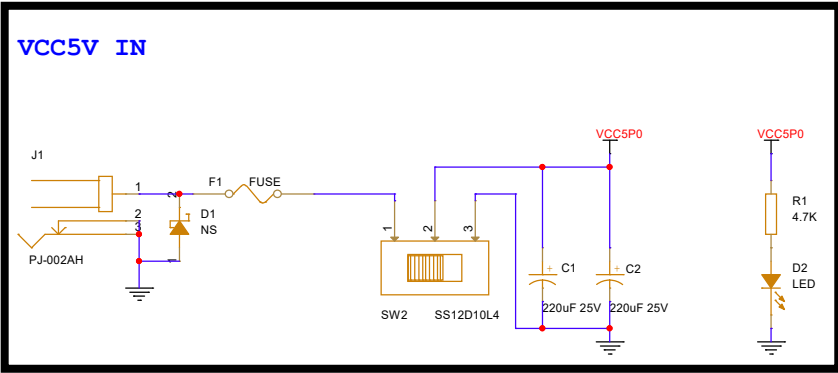
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B

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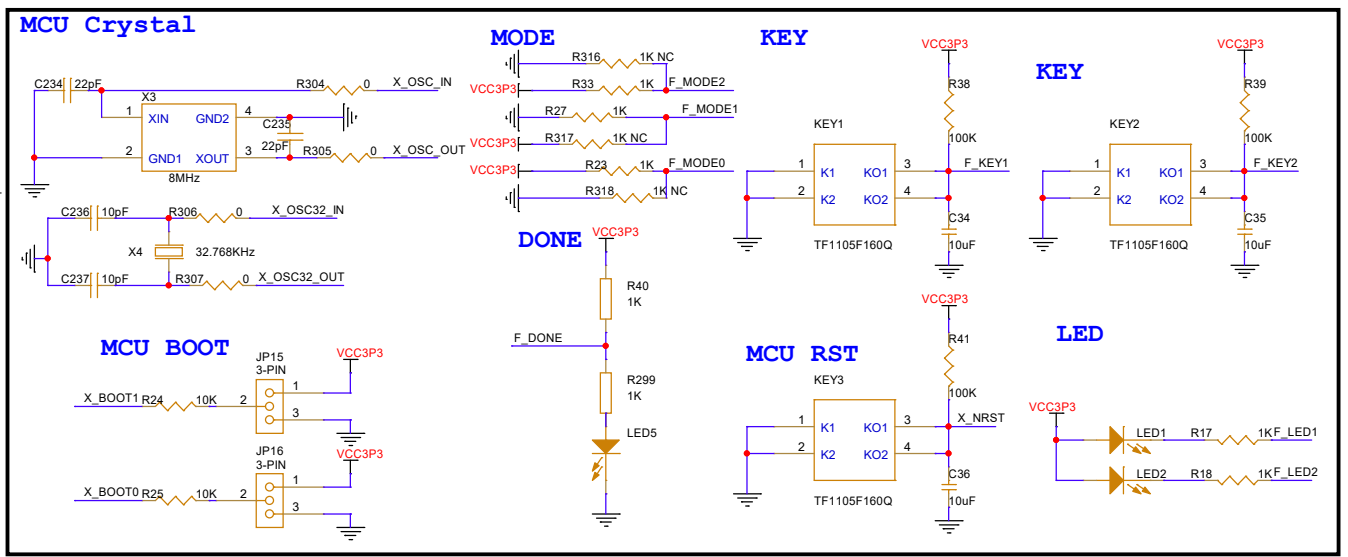
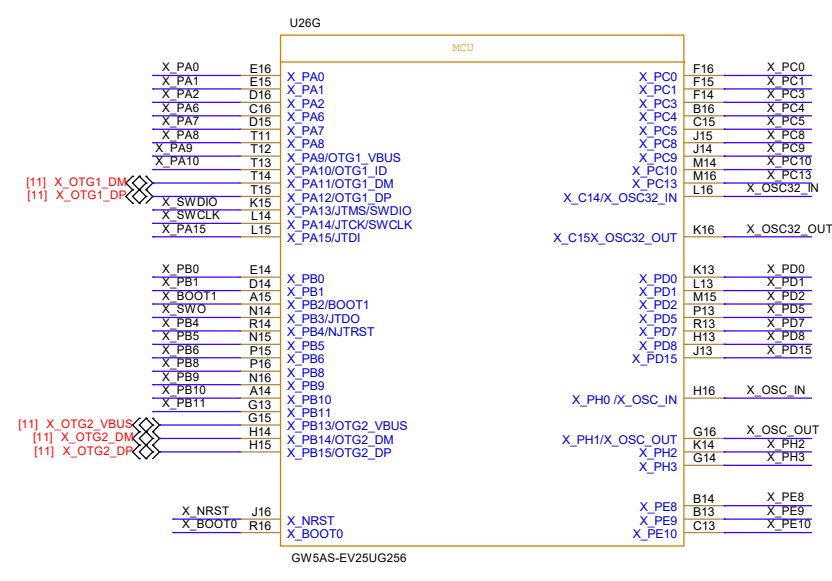
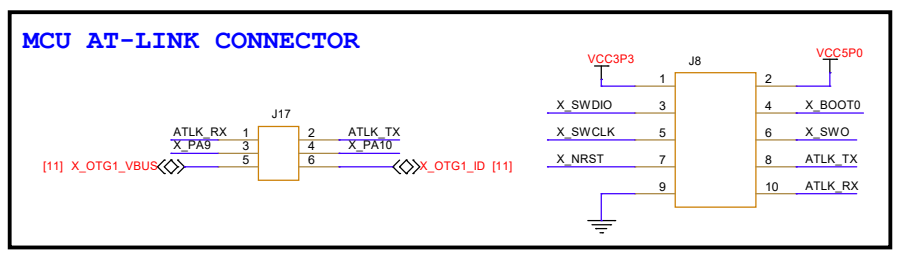
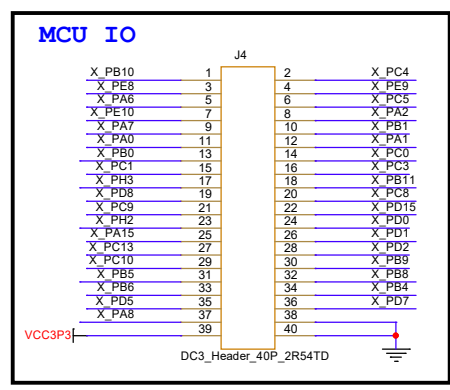
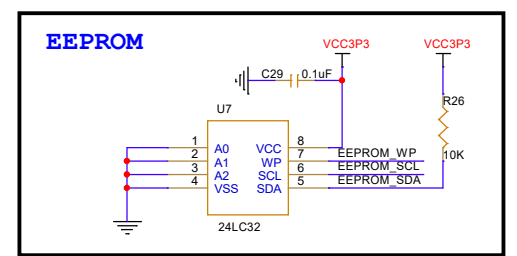
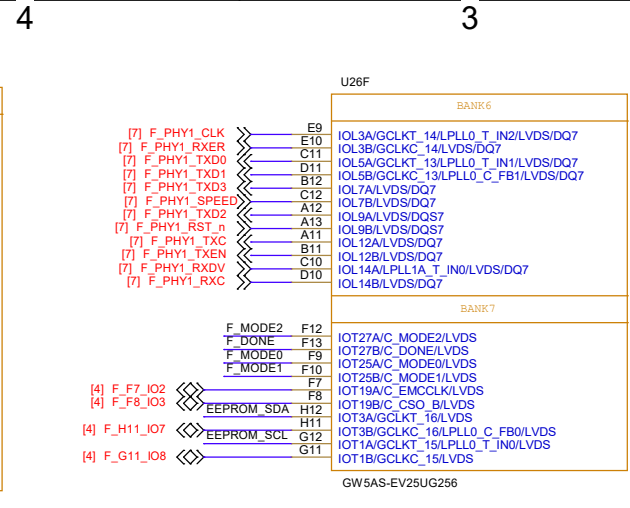
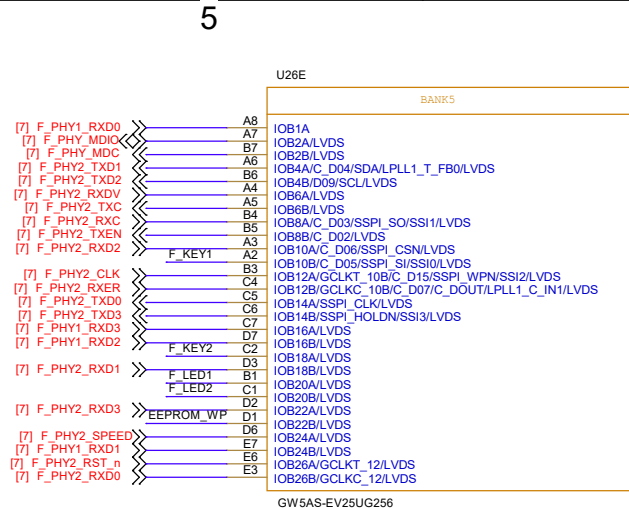
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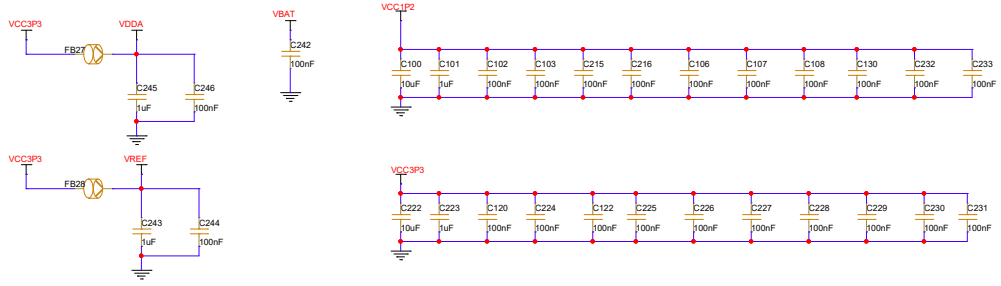
SCHEMATIC	CONTENT	PAGE
BLOCK DIAGRAM	BLOCK DIAGRAM	01
COVER PAGE	COVER PAGE	02
POWER	DC5V/DC3.3V,DC5V/DC1.2V	03
FPGA	FPGA,SPI FLASH,EEPROM,OSC,AT-Link	04-06
ETHERNET PHY	PHY1,PHY2	07
FOC1	RS422,RS485,PWM	08
FOC2	RS422,RS485,PWM	09
USB-LVDS	FPGA DOWNLOAD,MCU USB,LVDS	10



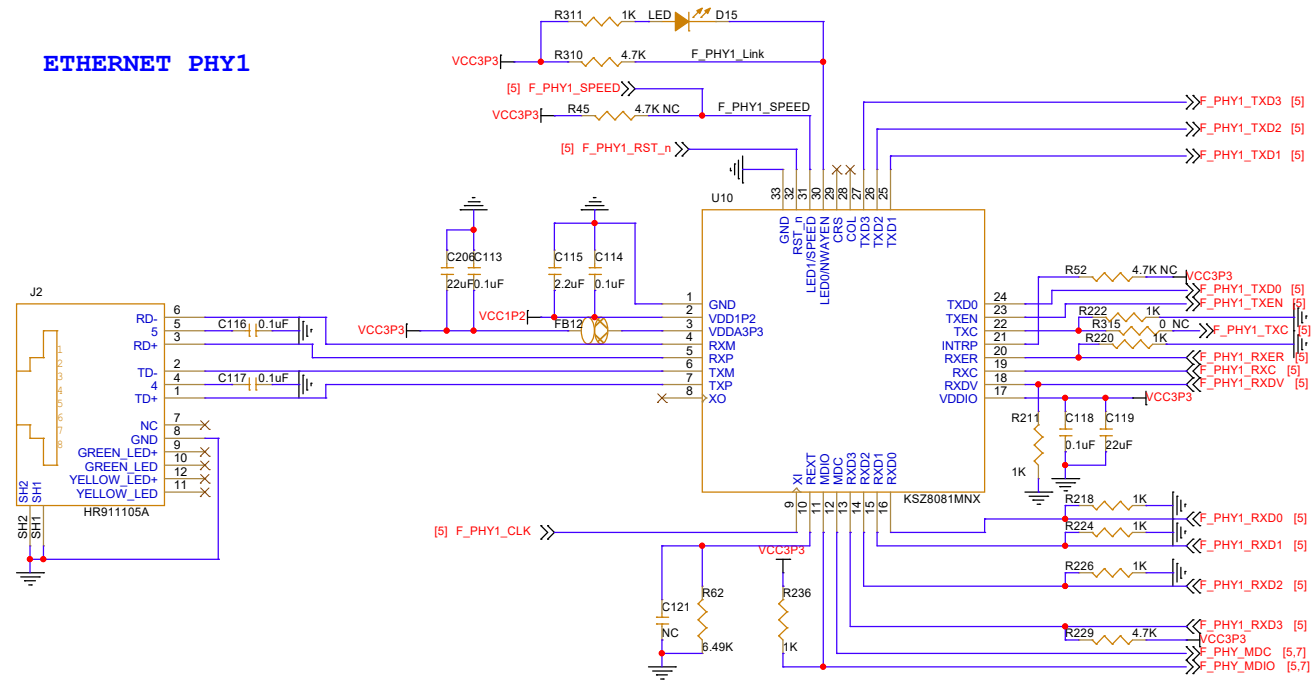
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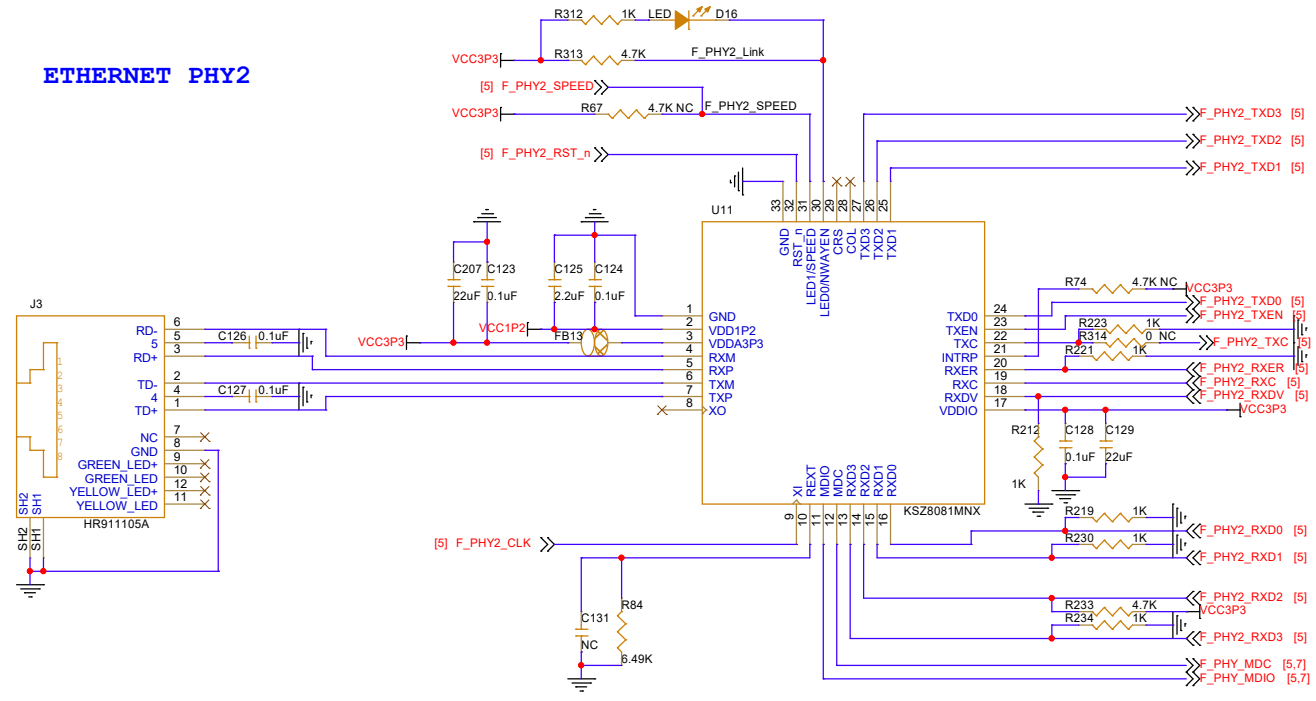




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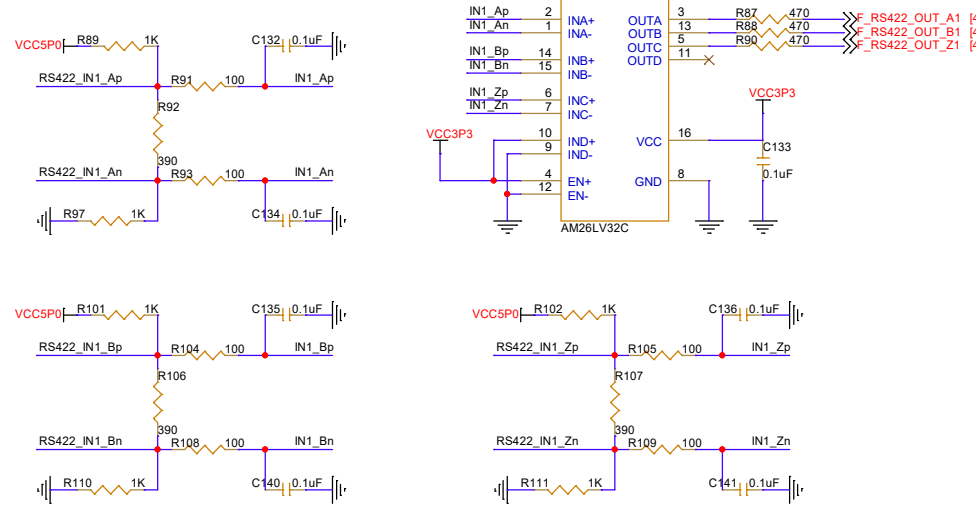


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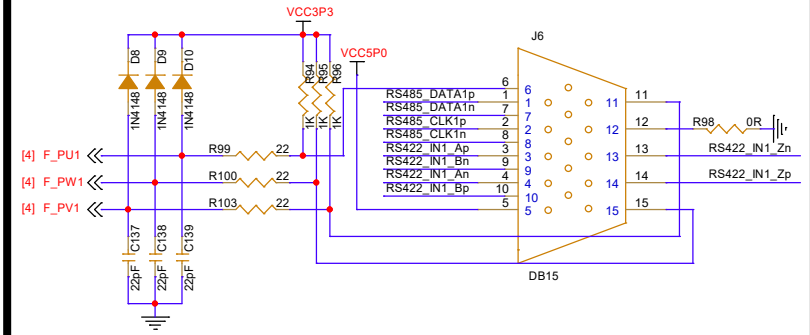


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Size	Document Number	Rev
A3	ETHERNET PHY	1.1
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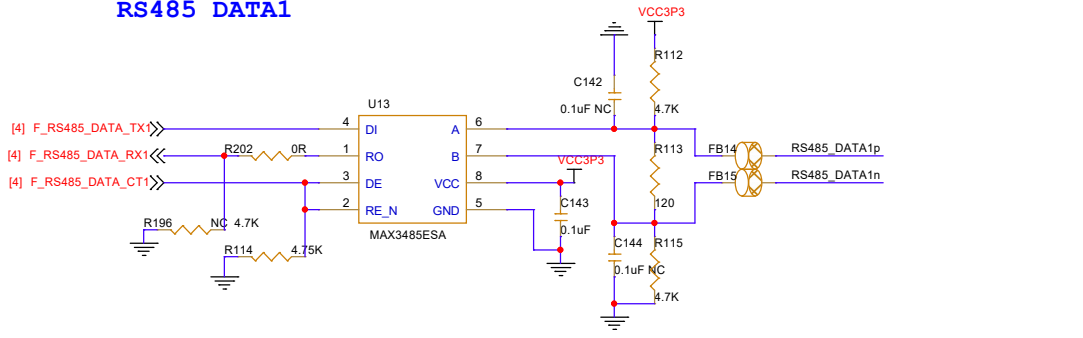
### RS422 1



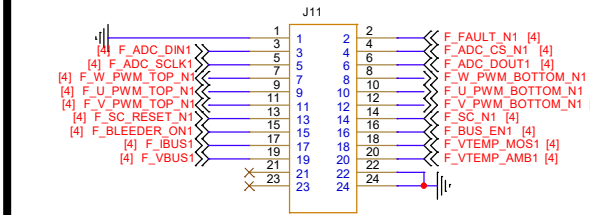
### MOTOR1



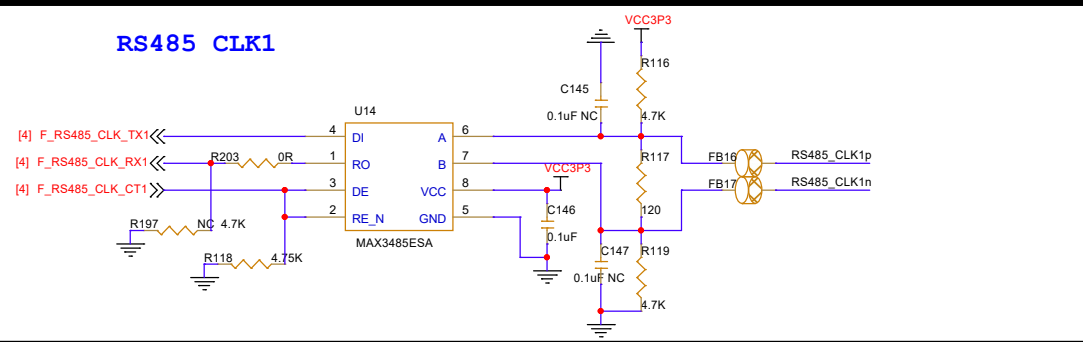
### RS485 DATA1



### PWM1

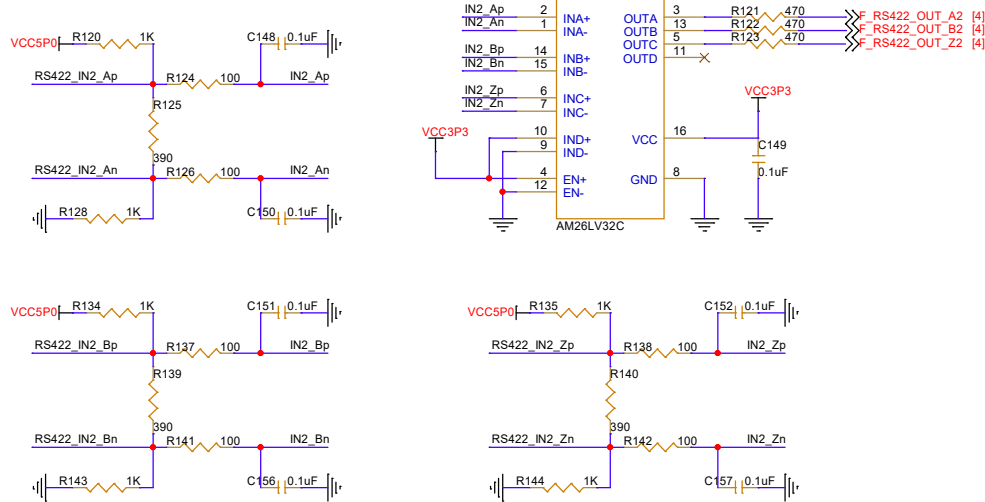


### RS485 CLK1

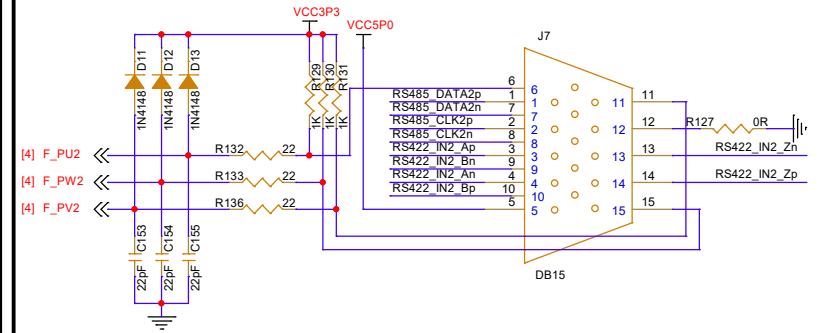




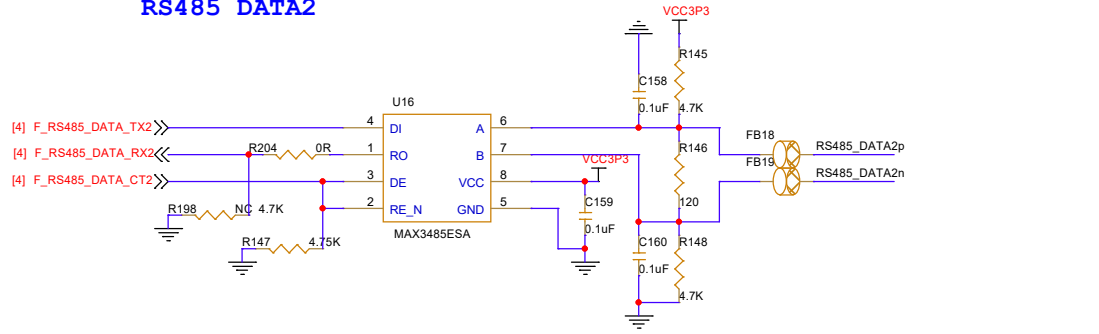
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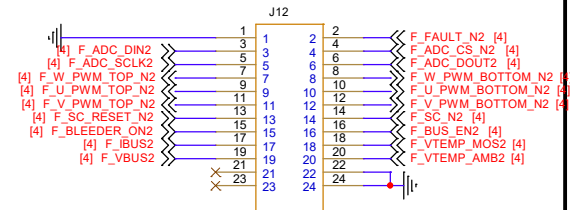
### MOTOR2



### RS485 DATA2



### PWM2



### RS485 CLK2

