

FMC HPC BANK2,4,5 Q1 IO:141

34 LA pairs (LA00-LA33)  
24 HA pairs (HA00-HA23)  
2 Differential Clock  
3 GPIO

SFP\*2

POWER

Clock 50M BANK3 IO:1  
Differential Clock 200M  
BANK7,Q1 IO:4  
MGT SMA  
BANKQ1 IO:2  
SMA Clock  
BANKQ0 IO:2

GW5AT-138-PPBGA676

Switches LEDs, Buttons  
BANK3

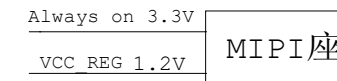
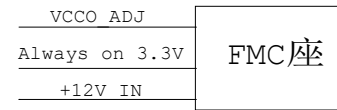
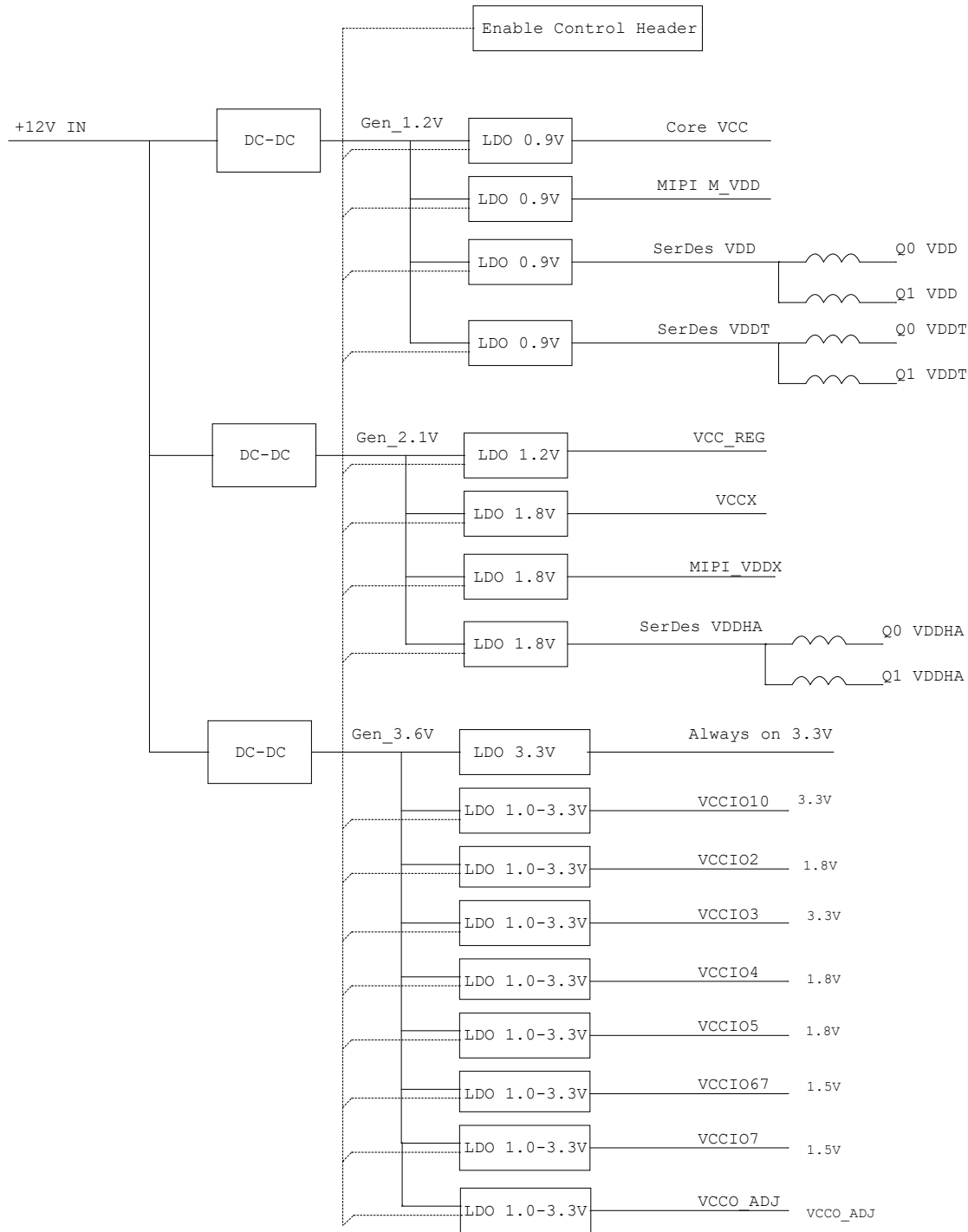
PCIe x4 Edge Connector  
BANK Q0 IO:20

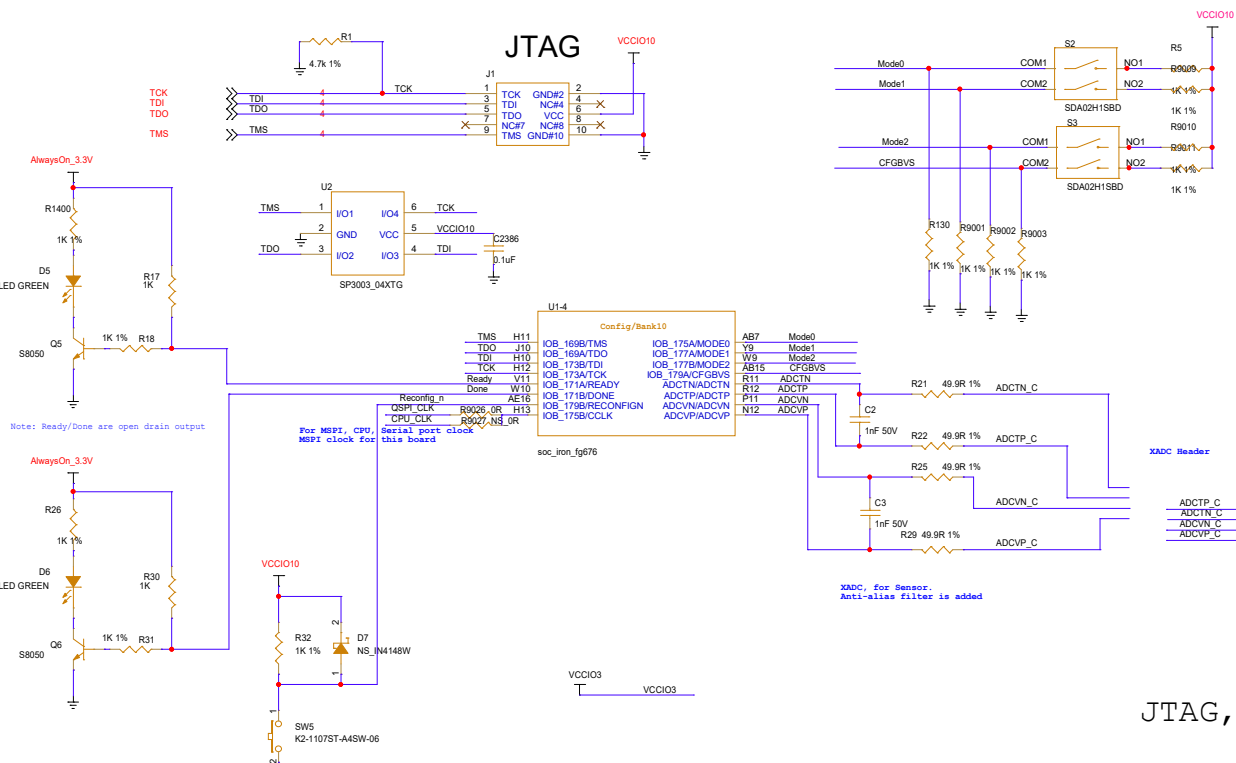
JTAG ,SSPI, MSPI, CPU,  
SERIAL, I2C  
BANK10,3 IO:21

16bit 512M \*2 DDR3  
BANK6,7 IO:60

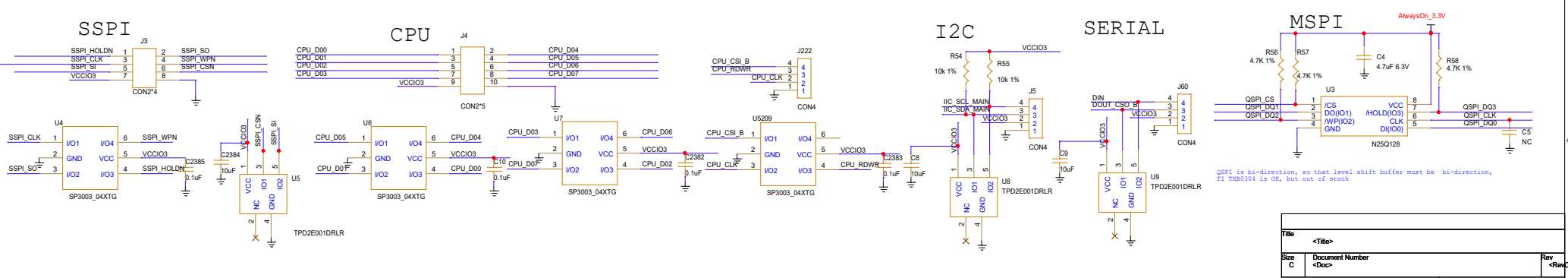
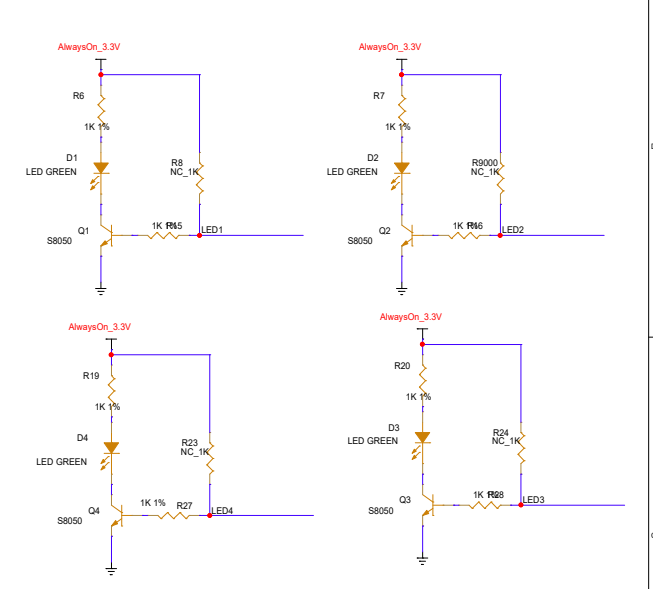
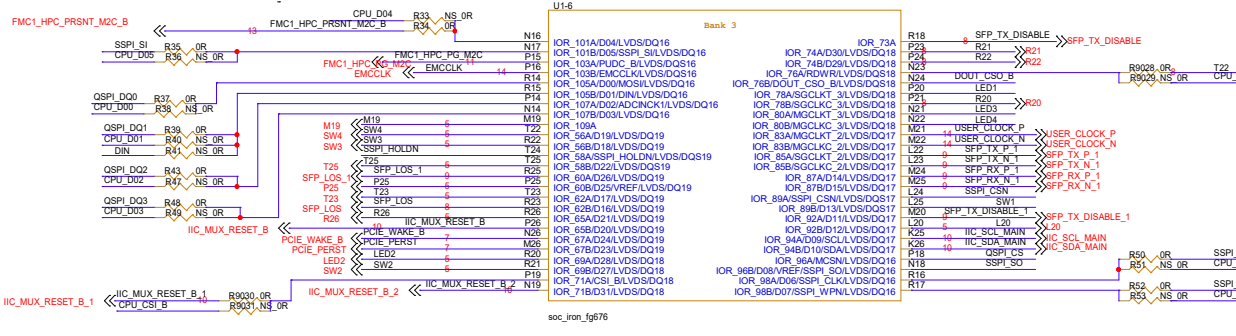
MIPI RX&TX  
MIPI BANK IO:20

# Power Tree





### JTAG, SSPI, MSPI, CPU, SERIAL, I2C

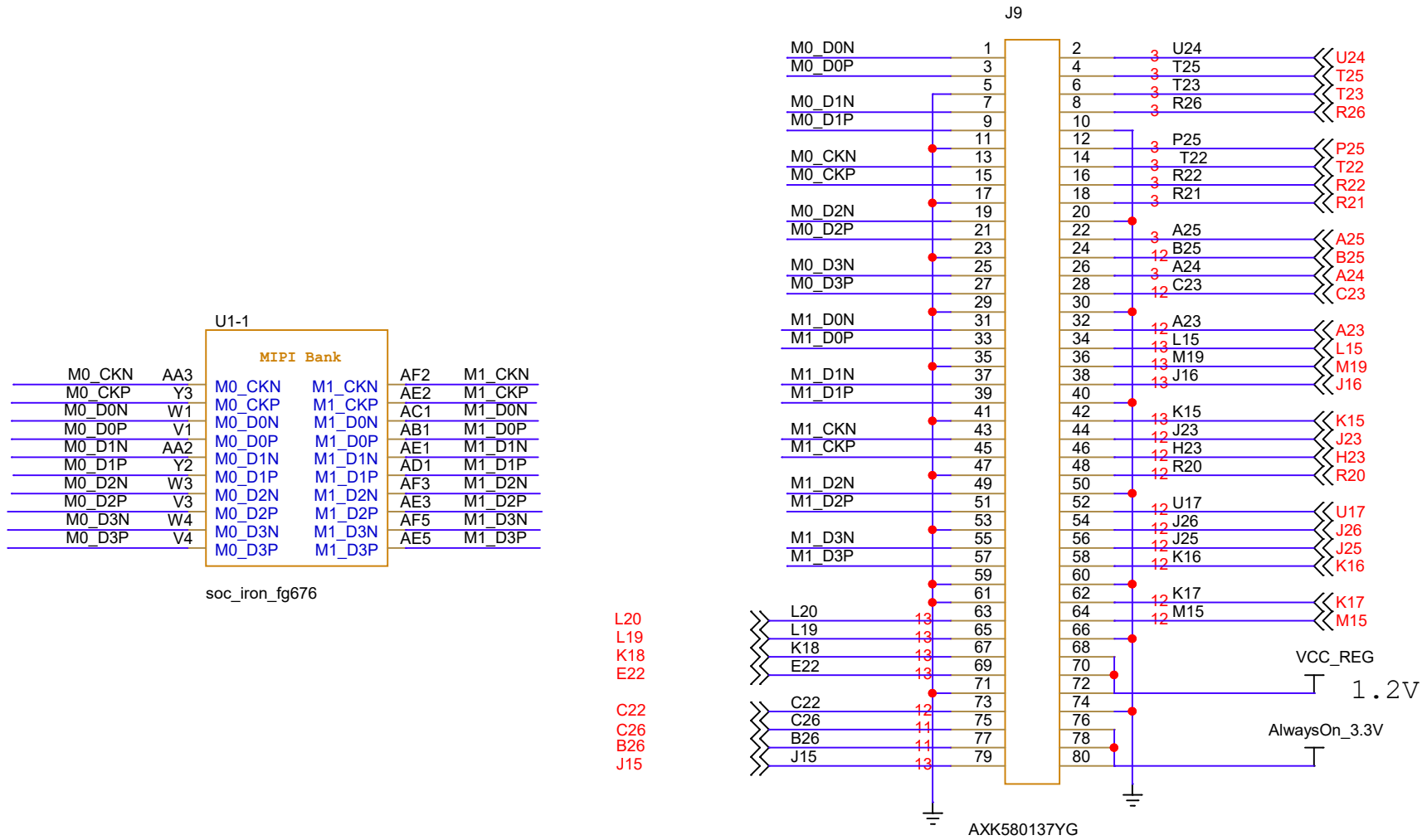


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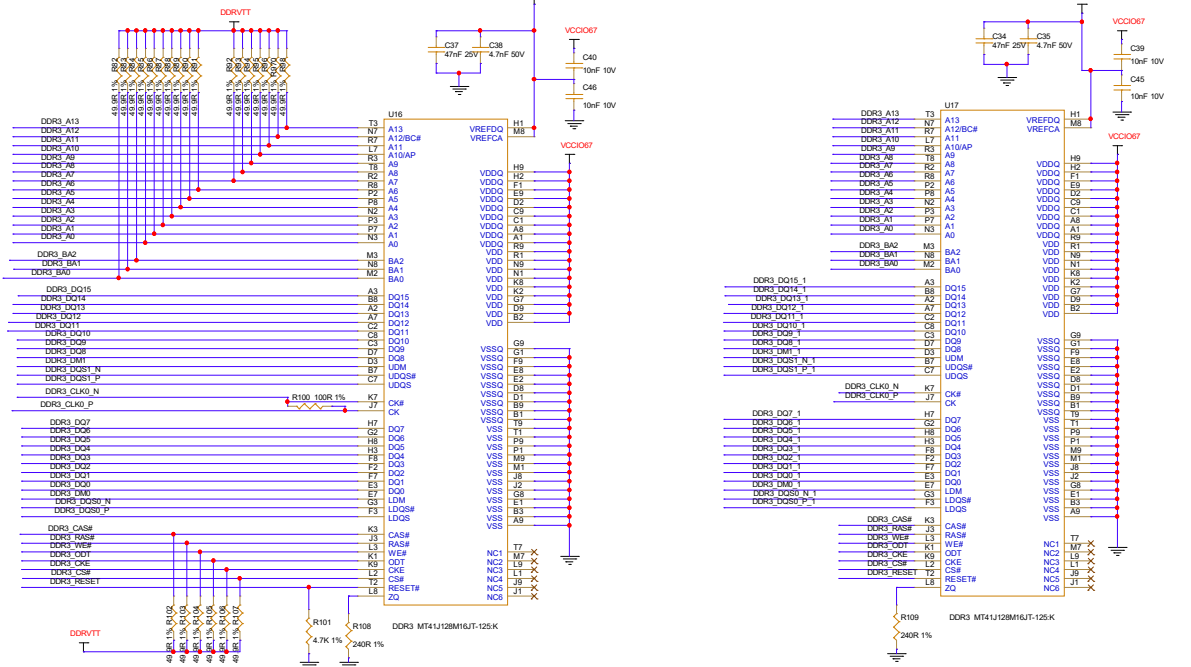
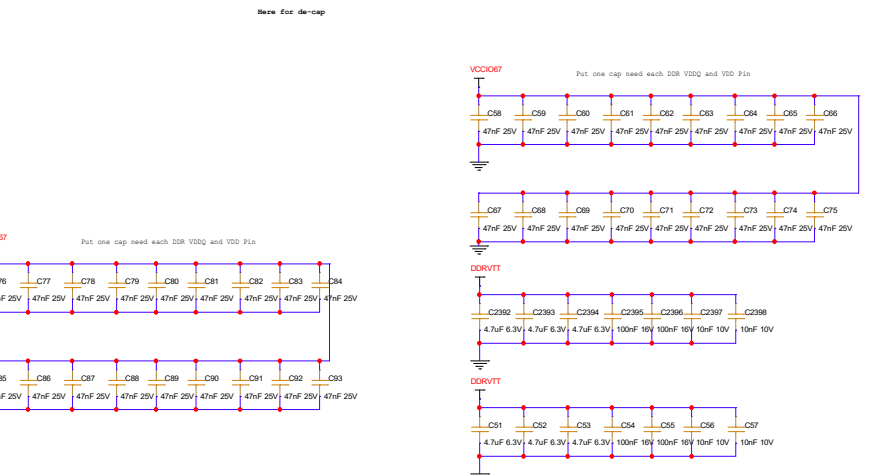
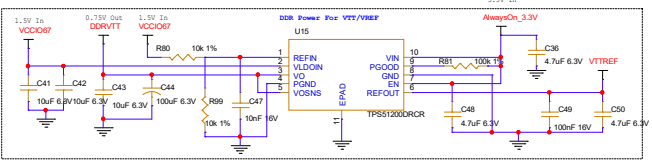
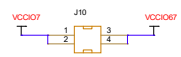
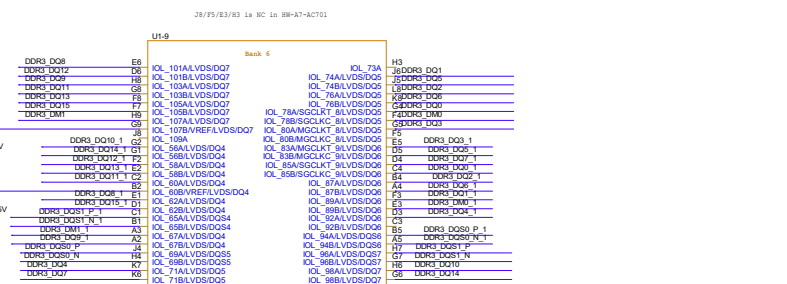
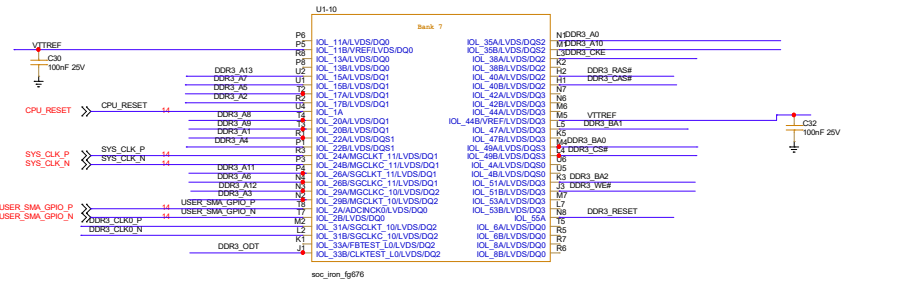
MIPI bank is for MIPI RX hard macro.  
 As the board is for characterization purpose, SMA connector is used.  
 MIPI bank only have SMA connectors. Length match rules:  
 1. M0/M1 length match for each intra group  
 2. M0 and M1 inter group length match is nice to have

# MIPI



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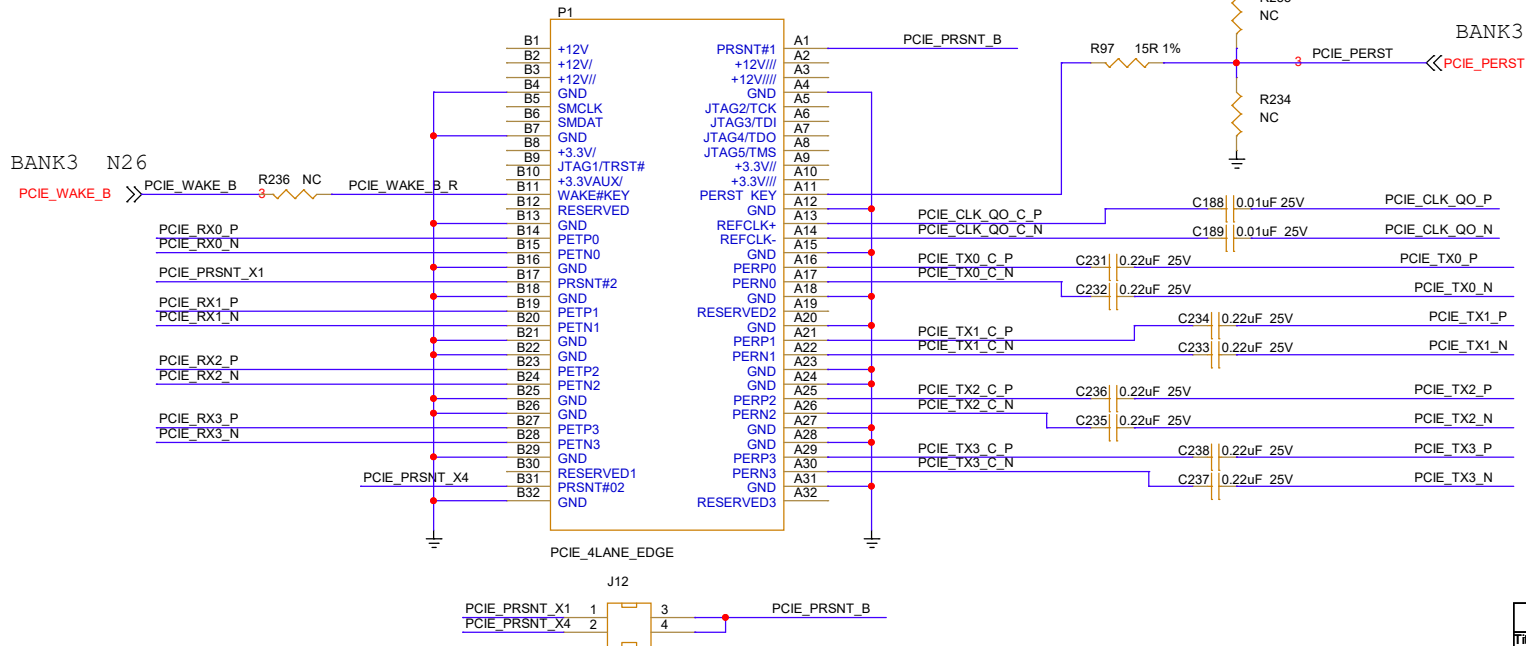
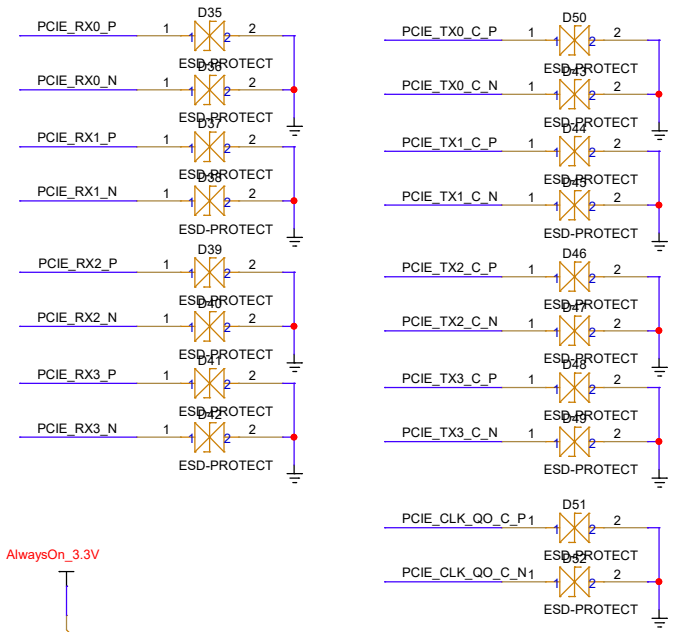
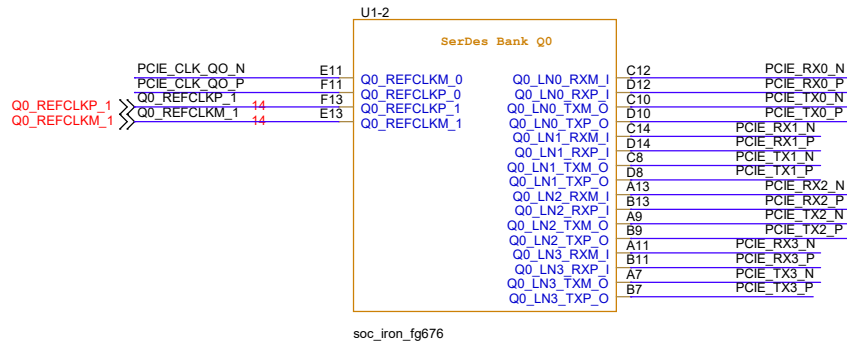
# DDR3\*2



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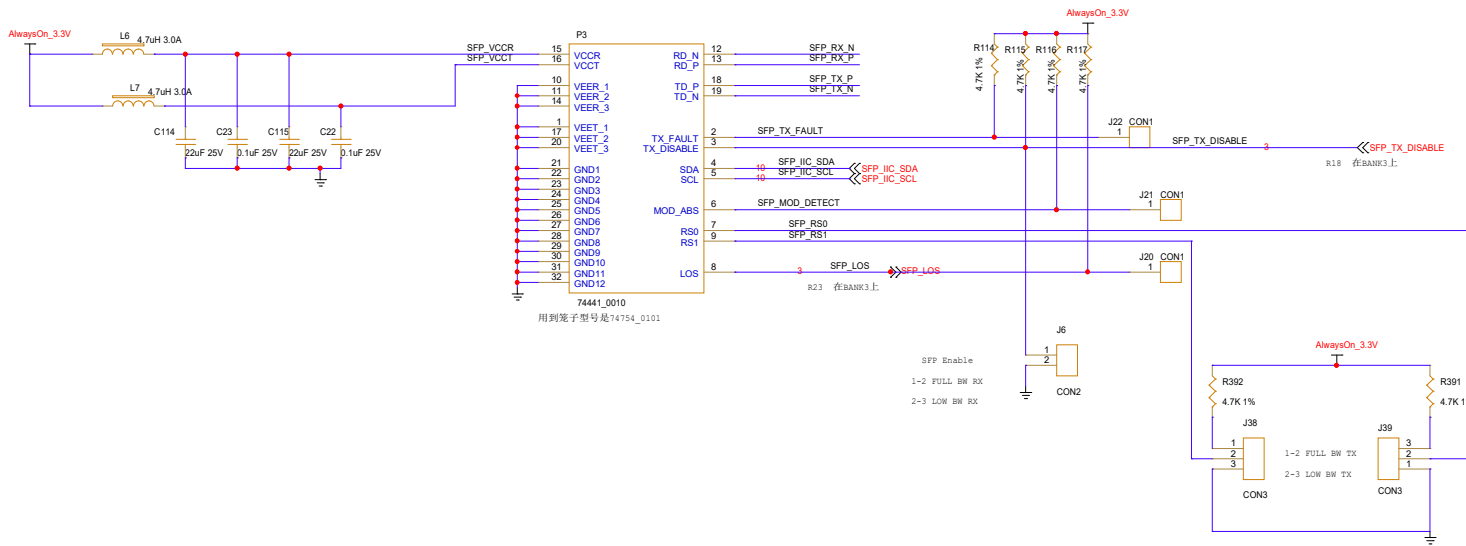
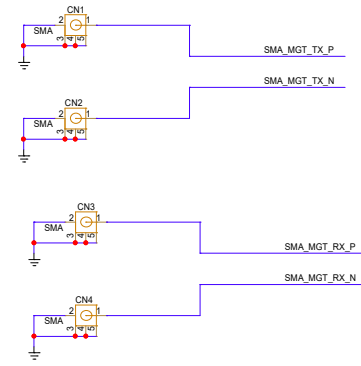
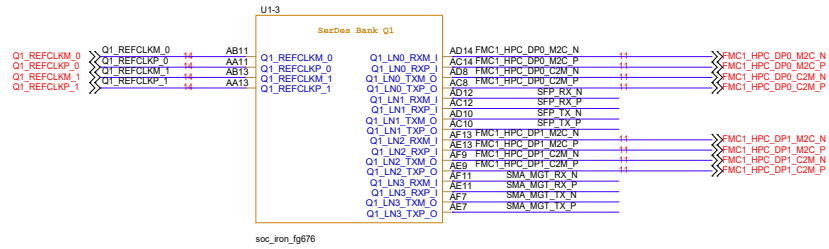
# PCIe

SerDes to SMP pin order could be swapped.



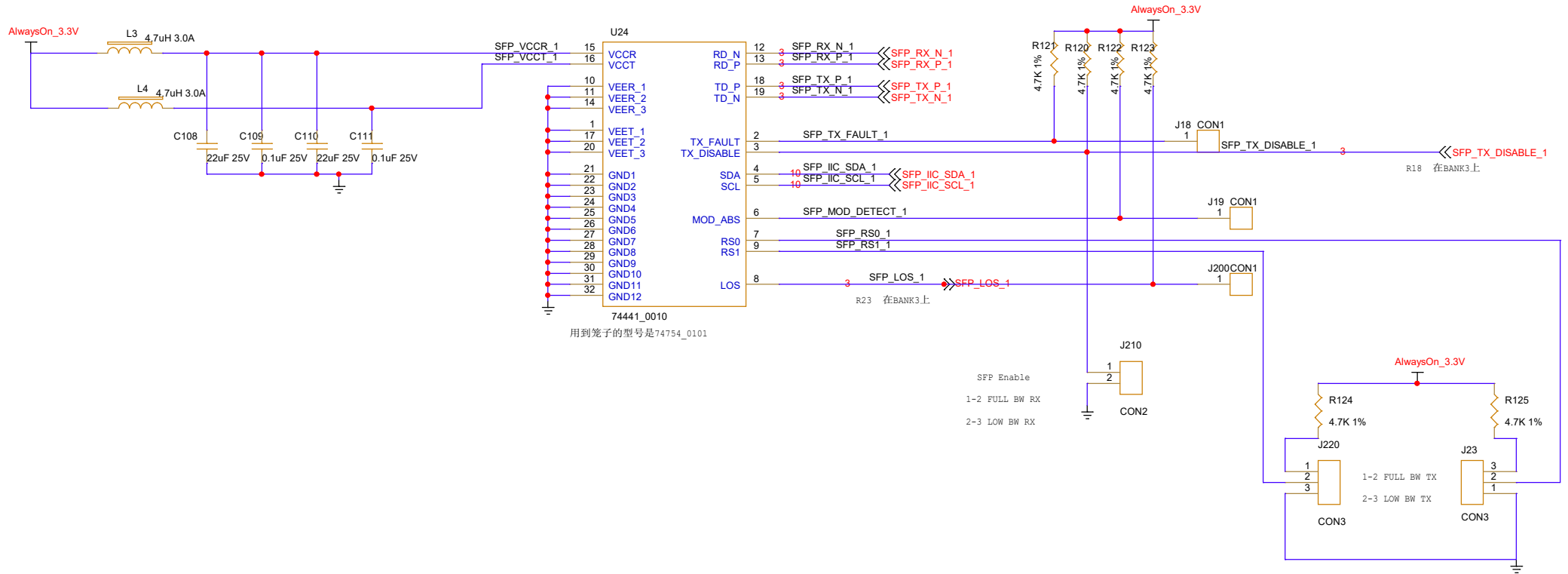
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# SFP



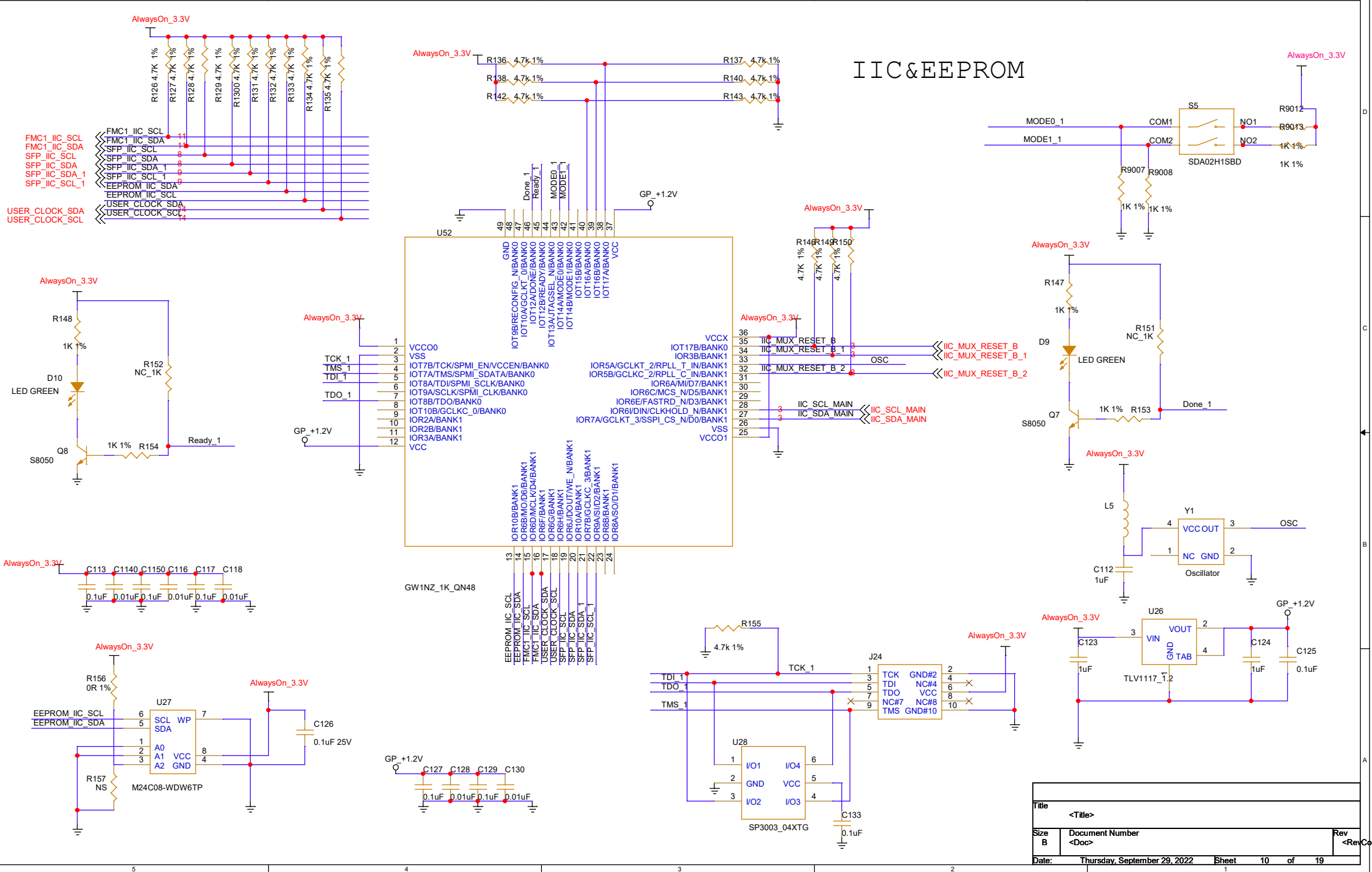


# SFP



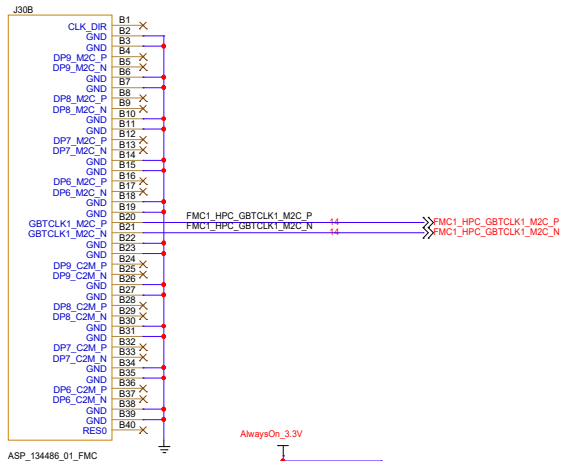
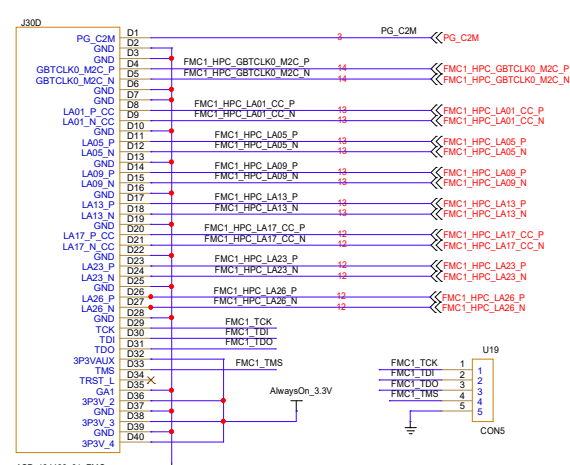
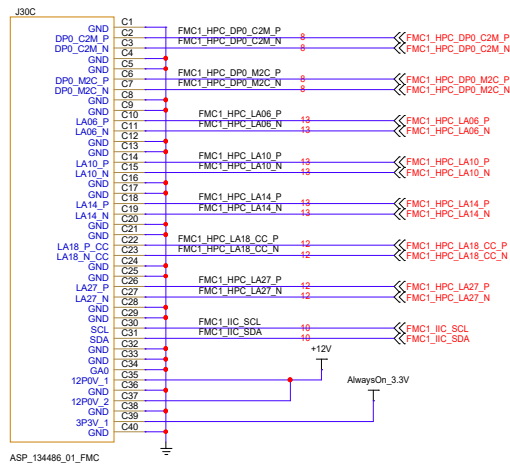
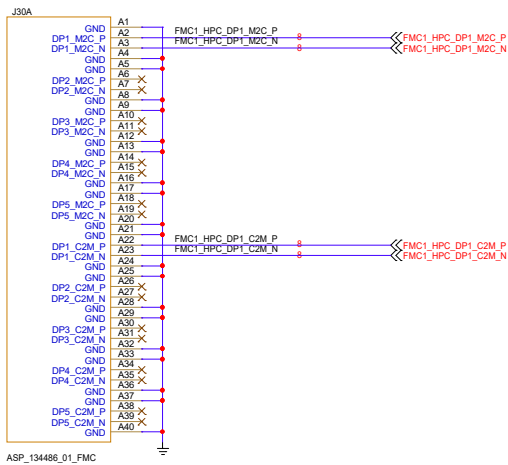
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# IIC & EEPROM

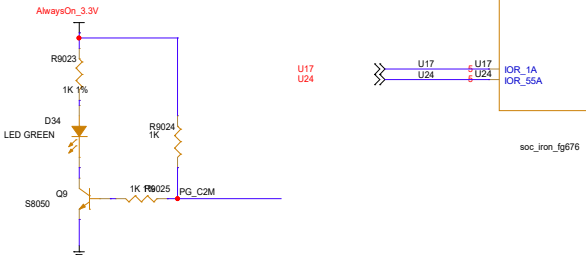
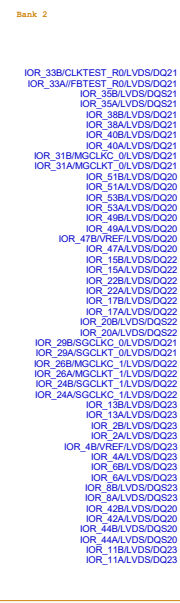


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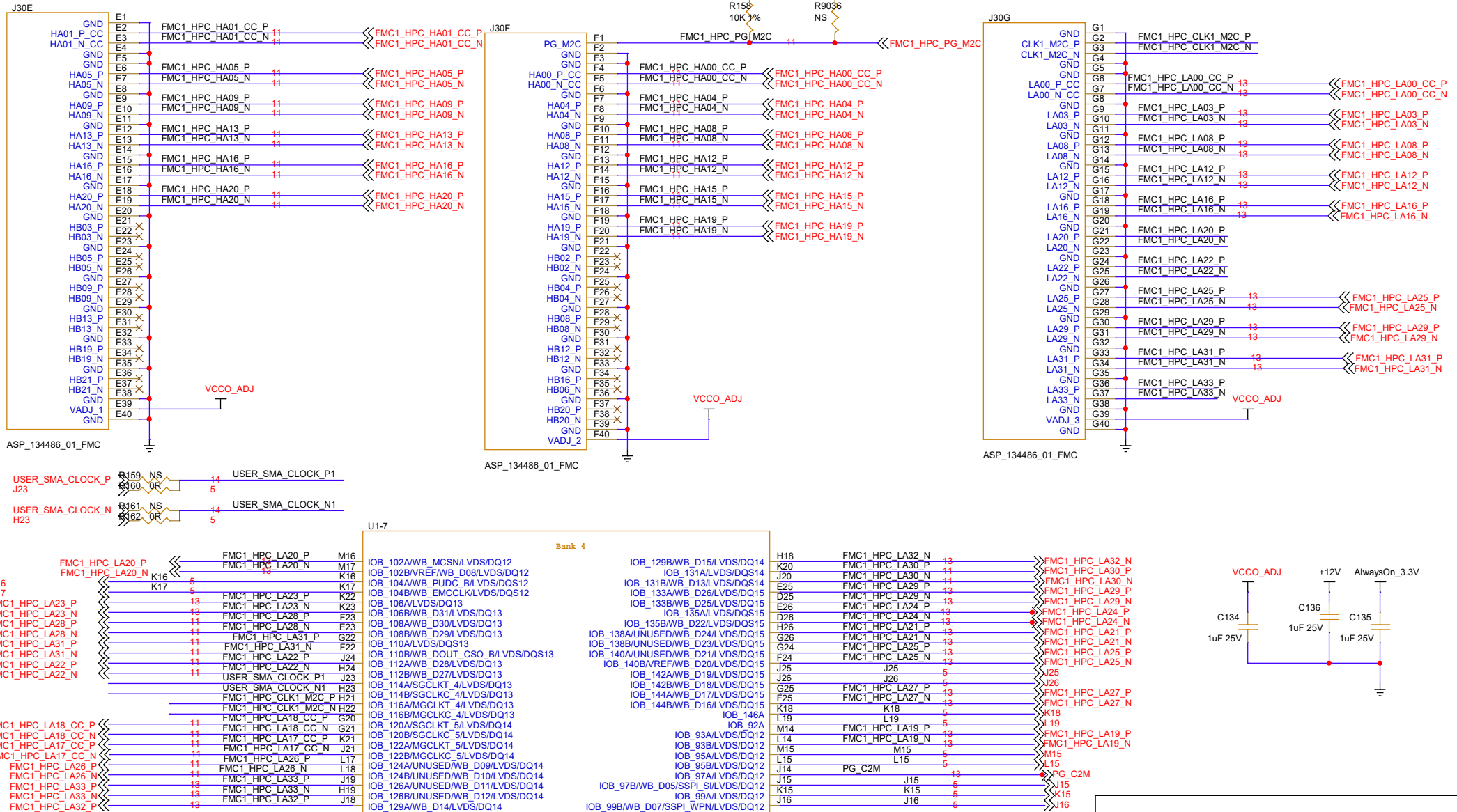
# FMC



U1-5

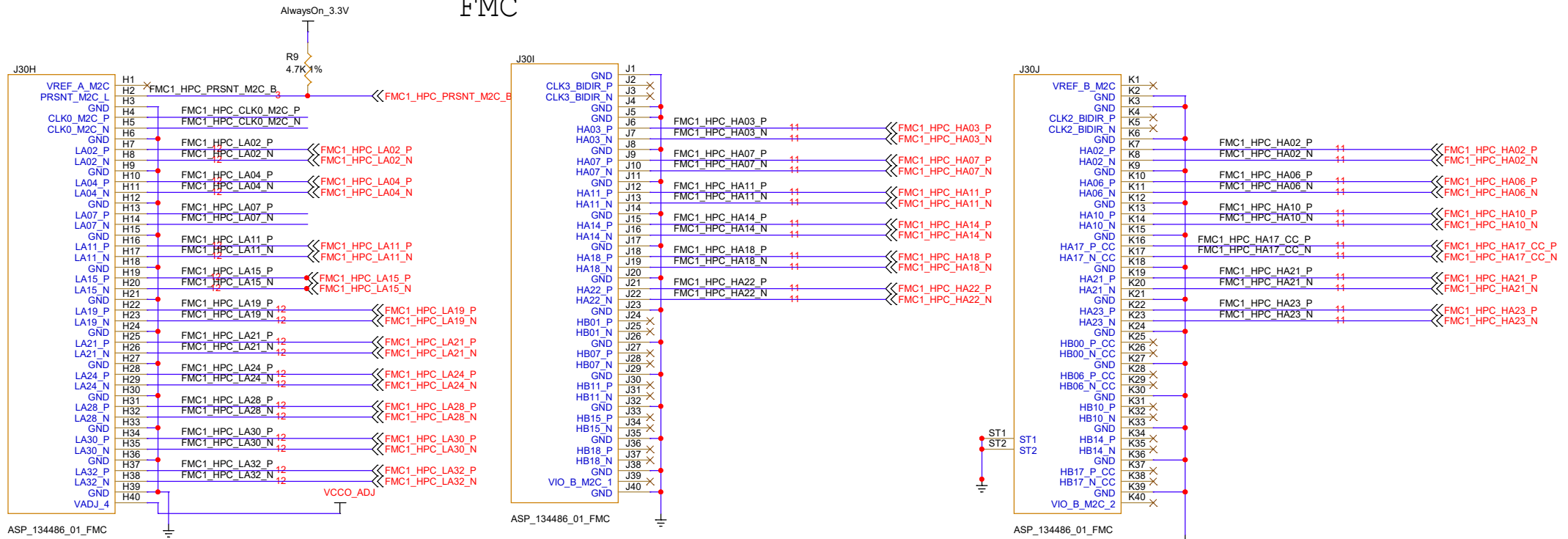


# FMC



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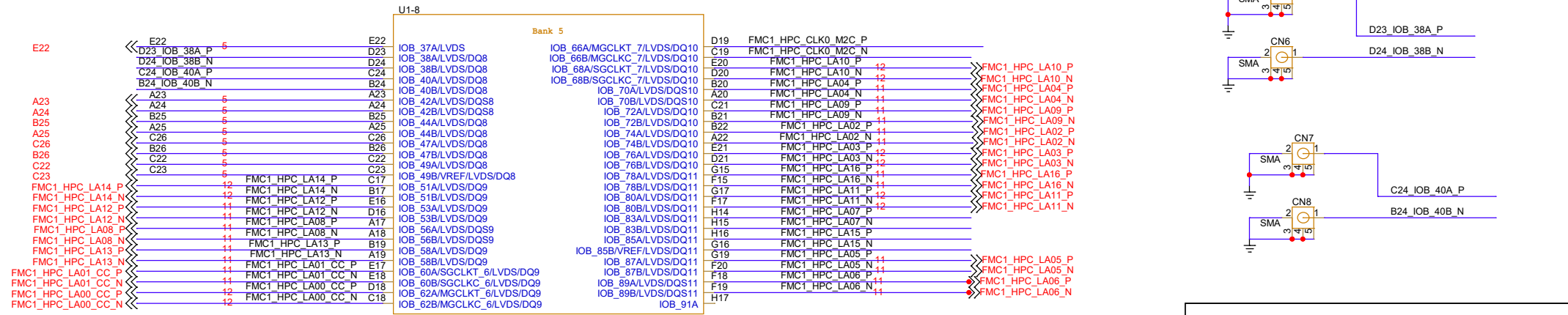
# FMC



ASP\_134486\_01\_FMC

ASP\_134486\_01\_FMC

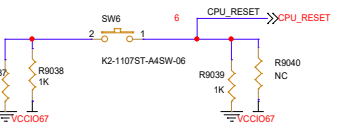
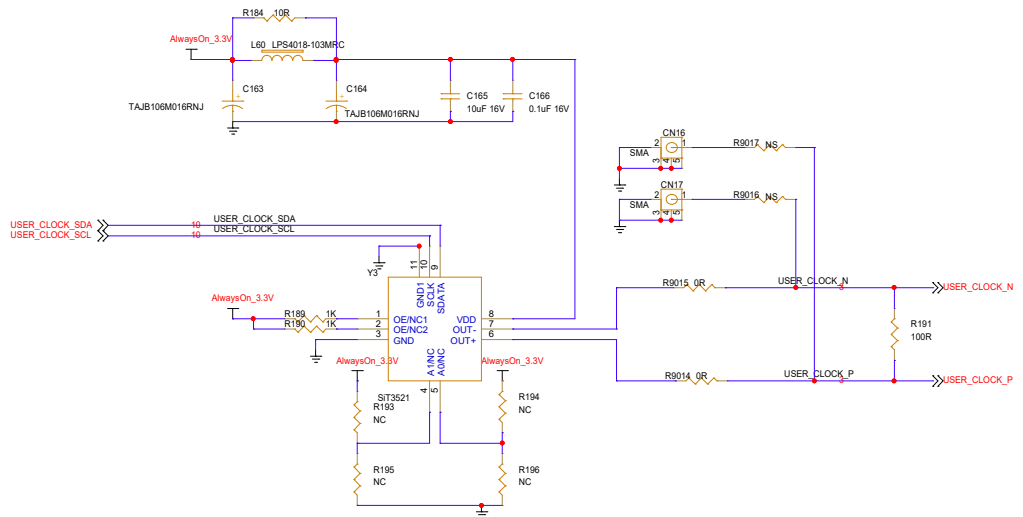
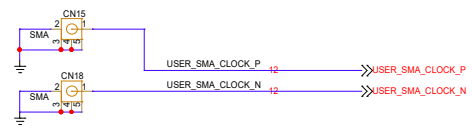
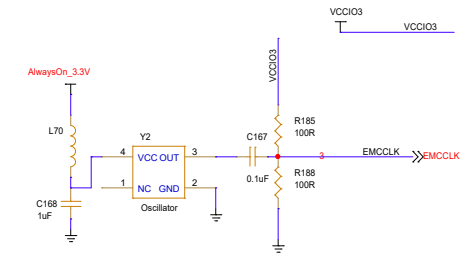
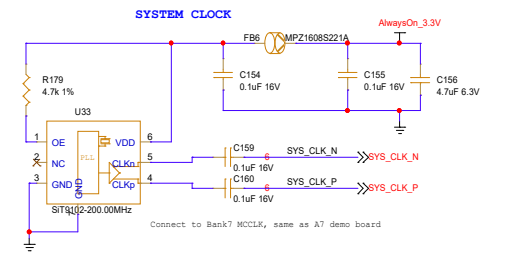
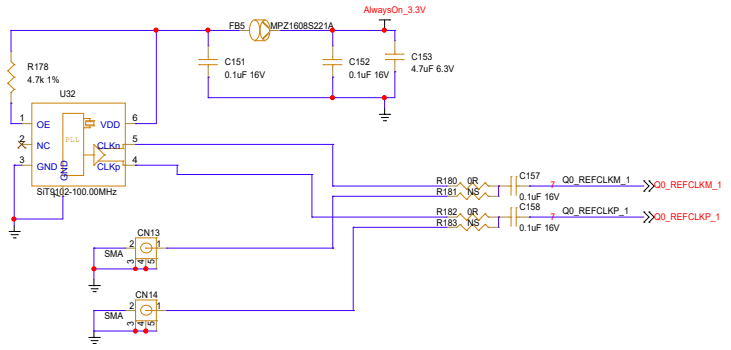
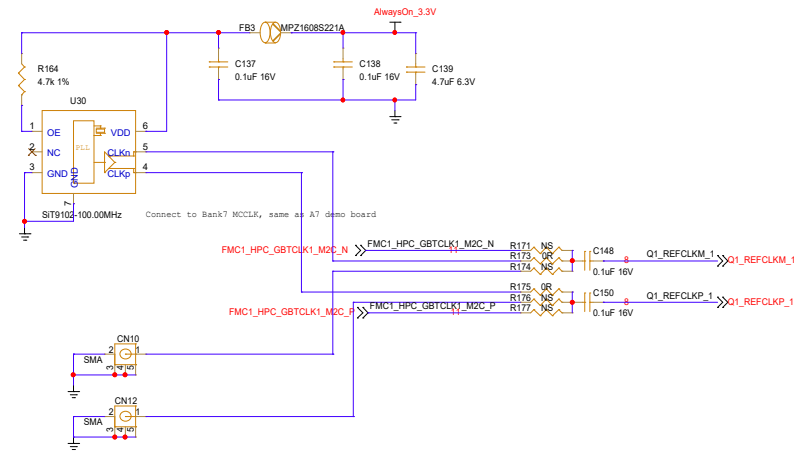
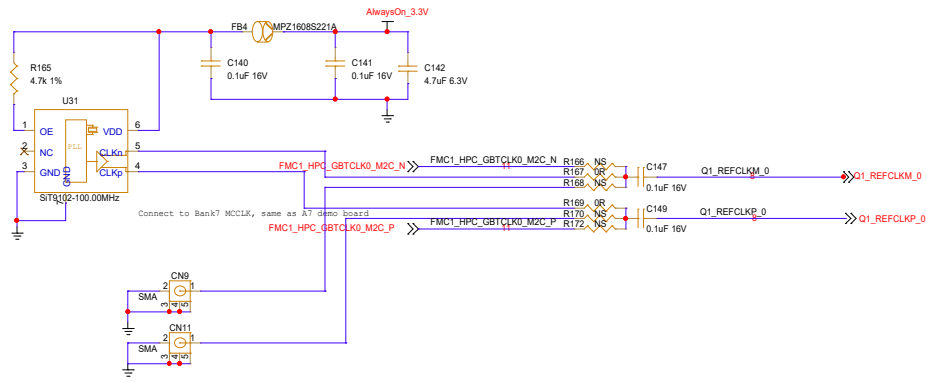
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soc\_iron\_fg676

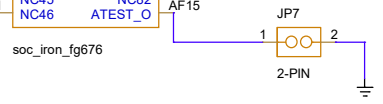
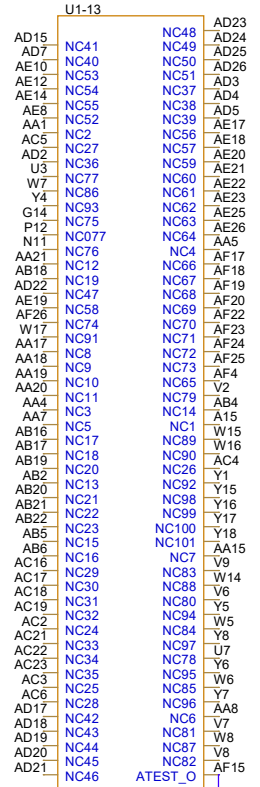
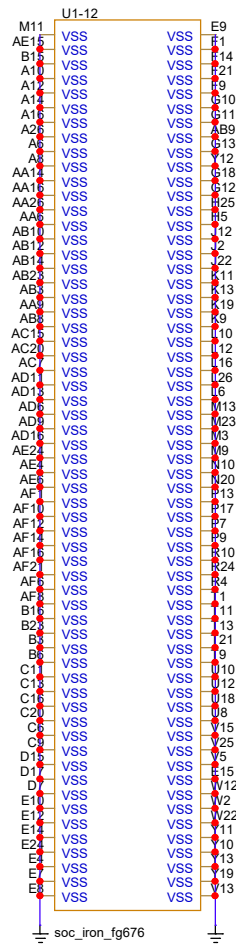
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# CLOCK



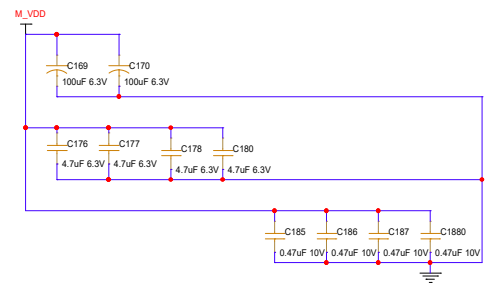
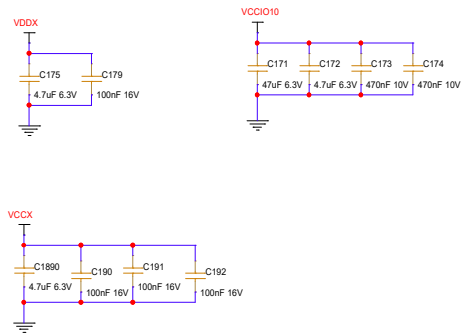
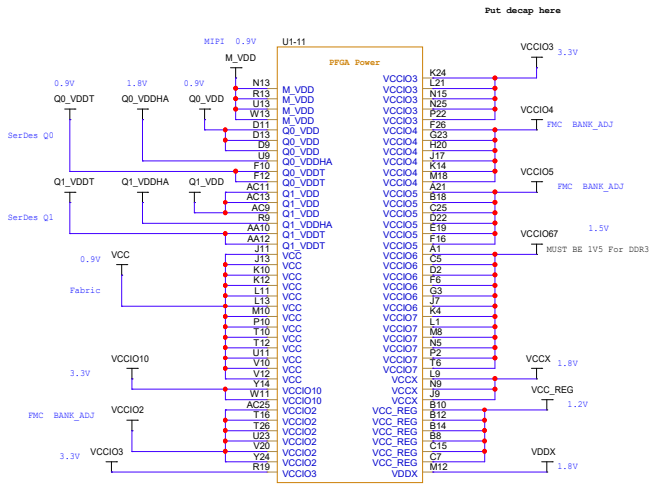
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# GND & NC

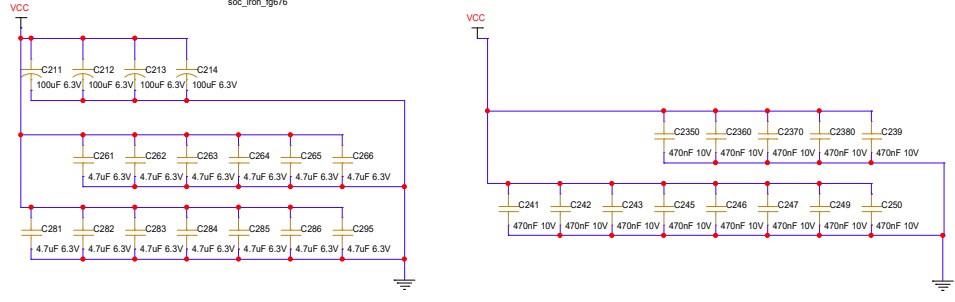
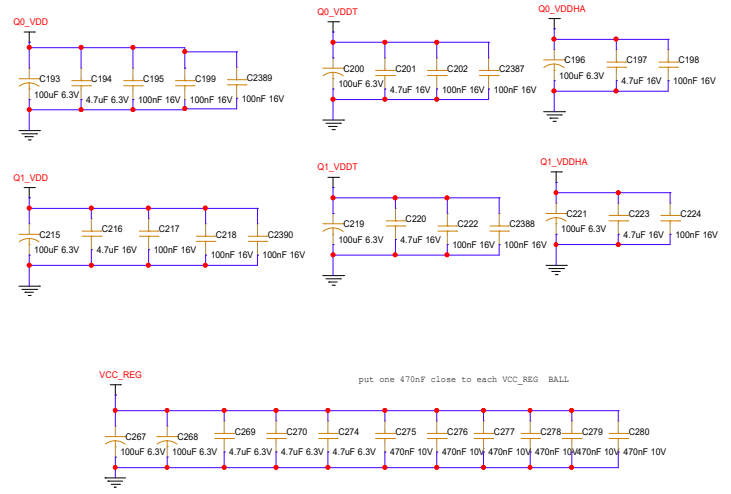


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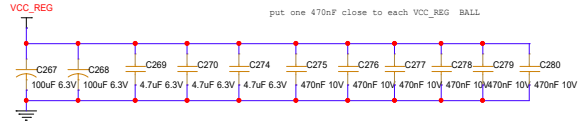
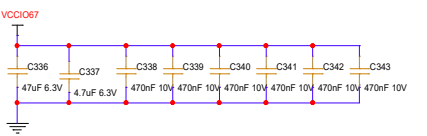
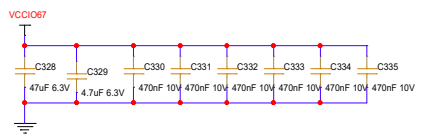
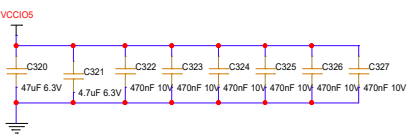
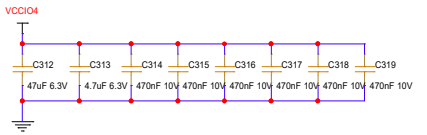
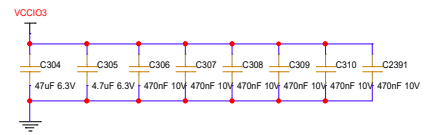
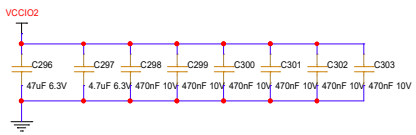
# FPGA\_POWER



2x100uF, 4x4.7uF, 4x0.47uF



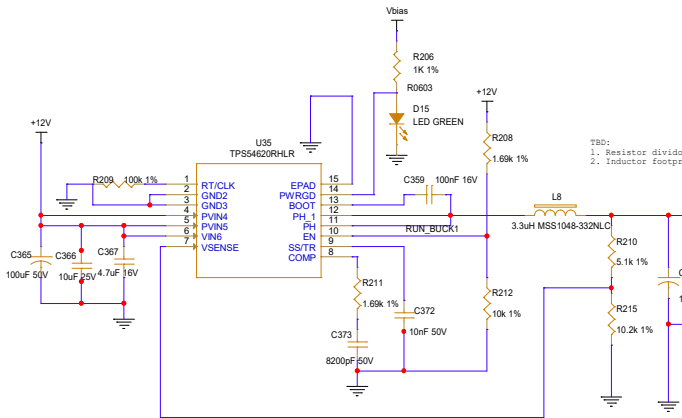
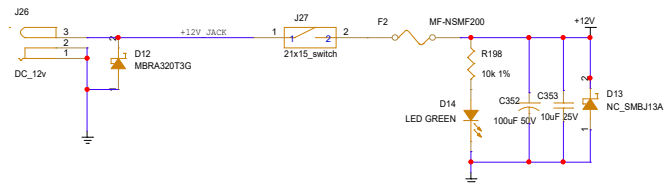
4x100uF, 13x4.7uF, 26x0.47uF



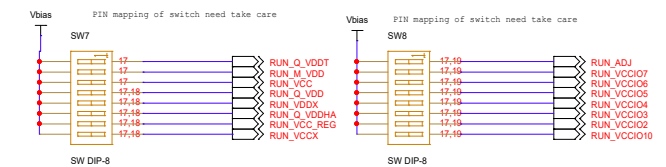
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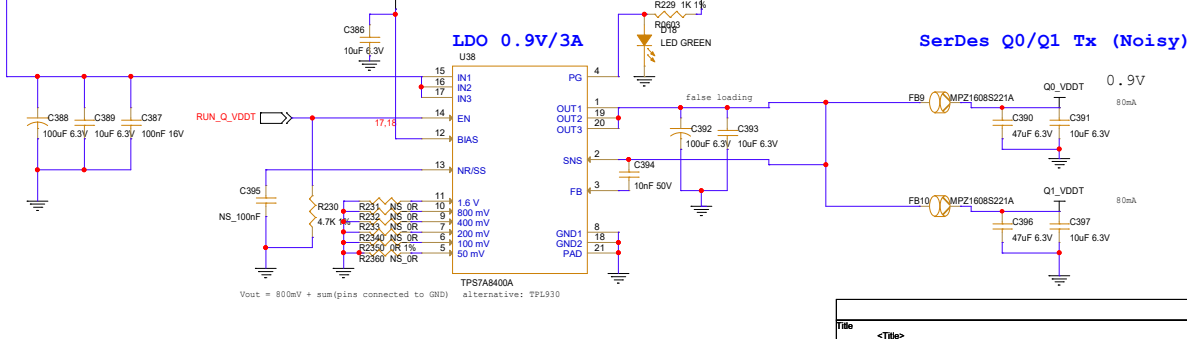
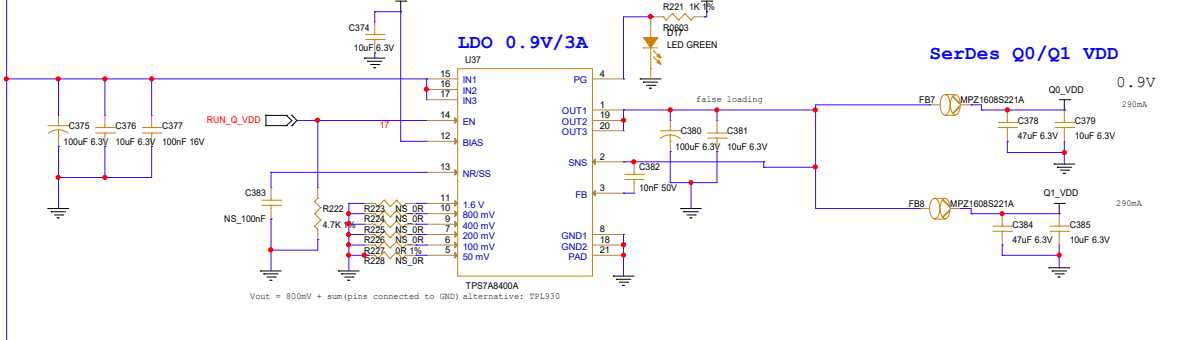
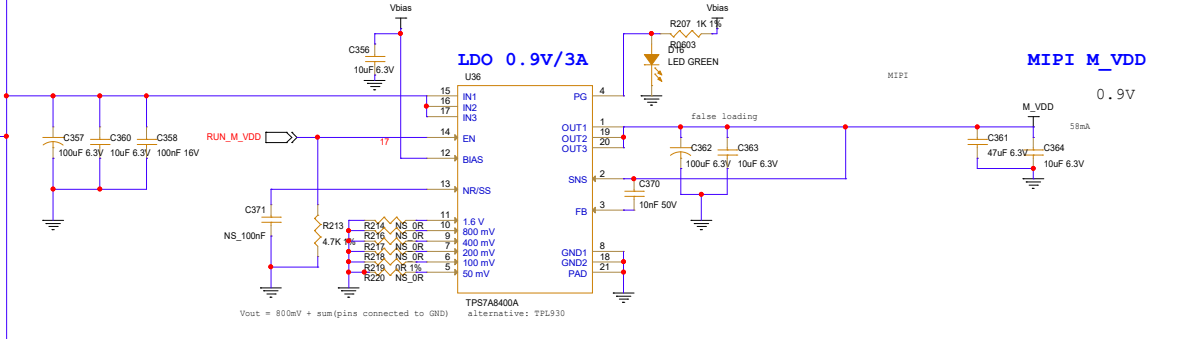
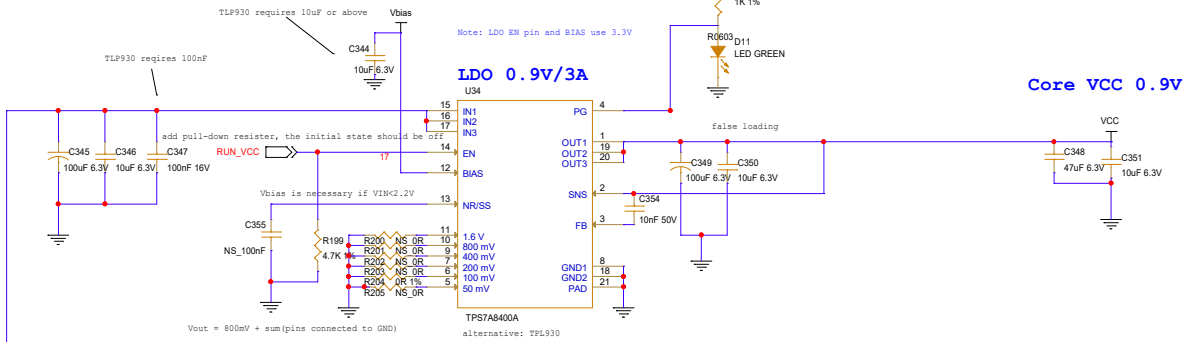
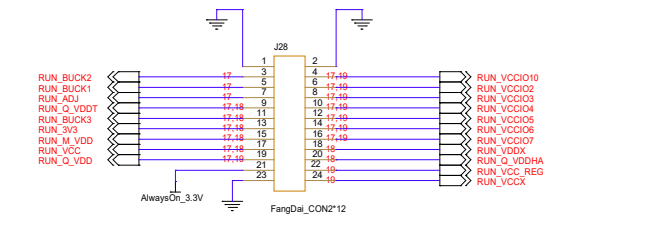
# 0.9V Power Supply



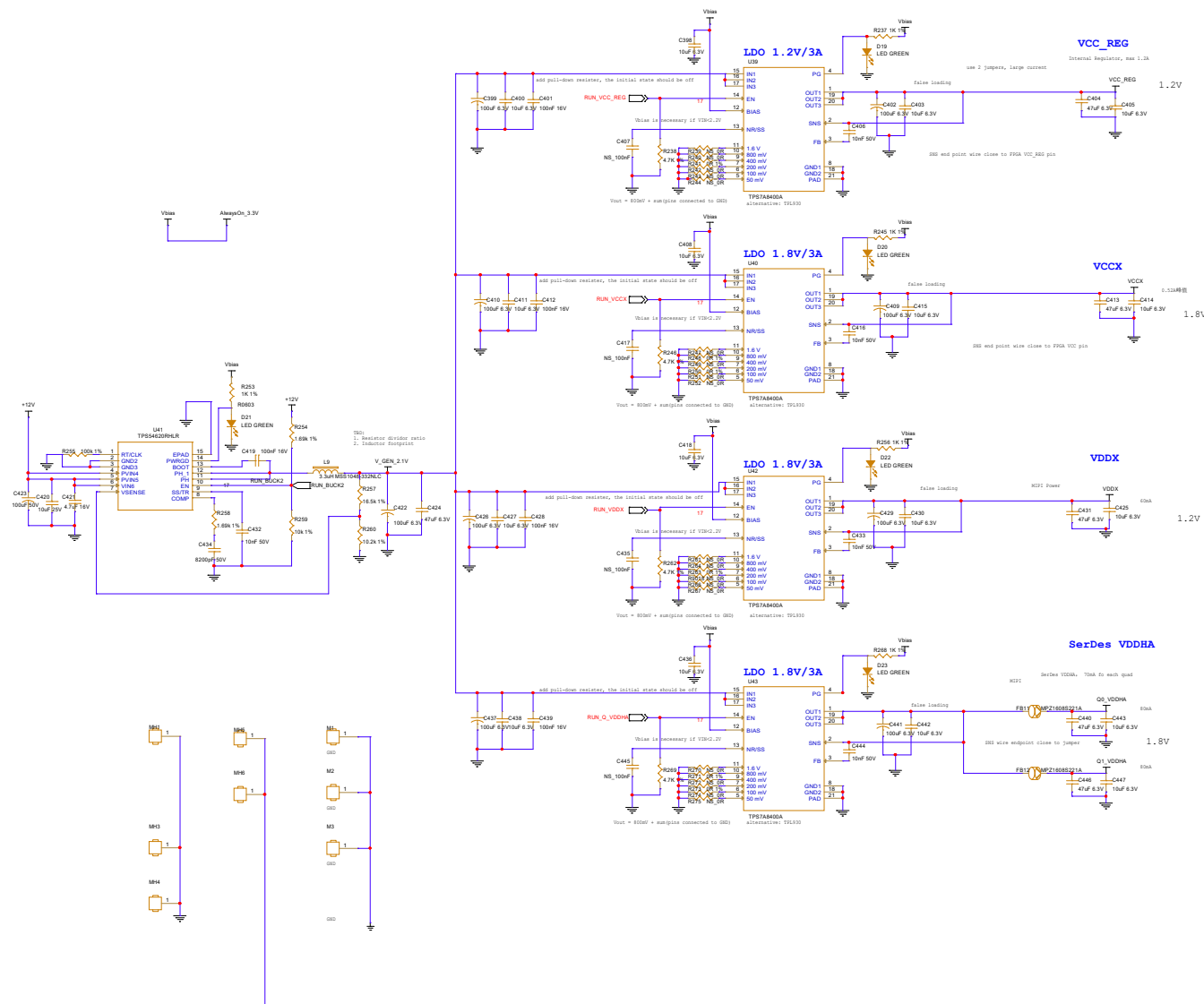
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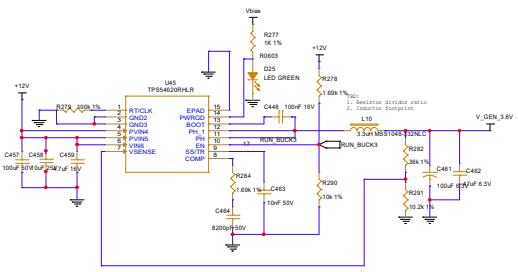


Totally 15 channel independent power supply, need external FPGA or MCU for power up sequence



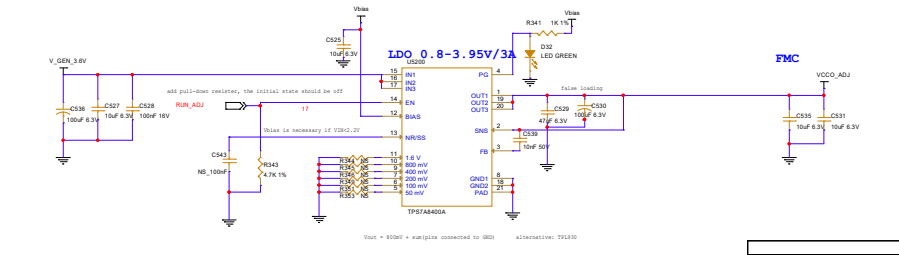
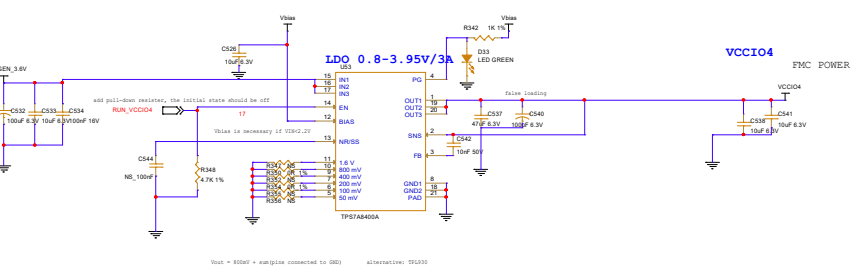
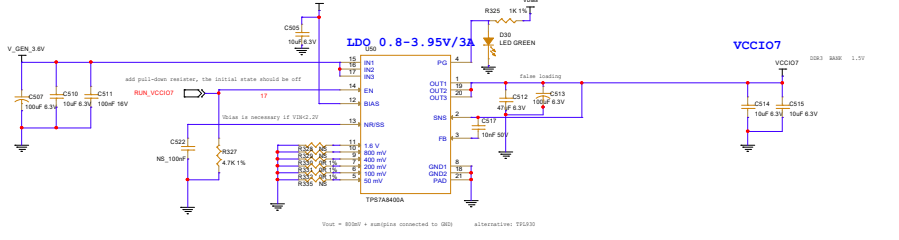
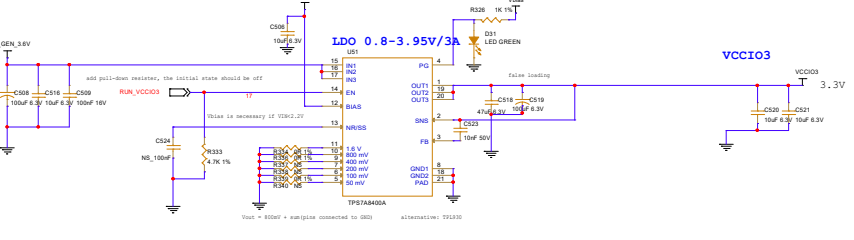
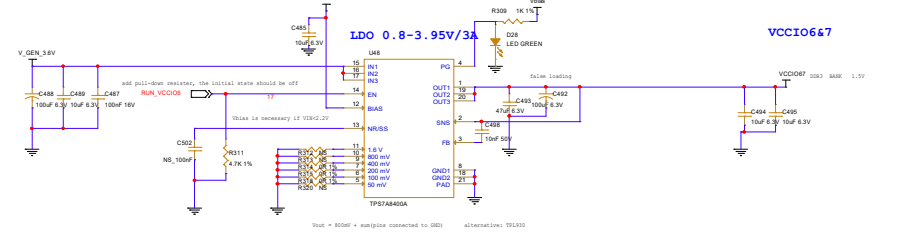
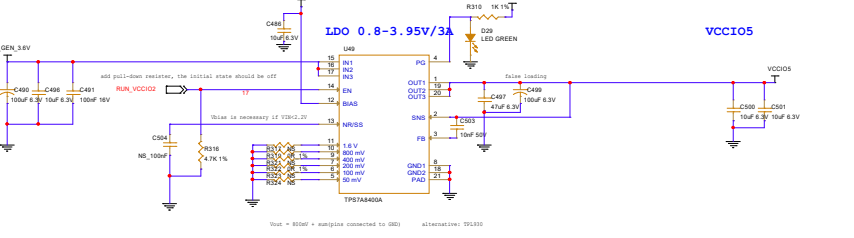
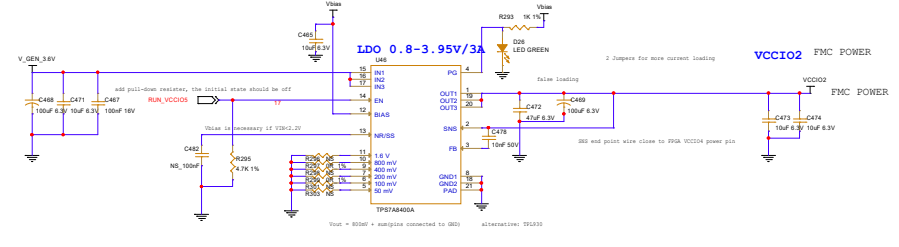
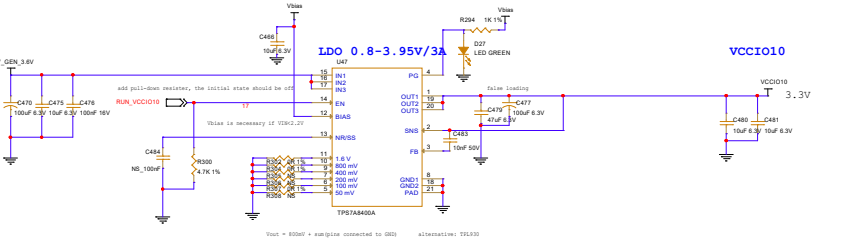
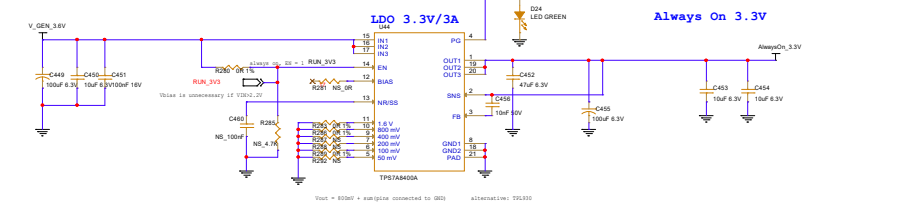
# 1.2V & 1.8V Power Supply





GPIO Power Supply

Provide 3.3V Bias Always On LDO



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