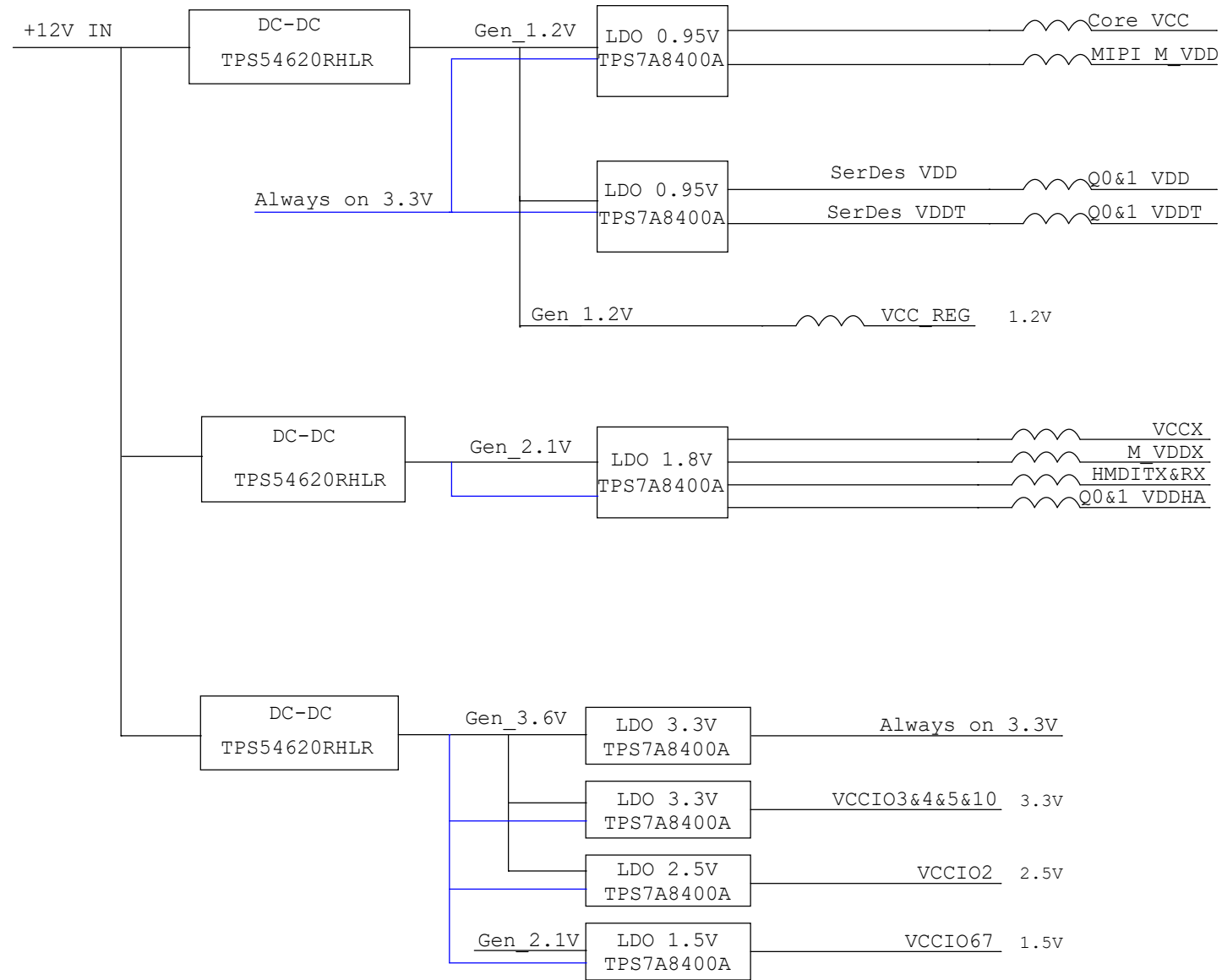


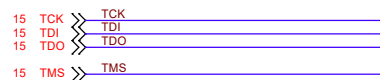
Power Tree



Always on 3.3V MIPI座

Title		
DK_GW5AT-LV138FPG676A		
Size	Document Number	Rev
A3	Power tree	V2.1
Date:	Thursday, December 05, 2024	Sheet 2 of 25

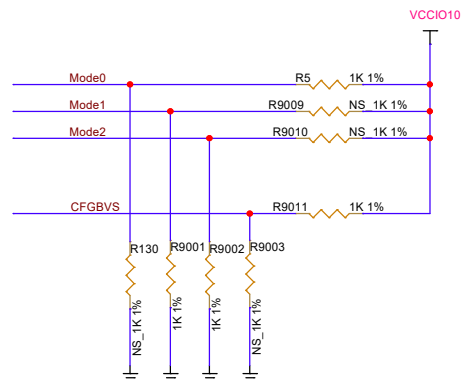
Jtag



MSPI



ModeS

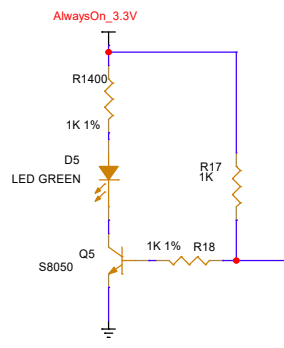


```

MODE[2:0]:
JTAG:XXX/101
MSPI:001V
SSPI:010
Master SERIAL:000
Slave SERIAL:111
Master CPU:100
Slave CPU:110
    
```

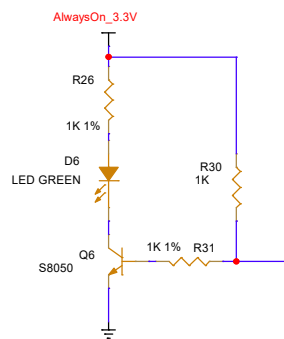
CFGBVS=1, BANK3&4&10=3.3V Or 2.5V

Ready

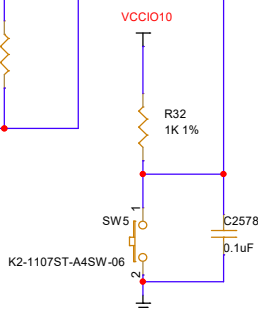


Note: Ready/Done are open drain output

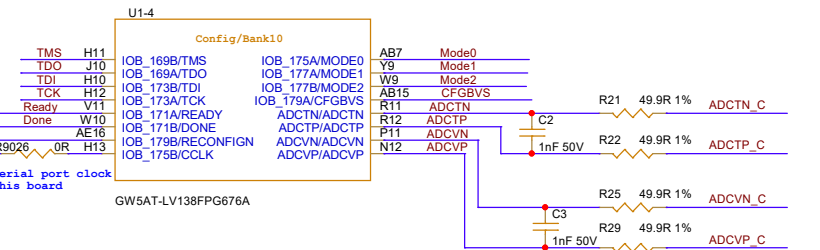
Done



Reconfig

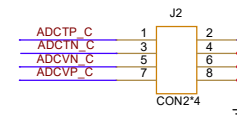


For MSPI, CPU, Serial port clock
MSPI clock for this board



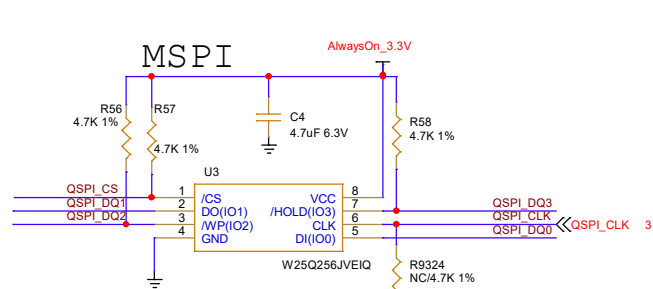
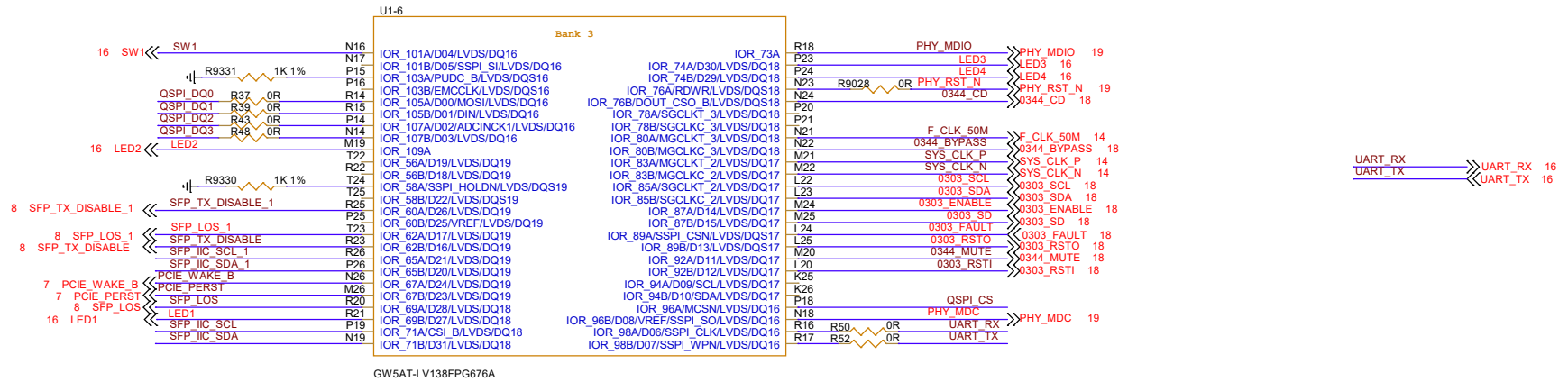
XADC, for Sensor.
Anti-alias filter is added

XADC Header

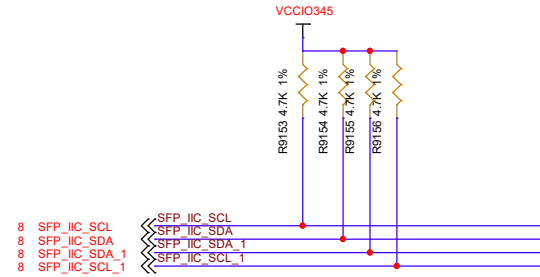


Title		
DK_GW5AT-LV138FPG676A		
Size	Document Number	Rev
A3	Bank10_Cfg_Modes_Jtag_ADC	V2.1
Date:	Thursday, December 05, 2024	Sheet 3 of 25

MSPI, GPIO, SERIAL, I2C



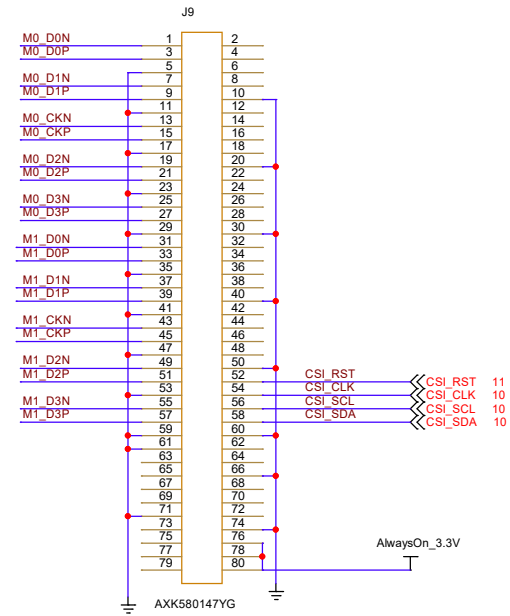
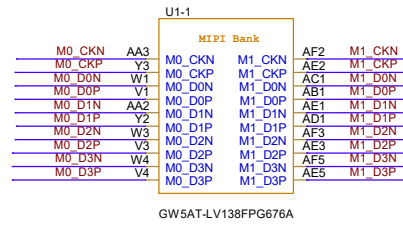
QSPI is bi-direction, so that level shift buffer must be bi-direction, TI TXB0304 is OK, but out of stock



Title		
DK_GW5AT-LV138FPG676A		
Size	Document Number	Rev
A3	Bank3_MSPI_I2C_GPIO	V2.1
Date:	Thursday, December 05, 2024	Sheet 4 of 25

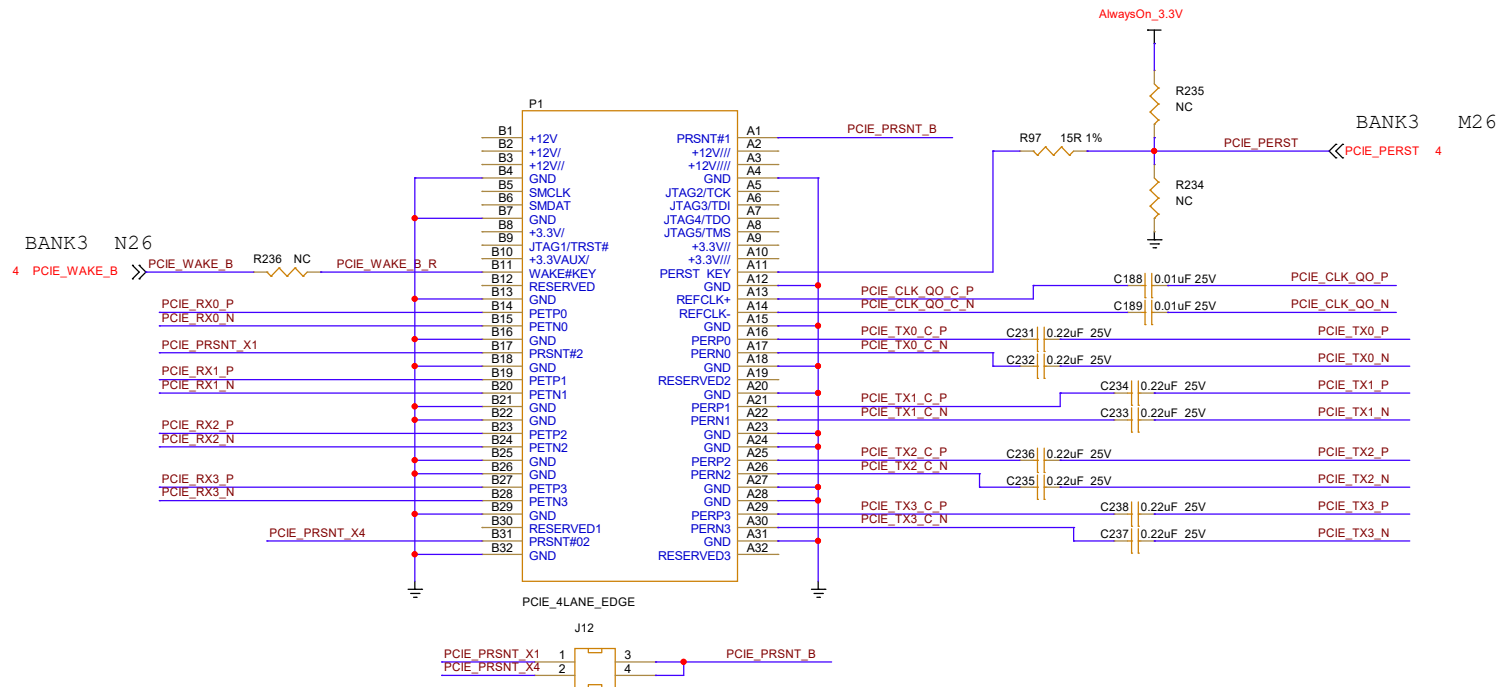
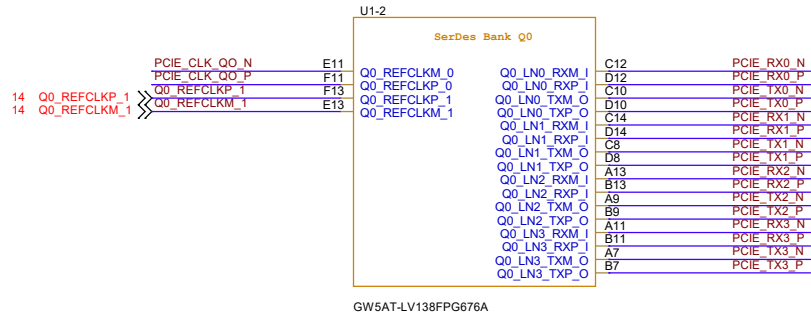
MIPI

MIPI bank is for MIPI RX hard macro.
 As the board is for characterization purpose, SMA connector is used.
 MIPI bank only have SMA connectors. Length match rules:
 1. M0/M1 length match for each intra group
 2. M0 and M1 inter group length match is nice to have



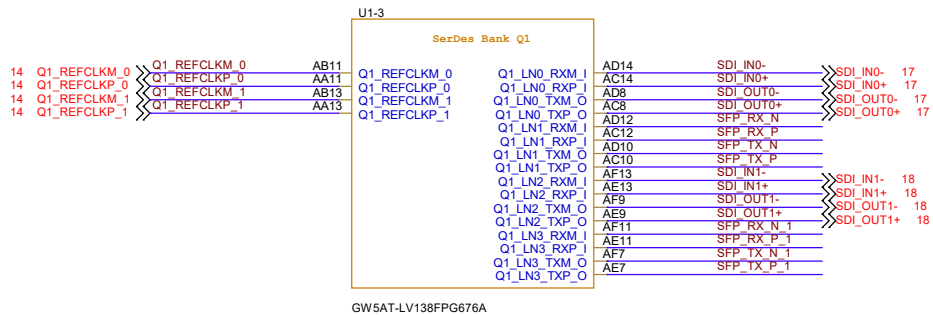
PCIe

SerDes to SMP pin order could be swapped.



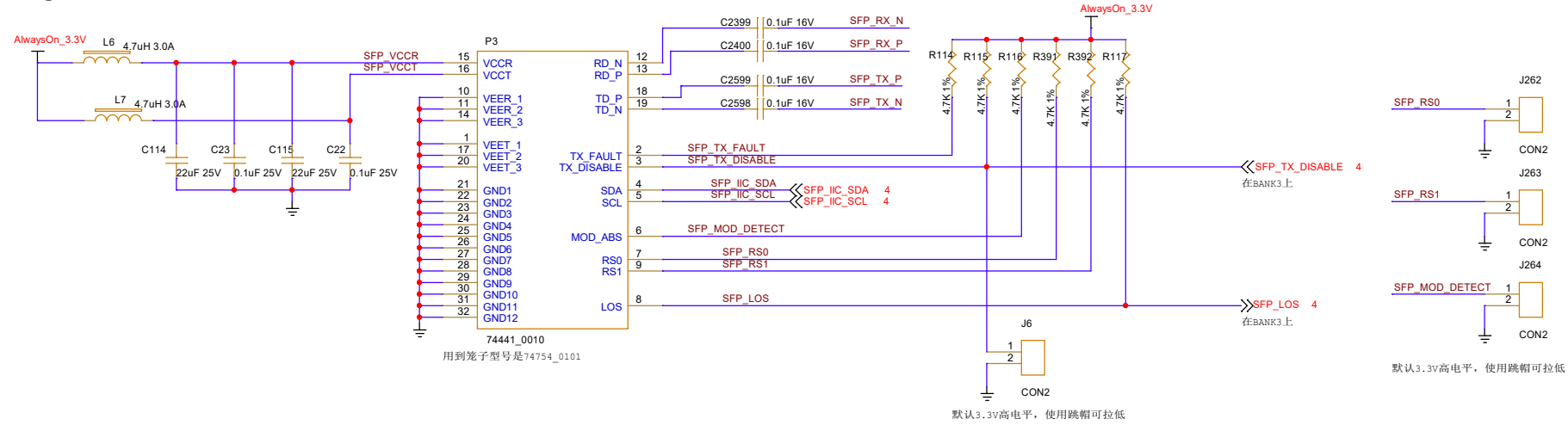
Title		
DK_GW5AT-LV138FPG676A		
Size	Document Number	Rev
A3	BankQ0_PcIe	V2.1
Date:	Thursday, December 05, 2024	Sheet 7 of 25

SFP*2



GW5AT-LV138FPG676A

SFP1

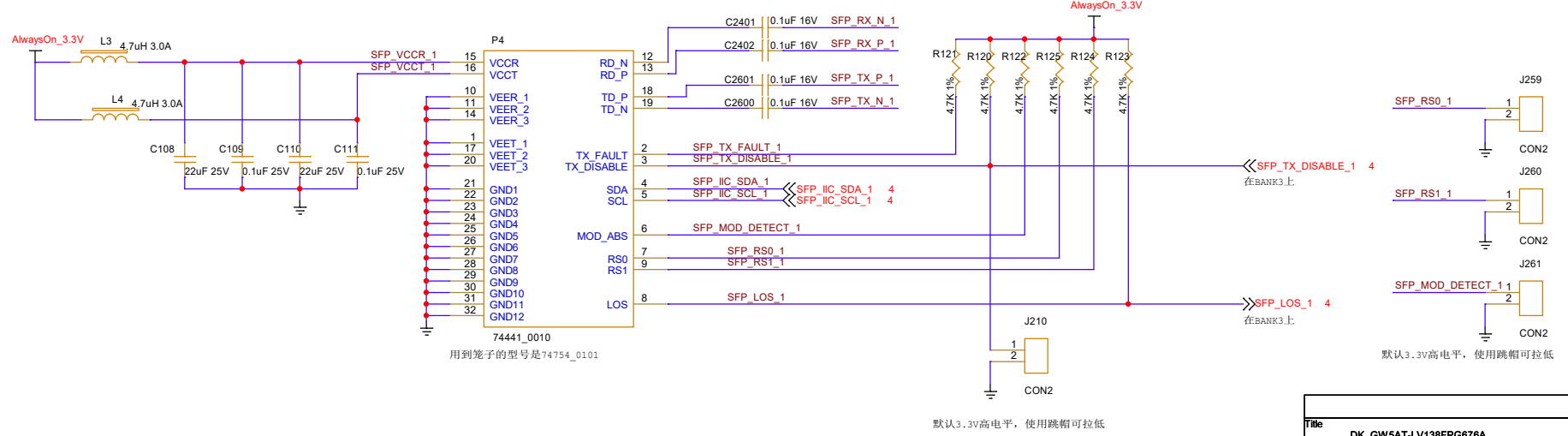


74441_0010
用到笼子的型号是74754_0101

默认3.3V高电平，使用跳帽可拉低

默认3.3V高电平，使用跳帽可拉低

SFP2



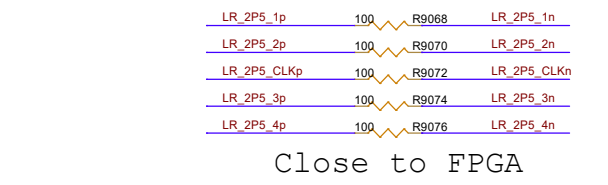
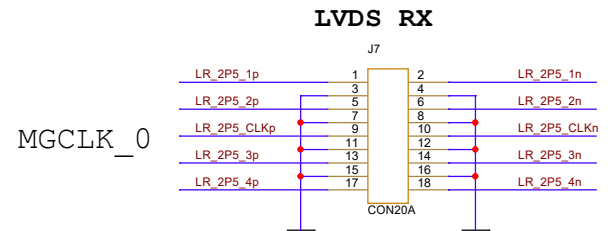
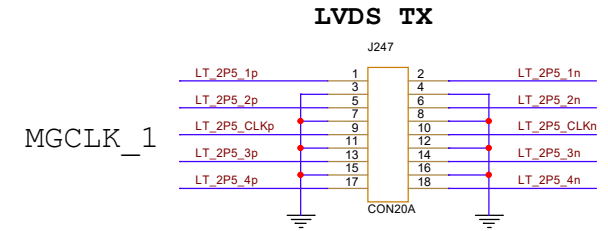
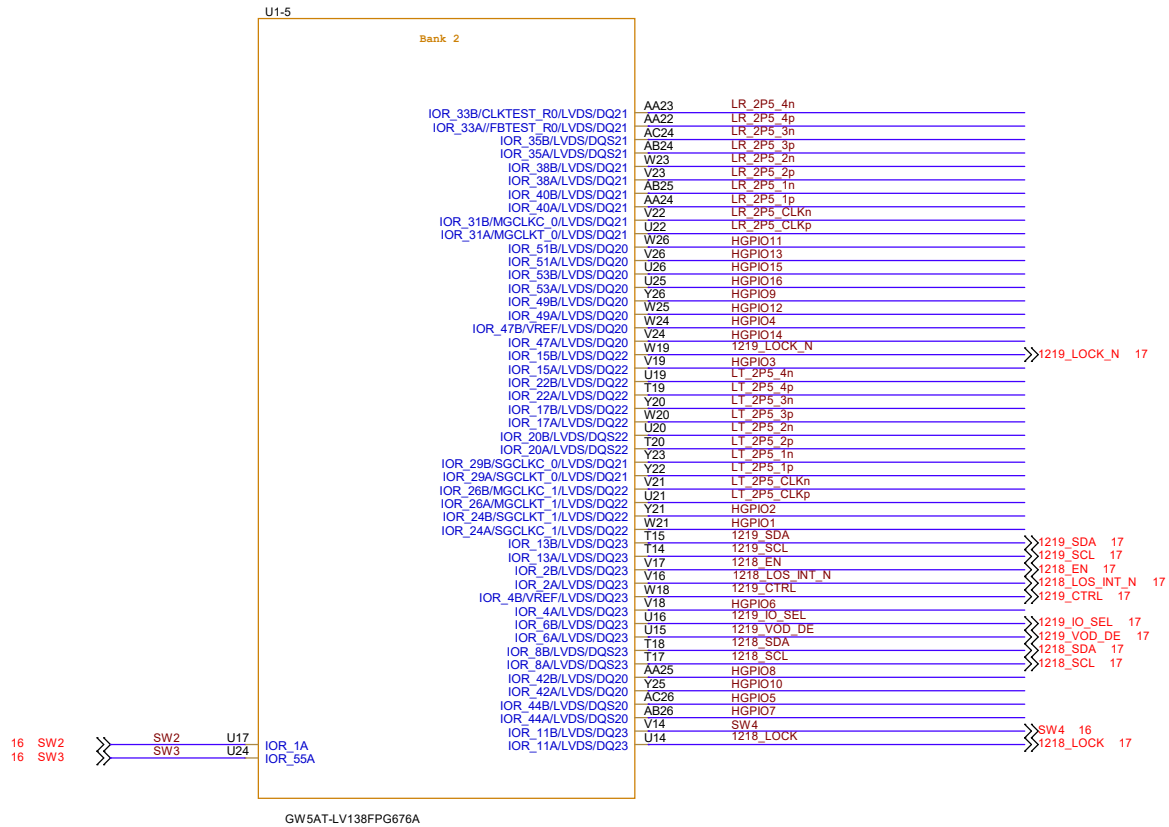
74441_0010
用到笼子的型号是74754_0101

默认3.3V高电平，使用跳帽可拉低

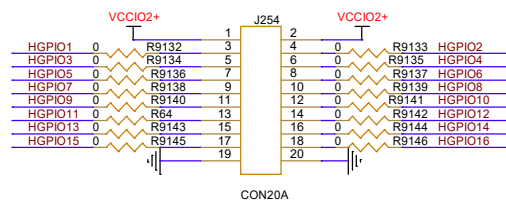
默认3.3V高电平，使用跳帽可拉低

Title		
DK_GW5AT-LV138FPG676A		
Size	Document Number	Rev
A3	BankQ1_SFP1-2	V2.1
Date:	Thursday, December 05, 2024	Sheet 8 of 25

LVDS TX/RX



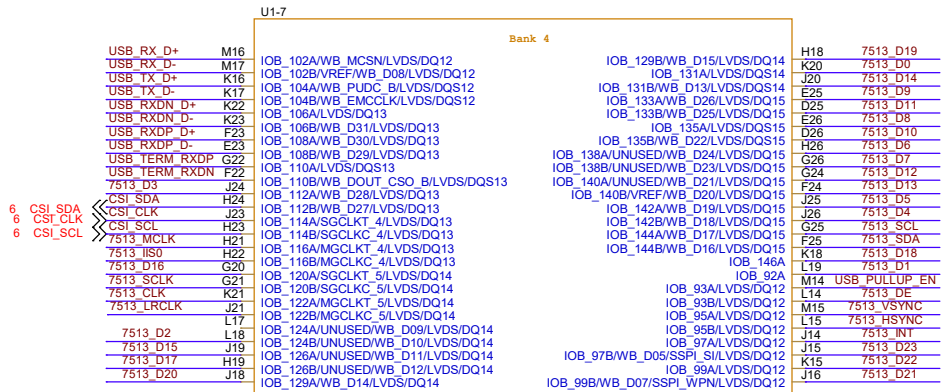
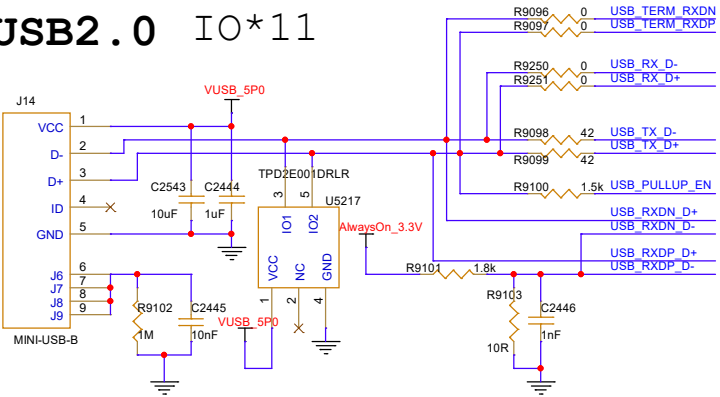
2.5V IO



Title		
DK_GW5AT-LV138FPG676A		
Size	Document Number	Rev
A3	Bank2_LVDS_GPIO*16	V2.1
Date:	Thursday, December 05, 2024	Sheet 9 of 25

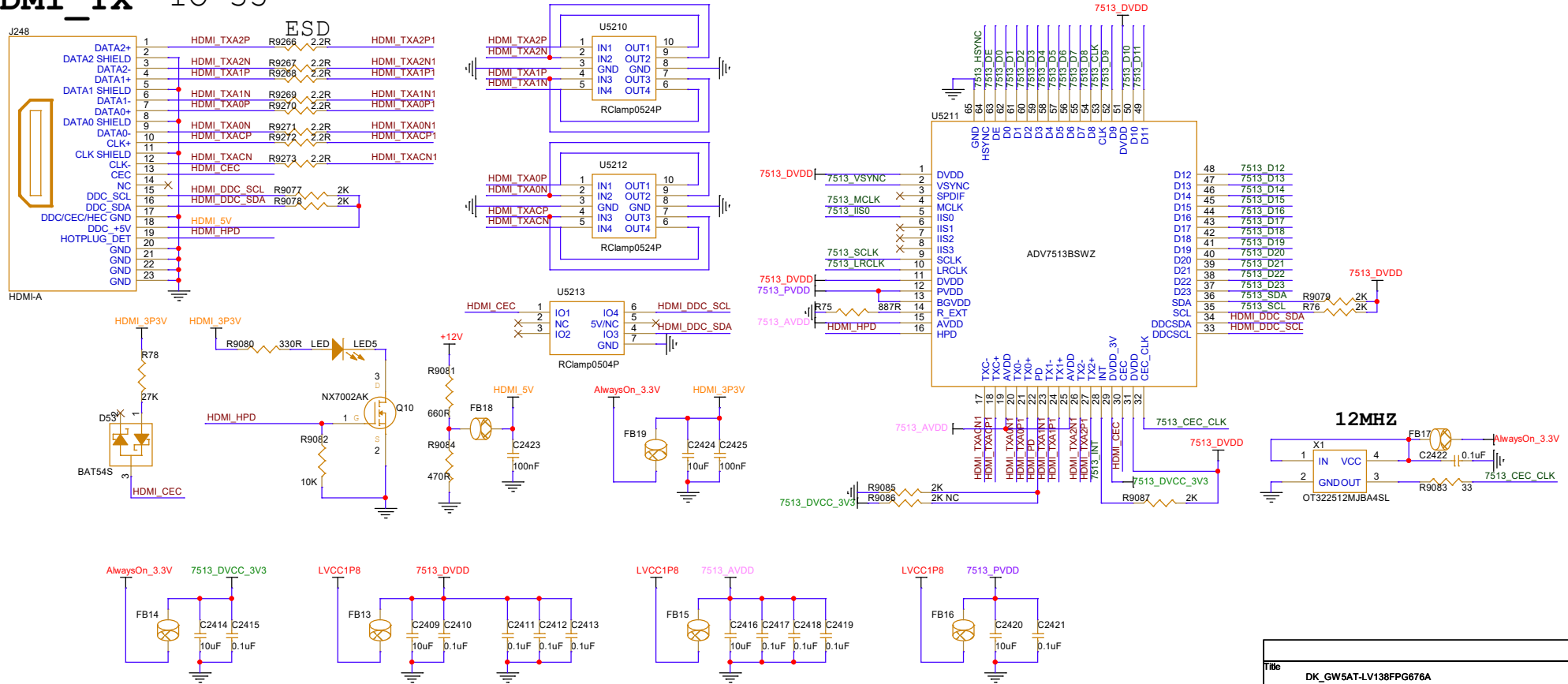
HDMI-TX/USB2.0

USB2.0 IO*11



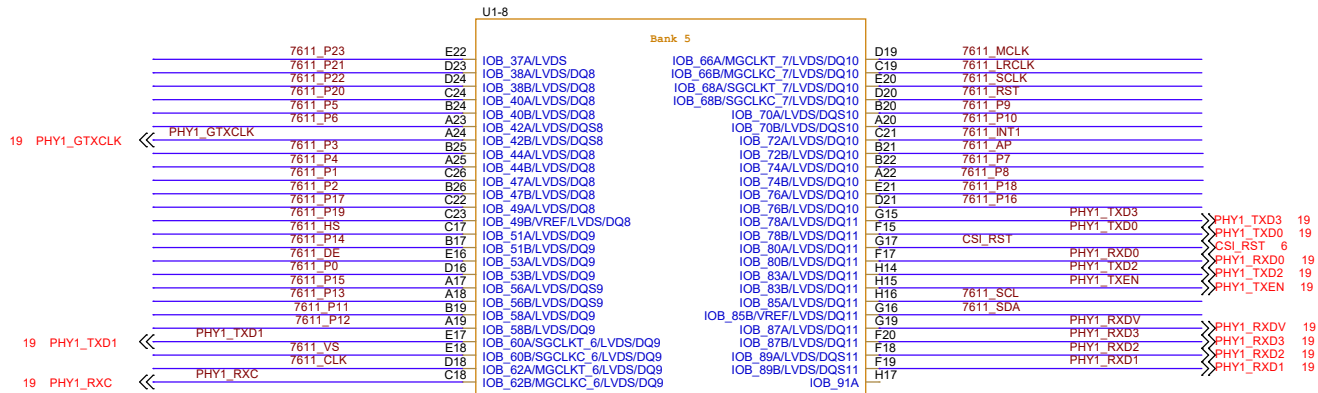
GW5AT-LV138FPG676A

HDMI_TX IO*35



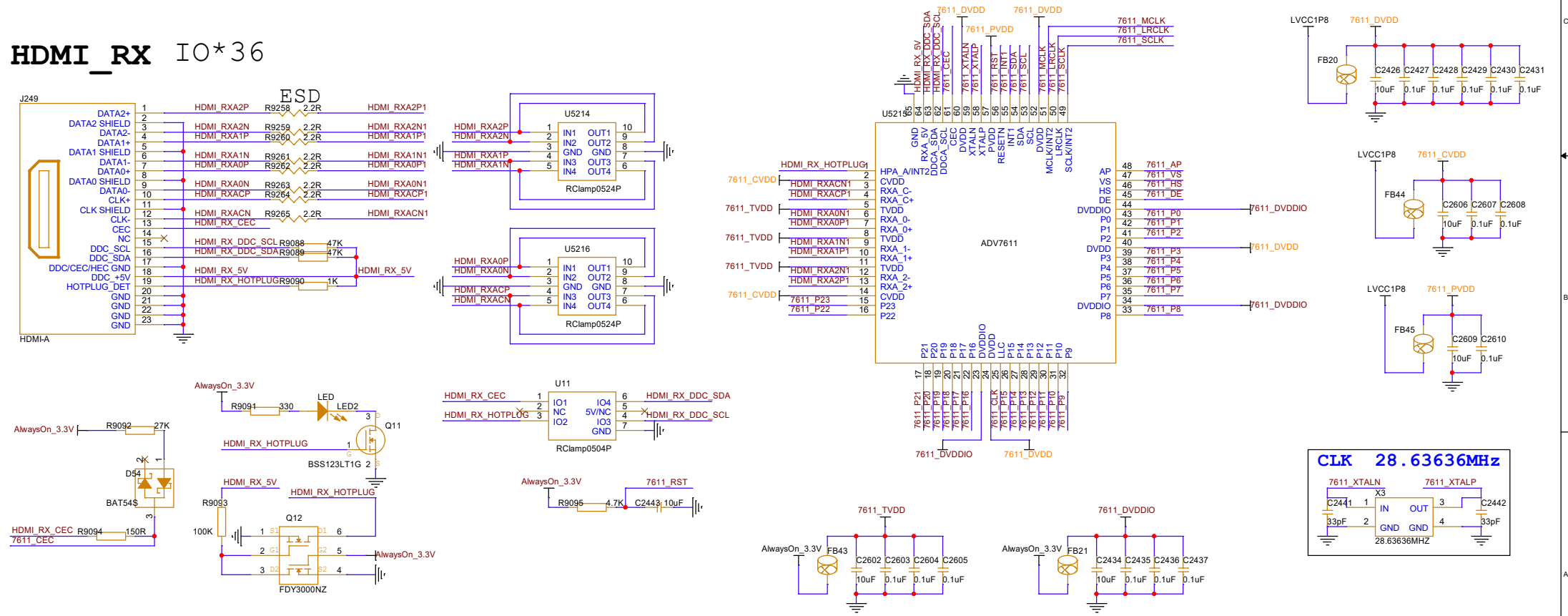
Title		
DK_GW5AT-LV138FPG676A		
Size	Document Number	Rev
A3	Bank4_HDMI-TX_USB20	V2.1
Date:	Thursday, December 05, 2024	Sheet 10 of 25

HDMI-RX



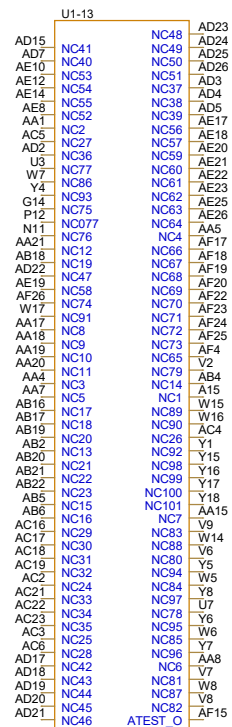
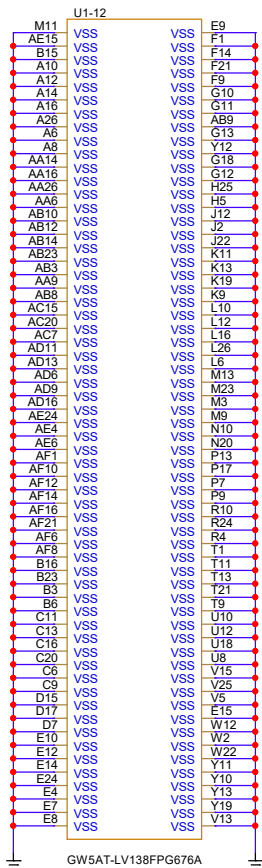
GW5AT-LV138FPG676A

HDMI_RX IO*36



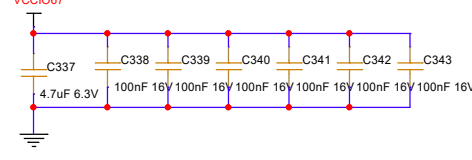
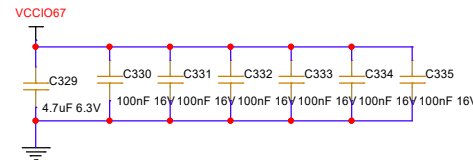
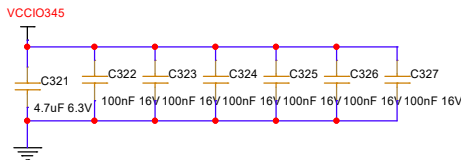
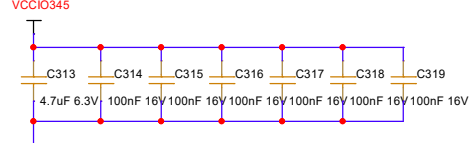
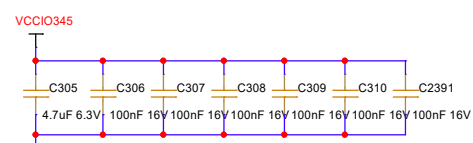
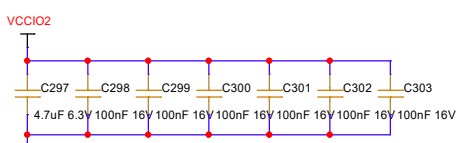
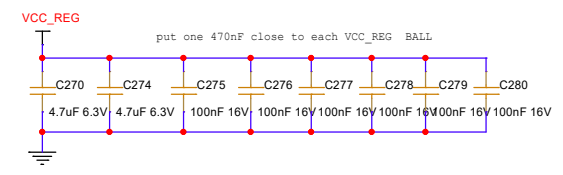
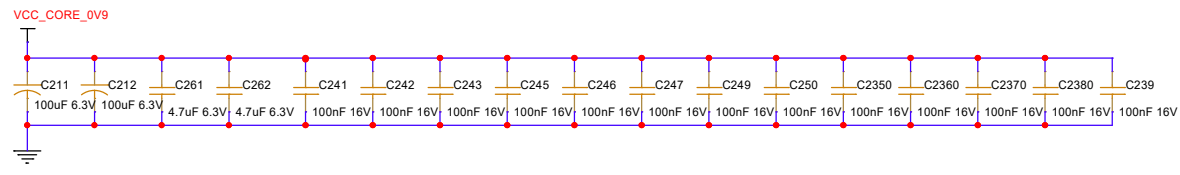
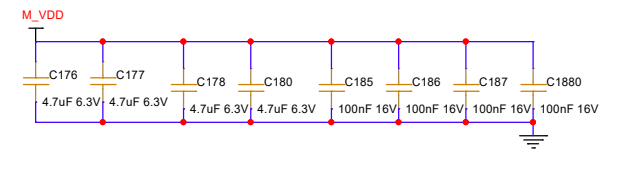
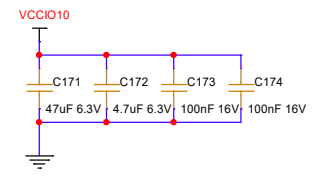
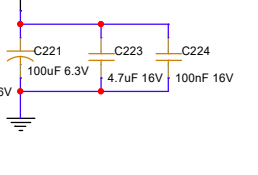
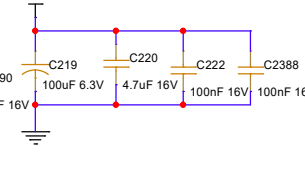
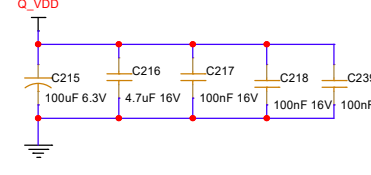
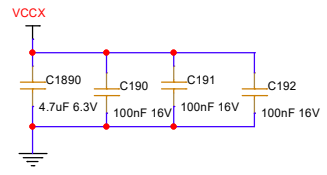
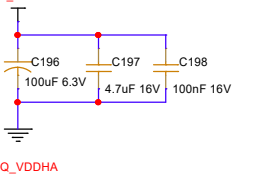
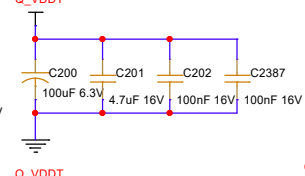
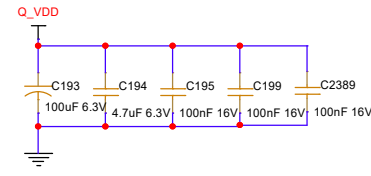
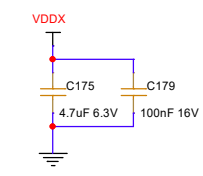
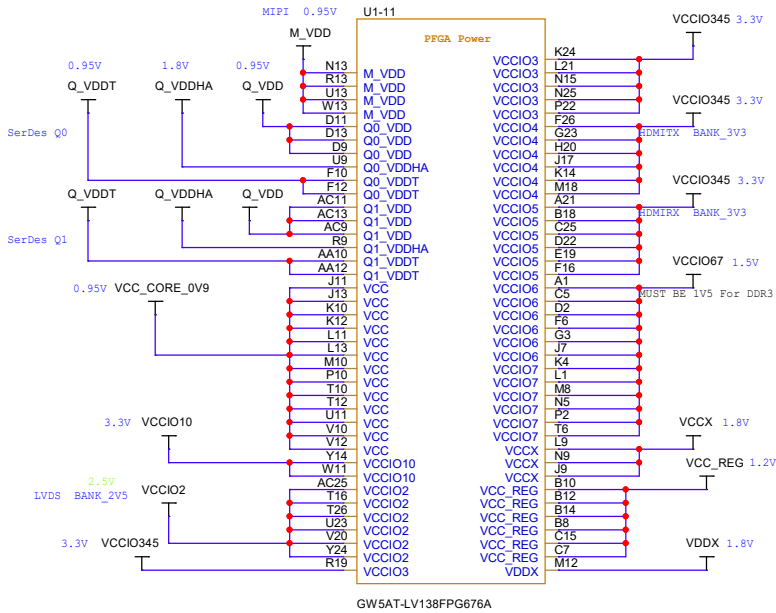
Title		DK_GW5AT-LV138FPG676A
Size	Document Number	Bank5_HDMI-RX_RGMII
A3	Rev	V2.1
Date:	Thursday, December 05, 2024	Sheet 11 of 25

GND & NC



FPGA_POWER

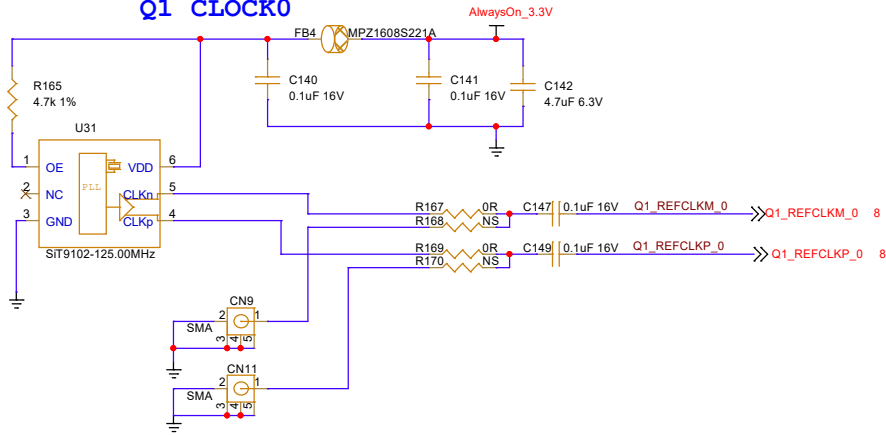
Put decap here



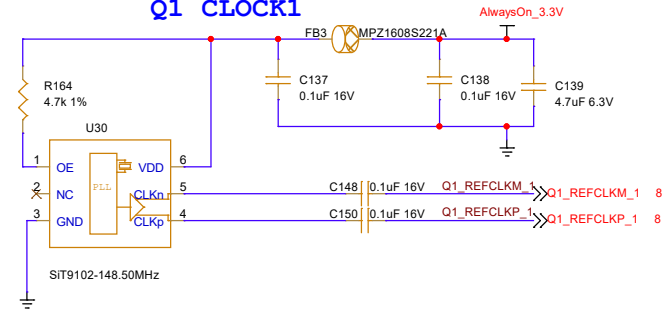
Title		
DK_GW5AT-LV138FPG676A		
Size	Document Number	Rev
A3	FPGA_POWER	V2.1
Date:	Thursday, December 05, 2024	Sheet 13 of 25

CLOCK

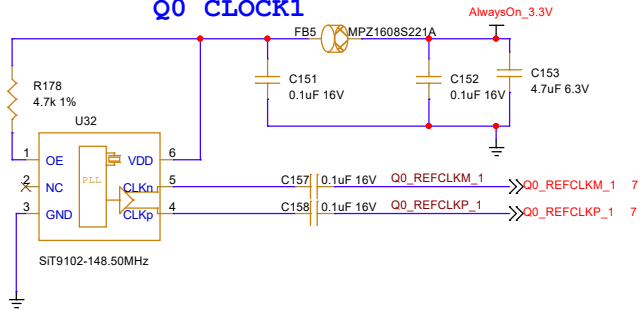
Q1 CLOCK0



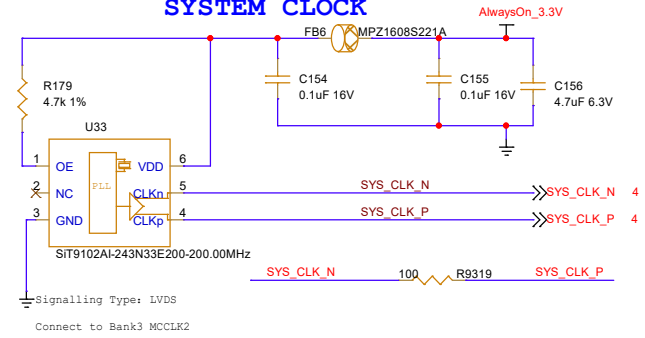
Q1 CLOCK1



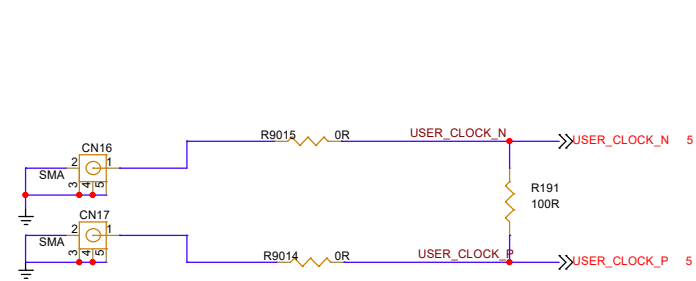
Q0 CLOCK1



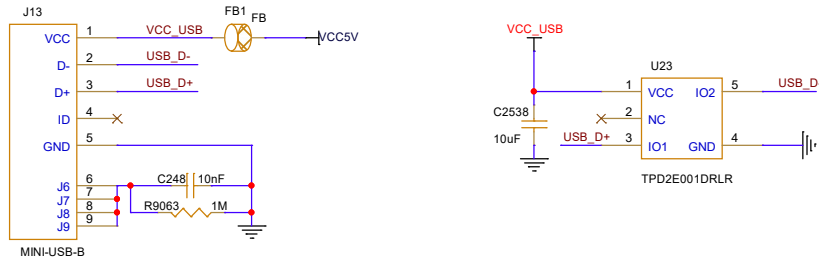
SYSTEM CLOCK



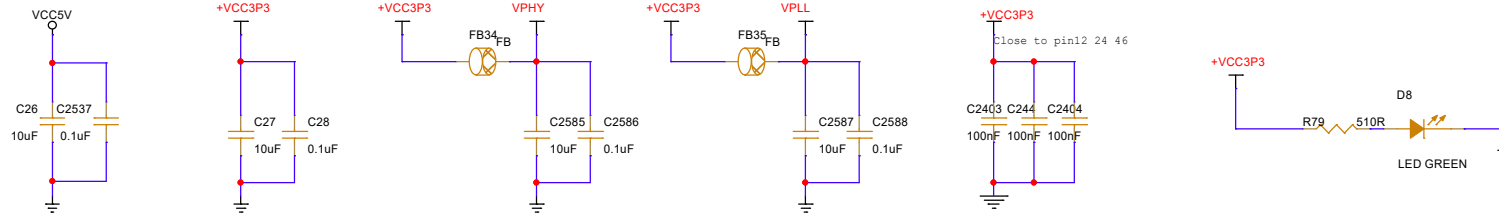
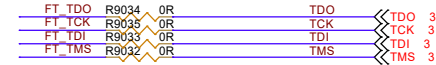
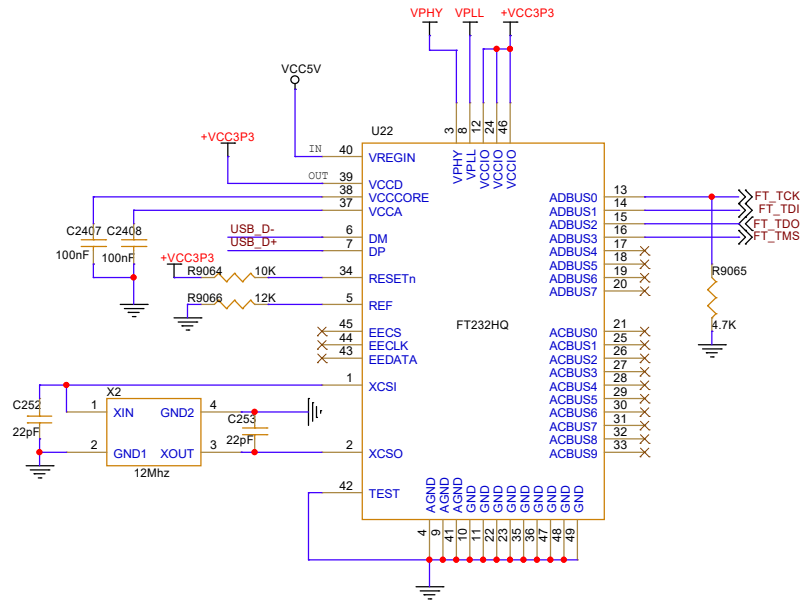
50M-GCLK



Title		
DK_GW5AT-LV138FPG676A		
Size	Document Number	Rev
A3	CLOCK	V2.1
Date:	Thursday, December 05, 2024	Sheet 14 of 25

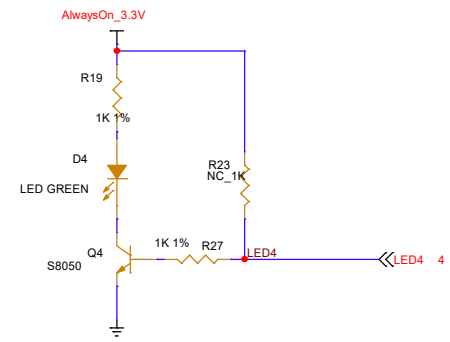
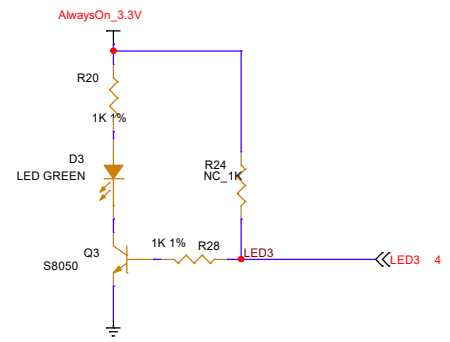
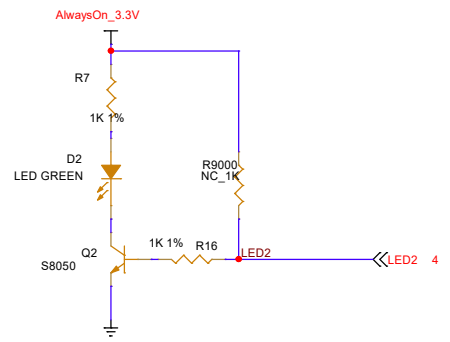
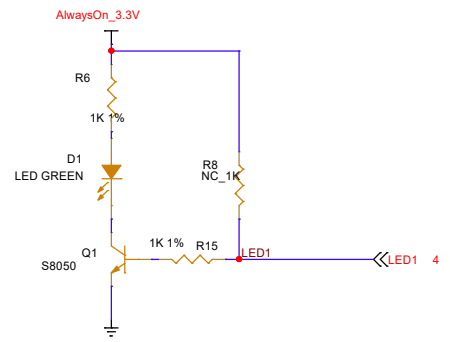
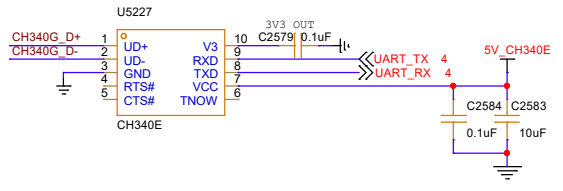
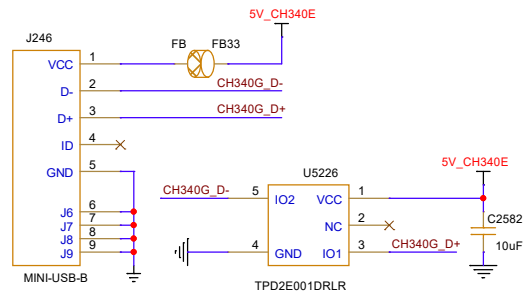


alter:USB_MINI_B_9R00_9R90_0R50

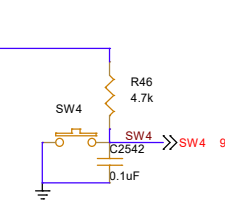
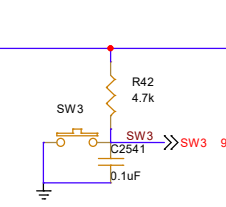
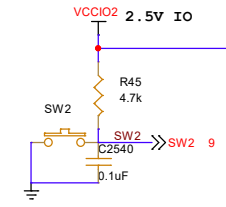
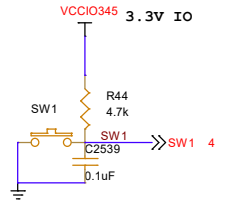


Title		
DK_GW5AT-LV138FPG676A		
Size	Document Number	Rev
A3	USB-JTAG_FT232HQ	V2.1
Date:	Thursday, December 05, 2024	Sheet 15 of 25

USB-UART

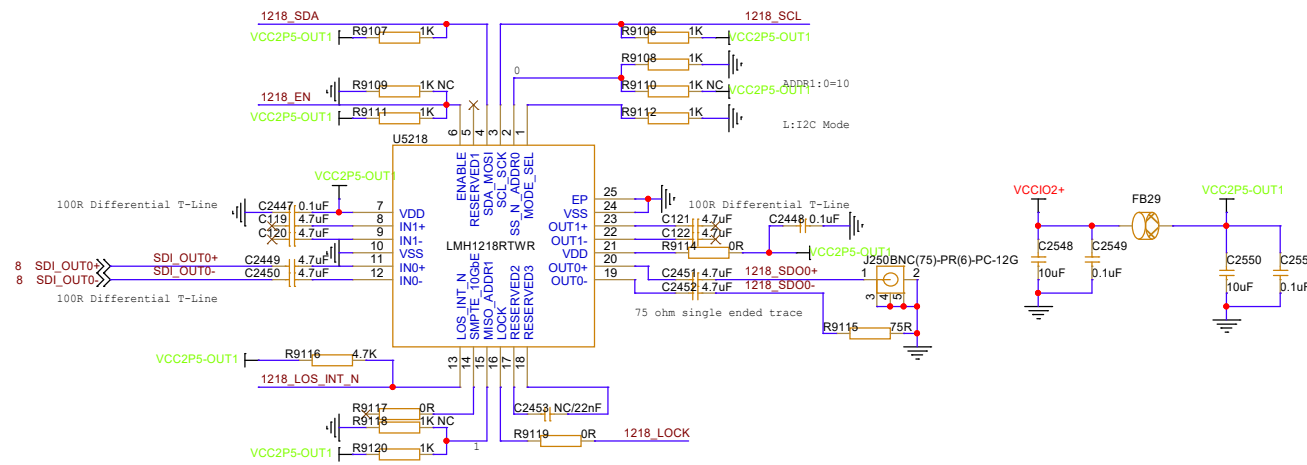


KEY*4



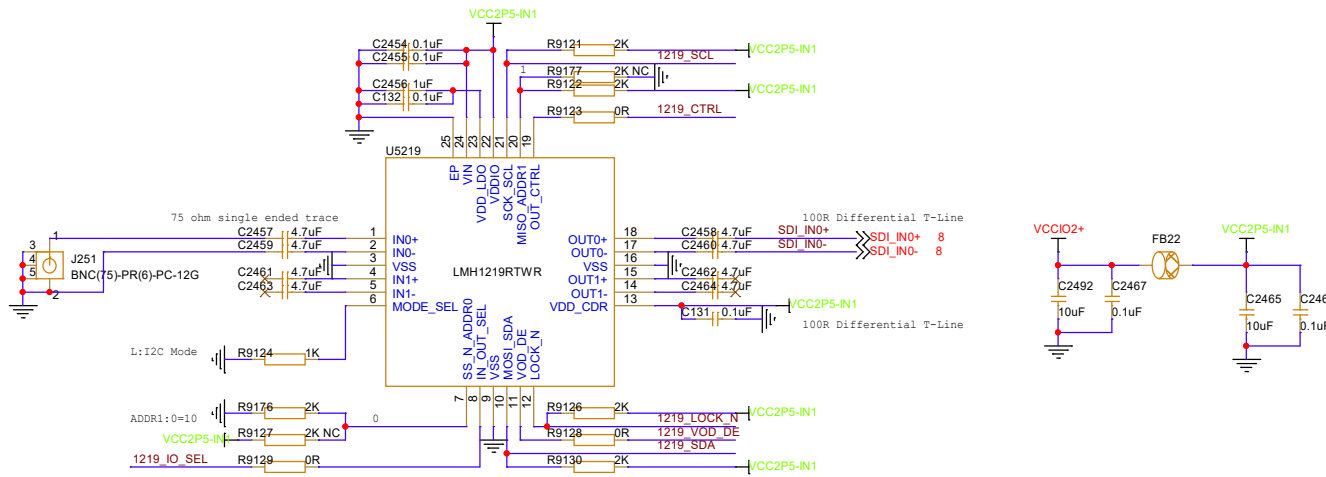
Title		
DK_GW5AT-LV138FPG676A		
Size	Document Number	Rev
A3	USB-UART_LED_KEY	V2.1
Date:	Thursday, December 05, 2024	Sheet 16 of 25

SDI-OUT-6G



- 1218_SDA <-> 1218_SDA 9
- 1218_SCL <-> 1218_SCL 9
- 1218_EN <-> 1218_EN 9
- 1218_LOS_INT_N <-> 1218_LOS_INT_N 9
- 1218_LOCK <-> 1218_LOCK 9

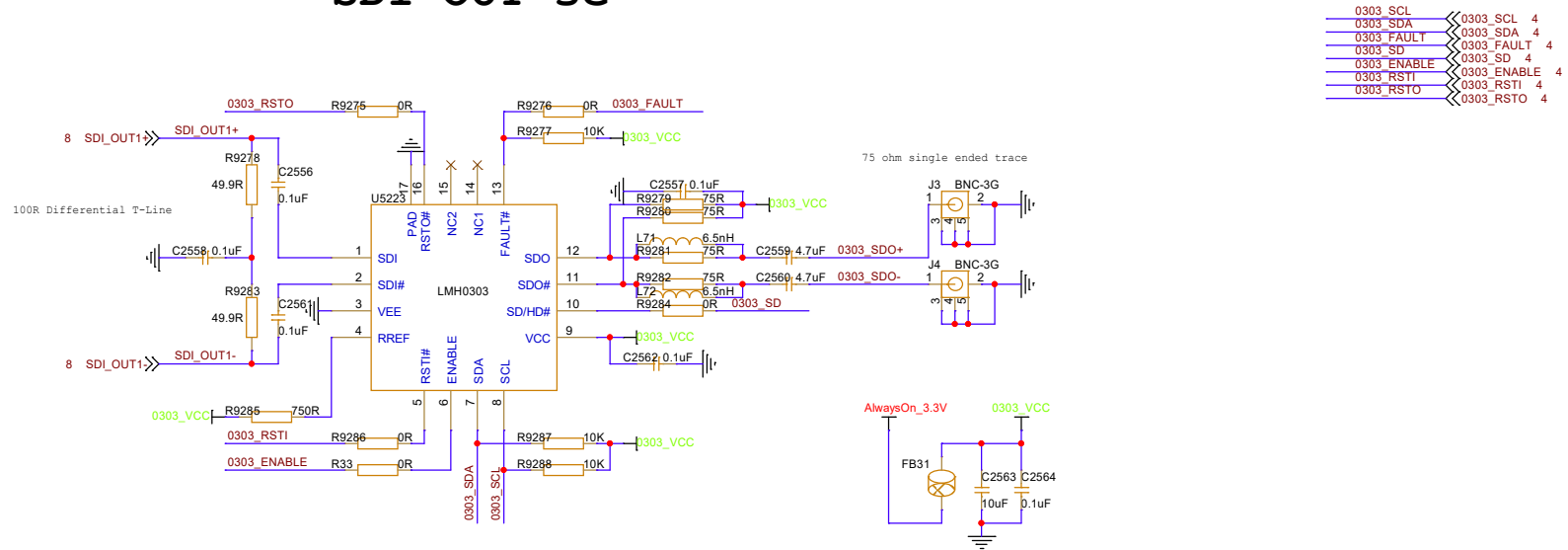
SDI-IN-6G



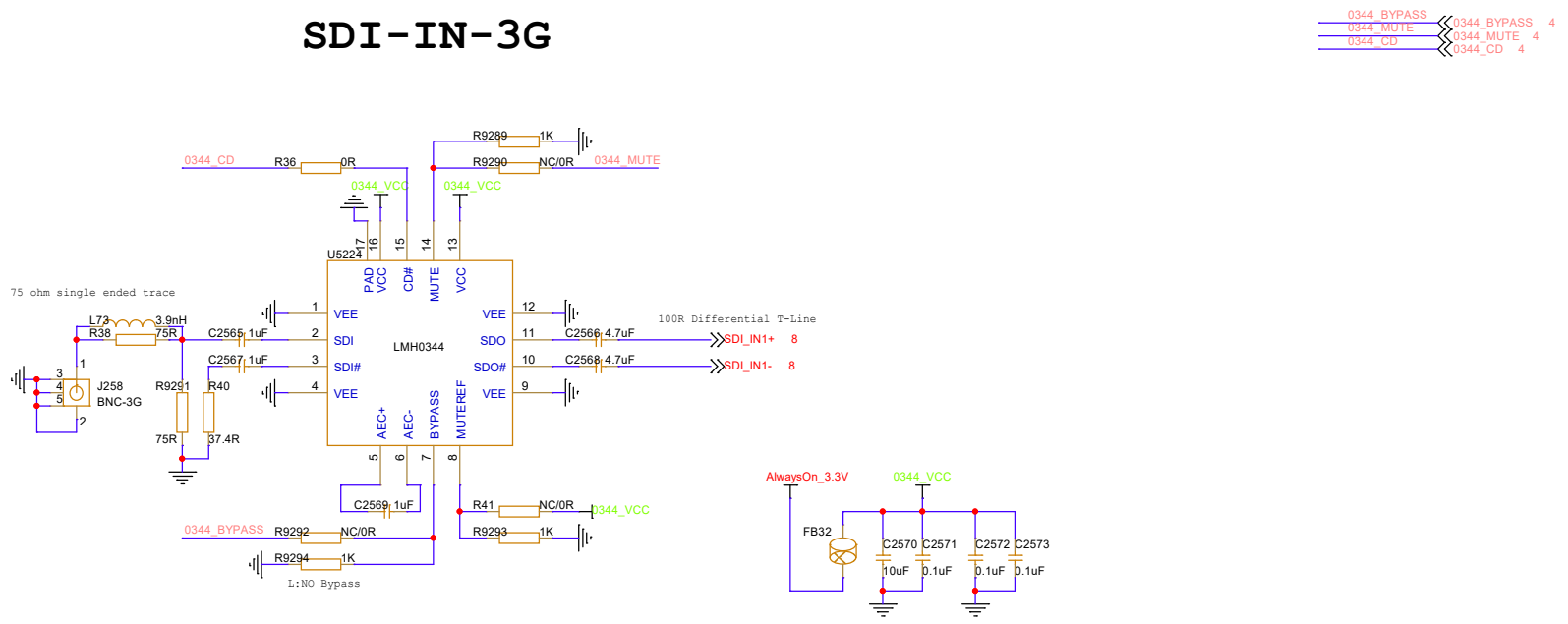
- 1219_SDA <-> 1219_SDA 9
- 1219_SCL <-> 1219_SCL 9
- 1219_IO_SEL <-> 1219_IO_SEL 9
- 1219_CTRL <-> 1219_CTRL 9
- 1219_LOCK_N <-> 1219_LOCK_N 9
- 1219_VOD_DE <-> 1219_VOD_DE 9

Title		
DK_GW5AT-LV138FPG676A		
Size	Document Number	Rev
A3	SDI-OUT/IN-6G	V2.1
Date:	Thursday, December 05, 2024	Sheet 17 of 25

SDI-OUT-3G

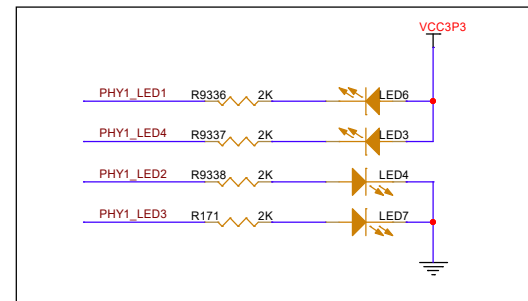
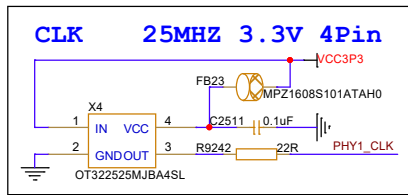
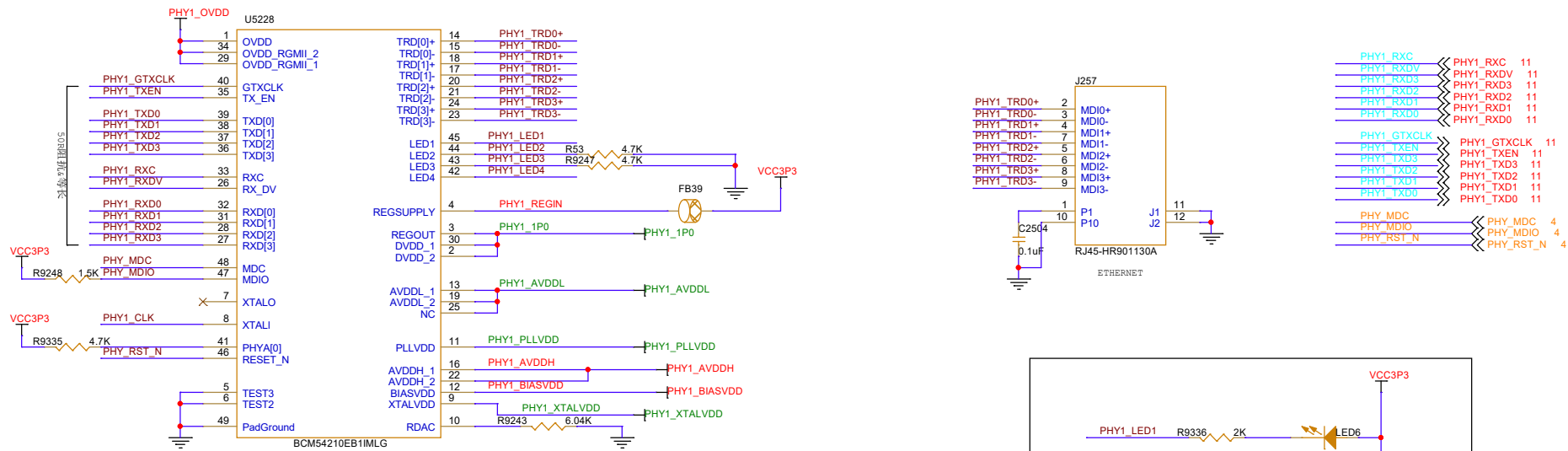


SDI-IN-3G



Title		
DK_GW5AT-LV138FPG676A		
Size	Document Number	Rev
A3	SDI-OUT/IN-3G	V2.1
Date:	Thursday, December 05, 2024	Sheet 18 of 25

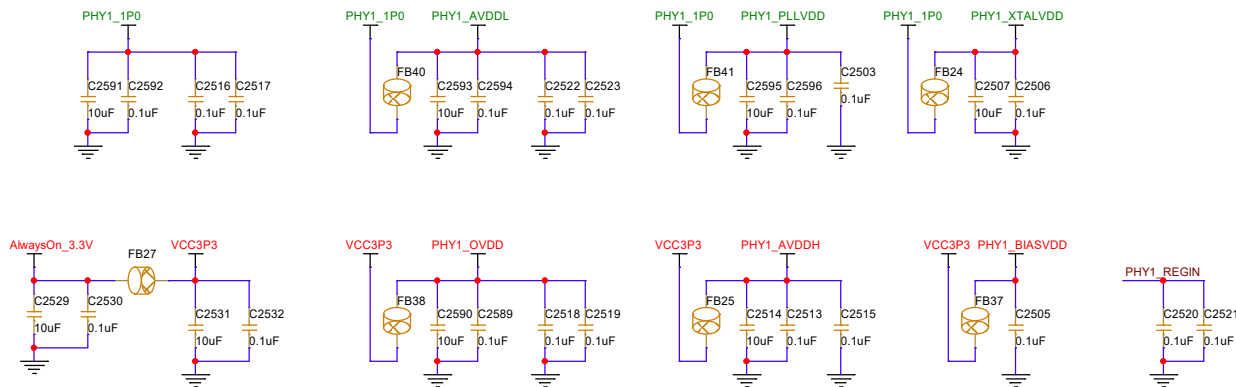
BCM54210E_RGMII



配置信号

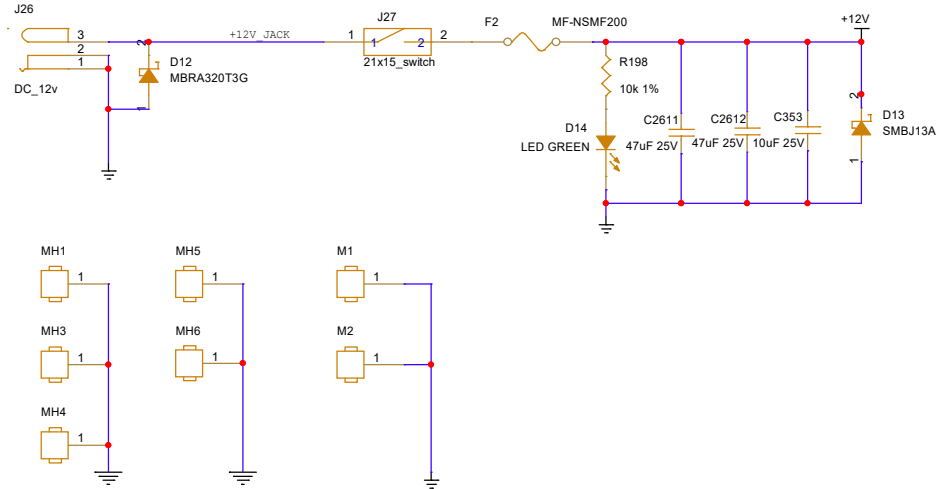
Default-LED Mode (Non-LOM-LED mode):			
Status	LED[2]	LED[1]	
100BASE-T	ON	ON	
100BASE-T	ON	OFF	
10BASE-T	OFF	ON	
No link	OFF	OFF	

Set PHY Address as required.
 TEST3/TEST2 = 00, PHY[A] = 0: PHY address = 00000.
 TEST3/TEST2 = 00, PHY[A] = 1: PHY address = 00001.

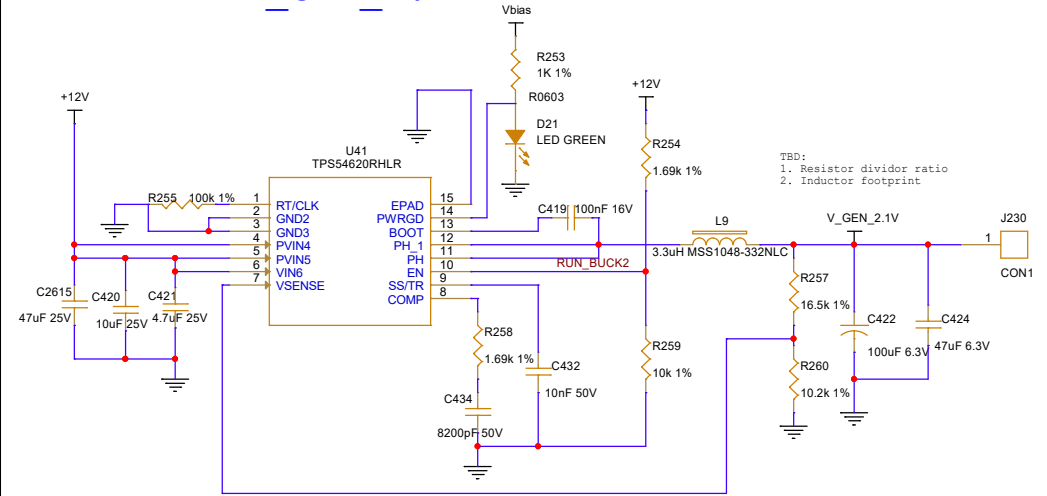


Title			DK_GW5AT-LV138FPG676A
Size	Document Number	Rev	
A3	GPHY_BCM54210S	V2.1	
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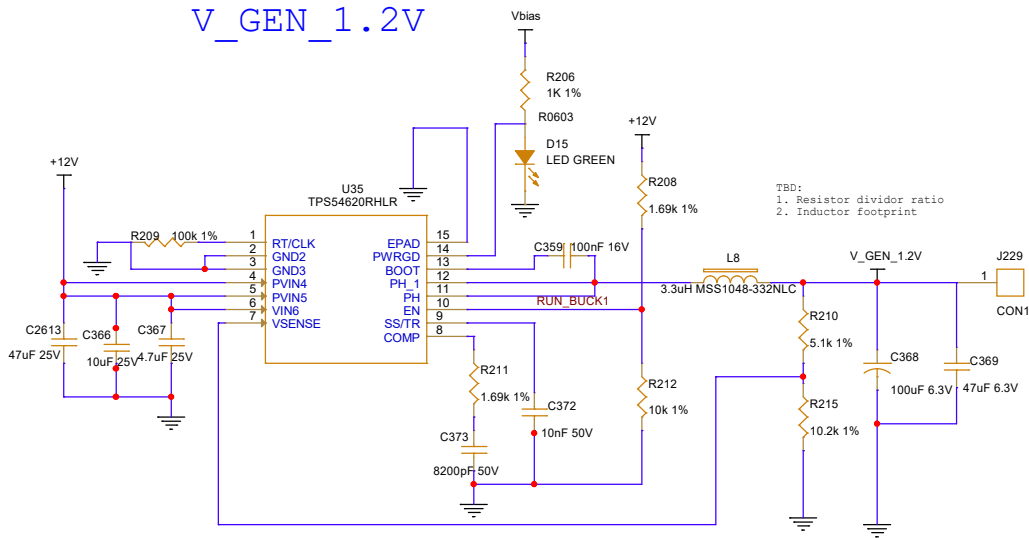
12V Power Supply



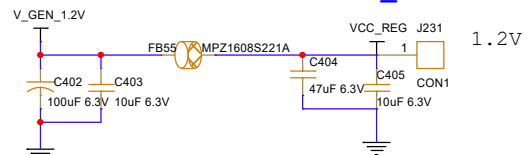
V_GEN_2.1V



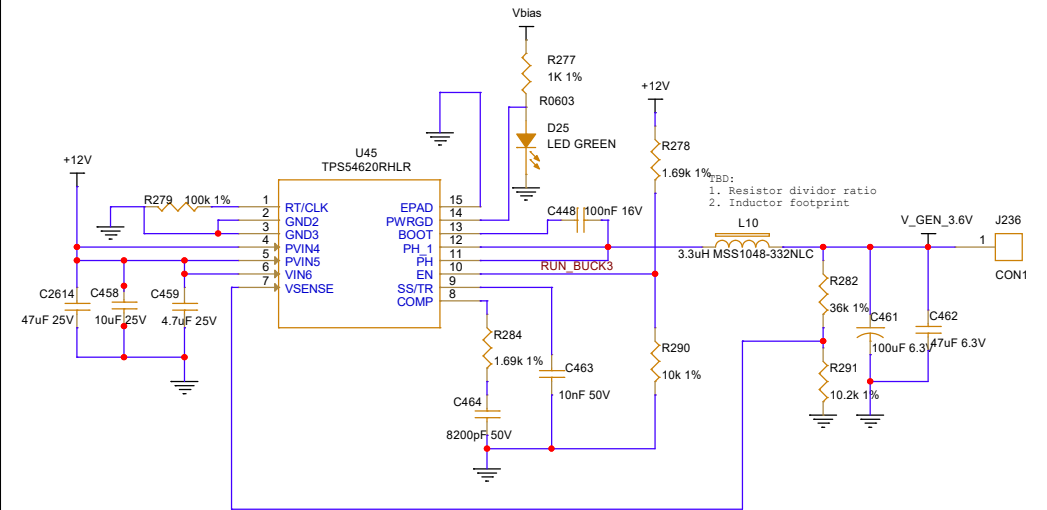
V_GEN_1.2V



VCC_REG

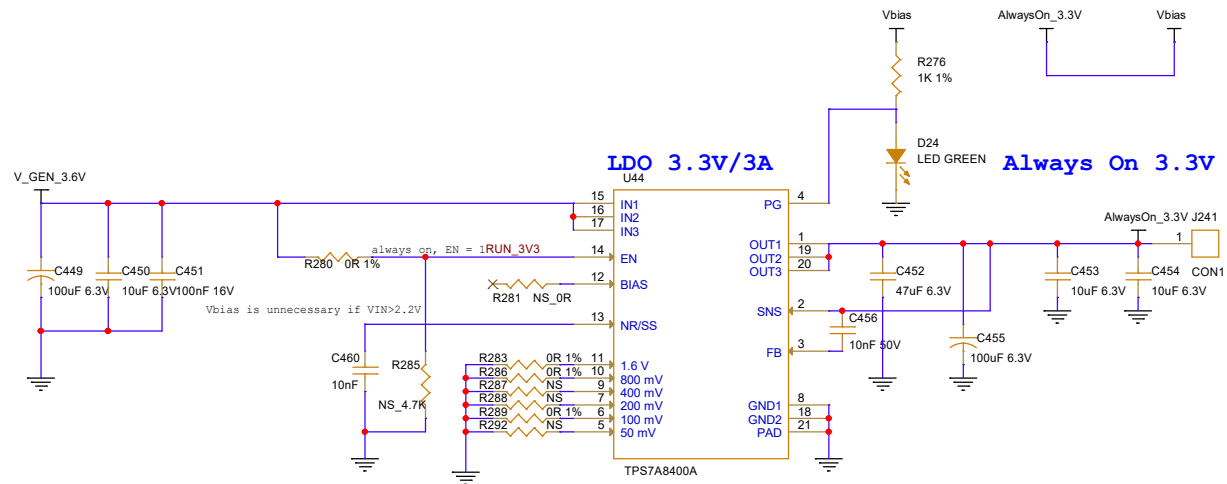


V_GEN_3.6V



Title		DK_GW5AT-LV138FPG676A
Size	Document Number	POWERIN_1V2_2V1_3V6
A3	Date:	Thursday, December 05, 2024
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	Rev	V2.1

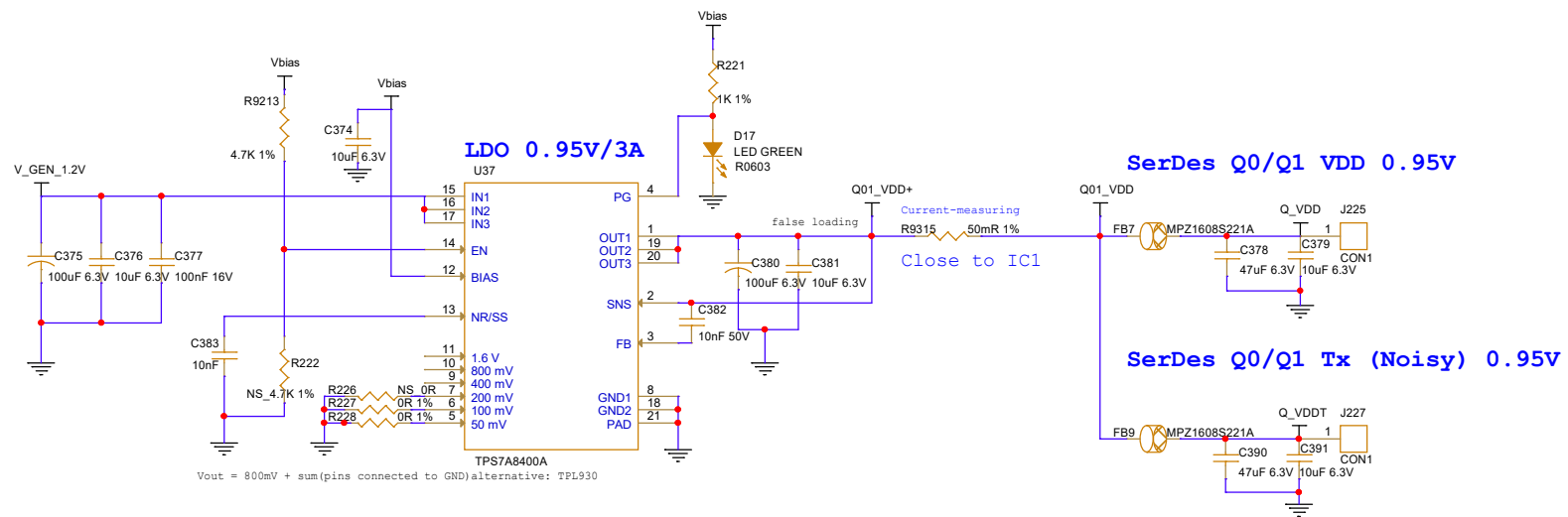
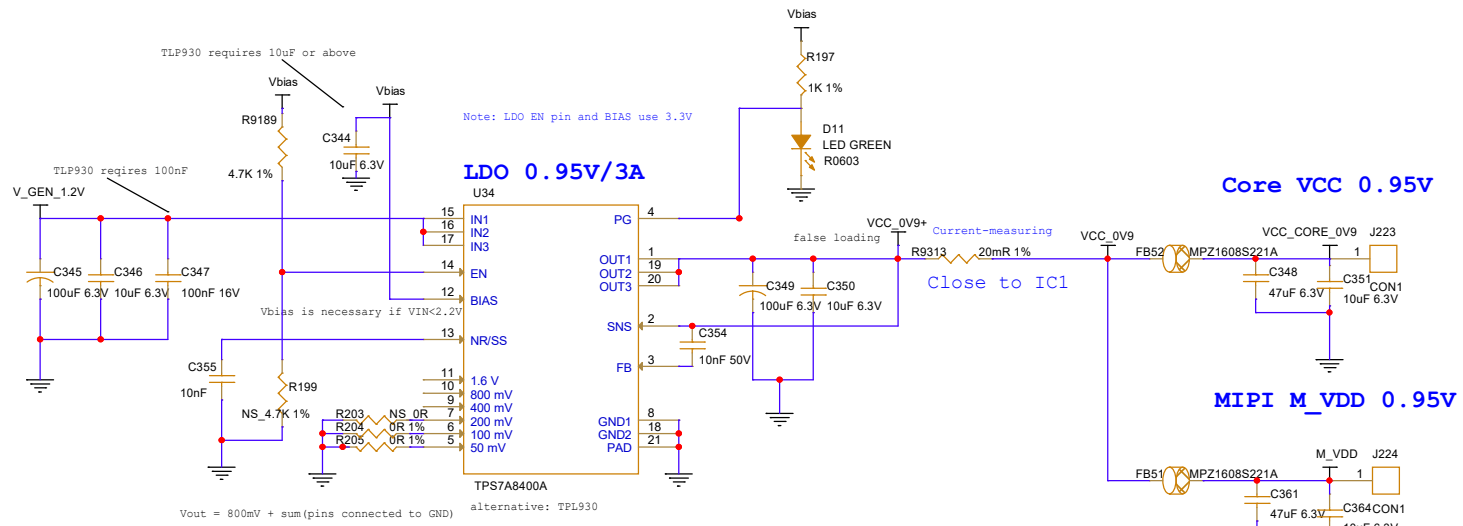
Provide 3.3V Bias Always On LDO



$V_{out} = 800mV + \text{sum}(\text{pins connected to GND})$ alternative: TPL930
 $V_{out} = 800mV + \text{sum}(1600+800+100)$

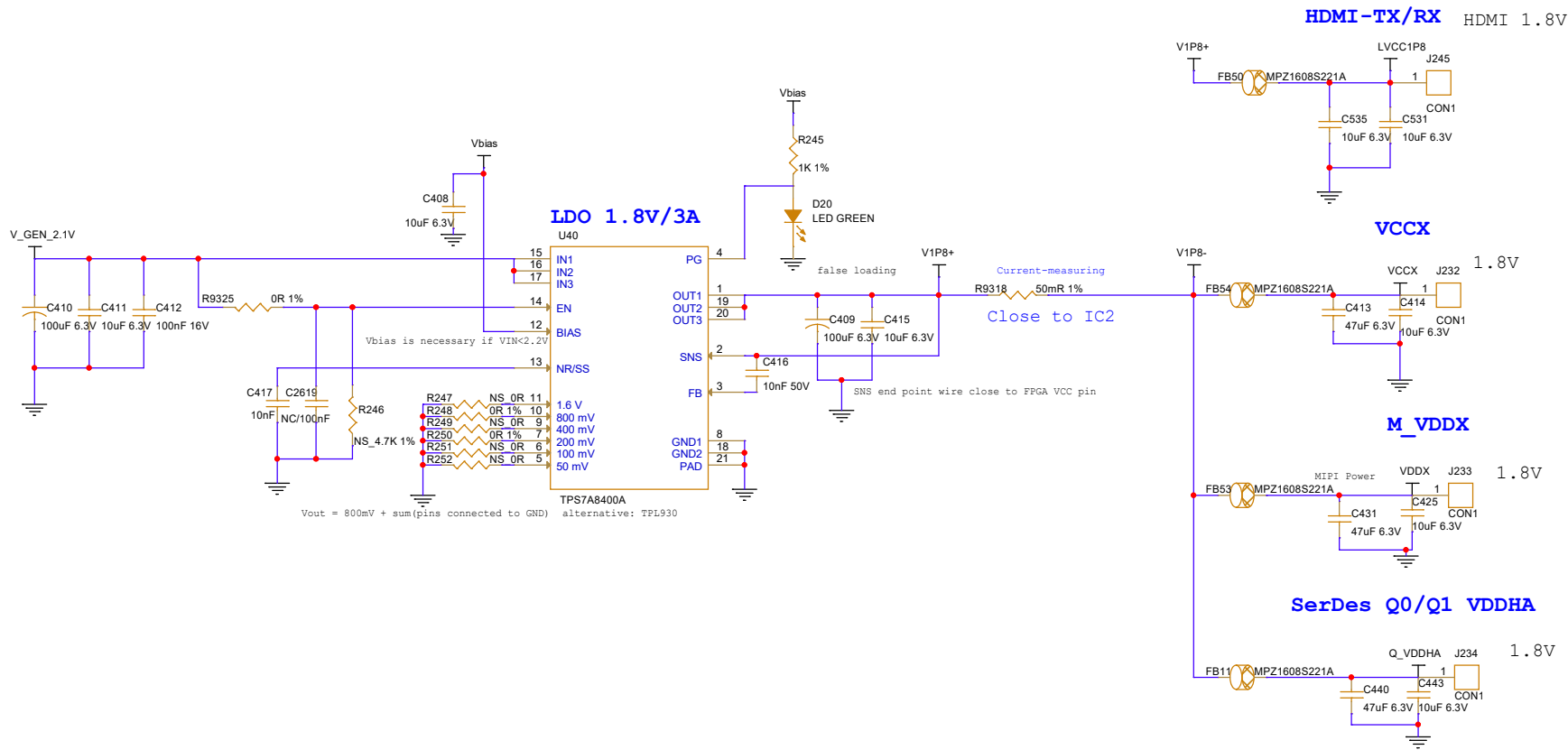
Title		
DK_GW5AT-LV138FPG676A		
Size	Document Number	Rev
A3	POWER_AON3V3	V2.1
Date:	Thursday, December 05, 2024	Sheet 21 of 25

0.95V Power Supply



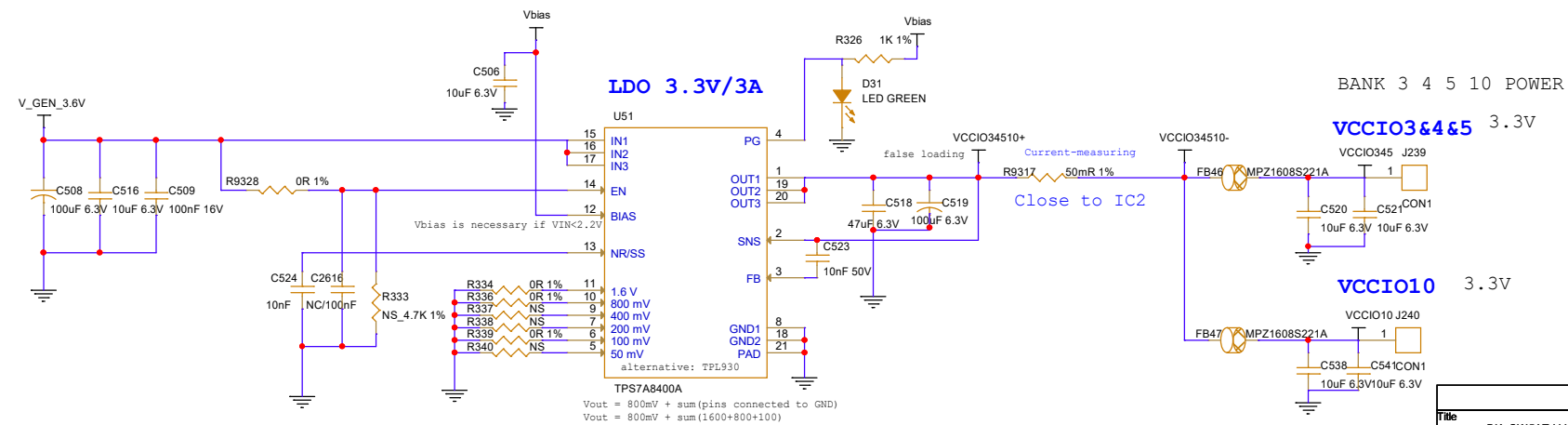
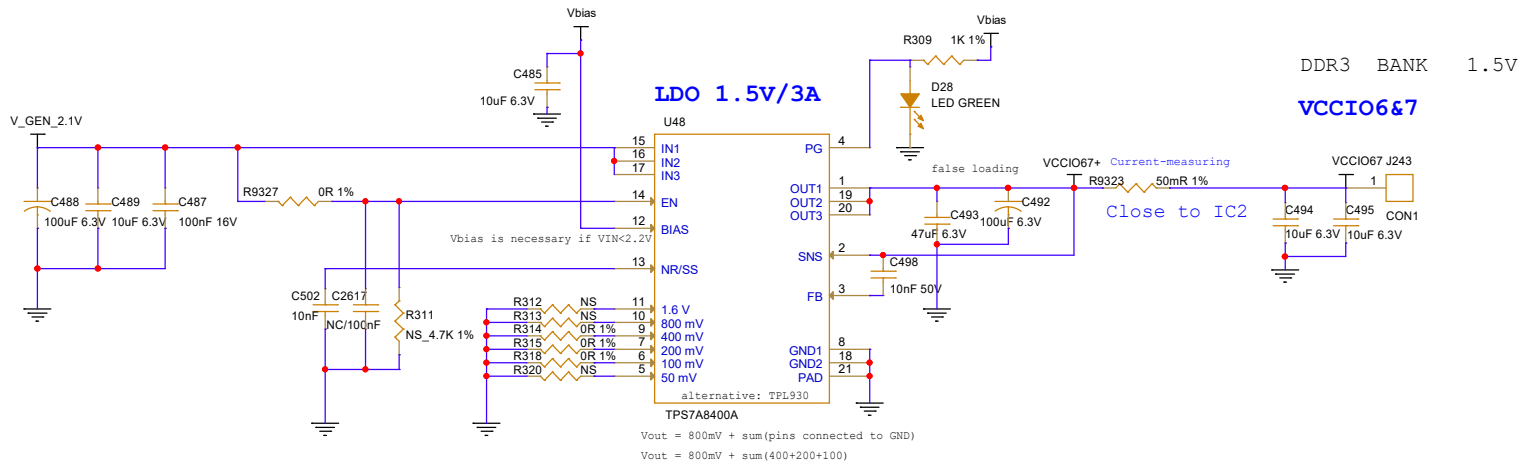
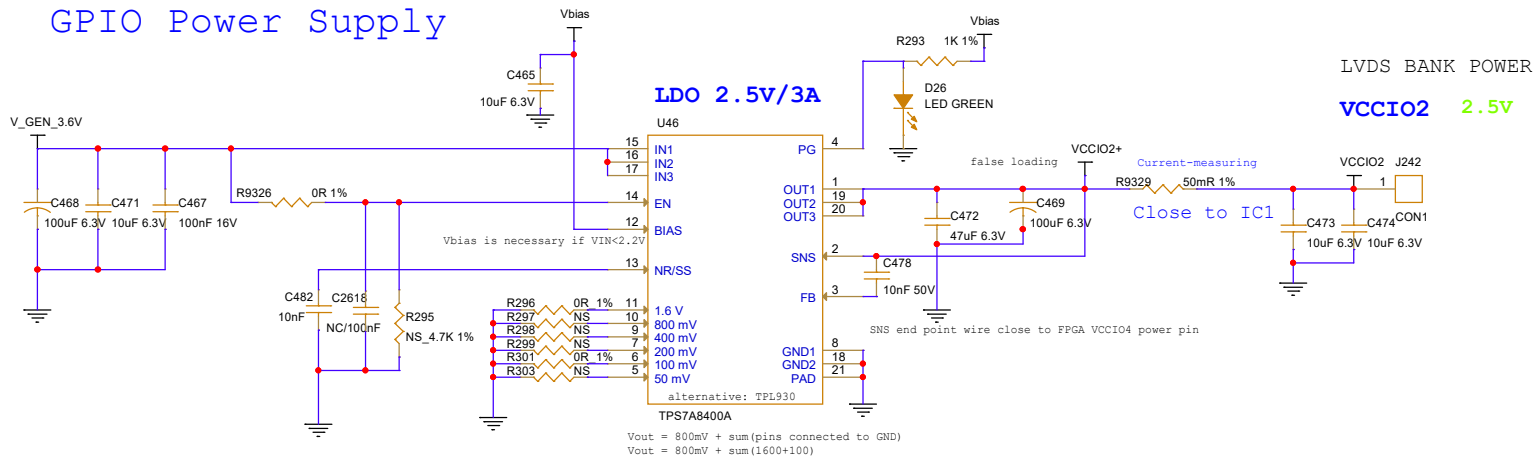
Title		
DK_GW5AT-LV138FPG676A		
Size	Document Number	Rev
A3	POWER_0V95	V2.1
Date:	Thursday, December 05, 2024	Sheet 22 of 25

1.8V Power Supply



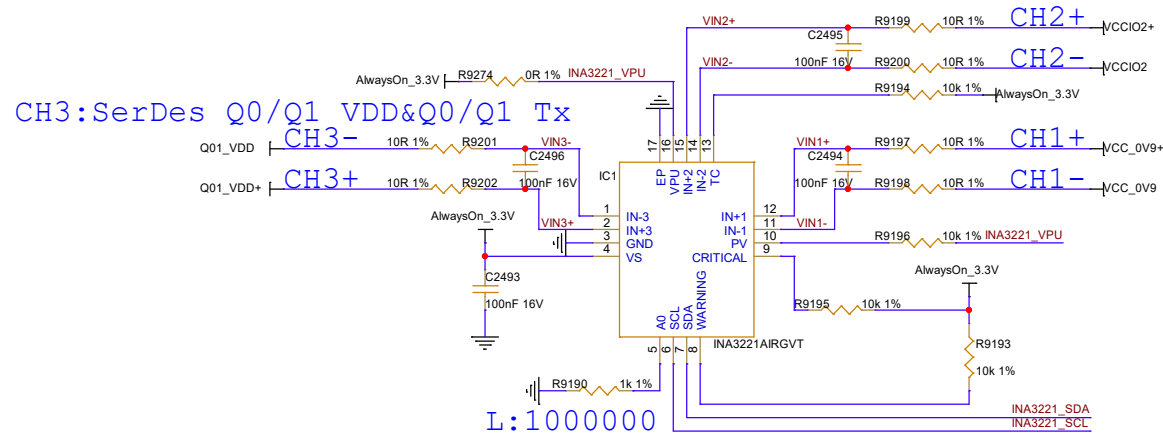
Title		
DK_GW5AT-LV138FPG676A		
Size	Document Number	Rev
A3	POWER_1V2_1V8	V2.1
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GPIO Power Supply



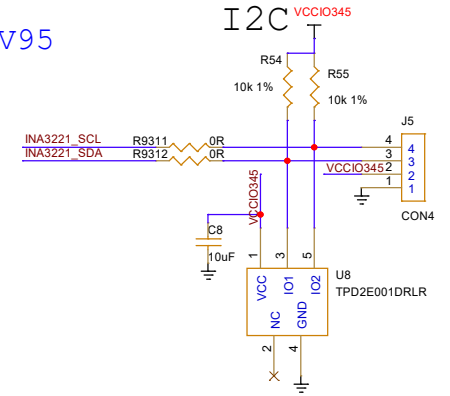
Title		
DK_GW5AT-LV138FPG676A		
Size	Document Number	Rev
A3	POWER_GPIO_2V5_1V5_3V3	V2.1
Date:	Thursday, December 05, 2024	Sheet 24 of 25

Current-measuring*3CH



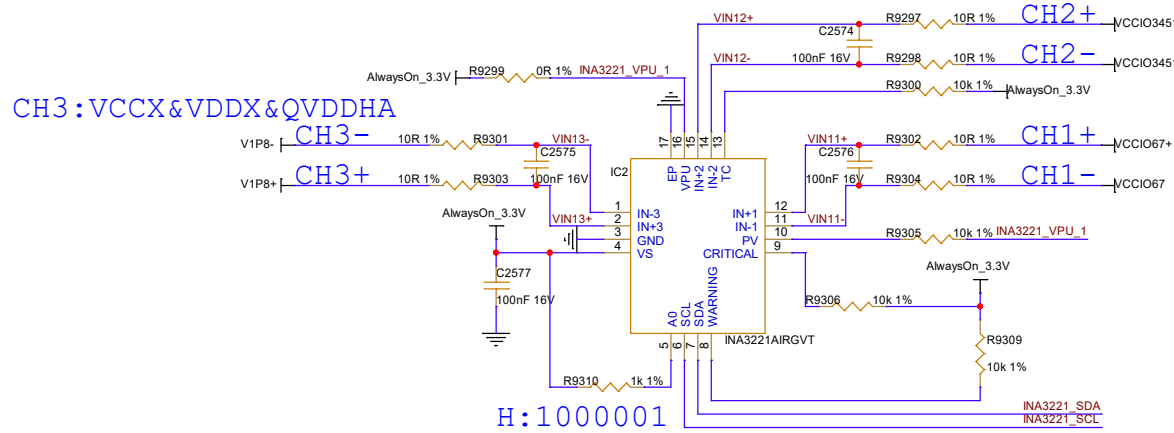
CH2:VCCIO2-2.5V

CH1:VCC_CORE_0V95



$R_{shunt} < V_{sense_max} / I_{max}$

Current-measuring*3CH



CH2:VCCIO34510-3.3V

CH1:VCCIO67-DDR1.5V

$R_{shunt} < V_{sense_max} / I_{max}$

Title		
DK_GW5AT-LV138FPG676A		
Size	Document Number	Rev
A3	Current_Det_INA3221	V2.1
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