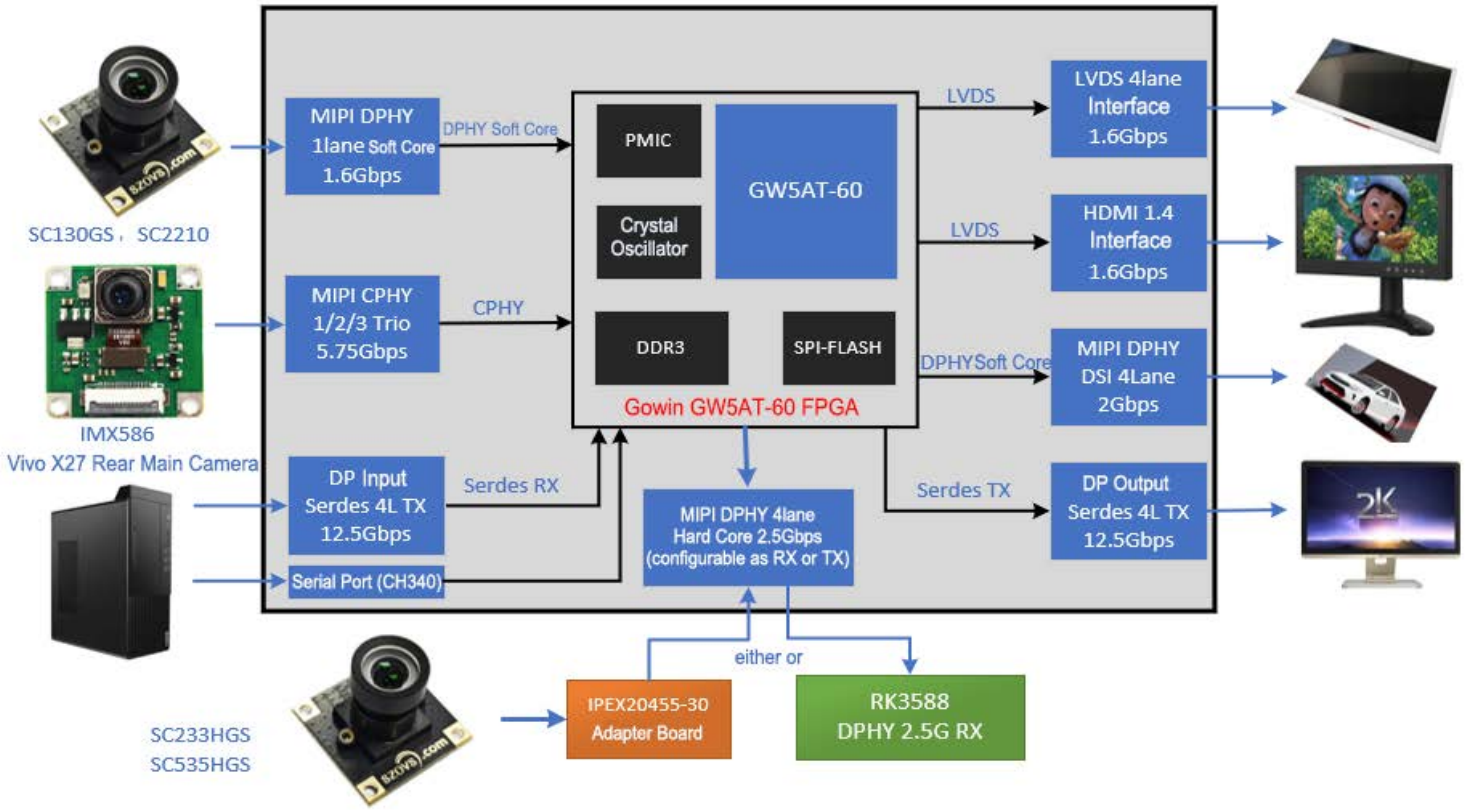
GW5AT-60G FPGA Image Solution



V3
1. Fixed HDMI VTT 2.8V to DSI connect.
2. Added additional 5V power input.
3. Added 5V/3.3V switch resistor for 20455 DPHY.

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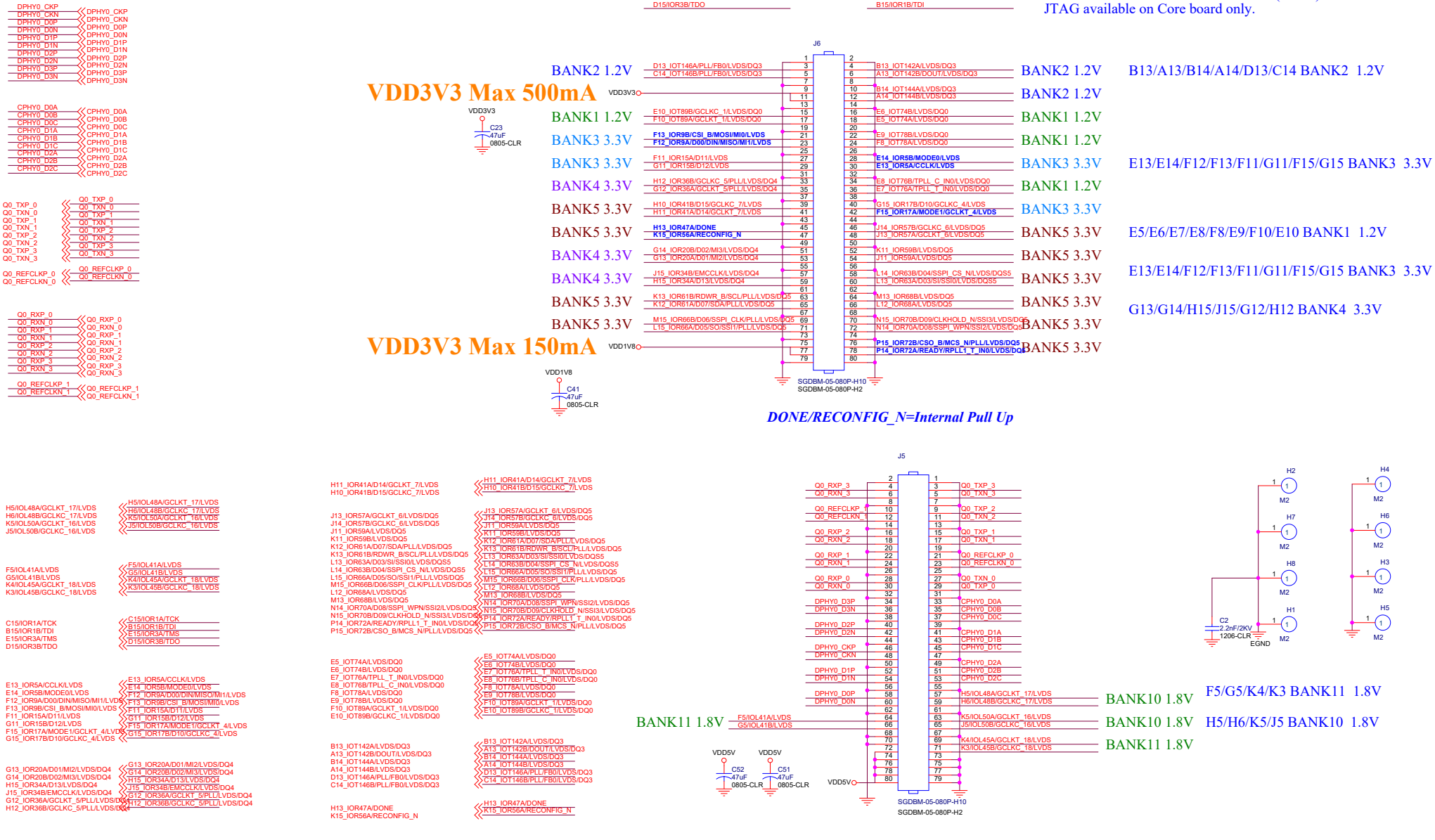
Interface



VDD3V3 Max 500mA

VDD3V3 Max 150mA

BANK2 1.2V

BANK1 1.2V

BANK3 3.3V

BANK4 3.3V

BANK5 3.3V

BANK11 1.8V

BANK10 1.8V

Removed C15/B15/E15/D15 BANK12 (JTAG) 3.3V
JTAG available on Core board only.

B13/A13/B14/A14/D13/C14 BANK2 1.2V

E13/E14/F12/F13/F11/G11/F15/G15 BANK3 3.3V

E5/E6/E7/E8/F8/E9/F10/E10 BANK1 1.2V

E13/E14/F12/F13/F11/G11/F15/G15 BANK3 3.3V

G13/G14/H15/J15/G12/H12 BANK4 3.3V

F5/G5/K4/K3 BANK11 1.8V

H5/H6/K5/J5 BANK10 1.8V

DONE/RECONFIG_N=Internal Pull Up

1. Restricted usage on E14/F15. MODE0 must be pulled high, F15 must be pulled low. Incorrect states are not allowed.

2. Configuration Flash Pins E13, F12, F13, P15 are not recommended to be used.

3. P14 may be used without restriction.

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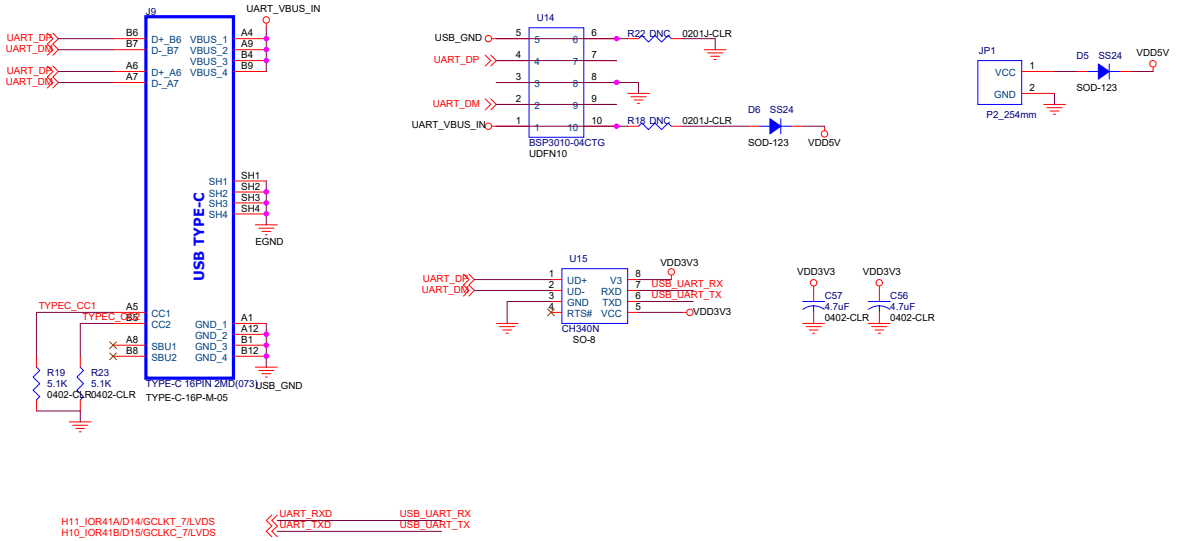
Power & UART



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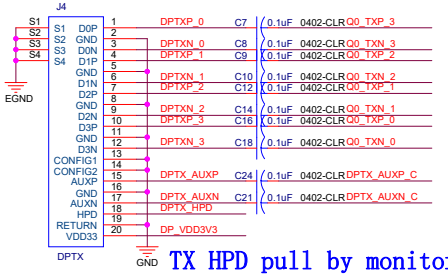
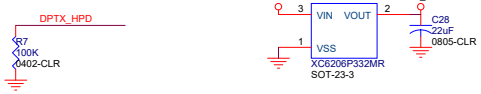
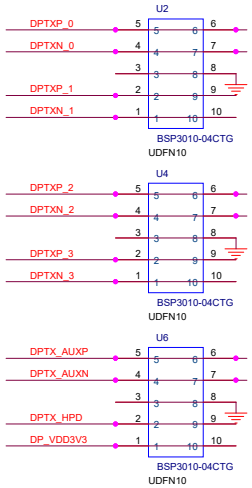
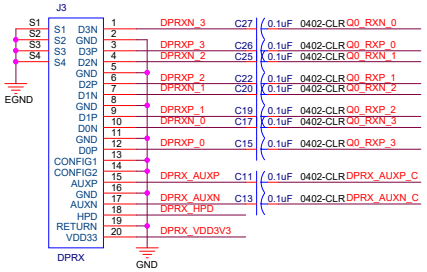
DP TX & RX



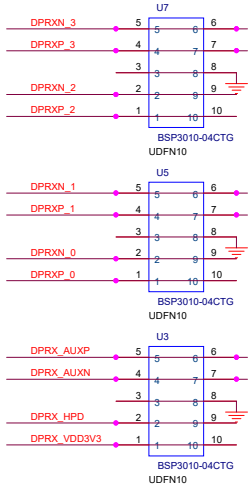
TX HPD pull by monitor

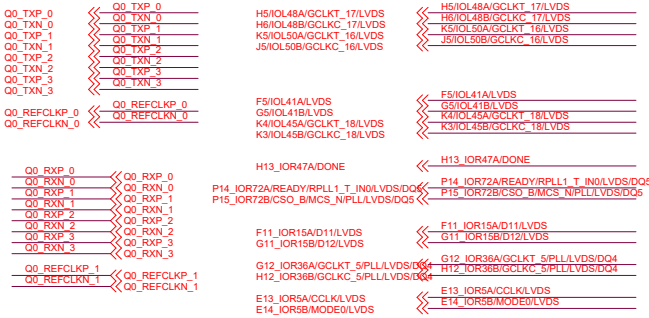


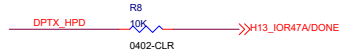




DPRX Pinout Different Than DPTX
Invert P/N for Q0_RX Lanes.

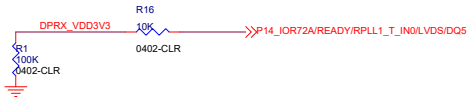




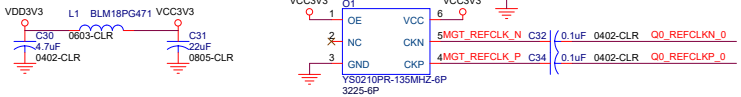


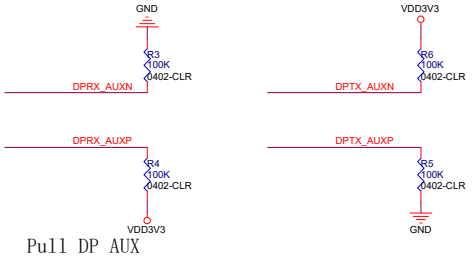
DP TX HPD Detect:
Asserted when DPTX_HPD is high.

RX HPD Pull by FPGA.



DP RX HPD Detect:
Asserted when DPRX_VDD3V3 is high.





Pull DP AUX

Place TERM Resistor (240R) to Core Header

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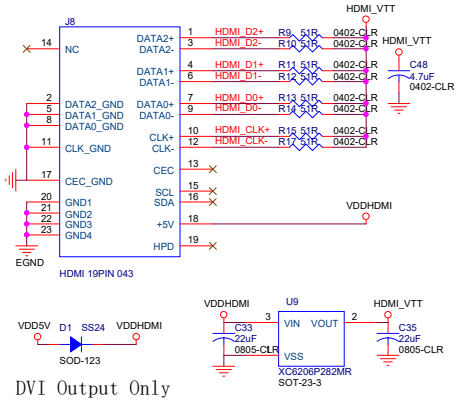
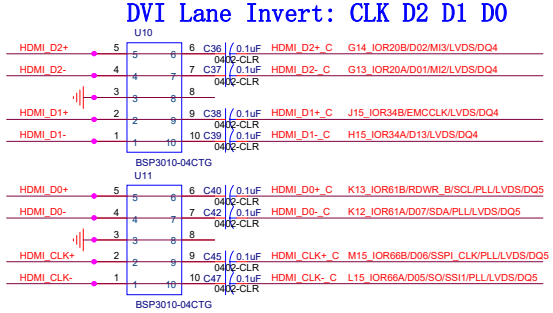
LVDS & DVI

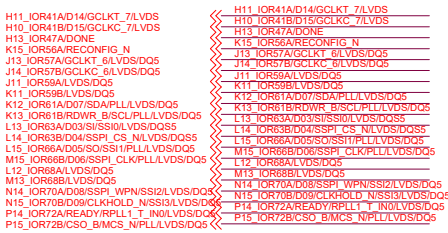


DVI Output Only

DVI Lane Invert: CLK D2 D1 D0



DONE/RECONFIG_N=Internal Pull Up



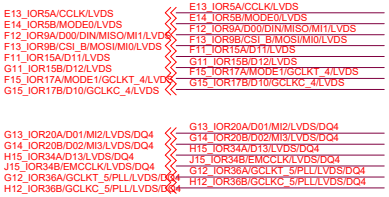
H5/H6/K5/J5 BANK10

F5/G5/K4/K3 BANK11

BANK 10 & 11 1.8V IO

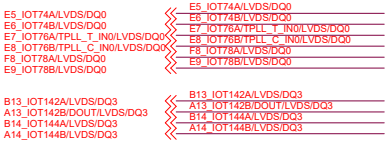
E13/E14/F12/F13/F11/G11/F15/G15 BANK3

G13/G14/H15/J15/G12/H12 BANK4



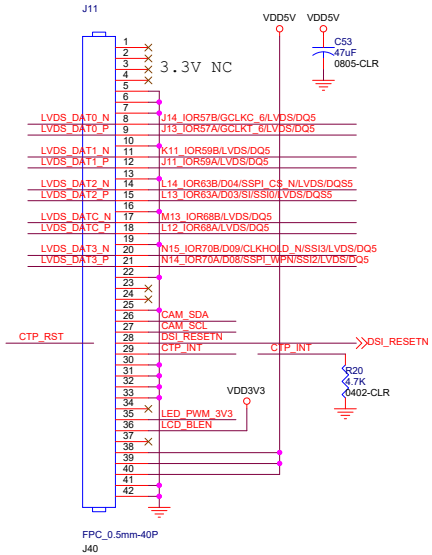
E5/E6/E7/E8/F8/E9 BANK1

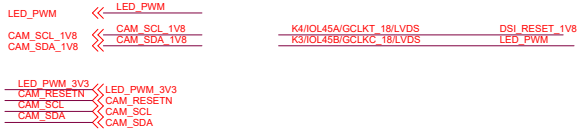
B13/A13/B14/A14 BANK2



BANK 1 & 2 1.2V MIPI IO

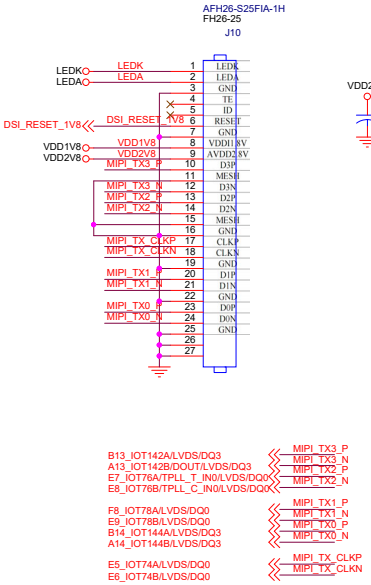
LVDS Lane Invert: None

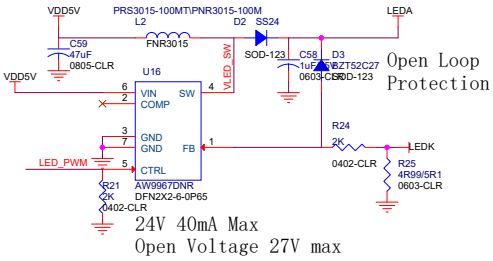




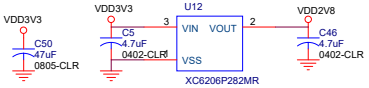
1.8V / 3.3V I2C

DSI Lane Invert: None





1.8V from Core Board directly.



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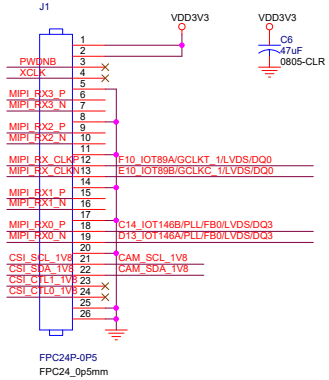
Soft MIPI CSI



Ext Trig Not Supported.

F10_IOT89A/GCLKT_1/LVDS/DQ0
E10_IOT89B/GCLKC_1/LVDS/DQ0
D13_IOT146A/PLL/FB0/LVDS/DQ3
C14_IOT146B/PLL/FB0/LVDS/DQ3

BANK 1 & 2 1.2V MIPI IO Reserved Pins

CAM_SCL_1V8
CAM_SDA_1V8

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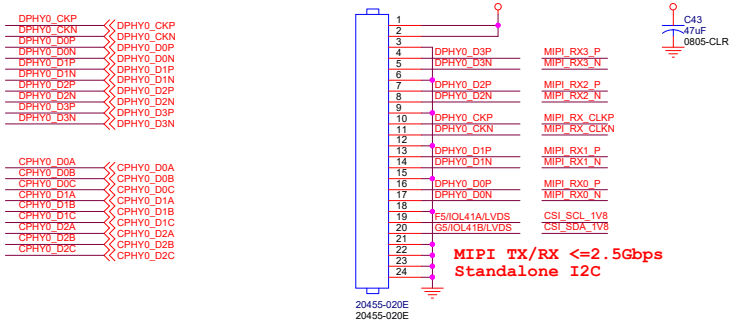
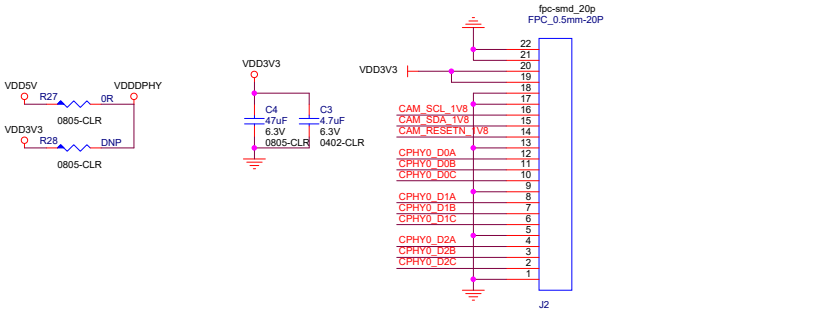
CPHY & DPHY

MIPI Hard DPHY
Connect 5V Input.



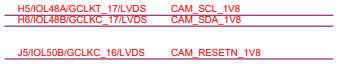
CPHY Use FB35K

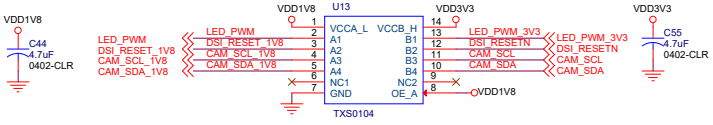


H5/H6/K5/J5 BANK10

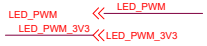
F5/G5/K4/K3 BANK11

BANK 10 & 11 1.8V IO





Shared SCL / SDA / RESETN / REFCLK Level Shift



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