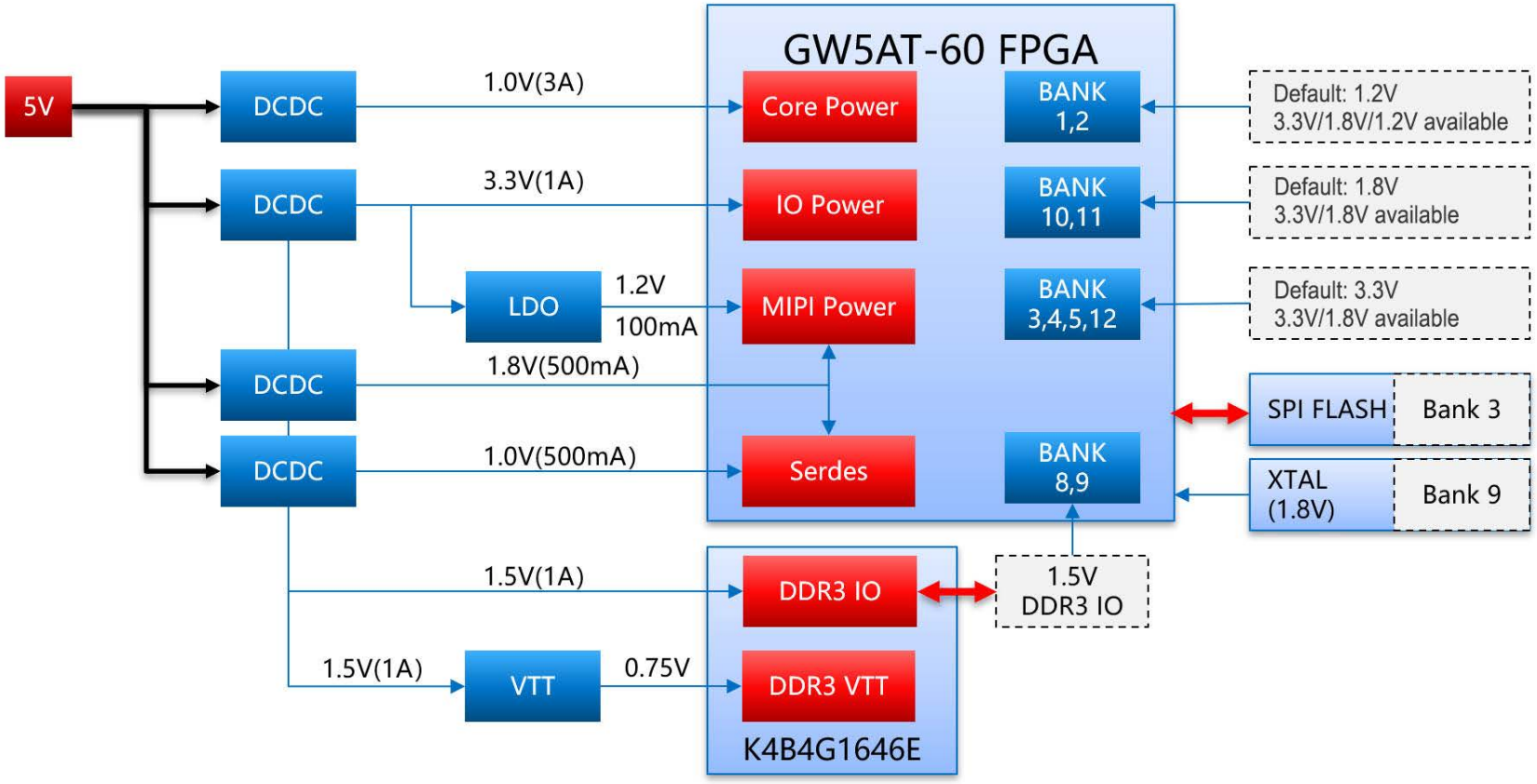
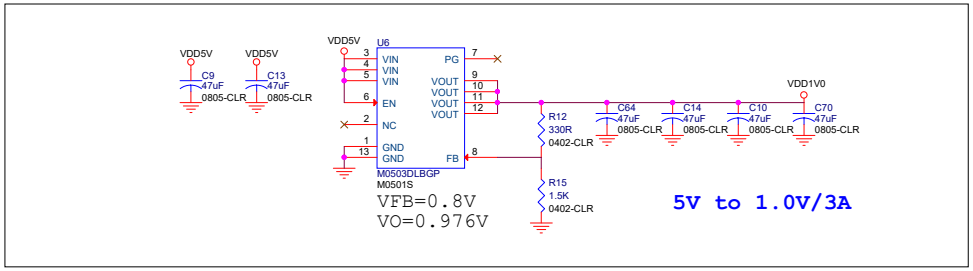


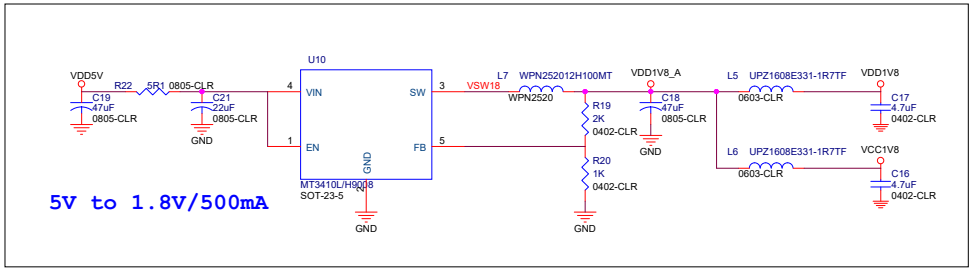
V2

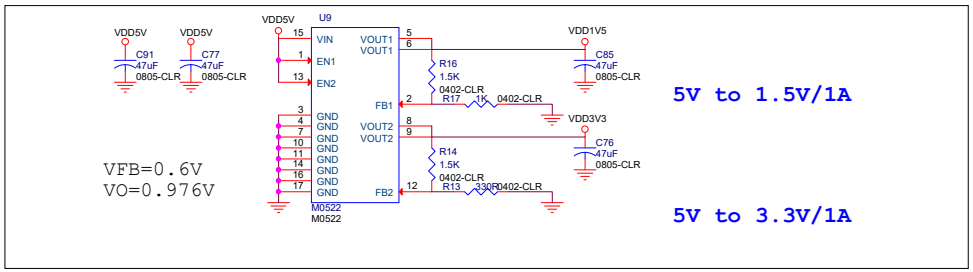
1. Added 1.2V for Bank 1 & 2.
2. Fix DDR CK P/N Swap issue. The clock pair on DDR3 chip is swapped accidentally.
3. Add 3.3V LED.
4. Removed 809 connection to RECONFIGN. Connects to READY.
5. Changed flash to SO-8 150mil part.

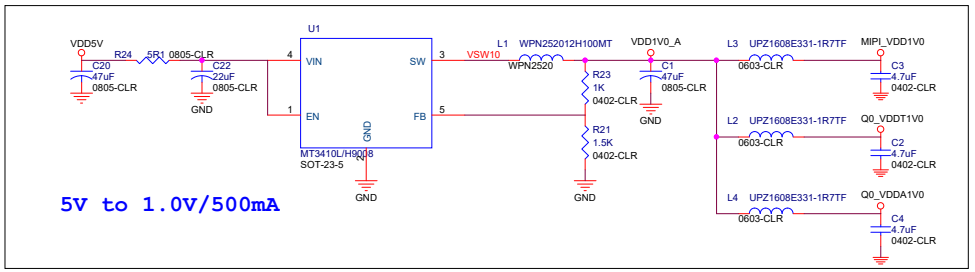
	https://www.szovs.com	
Title	DK_DP_GW5AT-LV60UG225	
Size	Document Number Block Design	Rev 1.0
Date:	Monday, February 17, 2025	Sheet 1 of 7

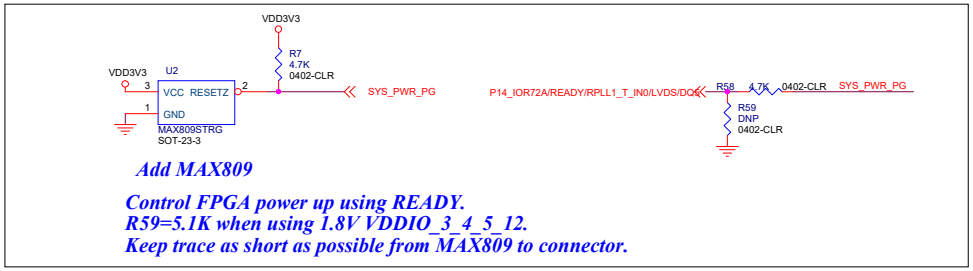
SOM POWER

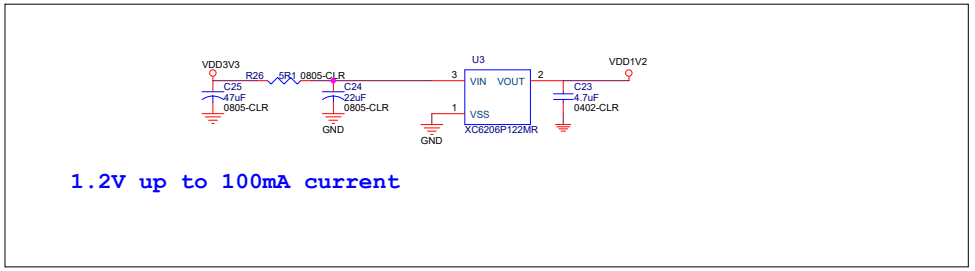






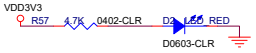


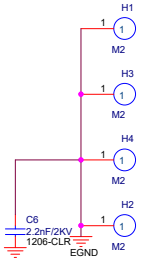




Power Tree

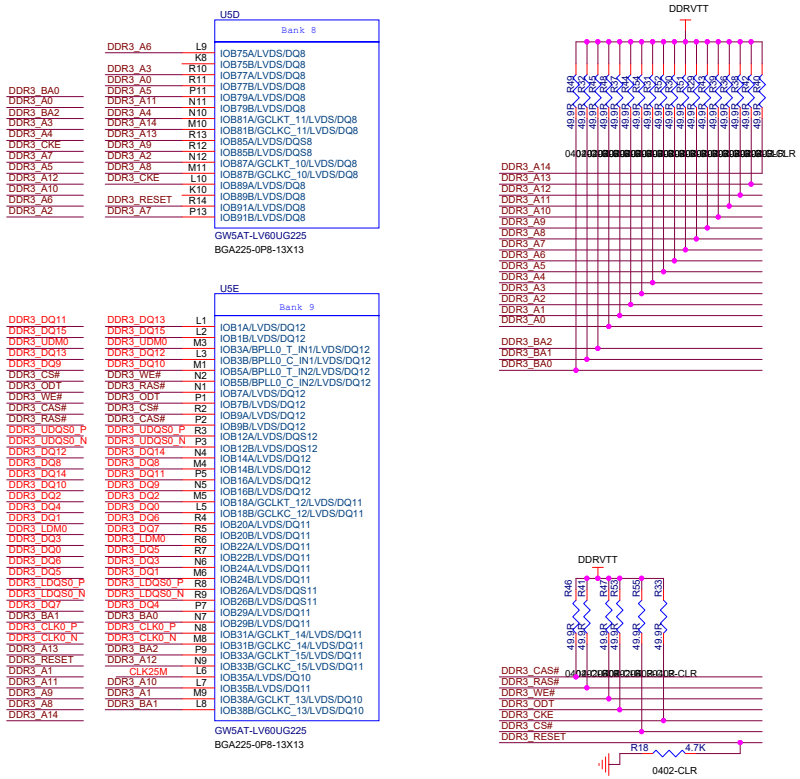
```
5V -----> 3.3V 1A DCDC (Shared M0522) (IO)    --> 1.2V 200mA LDO (XC6206) (MIPI LP)
      |
      |--> 1.5V 1A DCDC (Shared M0522) (DDR3) --> 0.75V VTT (SGM2054)
      |
      |--> 1.0V 3A DCDC (M0503) (Core)
      |
      |--> 1.8V 500mA DCDC (MT3410L Low Ripple) (SERDES / MIPI)
      |
      |--> 1.0V 500mA DCDC (MT3410L Low Ripple) (SERDES)
```

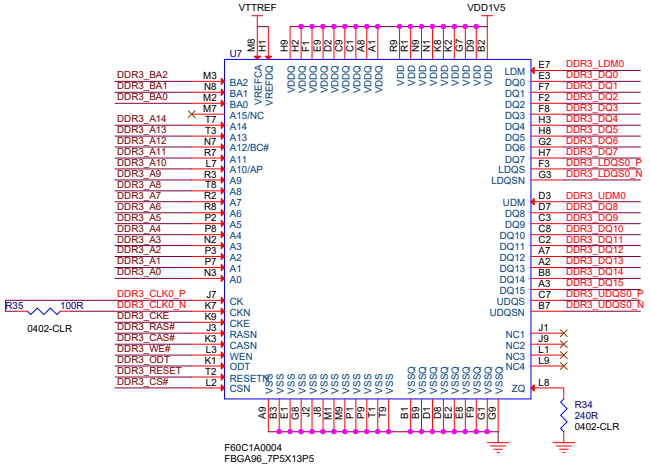


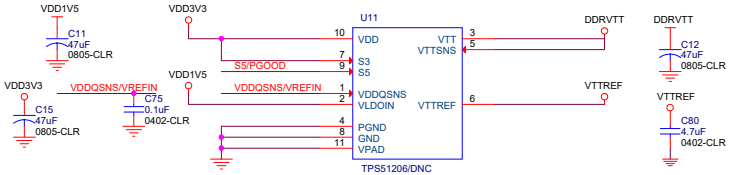


	https://www.szovs.com	
Title	DK_DP_GW5AT-LV60UG225	SZOVS GOWIN
Size	Document Number SOM Power_Module V1.0	Rev 1.0
Date:	Monday, February 17, 2025	Sheet 2 of 7

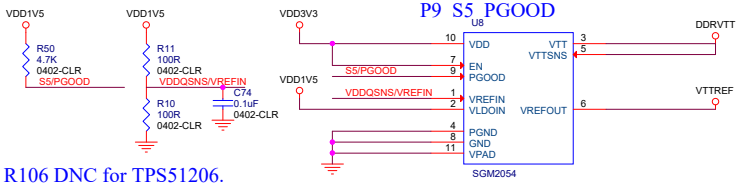
DDR3



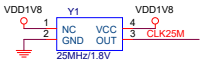


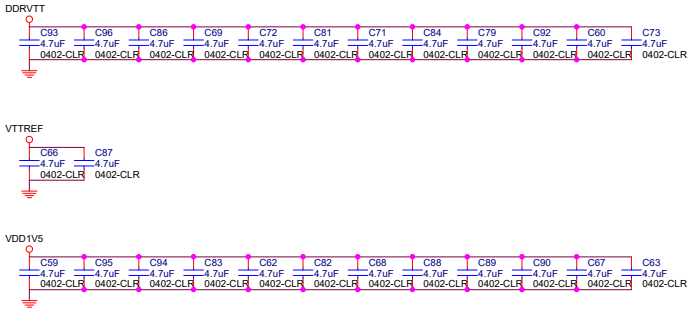


TPS51206 VS SGM2054
P1 VDDQSNS VREFIN
P9 S5_PGOOD



R106 DNC for TPS51206.

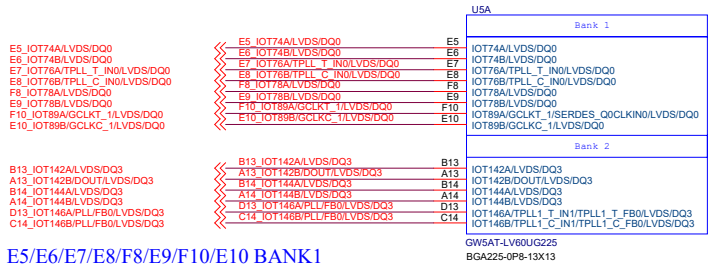




https://www.szovs.com

Title	DK_DP_GW5AT-LV60UG225	
Size	Document Number FPGA DDR3_Module V1.0	Rev 1.0
Date: Friday, February 14, 2025	Sheet 3 of 7	

FPGA IO

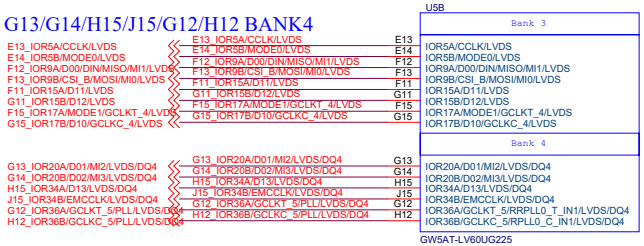


E5/E6/E7/E8/F8/E9/F10/E10 BANK1

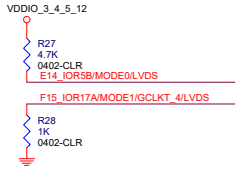
B13/A13/B14/A14/D13/C14 BANK2

E13/E14/F12/F13/F11/G11/F15/G15 BANK3

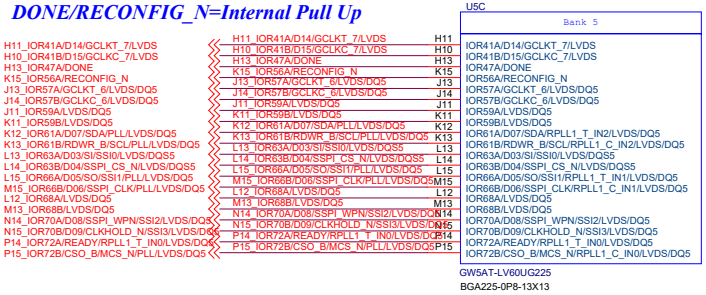
G13/G14/H15/J15/G12/H12 BANK4

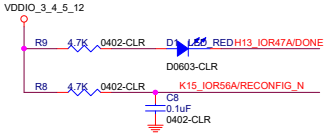


Mode[1:0]=2'b01

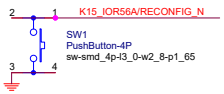


DONE/RECONFIG_N=Internal Pull Up



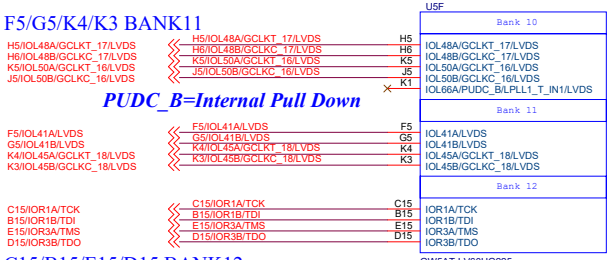


Button Manual Reset FPGA



H5/H6/K5/J5 BANK10

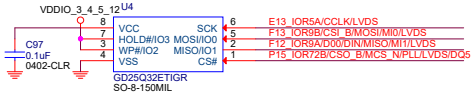
F5/G5/K4/K3 BANK11



PUDC_B=Internal Pull Down

C15/B15/E15/D15 BANK12

Dual SPI mode only.



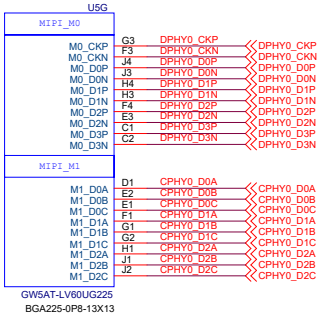
When 1.8V selected, SPI flash must be changed to 1.8V parts.

https://www.szovs.com

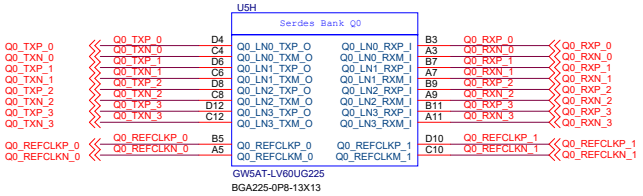
Title	DK_DP_GW5AT-LV60UG225	
Size	Document Number: FPGA IO_Module V1.0	Rev: 1.0
Date: Monday, February 17, 2025	Sheet 4 of 7	

MIPI & SERDES

DPHY & CPHY



SERDES

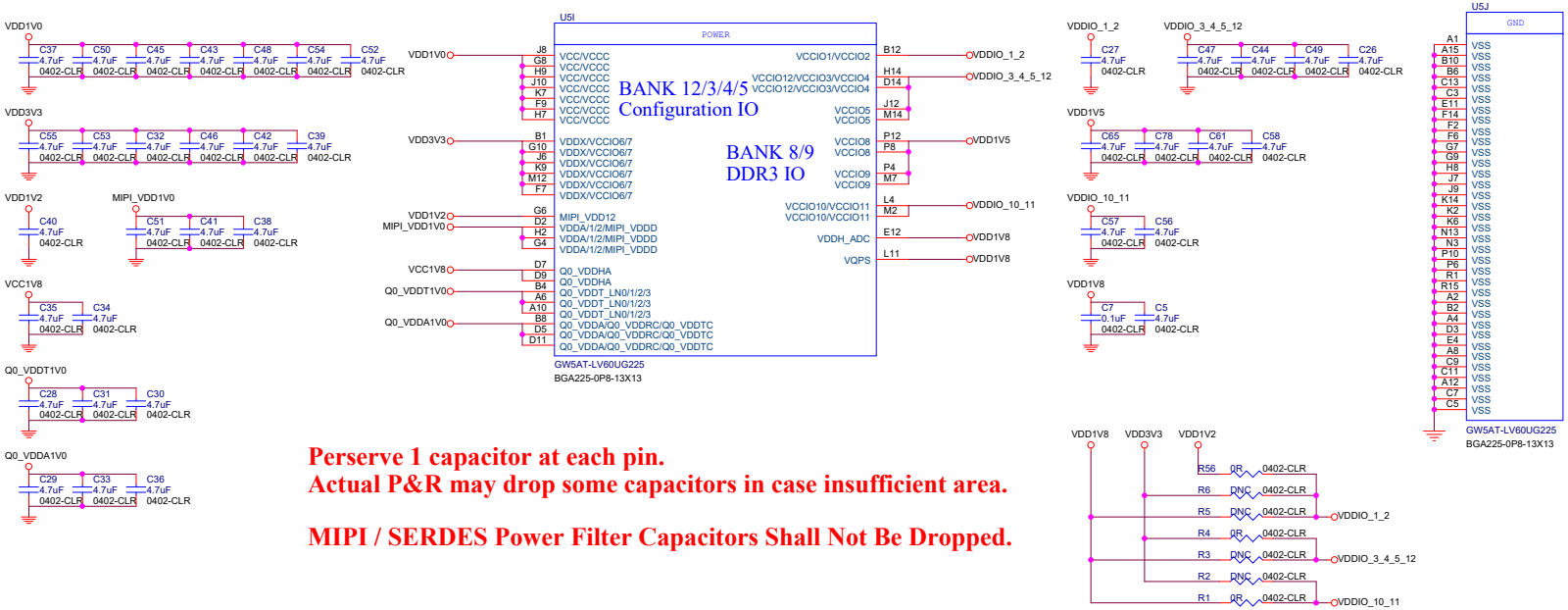


Capacitors must be placed at bottom board.

https://www.szovs.com

Title	DK_DP_GW5AT-LV60UG225	
Size	Document Number: FPGA MIPI & SERDES_Module V1.0	Rev: 1.0
Date: Friday, February 14, 2025	Sheet 5 of 7	

FPGA Power



Perserve 1 capacitor at each pin.
Actual P&R may drop some capacitors in case insufficient area.

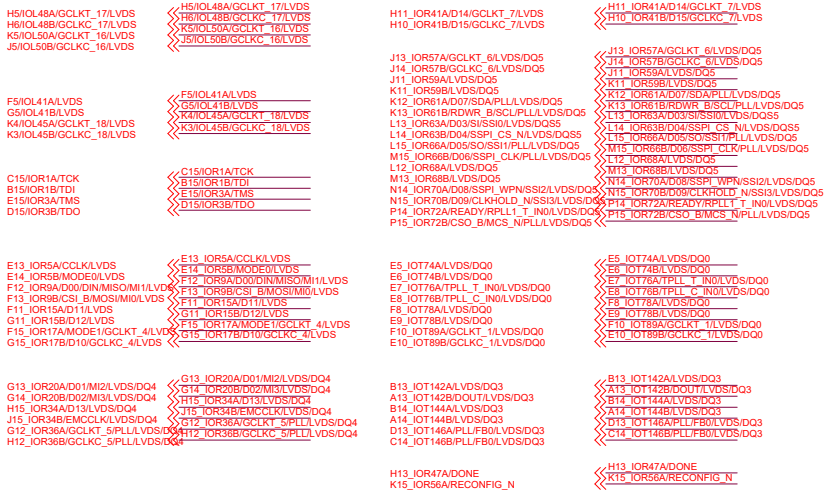
MIPI / SERDES Power Filter Capacitors Shall Not Be Dropped.

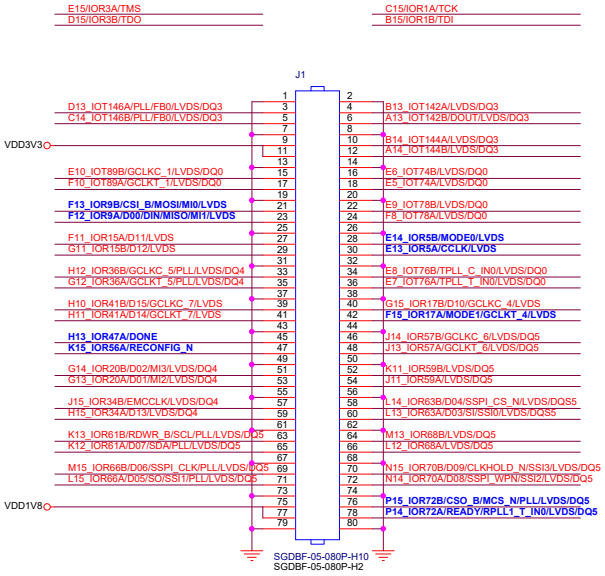
Bank 1 & 2: 1.2V By Default.
Bank 10 & 11: 1.8V By Default.
Bank 3 & 4 & 5 & 12: 3.3V By Default.

https://www.szovs.com

Title	DK_DP_GW5AT-LV60UG225	
Size	Document Number: FPGA Power_Module V1.0	Rev: 1.0
Date: Friday, February 14, 2025	Sheet 6 of 7	

Interface





Removed C15/B15/E15/D15 BANK12 (JTAG)

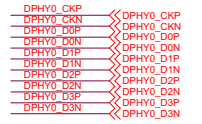
B13/A13/B14/A14/D13/C14 BANK2

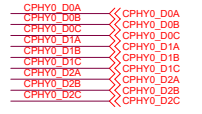
E5/E6/E7/E8/F8/E9/F10/E10 BANK1

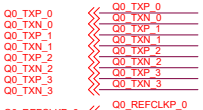
E13/E14/F12/F13/F11/G11/F15/G15 BANK3

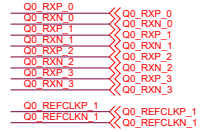
G13/G14/H15/J15/G12/H12 BANK4

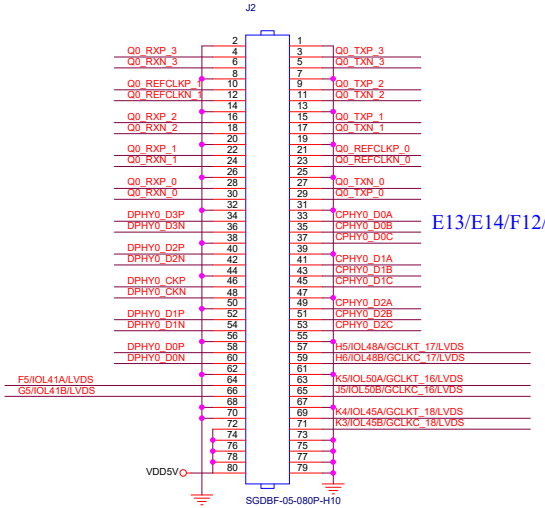
DONE/RECONFIG_N=Internal Pull Up







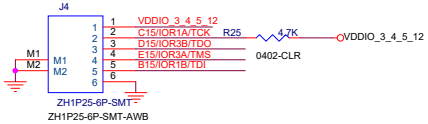




E13/E14/F12/F13/F11/G11/F15/G15 BANK3

F5/G5/K4/K3 BANK11

H5/H6/K5/J5 BANK10



1. Restricted usage on E14/F15. MODE0 must be pulled high, F15 must be pulled low. Incorrect states are not allowed.

2. Configuration Flash Pins E13, F12, F13, P15 are not recommended to be used.

3. P14 may be used without restriction.

https://www.szovs.com

Title	DK_DP_GW5AT-LV60UG225	
Size	Document Number: FPGA Interface_Module V1.0	Rev: 1.0
Date: Friday, February 14, 2025	Sheet 7 of 7	