



# GW5A Series of FPGA Products

## Data Sheet

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## Revision History

Date	Version	Description
3/29/2024	1.0E	Preliminary version.
6/14/2024	1.0E	Initial version published.
6/28/2024	1.0.1E	Power supply names unified.
10/25/2024	1.0.2E	BSRAM description optimized.
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11/29/2024	1.0.4E	Speed grade descriptions unified; <a href="#">Figure 4-2</a> modified.
01/14/2025	1.0.5E	<ul style="list-style-type: none"><li>• Transfer rates optimized for the soft MIPI D-PHY RX/TX implemented by the MIPI IO type.</li><li>• MIPI D-PHY Characteristics updated.</li><li>• Power Supply Ramp Rates updated.</li></ul>
02/28/2025	1.0.6E	<ul style="list-style-type: none"><li>• <math>R_{ODT}</math> added in <a href="#">3.3.1 DC Electrical Characteristics-Recommended Operating Conditions</a>.</li><li>• <math>V_{CCLDOADC}</math> added in <a href="#">3.1.1 Absolute Max. Ratings</a> and <a href="#">3.1.2 Recommended Operating Conditions</a>.</li></ul>
04/11/2025	1.0.7E	<ul style="list-style-type: none"><li>• The DDR3 interface speed description refined.</li><li>• The description of GPIO supporting MIPI C-PHY RX/TX (MIPI IO) removed.</li><li>• LVDS rate and Gearbox Timing Parameters updated.</li><li>• Soft-Core MIPI D-PHY RX Data Rate updated.</li></ul>

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# 1 Product Overview

GW5A Series of FPGA Products are the 5 series products of Arora family, with abundant internal resources, a new-architecture and high-performance DSP supporting AI operations, MIPI D-PHY and MIPI C-PHY hardcores, and abundant BSRAM resources. At the same time, it supports GPIO with multiple voltage standards, including high-speed LVDS interfaces, DDR3, and MIPI. It provides a variety of packages. It is suitable for applications such as low power, high performance and compatibility designs.

GOWINSEMI provides a new generation of FPGA hardware development environment that supports FPGA placement & routing, bitstream generation and download, etc.

## 1.1 Features

- Lower power consumption
  - 22nm SRAM process
  - Core Power(LV version): 0.9V/ 1.0V
  - Core voltage(EV version): 1.2V
  - Supports dynamic on/off of clock
- Abundant logic cells
  - Provides up to 23K~ 138K LUT4s
  - Supports shadow SRAMs
- Block SRAMs with multiple modes
  - Supports Dual Port, Single Port, Semi Dual Port, and ROM
  - Supports bytes write enable
  - Supports ECC detection and error correction
- High performance DSP blocks with a new architecture
  - High performance digital signal processing
  - Supports 27x18, 12x12, 27x36 multiplier and 48-bit accumulator
  - Supports cascading of multipliers
  - Supports pipeline mode and bypass mode
  - Pre-addition operation for filter function
  - Supports barrel shifter
- A new and flexible X-channel oversampling ADC with high accuracy, no external voltage source required
- Supports MIPI D-PHY RX/TX hardcore
  - Supports MIPI DSI and MIPI CSI-2 RX/TX
  - Up to 2.5 Gbps(RX/TX) per MIPI lane

- Supports up to eight data lanes and two clock lanes, with the max. transmission bandwidth up to 20 Gbps
- GPIO supports MIPI D-PHY RX/TX (MIPI IO)
  - GPIO can be configured as MIPI DSI and MIPI CSI-2 RX/TX interfaces
  - GW5A-138: Up to 1.5 Gbps per MIPI lane for MIPI D-PHY RX, and Up to 1.6 Gbps per MIPI lane for MIPI D-PHY TX
  - GW5A-25/GW5A-60: Up to 1.6 Gbps per MIPI lane for MIPI D-PHY RX, and Up to 2.0 Gbps per MIPI lane for MIPI D-PHY TX
- Supports MIPI C-PHY RX/TX hardcore
  - One MIPI Quad supports up to 3-trios data lanes and supports up to RX/TX data rate per lanes
- Supports various SDRAM interfaces, up to SSTL15 1333 Mbps
 

**Note!**

For the DDR/DDR2/DDR3 Memory Interface speed, please refer to [IPUG281](#), [Gowin DDR3 Memory Interface IP User Guide](#), [IPUG506](#), [Gowin DDR2 Memory Interface IP User Guide](#), [IPUG507](#), [Gowin DDR Memory Interface IP User Guide](#).
- Multiple I/O standards
  - Hysteresis option for input signals
- Supports drive strengths of 2mA, 4mA, 6mA, 8mA, 12mA, 16mA, 24mA, etc.
- Individual Bus Keeper, Pull-up, Pull-down, and Open Drain options
- Hot Socket
- 16 global clocks, 6/ 6/12 high-performance PLLs, 16/24 high speed clocks
- MIPI D-PHY, MIPI C-PHY, PLL, and ADC modules support Mini Dynamic Re-Program Port (mDRP)
- Configuration & Programming
  - JTAG configuration
  - Multiple GowinConfig configurations: SSPI, MSPI, Master CPU, Slave CPU, Master SERIAL, Slave SERIAL
  - Supports programming the SPI Flash directly in JTAG and SSPI modes; For other modes, you can program the SPI Flash using IP
  - Supports background upgrade
  - Supports bitstream file encryption and security bit settings
  - Supports Configuration Memory Soft Error Recovery (CMSER)
  - Supports OTP, a unique 64-bit DNA identifier for each device

## 1.2 Product Resources

Table 1-1 Product Resources

Device	GW5A-25	GW5A-60	GW5A-138
LUT4	23040	59904	138240
Flip-Flop (REG)	23040	59904	138240
Shadow Static Random Access Memory(SSRAM) (Kb)	180	468	1080
Block Static Random Access Memory (BSRAM) (Kb)	1008	2124	6120

Device	GW5A-25	GW5A-60	GW5A-138
Number of BSRAMs	56	118	340
DSP (27-bit x 18-bit)	28	118	298
Maximum phase locked loop <sup>[1]</sup> (PLLs)	6	8	12
Global Clocks	16	16	16
High-speed Clocks	16	20	24
LVDS (Gbps)	1.6(RX) 2.0(TX)	1.6(RX) 2.0(TX)	1.5(RX) 1.6(TX)
DDR3 (Mbps)	1100	1100	800
MIPI D-PHY hard core <sup>[5]</sup> (Gbps)	2.5 (RX/TX), 4 data lanes 1 clock lane	2.5 (RX/TX), 4 data lanes 1 clock lanes	2.5 (RX) 8 data lanes 2 clock lane
MIPI C-PHY Hardcore (Gsps)	-	2.5 <sup>[6]</sup> (RX/TX), 3-trios data lanes	-
ADC	1	2	2
Number of GPIO banks	8 <sup>[2]</sup>	11	6
Maximum number of GPIOs <sup>[3]</sup>	239	320	312
Core voltage	0.9V/1.0V/1.2V <sup>[4]</sup>	0.9V/1.0V/1.2V <sup>[4]</sup>	0.9V/1.0V

**Note!**

- <sup>[1]</sup> Different packages support different numbers of PLLs, and here is the max. number.
- <sup>[2]</sup> In addition to GPIO Banks, there is one JTAG Bank with four I/Os and one Config Bank with one I/O.
- <sup>[3]</sup> This is the max. number of GPIOs that the device can provide without package limitation. Please refer to [Table 1-2](#), [Table 1-3](#) and [Table 1-4](#) for the maximum number of user I/O available in specific packages.
- <sup>[4]</sup> The EV version has a built-in LDO and supports 1.2V V<sub>CC</sub>.
- <sup>[5]</sup> MIPI D-PHY support and the number of channels vary depending on the package, with the maximum values listed here.
- <sup>[6]</sup> The data rate of C-PHY RX depends on the supply voltage, device speed grade, and package. For more details, please refer to [3.6 MIPI C-PHY Switching Characteristics](#).

**Table 1-2 GW5A-25 Package Information**

Package	Pitch (mm)	Size (mm)	GW5A-25	
			User I/O(True LVDS Pair)	MIPI D-PHY hardcore
LQ100	0.5	14x14	80 (36)	–
LQ144	0.5	20x20	109 (50)	–
MG121N	0.5	6x6	82 (36)	RX/TX, Configurable 4 data lanes

Package	Pitch (mm)	Size (mm)	GW5A-25	
			User I/O(True LVDS Pair)	MIPI D-PHY hardcore
MG121N	0.5	6x6	82 (36)	1 clock lane
MG196S	0.5	8x8	114 (53)	–
PG196S	1.0	15x15	110 (48)	RX/TX, Configurable 4 data lanes 1 clock lane
PG256C	1.0	17x17	191 (90)	–
PG256	1.0	17x17	184 (88)	RX/TX, Configurable 4 data lanes 1 clock lane
PG256S	1.0	17x17	194 (93)	–
UG225S	0.8	13x13	168 (80)	–
UG256C	0.8	14x14	191 (90)	–
UG324	0.8	15x15	222 (104)	RX/TX, Configurable 4 data lanes 1 clock lane
UG324S	0.8	15x15	239 (116)	–

**Note!**

[1] The package types in this GW5A Series of FPGA Products data sheet are written with abbreviations. See [4.1 Part Name](#) for further information.

**Table 1-3 GW5A-60 Package Information**

Package			Pitch (mm)	Size (mm)	GW5A-60		
Name	Type	Description			User I/O (True LVDS Pair)	MIPI D-PHY Hard Core Processor	MIPI C-PHY Hard Core Processor
UG324A	UBGA	Wire Bond	0.8	15x15	222(106)	–	–
UG324S	UBGA	Wire Bond	0.8	15x15	226(110)	–	–
PG324C	PBGA	Wire Bond	1.0	19x19	205(97)	–	–

**Note!**

[1] The package types in this GW5A Series of FPGA Products data sheet are written with abbreviations. See [4.1 Part Name](#) for further information.

**Table 1-4 GW5A-138 Package Information**

Package	Pitch (mm)	Size (mm)	GW5A-138	
			I/O(True LVDS Pair)	MIPI D-PHY hardcore
UG324A	0.8	15x15	221 (106)	–

**Note!**

[1] The package types in this GW5A Series of FPGA Products data sheet are written with abbreviations. See [4.1 Part Name](#) for further information.

# 2 Architecture

## 2.1 Architecture

Figure 2-1 Architecture Diagram (GW5A-25)

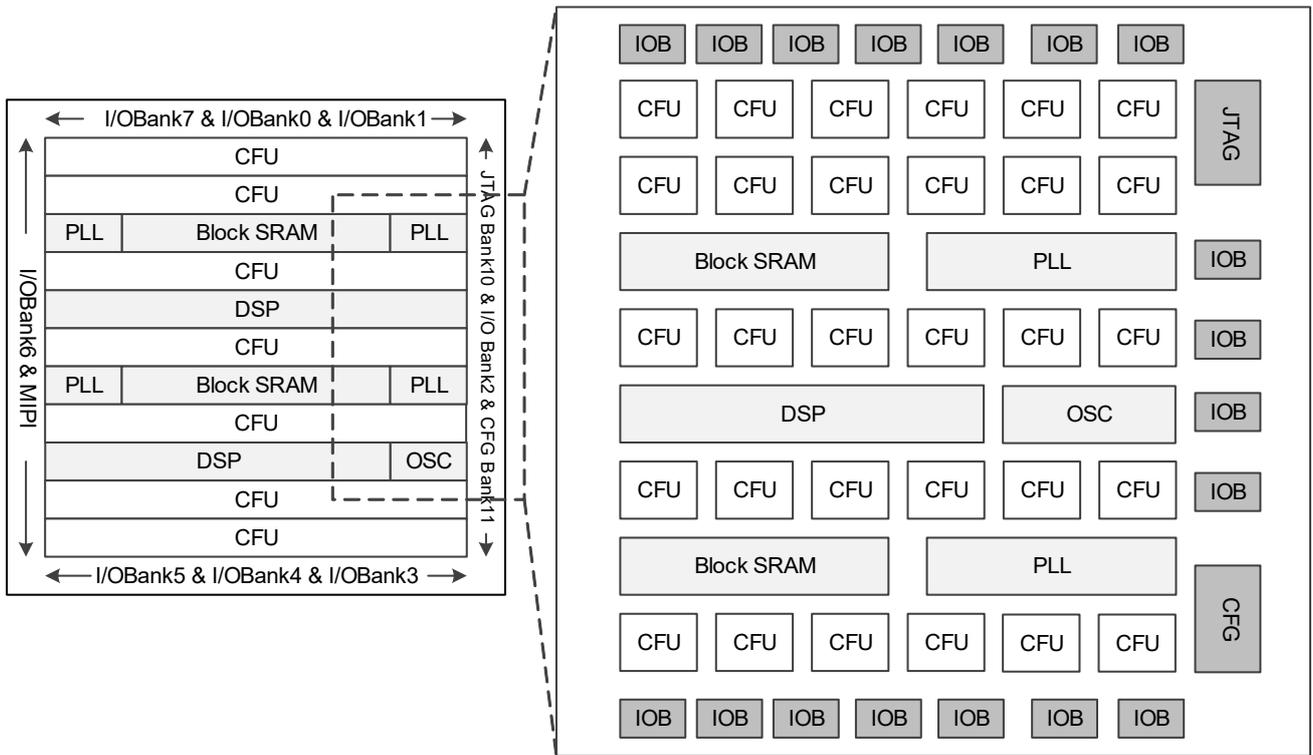


Figure 2-2 Architecture Diagram (GW5A-60)

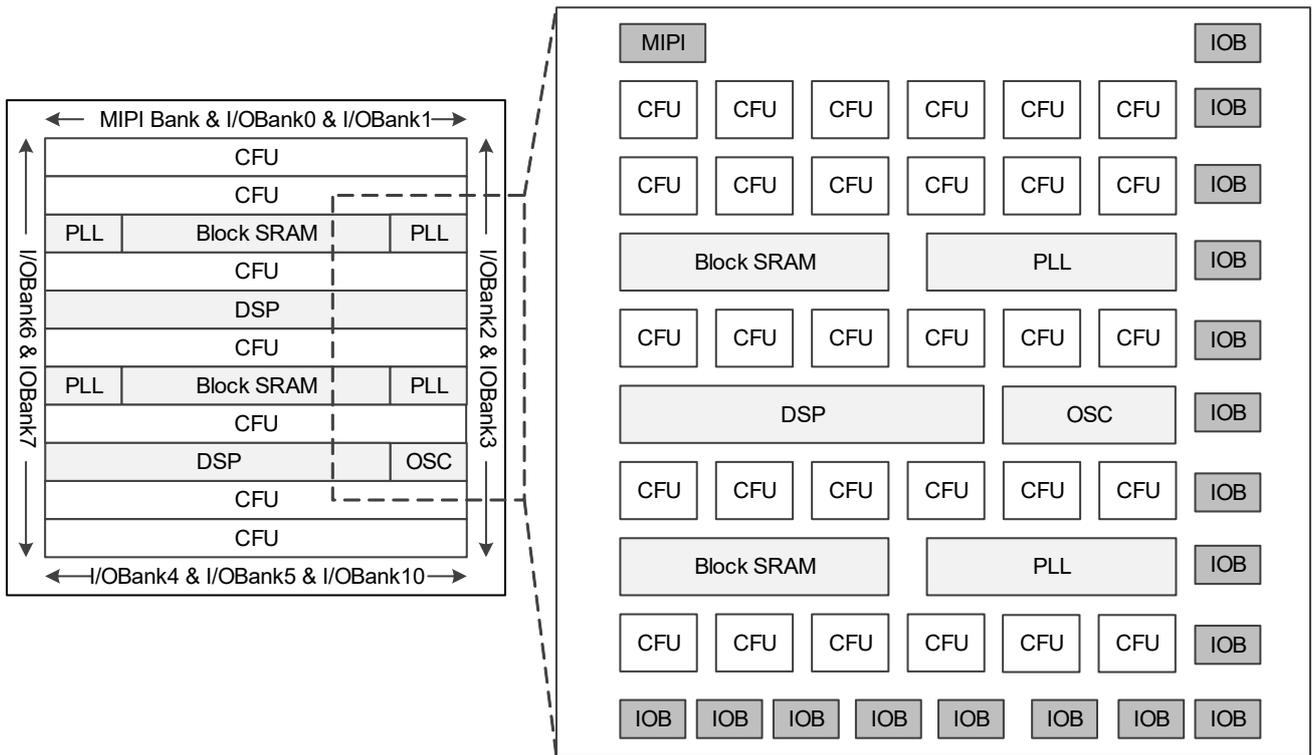
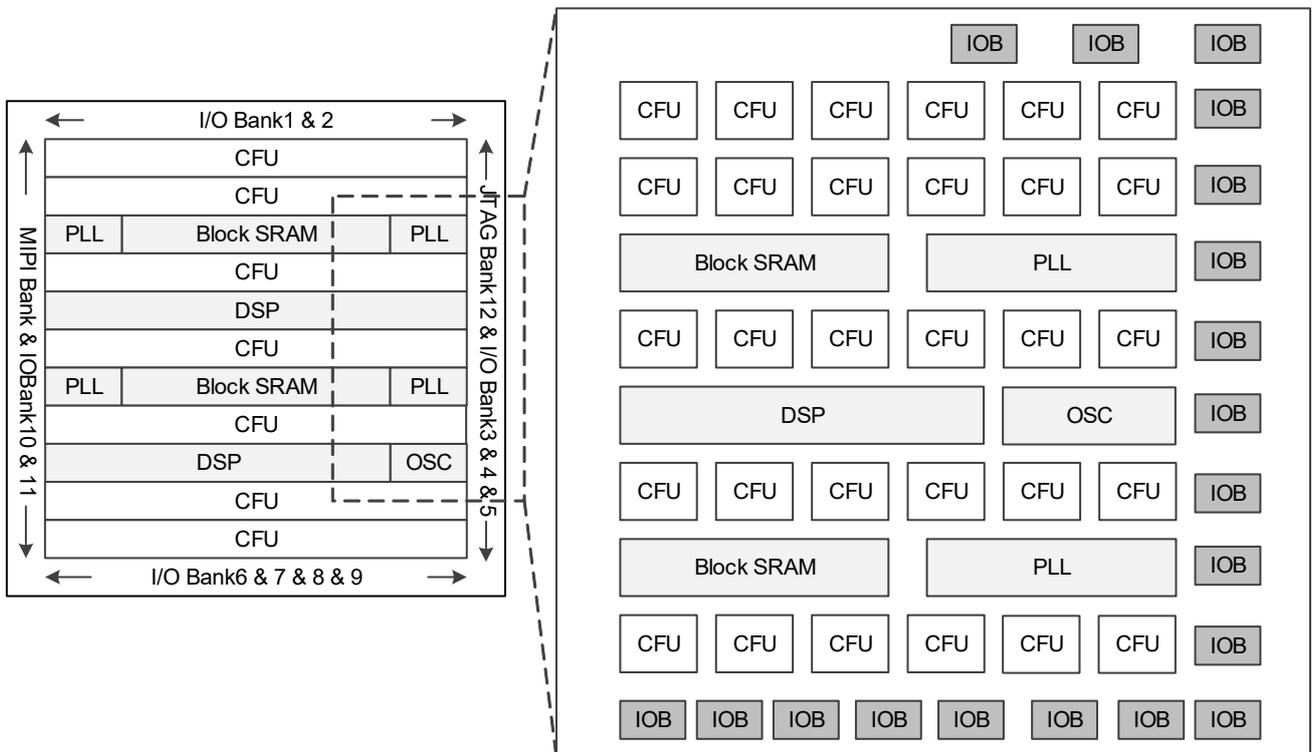


Figure 2-3 Architecture Diagram (GW5A-138)



The core of the GW5A Series of FPGA Products is an array of Configurable Function Units (CFU) surrounded by IO blocks. Besides, BSRAMs, DSP blocks, MIPI D-PHY, ADC, PLLs, and on chip oscillators are supported. For more detailed information, see [Table 1-1](#).

Configurable Function Unit (CFU) is the base cell for the array of the Products. Devices with different capacities have different numbers of rows and columns. CFU can be configured as LUT4 mode, ALU mode, and memory mode. For more detailed information, see [2.2 Configurable Function Units](#).

The I/O resources in are arranged around the periphery of the devices in groups referred to as banks. I/O resources support multiple I/O standards, and support regular mode, SRD mode, generic DDR mode, and DDR\_MEM mode. For more detailed information, see [2.3 Input/Output Block](#).

The BSRAM is embedded as a row in the products and supports multiple configuration modes and operation modes. For more detailed information, see [2.4 Block SRAM](#).

GW5A Series of FPGA Products are embedded with a brand-new DSP, which can meet the your high-performance digital signal processing requirements DSP. For further details, refer to [2.5 DSP](#).

GW5A Series of FPGA Products provide a MIPI D-PHY hardcore supporting the “MIPI Alliance Standard for D-PHY Specification(V1.2)”. For details, see [2.6 MIPI D-PHY](#).

GW5A-60 devices contain a hard core MIPI C-PHY, see [2.7 MIPI C-PHY](#) for details .

GW5A Series of FPGA Products integrates different types of ADCs. Please refer to [2.8 ADC](#) for details.

GW5A Series of FPGA Products have embedded PLL resources. PLL blocks provide the ability to synthesize clock frequencies. Frequency adjustment (multiply and division), phase adjustment, and duty cycle can be adjusted using the configuration of parameters . The FPGAs also have an embedded programmable on-chip clock oscillator that supports clock frequencies ranging from 1.67 MHz to 105MHz, providing clocking resources for the MSPI mode. The on-chip clock oscillator also provides programmable user clocks. For more information, see [2.9 Clock and 2.12 On Chip Oscillator](#).

FPGA provides abundant CRUs, connecting all the resources in FPGA. For example, routing resources distributed in CFU and IOB connect the internal resources of the CFU to the logical resources inside the IOB. Routing resources can automatically be generated by Gowin software. In addition, GW5A Series of FPGA Products also provide abundant GCLKs, long wires (LW), global set/reset (GSR), and programming options, etc. For more details, see [2.10 Global Reset](#) and [2.11 Programming Configuration](#).

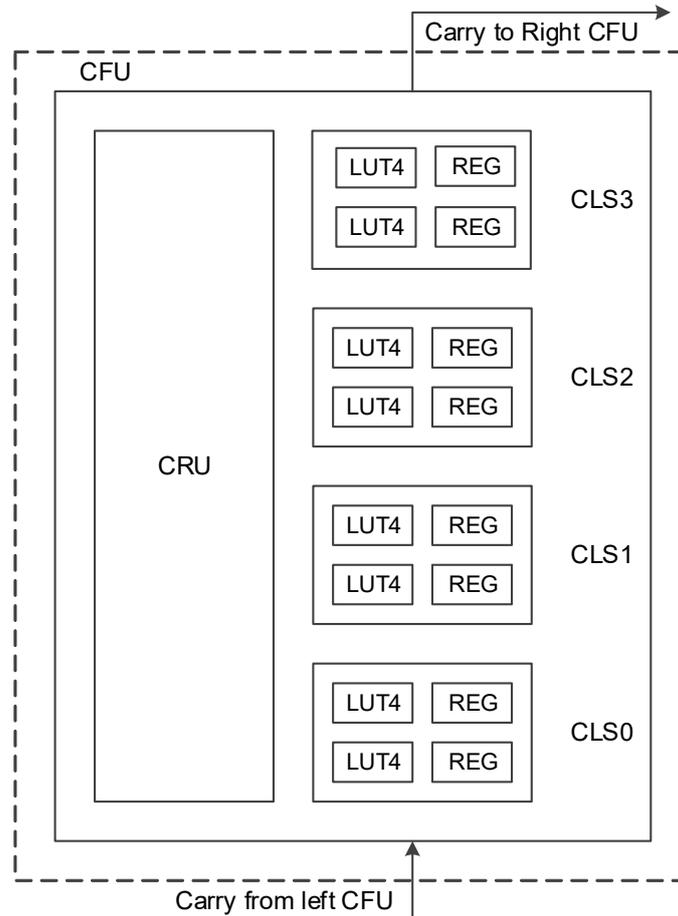
## 2.2 Configurable Function Units

Configurable Function Units (CFUs) are the basic cells for the array of GOWINSEMI FPGA Products. Each basic cell consists of four Configurable Logic Sections (CLSs) and their routing resource Configurable Routing Units (CRUs). Each CLS includes two 4 input look-up-tables (LUTs) and two registers (REGs), as shown in [Figure 2-4](#).

CLSs in the CFUs can be configured as basic look-up tables, arithmetic logic units, static random access memories, and read only memories according to application scenarios.

For more details, please see [UG303, Arora V Configurable Function Unit \(CFU\) User Guide](#).

Figure 2-4 CFU Structure View



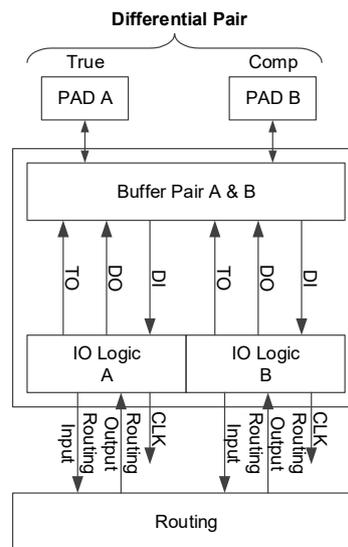
## 2.3 Input/Output Blocks

The GPIOs meet a variety of I/O standards and supports both single-ended and differential level standards, providing an easy connection with external buses, storage devices, video applications, and other standards.

The basic units are IOB, including I/O buffer, I/O logic, and the relevant programmable routing unit. The programmable routing unit is similar to the CRU in CFU.

As shown in [Figure 2-5](#), each IOB connects to two Pins (Marked as A and B They can be used as a differential pair or as a single end input/output. The I/O logic supports deserializer, serializer, delay control, and byte alignment, and is suitable for high-speed data transmission. The programmable routing unit is used to inter-connect I/O blocks with other on-chip resources.

Figure 2-5 IOB Structure View



#### IOB Features:

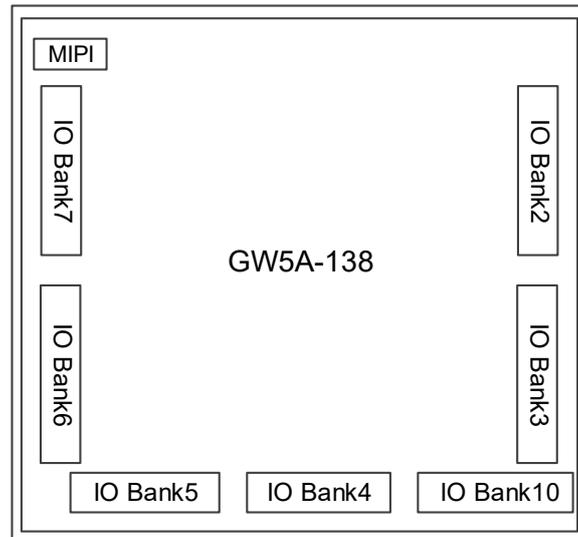
- $V_{CCIO}$  supplied with each bank
- Support multiple levels: LVCMOS, PCI, LVTTTL, SSTL, HSTL, LVDS, Mini\_LVDS, RSDS, PPDS, BLVDS, etc
- Support MIPI and MIPI I3C OpenDrain/PushPull conversion
- Hysteresis option for input signals
- Output drive strength option
- GW5A-60 supports slew rate option for output signals
- Individual bus keeper, pull-up/down resistor, and open drain output options
- Hot Socket
- I/O logic supports SDR, DDR, etc.

### 2.3.1 I/O Buffer

#### GW5A-138

GW5A-138 has six GPIO Banks (Bank2~7), two SerDes Banks and a Bank for configuration (Bank 10), as shown in [Figure 2-6](#). Bank 10 can also be used as an I/O Bank.

Figure 2-6 I/O Bank Distribution View (GW5A-138)



Each Bank has independent I/O power supply  $V_{CCIO}$ .  $V_{CCIO}$  can be set as 3.3V, 2.5V, 1.8V, 1.5V, 1.35V, 1.2V, or 1V. The auxiliary voltage  $V_{CCX}$  supports 1.8V.

To support SSTL, HSTL, etc., each bank also provides one independent voltage source (VREF) as the reference voltage. You can choose from the internal reference voltage of the bank (0.6V, 0.675V, 0.75V, 0.9V and (33%,42%,50%,58%) $V_{CCIO}$ ) or the external reference voltage using any IO from the bank.

Different banks in the support different on-chip resistor settings, including single-ended resistors and differential resistors. Single-ended resistor settings are used for SSTL/HSTL inputs and outputs. Differential resistor settings are used for LVDS/PPDS/ RSDS inputs. For more details, refer to [UG304, Arora V Programmable IO \(GPIO\) User Guide](#).

GW5A-138 I/O standards and configuration options supported are as listed in [Table 2-1](#) and [Table 2-2](#).

Table 2-1 Output I/O Standards and Configuration Options

I/O Output Standard	Single-ended/ Differential	Bank $V_{CCIO}$ (V)	Output Drive Strength (mA)	Typical Applications
LVDS25	Differen- tial(TLVDS)	2.5/3.3	3.5/2.5/4.5/6	High-speed point-to-point data transmission
BLVDS25		2.5/3.3	3.5/2.5/4.5/6	Multi-point high-speed data transmission
RSDS		2.5/3.3	3.5/2.5/4.5/6	High-speed point-to-point data transmission

I/O Output Standard	Single-ended/ Differential	Bank $V_{CCIO}(V)$	Output Drive Strength (mA)	Typical Applications
MINILVDS	Differential(TLVDS)	2.5/3.3	3.5/2.5/4.5/6	LCD timing driver interface and column driver interface
PPLVDS		2.5/3.3	3.5/2.5/4.5/6	LCD row/column driver
LVDS25E	Differential	2.5	8/4/12/16/24	High-speed point-to-point data transmission
BLVDS25E		2.5	8/4/12/16/24	Multi-point high-speed data transmission
MLVDS25E		2.5	8/4/12/16/24	LCD timing driver interface and column driver interface
RSDS25E		2.5	8/4/12/16/24	High-speed point-to-point data transmission
LVPECL33E		3.3	8/4/12/16/24	Universal interface
HSUL12D		1.2	8/4/12	LPDDR2
HSUL12D_I		1.2	8/4/12	LPDDR2
HSTL15D_I		1.5	8/4/12/16	Memory interface
HSTL15D_II		1.5	8/4/12/16	Memory interface
HSTL18D_I		1.8	8/4/12/16	Memory interface
HSTL18D_II		1.8	8/4/12/16	Memory interface
SSTL135D		1.35	8/4/12	Memory interface
SSTL15D		1.5	8/4/12/16	Memory interface
SSTL18D_I		1.8	8/4/12/16/24	Memory interface
SSTL18D_II		1.8	8/4/12/16/24	Memory interface
LPDDR		1.8	8/4/12/16/24	LPDDR and Mobile DDR
LVC MOS10D		1.0	4	Universal interface
LVC MOS12D		1.2	4/8	Universal interface
LVC MOS15D		1.5	4/8/12	Universal interface
LVC MOS18D		1.8	4/8/12/16/24	Universal interface
LVC MOS25D	2.5	4/8/12/16/24	Universal interface	
LVC MOS33D	3.3	8/4/12/16/24	Universal interface	
HSUL12	Single-ended	1.2	8/4/12	Memory interface
HSTL12_I		1.2	8/4/12	Memory interface
HSTL15_I		1.5	8/4/12/16	Memory interface

I/O Output Standard	Single-ended/ Differential	Bank $V_{CCIO}(V)$	Output Drive Strength (mA)	Typical Applications
HSTL15_II	Single-ended	1.5	8/4/12/16	Memory interface
HSTL18_I		1.8	8/4/12/16/24	Memory interface
HSTL18_II		1.8	8/4/12/16/24	Memory interface
SSTL135		1.35	8/4/12	Memory interface
SSTL15		1.5	8/4/12/16	Memory interface
SSTL18_I		1.8	8/4/12/16/24	Memory interface
SSTL18_II		1.8	8/4/12/16/24	Memory interface
LVC MOS10		1.0	4	Universal interface
LVC MOS12		1.2	4/8/12	Universal interface
LVC MOS15		1.5	4/8/12/16	Universal interface
LVC MOS18		1.8	4/8/12/16/24	Universal interface
LVC MOS25		2.5	4/8/12/16/24	Universal interface
LVC MOS33/ LV TTL33		3.3	8/4/12/16/24	Universal interface
LPDDR		1.8	8/4/12/16/24	LPDDR and Mobile DDR
PCI33		3.3	8/4/12/16/24	PC and embedded system

Table 2-2 Input I/O Standards and Configuration Options

I/O Input Standard	Single-ended/ Differential	Bank $V_{CCIO}(V)$	Hysteresis	Need $V_{REF}$
MIPI	Differential	1.2	No	No
ADC_IN		2.5/1.0/1.2/1.5/1.8/3.3	No	No
LVDS25		2.5/1.0/1.2/1.5/1.8/3.3	No	No
BLVDS25		2.5/1.0/1.2/1.5/1.8/3.3	No	No
RSDS		2.5/1.0/1.2/1.5/1.8/3.3	No	No
MINILVDS		2.5/1.0/1.2/1.5/1.8/3.3	No	No
PPLVDS		2.5/1.0/1.2/1.5/1.8/3.3	No	No
HSUL12D		1.2/1.0/1.5/1.8/2.5/3.3	No	No
HSTL12D_I		1.2/1.0/1.5/1.8/2.5/3.3	No	No
HSTL15D_I		1.5/1.0/1.2/1.8/2.5/3.3	No	No
HSTL15D_II		1.5/1.0/1.2/1.8/2.5/3.3	No	No
HSTL18D_I		1.8/1.0/1.2/1.5/2.5/3.3	No	No

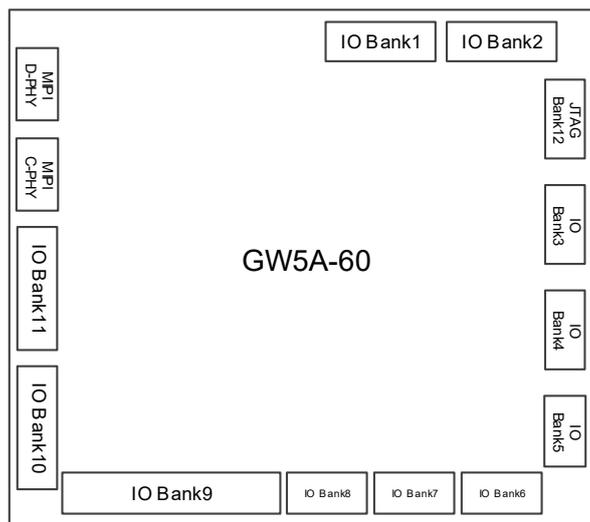
I/O Input Standard	Single-ended/ Differential	Bank $V_{CCIO}$ (V)	Hysteresis	Need $V_{REF}$
HSTL18D_II	Differential	1.8/1.0/1.2/1.5/2.5/3.3	No	No
SSTL135D		1.35/1.0/1.2/1.5/1.8/2.5/3.3	No	No
SSTL15D		1.5/1.0/1.2/1.8/2.5/3.3	No	No
SSTL18D_I		1.8/1.0/1.2/1.5/2.5/3.3	No	No
SSTL18D_II		1.8/1.0/1.2/1.5/2.5/3.3	No	No
LPDDR		1.8/1.0/1.2/1.5/2.5/3.3	No	No
LVC MOS10D		1.0/1.2/1.5/1.8/2.5/3.3	No	No
LVC MOS12D		1.2/1.0/1.5/1.8/2.5/3.3	No	No
LVC MOS15D		1.5/1.0/1.2/1.8/2.5/3.3	No	No
LVC MOS18D		1.8/1.0/1.2/1.5/2.5/3.3	No	No
HSUL12		Single-ended	1.2	No
HSTL12_I	1.2		No	Yes
HSTL15_I	1.5		No	Yes
HSTL15_II	1.5		No	Yes
HSTL18_I	1.8		No	Yes
HSTL18_II	1.8		No	Yes
SSTL135	1.35		No	Yes
SSTL15	1.5		No	Yes
SSTL18_I	1.8		No	Yes
SSTL18_II	1.8		No	Yes
LVC MOS10	1.0		No	No
LVC MOS10UD12	1.2		No	No
LVC MOS10UD15	1.5		No	No
LVC MOS10UD18	1.8		No	No
LVC MOS10UD25	2.5		No	No
LVC MOS10UD33	3.3		No	No
LVC MOS12	1.2		Yes	No
LVC MOS15	1.5		Yes	No
LVC MOS15OD10	1.0		Yes	No
LVC MOS15OD12	1.2		Yes	No
LVC MOS15UD18	1.8		Yes	No
LVC MOS15UD25	2.5		Yes	No

I/O Input Standard	Single-ended/ Differential	Bank $V_{CCIO}$ (V)	Hysteresis	Need $V_{REF}$
LVC MOS15UD33	Single-ended	3.3	Yes	No
LVC MOS18		1.8	Yes	No
LVC MOS18OD10		1.0	Yes	No
LVC MOS18OD12		1.2	Yes	No
LVC MOS18OD15		1.5	Yes	No
LVC MOS18UD25		2.5	Yes	No
LVC MOS18UD33		3.3	Yes	No
LVC MOS25		2.5	Yes	No
LVC MOS25UD33		3.3	Yes	No
LVC MOS33/ LV TTL33		3.3	Yes	No
LVC MOS33OD25		2.5	Yes	No
LPDDR		1.8	Yes	No
PCI33		3.3	Yes	No
VREF1_DRIVER		1.8/1.2/1.35/1.5	No	Yes

GW5A-60

GW5A-60 has eleven GPIO Banks. Bank12 is a JTAG Bank with four IOs, as shown in Figure 2-7.

Figure 2-7 I/O Bank Distribution View (GW5A-60)



Each Bank has independent I/O power supply  $V_{CCIO}$ .  $V_{CCIO}$  can be set as 3.3V, 2.5V, 1.8V, 1.5V, 1.35V, or 1.2V. The auxiliary voltage  $V_{CCX}$  supports 1.8V, 2.5V, and 3.3V.

To support SSTL, HSTL, etc., each bank also provides one independent voltage source (VREF) as the reference voltage. You can choose from the internal reference voltage of the bank (0.6V, 0.75V, 0.9V, 1.25V, 1.5V and (36%,50%,64%) $V_{CCIO}$ ) or the external reference voltage using any IO from the bank.

Different banks in the support different on-chip resistor settings, including single-ended resistors and differential resistors. Single-ended resistor settings are used for SSTL/HSTL inputs and outputs. Differential resistor settings are used for LVDS/PPDS/ RSDS inputs. For more details, refer to [UG304, Arora V Programmable IO \(GPIO\) User Guide](#) .

GW5A-60 I/O standards and configuration options supported are as listed in [Table 2-3](#) and [Table 2-4](#).

**Table 2-3 Output I/O Standards and Configuration Options**

I/O Output Standard	Single-ended/ Differential	Bank $V_{CCIO}$ (V)	Output Drive Strength (mA)	Typical Applications
MIPI_CPHY	Differential (TLVDS)	2.5/3.3	2	Mobile Industry Processor Interface
MIPI		1.8/2.5/3.3	2	Mobile Industry Processor Interface
MIPI_3MA	Differential (ELVDS)	1.8	3	Mobile Industry Processor Interface
MIPI_4MA		1.8	4	Mobile Industry Processor Interface
LVDS25	Differential (TLVDS)	2.5/3.3	3.5/2.5/4.5/6	High-speed point-to-point data transmission
BLVDS25		2.5/3.3	3.5/2.5/4.5/6	Multi-point high-speed data transmission
RSDS		2.5/3.3	3.5/2.5/4.5/6	High-speed point-to-point data transmission
MINILVDS		2.5/3.3	3.5/2.5/4.5/6	LCD timing driver interface and column driver interface
PPLVDS		2.5/3.3	3.5/2.5/4.5/6	LCD row/column driver
LVDS25E	Differential	2.5	8/2/4/6/12/16	High-speed point-to-point data transmission
BLVDS25E		2.5	8/2/4/6/12/16	Multi-point high-speed data transmission
MLVDS25E		2.5	8/2/4/6/12/16	LCD timing driver interface and column driver interface
RSDS25E		2.5	8/2/4/6/12/16	High-speed point-to-point data transmission

I/O Output Standard	Single-ended/ Differential	Bank $V_{CCIO}(V)$	Output Drive Strength (mA)	Typical Applications
LVPECL33E	Differential	3.3	8/2/4/6/12/16	Universal interface
HSUL12D		1.2	8/2/4/6	LPDDR2
HSUL12D_I		1.2	8/2/4/6	LPDDR2
HSTL15D_I		1.5	8/4/12	Memory interface
HSTL18D_I		1.8	8/2/4/6/12/16	Memory interface
HSTL18D_II		1.8	8/2/4/6/12/16	Memory interface
SSTL12D_I		1.2	8/2/4/6	Memory interface
SSTL135D_I		1.35	8/2/4/6	Memory interface
SSTL15D_I		1.5	8/2/4/6/12	Memory interface
SSTL18D_I		1.8	8/2/4/6/12/16	Memory interface
SSTL18D_II		1.8	8/2/4/6/12/16	Memory interface
SSTL25D_I		2.5	8/2/4/6/12/16	Memory interface
SSTL25D_II		2.5	8/2/4/6/12/16	Memory interface
SSTL33D_I		3.3	8/2/4/6/12/16	Memory interface
SSTL33D_II		3.3	8/2/4/6/12/16	Memory interface
LPDDR		1.8	8/2/4/6/12/16	LPDDR and Mobile DDR
LVC MOS10D		1.0	2/4	Universal interface
LVC MOS12D		1.2	8/2/4/6	Universal interface
LVC MOS15D		1.5	8/2/4/6/12	Universal interface
LVC MOS18D		1.8	8/2/4/6/12/16	Universal interface
LVC MOS25D		2.5	8/2/4/6/12/16	Universal interface
LVC MOS33D		3.3	8/2/4/6/12/16	Universal interface
HSUL12		Single-ended	1.2	8/2/4/6
HSTL12_I	1.2		8/2/4/6	Memory interface
HSTL15_I	1.5		8/2/4/6/12	Memory interface
HSTL18_I	1.8		8/2/4/6/12/16	Memory interface
HSTL18_II	1.8		8/2/4/6/12/16	Memory interface
SSTL12_I	1.2		8/2/4/6	Memory interface
SSTL135_I	1.35		8/2/4/6	Memory interface
SSTL15_I	1.5		8/2/4/6/12	Memory interface
SSTL18_I	1.8		8/2/4/6/12/16	Memory interface
SSTL18_II	1.8		8/2/4/6/12/16	Memory interface

I/O Output Standard	Single-ended/ Differential	Bank $V_{CCIO}(V)$	Output Drive Strength (mA)	Typical Applications
SSTL25_I	Single-ended	2.5	8/2/4/6/12/16	Memory interface
SSTL25_II		2.5	8/2/4/6/12/16	Memory interface
SSTL33_I		3.3	8/2/4/6/12/16	Memory interface
SSTL33_II		3.3	8/2/4/6/12/16	Memory interface
LVC MOS10		1.0	2/4	Universal interface
LVC MOS12		1.2	8/2/4/6	Universal interface
LVC MOS15		1.5	8/2/4/6/12	Universal interface
LVC MOS18		1.8	8/2/4/6/12/16	Universal interface
LVC MOS25		2.5	8/2/4/6/12/16	Universal interface
LVC MOS33/ LV TTL33		3.3	8/2/4/6/12/16	Universal interface
LPDDR		1.8	8/2/4/6/12/16	LPDDR and Mobile DDR
PCI33		3.3	8/2/4/6/12/16	PC and embedded system

Table 2-4 Input I/O Standards and Configuration Options

I/O Input Standard	Single-ended/ Differential	Bank $V_{CCIO}(V)$	Hysteresis	Need $V_{REF}$
MIPI_CPHY	Differential	1.2/1.5/1.8	No	No
MIPI		1.2/1.5/1.8	No	No
ADC_IN		2.5/1.0/1.2/1.5/1.8/3.3	No	No
LVDS25		2.5/1.0/1.2/1.5/1.8/3.3	No	No
BLVDS25		2.5/1.0/1.2/1.5/1.8/3.3	No	No
RS DS		2.5/1.0/1.2/1.5/1.8/3.3	No	No
MINILVDS		2.5/1.0/1.2/1.5/1.8/3.3	No	No
PPLVDS		2.5/1.0/1.2/1.5/1.8/3.3	No	No
HSUL12D		1.2/1.0/1.5/1.8/2.5/3.3	No	No
HSTL12D_I		1.2/1.0/1.5/1.8/2.5/3.3	No	No
HSTL15D_I		1.5/1.0/1.2/1.8/2.5/3.3	No	No
HSTL18D_I		1.8/1.0/1.2/1.5/2.5/3.3	No	No
HSTL18D_II		1.8/1.0/1.2/1.5/2.5/3.3	No	No
SSTL135D_I		1.35/1.0/1.2/1.5/1.8/2.5/3.3	No	No
SSTL15D_I		1.5/1.0/1.2/1.8/2.5/3.3	No	No

I/O Input Standard	Single-ended/ Differential	Bank V <sub>CCIO</sub> (V)	Hysteresis	Need V <sub>REF</sub>
SSTL18D_I	Differential	1.8/1.0/1.2/1.5/2.5/3.3	No	No
SSTL18D_II		1.8/1.0/1.2/1.5/2.5/3.3	No	No
SSTL25D_I		2.5/1.0/1.2/1.5/1.8/3.3	No	No
SSTL25D_II		2.5/1.0/1.2/1.5/1.8/3.3	No	No
SSTL33D_I		3.3/1.0/1.2/1.5/1.8/2.5	No	No
SSTL33D_II		3.3/1.0/1.2/1.5/1.8/2.5	No	No
LPDDR		1.8/1.0/1.2/1.5/2.5/3.3	No	No
LVC MOS10D		1.0/1.2/1.5/1.8/2.5/3.3	No	No
LVC MOS12D		1.2/1.0/1.5/1.8/2.5/3.3	No	No
LVC MOS15D		1.5/1.0/1.2/1.8/2.5/3.3	No	No
LVC MOS18D		1.8/1.0/1.2/1.5/2.5/3.3	No	No
LVC MOS25D		2.5/1.0/1.2/1.5/1.8/3.3	No	No
LVC MOS33D		3.3/1.0/1.2/1.5/2.5/1.8	No	No
HSUL12		Single-ended	1.2	Yes
HSTL12_I	1.2		Yes	No
HSTL15_I	1.5		Yes	No
HSTL15_II	1.5		Yes	No
HSTL18_I	1.8		Yes	No
HSTL18_II	1.8		Yes	No
SSTL135_I	1.35		Yes	No
SSTL15_I	1.5		Yes	No
SSTL18_I	1.8		Yes	No
SSTL18_II	1.8		Yes	No
SSTL25_I	2.5		Yes	No
SSTL25_II	2.5		Yes	No
SSTL33_I	3.3		Yes	No
SSTL33_II	3.3		Yes	No
LVC MOS10	1.0		Yes	No
LVC MOS12	1.2		Yes	No
LVC MOS15	1.5		Yes	No
LVC MOS18	1.8		Yes	No
LVC MOS25	2.5		Yes	No

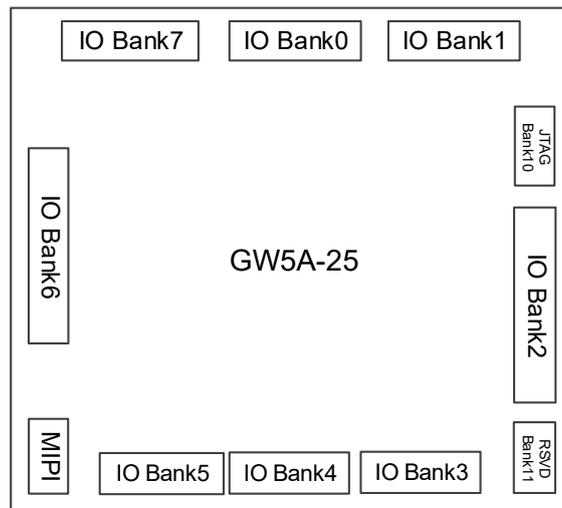
I/O Input Standard	Single-ended/ Differential	Bank $V_{CCIO}(V)$	Hysteresis	Need $V_{REF}$
LVC MOS33/ LV TTL33	Single-ended	3.3	Yes	No
LPDDR		1.8	Yes	No
PCI33		3.3	Yes	No
LVC MOS10UD12		1.2	Yes	No
LVC MOS10UD15		1.5	Yes	No
LVC MOS10UD18		1.8	Yes	No
LVC MOS10UD25		2.5	Yes	No
LVC MOS10UD33		3.3	Yes	No
LVC MOS12OD10		1.0	Yes	No
LVC MOS12UD15		1.5	Yes	No
LVC MOS12UD18		1.8	Yes	No
LVC MOS12UD25		2.5	Yes	No
LVC MOS12UD33		3.3	Yes	No
LVC MOS15OD10		1.0	Yes	No
LVC MOS15OD12		1.2	Yes	No
LVC MOS15UD18		1.8	Yes	No
LVC MOS15UD25		2.5	Yes	No
LVC MOS15UD33		3.3	Yes	No
LVC MOS18OD10		1.0	Yes	No
LVC MOS18OD12		1.2	Yes	No
LVC MOS18OD15		1.5	Yes	No
LVC MOS18UD25		2.5	Yes	No
LVC MOS18UD33		3.3	Yes	No
LVC MOS25OD10		2.5	Yes	No
LVC MOS25OD12		3.3	Yes	No
LVC MOS25OD15		1.5	Yes	No
LVC MOS25OD18		1.8	Yes	No
LVC MOS25UD33		3.3	Yes	No
LVC MOS33OD10		1.0	Yes	No
LVC MOS33OD12		1.2	Yes	No
LVC MOS33OD15		1.5	Yes	No
LVC MOS33OD18		1.8	Yes	No

I/O Input Standard	Single-ended/ Differential	Bank $V_{CCIO}$ (V)	Hysteresis	Need $V_{REF}$
LVC MOS33OD25	Single-ended	2.5	Yes	No
VREF1_DRIVER		1.8/1.2/1.5/2.5/3.3	No	Yes

### GW5A-25

GW5A-25 has eight GPIO Banks. Bank10 is a JTAG Bank with four IOs, Bank11 is Reserved Bank with one IO, as shown in [Figure 2-8](#).

**Figure 2-8 I/O Bank Distribution View (GW5A-25)**



Each Bank has independent I/O power supply  $V_{CCIO}$ .  $V_{CCIO}$  can be set as 3.3V, 2.5V, 1.8V, 1.5V, 1.35V, or 1.2V. The auxiliary voltage  $V_{CCX}$  supports 2.5V and 3.3V.

To support SSTL, HSTL, etc., each bank also provides one independent voltage source (VREF) as the reference voltage. You can choose from the internal reference voltage of the bank (0.6V, 0.75V, 0.9V, 1.25V, 1.5V and (36%,50%,64%) $V_{CCIO}$ ) or the external reference voltage using any IO from the bank.

Different banks in the support different on-chip resistor settings, including single-ended resistors and differential resistors. Single-ended resistor settings are used for SSTL/HSTL inputs and outputs. Differential resistor settings are used for LVDS/PPDS/ RSDS inputs. For more details, refer to [UG304, Arora V Programmable IO \(GPIO\) User Guide](#).

GW5A-25 I/O standards and configuration options supported are as listed in [Table 2-5](#) and [Table 2-6](#).

**Table 2-5 Output I/O Standards and Configuration Options**

I/O Output Standard	Single-ended/ Dif-ferential	Bank $V_{CCIO}$ (V)	Output Drive Strength (mA)	Typical Applications
MIPI_CPHY	Differential (TLVDS)	2.5/3.3	2	Mobile Industry Processor Interface

I/O Output Standard	Single-ended/ Differential	Bank $V_{CCIO}(V)$	Output Drive Strength (mA)	Typical Applications
MIPI	Differential (TLVDS)	1.8/2.5/3.3	2	Mobile Industry Processor Interface
MIPI_3MA	Differential (ELVDS)	1.8	3	Mobile Industry Processor Interface
MIPI_4MA		1.8	4	Mobile Industry Processor Interface
LVDS25	Differential (TLVDS)	2.5/3.3	3.5/2.5/4.5/6	High-speed point-to-point data transmission
BLVDS25		2.5/3.3	3.5/2.5/4.5/6	Multi-point high-speed data transmission
RSDS		2.5/3.3	3.5/2.5/4.5/6	High-speed point-to-point data transmission
MINILVDS		2.5/3.3	3.5/2.5/4.5/6	LCD timing driver interface and column driver interface
PPLVDS		2.5/3.3	3.5/2.5/4.5/6	LCD row/column driver
LVDS25E	Differential	2.5	8/2/4/6/12/16	High-speed point-to-point data transmission
BLVDS25E		2.5	8/2/4/6/12/16	Multi-point high-speed data transmission
MLVDS25E		2.5	8/2/4/6/12/16	LCD timing driver interface and column driver interface
RSDS25E		2.5	8/2/4/6/12/16	High-speed point-to-point data transmission
LVPECL33E		3.3	8/2/4/6/12/16	Universal interface
HSUL12D		1.2	8/2/4/6	LPDDR2
HSUL12D_I		1.2	8/2/4/6	LPDDR2
HSTL15D_I		1.5	8/4/12	Memory interface
HSTL18D_I		1.8	8/2/4/6/12/16	Memory interface
HSTL18D_II		1.8	8/2/4/6/12/16	Memory interface
SSTL12D_I		1.2	8/2/4/6	Memory interface
SSTL135D_I		1.35	8/2/4/6	Memory interface
SSTL15D_I		1.5	8/2/4/6/12	Memory interface
SSTL18D_I		1.8	8/2/4/6/12/16	Memory interface
SSTL18D_II	1.8	8/2/4/6/12/16	Memory interface	
SSTL25D_I	2.5	8/2/4/6/12/16	Memory interface	

I/O Output Standard	Single-ended/ Differential	Bank V <sub>CCIO</sub> (V)	Output Drive Strength (mA)	Typical Applications
SSTL25D_II	Differential	2.5	8/2/4/6/12/16	Memory interface
SSTL33D_I		3.3	8/2/4/6/12/16	Memory interface
SSTL33D_II		3.3	8/2/4/6/12/16	Memory interface
LPDDR		1.8	8/2/4/6/12/16	LPDDR and Mobile DDR
LVC MOS10D		1.0	2/4	Universal interface
LVC MOS12D		1.2	8/2/4/6	Universal interface
LVC MOS15D		1.5	8/2/4/6/12	Universal interface
LVC MOS18D		1.8	8/2/4/6/12/16	Universal interface
LVC MOS25D		2.5	8/2/4/6/12/16	Universal interface
LVC MOS33D		3.3	8/2/4/6/12/16	Universal interface
HSUL12	Single-ended	1.2	8/2/4/6	Memory interface
HSTL12_I		1.2	8/2/4/6	Memory interface
HSTL15_I		1.5	8/2/4/6/12	Memory interface
HSTL18_I		1.8	8/2/4/6/12/16	Memory interface
HSTL18_II		1.8	8/2/4/6/12/16	Memory interface
SSTL12_I		1.2	8/2/4/6	Memory interface
SSTL135_I		1.35	8/2/4/6	Memory interface
SSTL15_I		1.5	8/2/4/6/12	Memory interface
SSTL18_I		1.8	8/2/4/6/12/16	Memory interface
SSTL18_II		1.8	8/2/4/6/12/16	Memory interface
SSTL25_I		2.5	8/2/4/6/12/16	Memory interface
SSTL25_II		2.5	8/2/4/6/12/16	Memory interface
SSTL33_I		3.3	8/2/4/6/12/16	Memory interface
SSTL33_II		3.3	8/2/4/6/12/16	Memory interface
LVC MOS10		1.0	2/4	Universal interface
LVC MOS12		1.2	8/2/4/6	Universal interface
LVC MOS15		1.5	8/2/4/6/12	Universal interface
LVC MOS18		1.8	8/2/4/6/12/16	Universal interface
LVC MOS25		2.5	8/2/4/6/12/16	Universal interface
LVC MOS33/ LVTTTL33		3.3	8/2/4/6/12/16	Universal interface
LPDDR	1.8	8/2/4/6/12/16	LPDDR and Mobile DDR	

I/O Output Standard	Single-ended/ Differential	Bank $V_{CCIO}(V)$	Output Drive Strength (mA)	Typical Applications
PCI33	Single-ended	3.3	8/2/4/6/12/16	PC and embedded system

Table 2-6 Input I/O Standards and Configuration Options

I/O Input Standard	Single-ended/ Differential	Bank $V_{CCIO}(V)$	Hysteresis	Need $V_{REF}$
MIPI_CPHY	Differential	1.2/1.5/1.8	No	No
MIPI		1.2/1.5/1.8	No	No
ADC_IN		2.5/1.0/1.2/1.5/1.8/3.3	No	No
LVDS25		2.5/1.0/1.2/1.5/1.8/3.3	No	No
BLVDS25		2.5/1.0/1.2/1.5/1.8/3.3	No	No
RSDS		2.5/1.0/1.2/1.5/1.8/3.3	No	No
MINILVDS		2.5/1.0/1.2/1.5/1.8/3.3	No	No
PPLVDS		2.5/1.0/1.2/1.5/1.8/3.3	No	No
HSUL12D		1.2/1.0/1.5/1.8/2.5/3.3	No	No
HSTL12D_I		1.2/1.0/1.5/1.8/2.5/3.3	No	No
HSTL15D_I		1.5/1.0/1.2/1.8/2.5/3.3	No	No
HSTL18D_I		1.8/1.0/1.2/1.5/2.5/3.3	No	No
HSTL18D_II		1.8/1.0/1.2/1.5/2.5/3.3	No	No
SSTL135D_I		1.35/1.0/1.2/1.5/1.8/2.5/3.3	No	No
SSTL15D_I		1.5/1.0/1.2/1.8/2.5/3.3	No	No
SSTL18D_I		1.8/1.0/1.2/1.5/2.5/3.3	No	No
SSTL18D_II		1.8/1.0/1.2/1.5/2.5/3.3	No	No
SSTL25D_I		2.5/1.0/1.2/1.5/1.8/3.3	No	No
SSTL25D_II		2.5/1.0/1.2/1.5/1.8/3.3	No	No
SSTL33D_I		3.3/1.0/1.2/1.5/1.8/2.5	No	No
SSTL33D_II		3.3/1.0/1.2/1.5/1.8/2.5	No	No
LPDDR		1.8/1.0/1.2/1.5/2.5/3.3	No	No
LVC MOS10D		1.0/1.2/1.5/1.8/2.5/3.3	No	No
LVC MOS12D		1.2/1.0/1.5/1.8/2.5/3.3	No	No
LVC MOS15D		1.5/1.0/1.2/1.8/2.5/3.3	No	No
LVC MOS18D		1.8/1.0/1.2/1.5/2.5/3.3	No	No
LVC MOS25D		2.5/1.0/1.2/1.5/1.8/3.3	No	No

I/O Input Standard	Single-ended/ Differential	Bank $V_{CCIO}(V)$	Hysteresis	Need $V_{REF}$
LVC MOS33D	Differential	3.3/1.0/1.2/1.5/2.5/1.8	No	No
HSUL12	Single-ended	1.2	Yes	No
HSTL12_I		1.2	Yes	No
HSTL15_I		1.5	Yes	No
HSTL15_II		1.5	Yes	No
HSTL18_I		1.8	Yes	No
HSTL18_II		1.8	Yes	No
SSTL135_I		1.35	Yes	No
SSTL15_I		1.5	Yes	No
SSTL18_I		1.8	Yes	No
SSTL18_II		1.8	Yes	No
SSTL25_I		2.5	Yes	No
SSTL25_II		2.5	Yes	No
SSTL33_I		3.3	Yes	No
SSTL33_II		3.3	Yes	No
LVC MOS10		1.0	Yes	No
LVC MOS12		1.2	Yes	No
LVC MOS15		1.5	Yes	No
LVC MOS18		1.8	Yes	No
LVC MOS25		2.5	Yes	No
LVC MOS33/ LV TTL33		3.3	Yes	No
LPDDR		1.8	Yes	No
PCI33		3.3	Yes	No
LVC MOS10UD12		1.2	Yes	No
LVC MOS10UD15		1.5	Yes	No
LVC MOS10UD18		1.8	Yes	No
LVC MOS10UD25		2.5	Yes	No
LVC MOS10UD33	3.3	Yes	No	
LVC MOS12OD10	1.0	Yes	No	
LVC MOS12UD15	1.5	Yes	No	
LVC MOS12UD18	1.8	Yes	No	
LVC MOS12UD25	2.5	Yes	No	

I/O Input Standard	Single-ended/ Differential	Bank $V_{CCIO}$ (V)	Hysteresis	Need $V_{REF}$
LVC MOS12UD33	Single-ended	3.3	Yes	No
LVC MOS15OD10		1.0	Yes	No
LVC MOS15OD12		1.2	Yes	No
LVC MOS15UD18		1.8	Yes	No
LVC MOS15UD25		2.5	Yes	No
LVC MOS15UD33		3.3	Yes	No
LVC MOS18OD10		1.0	Yes	No
LVC MOS18OD12		1.2	Yes	No
LVC MOS18OD15		1.5	Yes	No
LVC MOS18UD25		2.5	Yes	No
LVC MOS18UD33		3.3	Yes	No
LVC MOS25OD10		2.5	Yes	No
LVC MOS25OD12		3.3	Yes	No
LVC MOS25OD15		1.5	Yes	No
LVC MOS25OD18		1.8	Yes	No
LVC MOS25UD33		3.3	Yes	No
LVC MOS33OD10		1.0	Yes	No
LVC MOS33OD12		1.2	Yes	No
LVC MOS33OD15		1.5	Yes	No
LVC MOS33OD18		1.8	Yes	No
LVC MOS33OD25		2.5	Yes	No
VREF1_DRIVER			1.8/1.2/1.5/2.5/3.3	No

### 2.3.2 I/O Logic

Figure 2-9 shows the I/O logic output of GW5A Series of FPGA Products

Figure 2-9 I/O Logic Output

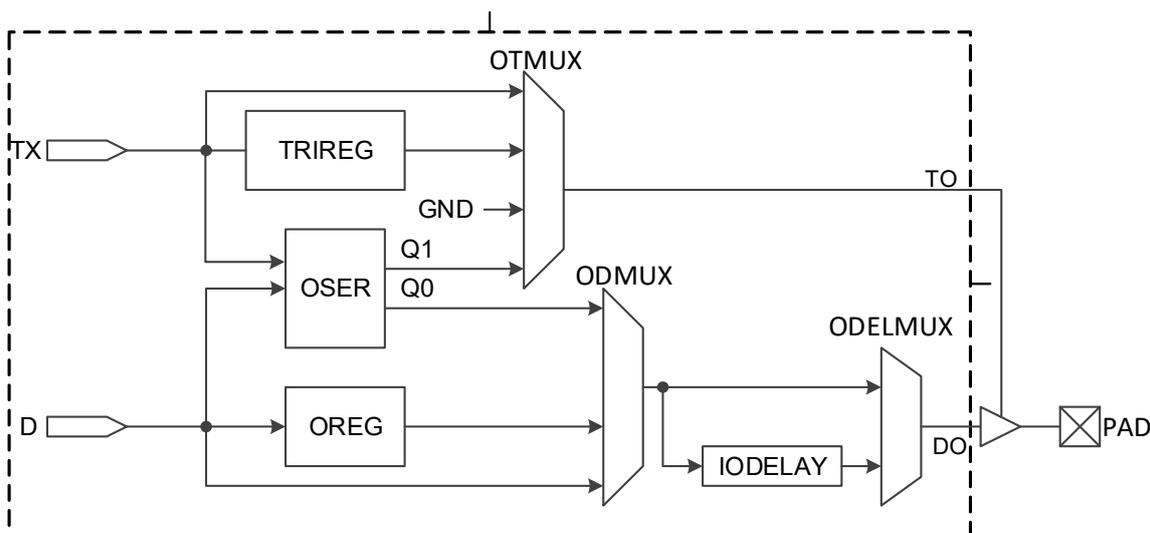
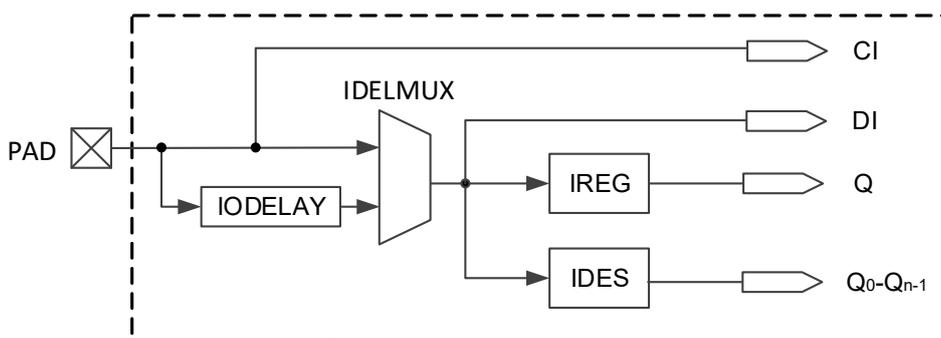


Figure 2-10 shows the I/O logic input of GW5A Series of FPGA Products.

Figure 2-10 I/O Logic Input



Descriptions of the I/O logic modules of products are presented below.

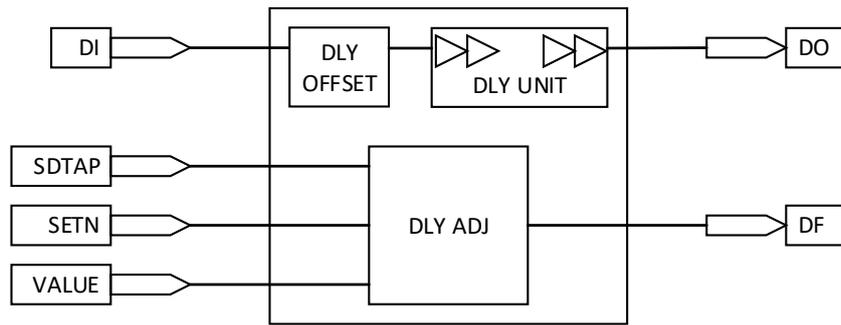
Delay Module

See Figure 2-11 for an overview of the IODELAY. Each I/O contains an IODELAY module, which allows the user to add additional delays to the I/Os to adjust the delay of the input and output signals. The delay time for each step is  $T_{dlyunit}$ , and the total number of delay steps is DLYSTEP. The total IODELAY delay time is:  $T_{totdly} = T_{dlyoffset} + T_{dlyunit} * DLYSTEP$ . The total delay reference time is as shown in Table 2-7.

Table 2-7 Total Delay Reference of IODELAY

	Min.	Typ.	Max.
$T_{dlyoffset}$	200 ps	250 ps	300 ps
$T_{dlyunit}$	10 ps	12.5 ps	15 ps
DLYSTEP	1	-	256

Figure 2-11 IODELAY View



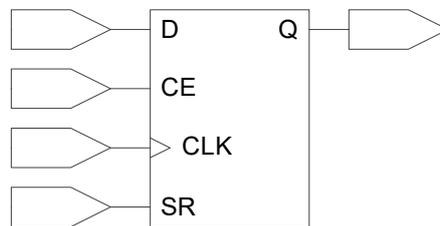
There are three ways to control the delay:

- Static control.
- Dynamic control, which can be combined with logic function circuits to achieve dynamic delay adjustment.
- Adaptive control.

I/O Register

See Figure 2-12 for the I/O Register diagram. Each I/O provides an input register (IREG), an output register(OREG), and a tristate Register(TRIREG).

Figure 2-12 Diagram of I/O registers



**Note!**

- CE can be either active low (0: enable) or active high (1: enable).
- CLK can be either rising edge trigger or falling edge trigger.
- SR can be either synchronous/asynchronous SET or RESET or disable.
- The registers can be programmed as registers(DFFs) or latches.

DES and SER

GW5A Series of FPGA Products support serialization and deserialization of various ratios, as listed in Table 2-8.

Table 2-8 Serialization/Deserialization

Input/output	Ratios Supported
Input Logic	1:2 / 1:4 / 1:7 / 1:8 / 1:10 / 1:14 / 1:16 / 1:32

Input/output	Ratios Supported
Output Logic	2:1 / 4:1/ 7:1 / 8:1 / 10:1 / 16:1 / 14:1 <sup>[1]</sup>

**Note!**

GW5A-138 does not support 14:1.

**2.3.3 I/O Logic Modes**

The I/O Logic supports multiple modes. In each operation, the I/O (or I/O differential pair) can be configured as output, input, and INOUT or tristate output (output signal with tristate control).

For further details about the I/O logic modes, please refer to [UG304, Arora V Programmable IO \(GPIO\) User Guide](#).

**2.4 Block SRAM (BSRAM)****2.4.1 Introduction**

GW5A Series of FPGA Products provide abundant block SRAM resources. These memory resources are distributed throughout the FPGA array in rows. Therefore, they are called block static random access memories (BSRAMs). There are five operation modes: Single Port mode, Dual Port mode, Semi Dual Port mode, Semi Dual Port mode with ECC function, and ROM mode.

An abundance of BSRAM resources provide a guarantee for the user's high-performance design. BSRAM's features:

- The capacity of a BSRAM is 18 Kbits, can be configured up to 36Kbits
- Clock frequency up to 380MHz
- Supports Single Port mode
- Supports Dual Port mode
- Supports Semi Dual Port Mode
- Supports Semi-Dual Port mode with ECC function, provides ECC detection and error correction function
- Supports ROM Mode
- Data width up to 72bits
- Supports byte-enable
- Dual Port and Semi-dual Port support independent clocks and independent data width
- Read mode supports Register Output and Bypass Output
- Write mode supports Normal, Read-before-Write, and Write-Through
- Input registers support synchronous writes

## 2.4.2 Configuration Mode

BSRAMs in the products support various data widths. See [Table 2-9](#).

**Table 2-9 Memory Size Configuration**

Capacity	Single Port Mode	Dual Port Mode	Semi Dual Port Mode	Semi Dual Port Mode with ECC Function	Read Only Mode
16Kbits	16K x 1	16K x 1	16K x 1	–	16K x 1
	8K x 2	8K x 2	8K x 2	–	8K x 2
	4K x 4	4K x 4	4K x 4	–	4K x 4
	2K x 8	2K x 8	2K x 8	–	2K x 8
	1K x 16	1K x 16	1K x 16	–	1K x 16
	512 x 32	–	512 x 32	–	512 x 32
18Kbits	2K x 9	2K x 9	2K x 9	–	2K x 9
	1K x 18	1K x 18	1K x 18	–	1K x 18
	512 x 36	–	512 x 36	–	512 x 36
36Kbits <sup>[1]</sup>	–	–	–	512 x 72	–

### Note!

<sup>[1]</sup>25K devices do not support Semi Dual Port Mode with ECC Function.

For more information on Single Port mode, Dual Port mode, Semi-Dual Port mode, Semi-Dual Port with ECC Function, and ROM mode, please refer to [UG300, Arora V BSRAM & SSRAM User Guide](#).

## 2.4.3 ECC

The BSRAM has a built-in ECC hardcore module, which is mainly used for data detection and correction during data transfer and storage. The features are as follows:

- ECC error detection and correction only supported in SDP 512 x 64 mode
- Supports 1-bit error correction and 2-bit error alarm in 64-bit SRAM data
- 72-bit ECC module contains 64-bit data bits and 8-bit parity bits;
- Bit 31 and bit 63 support 1-bit and 2-bit error injection

## 2.5 DSP

GW5A Series of FPGA Products provide brand new DSP resources. This DSP solution can meet user demands for high performance digital signal processing design, such as FIR, FFT, etc. The DSP blocks have the advantages of stable timing performance, high resource utilization, and low power consumption.

The features of DSP are as follows.

- Multiplier with three widths: 12X12, 27X18, 27X36
- 26-bit pre-adder
- 48-bit ALU
- Supports Shift function
- Multiple multipliers can achieve multiply of larger data widths by cascading
- Supports accumulation, multiplication and addition of 27X18 multipliers
- Supports the accumulation after summation of two 12X12 multipliers
- Supports the pipeline and bypass functions of registers
- All operands for arithmetic operation are signed numbers

Each DSP consists of three stages:

- PADD
- MULT
- Arithmetic Logic Unit

### 2.5.1 PADD

Each DSP features one PADD(pre-adder) for implementing pre-addition, pre-subtraction, and shifting.

PADD locates at the first stage with two inputs. Each input end supports pipeline mode and bypass mode.

### 2.5.2 MULT

Each DSP block has one 27 x 18 multiplier M0 and one 12 x 12 multiplier M1. The multipliers are located after the pre-adders to implement multiplication operations, and both the inputs and outputs support register mode and bypass mode.

Multiplier M0 can be configured as:

- One 27 x 18 multiplier
- One 12 x 12 multiplier
- Two DSPs can form a 27 x 36 multiplier

Multiplier M1 can only be configured as one 12 x 12 multiplier.

When multiplier M0 and multiplier M1 are both configured as a 12 x 12 multiplier and the ALU is enabled, 12 x 12 SUM mode can be achieved.

### 2.5.3 Arithmetic Logic Unit

Each Macro has one four-input 48-bit ALU, which can further enhance MULT's functions. Register mode and bypass mode are supported both in the inputs and outputs.

The ALU supports the addition/subtraction operations of multiplier output, ALU cascade input and ALU output feedback, or static PRE\_LOAD value.

### 2.5.4 Operating Mode

Multiple operation modes of the DSP can be realized by control signals. Operation Modes:

- Multiplier
- Accumulator
- MULTADDALU
- Addition (48+48)

For more information on DSP Blocks, see [UG305, Arora V Digital Signal Processing \(DSP\) User Guide](#).

## 2.6 MIPI D-PHY

### 2.6.1 Hardcore MIPI D-PHY RX/TX

GW5A Series of FPGA Products include the Hardcore MIPI D-PHY RX/TX. The dedicated D-PHY core supports MIPI DSI and CSI-2 mobile video interfaces for cameras and displays. The main features are as follows:

- In line with *MIPI Supported Standard for D-PHY Specification*, version 1.2.
- GW5A-60 and GW5A-15 support RX/TX Combo-PHY, which can be configured as either RX or TX based on user requirements.
- Unidirectional HS (High-speed) mode at up to 2.5 Gbps per lane and 10 Gbps per quad (4 data lanes). Up to 20 Gbps supported by each chip (8 data lanes).
- Supports two MIPI D-PHY quads, up to 4 data lanes and one clock lane for each quad.
- Bidirectional Low-power (LP) mode with a bit rate of 10Mbps.
- Built-in HS Sync, bit alignment in the lane (Word Alignment) and word alignment between lanes (Lane Alignment).
- MIPI D-PHY RX supports 1:8 mode and 1:16 mode.
- GW5A-25 and GW5A-60 MIPI D-PHY TX supports 8:1 mode and 16:1 mode.
- Supports MIPI DSI and MIPI CSI-2 link layers.
- A dedicated MIPI Bank for the hardcore MIPI D-PHY.

For more information on Gowin MIPI D-PHY RX, please refer to [UG296](#), [Arora V Hardened MIPI D-PHY User Guide](#).

### 2.6.2 GPIO Supports MIPI D-PHY RX/TX

When implementing soft MIPI D-PHY RX/TX with GPIOs, three IO types are available: TLVDS, ELVDS, and MIPI IO.

All GW5A Series of FPGA Products support the TLVDS/ELVDS types. To implement MIPI D-PHY with the TLVDS/ELVDS types, you need to emulate MIPI HS and MIPI LP by using LVDS25(E)+LVCMOS12 and need to add external resistors. Some GW5A Series of FPGA Products support the MIPI-IO type. The MIPI IO has an internal resistor network and supports automatic switching between HS and LP. The support list of the MIPI IO type is shown in [Table 2-10](#).

For information on IO type selection and off-chip termination, please refer to [IPUG948E](#), [MIPI D-PHY RX TX Advance User Guide](#) > “4 Functional Description”.

Table 2-10 GW5A Series of FPGA Products MIPI IO Type Support List

Device	MIPI RX	MIPI TX
GW5A-25	All Banks (except JTAG bank and Reserved Bank)	All Banks (except JTAG bank and Reserved Bank)
GW5A-60	All Banks (except JTAG Bank)	All Banks (except JTAG Bank)
GW5A-138	All Banks	–

The main features are as follows:

- In line with *MIPI Supported Standard for D-PHY Specification*, version 1.2;
- 138K: High Speed RX and TX interfaces with RX transfer rates of up to 1.5 Gbps per lane and TX transfer rates up to 1.6Gbps per lane.
- 60K/25K: High Speed RX and TX interfaces with RX transfer rates of up to 1.6 Gbps per lane and TX transfer rates up to 2.0Gbps per lane.
- Supports unidirectional High-speed (HS) mode
- Supports bidirectional Low-power operation mode
- Deserializes and serializes high-speed data into byte data packets
- Supports MIPI D-PHY TX 8:1 mode and 16:1 mode
- Supports MIPI D-PHY RX 1:8 mode and 1:16 mode
- Supports IO Types of ELVDS, TLVDS, and MIPI IO
- Control data is transmitted in LP mode at a data rate of 10 Mb/s.

## 2.7 MIPI C-PHY

### 2.7.1 Hardcore MIPI C-PHY

The GW5A-60 products offer the hard-core MIPI C-PHY RX and TX, featuring highly efficient data transfer rates, and is primarily suitable for high-speed serial interfaces between cameras and image processors.

- MIPI Alliance Standard for C-PHY Specification, Version 1.2.
- Supports RX/TX Combo-PHY, which can be configured as either RX or TX based on user requirements.
- One MIPI Quad supports up to 3-trios data lanes and RX/TX supports up to 2.5Gbps per lane.
- MIPI C-PHY RX supports high-speed mode and automatic interrupt control..
- MIPI C-PHY TX supports high-speed mode.
- Bidirectional Low mode with data rates up to 10Mbps.
- High speed RX mode supports De-skew function.
- RX supports a linear equalizer with a maximum Delta peak > 8dB.

- Supports ALP mode (optional).

## 2.8 ADC

### 2.8.1 ADC

GW5A-138 and GW5A-25 devices integrate one eight-channel 10 bits Delta-sigma ADC. It is an ADC with low power, low-leakage current, and high dynamic performance.

Combined with the programmable logic capability of the FPGA, and the integrated voltage and temperature sensing unit, the ADC can meet the internal temperature and power monitoring and data collection requirements. At the same time, the FPGA provides rich and free configurable GPIO interfaces and ADC analog signal interfaces to connect to the voltage channel of the ADC, which can meet the voltage data collection and monitoring requirements outside the chip.

The main features are as follows:

- Number of ADCs for 25K devices: 1
- Number of ADCs for 138K devices: 2
- Reference voltage source: Built-in
- Bit width accuracy: 10 bits
- Sampling Clock: < 2MHz
- ADC unipolar input voltage: 0~1V
- 60dB SNR
- Temperature sensor accuracy: +/-2°C
- Voltage sensor accuracy: +/-5mV

For more information on ADC, see [UG299E, Arora V ADC User Guide](#).

### 2.8.2 SARADC

GW5A-60 integrates a SARADC. SARADC is a 13bit ADC for high-speed signal sampling, which is capable of meeting high-precision reference voltage requirements, and is usually used in scenarios requiring high precision. The main features are as follows:

- Reference voltage source: Built-in
- Number of input channel per ADC: Supports up to 122 channels<sup>[1]</sup>
- Bit width accuracy: 13 bits
- Maximum sampling rate: 10Msps
- Sampling Clock: 10MHz~ 320MHz
- Single-ended input signal range: 0V -1V
- Differential signal range: -1V ~ 1V
- Voltage sensor resolution: +/-0.3mV

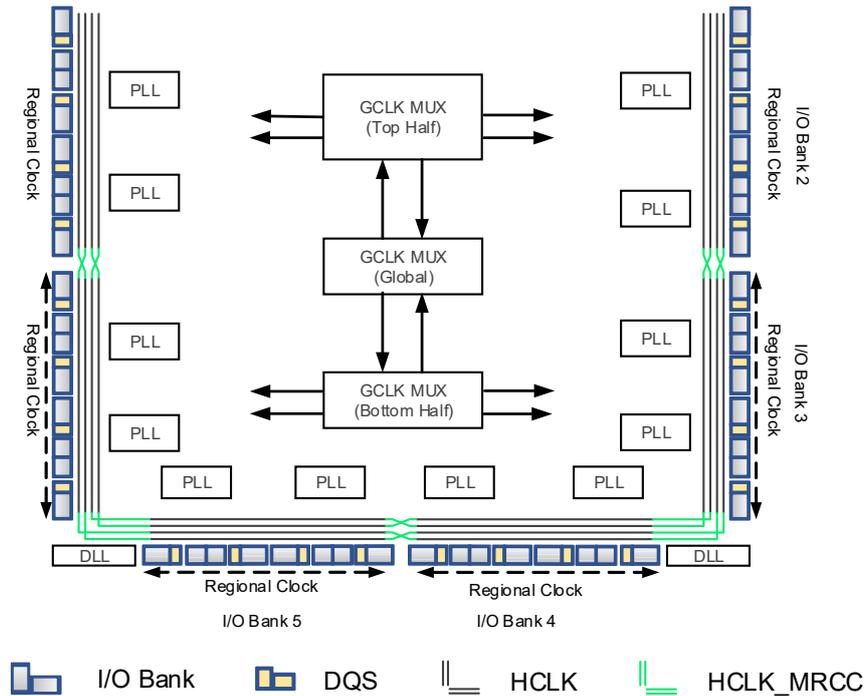
**Note!**

Refer to Pinout manuals for details on the number of input channels supported.

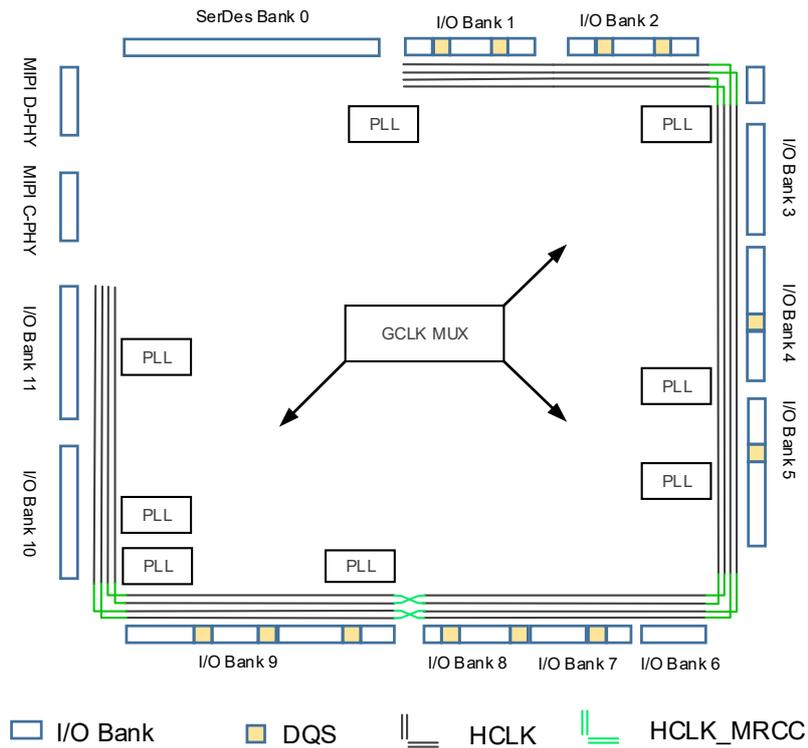
## 2.9 Clock

The clock resources and wiring are critical for high-performance applications in FPGA. GW5A Series of FPGA Products provide the global clock network (GCLK) which connects to all the registers directly. In addition to the GCLK, PLL, HCLK, DDR memory interface, and DQS, etc. are also provided.

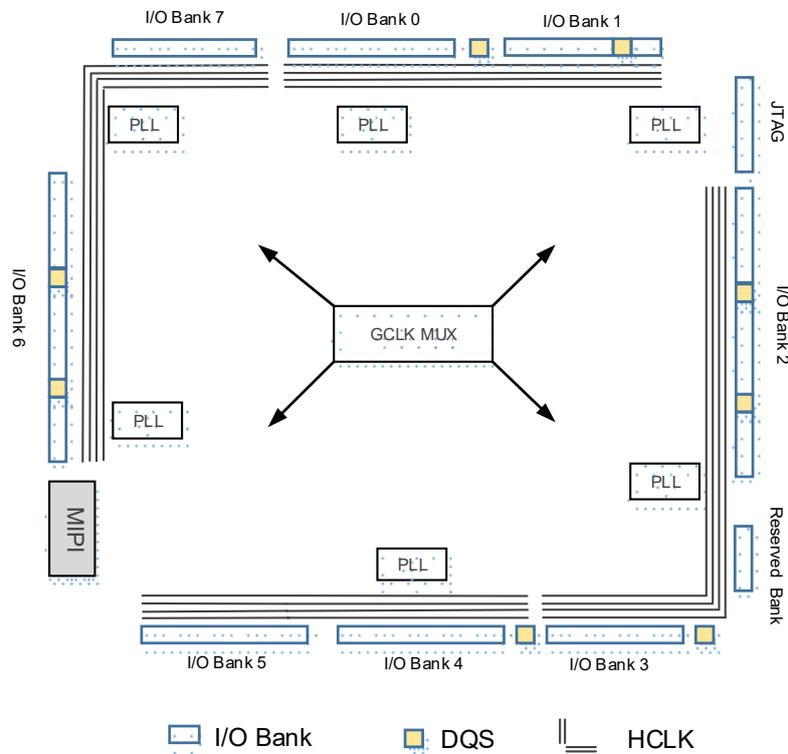
Figure 2-13 Clock Resources(GW5A-138)



**Figure 2-14 Clock Resources(GW5A-60)**



**Figure 2-15 Clock Resources(GW5A-25)**



Please refer to [2.9.1 Global Clock](#) ~ [2.9.4 DDR Memory Interface Clock Management](#) **DQS** for a brief introduction. For further detailed information on the GCLK, HCLK, DDR memory interface, and DQS, see [UG306, Arora V Clock User Guide](#).

### 2.9.1 Global Clock

GW5A Series of FPGA Products provide 16 global clocks. The clock source of GCLK comes from dedicated clock pins, PLL outputs, SERDES clocks, HCLK outputs, and common routing resources. Using a dedicated clock input pin provides better clock performance and enables driving of the global.

### 2.9.2 High-speed Clock

HCLK is the high-speed clock with low jitter and low skew. It can support high-performance data transfer and is mainly suitable for source synchronous data transfer protocols. One bank supports 4 HCLKs, as shown in Figure 2-16, Figure 2-17, Figure 2-18 .

Figure 2-16 HCLK Structure View (GW5A-138)

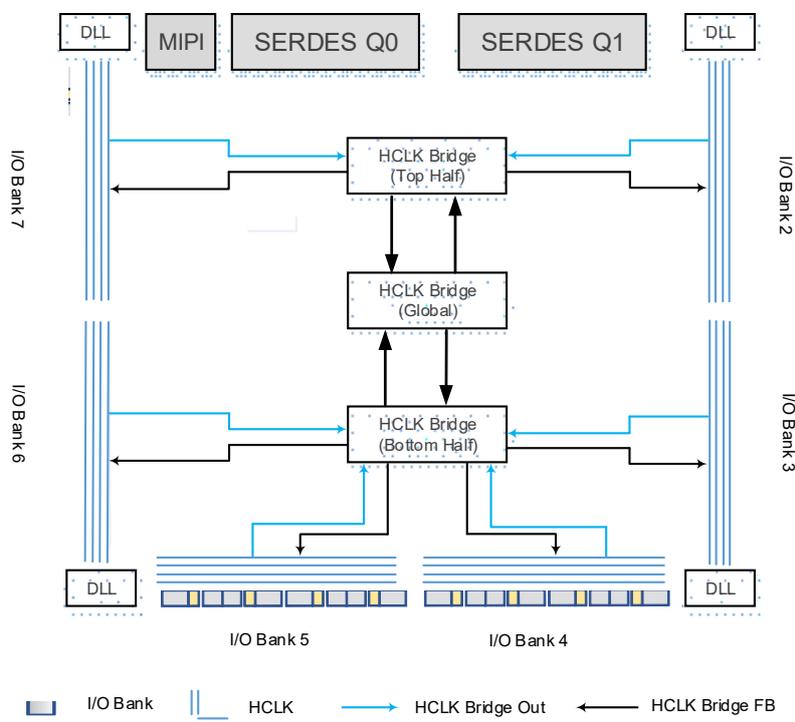


Figure 2-17 HCLK Structure View (GW5A-60)

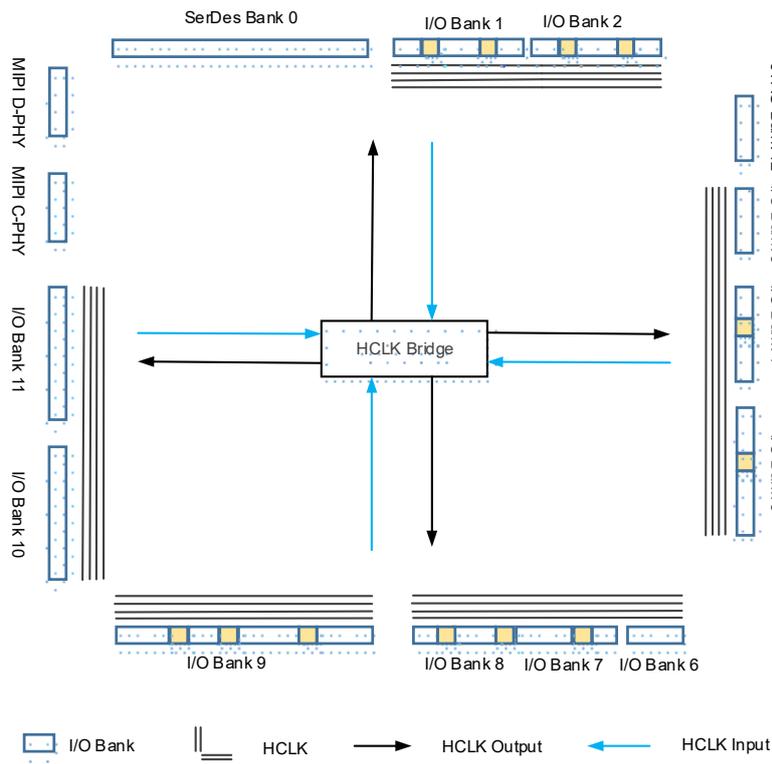
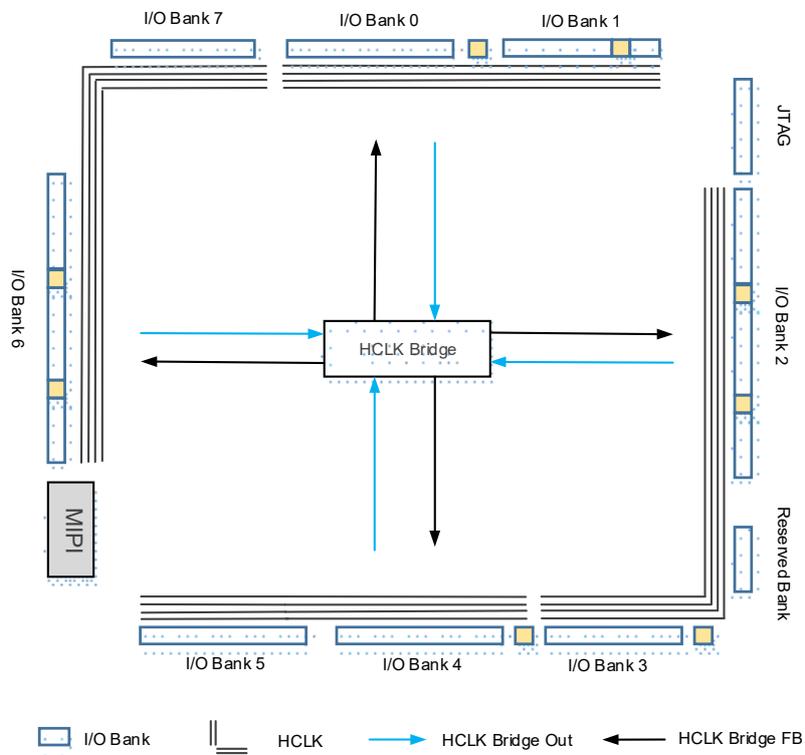


Figure 2-18 HCLK Structure View (GW5A-25)



HCLK can provide user with the function modules as follows:

- Dynamic high-speed clock enable module. Able to dynamically turn on/off the high-speed clock signal.
- High speed clock frequency division module, generating a divided clock of the input clock. Used in the IO logic mode.
- Dynamic high speed clock selector.
- Dynamic delay adjustment module, producing the clock signal for the dedicated clock pin input.
- HCLK Bridge, able to send HCLK clock signals to any of the Banks. In addition, the HCLK clock signal can span to the clock tree of the adjacent IO Bank after entering from the IO Bank.

**Note!**

For high speed signals of the same source, it is recommended to put them in the same IO Bank to achieve a minimum skew between signals.

### 2.9.3 Phase-locked Loop

PLL (Phase-locked Loop) is one kind of a feedback control circuit. The frequency and phase of the internal oscillator signal is controlled by the external input reference clock.

The PLL module can provide synthesizable clock frequencies. Frequency adjustment (multiply and division), phase adjustment, and duty cycle adjustment can be achieved by configuring the parameters.

The PLL features are as follows:

- Supports seven clock outputs
- Integer PLL, the first clock output and feedback clock output support 1/8 fractional output division
- Supports phase shift and duty cycle adjustment
- Frequency Lock detection
- Supports spread spectrum clock generation(IP required)
- VCO frequency range: 800 MHz ~ 1600 MHz
- CLKIN frequency range: 19 MHz ~ 800 MHz.

### 2.9.4 DDR Memory Interface Clock Management DQS

The DQS module of the products provides the following features to support the clock requirements of the DDR memory interface:

- Receive DQS input, sort out waveform and shift 1/4 phase
- Provide a read / write pointer for input cache
- Provide valid data for internal logic
- Provide DDR output clock signal
- Support DDR3 write voltage control

The DQS module supports multiple operating modes to meet the needs of different I/O interfaces.

## 2.9.5 Long Wire

As an effective complement to CRUs, GW5A Series of FPGA Products provide flexible and rich long-wire (LW) resources. LW can be used as a control wire to provide clock enable (CE) for DFF, set/reset signal; it can also be used as logic winding and as a common data signal.

## 2.10 Global Set/Reset (GSR)

A global set/reset (GSR) network is built in the product. There is a direct connection to core logic. It can be used as asynchronous/synchronous set. The registers in CFU and I/O can be individually configured to use GSR.

## 2.11 Programming & Configuration

GW5A Series of FPGA Products support SRAM configuration. Each time the device is powered on, the bitstream needs to be downloaded to configure the device. You can also save the configuration data in an external Flash. After power-up, the devices load configuration data from the external Flash into the SRAM.

Besides JTAG, the devices also support GowinCONFIG configuration modes: SSPI, MSPI, Master CPU, Slave CPU, Master SERIAL, and Slave SERIAL. The FPGAs also support background programming, datastream file encryption and security bit setting, SEU detection and error correction, and OTP.

For more detailed information, please refer to:

- [UG704E, Arora V 138K& 75K FPGA Products Programming and Configuration User Guide](#)
- [UG718E, Arora V 60K FPGA Products Programming and Configuration User Guide](#)
- [UG714E, Arora V 25K FPGA Products Programming and Configuration User Guide](#)

### 2.11.1 Background Upgrade

The products support background upgrade by JTAG/SSPI/QSSPI or using the goConfig I2C IP / goConfig JTAG IP, that is, the device supports programming the embedded Flash or the external Flash without affecting the existing working state, the device can work normally according to the original configuration during the programming process. After the programming is completed, trigger RECONFIG\_N with a low level or use "Reboot" to complete the online upgrade. This feature applies to the applications requiring long online time and irregular upgrades.

## 2.11.2 Bitstream File Encryption & Security Bit Setting

GW5A Series of FPGA Products support bitstream data encryption with 128-bit AES encryption algorithm. At the same time, GOWINSEMI adds CRC and sets security bits in the bitstream file of FPGA products by default in order to guarantee the safe and accurate transmission of configuration data. During the data configuration process, the input data is verified in real time for errors, and the device cannot be woken up by incorrect data. After the configuration of the bitstream with security bit is complete, data readback cannot be performed.

## 2.11.3 SEU Handler

The SEU Handler module integrated features Configuration Memory Soft Error Recovery (CMSER). It detects the possible soft errors by continuously monitoring the configuration memory and attempts to correct them within its capabilities. While the FPGA is working, it reads the configuration data frame by frame from the background and performs ECC decoding and CRC checksum comparison to detect errors. If the error can be corrected, the calculated error-corrected data bits are rewritten to the SRAM.

The SEU Handler module functions and features are as follows:

- Based on ECC and CRC detection and correction algorithms
- CRC can report any number of bit errors during configuration of the SRAM.
- ECC supports 2-bit error location report and error correction<sup>[1]</sup> and 4-bit error alarm in each SRAM Frame. 138K devices support 1-bit error location report and error correction and 2-bit error alarm in each 64-bit SRAM Frame.

### Note!

<sup>[1]</sup> SEU Handler can support faster error correction. Please contact local technical support for details.

- Can be enabled or disabled by user logic or enabled automatically upon program wakeup
- Supports single bit error injection by user logic for the functional verification and evaluation.

## 2.11.4 OTP

GW5A Series of FPGA Products provide a 128-bit OTP space and support one-time programming. Bit0~Bit31 is the user space, which can be used to store security and other important information. Bit32~Bit95 is the DNA space, which stores the 64-bit unique identification information of the device.

## 2.12 On Chip Oscillator

There is an internal oscillator in each of the products. During the configuration process, it can provide a clock for the MSPI mode. The on-chip oscillator also provides a clock

resource for user designs. Up to 64 clock frequencies can be obtained by setting the parameters. The following formula is employed to get the output clock frequency:

$$f_{\text{out}} = 210\text{MHz}/\text{Param}$$

**Note!**

“Param” is the configuration parameter. It is 3 or an even number between 2 and 126.

# 3 AC/DC Characteristic

## Note!

You should ensure GOWINSEMI® products are always used within recommended operating conditions and range. Data beyond the working conditions and range are for reference only. GOWINSEMI® does not guarantee that all devices will operate as expected beyond the standard operating conditions and range.

## 3.1 Operating Conditions

### 3.1.1 Absolute Max. Ratings

GW5A-138

Table 3-1 Absolute Max. Ratings(GW5A-138)

Name	Description	Min.	Max.
FPGA Logic			
$V_{CC}$	Core voltage	-0.5V	1.05V
$V_{CCIO}$	I/O Bank voltage	-0.5V	3.75V
$V_{CCX}$	Auxiliary voltage	-0.5V	3.75V
$V_{CCLDO}$	Voltage for the internal LDO module that powers the PLL and SRAM	-0.5V	1.98V
MIPI			
$V_{DDAM}$	Analog core power supply	-0.5V	1.05V
$V_{DDXM}$	Analog auxiliary power supply	-0.5V	1.98V
$V_{DDDM}$	Digital core power supply	-0.5V	1.05V
Temperature			
Storage Temperature	Storage Temperature	-65°C	+150°C
Junction Temperature	Junction Temperature	-40°C	+125°C

## GW5A-60

Table 3-2 Absolute Max. Ratings(GW5A-60)

Name	Description	Min.	Max.
FPGA Logic			
V <sub>CC</sub>	Core voltage, LV	-0.5V	1.05V
	Core voltage, EV	-0.5V	3.75V
V <sub>CCIO</sub>	I/O Bank voltage	-0.5V	3.75V
V <sub>CCX</sub>	Auxiliary voltage	-0.5V	3.75V
V <sub>EFUSE</sub>	Voltage required for eFuse writing	-0.5V	2.07V
MIPI			
V <sub>DDAM</sub>	Analog core power supply	-0.5V	1.08V
V <sub>DDXM</sub>	Analog auxiliary power supply	-0.5V	3.75V
V <sub>DDDM</sub>	Digital core power supply	-0.5V	1.08V
V <sub>DD12M</sub>	MIPI LP power supply	-0.5V	1.32V
ADC			
V <sub>CCLDOADC</sub>	The supply voltage for the internal LDO module that powers the ADC	-0.5V	1.98V
V <sub>CCADC</sub>	ADC power supply	-0.5V	2.07V
V <sub>REFN</sub>	ADC Module reference voltage	-0.5V	0.3V
V <sub>REFP</sub>	ADC Module reference voltage	-0.5V	2.07V
Temperature			
Storage Temperature	Storage Temperature	-65°C	+150°C
Junction Temperature	Junction Temperature	-40°C	+125°C

## GW5A-25

Table 3-3 Absolute Max. Ratings(GW5A-25)

Name	Description	Min.	Max.
V <sub>CC</sub>	Core voltage, LV	-0.5V	1.05V
	Core voltage, EV	-0.5V	3.75V
V <sub>CCIO</sub>	I/O Bank voltage	-0.5V	3.75V
V <sub>CCX</sub>	Auxiliary voltage	-0.5V	3.75V
V <sub>CCLDO</sub>	Voltage for the internal LDO module that powers the PLL and SRAM	-0.5V	3.75V
V <sub>EFUSE</sub>	Voltage required for eFuse writing	-0.5V	2.07V

Name	Description	Min.	Max.
V <sub>DDAM</sub>	Analog core power supply	-0.5V	1.05V
V <sub>DDDM</sub>	Digital core power supply	-0.5V	1.05V
V <sub>DDXM</sub>	Analog auxiliary voltage power supply	-0.5V	3.75V
V <sub>DD12M</sub>	MIPI LP power supply	-0.5V	1.32V
Storage Temperature	Storage Temperature	-65°C	+150°C
Junction Temperature	Junction Temperature	-40°C	+125°C

### 3.1.2 Recommended Operating Conditions

GW5A-138

Table 3-4 Recommended Operating Conditions(GW5A-138)

Name	Description	Min.	Max.
FPGA Logic			
V <sub>CC</sub>	Core voltage	0.87V	1.03V
V <sub>CCIO</sub>	I/O Bank voltage	1V	3.465V
V <sub>CCX</sub>	Auxiliary voltage	1.71V	1.89V
V <sub>CCLDO</sub> <sup>[1]</sup>	Voltage for the internal LDO module that powers the PLL and SRAM	1.14V	1.89V
MIPI			
V <sub>DDAM</sub>	Analog core power supply	0.87V	1.03V
V <sub>DDXM</sub>	Analog auxiliary voltage power supply	1.71V	1.89V
V <sub>DDDM</sub>	Digital core power supply	0.87V	1.03V
Temperature			
T <sub>JCOM</sub>	Junction temperature Commercial operation	0°C	+85°C
T <sub>JIND</sub>	Junction temperature Industrial operation	-40°C	+100°C

**Note!**

- <sup>[1]</sup> The greater the V<sub>CCLDO</sub> voltage, the higher the power consumption.
- If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.

## GW5A-60

Table 3-5 Recommended Operating Conditions(GW5A-60)

Name	Description	Min.	Max.
FPGA Logic			
V <sub>CC</sub>	Core voltage, LV	0.87V	1.03V
	Core voltage, EV	1.14V	1.8V
V <sub>CCIO</sub>	I/O Bank voltage	1V	3.465V
V <sub>CCX</sub> <sup>[1]</sup>	Auxiliary voltage	1.71V	3.465V
V <sub>EFUSE</sub> <sup>[2]</sup>	Voltage required for eFuse writing	1.62V	1.98V
MIPI			
V <sub>DDAM</sub>	Analog core power supply	0.87V	1.08V
V <sub>DDXM</sub>	Analog auxiliary power supply	1.71V	3.465V
V <sub>DDDM</sub>	Digital core power supply	0.87V	1.08V
V <sub>DD12M</sub>	MIPI LP power supply	1.14V	1.32V
ADC			
V <sub>CCLDOADC</sub>	The supply voltage for the internal LDO module that powers the ADC	1.71V	1.89V
V <sub>CCADC</sub>	ADC power supply	1.62V	1.98V
V <sub>REFN</sub>	ADC Module reference voltage	0V	0V
V <sub>REFP</sub>	ADC Module reference voltage	0V	1.25V
Temperature			
T <sub>JCOM</sub>	Junction temperature Commercial operation	0°C	+85°C
T <sub>JIND</sub>	Junction temperature Industrial operation	-40°C	+100°C

**Note!**

- <sup>[1]</sup> When internal differential termination resistors are required, V<sub>ccx</sub> must be greater than or equal to 3V; the IO input-output F<sub>max</sub> is limited when V<sub>ccx</sub>=1.8V, and V<sub>ccx</sub> needs to be greater than or equal to 2.5V for input-output applications with F<sub>max</sub> greater than 600Mbps.
- <sup>[2]</sup> When eFuse is not required, this power supply can be either connected to GND or floating.
- If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.

## GW5A-25

Table 3-6 Recommended Operating Conditions(GW5A-25)

Name	Description	Min.	Max.
V <sub>CC</sub>	Core voltage, LV	0.87V	1.03V

Name	Description	Min.	Max.
V <sub>CC</sub>	Core voltage, EV	1.14V	1.8V
V <sub>CCIO</sub>	I/O Bank voltage	1.14V	3.465V
V <sub>CCX</sub>	Auxiliary voltage	2.375V	3.465V
V <sub>CCLDO</sub> <sup>[1]</sup>	Voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V <sub>EFUSE</sub> <sup>[2]</sup>	Voltage required for eFuse writing	1.62V	1.98V
V <sub>DDAM</sub>	Analog core power supply	0.87V	1V
V <sub>DDDM</sub>	Digital core power supply	0.87V	1V
V <sub>DDXM</sub>	Analog auxiliary voltage power supply	2.375V	3.465V
V <sub>DD12M</sub>	MIPI LP power supply	1.14V	1.32V
T <sub>JCOM</sub>	Junction temperature Commercial operation	0°C	+85°C
T <sub>JIND</sub>	Junction temperature Industrial operation	-40°C	+100°C

**Note!**

- <sup>[1]</sup> The greater the V<sub>CCLDO</sub> voltage, the higher the power consumption.
- <sup>[2]</sup> When eFuse is not required, this power supply can be either connected to GND or floating.
- If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.

### 3.1.3 Power Supply Ramp Rates

Table 3-7 Power Supply Ramp Rates

Name	Min.	Typ.	Max.
V <sub>CC</sub> Ramp Rate	0.1mV/μs	TBD	15mV/μs
V <sub>CCLDO</sub> Ramp Rate	0.09mV/μs	TBD	15mV/μs
V <sub>CCX</sub> Ramp Rate	0.005mV/μs	TBD	15mV/μs
V <sub>CCIO</sub> Ramp Rate	0.06mV/μs	TBD	15mV/μs

### 3.1.4 Hot Socket Specifications

Table 3-8 Hot Socket Specifications

Name	Description	Condition	I/O	Max.
I <sub>HS</sub>	Input or I/O leakage current	V <sub>IN</sub> =V <sub>IL</sub> (MAX)	I/O	150uA
I <sub>HS</sub>	Input or I/O leakage current	V <sub>IN</sub> =V <sub>IL</sub> (MAX)	TDI, TDO, TMS, TCK	120uA

### 3.1.5 POR Specifications

GW5A-138

Table 3-9 POR Voltage (GW5A-138)

Name	Description	Name	Typ.
POR Voltage	Power on reset voltage	$V_{CC}$	0.72V
		$V_{CCX}$	1.5V
		$V_{CCIO}$ (Bank10)	1.04V
		$V_{CCLDO}$	1.03V

GW5A-60

Table 3-10 POR Voltage (GW5A-60)

Name	Description	Name	Typ.
POR Voltage	Power on reset voltage	$V_{CC}$	0.69V
		$V_{CCX}$	1.5V
		$V_{CCIO}$ (Bank3/5/12)	1.05V

GW5A-25

Table 3-11 POR Voltage(GW5A-25)

Name	Description	Name	Typ.
POR Voltage	Power on reset voltage	$V_{CC}$	0.69V
		$V_{CCX}$	1.5V
		$V_{CCIO}$ (Bank4/5/7)	1.05V
		$V_{CCLDO}$	0.92V

## 3.2 ESD performance

Table 3-12 ESD - HBM

Device	HBM
GW5A-25	HBM $\geq$ 2000V (GPIO) HBM $\geq$ 1000V (MIPI D-PHY)
GW5A-60	HBM $\geq$ 2000V (GPIO) HBM $\geq$ 1000V (MIPI C-PHY, MIPI D-PHY)
GW5A-138	HBM $\geq$ 2000V (GPIO) HBM $\geq$ 1000V (MIPI D-PHY)

**Table 3-13 ESD- CDM**

Device	CDM
GW5A-25	CDM $\geq$ 500V
GW5A-60	CDM $\geq$ 500V
GW5A-138	CDM $\geq$ 250V

## 3.3 DC Characteristics

### 3.3.1 DC Electrical Characteristics-Recommended Operating Conditions

GW5A-138

Table 3-14 DC Electrical Characteristics-Recommended Operating Conditions(GW5A-138)

Name	Description	Condition	Min.	Typ.	Max.
$I_{IL}, I_{IH}$	Input or I/O leakage	$V_{CCIO} < V_{IN} < V_{IH}(MAX)$	-	-	210uA
		$0V < V_{IN} < V_{CCIO}$	-	-	10uA
$I_{PU}$	I/O Active Pull-up Current	$0 < V_{IN} < 0.7V_{CCIO}$ , Pull Strength=Strong	-	-	-400uA
		$0 < V_{IN} < 0.7V_{CCIO}$ , Pull Strength=Medium	-	-	-150uA
		$0 < V_{IN} < 0.7V_{CCIO}$ , Pull Strength=Weak	-	-	-50uA
$I_{PD}$	I/O Active Pull-down Current	$V_{IL}(MAX) < V_{IN} < V_{CCIO}$ , Pull Strength=Strong	-	-	400uA
		$V_{IL}(MAX) < V_{IN} < V_{CCIO}$ , Pull Strength=Medium	-	-	150uA
		$V_{IL}(MAX) < V_{IN} < V_{CCIO}$ , Pull Strength=Weak	-	-	50uA
C1	I/O Capacitance	-	-	5pF	8pF
$R_{ODT}^{[1]}$	Resistance of input differential On-Die Termination	$V_{CCX}=3.3V$	-	100Ω	-
$V_{HYST}$	Hysteresis for Schmitt Trigger inputs	$V_{CCIO}=3.3V$ , Hysteresis=ON	-	400mV	
		$V_{CCIO}=2.5V$ , Hysteresis=ON	-	200mV	
		$V_{CCIO}=1.8V$ , Hysteresis=ON	-	100mV	
		$V_{CCIO}=1.5V$ , Hysteresis=ON	-	70mV	
		$V_{CCIO}=1.2V$ , Hysteresis=ON		40mV	

#### Note!

[1]The Top bank and Bottom bank of 138K devices support  $R_{ODT}$ .

## GW5A-60

Table 3-15 DC Electrical Characteristics - Recommended Operating Conditions (GW5A-60)

Name	Description	Condition	Min.	Typ.	Max.
$I_{IL}, I_{IH}$	Input or I/O leakage	$V_{CCIO} < V_{IN} < V_{IH}(MAX)$	-		210uA
		$0V < V_{IN} < V_{CCIO}$	-		10uA
$I_{PU}$	I/O Active Pull-up Current	$0 < V_{IN} < 0.7V_{CCIO}$ , Pull Strength=Strong	-		-400uA
		$0 < V_{IN} < 0.7V_{CCIO}$ , Pull Strength=Medium			-150uA
		$0 < V_{IN} < 0.7V_{CCIO}$ , Pull Strength=Weak			-50uA
$I_{PD}$	I/O Active Pull-down Current	$V_{IL}(MAX) < V_{IN} < V_{CCIO}$ , Pull Strength=Strong	-		400uA
		$V_{IL}(MAX) < V_{IN} < V_{CCIO}$ , Pull Strength=Medium			150uA
		$V_{IL}(MAX) < V_{IN} < V_{CCIO}$ , Pull Strength=Weak			50uA
C1	I/O Capacitance			5pF	8pF
$R_{ODT}^{[1]}$	Resistance of input differential On-Die Termination	$V_{CCX}=3.3V$	-	100Ω	-
$V_{HYST}$	Hysteresis for Schmitt Trigger inputs	$V_{CCIO}=3.3V$ , Hysteresis=ON	-	400mV	
		$V_{CCIO}=2.5V$ , Hysteresis=ON	-	250mV	
		$V_{CCIO}=1.8V$ , Hysteresis=ON	-	150mV	
		$V_{CCIO}=1.5V$ , Hysteresis=ON	-	130mV	
		$V_{CCIO}=1.2V$ , Hysteresis=ON		40mV	

## GW5A-25

Table 3-16 DC Electrical Characteristics - Recommended Operating Conditions (GW5A-25)

Name	Description	Condition	Min.	Typ.	Max.
$I_{IL}, I_{IH}$	Input or I/O leakage	$V_{CCIO} < V_{IN} < V_{IH}(MAX)$	-		210uA
		$0V < V_{IN} < V_{CCIO}$	-		10uA
$I_{PU}$	I/O Active Pull-up Current	$0 < V_{IN} < 0.7V_{CCIO}$ , Pull Strength=Strong	-		-400uA

Name	Description	Condition	Min.	Typ.	Max.
$I_{PU}$	I/O Active Pull-up Current	$0 < V_{IN} < 0.7V_{CCIO}$ , Pull Strength=Medium			-150uA
		$0 < V_{IN} < 0.7V_{CCIO}$ , Pull Strength=Weak			-50uA
$I_{PD}$	I/O Active Pull-down Current	$V_{IL}(MAX) < V_{IN} < V_{CCIO}$ , Pull Strength=Strong	-		400uA
		$V_{IL}(MAX) < V_{IN} < V_{CCIO}$ , Pull Strength=Medium			150uA
		$V_{IL}(MAX) < V_{IN} < V_{CCIO}$ , Pull Strength=Weak			50uA
C1	I/O Capacitance			5pF	8pF
$R_{ODT}^{[1]}$	Resistance of input differential On-Die Termination	$V_{CCX}=3.3V$	-	100Ω	-
$V_{HYST}$	Hysteresis for Schmitt Trigger inputs	$V_{CCIO}=3.3V$ , Hysteresis=ON	-	400mV	
		$V_{CCIO}=2.5V$ , Hysteresis=ON	-	250mV	
		$V_{CCIO}=1.8V$ , Hysteresis=ON	-	150mV	
		$V_{CCIO}=1.5V$ , Hysteresis=ON	-	130mV	
		$V_{CCO}=1.2V$ , Hysteresis=ON		40mV	

**Note!**

<sup>[1]</sup>The Top bank and Bottom bank of 25K devices support  $R_{ODT}$ .

### 3.3.2 Static Current

GW5A-138

Table 3-17 Static Current (GW5A-138)

Name	Description	LV/UV	Typ. <sup>[1]</sup>
$I_{CC}$	Core current	LV	100 mA
$I_{CCX}$	$V_{CCX}$ current	LV	9 mA
$I_{CCIO}$	I/O Bank current ( $V_{CCIO}=2.5V$ )	LV	5 mA
$I_{CC\_LDO}$	Static current (Built-in Regulator)	LV	6 mA

**Note!**

<sup>[1]</sup> The test condition for the typical value is 25°C.

## GW5A-60

Table 3-18 Static Current (GW5A-60)

Name	Description	LV/UV	Typ. <sup>[1]</sup>
$I_{CC}$	Core current	LV	80 mA
$I_{CCX}$	$V_{CCX}$ current	LV	5 mA
$I_{CCIO}$	I/O Bank current ( $V_{CCIO}=2.5V$ )	LV	1 mA

**Note!**

<sup>[1]</sup> The test condition for the typical value is 25°C.

## GW5A-25

Table 3-19 Static Current (GW5A-25)

Name	Description	LV/UV	Typ. <sup>[1]</sup>
$I_{CC}$	Core current	LV	30mA
$I_{CCX}$	$V_{CCX}$ current	LV	2mA
$I_{CCIO}$	I/O Bank current ( $V_{CCIO}=2.5V$ )	LV	1mA
$I_{CC\_LDO}$	Static current (Built-in Regulator)	LV	4mA

**Note!**

<sup>[1]</sup> The test condition for the typical value is 25°C.

### 3.3.3 Recommended I/O Operating Conditions

Table 3-20 Recommended I/O Operating Conditions

Name	Output $V_{CCIO}$ (V)			Input $V_{REF}$ (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVTTTL33	3.135	3.3	3.465	-	-	-
LVC MOS33	3.135	3.3	3.465	-	-	-
LVC MOS25	2.375	2.5	2.625	-	-	-
LVC MOS18	1.71	1.8	1.89	-	-	-
LVC MOS15	1.425	1.5	1.575	-	-	-
LVC MOS12	1.14	1.2	1.26	-	-	-
SSTL15	1.425	1.5	1.575	0.68	0.75	0.9
SSTL18_I	1.71	1.8	1.89	0.833	0.9	0.969
SSTL18_II	1.71	1.8	1.89	0.833	0.9	0.969
SSTL25_I	2.375	2.5	2.645	1.15	1.25	1.35
SSTL25_II	2.375	2.5	2.645	1.15	1.25	1.35

Name	Output $V_{CCIO}$ (V)			Input $V_{REF}$ (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
SSTL33_I	3.135	3.3	3.465	1.3	1.5	1.7
SSTL33_II	3.135	3.3	3.465	1.3	1.5	1.7
HSTL18_I	1.71	1.8	1.89	0.816	0.9	1.08
HSTL18_II	1.71	1.8	1.89	0.816	0.9	1.08
HSTL15	1.425	1.5	1.575	0.68	0.75	0.9
PCI33	3.135	3.3	3.465	-	-	-
LVPECL33E	3.135	3.3	3.465	-	-	-
MLVDS25E	2.375	2.5	2.625	-	-	-
BLVDS25E	2.375	2.5	2.625	-	-	-
RSDS25E	2.375	2.5	2.625	-	-	-
LVDS25E <sup>1</sup>	2.375	2.5	2.625	-	-	-
SSTL15D	1.425	1.5	1.575	-	-	-
SSTL18D_I	1.71	1.8	1.89	-	-	-
SSTL18D_II	1.71	1.8	1.89	-	-	-
SSTL25D_I	2.375	2.5	2.625	-	-	-
SSTL25D_II	2.375	2.5	2.625	-	-	-
SSTL33D_I	3.135	3.3	3.465	-	-	-
SSTL33D_II	3.135	3.3	3.465	-	-	-
HSTL15D	1.425	1.575	1.89	-	-	-
HSTL18D_I	1.71	1.8	1.89	-	-	-
HSTL18D_II	1.71	1.8	1.89	-	-	-

**Note!**

$V_{CCIO}$  of Banks with True LVDS is recommended to be set to 2.5 V.

### 3.3.4 Single ended I/O DC Characteristic

GW5A-138

Table 3-21 Single-ended I/O DC Characteristics (GW5A-138)

Name	$V_{IL}$		$V_{IH}$		$V_{OL}$ (Max)	$V_{OH}$ (Min)	$I_{OL}$ [1] (mA)	$I_{OH}$ [1] (mA)
	Min	Max	Min	Max				
LVC MOS33 LV TTL33	-0.3V	0.8V	2.0V	$V_{CCIO}+0.3$	0.4V	$V_{CCIO}-0.4V$	4	-4
							8	-8
							12	-12

Name	$V_{IL}$		$V_{IH}$		$V_{OL}$ (Max)	$V_{OH}$ (Min)	$I_{OL}^{[1]}$ (mA)	$I_{OH}^{[1]}$ (mA)
	Min	Max	Min	Max				
LVCMOS33 LVTTTL33	-0.3V	0.8V	2.0V	$V_{CCIO}+0.3$	0.4V	$V_{CCIO}-0.4V$	16	-16
							24	-24
					0.2V	$V_{CCIO}-0.2V$	0.1	-0.1
LVCMOS25	-0.3V	0.7V	1.7V	$V_{CCIO}+0.3$	0.4V	$V_{CCIO}-0.4V$	4	-4
							8	-8
							12	-12
							16	-16
							24	-24
					0.2V	$V_{CCIO}-0.2V$	0.1	-0.1
LVCMOS18	-0.3V	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO}+0.3$	0.4V	$V_{CCIO}-0.4V$	4	-4
							8	-8
							12	-12
							16	-16
							24	-24
					0.2V	$V_{CCIO}-0.2V$	0.1	-0.1
LVCMOS15	-0.3V	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO}+0.3$	0.4V	$V_{CCIO}-0.4V$	4	-4
							8	-8
							12	-12
							16	-16
							24	-24
					0.2V	$V_{CCIO}-0.2V$	0.1	-0.1
LVCMOS12	-0.3V	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO}+0.3$	0.4V	$V_{CCIO}-0.4V$	4	-4
							8	-8
							12	-12
					0.2V	$V_{CCIO}-0.2V$	0.1	-0.1
LVCMOS10	-0.3V	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	1.1V	0.4V	$V_{CCIO}-0.4V$	1.5	-0.5
PCI33	-0.3V	$0.3 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$V_{CCIO}+0.3$	$0.1 \times V_{CCIO}$	$0.9 \times V_{CCIO}$	1.5	-0.5
SSTL18_II	-0.3V	$V_{REF}-0.125V$	$V_{REF}+0.125V$	$V_{CCIO}+0.3$	0.4V	$V_{CCIO}-0.4V$	13.4	-13.4
SSTL18_I	-0.3V	$V_{REF}-0.125V$	$V_{REF}+0.125V$	$V_{CCIO}+0.3$	0.40V	$V_{CCIO}-0.40V$	8	-8
SSTL15	-0.3V	$V_{REF}-0.1V$	$V_{REF}+0.1V$	$V_{CCIO}+0.3$	0.40V	$V_{CCIO}-0.40V$	13	-13
SSTL135	-0.3V	$V_{REF}-0.09V$	$V_{REF}+0.09V$	$V_{CCIO}+0.3$	0.40V	$V_{CCIO}-0.40V$	13	-13
HSTL18_I	-0.3V	$V_{REF}-0.1V$	$V_{REF}+0.1V$	$V_{CCIO}+0.3$	0.40V	$V_{CCIO}-0.40V$	8	-8

Name	V <sub>IL</sub>		V <sub>IH</sub>		V <sub>OL</sub> (Max)	V <sub>OH</sub> (Min)	I <sub>OL</sub> [1] (mA)	I <sub>OH</sub> [1] (mA)
	Min	Max	Min	Max				
HSTL18_II	-0.3V	V <sub>REF</sub> -0.1V	V <sub>REF</sub> + 0.1V	V <sub>CCIO</sub> +0.3	0.40V	V <sub>CCIO</sub> -0.40V	16	-16
HSTL15_I	-0.3V	V <sub>REF</sub> -0.1V	V <sub>REF</sub> + 0.1V	V <sub>CCIO</sub> +0.3	0.40V	V <sub>CCIO</sub> -0.40V	8	-8
HSTL15_II	-0.3V	V <sub>REF</sub> -0.1V	V <sub>REF</sub> + 0.1V	V <sub>CCIO</sub> +0.3	0.40V	V <sub>CCIO</sub> -0.40V	16	-16
HSUL12	-0.3V	V <sub>REF</sub> -0.13V	V <sub>REF</sub> + 0.13V	V <sub>CCIO</sub> +0.3	0.40	V <sub>CCIO</sub> -0.40V	0.1	-0.1

**Note!**

[1] The total DC current limit(sourced and sinked) of all IOs in the same bank: the total DC current of all IOs in the same bank shall not be greater than n\*8mA, where n represents the number of IOs bonded out from a bank.

GW5A-60

**Table 3-22 Single-ended I/O DC Characteristics (GW5A-60)**

Name	V <sub>IL</sub>		V <sub>IH</sub>		V <sub>OL</sub> (Max)	V <sub>OH</sub> (Min)	I <sub>OL</sub> [1] (mA)	I <sub>OH</sub> [1] (mA)
	Min	Max	Min	Max				
LVCMOS33 LVTTTL33	-0.3V	0.8V	2.0V	3.45V	0.4V	V <sub>CCIO</sub> -0.4V	2	-2
							4	-4
							6	-6
							8	-8
							12	-12
					16	-16		
					0.2V	V <sub>CCIO</sub> -0.2V	0.1	-0.1
LVCMOS25	-0.3V	0.7V	1.7V	V <sub>CCIO</sub> +0.3	0.4V	V <sub>CCIO</sub> -0.4V	2	-2
							4	-4
							6	-6
							8	-8
							12	-12
					16	-16		
					0.2V	V <sub>CCIO</sub> -0.2V	0.1	-0.1
LVCMOS18	-0.3V	0.35 x V <sub>CCIO</sub>	0.65 x V <sub>CCIO</sub>	V <sub>CCIO</sub> +0.3	0.4V	V <sub>CCIO</sub> -0.4V	2	-2
							4	-4
							6	-6
							8	-8
							12	-12

Name	V <sub>IL</sub>		V <sub>IH</sub>		V <sub>OL</sub> (Max)	V <sub>OH</sub> (Min)	I <sub>OL</sub> [1] (mA)	I <sub>OH</sub> [1] (mA)
	Min	Max	Min	Max				
LVCMOS18	-0.3V	0.35 x V <sub>CCIO</sub>	0.65 x V <sub>CCIO</sub>	V <sub>CCIO</sub> +0.3	0.4V	V <sub>CCIO</sub> -0.4V	16	-16
					0.2V	V <sub>CCIO</sub> -0.2V	0.1	-0.1
LVCMOS15	-0.3V	0.35 x V <sub>CCIO</sub>	0.65 x V <sub>CCIO</sub>	V <sub>CCIO</sub> +0.3	0.4V	V <sub>CCIO</sub> -0.4V	2	-2
							4	-4
							6	-6
							8	-8
					12	-12		
					0.2V	V <sub>CCIO</sub> -0.2V	0.1	-0.1
LVCMOS12	-0.3V	0.35 x V <sub>CCIO</sub>	0.65 x V <sub>CCIO</sub>	V <sub>CCIO</sub> +0.3	0.4V	V <sub>CCIO</sub> -0.4V	2	-2
							4	-4
							6	-6
							8	-8
					0.2V	V <sub>CCIO</sub> -0.2V	0.1	-0.1
					LVCMOS10	-0.3	0.35 x V <sub>CCIO</sub>	0.65 x V <sub>CCIO</sub>
4	-4							
PCI33	-0.3V	0.3 x V <sub>CCO</sub>	0.5 x V <sub>CCO</sub>	V <sub>CCO</sub> +0.3	0.1x V <sub>CCO</sub>	0.9 x V <sub>CCO</sub>	1.5	-0.5
SSTL33_I	-0.3V	V <sub>REF</sub> -0.2V	V <sub>REF</sub> +0.2V	V <sub>CCO</sub> +0.3	V <sub>CCO</sub> /2-0.6	V <sub>CCO</sub> /2+0.6	8	-8
SSTL33_II	-0.3V	V <sub>REF</sub> -0.2V	V <sub>REF</sub> +0.2V	V <sub>CCO</sub> +0.3	V <sub>CCO</sub> /2-0.8	V <sub>CCO</sub> /2+0.8	13.4	-13.4
SSTL25_I	-0.3V	V <sub>REF</sub> -0.15V	V <sub>REF</sub> +0.15V	V <sub>CCO</sub> +0.3	V <sub>CCO</sub> /2-0.61	V <sub>CCO</sub> /2+0.61	8	-8
SSTL25_II	-0.3V	V <sub>REF</sub> -0.15V	V <sub>REF</sub> +0.15V	V <sub>CCO</sub> +0.3	V <sub>CCO</sub> /2-0.81	V <sub>CCO</sub> /2+0.81	13.4	-13.4
SSTL18_I	-0.3V	V <sub>REF</sub> -0.125V	V <sub>REF</sub> +0.125V	V <sub>CCO</sub> +0.3	V <sub>CCO</sub> /2-0.47	V <sub>CCO</sub> /2+0.47	8	-8
SSTL18_II	-0.3V	V <sub>REF</sub> -0.125V	V <sub>REF</sub> +0.125V	V <sub>CCO</sub> +0.3	V <sub>CCO</sub> /2-0.6	V <sub>CCO</sub> /2+0.6	13.4	-13.4
SSTL15_I	-0.3V	V <sub>REF</sub> -0.1V	V <sub>REF</sub> +0.1V	V <sub>CCO</sub> +0.3	V <sub>CCO</sub> /2-0.175	V <sub>CCO</sub> /2+0.175	8	-8
SSTL135_I	-0.3	V <sub>REF</sub> -0.09V	V <sub>REF</sub> +0.09V	V <sub>CCO</sub> +0.3	V <sub>CCO</sub> /2-0.15	V <sub>CCO</sub> /2+0.15	8	-8
SSTL12_I	-0.3	V <sub>REF</sub> -0.1V	V <sub>REF</sub> +0.1V	V <sub>CCO</sub> +0.3	0.2 x V <sub>CCO</sub>	0.8 x V <sub>CCO</sub>	0.1	-0.1
HSTL18_I	-0.3V	V <sub>REF</sub> -0.1V	V <sub>REF</sub> +0.1V	V <sub>CCO</sub> +0.3	0.40V	V <sub>CCO</sub> -0.40V	8	-8
HSTL18_II	-0.3V	V <sub>REF</sub> -0.1V	V <sub>REF</sub> +0.1V	V <sub>CCO</sub> +0.3	0.40V	V <sub>CCO</sub> -0.40V	16	-16
HSTL15_I	-0.3V	V <sub>REF</sub> -0.1V	V <sub>REF</sub> +0.1V	V <sub>CCO</sub> +0.3	0.40V	V <sub>CCO</sub> -0.40V	8	-8
HSTL15_II	-0.3V	V <sub>REF</sub> -0.1V	V <sub>REF</sub> +0.1V	V <sub>CCO</sub> +0.3	0.40V	V <sub>CCO</sub> -0.40V	8	-8
HSTL12_I	-0.3V	V <sub>REF</sub> -0.1V	V <sub>REF</sub> +0.1V	V <sub>CCO</sub> +0.3	0.2 x V <sub>CCO</sub>	0.8 x V <sub>CCO</sub>	8	-8
HSUL12	-0.3	V <sub>REF</sub> -0.13V	V <sub>REF</sub> +0.13V	V <sub>CCO</sub> +0.3	0.2 x V <sub>CCO</sub>	0.8 x V <sub>CCO</sub>	0.1	-0.1

**Note!**

[1] The total DC current limit(sourced and sinked) of all IOs in the same bank: the total DC current of all IOs in the same bank shall not be greater than  $n \times 8\text{mA}$ , where  $n$  represents the number of IOs bonded out from a bank.

GW5A-25

**Table 3-23 Single-ended I/O DC Characteristics (GW5A-25)**

Name	$V_{IL}$		$V_{IH}$		$V_{OL}$ (Max)	$V_{OH}$ (Min)	$I_{OL}^{[1]}$ (mA)	$I_{OH}^{[1]}$ (mA)
	Min	Max	Min	Max				
LVCMOS33 LVTTTL33	-0.3V	0.8V	2.0V	3.45V	0.4V	$V_{CCIO}-0.4V$	2	-2
							4	-4
							6	-6
							8	-8
							12	-12
					16	-16		
					0.2V	$V_{CCIO}-0.2V$	0.1	-0.1
LVCMOS25	-0.3V	0.7V	1.7V	$V_{CCIO}+0.3$	0.4V	$V_{CCIO}-0.4V$	2	-2
							4	-4
							6	-6
							8	-8
							12	-12
					16	-16		
					0.2V	$V_{CCIO}-0.2V$	0.1	-0.1
LVCMOS18	-0.3V	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO}+0.3$	0.4V	$V_{CCIO}-0.4V$	2	-2
							4	-4
							6	-6
							8	-8
							12	-12
					16	-16		
					0.2V	$V_{CCIO}-0.2V$	0.1	-0.1
LVCMOS15	-0.3V	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO}+0.3$	0.4V	$V_{CCIO}-0.4V$	2	-2
							4	-4
							6	-6
							8	-8
							12	-12

Name	V <sub>IL</sub>		V <sub>IH</sub>		V <sub>OL</sub> (Max)	V <sub>OH</sub> (Min)	I <sub>OL</sub> [1] (mA)	I <sub>OH</sub> [1] (mA)
	Min	Max	Min	Max				
LVC MOS15	-0.3V	0.35 x V <sub>CCIO</sub>	0.65 x V <sub>CCIO</sub>	V <sub>CCIO</sub> +0.3	0.2V	V <sub>CCIO</sub> -0.2V	0.1	-0.1
LVC MOS12	-0.3V	0.35 x V <sub>CCIO</sub>	0.65 x V <sub>CCIO</sub>	V <sub>CCIO</sub> +0.3	0.4V	V <sub>CCIO</sub> -0.4V	2	-2
							4	-4
							6	-6
					8	-8		
					0.2V	V <sub>CCIO</sub> -0.2V	0.1	-0.1
LVC MOS10	-0.3	0.35 x V <sub>CCIO</sub>	0.65 x V <sub>CCIO</sub>	1.1V	0.4V	V <sub>CCIO</sub> -0.4V	2	-2
							4	-4
PCI33	-0.3V	0.3 x V <sub>CCO</sub>	0.5 x V <sub>CCO</sub>	V <sub>CCO</sub> +0.3	0.1x V <sub>CCO</sub>	0.9 x V <sub>CCO</sub>	1.5	-0.5
SSTL33_I	-0.3V	V <sub>REF</sub> -0.2V	V <sub>REF</sub> +0.2V	V <sub>CCO</sub> +0.3	V <sub>CCO</sub> /2-0.6	V <sub>CCO</sub> /2+0.6	8	-8
SSTL33_II	-0.3V	V <sub>REF</sub> -0.2V	V <sub>REF</sub> +0.2V	V <sub>CCO</sub> +0.3	V <sub>CCO</sub> /2-0.8	V <sub>CCO</sub> /2+0.8	13.4	-13.4
SSTL25_I	-0.3V	V <sub>REF</sub> -0.15V	V <sub>REF</sub> +0.15V	V <sub>CCO</sub> +0.3	V <sub>CCO</sub> /2-0.61	V <sub>CCO</sub> /2+0.61	8	-8
SSTL25_II	-0.3V	V <sub>REF</sub> -0.15V	V <sub>REF</sub> +0.15V	V <sub>CCO</sub> +0.3	V <sub>CCO</sub> /2-0.81	V <sub>CCO</sub> /2+0.81	13.4	-13.4
SSTL18_I	-0.3V	V <sub>REF</sub> -0.125V	V <sub>REF</sub> +0.125V	V <sub>CCO</sub> +0.3	V <sub>CCO</sub> /2-0.47	V <sub>CCO</sub> /2+0.47	8	-8
SSTL18_II	-0.3V	V <sub>REF</sub> -0.125V	V <sub>REF</sub> +0.125V	V <sub>CCO</sub> +0.3	V <sub>CCO</sub> /2-0.6	V <sub>CCO</sub> /2+0.6	13.4	-13.4
SSTL15_I	-0.3V	V <sub>REF</sub> -0.1V	V <sub>REF</sub> + 0.1V	V <sub>CCO</sub> +0.3	V <sub>CCO</sub> /2-0.175	V <sub>CCO</sub> /2+0.175	8	-8
SSTL135_I	-0.3	V <sub>REF</sub> -0.09V	V <sub>REF</sub> +0.09V	V <sub>CCO</sub> +0.3	V <sub>CCO</sub> /2-0.15	V <sub>CCO</sub> /2+0.15	8	-8
SSTL12_I	-0.3	V <sub>REF</sub> -0.1V	V <sub>REF</sub> +0.1V	V <sub>CCO</sub> +0.3	0.2 x V <sub>CCO</sub>	0.8 x V <sub>CCO</sub>	0.1	-0.1
HSTL18_I	-0.3V	V <sub>REF</sub> -0.1V	V <sub>REF</sub> + 0.1V	V <sub>CCO</sub> +0.3	0.40V	V <sub>CCO</sub> -0.40V	8	-8
HSTL18_II	-0.3V	V <sub>REF</sub> -0.1V	V <sub>REF</sub> + 0.1V	V <sub>CCO</sub> +0.3	0.40V	V <sub>CCO</sub> -0.40V	16	-16
HSTL15_I	-0.3V	V <sub>REF</sub> -0.1V	V <sub>REF</sub> + 0.1V	V <sub>CCO</sub> +0.3	0.40V	V <sub>CCO</sub> -0.40V	8	-8
HSTL15_II	-0.3V	V <sub>REF</sub> -0.1V	V <sub>REF</sub> + 0.1V	V <sub>CCO</sub> +0.3	0.40V	V <sub>CCO</sub> -0.40V	8	-8
HSTL12_I	-0.3V	V <sub>REF</sub> -0.1V	V <sub>REF</sub> + 0.1V	V <sub>CCO</sub> +0.3	0.2 x V <sub>CCO</sub>	0.8 x V <sub>CCO</sub>	8	-8
HSUL12	-0.3	V <sub>REF</sub> -0.13V	V <sub>REF</sub> + 0.13V	V <sub>CCO</sub> +0.3	0.2 x V <sub>CCO</sub>	0.8 x V <sub>CCO</sub>	0.1	-0.1

**Note!**

[1] The total DC current limit(sourced and sinked) of all IOs in the same bank: the total DC current of all IOs in the same bank shall not be greater than n\*8mA, where n represents the number of IOs bonded out from a bank.

**3.3.5 Differential I/O DC Characteristic**

## GW5A-138

Table 3-24 Differential I/O DC Characteristics (GW5A-138)

Name	Description	Conditions	Min.	Typ.	Max.	Unit
$V_{ICM}$	Input Common Mode Voltage	Half the Sum of the Two Inputs	0.05		1.8	V
$V_{ID}$	Differential Input Threshold	Difference Between the Two Inputs	$\pm 100$	$\pm 350$	$\pm 600$	mV
$I_{IN}$	Input Current	Power On or Power Off			20	$\mu A$
$V_{OD}$	Output Voltage Differential	$(V_{OP} - V_{OM}), R_T = 100\Omega$	250	350	600	mV
$\Delta V_{OD}$	Change in VOD Between High and Low				50	mV
$V_{OS}$	Output Voltage Offset	$(V_{OP} + V_{OM})/2, R_T = 100\Omega$	1.000	1.250	1.425	V
$\Delta V_{OS}$	Change in VOS Between High and Low				50	mV
$I_S$	Short-circuit current	$V_{OD} = 0V$ output short-circuit			12	mA

## GW5A-60

Table 3-25 Differential I/O DC Characteristics (GW5A-60)

Name	Description	Conditions	Min.	Typ.	Max.	Unit
$V_{ICM}$	Input Common Mode Voltage	Half the Sum of the Two Inputs	0.3		2.35	V
$V_{ID}$	Differential Input Threshold	Difference Between the Two Inputs	$\pm 100$	$\pm 350$	$\pm 600$	mV
$I_{IN}$	Input Current	Power On or Power Off	–	–	20	$\mu A$
$V_{OD}$	Output Voltage Differential	$(V_{OP} - V_{OM}), R_T = 100\Omega$	250	350	600	mV
$\Delta V_{OD}$	Change in VOD Between High and Low		–	–	50	mV
$V_{OS}$	Output Voltage Offset	$(V_{OP} + V_{OM})/2, R_T = 100\Omega$	1.125	1.25	1.375	V
$\Delta V_{OS}$	Change in VOS Between High and Low		–	–	50	mV
$I_S$	Short-circuit current	$V_{OD} = 0V$ output short-circuit	–	–	12	mA

GW5A-25

Table 3-26 Differential I/O DC Characteristics (GW5A-25)

Name	Description	Conditions	Min.	Typ.	Max.	Unit
$V_{ICM}$	Input Common Mode Voltage	Half the Sum of the Two Inputs	0.3		2.35	V
$V_{ID}$	Differential Input Threshold	Difference Between the Two Inputs	$\pm 100$	$\pm 350$	$\pm 600$	mV
$I_{IN}$	Input Current	Power On or Power Off	–	–	20	$\mu A$
$V_{OD}$	Output Voltage Differential	$(V_{OP} - V_{OM})$ , $R_T = 100\Omega$	250	350	600	mV
$\Delta V_{OD}$	Change in VOD Between High and Low		–	–	50	mV
$V_{OS}$	Output Voltage Offset	$(V_{OP} + V_{OM})/2$ , $R_T = 100\Omega$	1.125	1.25	1.375	V
$\Delta V_{OS}$	Change in VOS Between High and Low		–	–	50	mV
$I_S$	Short-circuit current	$V_{OD} = 0V$ output short-circuit	–	–	12	mA

## 3.4 AC Switching Characteristics

### 3.4.1 CFU Switching Characteristics

Table 3-27 CFU Timing Parameters

Name	Description	C2/I1		C1/I0		Unit
		Min	Max	Min	Max	
$t_{LUT4\_CFU}$	LUT4 delay	0.297	0.539	0.371	0.674	ns
$t_{SR\_CFU}$	Set/Reset to Register output	1.075	1.148	1.344	1.435	ns
$t_{CO\_CFU}$	Clock to Register output	0.200	0.230	0.250	0.288	ns

### 3.4.2 BSRAM Switching Characteristics

Table 3-28 BSRAM Timing Parameters

Name	Description	C2/I1		C1/I0		Unit
		Min	Max	Min	Max	
$t_{COAD\_BSRAM}$	Clock to read address / data output	1.1	1.47	1.375	1.838	ns
$t_{COOR\_BSRAM}$	Clock to Register output	0.23	0.326	0.288	0.408	ns

### 3.4.3 DSP Switching Characteristics

Table 3-29 DSP Timing Parameters

Name	Description	C2/I1		C1/I0		Unit
		Min	Max	Min	Max	
$t_{COIR\_DSP}$	Clock to output from input register	0.2	0.22	0.24	0.25	ns
$t_{COPR\_DSP}$	Clock to output from pipeline register	0.06	0.07	0.07	0.08	ns
$t_{COOR\_DSP}$	Clock to output from output register	0.03	0.04	0.04	0.04	ns

### 3.4.4 Gearbox Switching Characteristics

Table 3-30 Gearbox Timing Parameters (25K)

Name	Description	Max.	Unit
$FMAX_{IDDR}$	1:2 Gearbox maximum serial input rate	400	Mbps
$FMAX_{IDES4}$	1:4 Gearbox maximum serial input rate	800	Mbps
$FMAX_{IDESx}$	1:8/1:10 Gearbox maximum serial input rate	1600	Mbps
$FMAX_{IDES14}$	1:14 Gearbox maximum serial input rate	1600	Mbps
$FMAX_{IDES16}$	1:16 Gearbox maximum serial input rate	1600	Mbps

Name	Description	Max.	Unit
FMAX <sub>IDES32</sub>	1:32 Gearbox maximum serial input rate	1600	Mbps
FMAX <sub>ODDR</sub>	2:1 Gearbox maximum serial output rate	400	Mbps
FMAX <sub>OSER4</sub>	4:1 Gearbox maximum serial output rate	800	Mbps
FMAX <sub>OSERx</sub>	8:1/10:1 Gearbox maximum serial output rate	2000	Mbps
FMAX <sub>OSERx</sub>	8:1/10:1 Gearbox maximum serial output rate	2000	Mbps
FMAX <sub>OSER16</sub>	16:1 Gearbox maximum serial output rate	2000	Mbps

Table 3-31 Gearbox Timing Parameters (60K)

Name	Description	Max.	Unit
FMAX <sub>IDDR</sub>	1:2 Gearbox maximum serial input rate	400	Mbps
FMAX <sub>IDES4</sub>	1:4 Gearbox maximum serial input rate	800	Mbps
FMAX <sub>IDESx</sub>	1:8/1:10 Gearbox maximum serial input rate	1600	Mbps
FMAX <sub>IDES14</sub>	1:14 Gearbox maximum serial input rate	1600	Mbps
FMAX <sub>IDES16</sub>	1:16 Gearbox maximum serial input rate	1600	Mbps
FMAX <sub>IDES32</sub>	1:32 Gearbox maximum serial input rate	1600	Mbps
FMAX <sub>ODDR</sub>	2:1 Gearbox maximum serial output rate	400	Mbps
FMAX <sub>OSER4</sub>	4:1 Gearbox maximum serial output rate	800	Mbps
FMAX <sub>OSERx</sub>	8:1/10:1 Gearbox maximum serial output rate	2000	Mbps
FMAX <sub>OSERx</sub>	8:1/10:1 Gearbox maximum serial output rate	2000	Mbps
FMAX <sub>OSER16</sub>	16:1 Gearbox maximum serial output rate	2000	Mbps

Table 3-32 Gearbox Timing Parameters (138K)

Name	Description	Max.	Unit
FMAX <sub>IDDR</sub>	1:2 Gearbox maximum serial input rate	400	Mbps
FMAX <sub>IDES4</sub>	1:4 Gearbox maximum serial input rate	800	Mbps
FMAX <sub>IDESx</sub>	1:8/1:10 Gearbox maximum serial input rate	1500	Mbps
FMAX <sub>IDES14</sub>	1:14 Gearbox maximum serial input rate	1500	Mbps
FMAX <sub>IDES16</sub>	1:16 Gearbox maximum serial input rate	1500	Mbps
FMAX <sub>IDES32</sub>	1:32 Gearbox maximum serial input rate	1500	Mbps
FMAX <sub>ODDR</sub>	2:1 Gearbox maximum serial output rate	400	Mbps
FMAX <sub>OSER4</sub>	4:1 Gearbox maximum serial output rate	800	Mbps
FMAX <sub>OSERx</sub>	8:1/10:1 Gearbox maximum serial output rate	1600	Mbps

Name	Description	Max.	Unit
F <sub>MAX</sub> <sub>OSERx</sub>	8:1/10:1 Gearbox maximum serial output rate	1600	Mbps
F <sub>MAX</sub> <sub>OSER16</sub>	16:1 Gearbox maximum serial output rate	1600	Mbps

### 3.4.5 On chip Oscillator Switching Characteristics

Table 3-33 On chip Oscillator Switching Characteristics

Name	Description	Min.	Typ.	Max.
f <sub>MAX</sub>	Output Frequency (0°C to + 85°C)	199.5 MHz	210 MHz	220.5 MHz
	Output Frequency (-40°C to +100°C)	189 MHz	210 MHz	231 MHz
t <sub>DT</sub>	Output Clock Duty Cycle	-	50%	-

### 3.4.6 PLL Switching Characteristics

Table 3-34 PLL Switching Characteristics

Parameter	Description	Speed Grade		Unit	Note
		C2/I1	C1/I0		
F <sub>INMAX</sub>	Maximum Input Clock Frequency	800	800	MHz	
F <sub>INMIN</sub>	Minimum Input Clock Frequency	19	19	MHz	
F <sub>PFDMAX</sub>	Maximum Frequency at the Phase Frequency Detector	400	400	MHz	
F <sub>PFDMIN</sub>	Minimum Frequency at the Phase Frequency Detector	19	19	MHz	
F <sub>INJITTER</sub>	Maximum Input Clock Period Jitter	< 20% of clock input period or 1 ns Max			
F <sub>INDUTY</sub>	Minimum Allowable Input Duty Cycle: 19–49 MHz	25	25	%	
	Minimum Allowable Input Duty Cycle: 50–199 MHz	30	30	%	
	Minimum Allowable Input Duty Cycle: 200–399 MHz	35	35	%	
F <sub>VCOMIN</sub>	Minimum PLL VCO Frequency	800	800	MHz	
F <sub>VCOMAX</sub>	Maximum PLL VCO Frequency	1600	1600	MHz	
F <sub>BW</sub>	Low PLL Bandwidth at Typical	1	1	MHz	
	High PLL Bandwidth at Typical	4	4	MHz	
T <sub>STATPHAOFF-SET</sub>	Static Phase Offset of the PLL Outputs	+/- 50	+/-50	ps	
T <sub>JIT-TER_CCJ_HCLK</sub>	PLL Output cycle-cycle Jitter Thru HCLK≥100MHz	<300	<300	ps	[3]

Parameter	Description	Speed Grade		Unit	Note
		C2/I1	C1/I0		
T <sub>JIT-TER_CCJ_HCLK</sub>	PLL Output cycle-cycle Jitter Thru HCLK <100MHz	<30	<30	mUI	
	PLL Output cycle-cycle Jitter Thru PCLK ≥100MHz	<400	<400	ps	
	PLL Output cycle-cycle Jitter Thru PCLK <100MHz	<40	<40	mUI	
T <sub>JIT-TER_PJ_PCLK</sub>	PLL Output period Jitter Thru HCLK ≥100MHz	<300	<300	ps	
	PLL Output period Jitter Thru HCLK <100MHz	<30	<30	mUI	
	PLL Output period Jitter Thru PCLK ≥100MHz	<400	<400	ps	
	PLL Output period Jitter Thru PCLK <100MHz	<40	<40	mUI	
T <sub>OUTDUTY</sub>	PLL Output Clock Duty Cycle Precision	<50	<50	mUI	[1],[4]
T <sub>LOCKMAX</sub>	PLL Maximum Lock Time	1	1	ms	
F <sub>OUTMAX</sub>	PLL Maximum Output Frequency	800	800	MHz	
F <sub>OUTMIN</sub>	PLL Minimum Output Frequency	6.25	6.25	MHz	[2]
T <sub>EXTFDVAR</sub>	External Clock Feedback Variation	< 20% of clock input period or 1 ns Max			
RST <sub>MINPULSE</sub>	Minimum Reset Pulse Width	10	10	ns	

**Note!**

- [1] This test data is derived from integer frequency divider outputs.
- [2] In Cascade mode, multiple dividers can be serially connected to achieve a reduced output frequency.
- [3] The level of output jitter correlates with the input source; this dataset is based on a low-jitter crystal as the source.
- [4] The observed duty cycle on IOs is influenced by the Clock Tree.

## 3.5 MIPI D-PHY

### 3.5.1 MIPI D-PHY Input Timing and Levels

Table 3-35 High Speed(Differential) Input DC Specification

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
V <sub>CMRX</sub>	Common-mode Voltage in High Speed Mode	-	70	-	330	mV
V <sub>IDTH</sub>	Differential Input HIGH Threshold	0.08 Gbps ≅ Data-Rate ≅ 1.5 Gbps	70	-	-	mV
		1.5 Gbps ≅ Data-Rate ≅ 2.5 Gbps	40	-	-	mV

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
V <sub>IDTL</sub>	Differential Input LOW Threshold	0.08 Gbps $\cong$ Data-Rate $\cong$ 1.5 Gbps	-	-	-70	mV
		1.5 Gbps $\cong$ Data-Rate $\cong$ 2.5 Gbps	-	-	-40	mV
V <sub>IHHS</sub>	Input HIGH Voltage(for HS mode)	-	-	-	460	mV
V <sub>ILHS</sub>	Input LOW Voltage	-	-40	-	-	mV
V <sub>TERM-EN</sub>	Single-ended voltage for HS Termination Enable	-	-	-	450	mV
Z <sub>ID</sub>	Differential Input Impedance	-	80	100	120	$\Omega$

Table 3-36 High Speed(Differential) Input AC Specification

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
$\Delta$ V <sub>CMRX</sub> (HF)	Common-mode Interference(>450 MHz)	0.08 Gbps $\cong$ Data-Rate $\cong$ 1.5 Gbps	-	-	100	mV
		1.5 Gbps $\cong$ Data-Rate $\cong$ 2.5 Gbps	-	-	50	mV
$\Delta$ V <sub>CMRX</sub> (LF)	Common-mode Interference(50MHz~450 MHz)	0.08 Gbps $\cong$ Data-Rate $\cong$ 1.5 Gbps	-50	-	50	mV
		1.5 Gbps $\cong$ Data-Rate $\cong$ 2.5 Gbps	-25	-	25	mV
C <sub>CM</sub>	Common-mode Termination	-	-	-	60	pF

Table 3-37 Low Power(Single-Ended) Input DC Specifications

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
V <sub>IH</sub>	Low Power Mode Input HIGH Voltage	-	760	-	-	mV
V <sub>IL</sub>	Low Power Mode Input LOW Voltage	-	-	-	550	mV
V <sub>HYST</sub>	Low Power Mode Input Hysteresis	-	25	-	-	mV
I <sub>LEAK</sub>	Pin Leakage Current	-	-100	-	100	$\mu$ A

### 3.5.2 MIPI D-PHY Output Timing and Levels

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**Table 3-38 Low Power(Single-Ended) Output DC Specifications (GW5A-138)**

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
V <sub>OH</sub>	Low Power Mode Thevenin Output High Level Voltage	0.08 Gbps $\cong$ Data-Rate $\leq$ 1.5 Gbps	1.1	1.2	1.3	V
		DataRate > 1.5Gbps	0.95	-	1.3	mV
V <sub>OL</sub>	Low Power Mode Thevenin Output Low Level Voltage	-	-50	-	50	mV
Z <sub>OLP</sub>	Output Impedance in LP mode	-	110	-	-	$\Omega$

**Table 3-39 Low Power(Single-Ended) Output AC Specifications (GW5A-138)**

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
t <sub>R</sub>	15%~85% Rise Time	-	-	-	25	ns
t <sub>F</sub>	85%~15% Fall Time	-	-	-	25	ns
t <sub>REOT</sub>	HS-LP Mode Rise and Fall Time, 30%~85%	-	-	-	35	ns
C <sub>LOAD</sub>	Load Capacitance	-	0	-	70	pF

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**Table 3-40 Low Power(Single-Ended) Output DC Specifications (GW5A-60)**

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
V <sub>OH</sub>	Low Power Mode Thevenin Output High Level Voltage	0.08 Gbps $\cong$ Data-Rate $\leq$ 1.5 Gbps	1.1	1.2	1.3	V
		DataRate > 1.5Gbps	0.95	-	1.3	mV
V <sub>OL</sub>	Low Power Mode Thevenin Output Low Level Voltage	-	-50	-	50	mV
Z <sub>OLP</sub>	Output Impedance in LP mode	-	110	-	-	$\Omega$

**Table 3-41 Low Power(Single-Ended) Output AC Specifications (GW5A-60)**

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
t <sub>R</sub>	15%~85% Rise Time	-	-	-	25	ns
t <sub>F</sub>	85%~15% Fall Time	-	-	-	25	ns

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
$t_{REOT}$	HS-LP Mode Rise and Fall Time, 30%~85%	-	-	-	35	ns
$C_{LOAD}$	Load Capacitance	-	0	-	70	pF

Table 3-42 High Speed(Differential) Output DC Specifications (GW5A-60)

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
$V_{CMTX}$	Common-mode Voltage in High Speed Mode	-	150	200	250	mV
$ V_{CMTX(1,0)} $	$V_{CMTX}$ Mismatch Between Differential HIGH and LOW	-	-	-	5	mV
$ V_{OD} $	Differential Output Voltage	D-PHY-P — D-PHY-N	140	200	270	mV
$ \Delta V_{OD} $	VOD Mismatch Between Differential HIGH and LOW	-	-	-	14	mV
$V_{OHHS}$	Single-Ended Output HIGH Voltage	-	-	-	360	mV
$Z_{OS}$	Single-Ended Differential Output Impedance	-	40	50	62.5	$\Omega$
$\Delta Z_{OS}$	$Z_{OS}$ mismatch	-	-	-	10	%

Table 3-43 High Speed(Differential) Output AC Specifications (GW5A-60)

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
$\Delta V_{CMTX}(HF)$	Common-mode Variation(>450 MHz)	-	-	-	15	mVrms
$\Delta V_{CMTX}(LF)$	Common-mode Variation(50MHz~450 MHz)	-	-	-	25	mVrms
$t_{HS-PREPARE}$	Time Interval of The Final LP-00 State before enabling HS mode	-	40ns + 4*UI	-	85ns + 6*UI	ns
$t_{HS-PREPARE} + t_{HS-ZERO}$	The Minimum duration of driving the extended Data HS-0 prior to starting HS sync sequence	-	145ns + 10*UI	-	-	ns
$t_R$	20%~80% Rise Time	$0.08 \text{ Gbps} \leq \text{DataRate} \leq 1 \text{ Gbps}$	-	-	0.3	UI
		$1 \text{ Gbps} \leq \text{DataRate} \leq 1.5 \text{ Gbps}$	-	-	0.35	UI
		$\text{DataRate} \leq 1.5 \text{ Gbps}$	100	-	-	ps
		$1.5 \text{ Gbps} \leq \text{DataRate} \leq 2.5 \text{ Gbps}$	-	-	0.4	UI

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
$t_R$	20%~80% Rise Time	DataRate>1.5 Gbps	50	-	-	ps
$t_F$	20%~80% Fall Time	0.08 Gbps $\leq$ DataRate $\leq$ 1 Gbps	-	-	0.3	UI
		1 Gbps $\leq$ DataRate $\leq$ 1.5 Gbps	-	-	0.35	UI
		DataRate $\leq$ 1.5 Gbps	100	-	-	ps
		1.5 Gbps $\leq$ DataRate $\leq$ 2.5 Gbps	-	-	0.4	UI
		DataRate>1.5 Gbps	50	-	-	ps
$t_{HS-TRAIL}$	The Duration of The Inverted Final Differential State Following The Last Payload Data Bit	-	60ns + 4*UI	-	-	ns
$t_{EOT}$	Combination of $t_{HS-TRAIL}$ and $t_{REOT}$	-	-	-	105ns + 12*UI	ns

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Table 3-44 Low Power(Single-Ended) Output DC Specifications (GW5A-25)

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
$V_{OH}$	Low Power Mode Thevenin Output High Level Voltage	0.08 Gbps $\leq$ DataRate $\leq$ 1.5 Gbps	1.1	1.2	1.3	V
		DataRate > 1.5Gbps	0.95	-	1.3	mV
$V_{OL}$	Low Power Mode Thevenin Output Low Level Voltage	-	-50	-	50	mV
$Z_{OLP}$	Output Impedance in LP mode	-	110	-	-	$\Omega$

Table 3-45 Low Power(Single-Ended) Output AC Specifications (GW5A-25)

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
$t_R$	15%~85% Rise Time	-	-	-	25	ns
$t_F$	85%~15% Fall Time	-	-	-	25	ns
$t_{REOT}$	HS-LP Mode Rise and Fall Time, 30%~85%	-	-	-	35	ns
$C_{LOAD}$	Load Capacitance	-	0	-	70	pF

Table 3-46 High Speed(Differential) Output DC Specifications (GW5A-25)

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
$V_{CMTX}$	Common-mode Voltage in High Speed Mode	-	150	200	250	mV
$ V_{CMTX(1,0)} $	$V_{CMTX}$ Mismatch Between Differential HIGH and LOW	-	-	-	5	mV
$ V_{OD} $	Differential Output Voltage	D-PHY-P — D-PHY-N	140	200	270	mV
$ \Delta V_{OD} $	VOD Mismatch Between Differential HIGH and LOW			-	14	mV
$V_{OHHS}$	Single-Ended Output HIGH Voltage	-	-	-	360	mV
$Z_{OS}$	Single-Ended Differential Output Impedance	-	40	50	62.5	$\Omega$
$\Delta Z_{OS}$	$Z_{OS}$ mismatch	-	-	-	10	%

Table 3-47 High Speed(Differential) Output AC Specifications (GW5A-25)

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
$\Delta V_{CMTX}(HF)$	Common-mode Variation(>450 MHz)	-	-	-	15	mVrms
$\Delta V_{CMTX}(LF)$	Common-mode Variation(50MHz~450 MHz)	-	-	-	25	mVrms
$t_{HS-PREPARE}$	Time Interval of The Final LP-00 State before enabling HS mode	-	40ns + 4*UI	-	85ns + 6*UI	ns
$t_{HS-PREPARE} + t_{HS-ZERO}$	The Minimum duration of driving the extended Data HS-0 prior to starting HS sync sequence	-	145ns + 10*UI	-	-	ns
$t_R$	20%~80% Rise Time	0.08 Gbps $\leq$ DataRate $\leq$ 1 Gbps	-	-	0.3	UI
		1 Gbps $\leq$ DataRate $\leq$ 1.5 Gbps	-	-	0.35	UI
		DataRate $\leq$ 1.5 Gbps	100	-	-	ps
		1.5 Gbps $\leq$ DataRate $\leq$ 2.5 Gbps	-	-	0.4	UI
		DataRate > 1.5 Gbps	50	-	-	ps
$t_F$	20%~80% Fall Time	0.08 Gbps $\leq$ DataRate $\leq$ 1 Gbps	-	-	0.3	UI
		1 Gbps $\leq$ DataRate $\leq$ 1.5 Gbps	-	-	0.35	UI

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
$t_F$	20%~80% Fall Time	DataRate $\leq$ 1.5 Gbps	100	-	-	ps
		1.5 Gbps $\leq$ DataRate $\leq$ 2.5 Gbps	-	-	0.4	UI
		DataRate > 1.5 Gbps	50	-	-	ps
$t_{HS-TRAIL}$	The Duration of The Inverted Final Differential State Following The Last Payload Data Bit	-	60ns + 4*UI	-	-	ns
$t_{EOT}$	Combination of $t_{HS-TRAIL}$ and $t_{REOT}$	-	-	-	105ns + 12*UI	ns

### 3.5.3 MIPI D-PHY Switching Characteristics

Table 3-48 MIPI D-PHY RX Switching Characteristics

Speed Grade	Conditions	Fmin (Typical Voltage)	Fmax (Typical Voltage)	Unit
C2/I1	-	-	2.5	Gbps
C1/I0	-	-	2.5	Gbps

Table 3-49 MIPI D-PHY TX Switching Characteristics

Speed Grade	Conditions	Fmin (Typical Voltage)	Fmax (Typical Voltage)	Unit
C2/I1	-	-	2.5	Gbps
C1/I0	-	-	2.5	Gbps

### 3.5.4 Data-Clock Timing Specifications

Table 3-50 Data-Clock Timing Specifications

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
$T_{SKEW}(TX)$	Data to Clock Skew	0.08 Gbps $\leq$ Data-Rate $\leq$ 1.5 Gbps	-0.15	-	0.15	UIINST
		1.5 Gbps $\leq$ Data-Rate $\leq$ 2.5 Gbps	-0.2	-	0.2	UIINST
$T_{SETUP}(RX)$	Input Data Setup Before CLK	0.08 Gbps $\leq$ Data-Rate $\leq$ 1.5 Gbps	0.15	-	-	UI
		1.5 Gbps $\leq$ Data-Rate $\leq$ 2.5 Gbps	0.2	-	-	UI
$T_{HOLD}(RX)$	Input Data Hold After CLK	0.08 Gbps $\leq$ Data-Rate $\leq$ 1.5 Gbps	0.15	-	-	UI
		1.5 Gbps $\leq$ Data-Rate $\leq$ 2.5 Gbps	0.2	-	-	UI

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
F <sub>IN</sub>	Input frequency to GPLL for DPHY	-	19	-	400	MHz
UI Instantaneous	U <sub>inst</sub>	-	-	-	12.5	ns
UI Variation	ΔUI	0.08 Gbps ≅ Data-Rate ≅ 1.5 Gbps	-0.1	-	0.1	ns
		DataRate > 1.5Gbps	-0.05	-	0.05	ns

## 3.6 MIPI C-PHY Switching Characteristics

Table 3-51 MIPI C-PHY RX Switching Characteristics

Speed Grade	Conditions	Fmin (Typical Voltage)	Fmax (Typical Voltage <sup>1</sup> )	Unit
C2/I1	V <sub>CC</sub> =0.9V; V <sub>DDAM</sub> =1.05V	-	2.3 <sup>[2]</sup>	Gsps
	V <sub>CC</sub> =0.9V; V <sub>DDAM</sub> =0.9V	-	2	Gsps
C1/I0	V <sub>CC</sub> =0.9V; V <sub>DDAM</sub> =1.05V	-	2	Gsps
	V <sub>CC</sub> =0.9V; V <sub>DDAM</sub> =0.9V	-	1.8	Gsps

**Note!**

<sup>[1]</sup> Typical Voltages: V<sub>CC</sub>=0.9V; V<sub>DDAM</sub>=0.9V ; V<sub>DDXM</sub>=1.8V; V<sub>DD12M</sub>=1.2V.

Table 3-52 MIPI C-PHY TX Switching Characteristics

Speed Grade	Conditions	Fmin (Typical Voltage)	Fmax (Typical Voltage)	Unit
C2/I1	-	-	2.5	Gsps
C1/I0	-	-	2.5	Gsps

## 3.7 Configuration Interface Timing Specification

GW5A Series of FPGA Products support multiple GowinConfig configurations: SSPI, MSPI, Master CPU, Slave CPU, Master SERIAL, Slave SERIAL. For more detailed information, see:

- [UG704, Arora V 138K&75K FPGA Products Programming and Configuration User Guide](#)
- [UG718, Arora V 60K FPGA Products Programming and Configuration User Guide](#)
- [UG714, Arora V 25K FPGA Products Programming and Configuration User Guide](#)

# 4 Ordering Information

## 4.1 Part Name

Figure 4-1 Part Naming Examples-ES

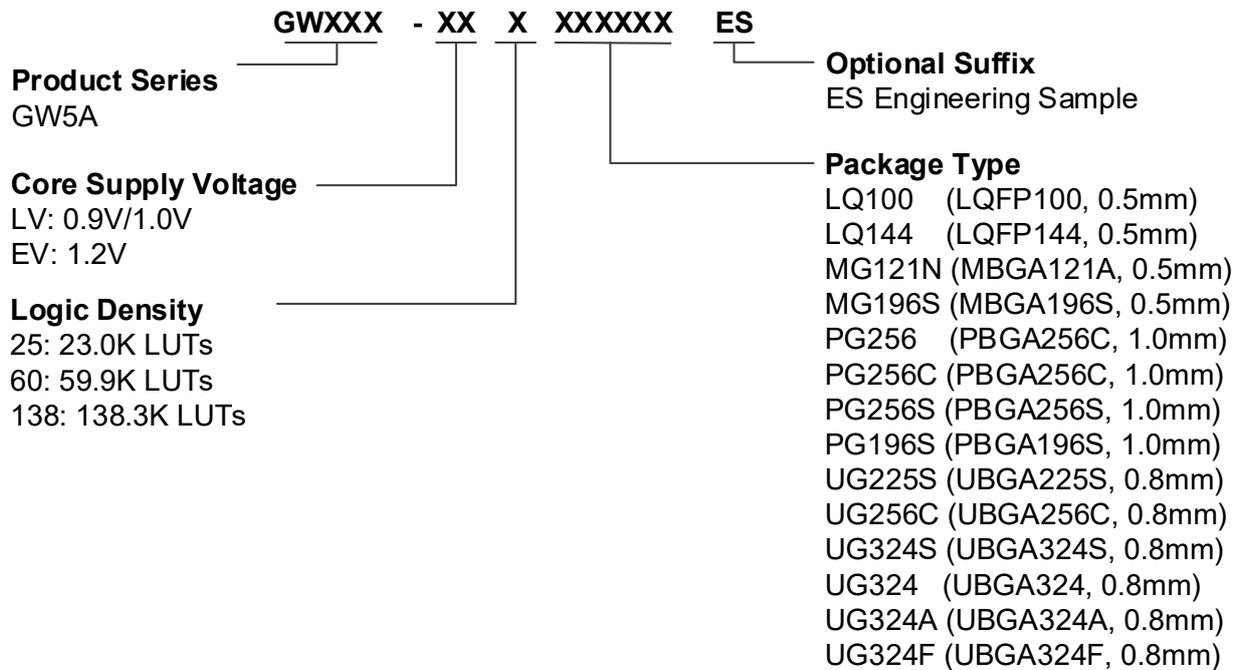
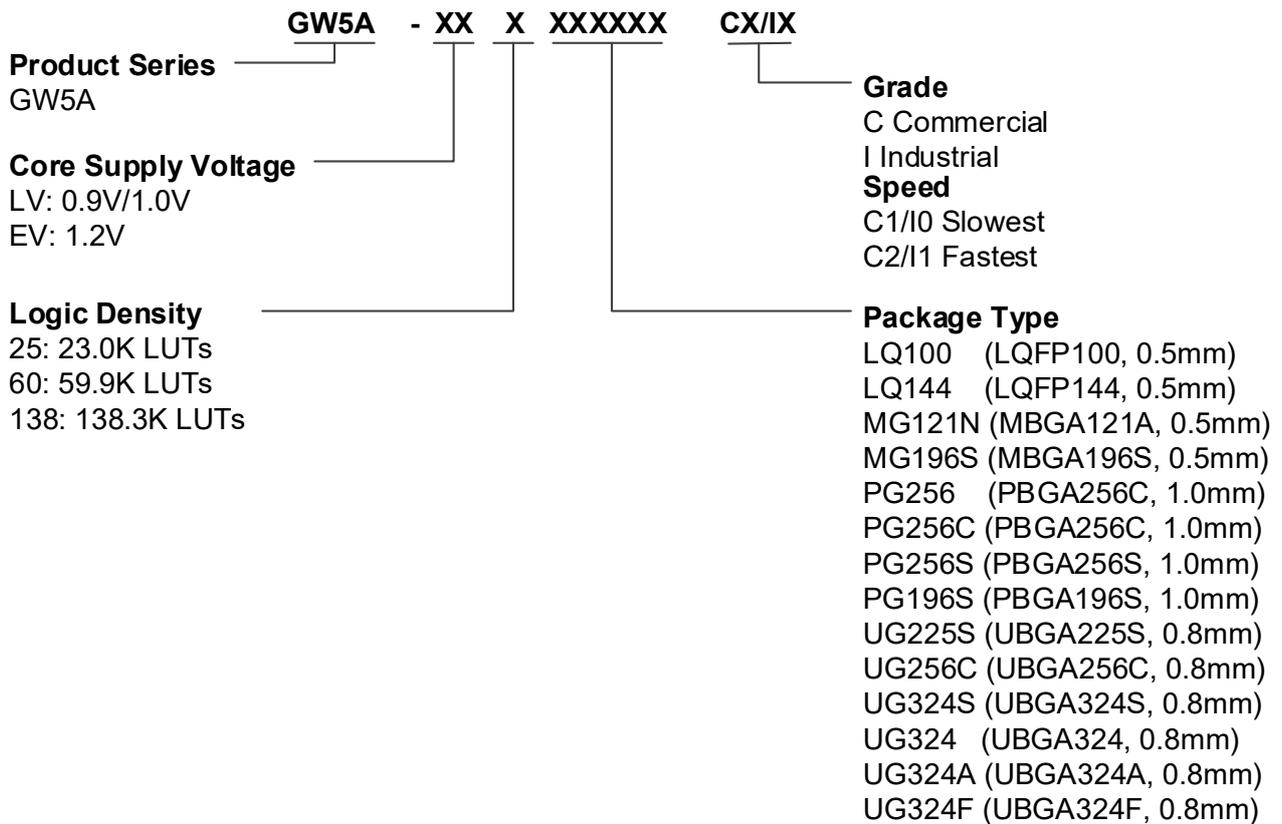


Figure 4-2 Part Naming Examples–Production

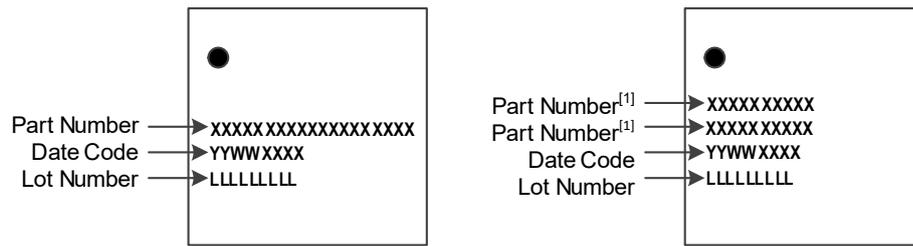
**Note!**

- For the further detailed information about the package information, please refer to [Table 1-1](#).
- The LittleBee family devices and Arora family devices of the same speed grade have different speeds.
- Both “C” and “I” are used in GOWIN part name marking for one device, such as C2/I1, C1/I0, etc. GOWIN devices are screened using industrial standards, so one same device can be used for both industrial (I) and commercial (C) applications. The maximum temperature of the industrial grade is 100°C, and the maximum temperature of the commercial grade is 85°C. Therefore, if the same chip meets the speed grade 2 in the commercial grade application, the speed grade is 1 in the industrial grade application.

## 4.2 Package Mark

The device information of GOWINSEMI is marked on the chip surface, as shown in [Figure 4-3](#).

Figure 4-3 Package Mark Examples



**Note!**

<sup>[1]</sup> The first two lines in the right figure above are the “Part Number”.

# 5 About This Guide

## 5.1 Purpose

This data sheet describes the features, product resources, structure, AC/DC characteristics, and the ordering information of GW5A Series of FPGA Products, making it easier for users to understand the products, which will help in the selection and use of the device.

## 5.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at [www.gowinsemi.com](http://www.gowinsemi.com):

- [UG714, Arora V 25K FPGA Products Programming and Configuration User Guide](#)
- [UG704, Arora V 138K& 75K FPGA Products Programming and Configuration User Guide](#)
- [UG718, Arora V 60K FPGA Products Programming and Configuration User Guide](#)
- [UG1101, GW5A Series of FPGA Products Package and Pinout Manual](#)
- [UG987, GW5A Series of FPGA Products Schematic Manual](#)
- [UG985, GW5A-25 Pinout](#)
- [UG1229, GW5A-60 Pinout](#)
- [UG988, GW5A-138 Pinout](#)

## 5.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in [Table 5-1](#).

Table 5-1 Terminology and Abbreviations

Terminology and Abbreviations	Full Name
ADC	Analog to Digital Converter
AER	Advanced Error Reporting

Terminology and Abbreviations	Full Name
ALP	Adaptive Low Power
ALU	Arithmetic Logic Unit
BSRAM	Block Static Random Access Memory
CFU	Configurable Function Unit
CLS	Configurable Logic Section
CMSER	Configuration Memory Soft Error Recovery
CRU	Configurable Routing Unit
CSI	Camera Serial Interface
CTC	Clock Tolerance Compensation
CTLE	Continuous Time Linear Equalizer
DCS	Dynamic Clock Selector
DFF	D Flip-flop
DNA	Device Identifier
DNL	Differential Non-Linearity
DP	True Dual Port 16K BSRAM
DSI	Display Serial Interface
DSP	Digital Signal Processing
ECC	Error Correction Code
ECRC	End-to-End Cyclic Redundancy Check
ESD	Electro-Static Discharge
FIFO	First In First Out
FPG	FCPBGA
FPGAs	Field Programmable Gate Array
GCLK	Global Clock
GPIO	Gowin Programmable IO
GSR	Global Set/Reset
HCLK	High Speed Clock
HS	High Speed
INL	Integral Non-Linearity
IOB	Input/Output Block
LP	Low Power
LUT	Look-up Table
LW	Long Wire

Terminology and Abbreviations	Full Name
mDRP	Mini Dynamic Re-Program Port
MIPI	Mobile Industry Processor Interface
OTP	One Time Programmable
PCIe	Peripheral Component Interface Express
PCS	Physical Coding Sublayer
PLL	Phase-locked Loop
PMA	Physical Medium Attachment Sublayer
REG	Register
SDP	Semi Dual Port 16K BSRAM
SEU	Single Event Upset
SP	Single Port 16K BSRAM
SSRAM	Shadow Static Random Access Memory
TDM	Time Division Multiplexing

## 5.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: [www.gowinsemi.com](http://www.gowinsemi.com)

E-mail: [support@gowinsemi.com](mailto:support@gowinsemi.com)

