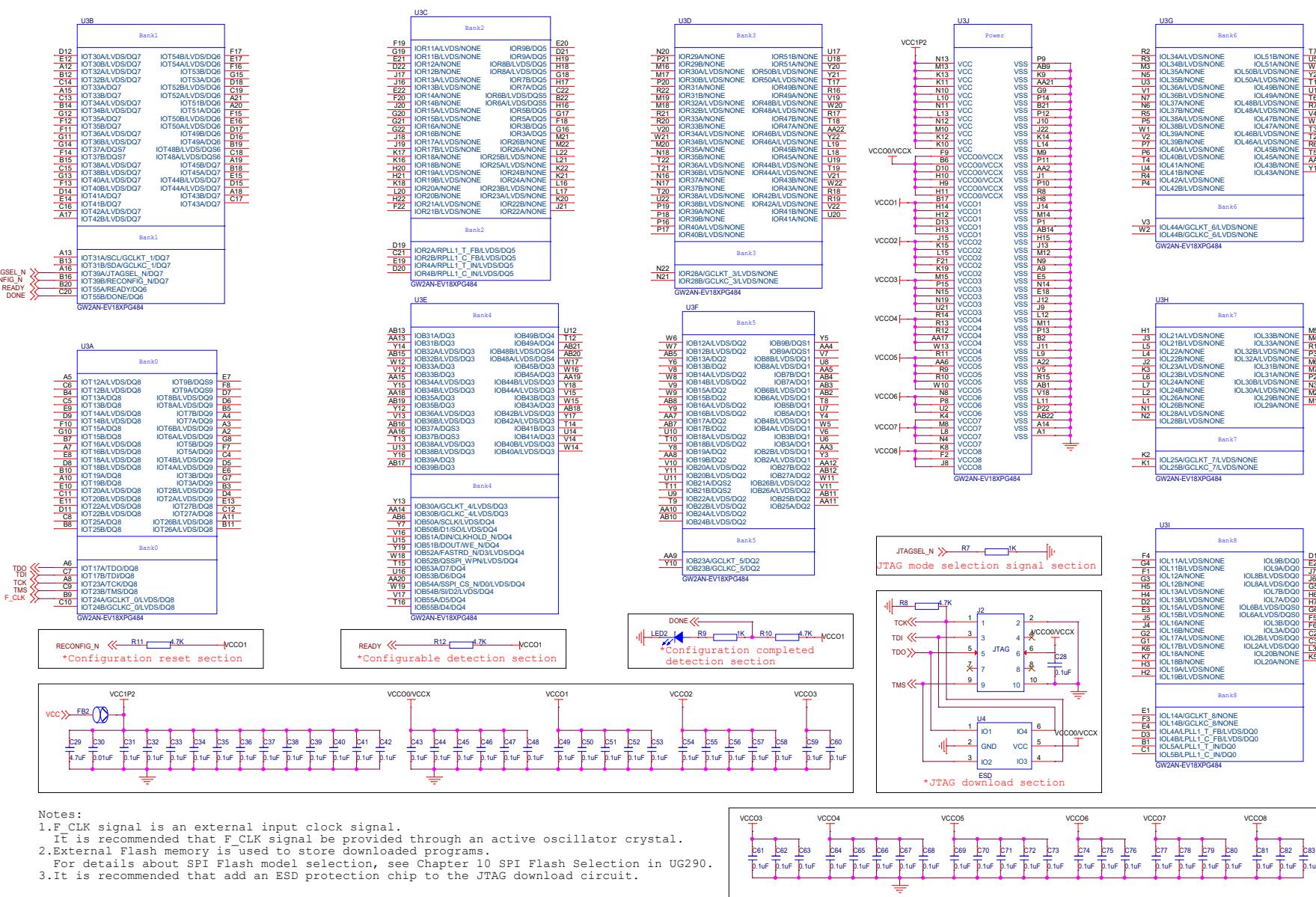
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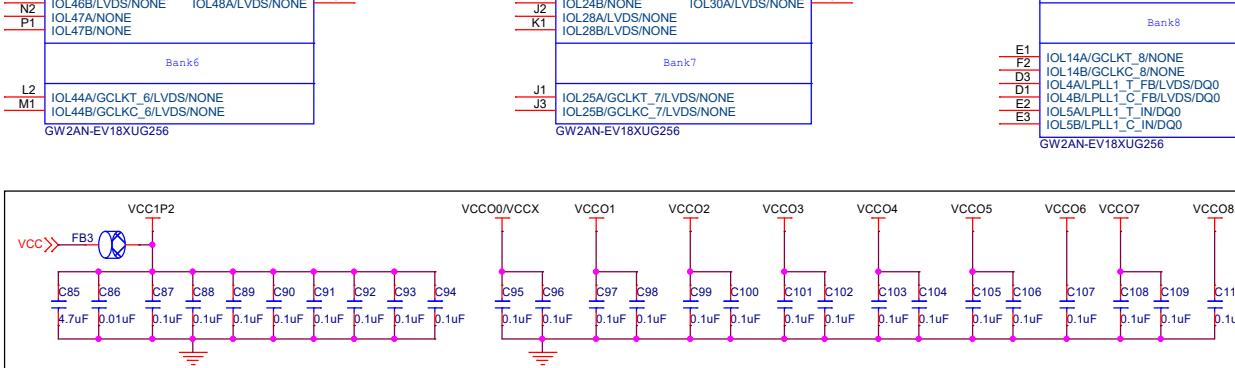
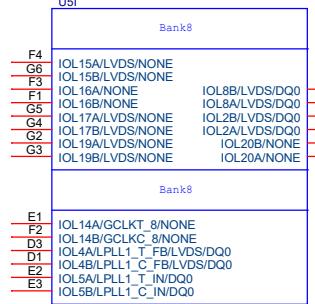
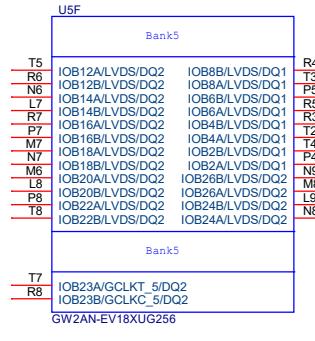
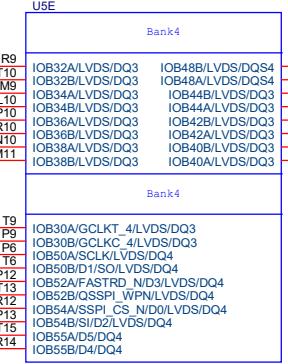
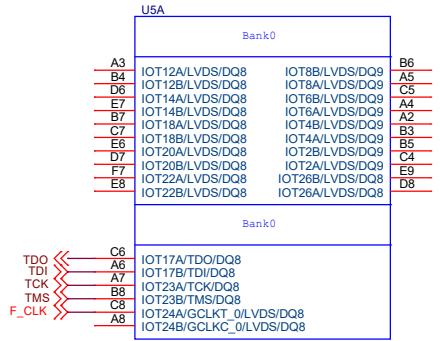
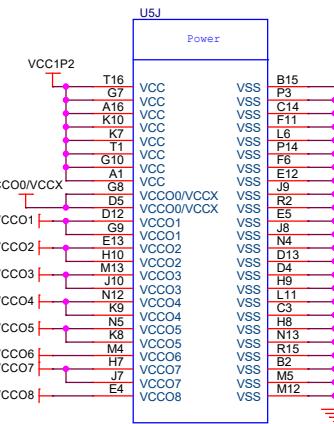
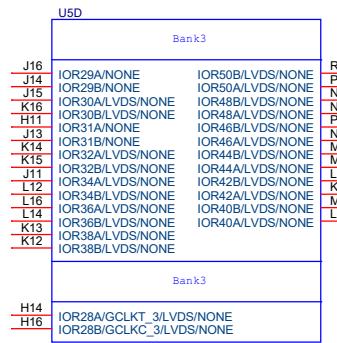
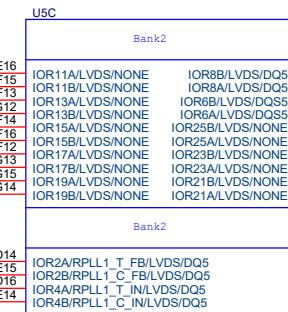
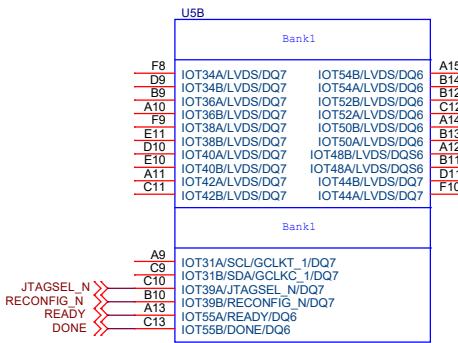
- F CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal.
- External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
- It is recommended that add an ESD protection chip to the JTAG download circuit.

| Title | |
|------------------------------|------------------|
| GOWIN Minimum System Diagram | |
| Size | Document Number |
| A3 | GW2AN-EV18XPG256 |
| Date: | Rev |
| Friday, April 07, 2023 | 2.0 |



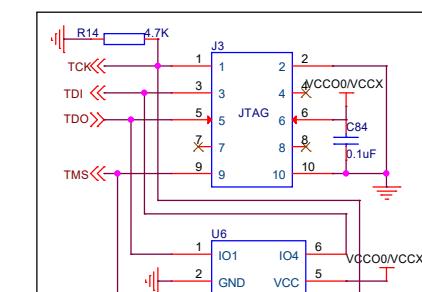
Notes:

- 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
3.It is recommended that add an ESD protection chip to the JTAG download circuit.



- Notes:**
1. F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
 2. External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
 3. It is recommended that add an ESD protection chip to the JTAG download circuit.

JTAGSEL_N → R13 → 1K → J13
JTAG mode selection signal section

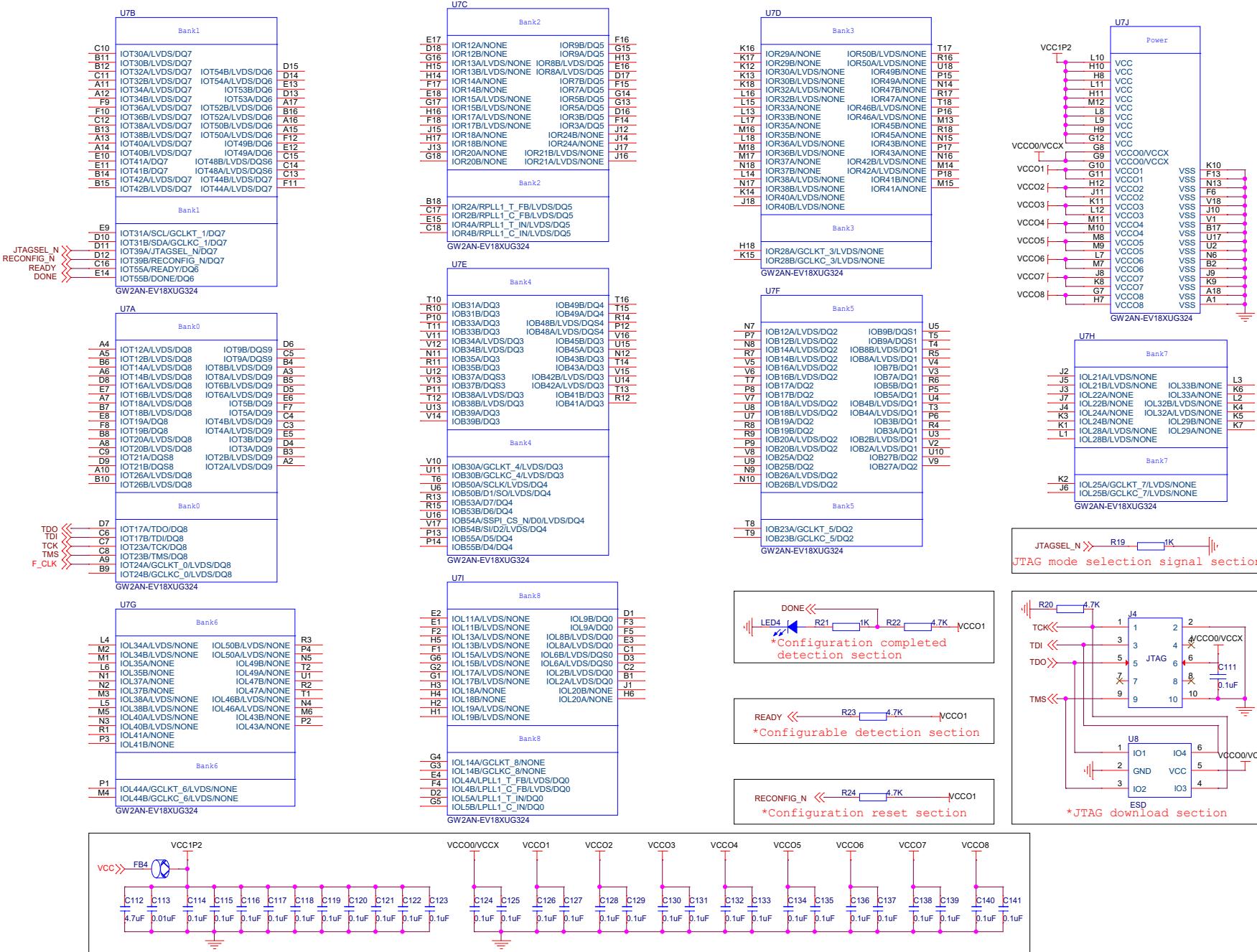


DONE → LED3 → R15 → 1K → R16 → 4.7K → VCCO1
*Configuration completed detection section

READY → R17 → 4.7K → VCCO1
*Configurable detection section

RECONFIG_N → R18 → 4.7K → VCCO1
*Configuration reset section

| Title | |
|------------------------------|------------------------|
| GOWIN Minimum System Diagram | |
| Size | Document Number |
| A3 | GW2AN-EV18XUG256 |
| Rev | 2.0 |
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| Sheet | 3 of 21 |

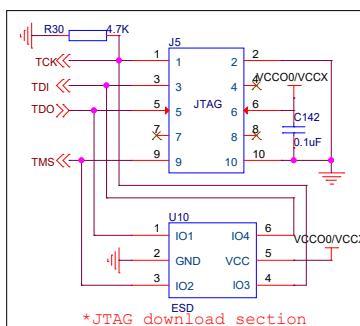
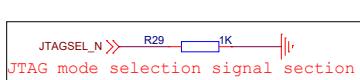
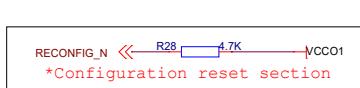
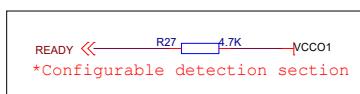
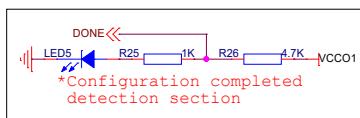
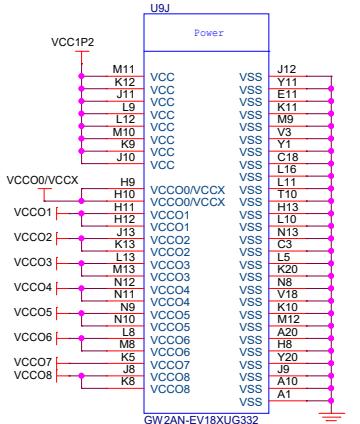
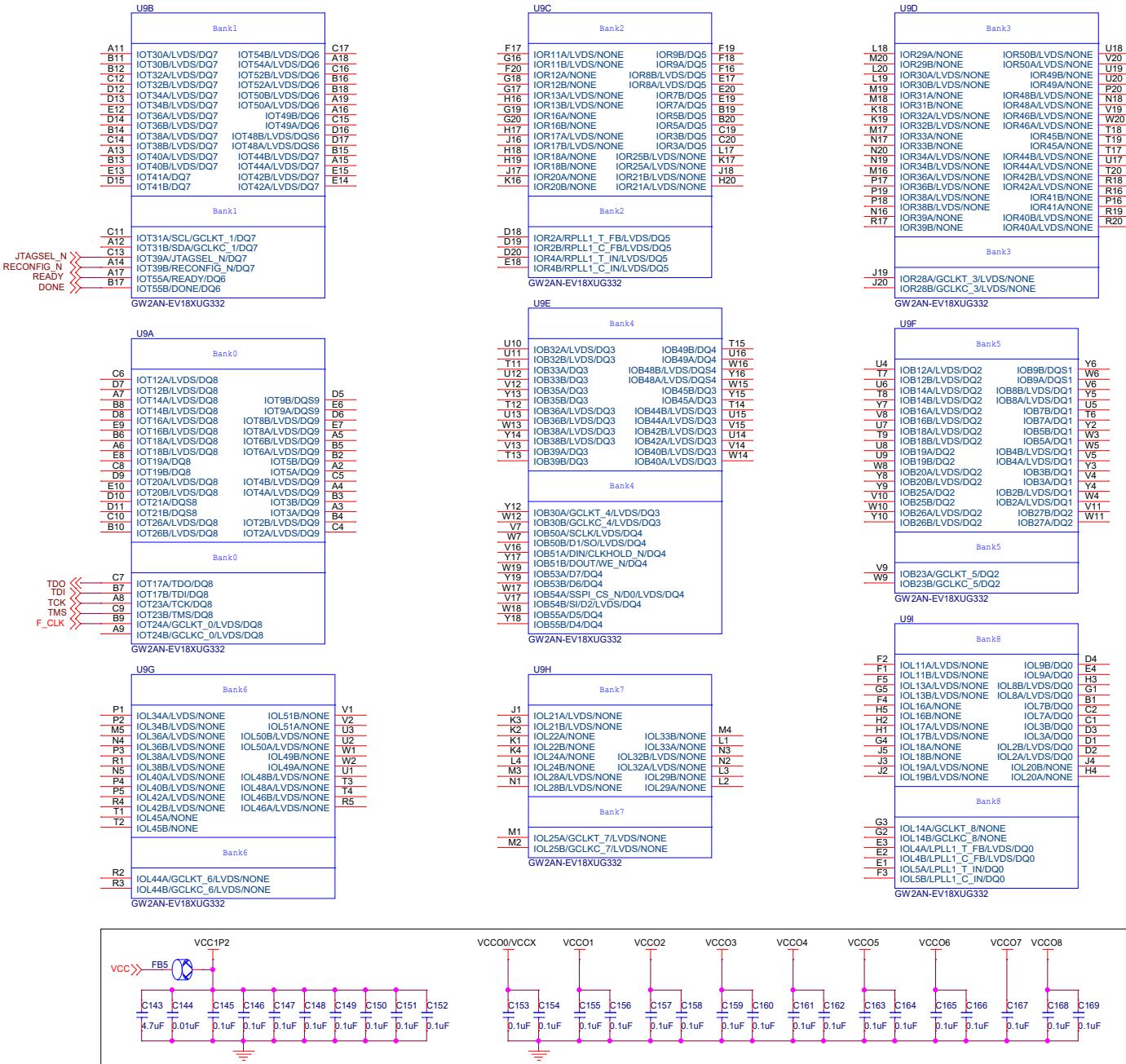


Notes:

- NOTES:

 - 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
 - 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290
 - 3.It is recommended that add an ESD protection chip to the JTAG download circuit.

| Title | | |
|------------------------------|------------------------|---------------|
| GOWIN Minimum System Diagram | | |
| Size | Document Number | Rev |
| Custom | GW2AN-EV18XUG324 | 2.0 |
| Date | Friday, April 07, 2023 | Sheet 4 of 21 |

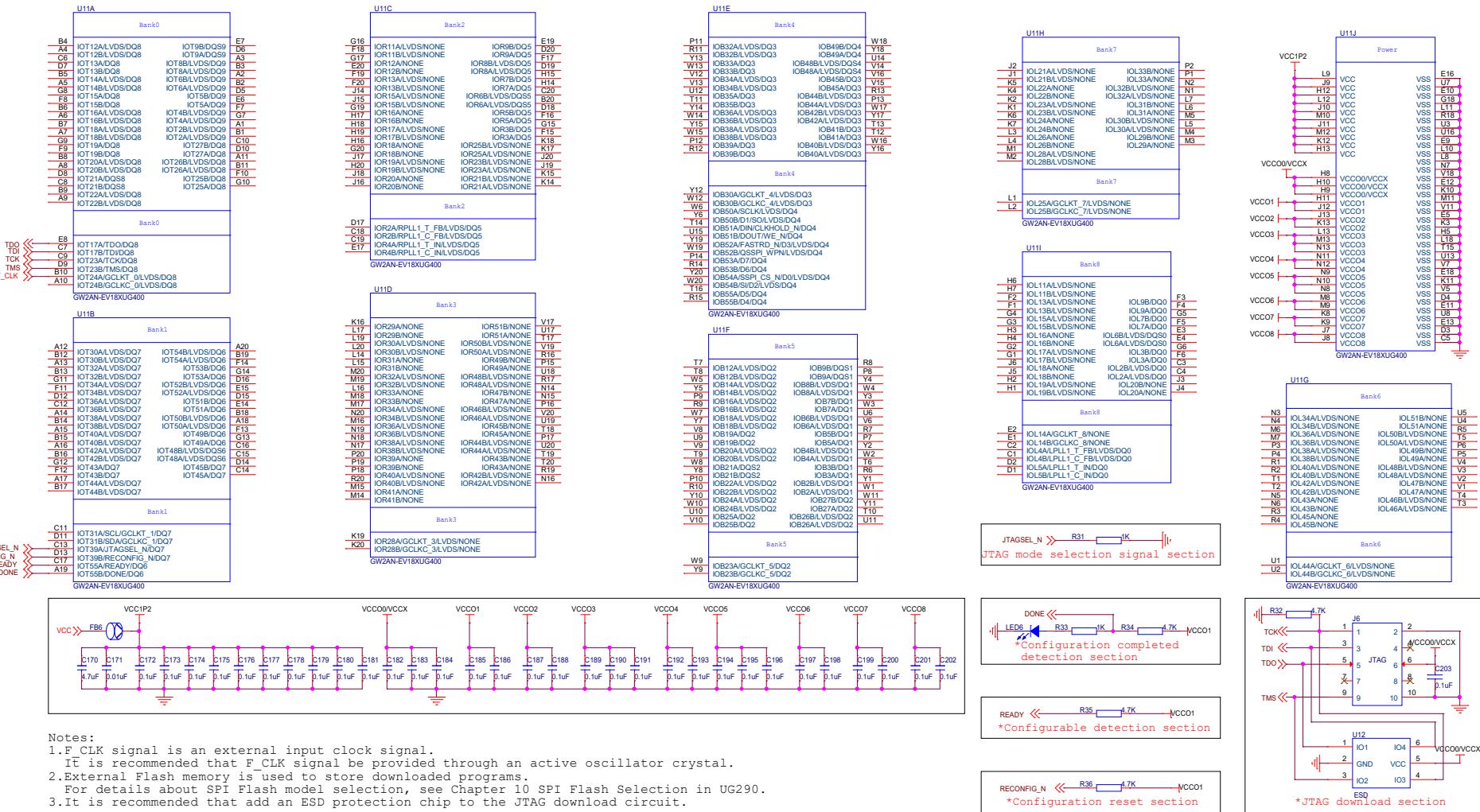


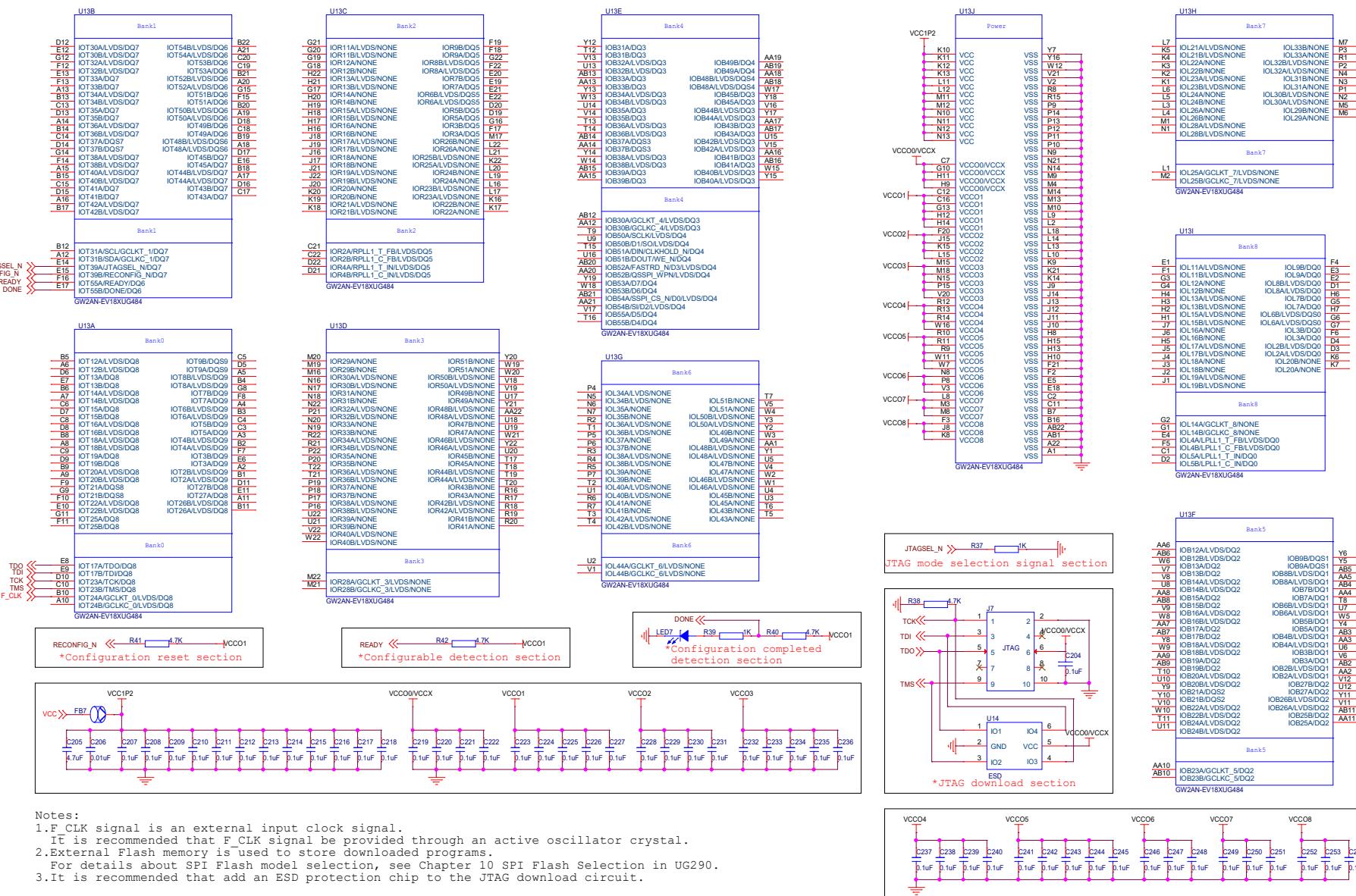
Notes:

- Notes:

 - 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
 - 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290
 - 3.It is recommended that add an ESD protection chip to the JTAG download circuit.

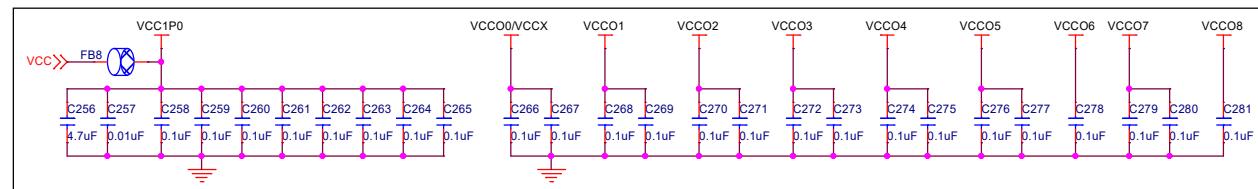
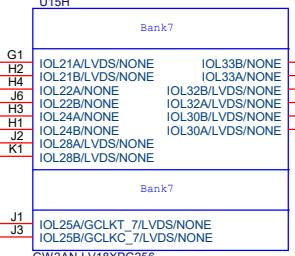
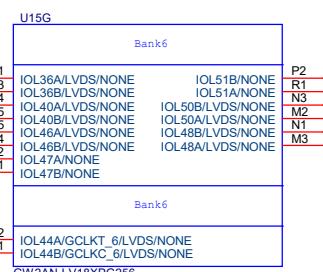
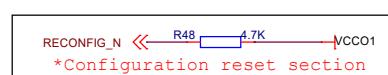
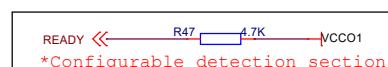
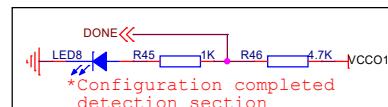
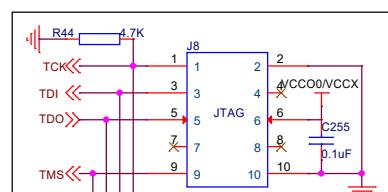
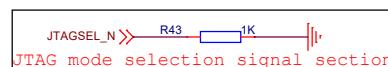
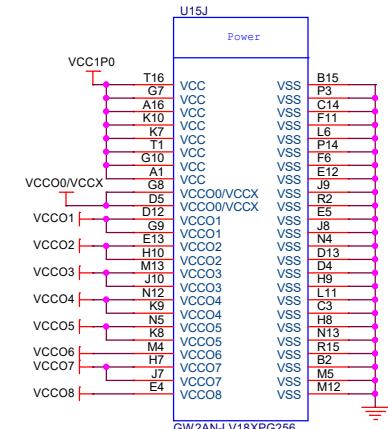
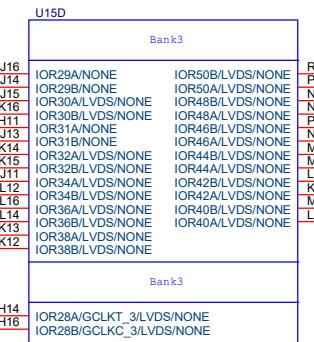
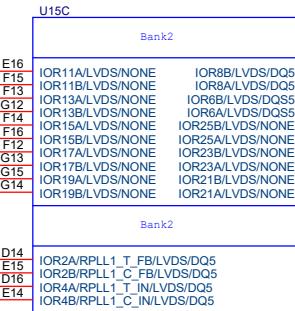
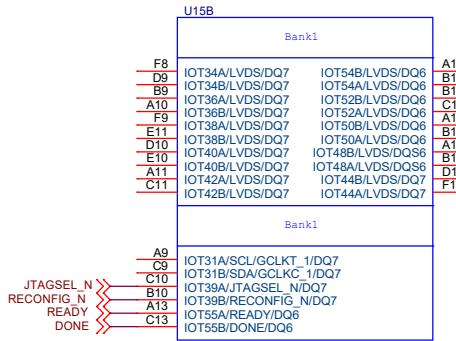
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| GOWIN Minimum System Diagram | | |
| Size | Document Number | Rev. |
| Custom | GW2AN-EV18XUG332 | 2.0 |
| Date: | Friday, April 07, 2023 | Sheet 5 of 21 |





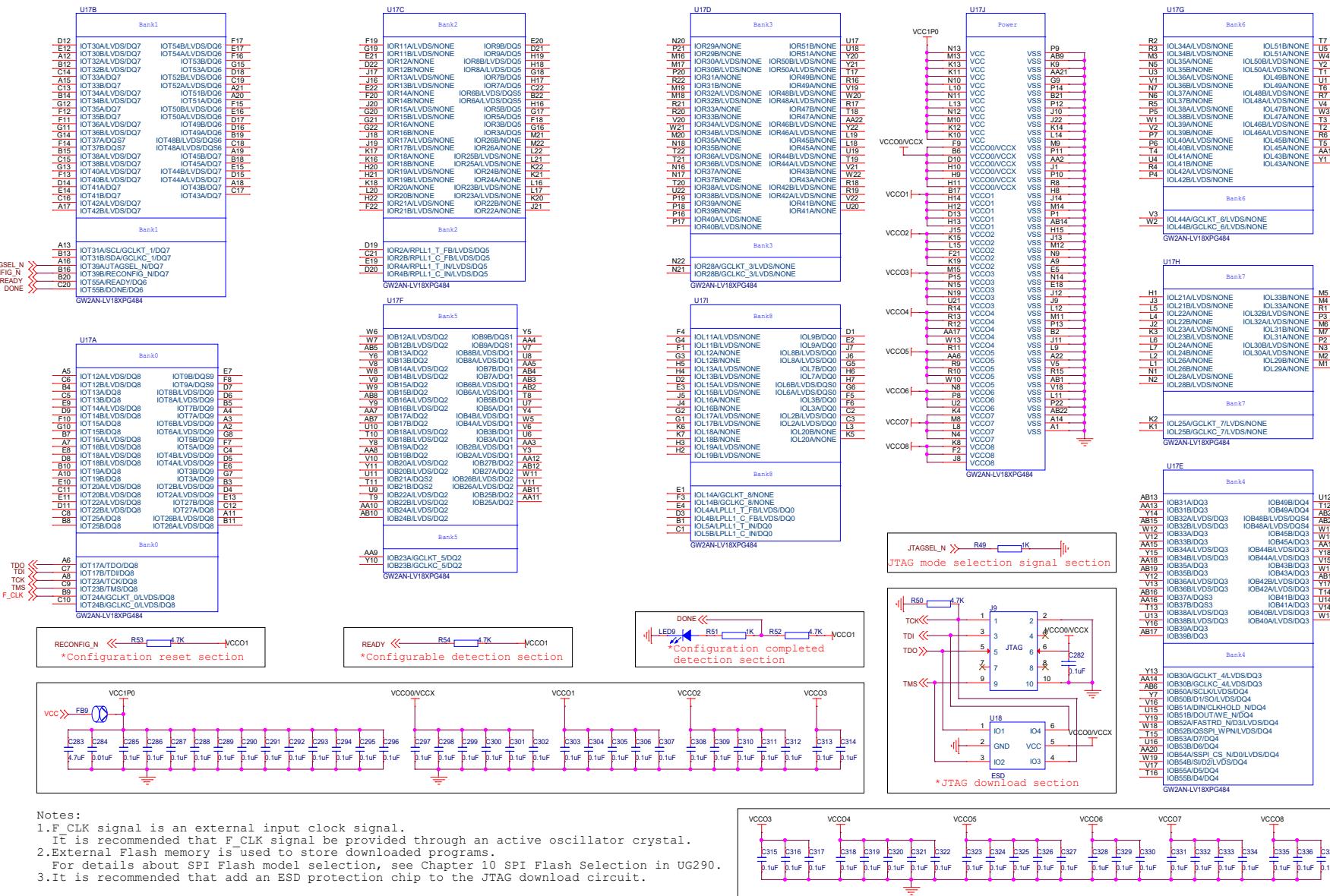
Notes:

- 1.F CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal.
 - 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290
 - 3.It is recommended that add an ESD protection chip to the JTAG download circuit.

**Notes:**

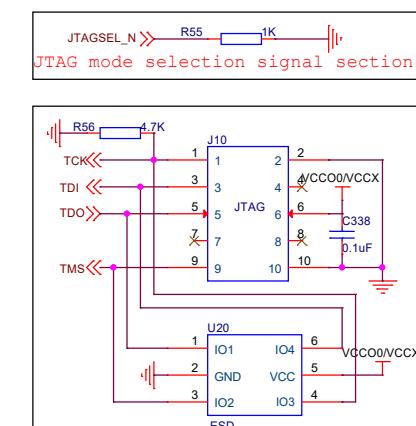
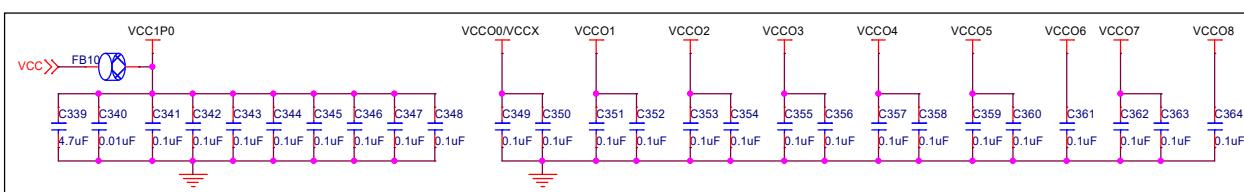
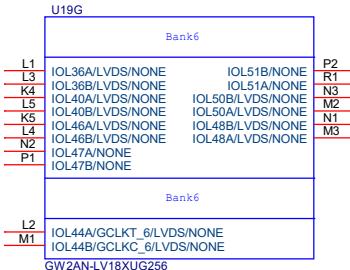
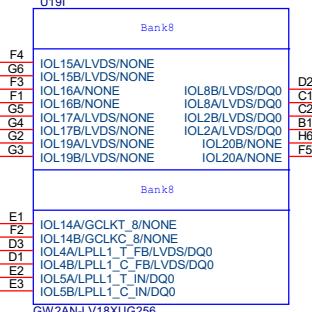
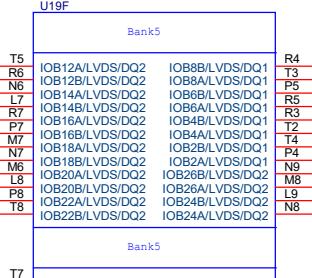
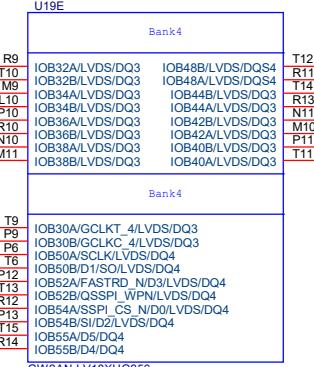
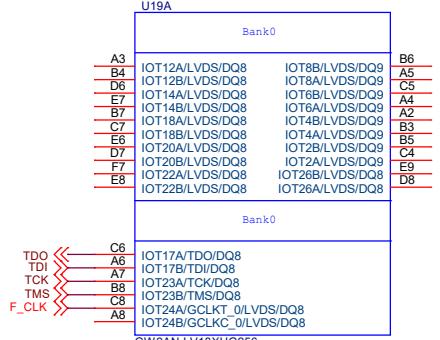
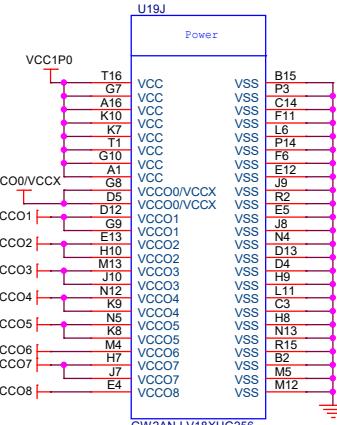
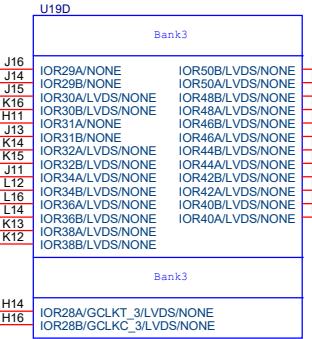
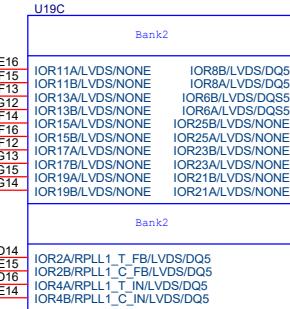
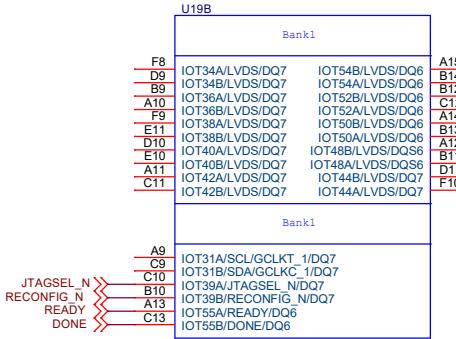
- F CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal.
- External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
- It is recommended that add an ESD protection chip to the JTAG download circuit.

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| Document Number | |
| Size | Rev |
| A3 | 2.0 |
| Date: Friday, April 07, 2023 | |



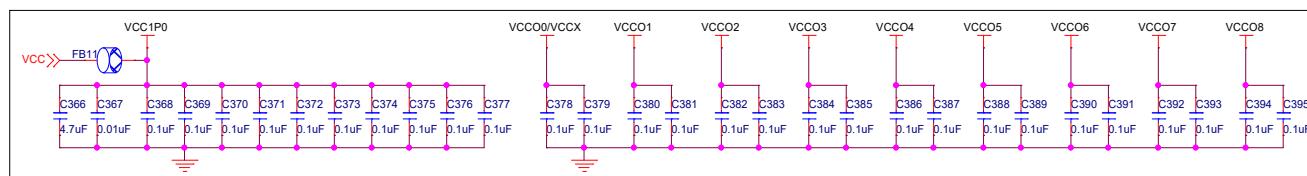
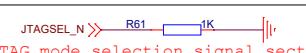
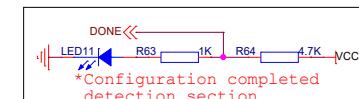
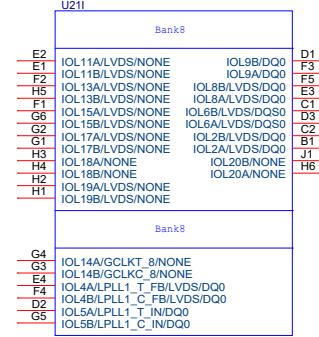
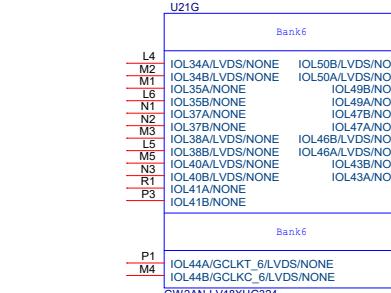
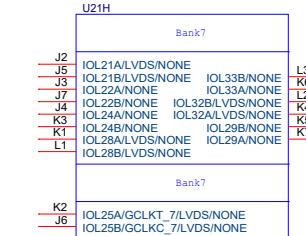
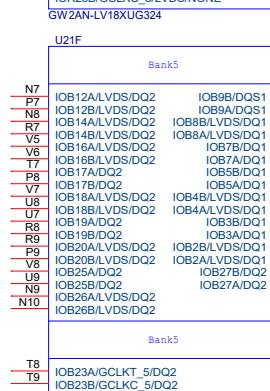
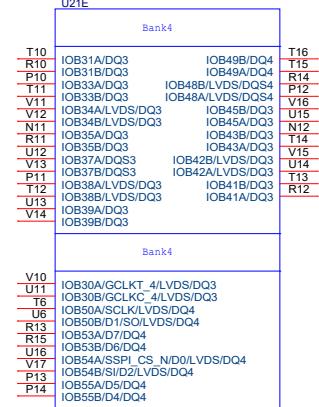
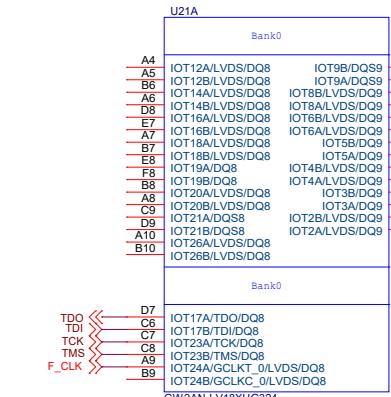
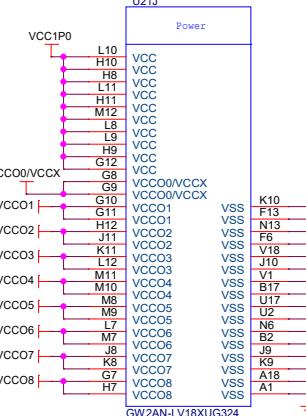
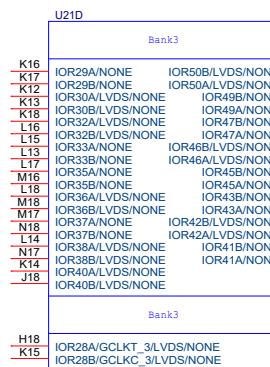
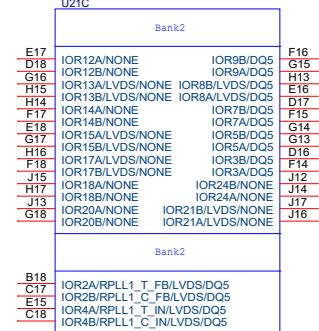
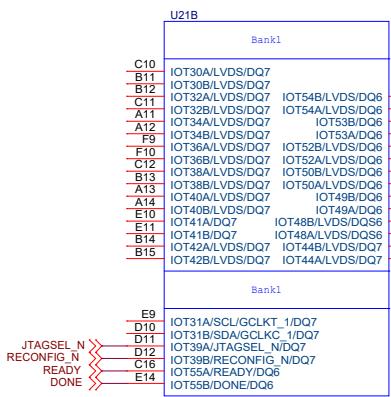
Notes:

- 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG251.
3.It is recommended that add an ESD protection chip to the JTAG download circuit.



Notes:

1. F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
3. It is recommended that add an ESD protection chip to the JTAG download circuit.

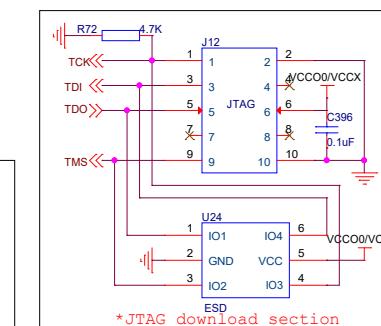
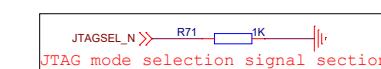
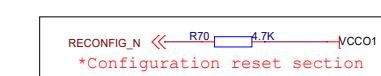
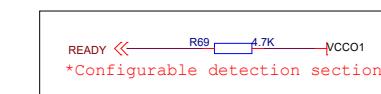
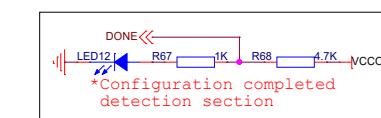
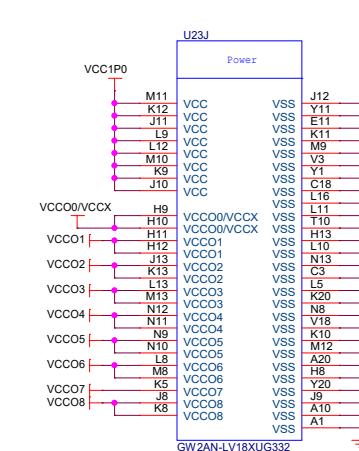
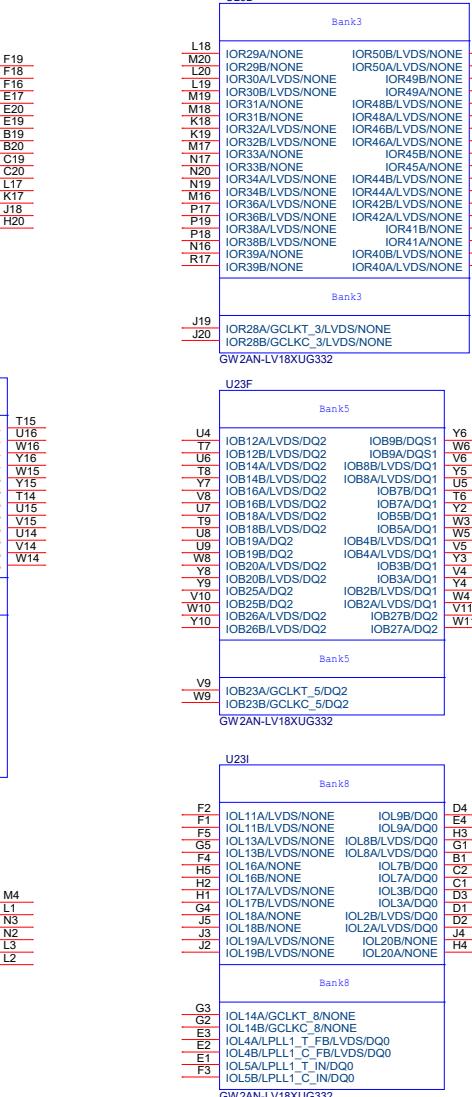
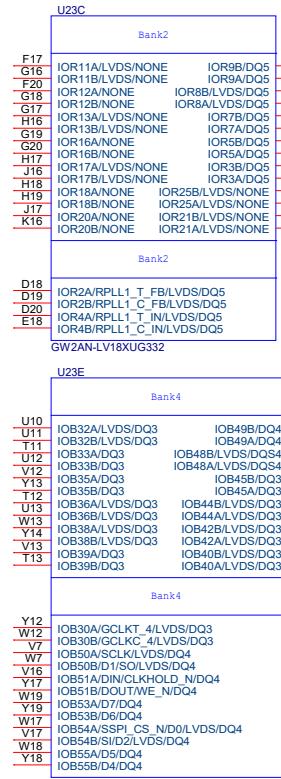
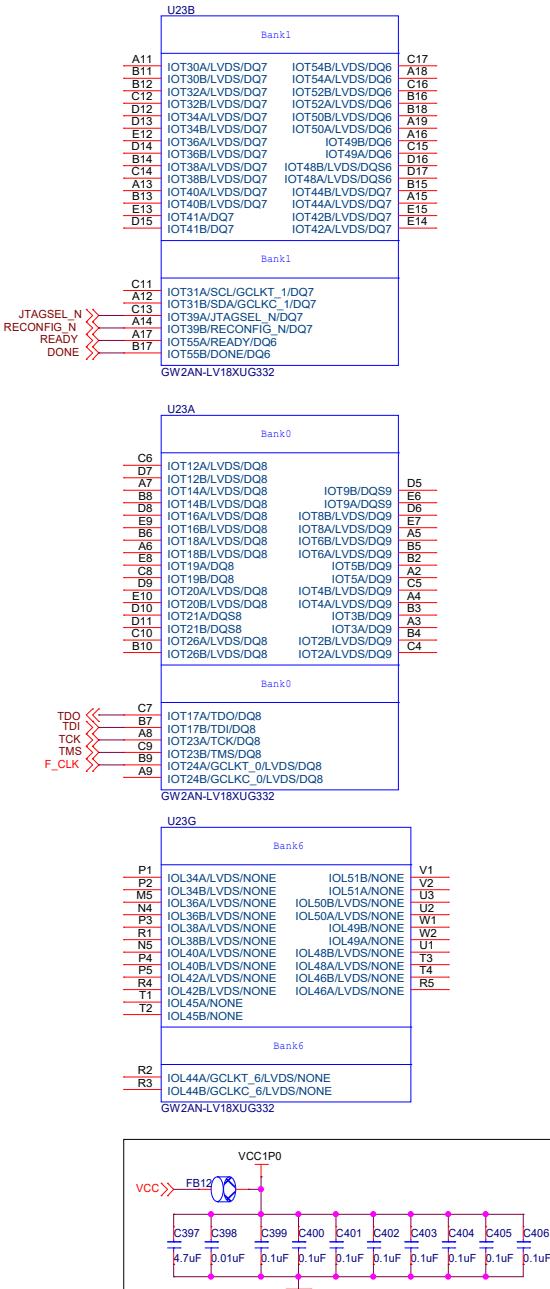


Notes:

- Notes:**

 - 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
 - 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
 - 3.It is recommended that add an ESD protection chip to the JTAG download circuit.

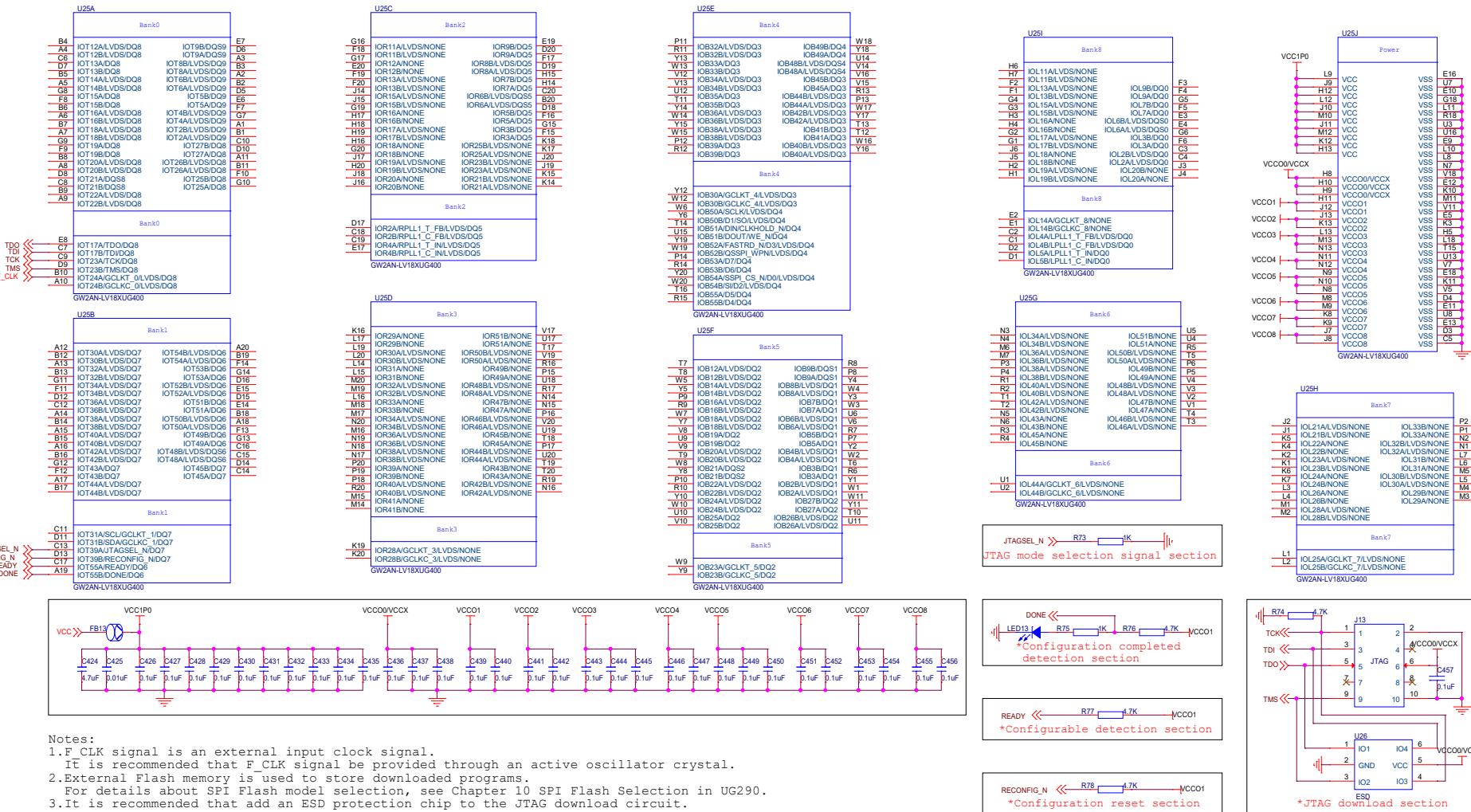
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| Size | Document Number | | | Rev. |
| Custom | GW2AN-LV16XUG324 | | | 2.0 |
| Date | Friday April 07 2023 | | | Sheet 11 of 21 |

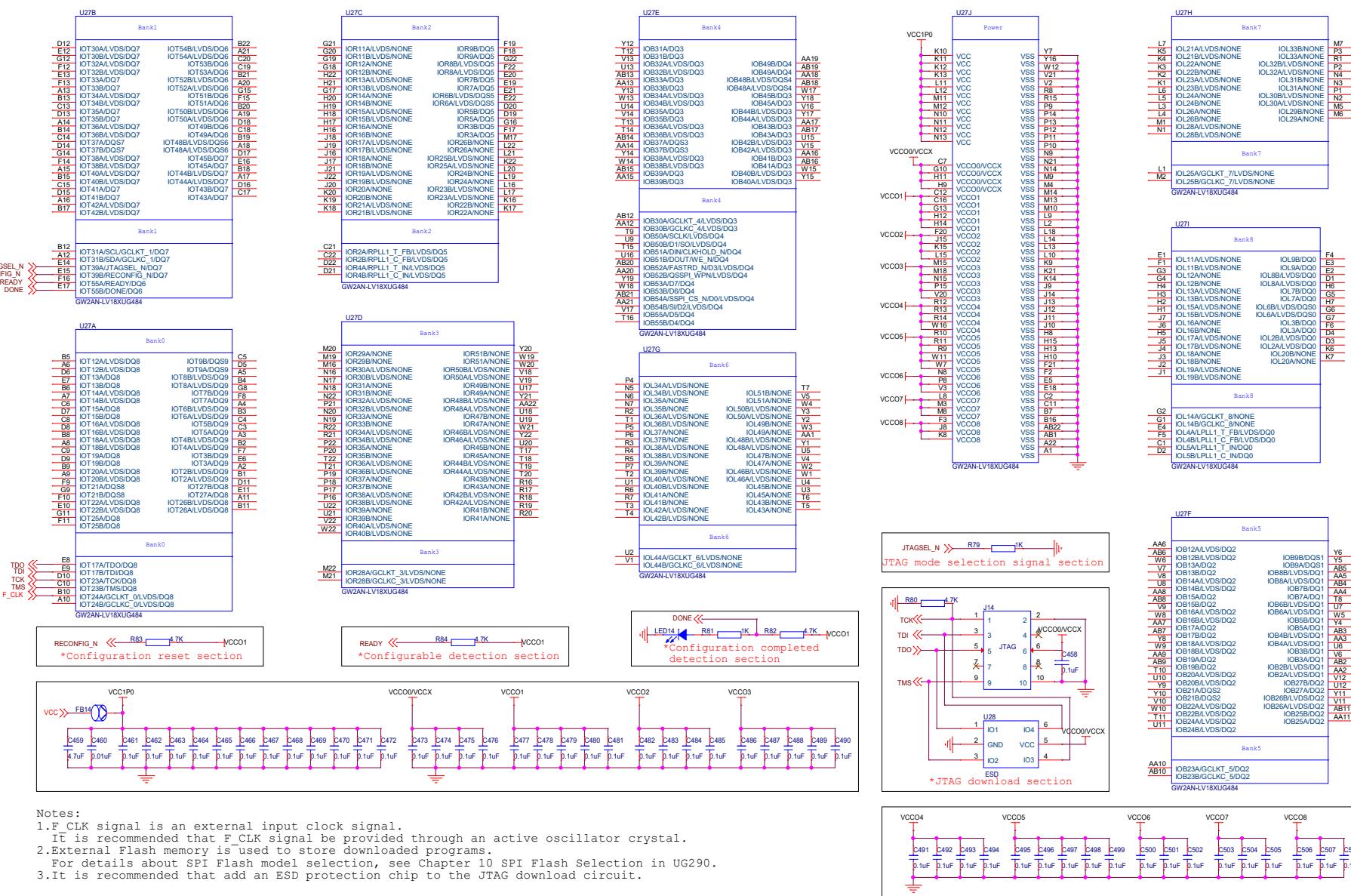


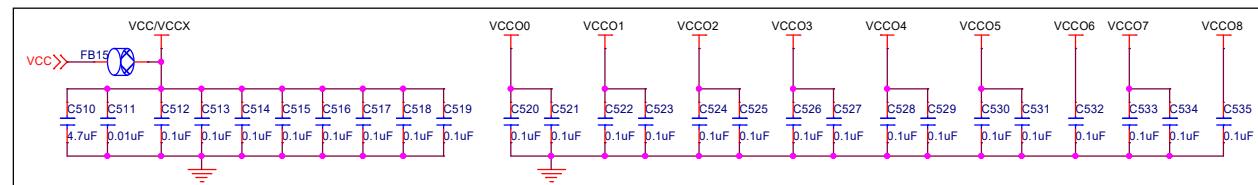
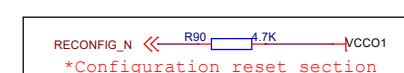
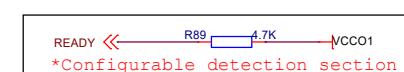
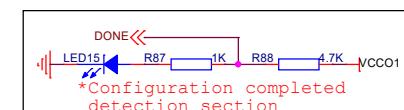
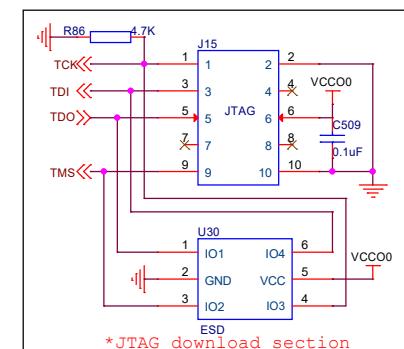
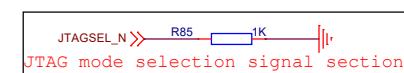
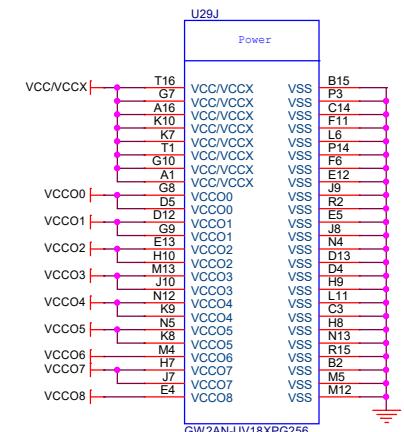
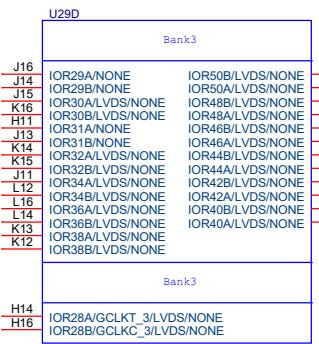
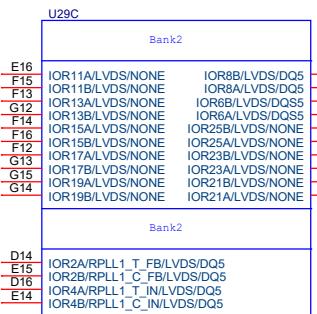
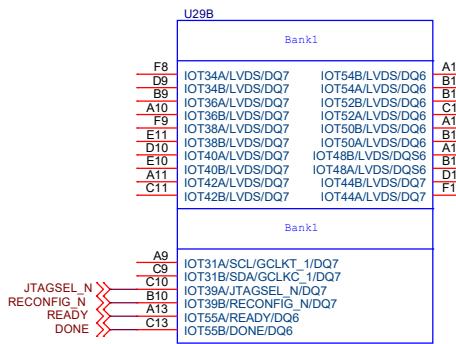
Notes:

- Notes:

 - 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
 - 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290
 - 3.It is recommended that add an ESD protection chip to the JTAG download circuit.

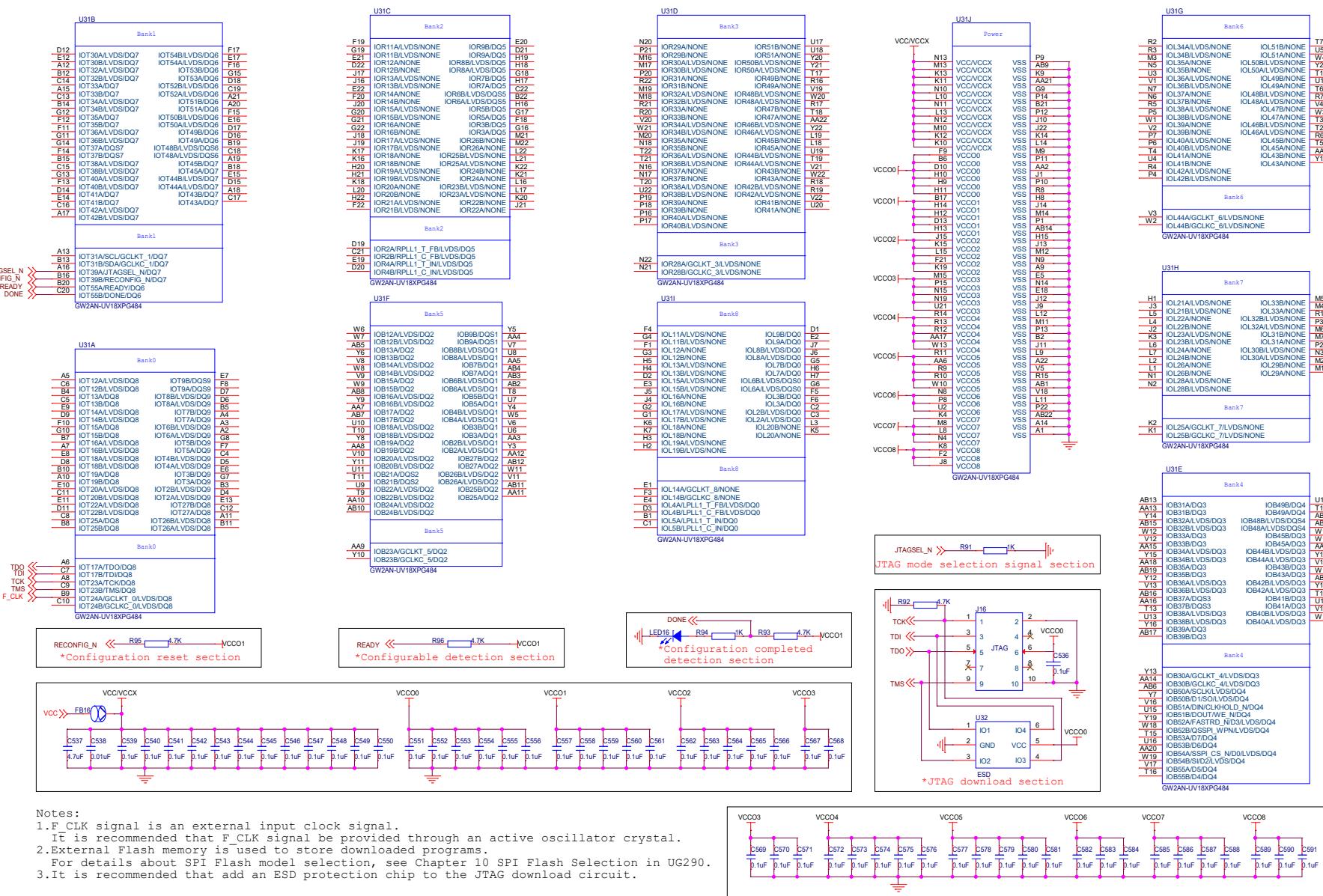




**Notes:**

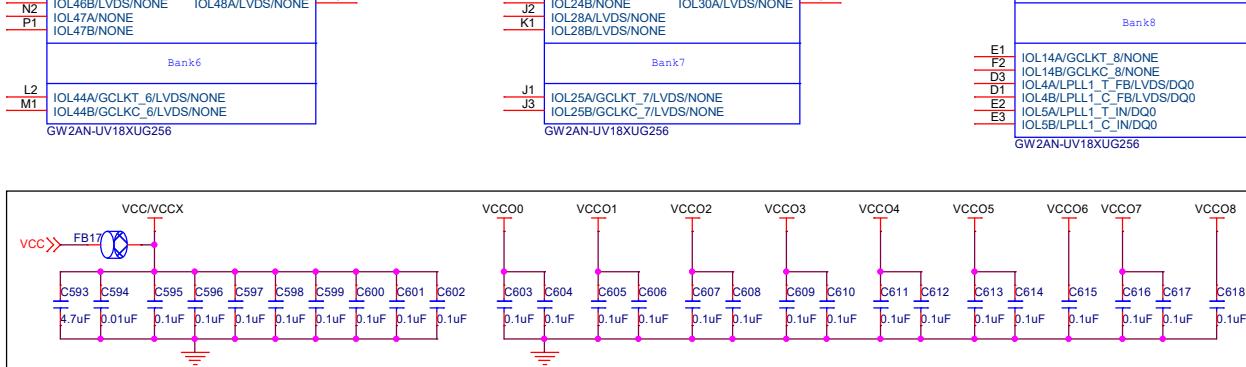
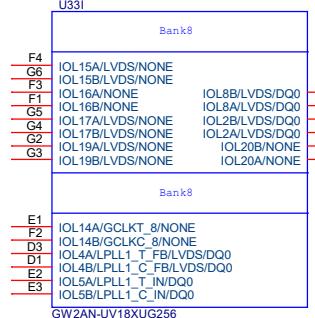
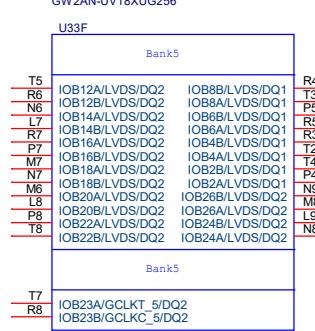
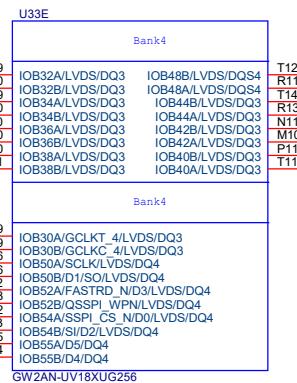
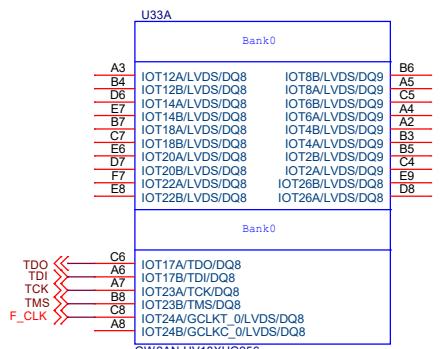
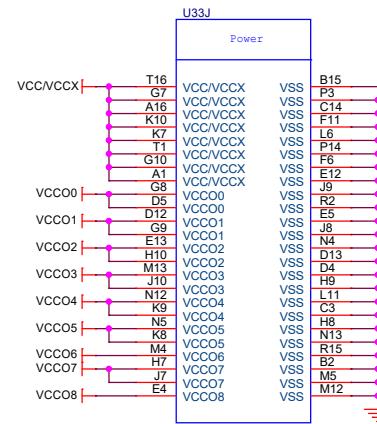
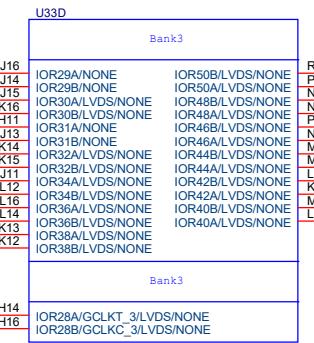
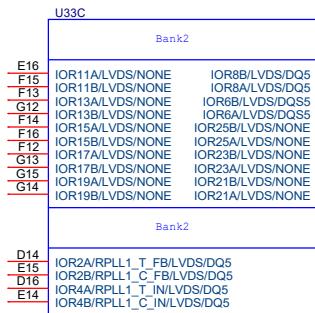
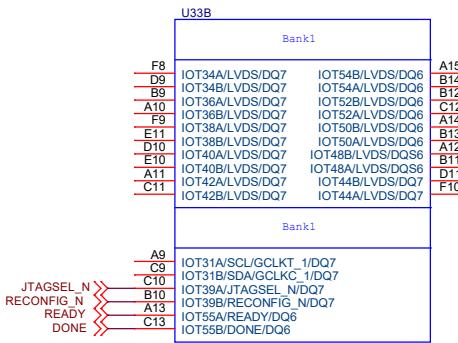
1. F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
3. It is recommended that add an ESD protection chip to the JTAG download circuit.

| Title | | |
|------------------------------|------------------------|----------------|
| GOWIN Minimum System Diagram | | |
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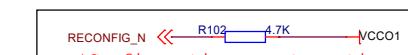
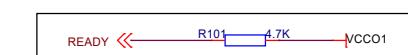
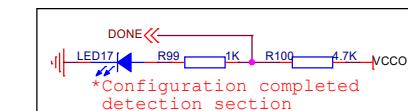
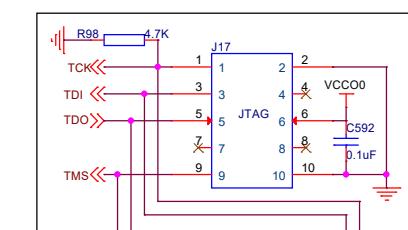
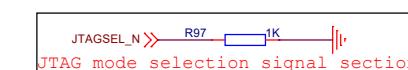
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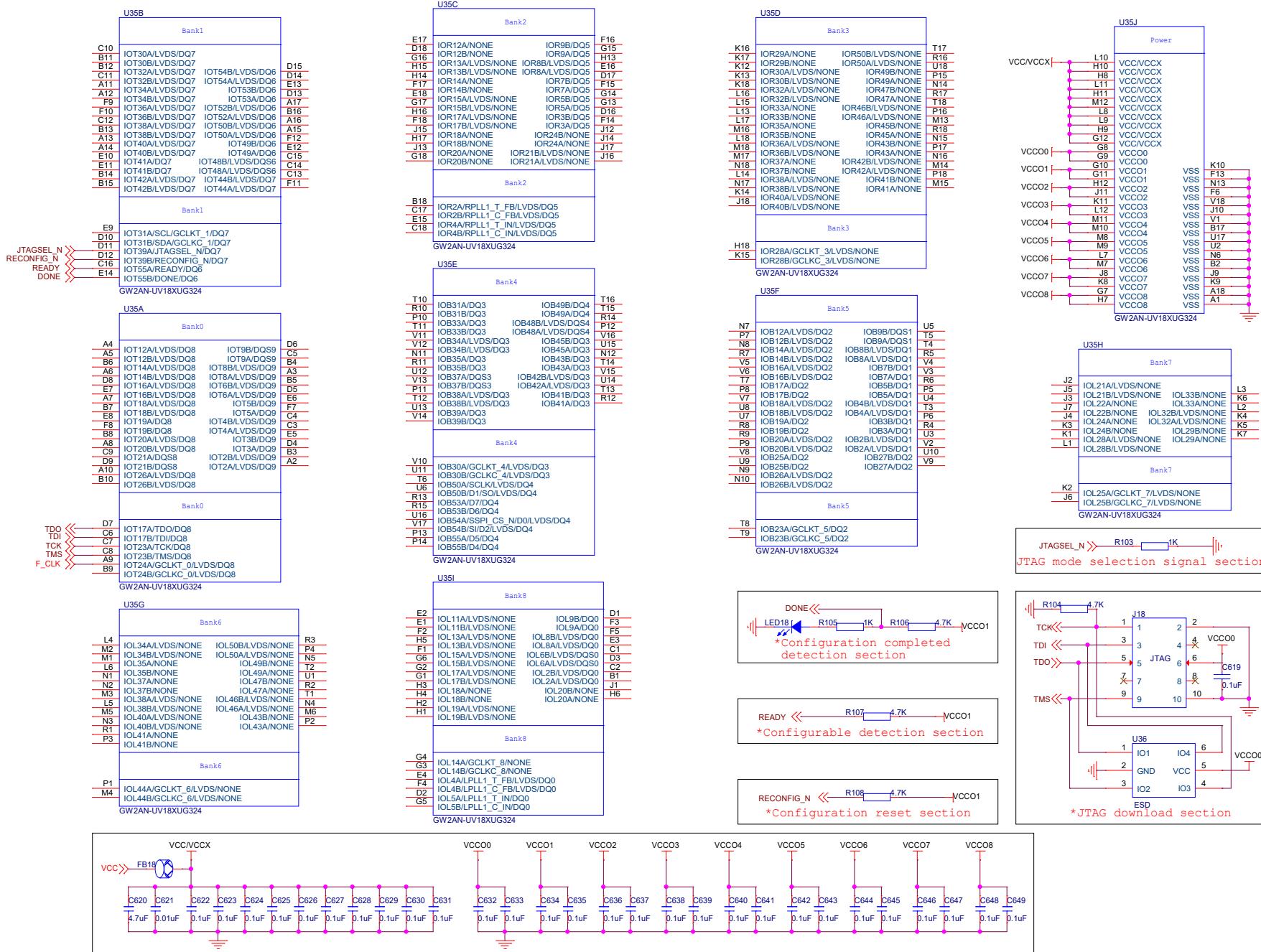
- 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
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Notes:

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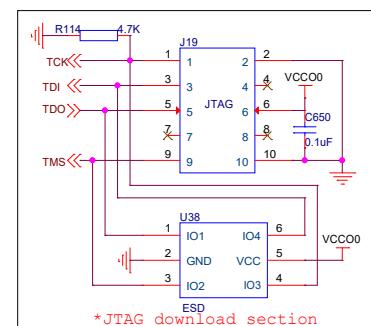
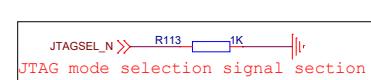
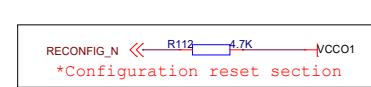
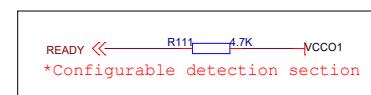
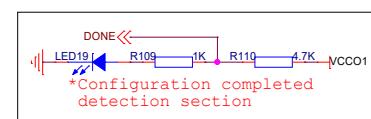
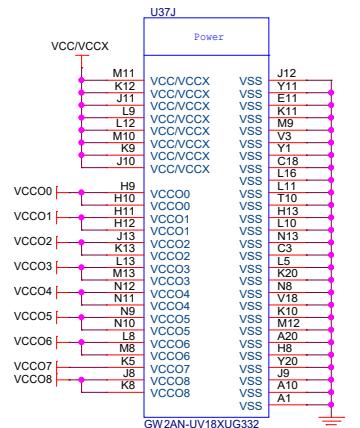
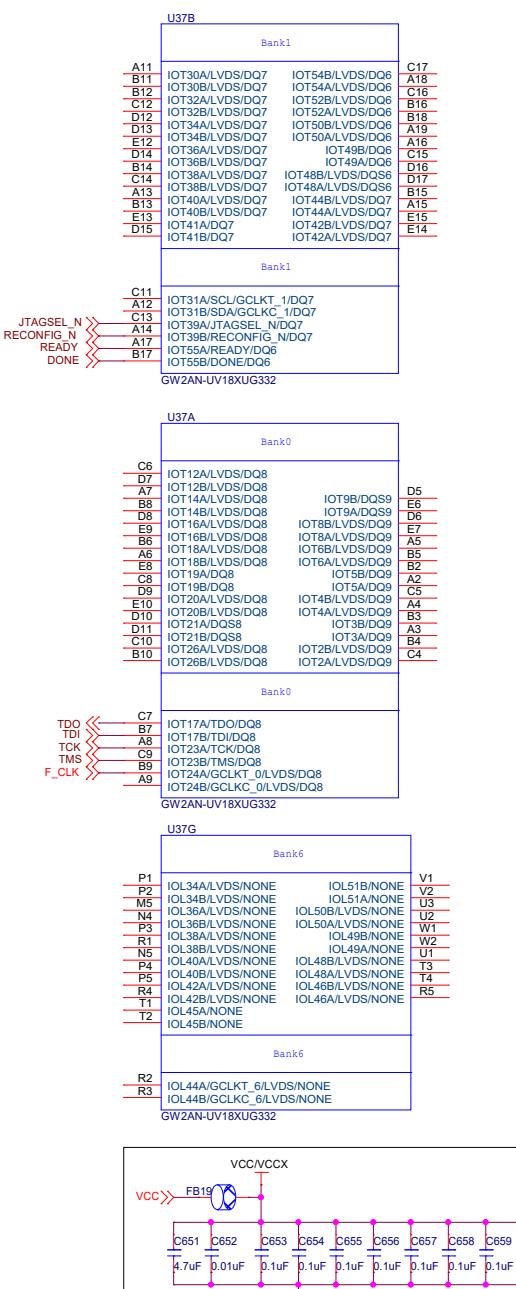


Notes:

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| Title | | |
|------------------------------|------------------------|----------------|
| GOWIN Minimum System Diagram | | |
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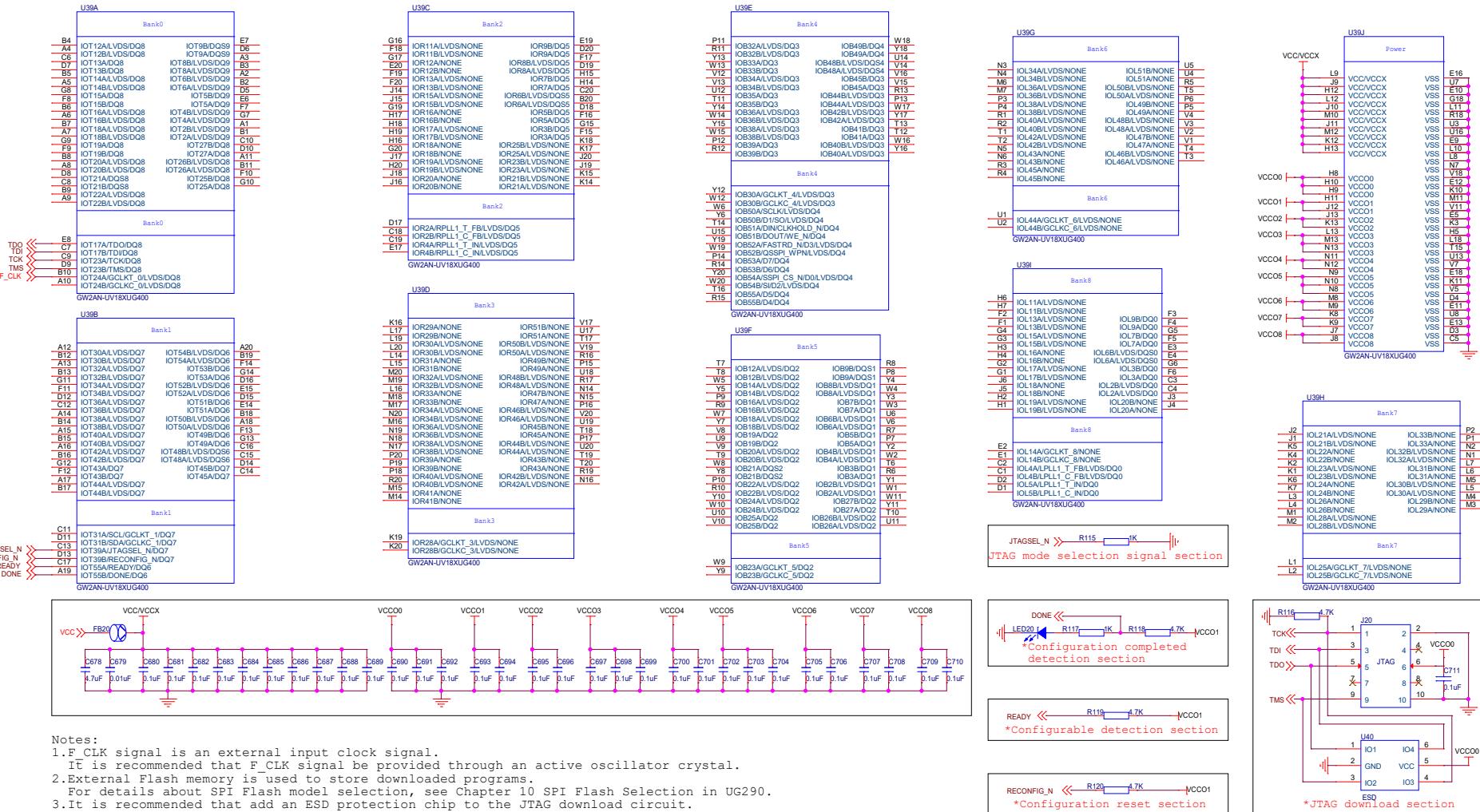


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| Title | | GOWIN Minimum System Diagram | | |
|--------|-----------------------|------------------------------|----|-------|
| Size | Document Number | | | Rev |
| Custom | GW2AN-UV18XUG332 | | | 2.0 |
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Notes:

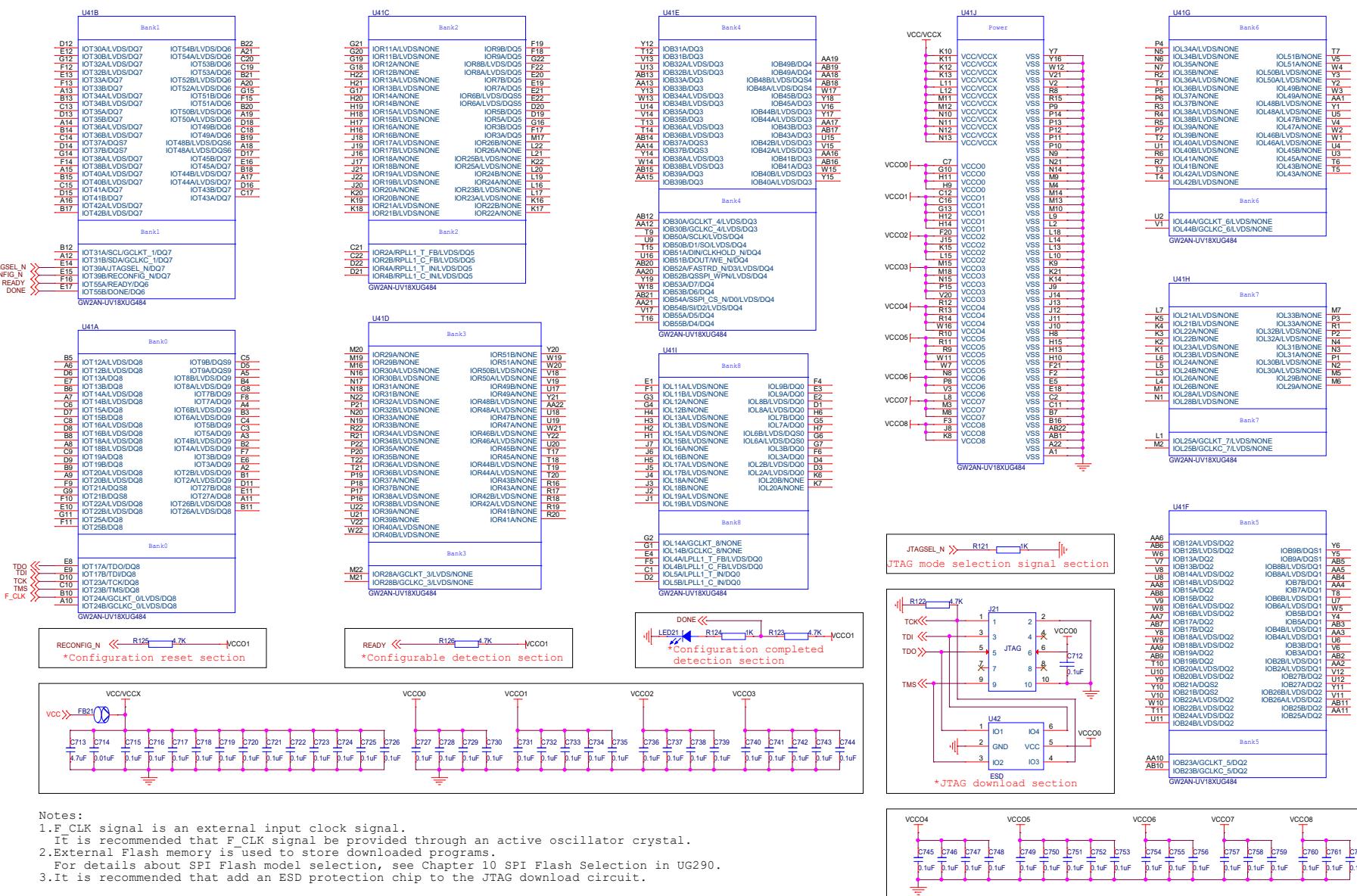
1 E CLK signal is an external input clock signal

1.F CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal.

It is recommended that F_CKE signal be provided through an External Flash memory is used to store downloaded programs

For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.

For details about SFI flash model selection, see Chapter 10 SFI Flash Selection. It is recommended that add an ESD protection chip to the JTAG download circuit.



Notes:

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 It is recommended that F_CLK signal be provided through an active oscillator crystal.

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 For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.

3.It is recommended that add an ESD protection chip to the JTAG download circuit.