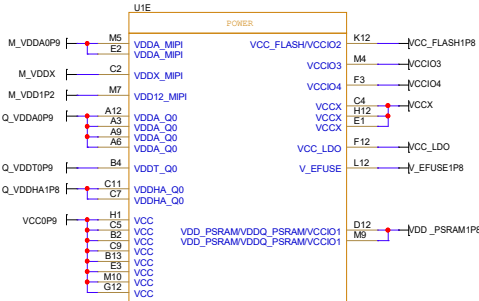
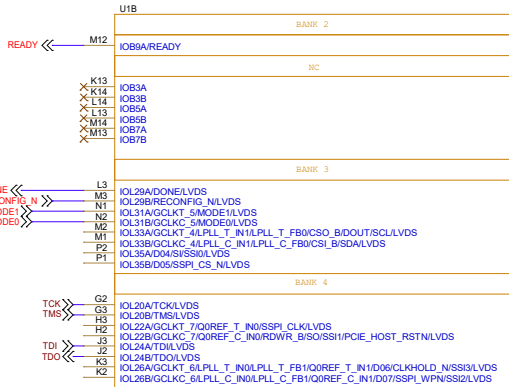


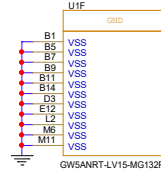
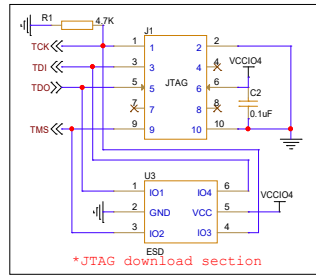
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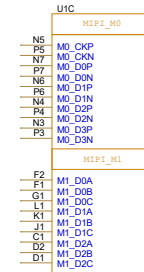
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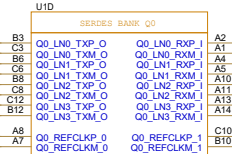
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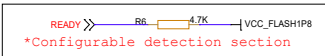
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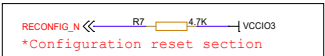
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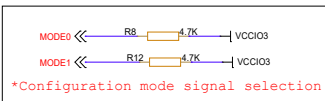
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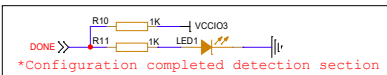
*Configurable detection section



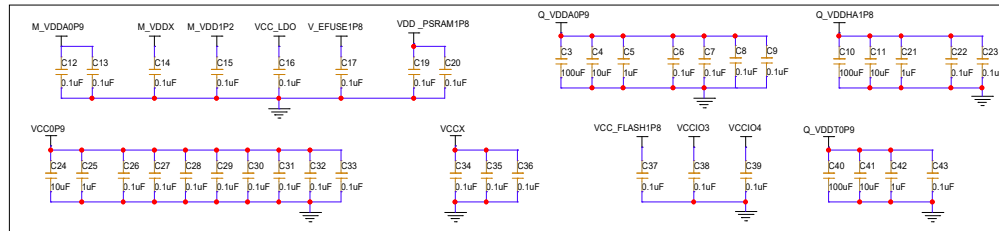
*Configuration reset section



*Configuration mode signal selection



*Configuration completed detection section



Notes:
1.F CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal.
2.It is recommended that add an ESD protection chip to the JTAG download circuit.
3.VCC core voltage requires a large current, so it is recommended to supply power separately.
4.The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG720,
Arora V 15K FPGA Products Programming and Configuration Guide.