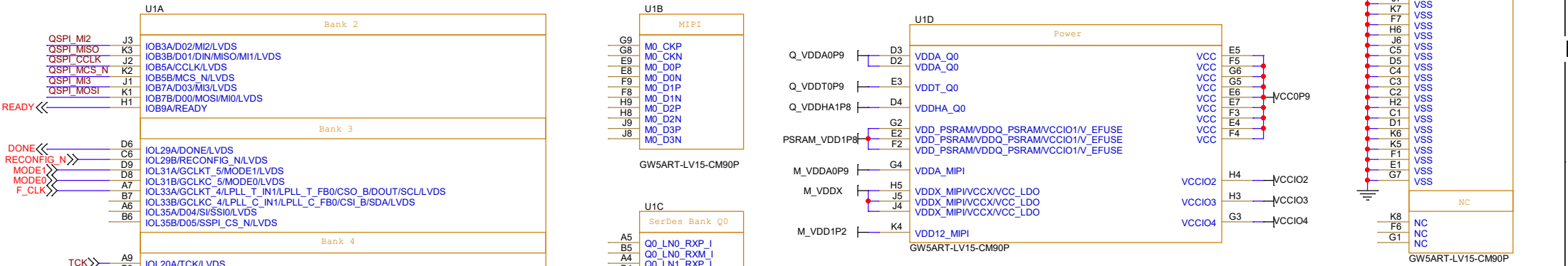
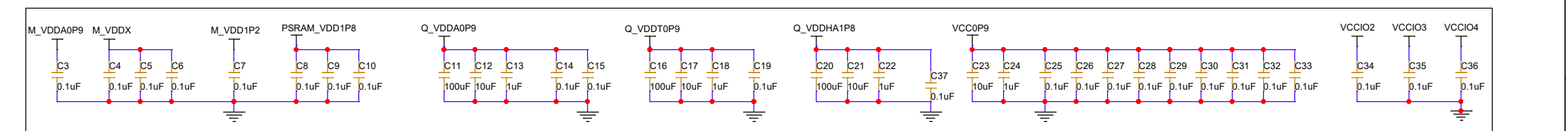
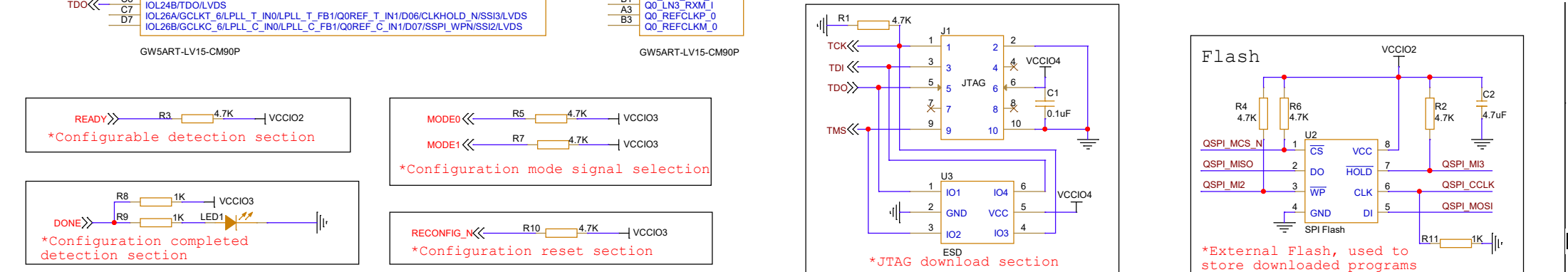


# GW5ART-LV15CM90P



K5, K6, F1, E1 must be shorted together



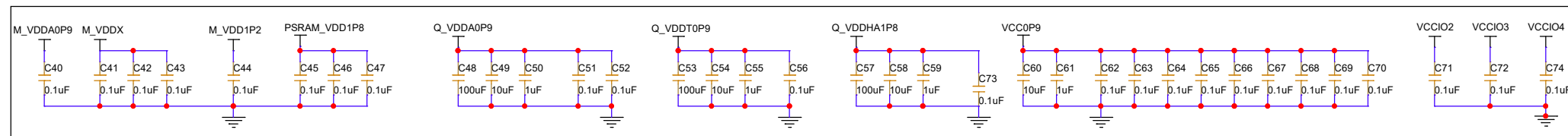
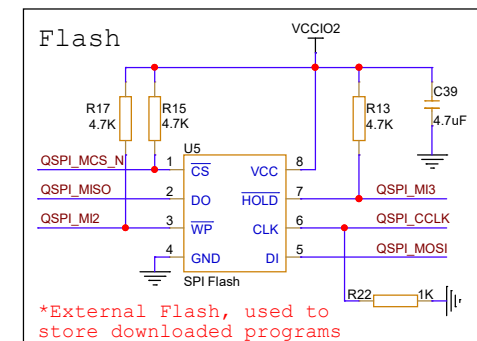
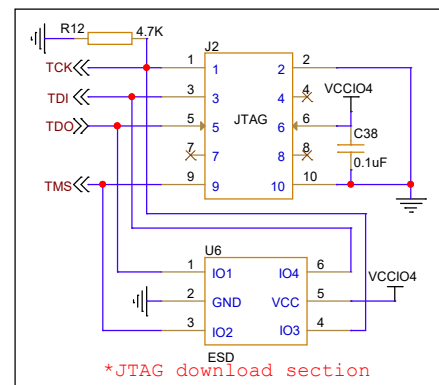
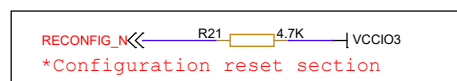
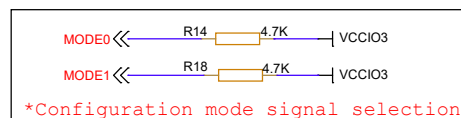
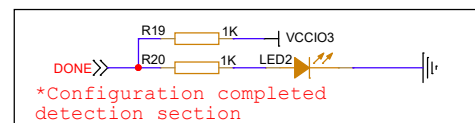
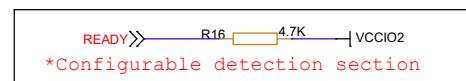
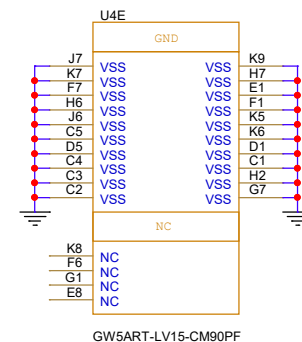
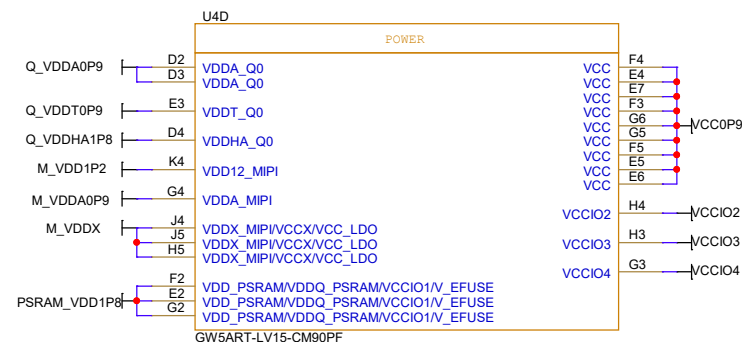
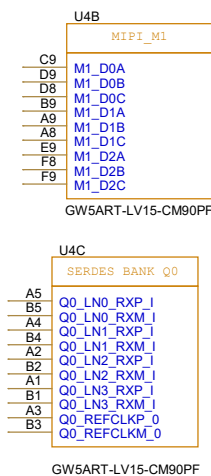
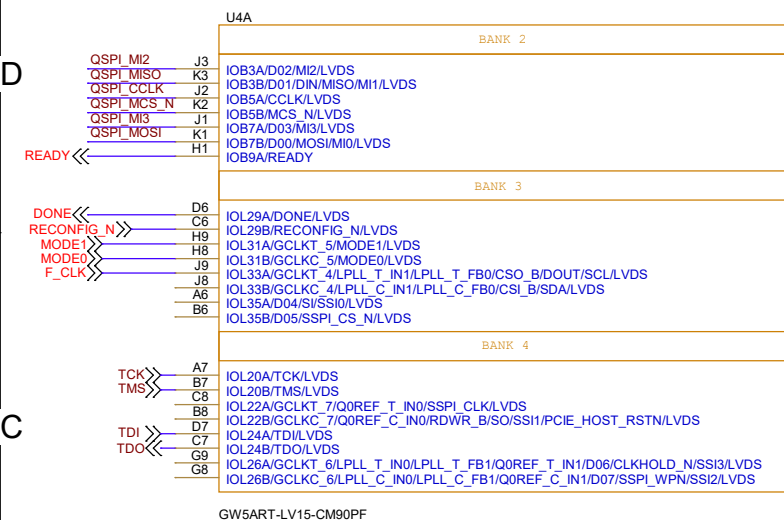
Notes:

- 1.F CLK signal is an external input clock signal. It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.

For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG720, Arora V 15K FPGA Products Programming and Configuration Guide.

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW5ART-LV15CM90P	1.3
Date:	Friday, August 09, 2024	Sheet 1 of 3

5  
***GW5ART-LV15CM90PF***

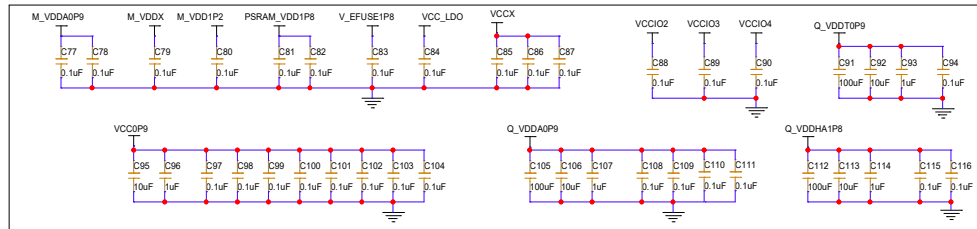
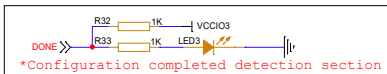
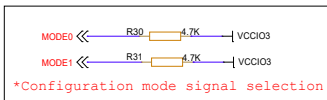
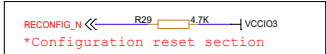
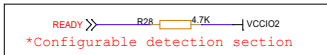
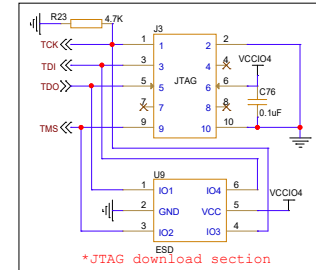
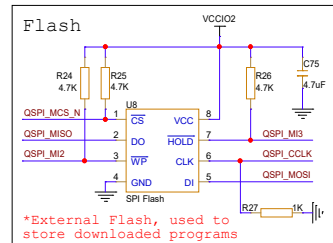
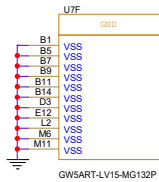
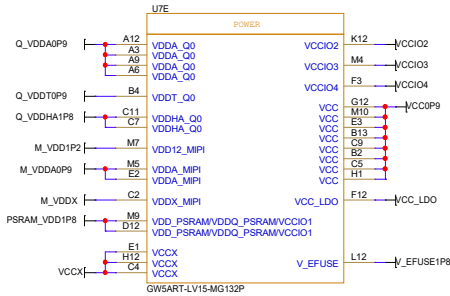
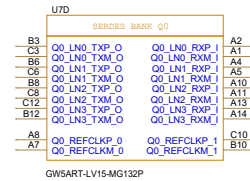
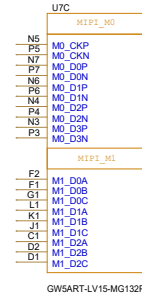
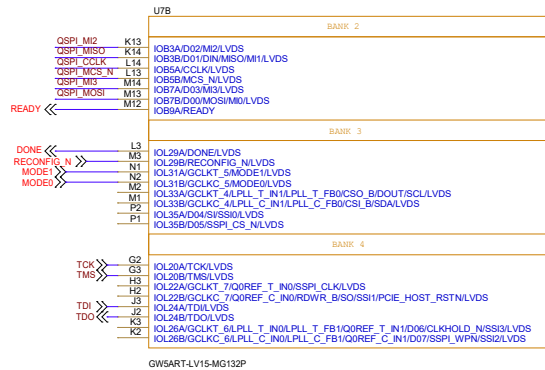
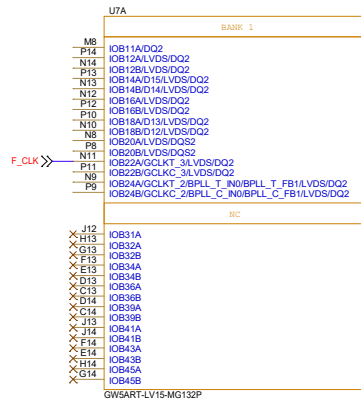


Notes:

- 1.F\_CLK signal is an external input clock signal. It is recommended that F\_CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs. For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG720, Arora 15K FPGA Products Programming and Configuration V Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal. For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG720, Arora V 15K FPGA Products Programming and Configuration Guide.

Title			
GOWIN Minimum System Diagram			
Size B	Document Number GW5ART-LV15CM90PF		Rev 1.3
Date:	Friday, August 09, 2024	Sheet	2 of 3

***GW5ART-LV15MG132P***



Notes:

- 1.F CLK signal is an external input clock signal.
  - It is recommended that F CLK signal be provided through an active oscillator crystal.
  - 2.External Flash memory is used to store downloaded programs.
  - For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG720, Arora 15K FPGA Products Programming and Configuration V Guide .
  - 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
  - 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
  - 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
- For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG720, Arora V 15K FPGA Products Programming and Configuration Guide.