

Notes.

- Notes:**

 - 1.FCLK signal is an external input clock signal.
 - 2.It is recommended that FCLK signal be provided through an active oscillator crystal.
 - 3.External Flash memory is used to store downloaded programs.
 - 4.For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
 - 5.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
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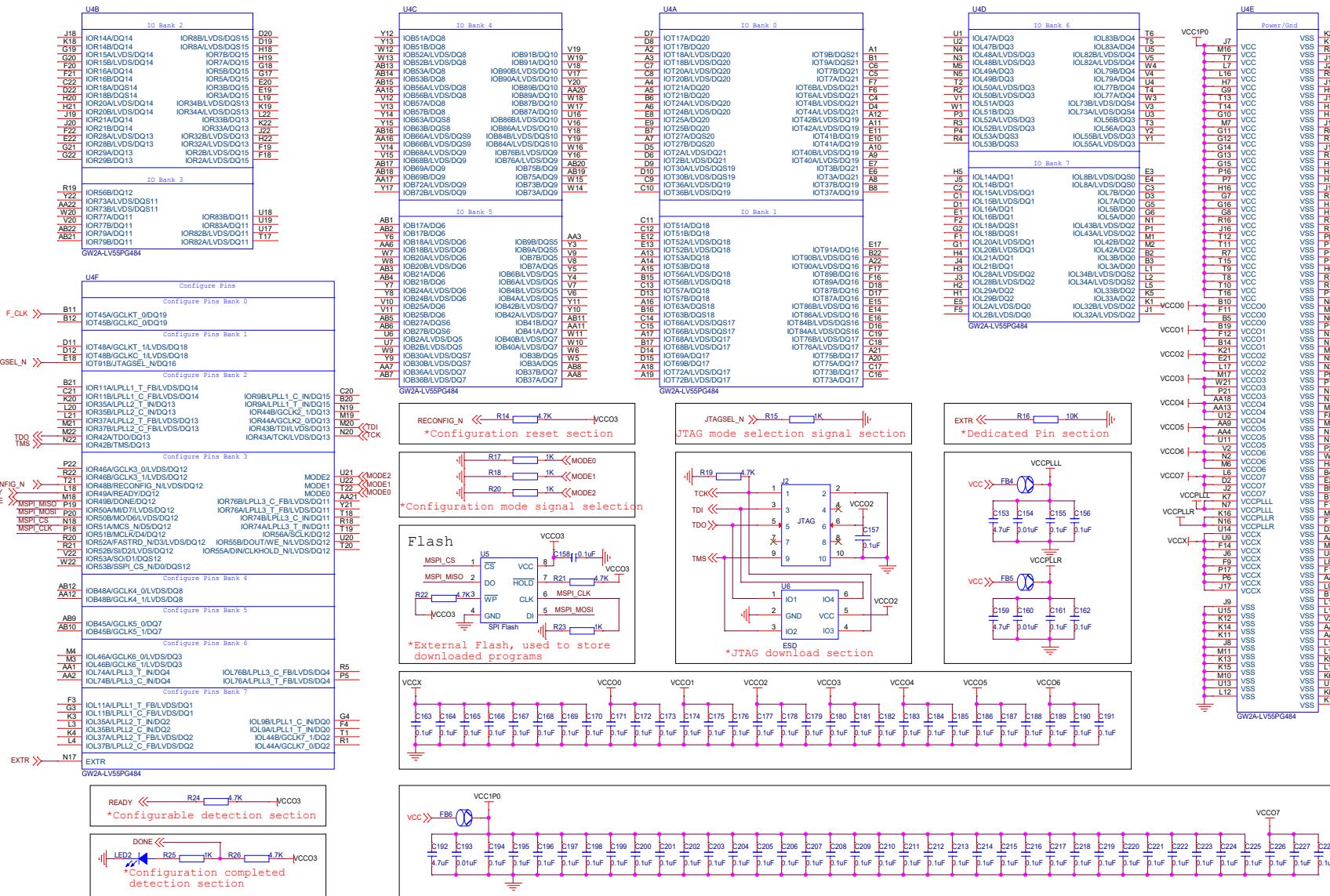
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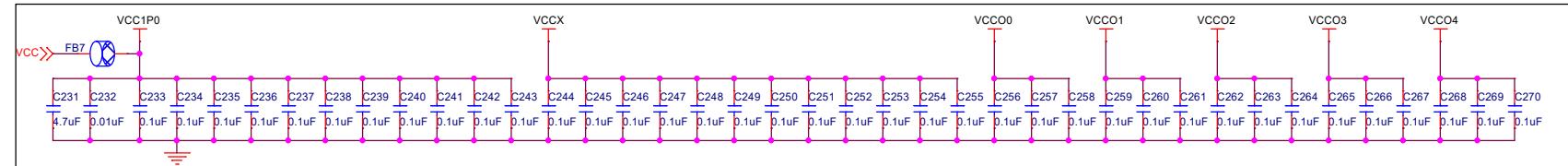
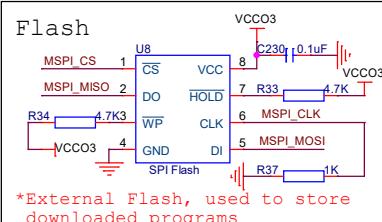
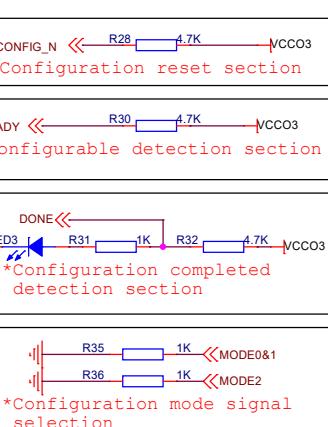
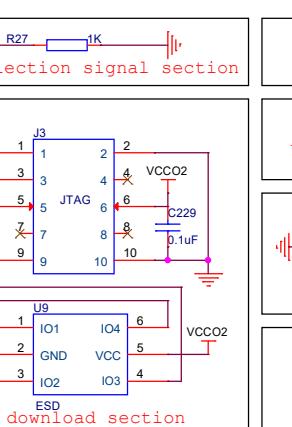
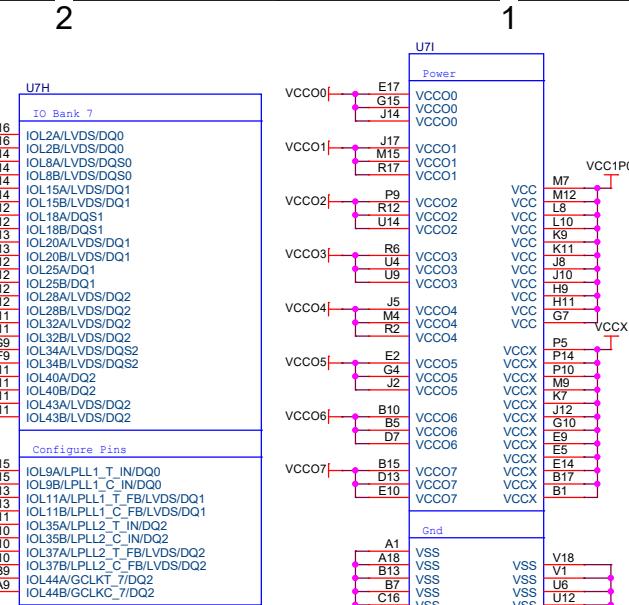
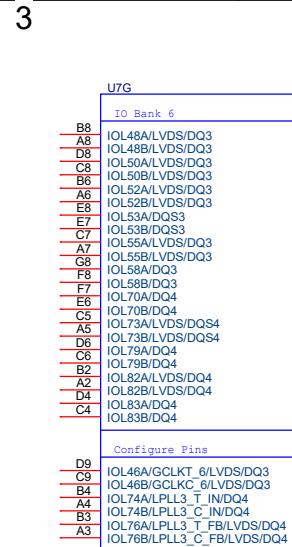
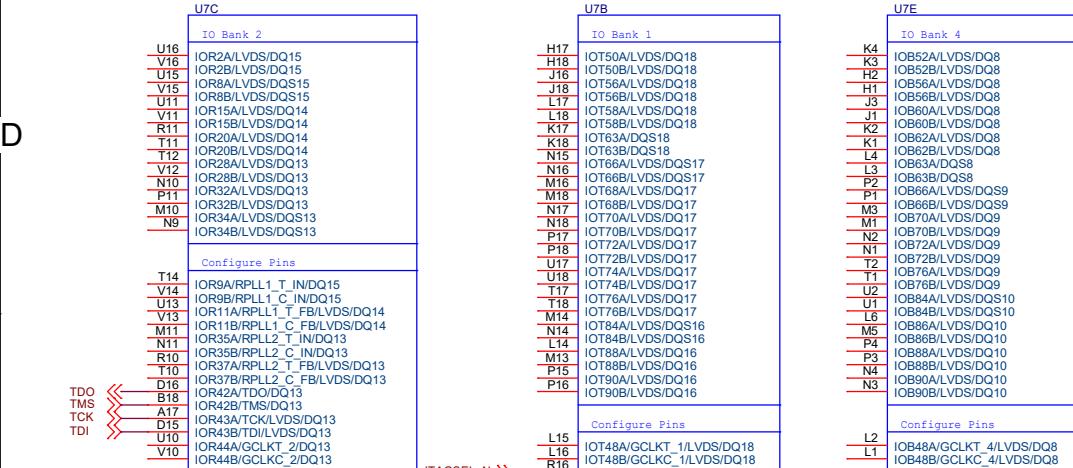
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A

**Notes:**

- F CLK signal is an external input clock signal. It is recommended that F_CLK signal be provided through an active oscillator crystal.
- External Flash memory is used to store downloaded programs. For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
- It is recommended that add an ESD protection chip to the JTAG download circuit.

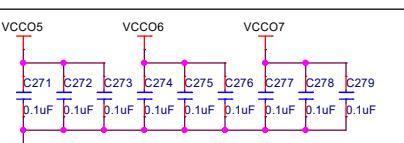
GOWIN Minimum System Diagram		
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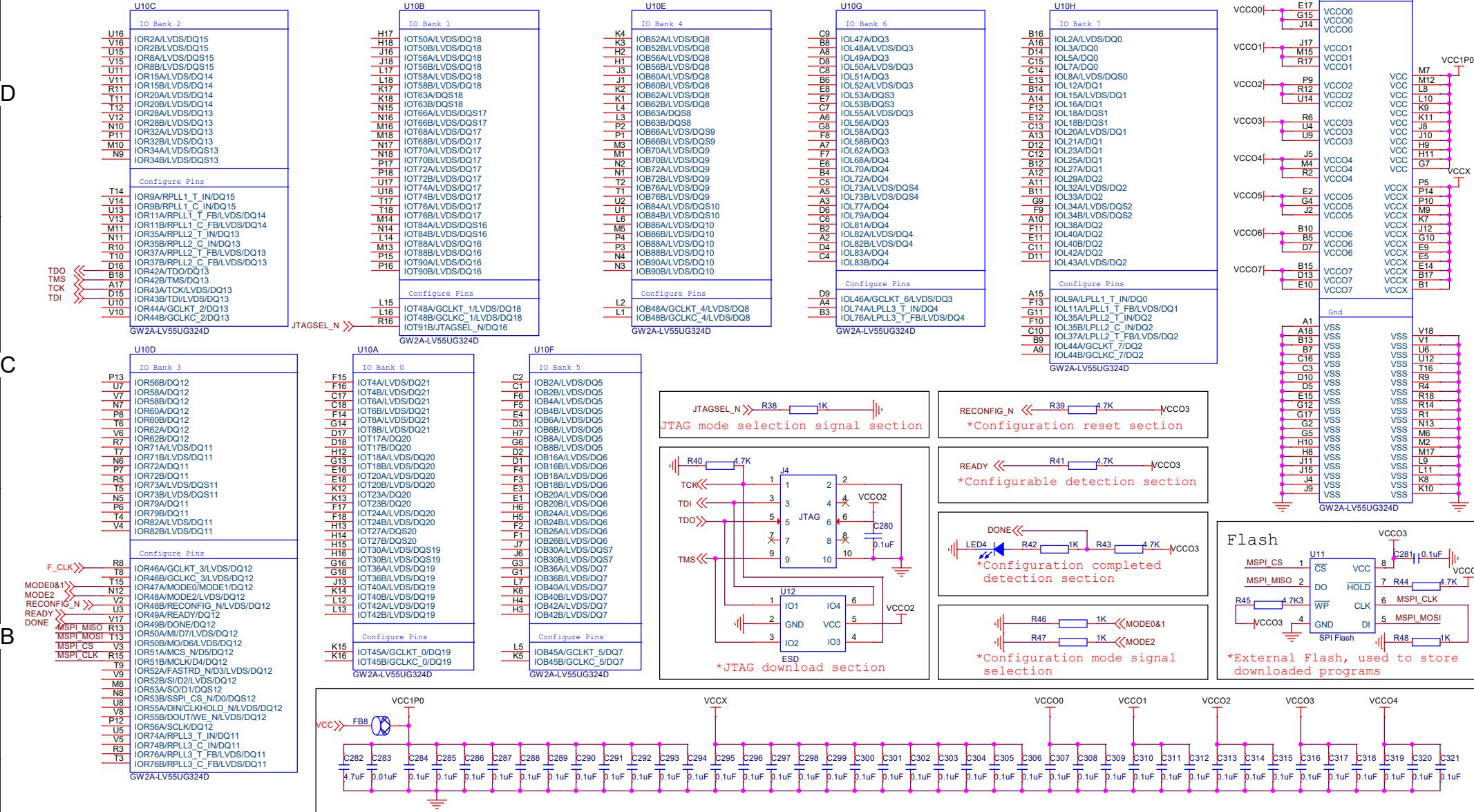


Notes

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For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
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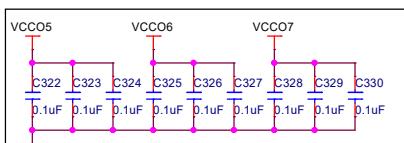




Notes

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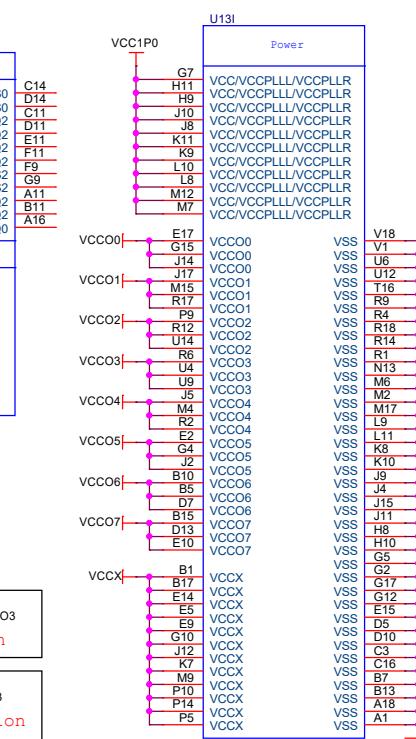
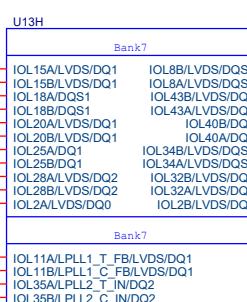
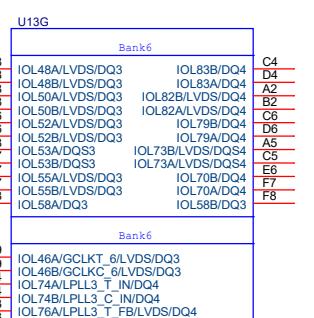
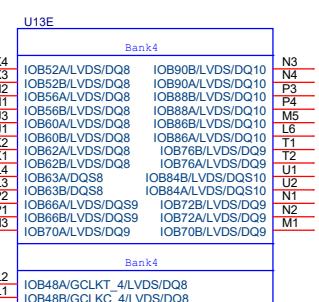
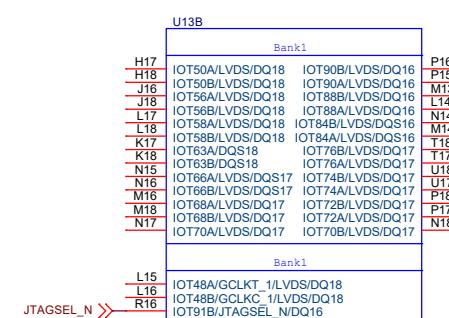
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A



JTAGSEL_N >> R49 1K |||
*JTAG mode selection signal section

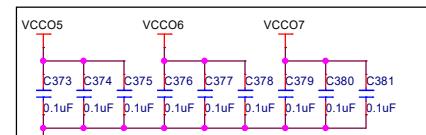
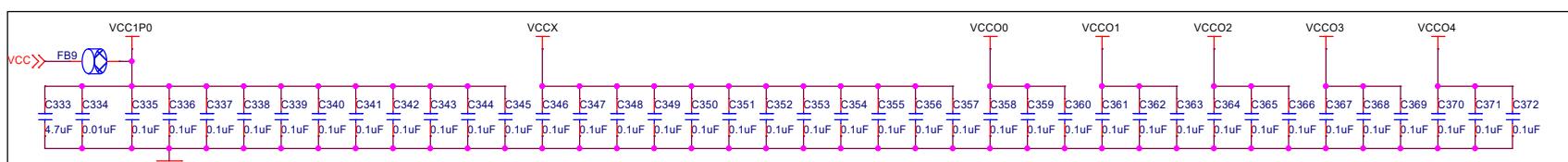
RECONFIG_N << R50 4.7K ||| VCC03
*Configuration reset section

READY << R52 4.7K ||| VCC03
*Configurable detection section

DONE << LED5 R53 1K ||| R54 4.7K ||| VCC03
*Configuration completed detection section

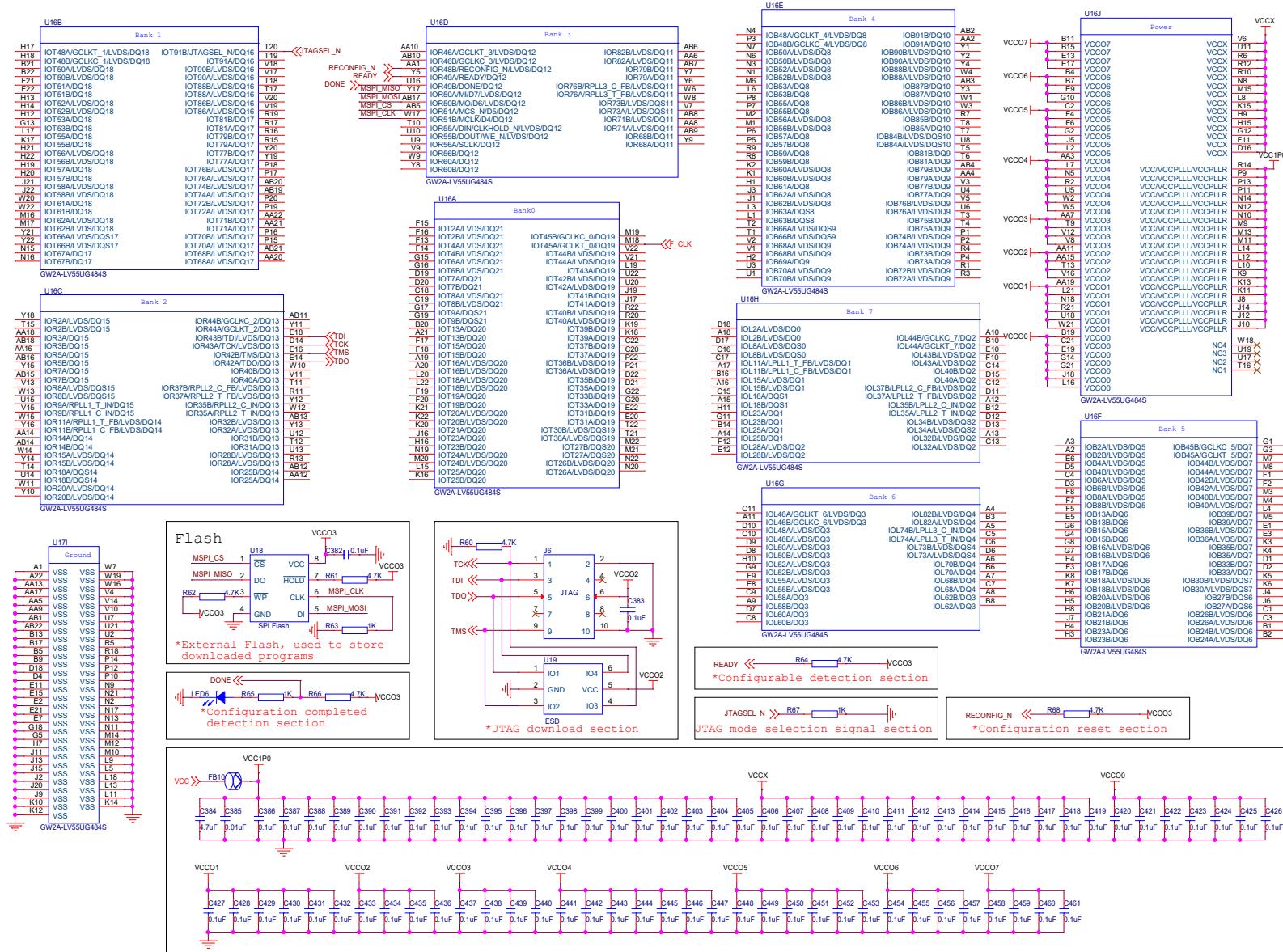
MODE0 R57 1K ||| MODE0
MODE2 R58 1K ||| MODE2
*Configuration mode signal selection

Flash
VCC03
U14 CS 8 C332 0.1uF ||| VCC03
MSPI_CS 7 R55 4.7K |||
MSPI_MISO 6 R56 4.7K |||
R56 WP CLK 4 SPI Flash DI 5 MSPI_MOSI
GND R57 1K ||| R58 1K ||| R59 1K
*External Flash, used to store downloaded programs



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