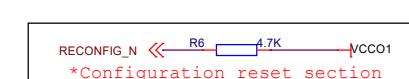
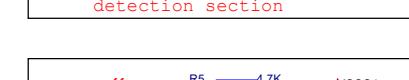
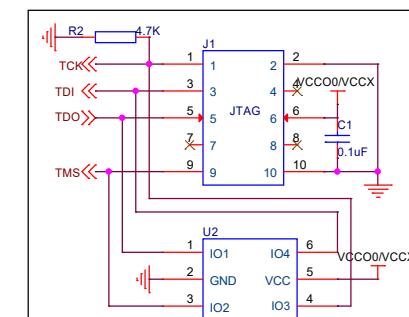
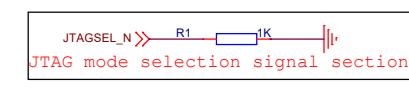
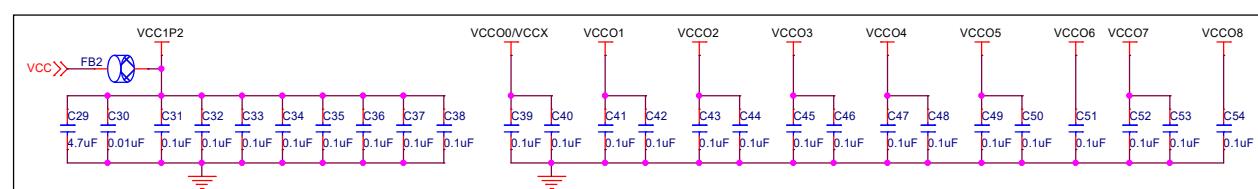
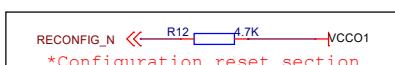
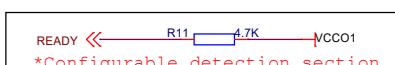
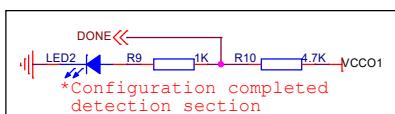
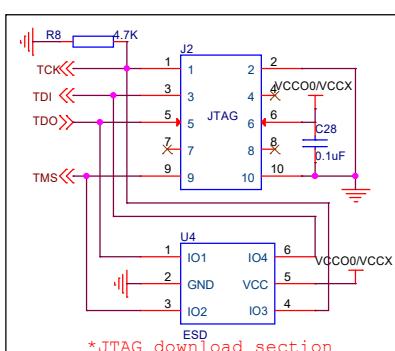
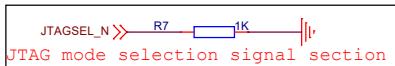
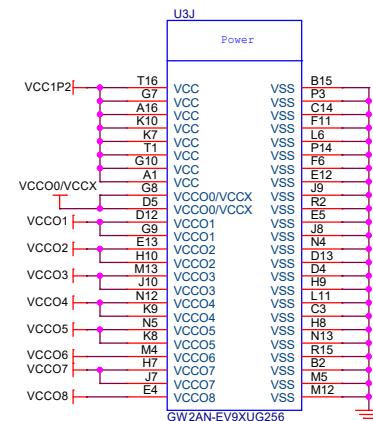
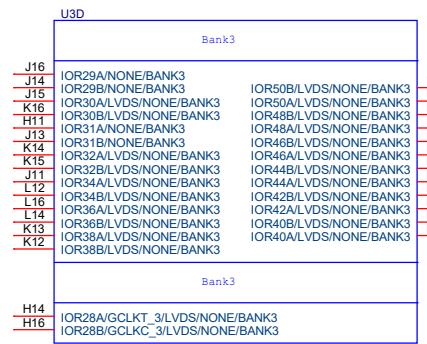
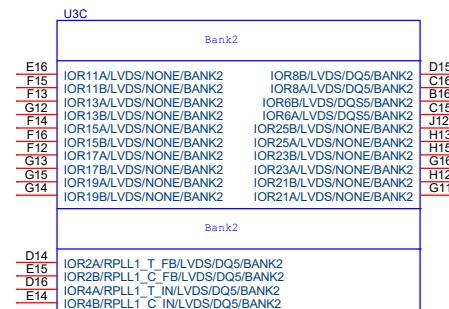
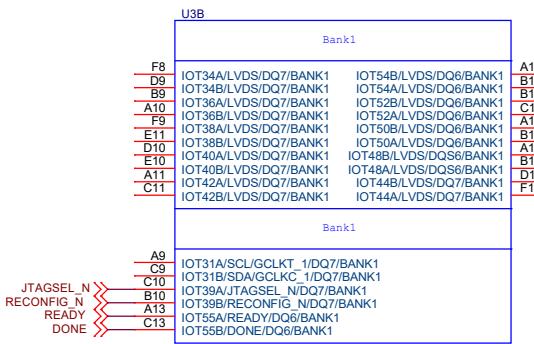


**Notes:**

1. F CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal.
2. External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
3. It is recommended that add an ESD protection chip to the JTAG download circuit.

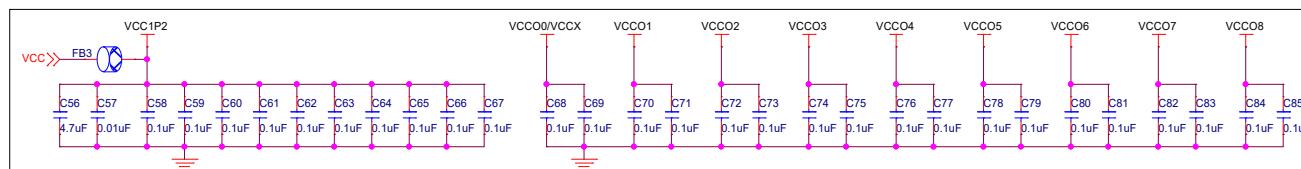
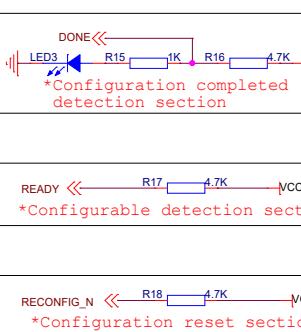
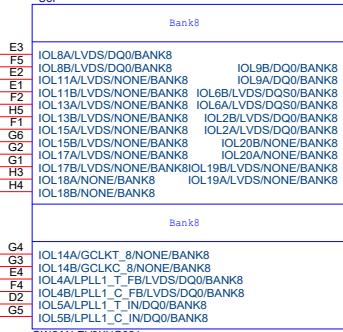
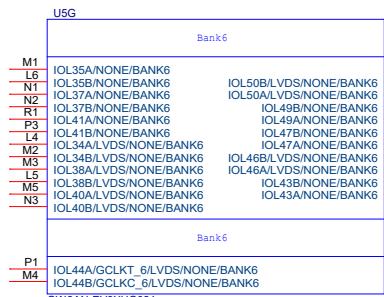
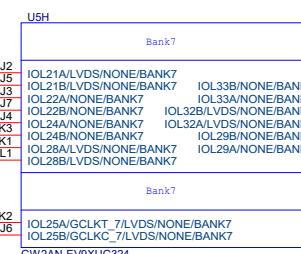
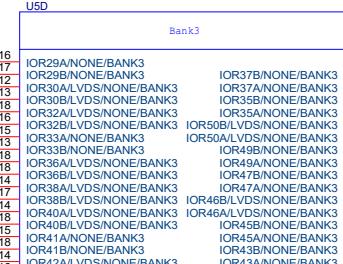
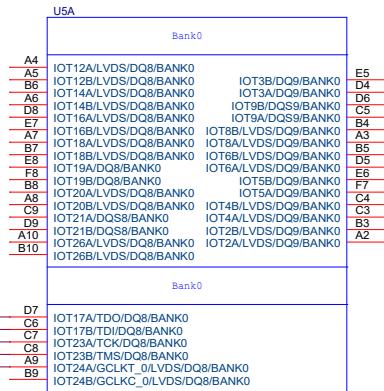
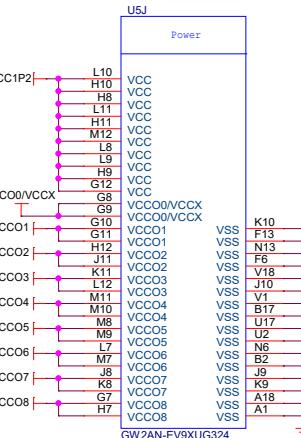
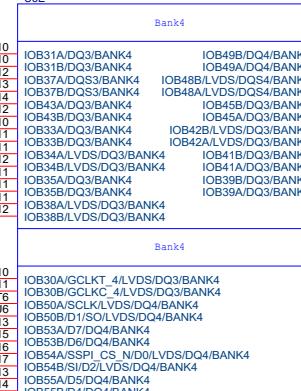
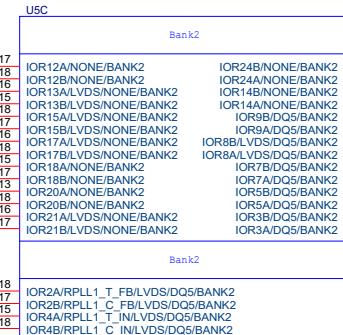
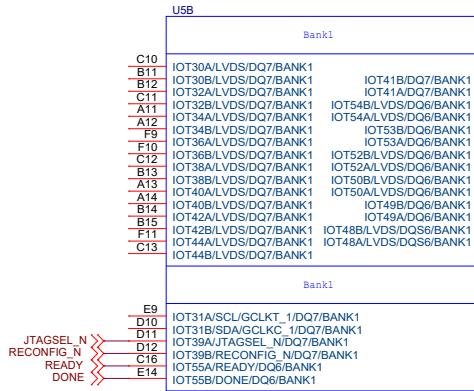


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**Notes:**

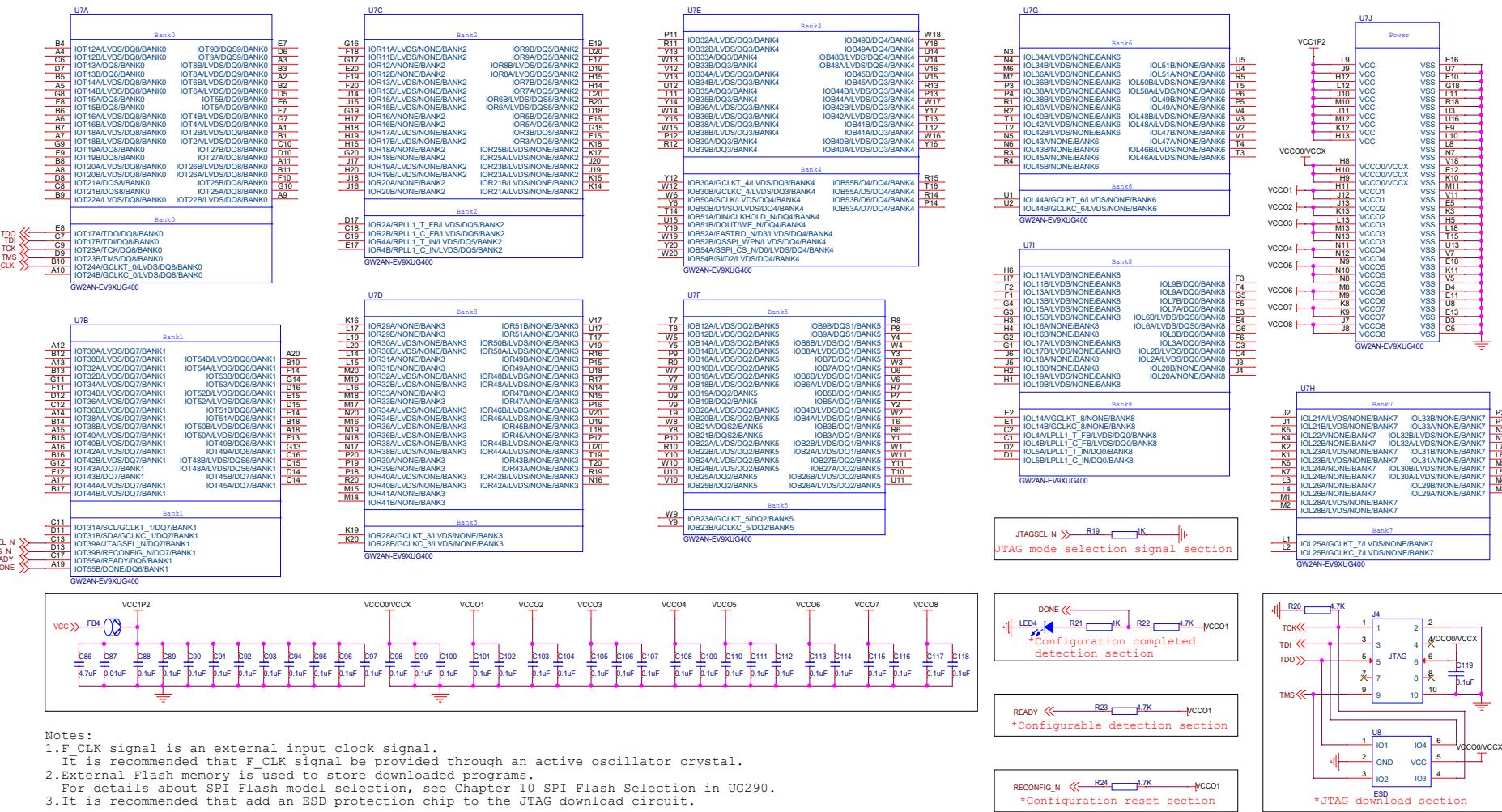
1. F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
3. It is recommended that add an ESD protection chip to the JTAG download circuit.

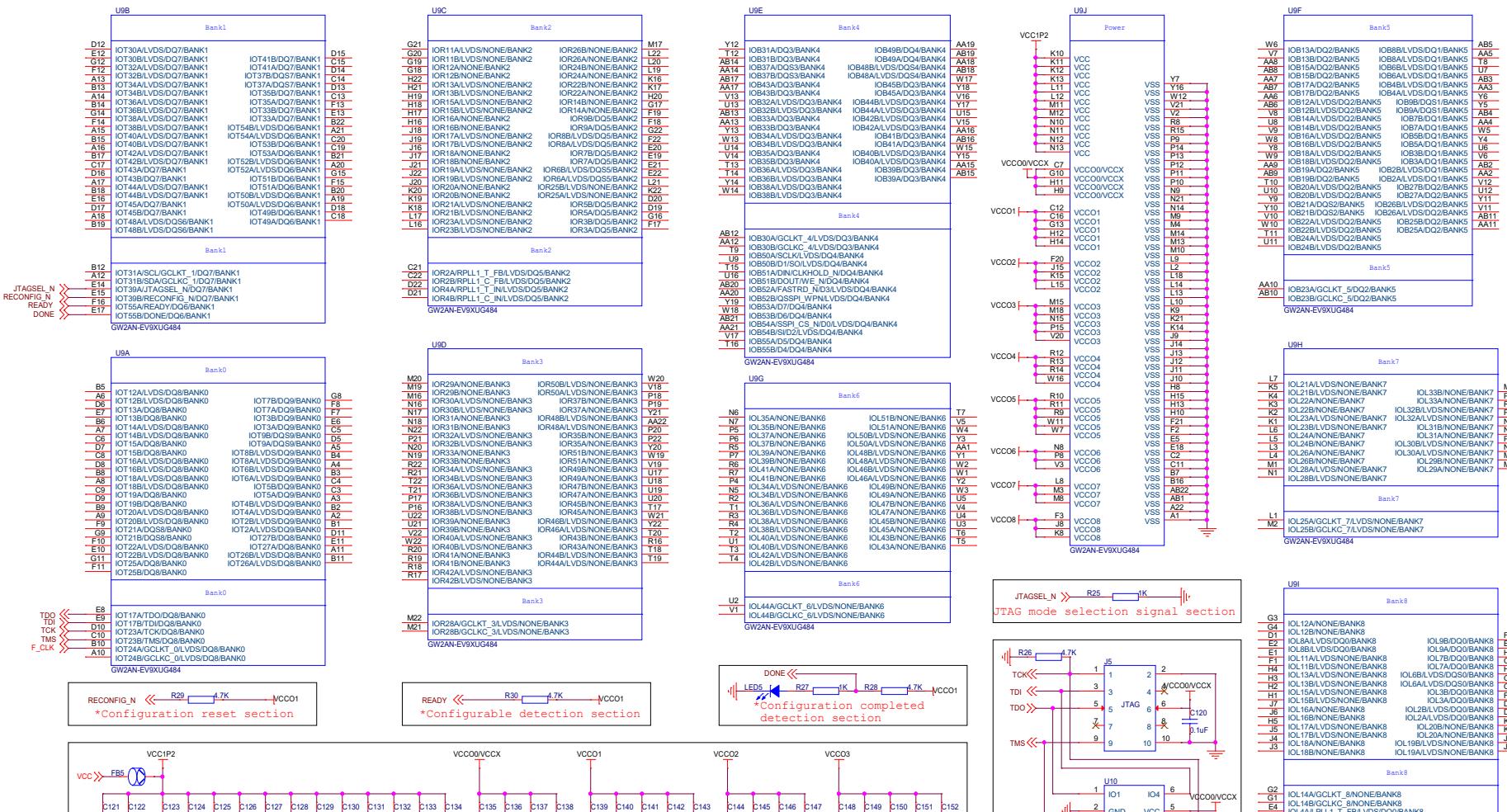
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Size	A3	GW2AN-EV9XUG256	2.0	
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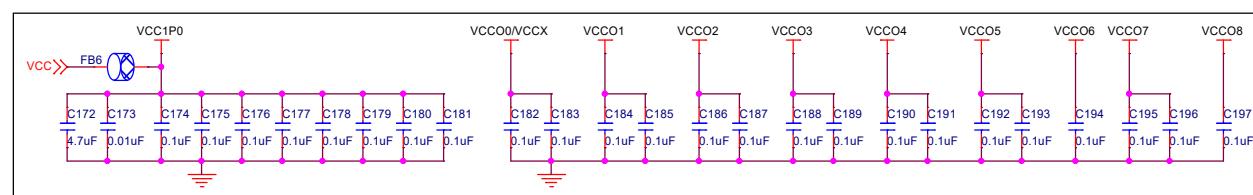
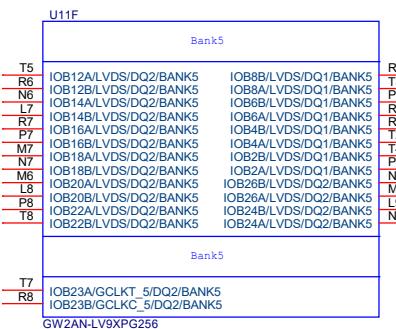
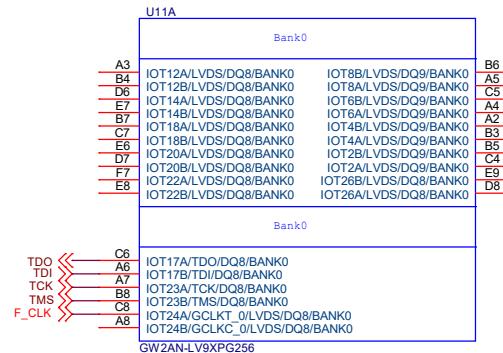
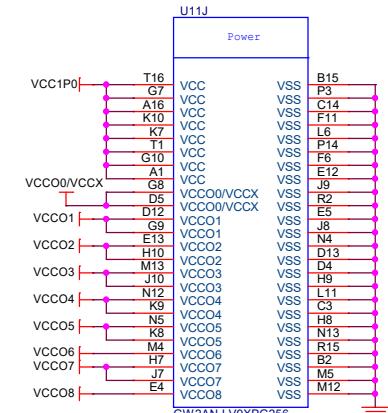
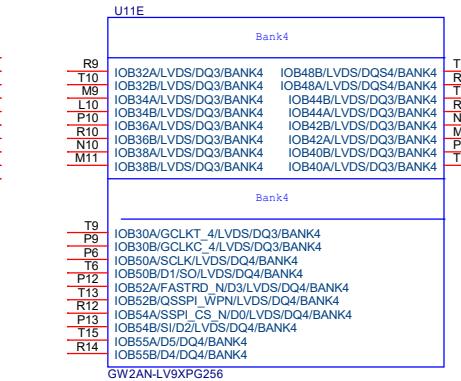
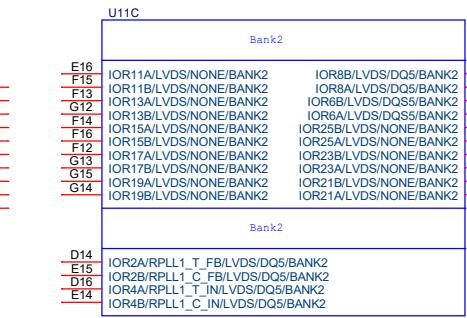
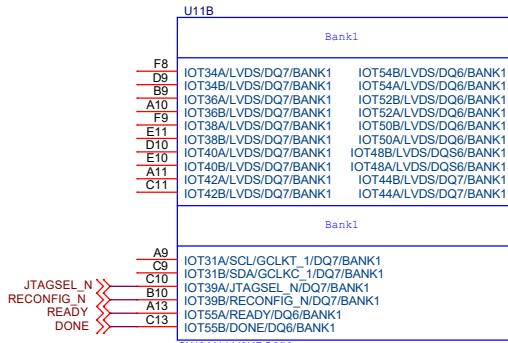


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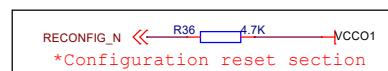
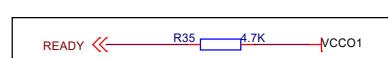
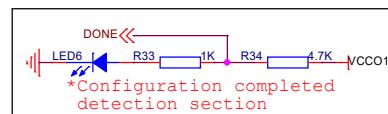
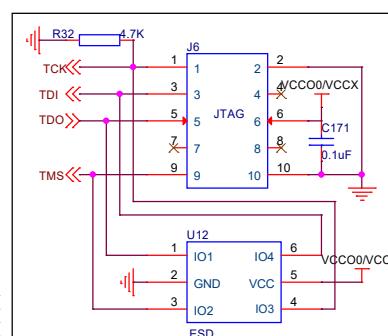
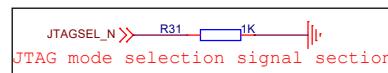
1. F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
3. It is recommended that add an ESD protection chip to the JTAG download circuit.



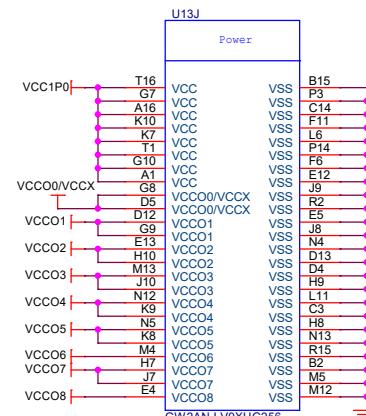
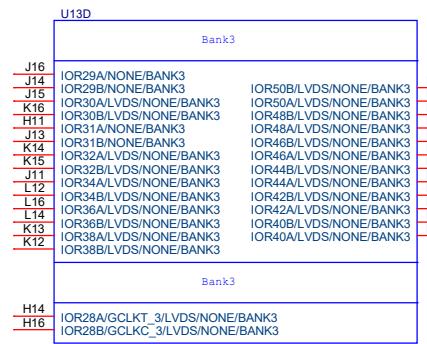
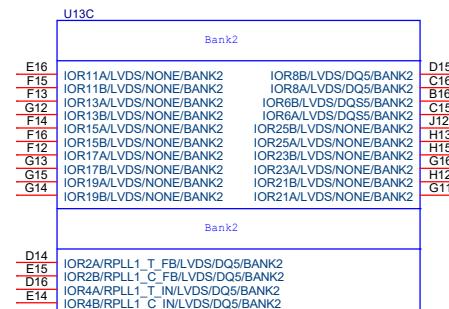
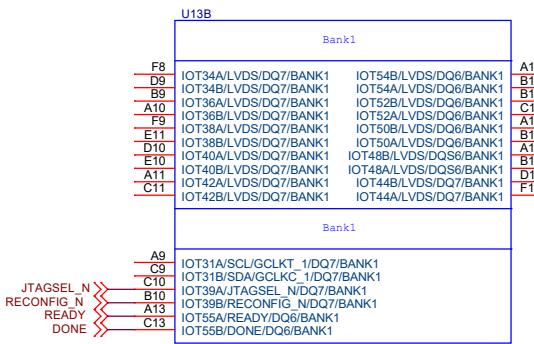


**Notes:**

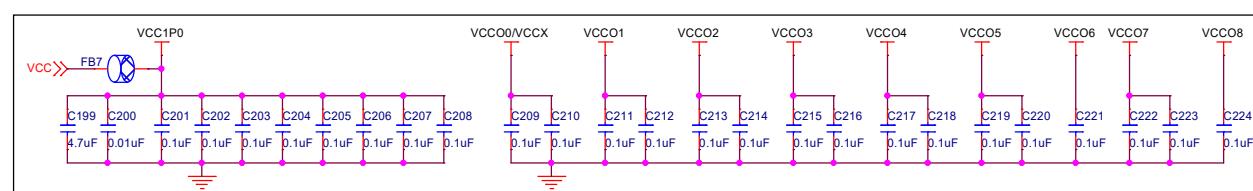
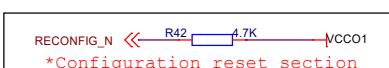
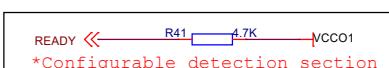
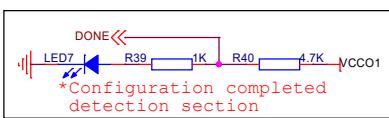
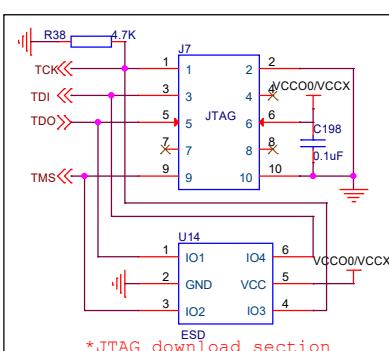
- F CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal.
- External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
- It is recommended that add an ESD protection chip to the JTAG download circuit.



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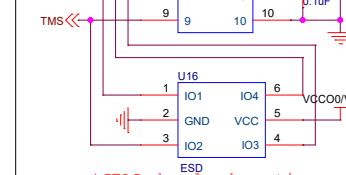
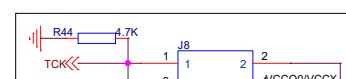
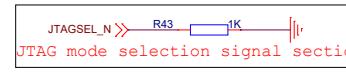
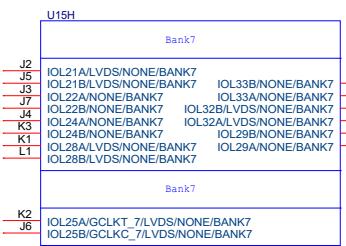
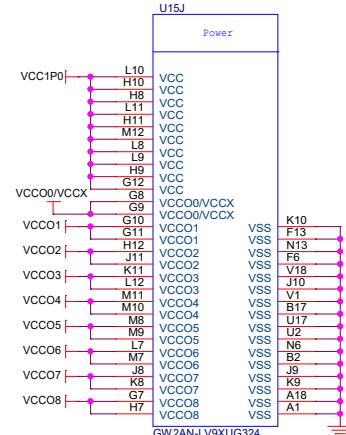
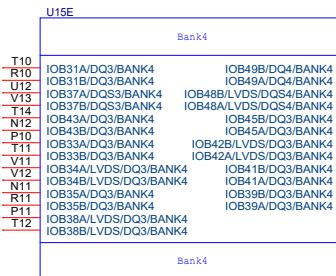
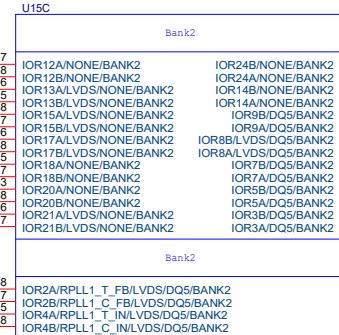
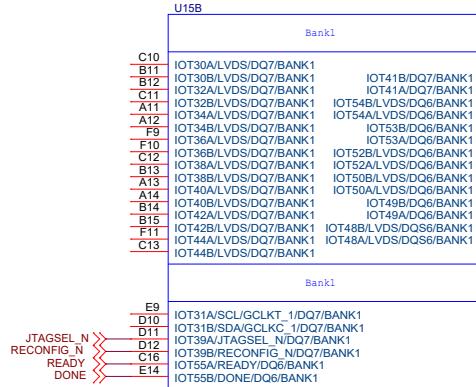
JTAGSEL_N → R37 → 1K → JTAG mode selection signal section



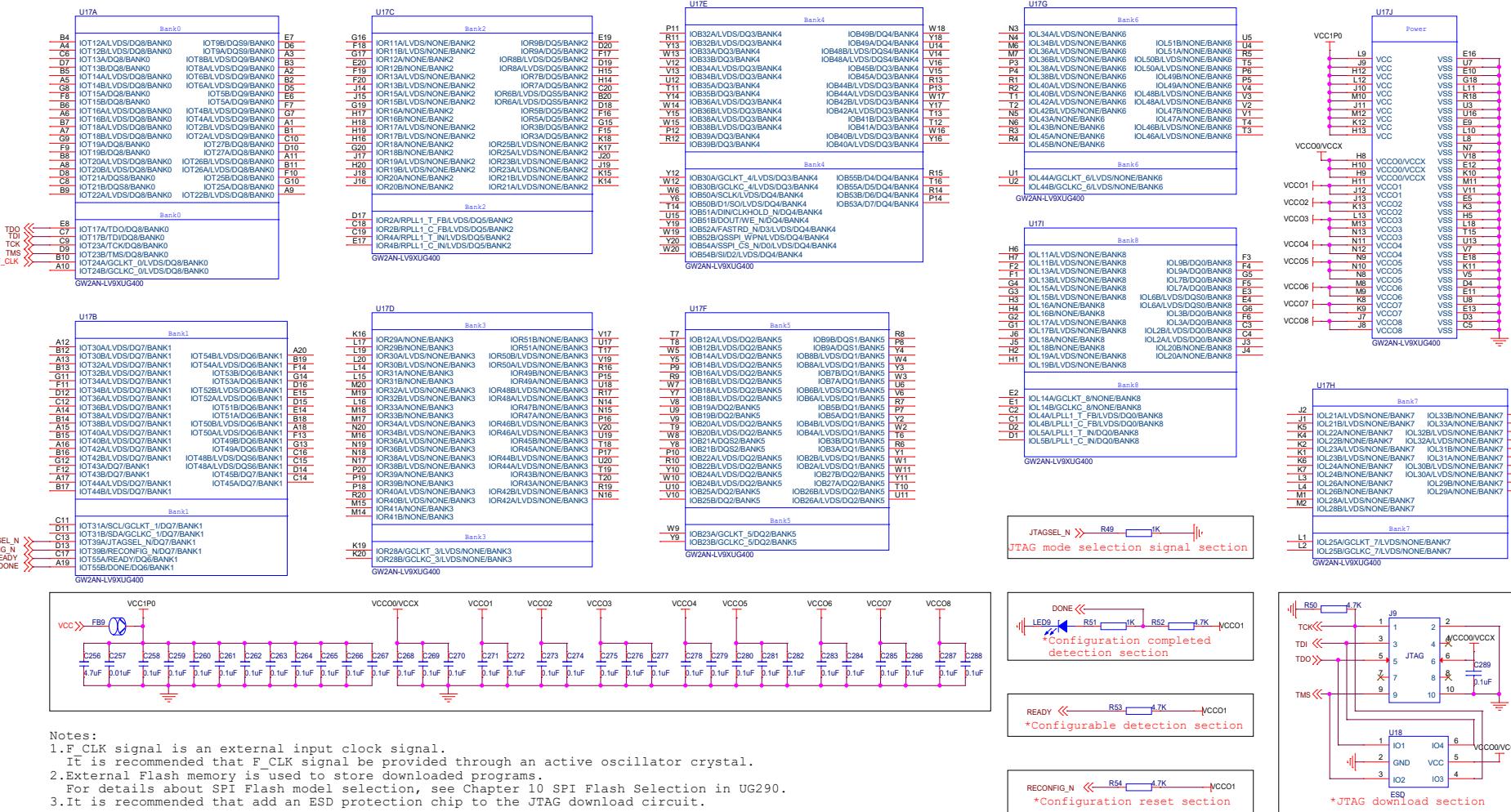
Notes:

1. F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
3. It is recommended that add an ESD protection chip to the JTAG download circuit.

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GOWIN Minimum System Diagram	
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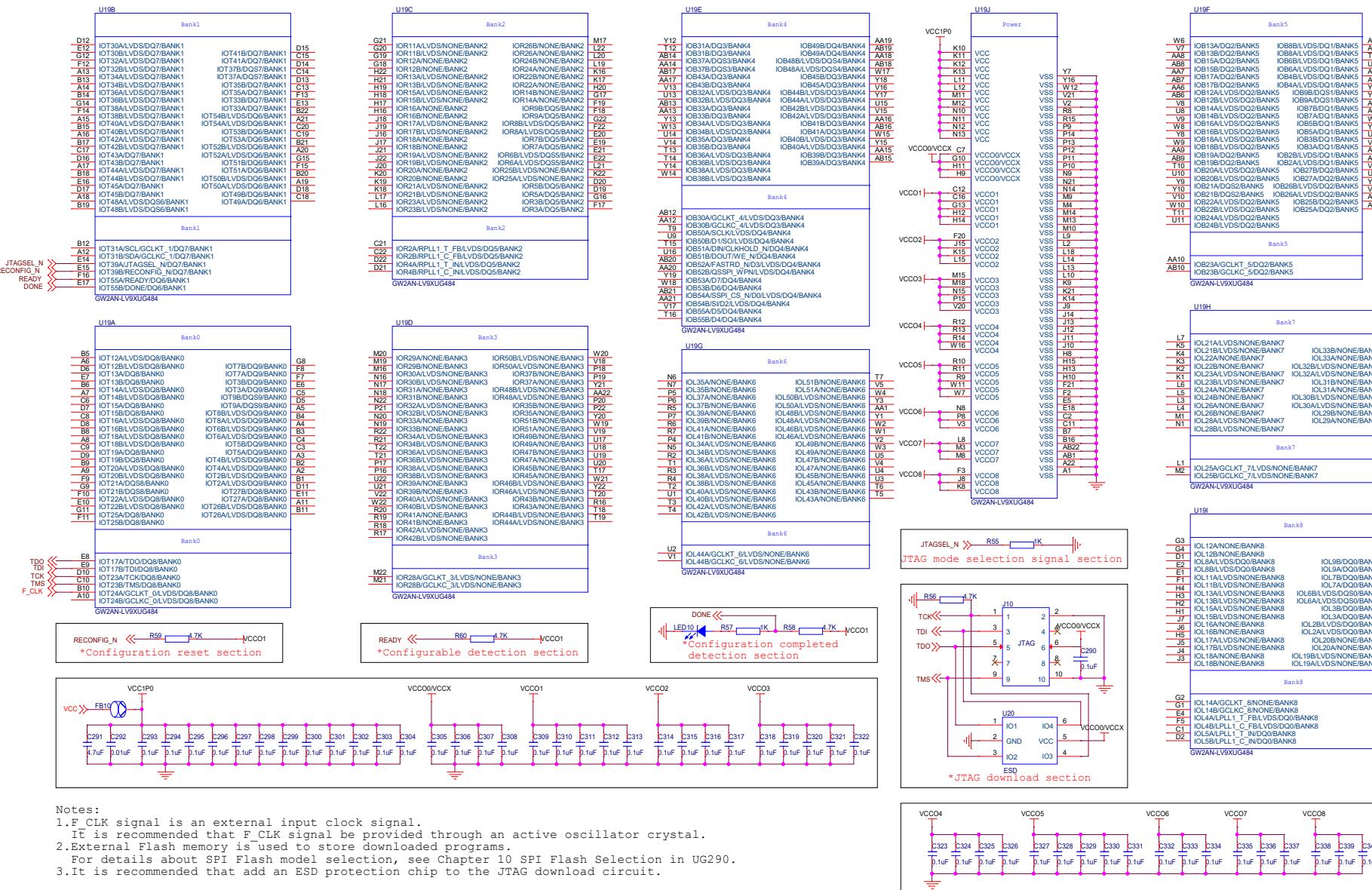
**Notes:**

1. F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
3. It is recommended that add an ESD protection chip to the JTAG download circuit.

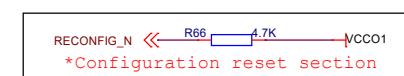
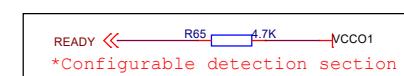
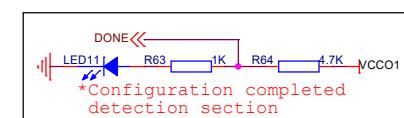
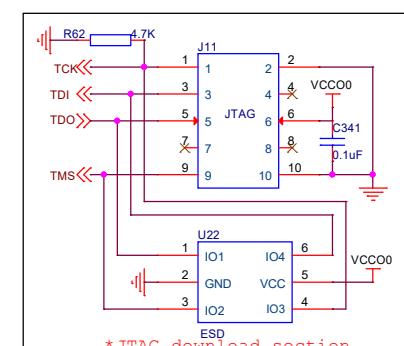
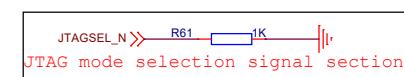
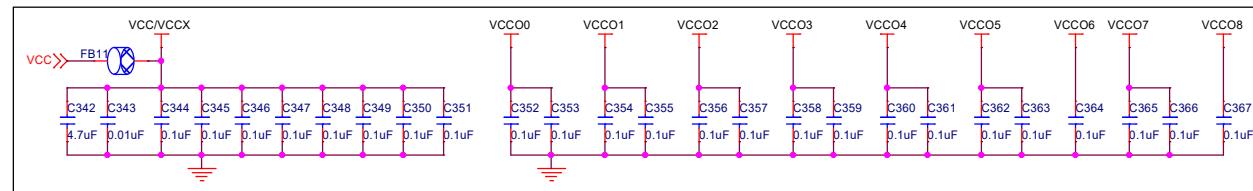
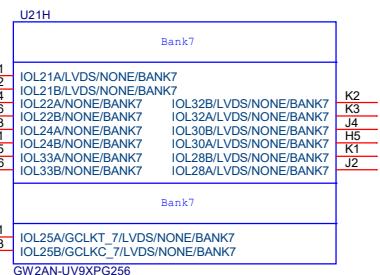
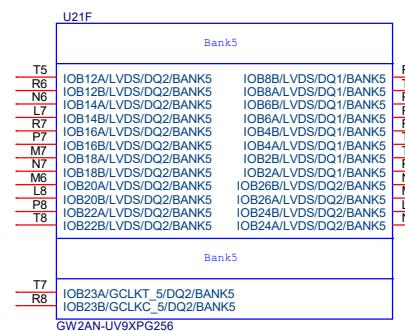
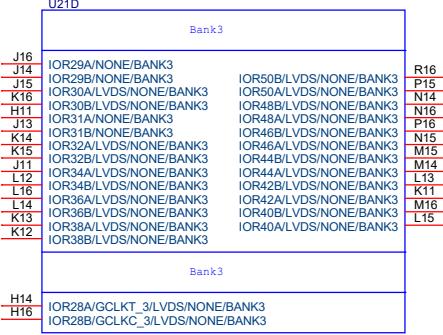
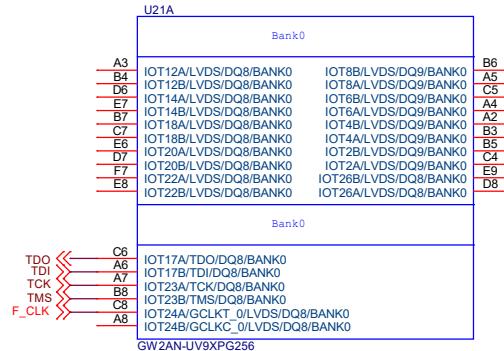
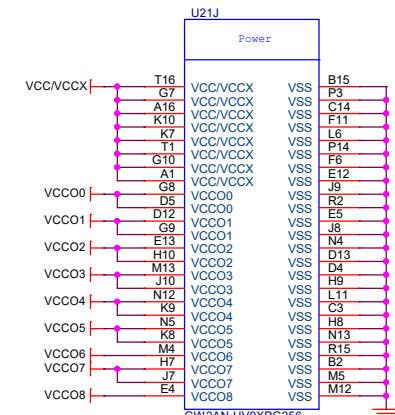
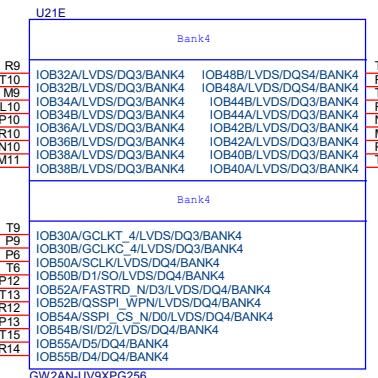
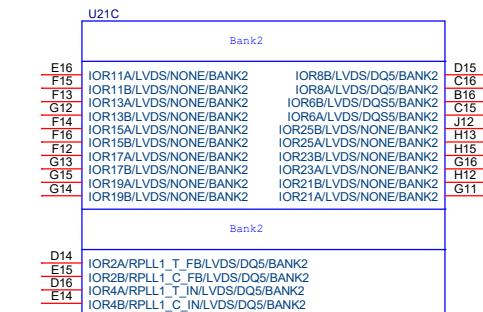
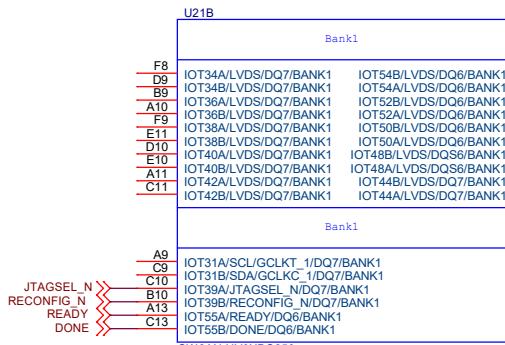


Notes:

1. F CLK signal is an external input clock signal.
- It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. External Flash memory is used to store downloaded programs.
- For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
3. It is recommended that add an ESD protection chip to the JTAG download circuit.

**Notes:**

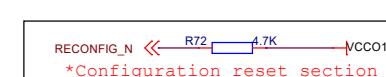
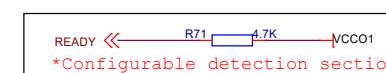
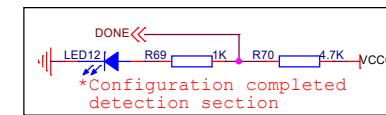
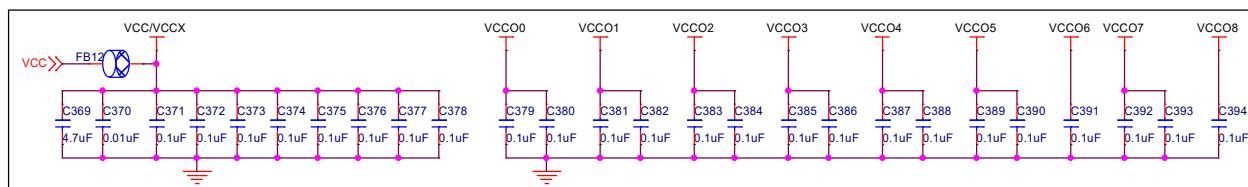
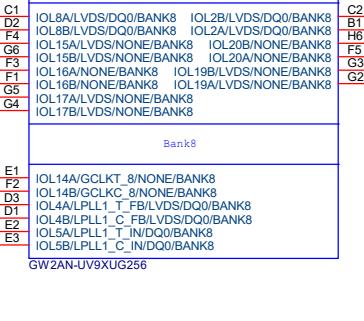
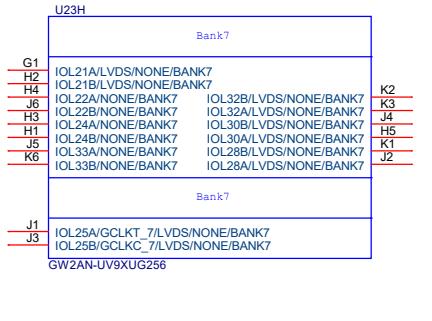
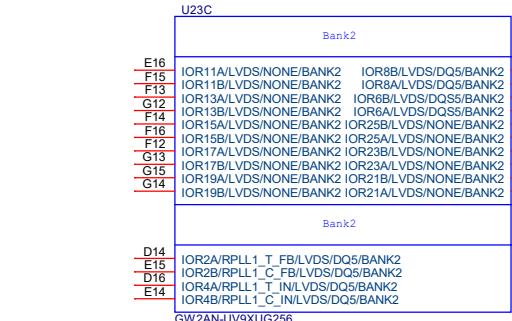
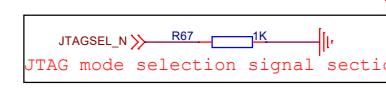
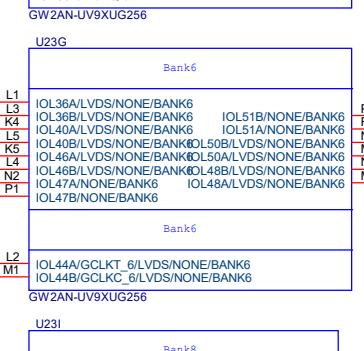
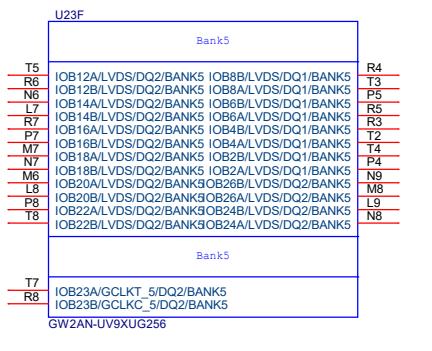
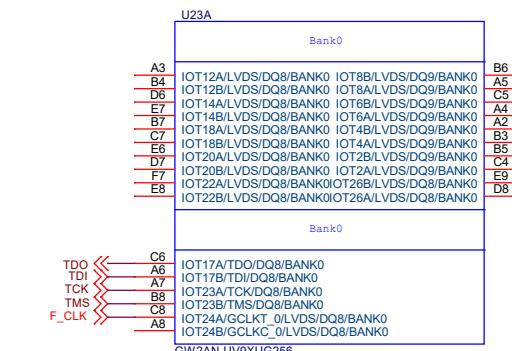
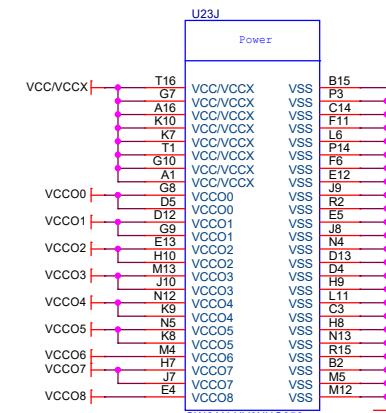
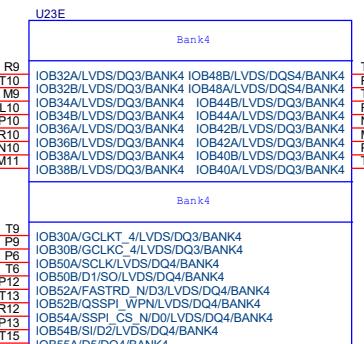
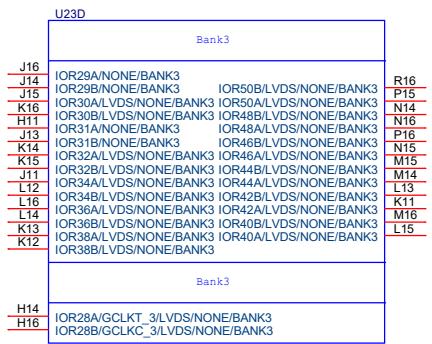
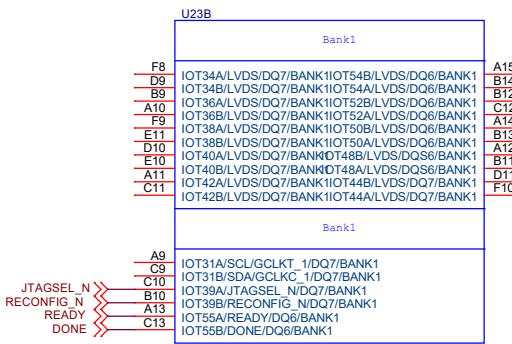
- F CLK signal is an external input clock signal.
- It is recommended that F CLK signal be provided through an active oscillator crystal.
- External Flash memory is used to store downloaded programs.
- For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
- It is recommended that add an ESD protection chip to the JTAG download circuit.



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Notes:

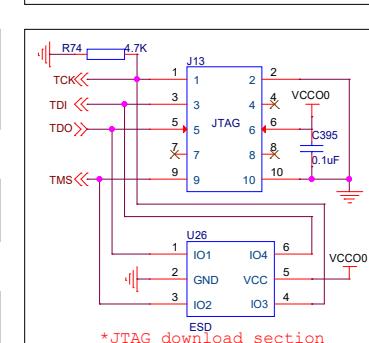
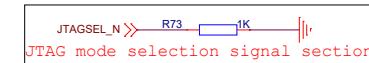
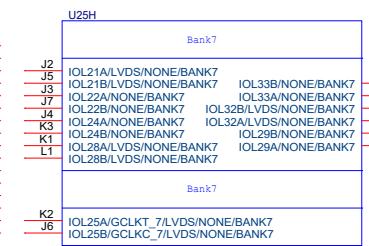
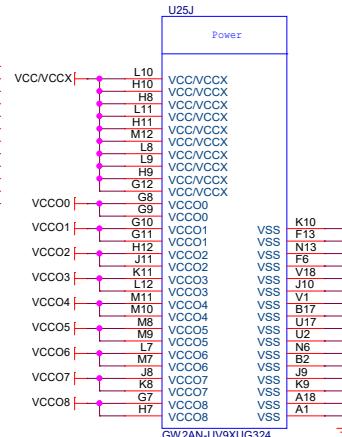
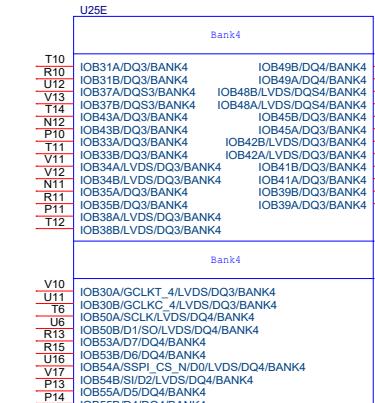
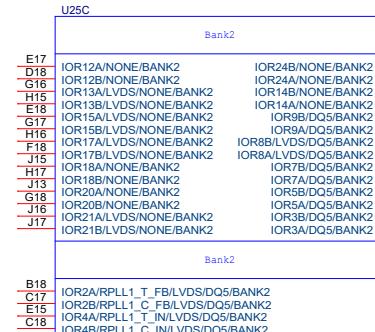
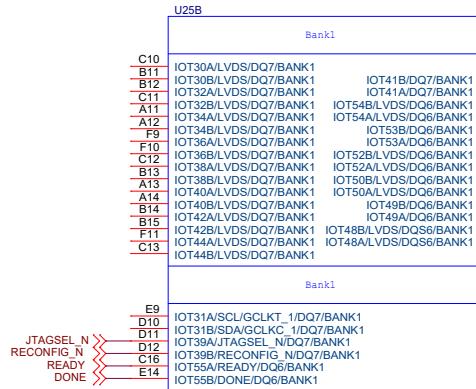
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For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
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Notes:

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For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
3. It is recommended that add an ESD protection chip to the JTAG download circuit.

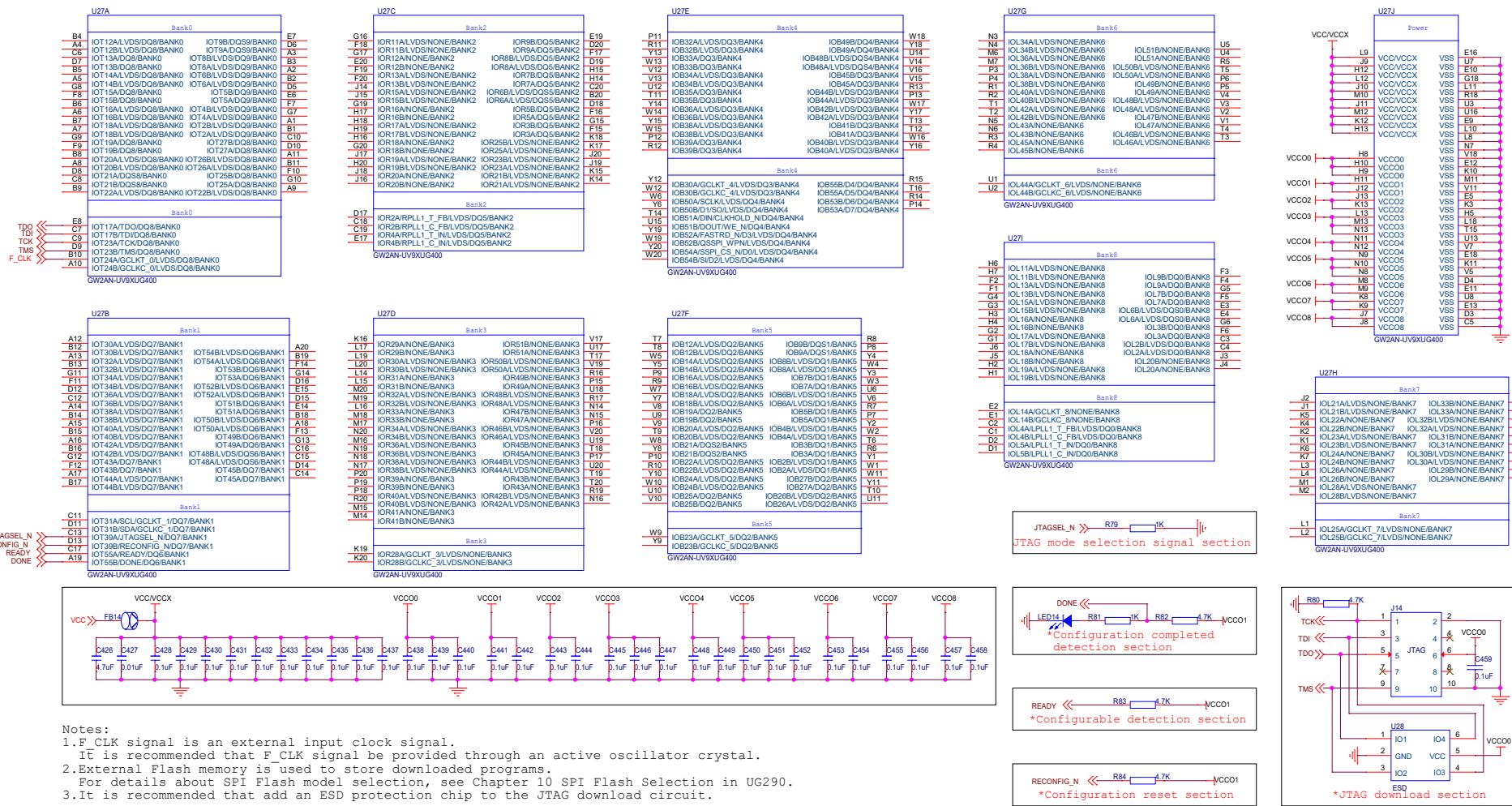
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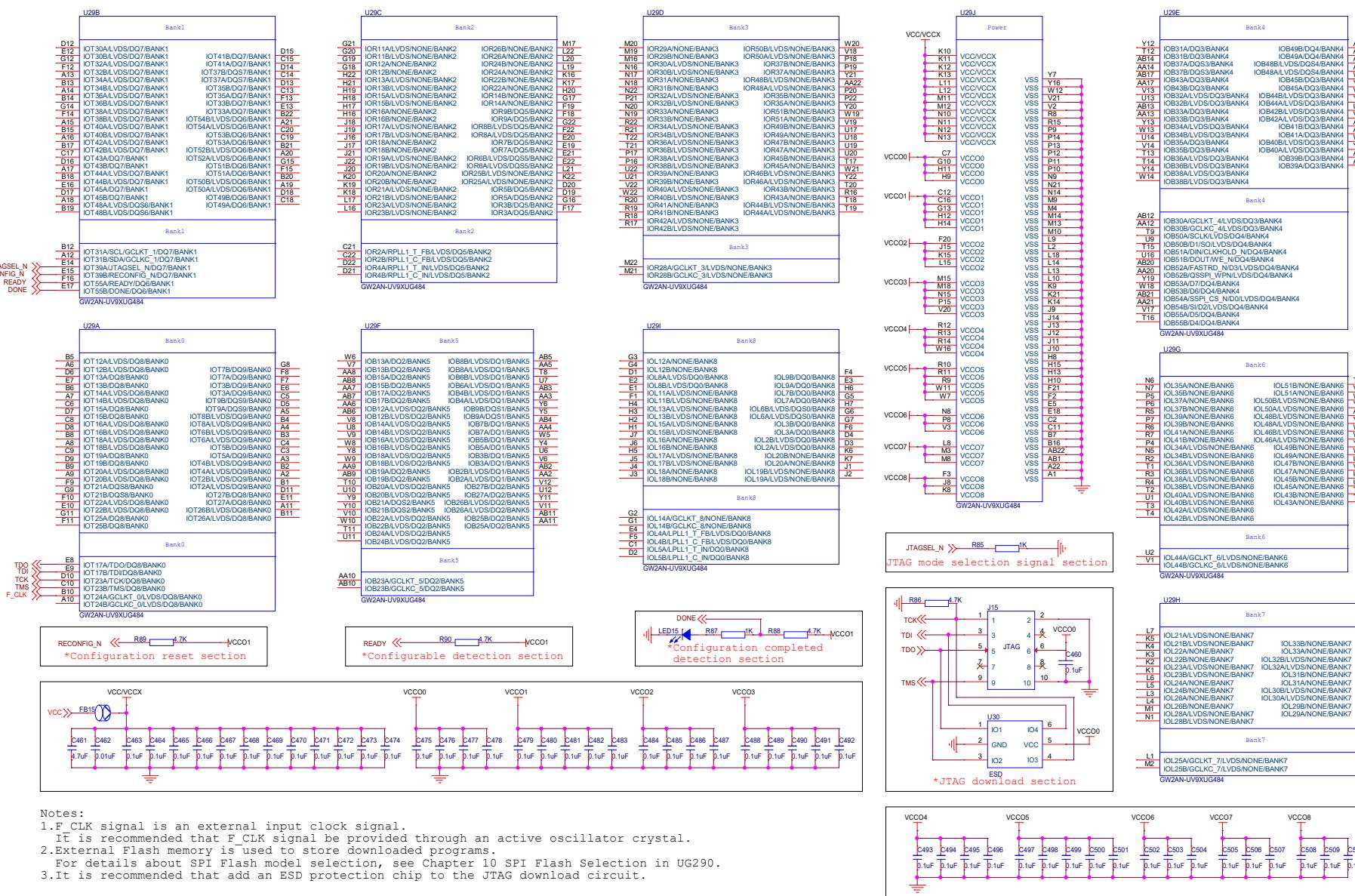
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