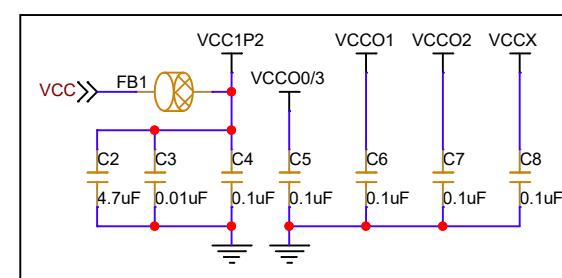
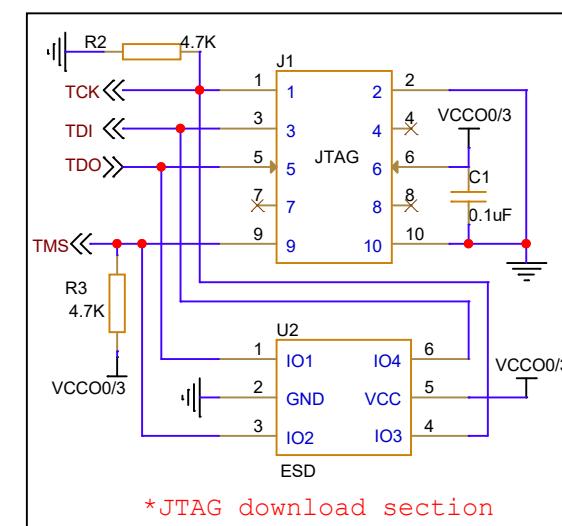
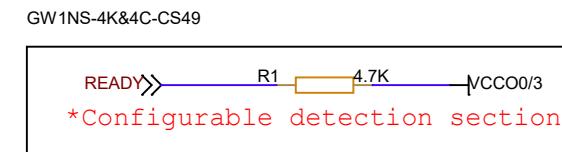
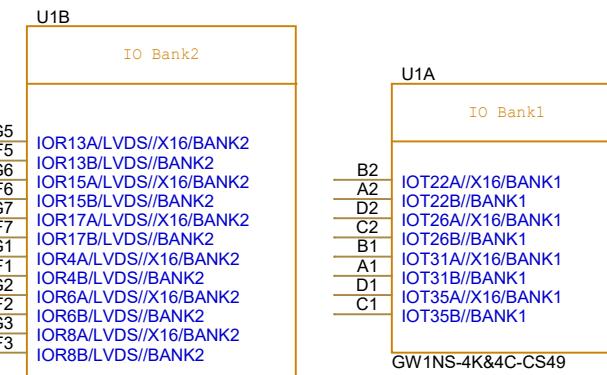
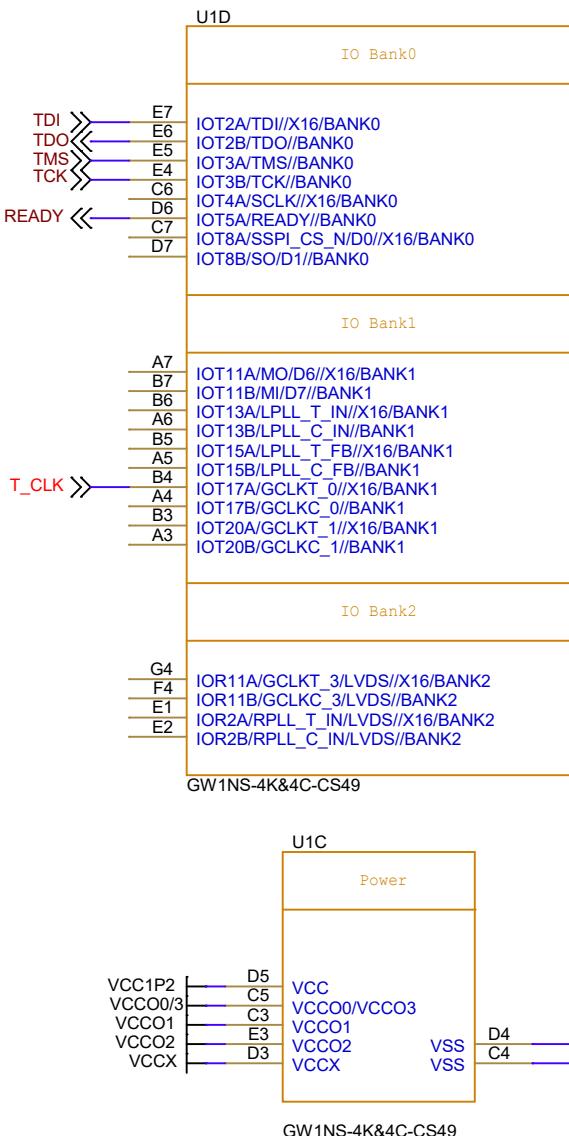


GW1NS-LV4CS49 & GW1NS-LV4CCS49



Notes:

1. F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.
3. The CS49 package supports GW1NS-4 & GW1NS-4C.

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5 GW1NS-LV4MG64 & GW1NS-LV4CMG64

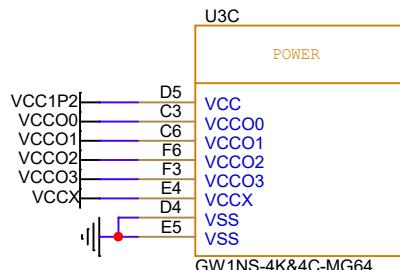
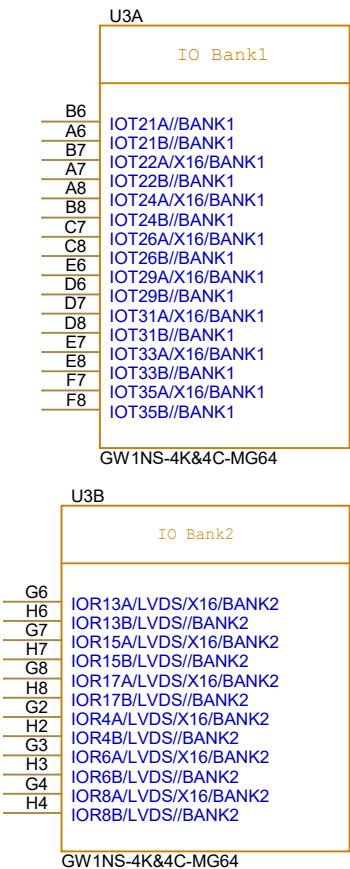
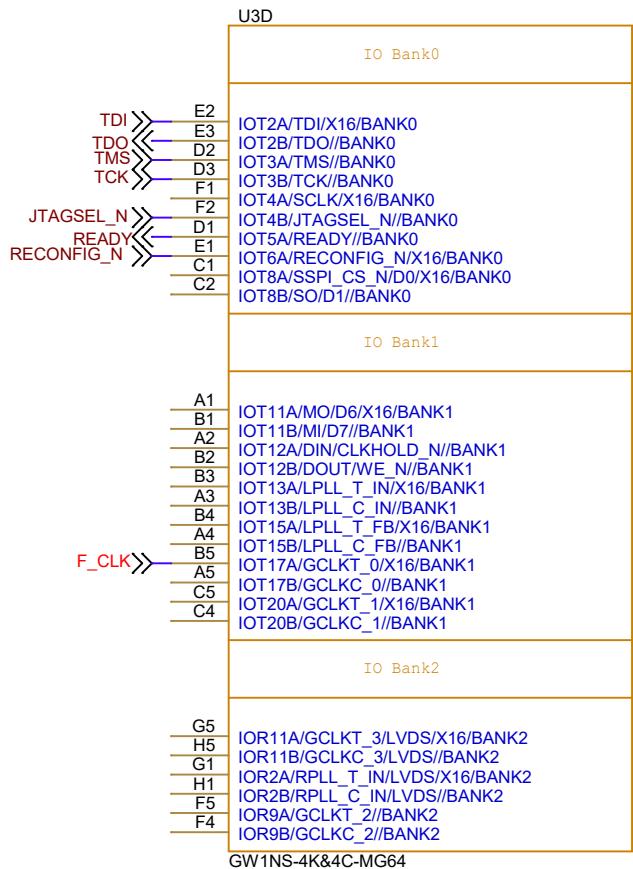
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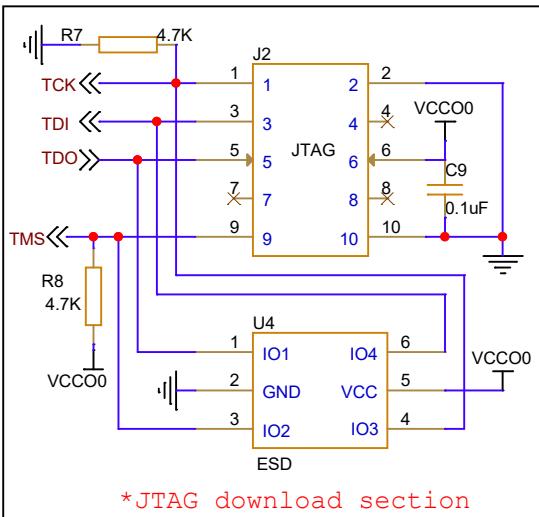
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READY » R4 4.7K VCCO0
*Configurable detection section

RECONFIG_N « R5 4.7K VCCO0
*Configuration reset section

JTAGSEL_N « R6 1K |||
JTAG mode selection signal section



Notes:

1. F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.
3. The MG64 package supports GW1NS-4 & GW1NS-4C.

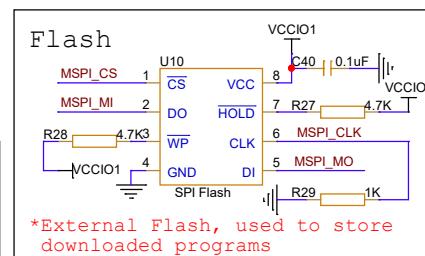
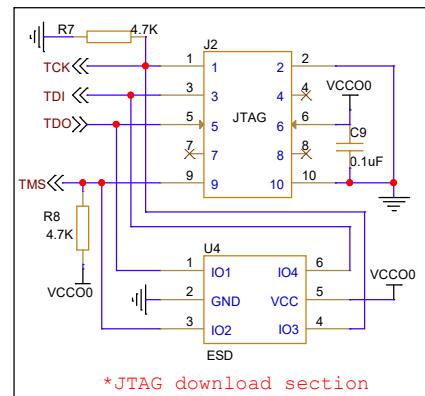
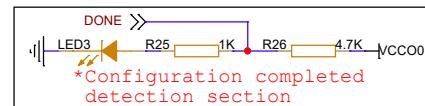
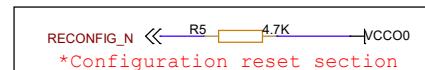
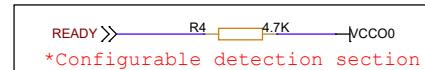
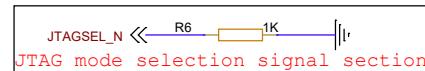
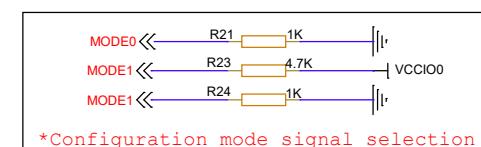
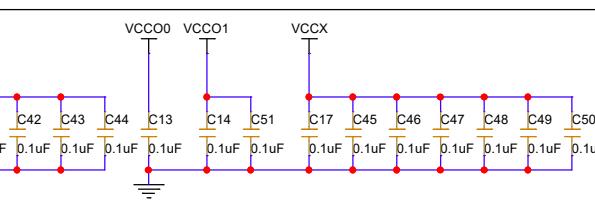
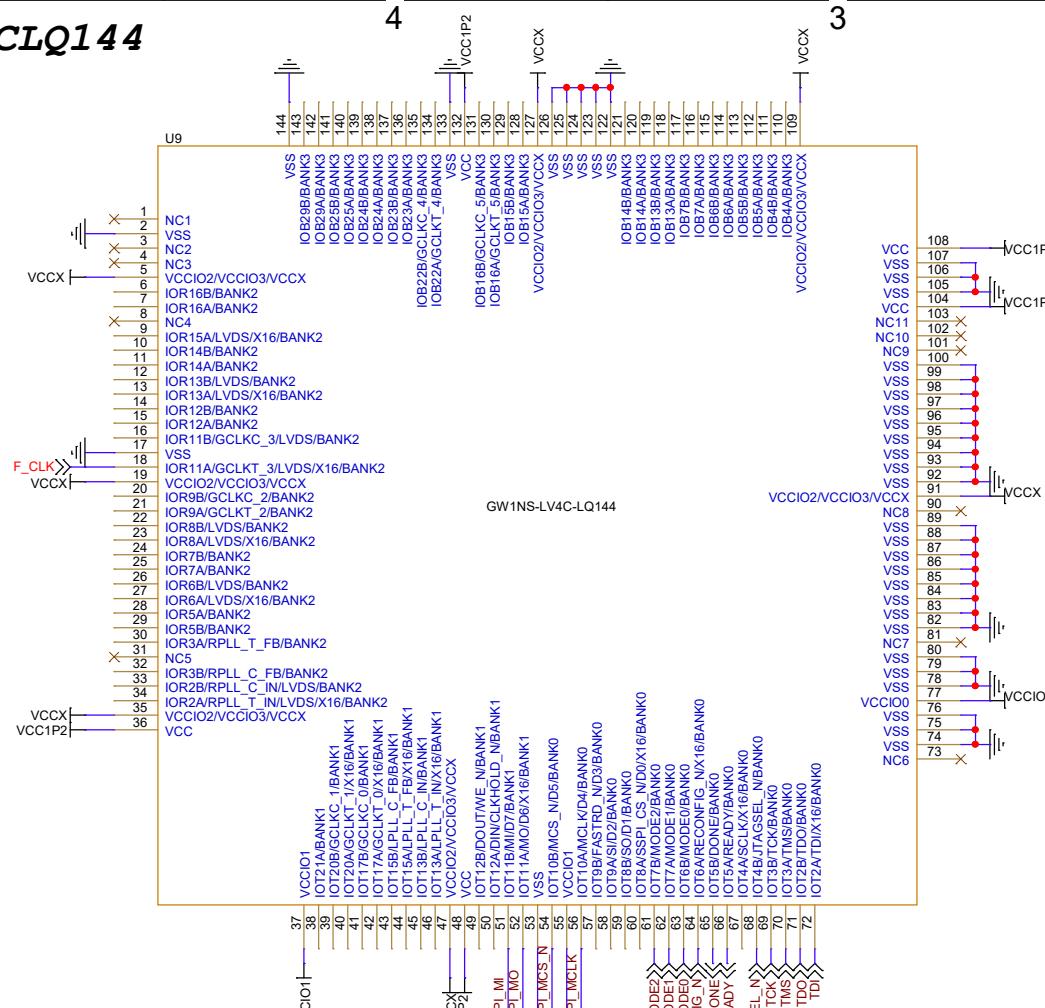
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A

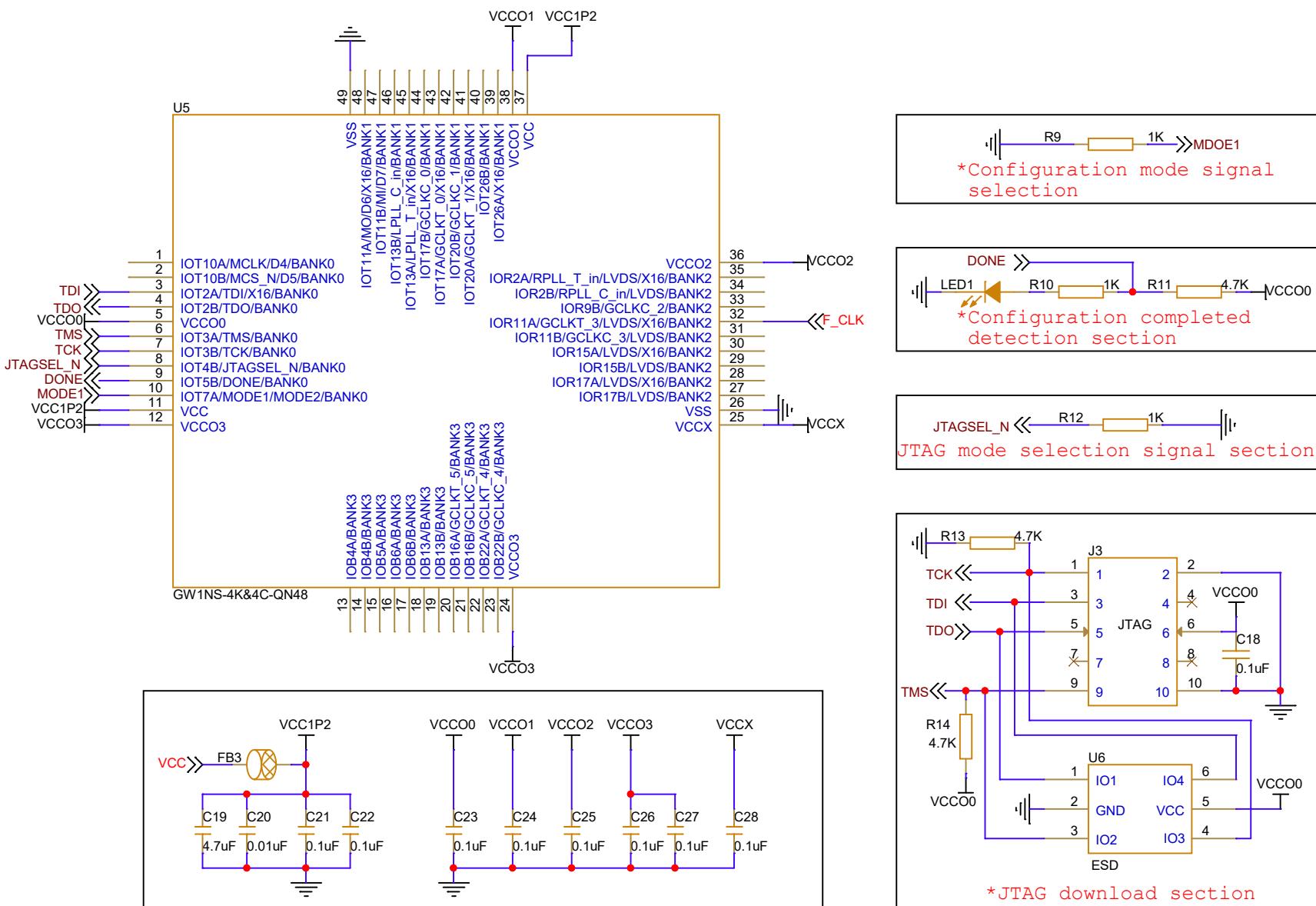


Notes:

1. F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.
3. The MG64 package supports GW1NS-4 & GW1NS-4C.

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GW1NS-LV4QN48 & GW1NS-LV4CQN48



Notes:

1. F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.
3. The QN48 package supports GW1NS-4 & GW1NS-4C.

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GW1NS-LV4QN48 & GW1NS-LV4CQN48

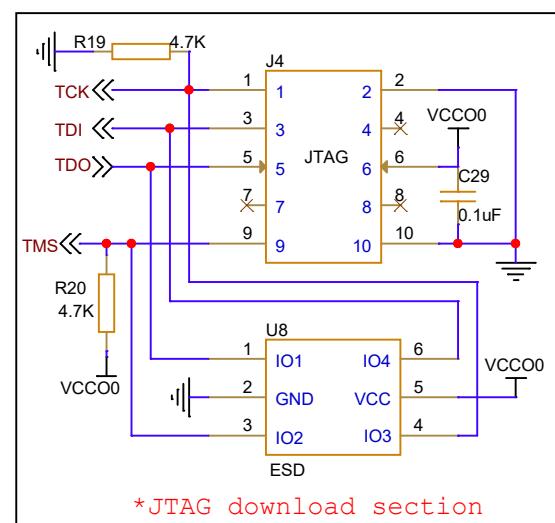
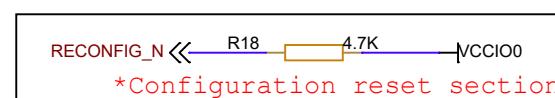
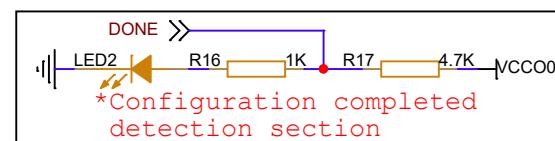
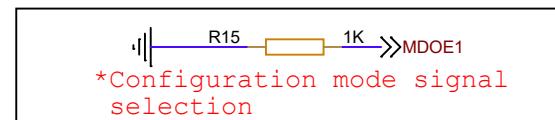
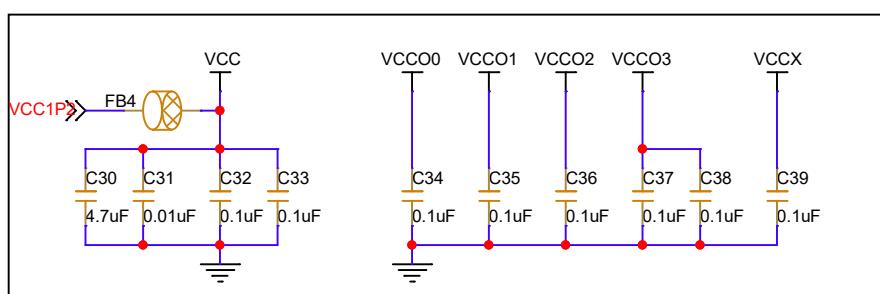
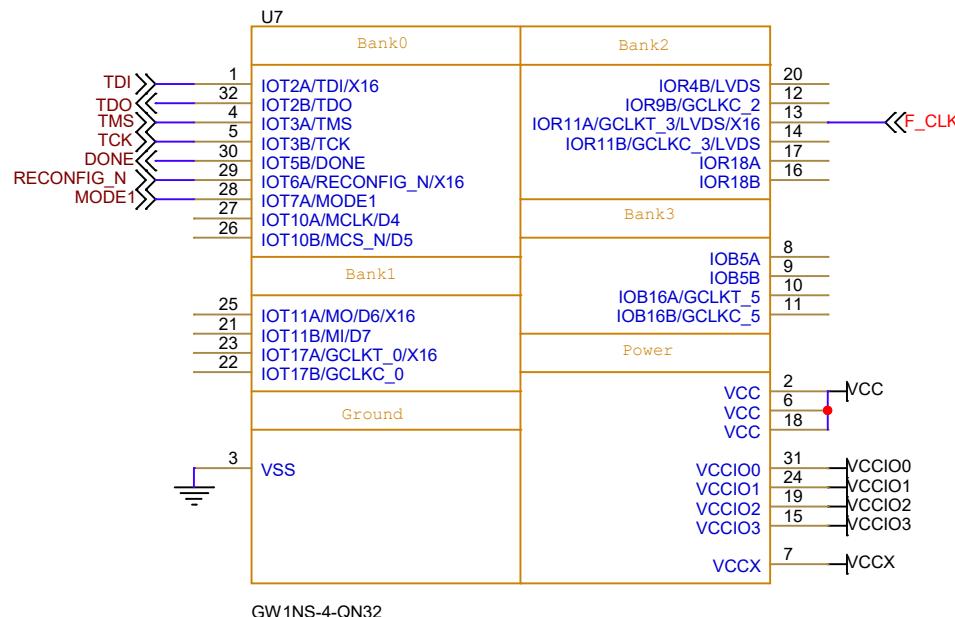
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GW1NS-LV4QN32



Notes:

1. F_CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.