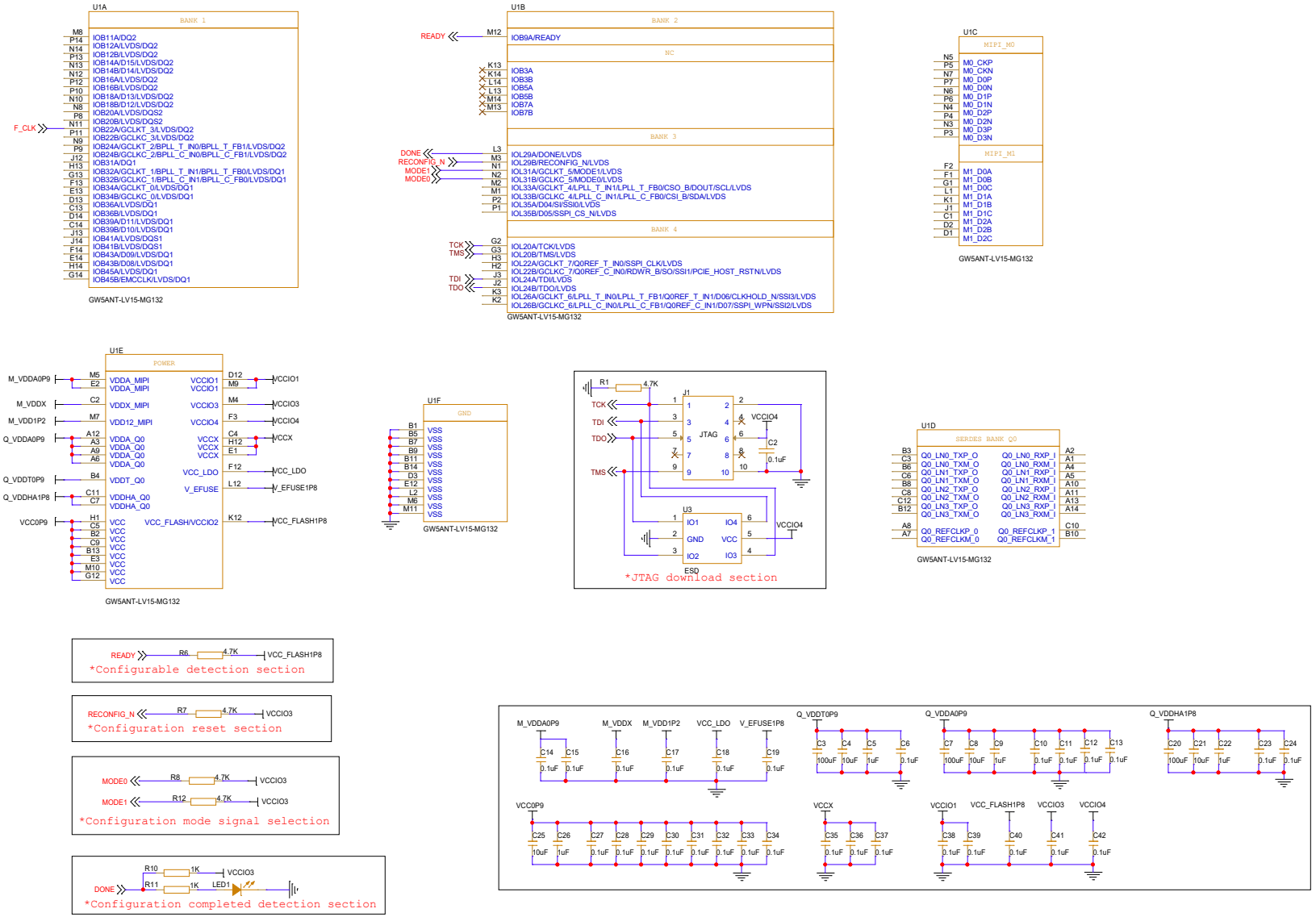
GW5ANT-LV15MG132



Notes:
1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2.It is recommended that add an ESD protection chip to the JTAG download circuit.
3.VCC core voltage requires a large current, so it is recommended to supply power separately.
4.The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG720, Arora V 15K FPGA Products Programming and Configuration Guide.

Title	GOWIN Minimum System Diagram	
Size C	Document Number GW5ANT-LV15MG132	Rev 1.1
Date: Friday, August 09, 2024	Sheet 1 of 1	