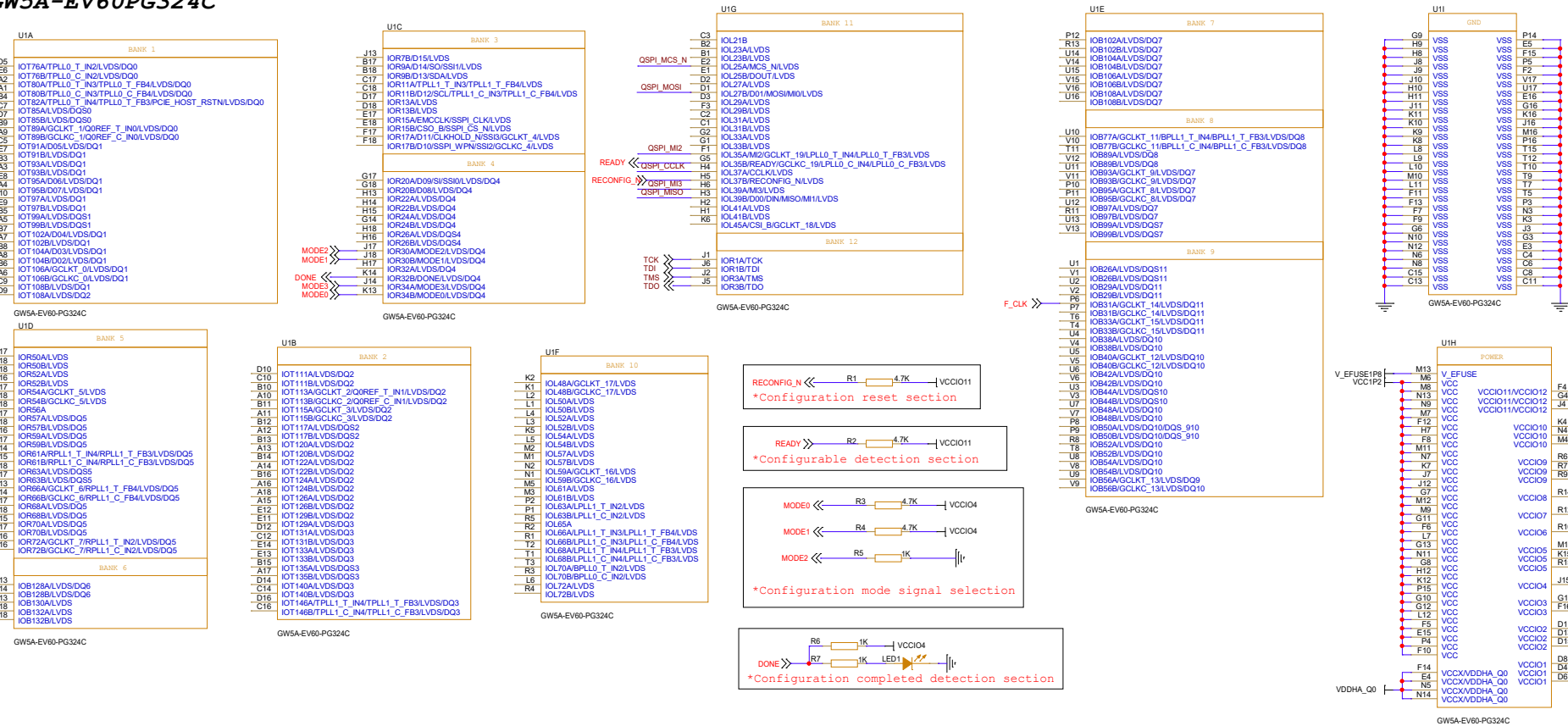
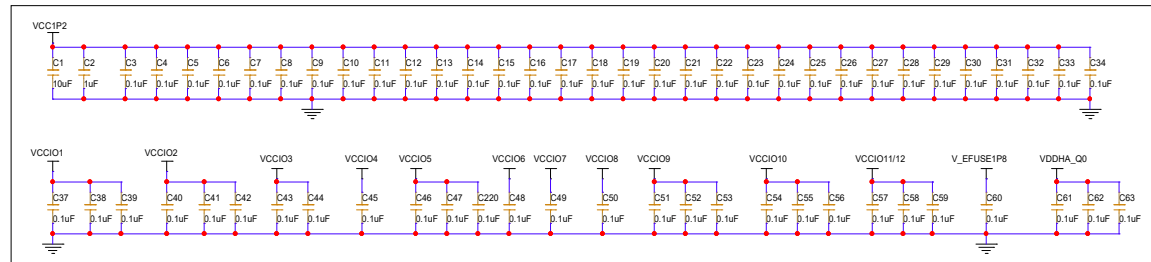
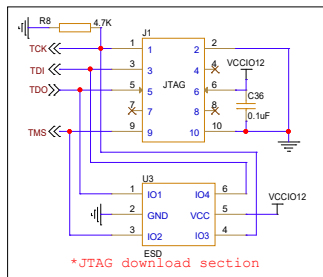
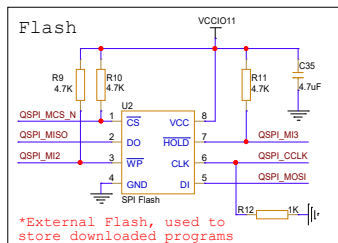


GW5A-EV60PG324C

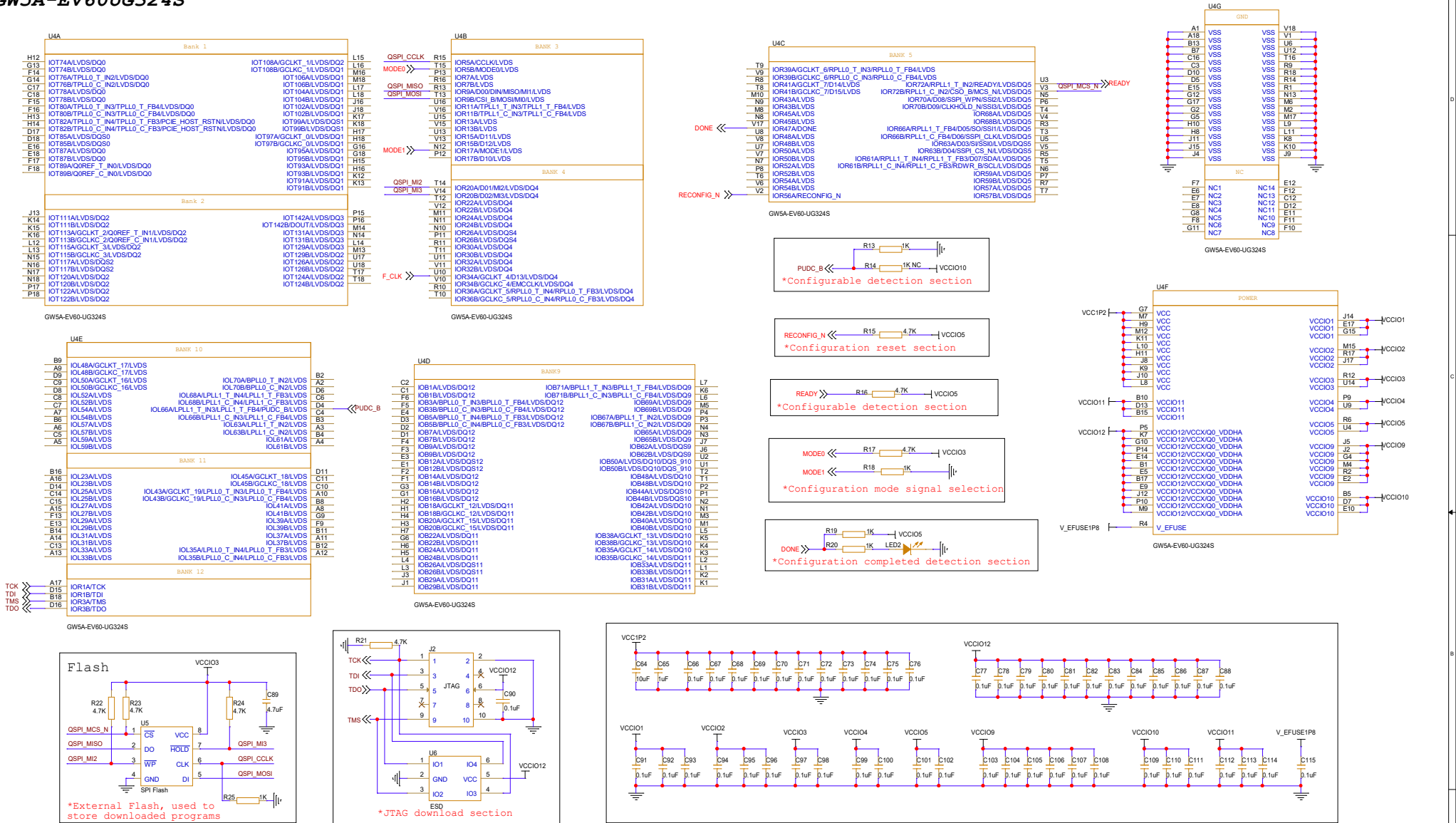


- 1.F CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash Model selection, see "Chapter 4.5 SPI Flash Selection" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide.
- 6.This package does not support the use of internal differential termination resistors.



Title			
GOWIN Minimum System Diagram			
Size	Document Number		Rev
C	GW5A-EV60PG-324C		1.1
Date:	Friday, August 09, 2024	Sheet	1 of 4

GW5A-EV60UG324S



Notes:

1.F CLK signal is an external input clock signal.

It is recommended that F CLK signal be provided through an active oscillator crystal.

2.External Flash memory is used to store downloaded programs.

For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG718,

Arora V 60K FPGA Products Programming and Configuration Guide .

3.It is recommended that add an ESD protection chip to the JTAG download circuit.

4.VCC core voltage requires a large current, so it is recommended to s

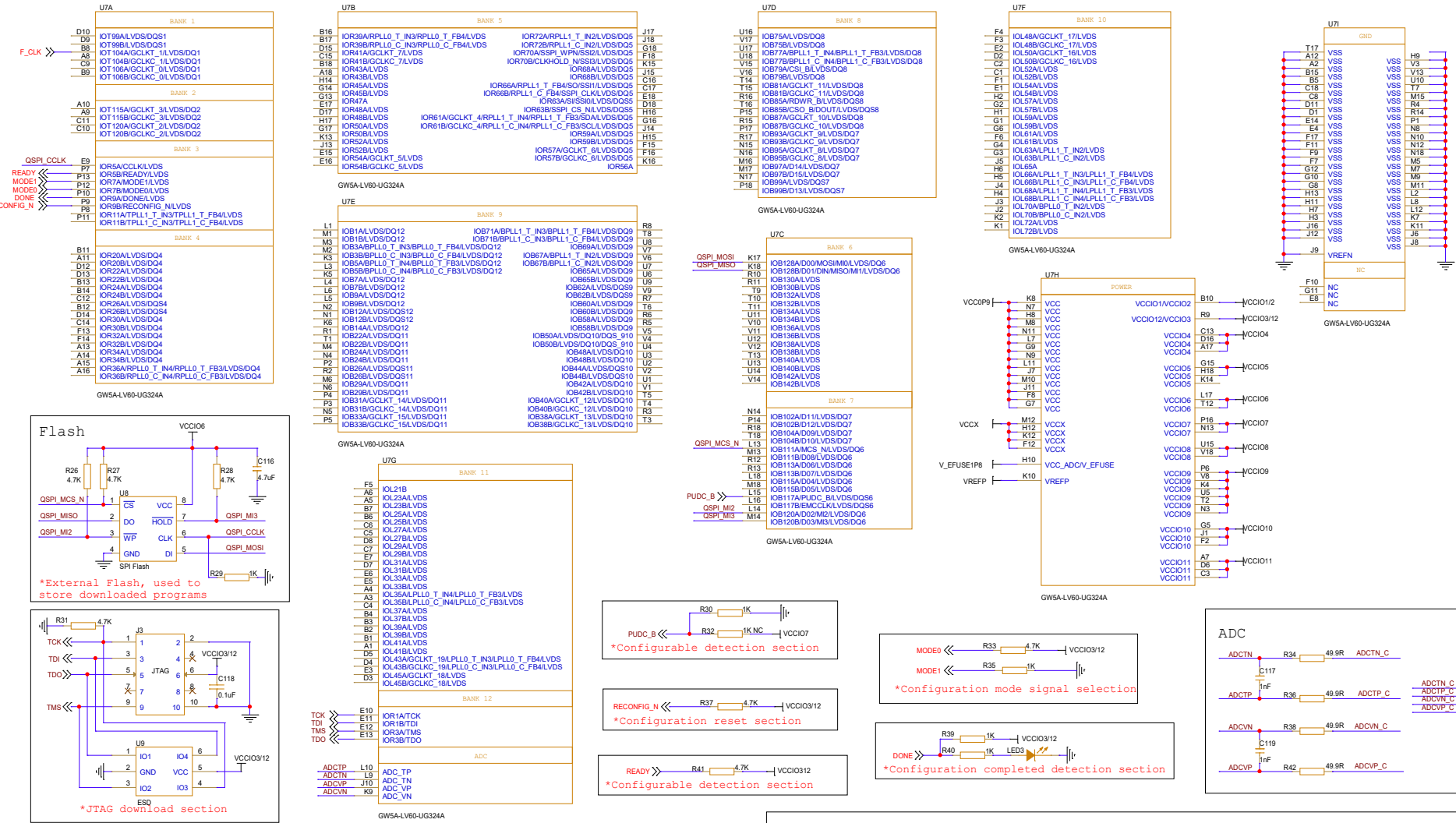
5.The MODE pin is the GowinCONFIG configuration mode selection signal.

For details about how to select the Mode signal, see "Chapter 3.1 Conf

For details about how to select the Mode signal, see Chapter 5.1 Configuration Modes in 6G10, Arora V 60K FPGA Products Programming and Configuration Guide.

ALORA

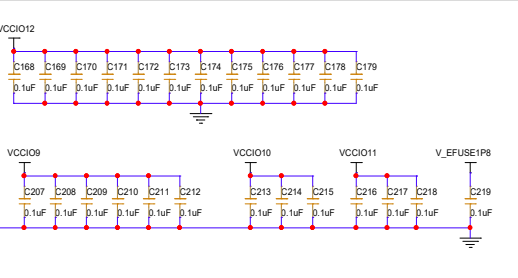
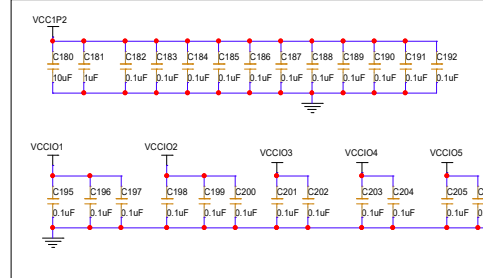
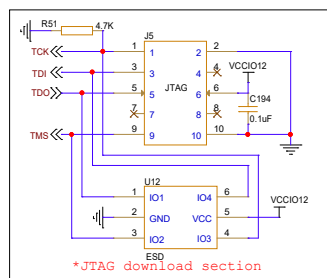
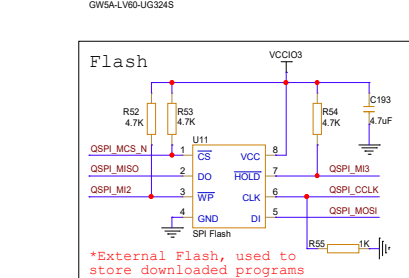
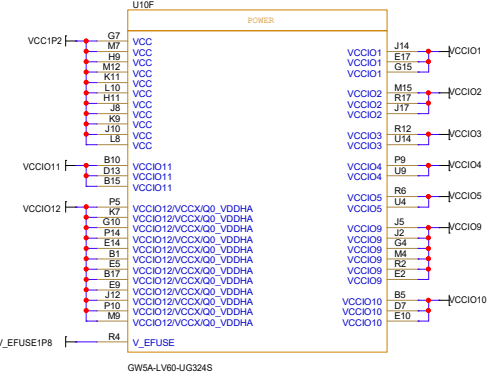
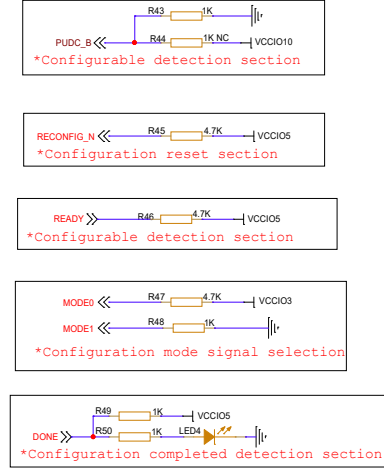
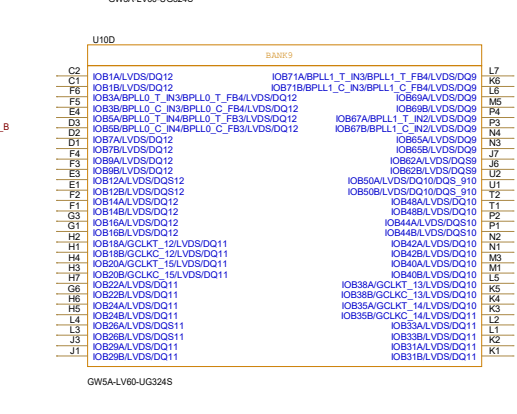
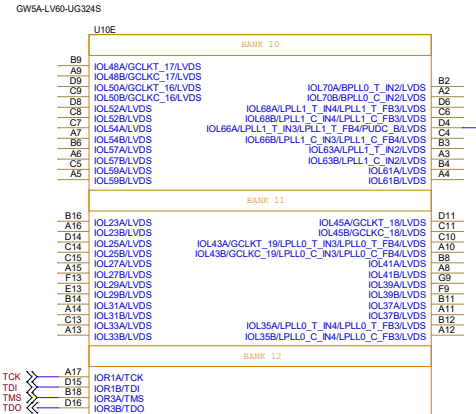
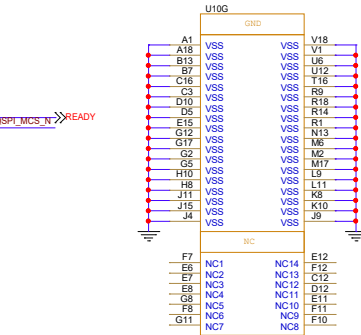
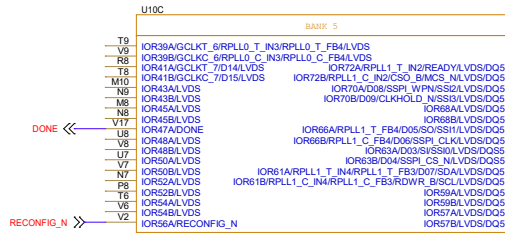
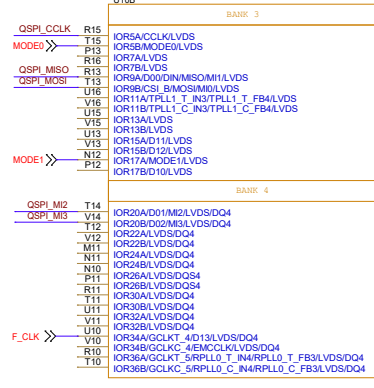
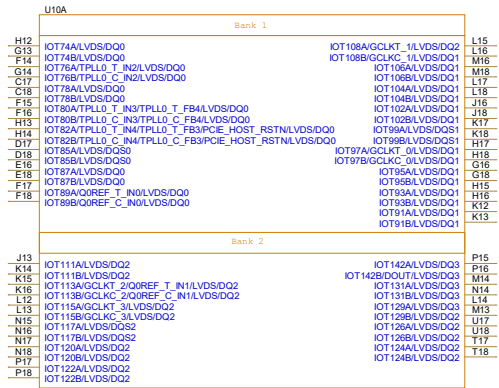
GW5A-1V60UG324A



Notes:

- 1.F CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide.

GW5A-LV60UG324S



Notes:

- 1.F CLK signal is an external input clock signal.
- It is recommended that F CLK signal be provided through an active oscillator crystal.
- External Flash memory is used to store downloaded programs.
- For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide.
- It is recommended that add an ESD protection chip to the JTAG download circuit.
- VCC core voltage requires a large current, so it is recommended to supply power separately.
- The MODE pin is the GowinCONFIG mode selection signal.
- For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide.

Title			GOWIN Minimum System Diagram
Size	Document Number	Rev	
C	GW5A-LV60UG324S	1.1	
Date	Friday, August 09, 2024	Sheet	4 of 4