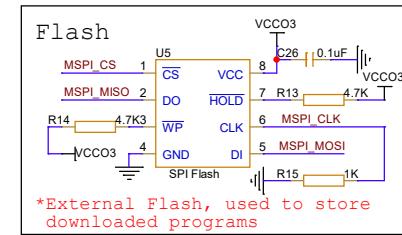
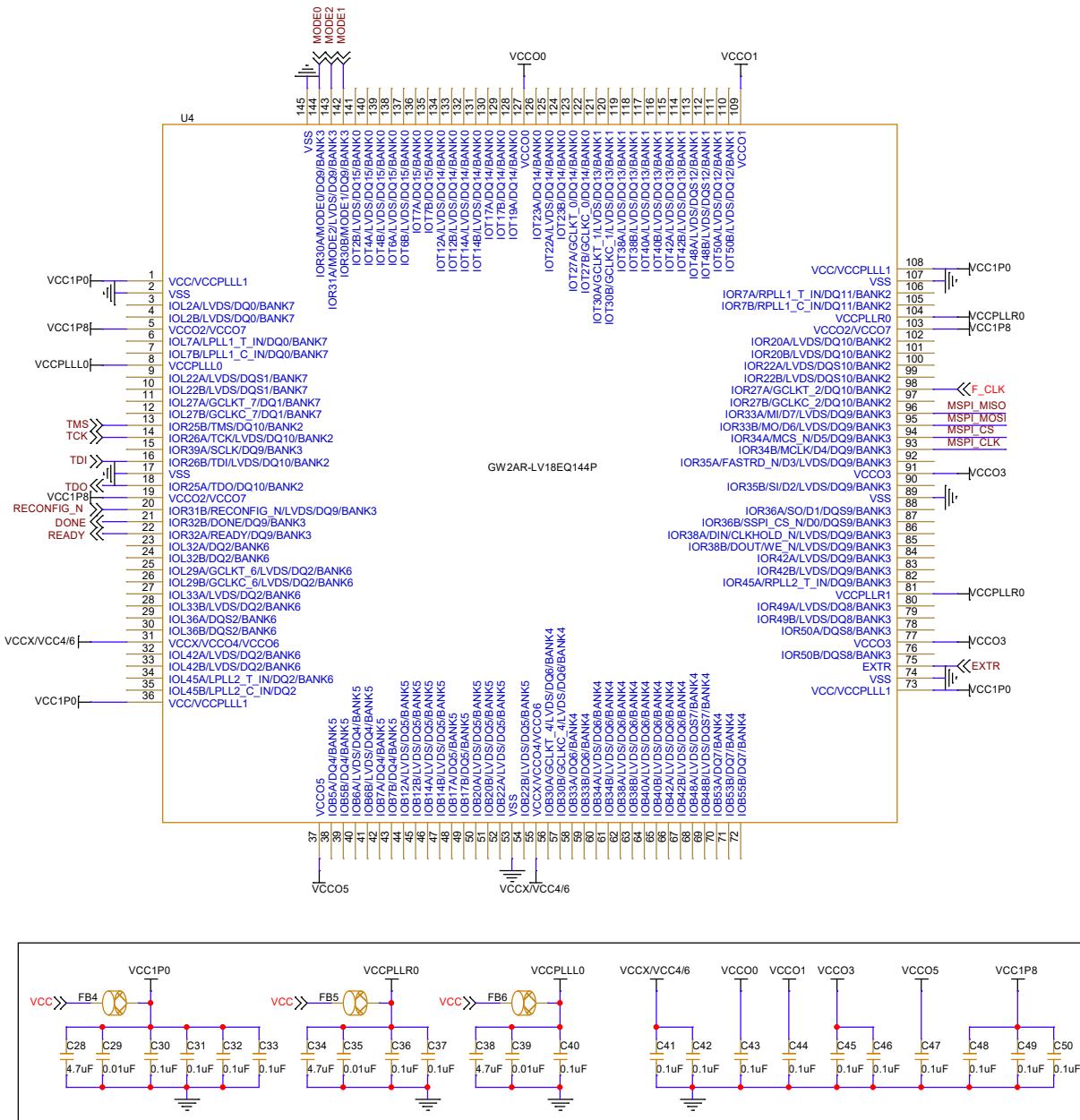
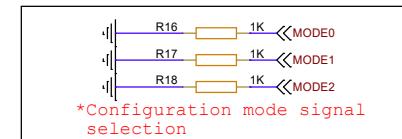
**Notes:**

1. F\_CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
2. External Flash memory is used to store downloaded programs.  
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
3. It is recommended that add an ESD protection chip to the JTAG download circuit.

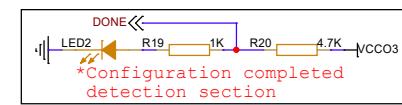
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Size	Document Number
A3	GW2AR-LV18EQ144
Rev	2.0
Date:	Thursday, November 09, 2023
Sheet	1 of 7



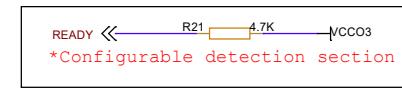
\*External Flash, used to store downloaded programs



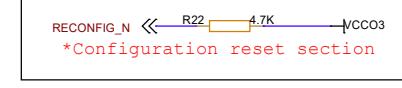
\*Configuration mode signal selection



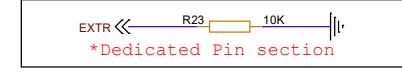
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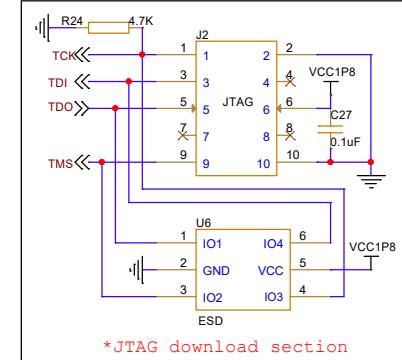
\*Configurable detection section



### \*Configuration reset section



\*Dedicated Bin section



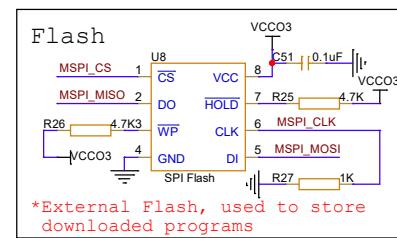
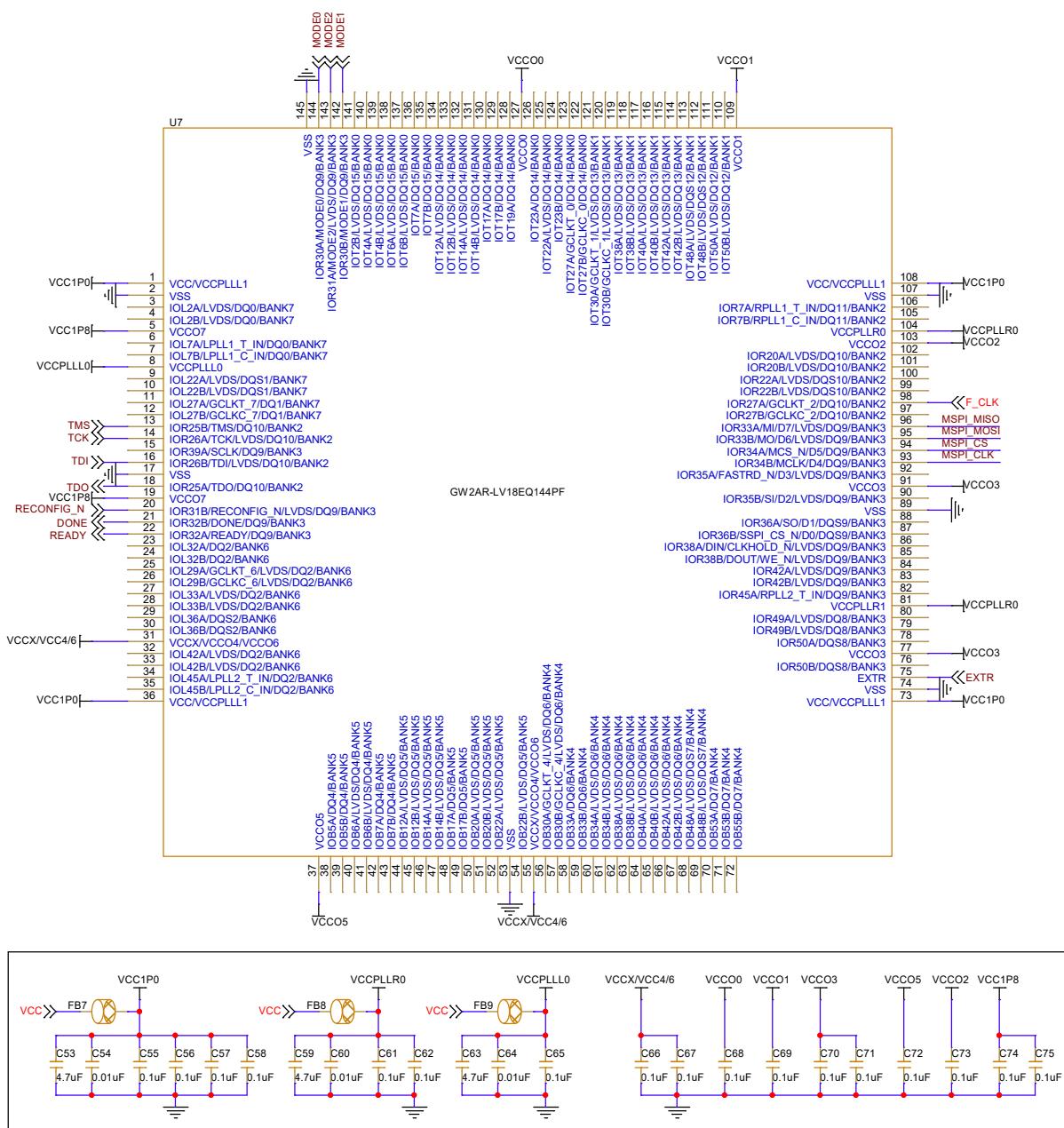
\*JTAG download section

### Notes:

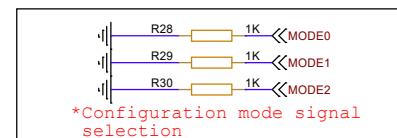
- Notes:

  - 1.F\_CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
  - 2.External Flash memory is used to store downloaded programs.  
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290
  - 3.It is recommended that add an ESD protection chip to the JTAG download circuit.

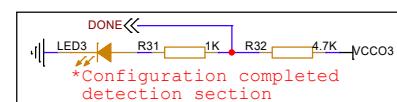
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Size A3	Document Number GW2AR-LV18EQ144P	Rev 2.0
Date:	Thursday, November 09, 2023	Sheet 2 of 7



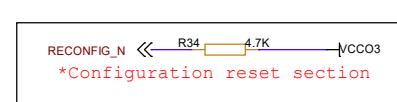
\*External Flash, used to store downloaded programs



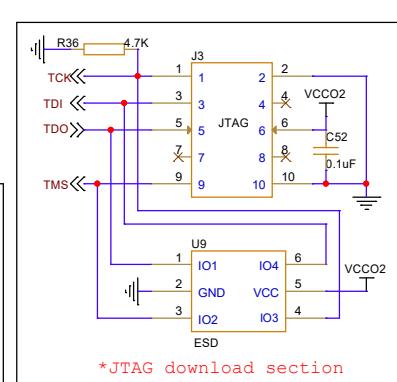
\*Configuration mode signal selection



READY << R33 4.7K VCCO3  
\*Configurable detection section



**EXTR << R35 10K ||**  
\*Dedicated Pin section



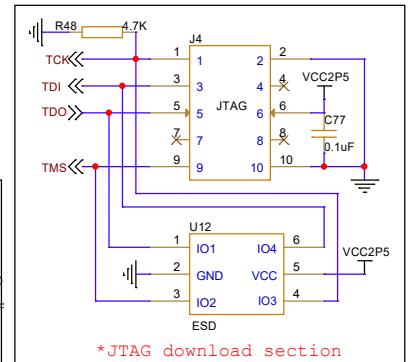
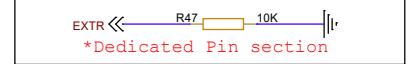
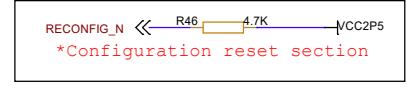
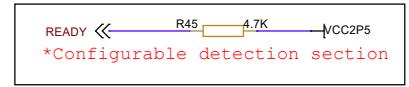
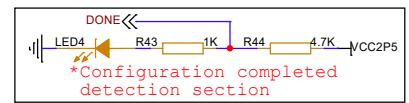
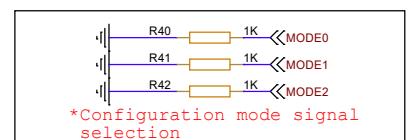
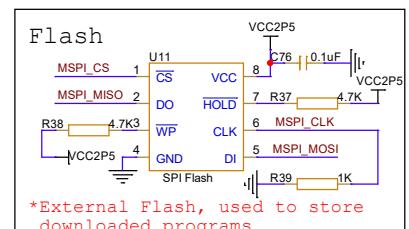
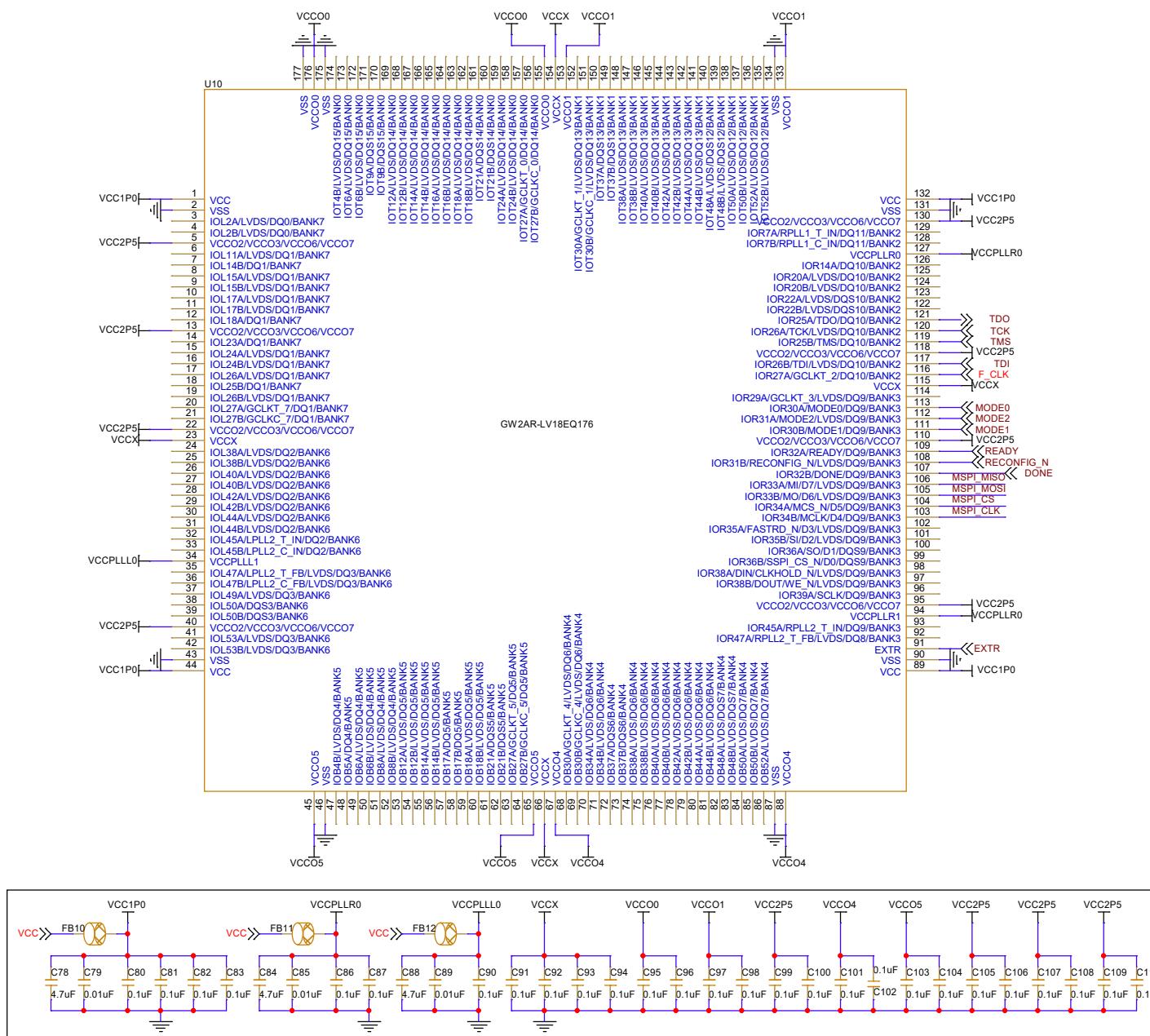
\*JTAG download section

#### Notes:

- NOTES:

  - 1.F CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
  - 2.External Flash memory is used to store downloaded programs.  
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
  - 3.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size A3	Document Number GW2AR-LV18EQ144PF	Rev 2.0
Date: Thursday, November 09, 2023	Sheet 3	of 7

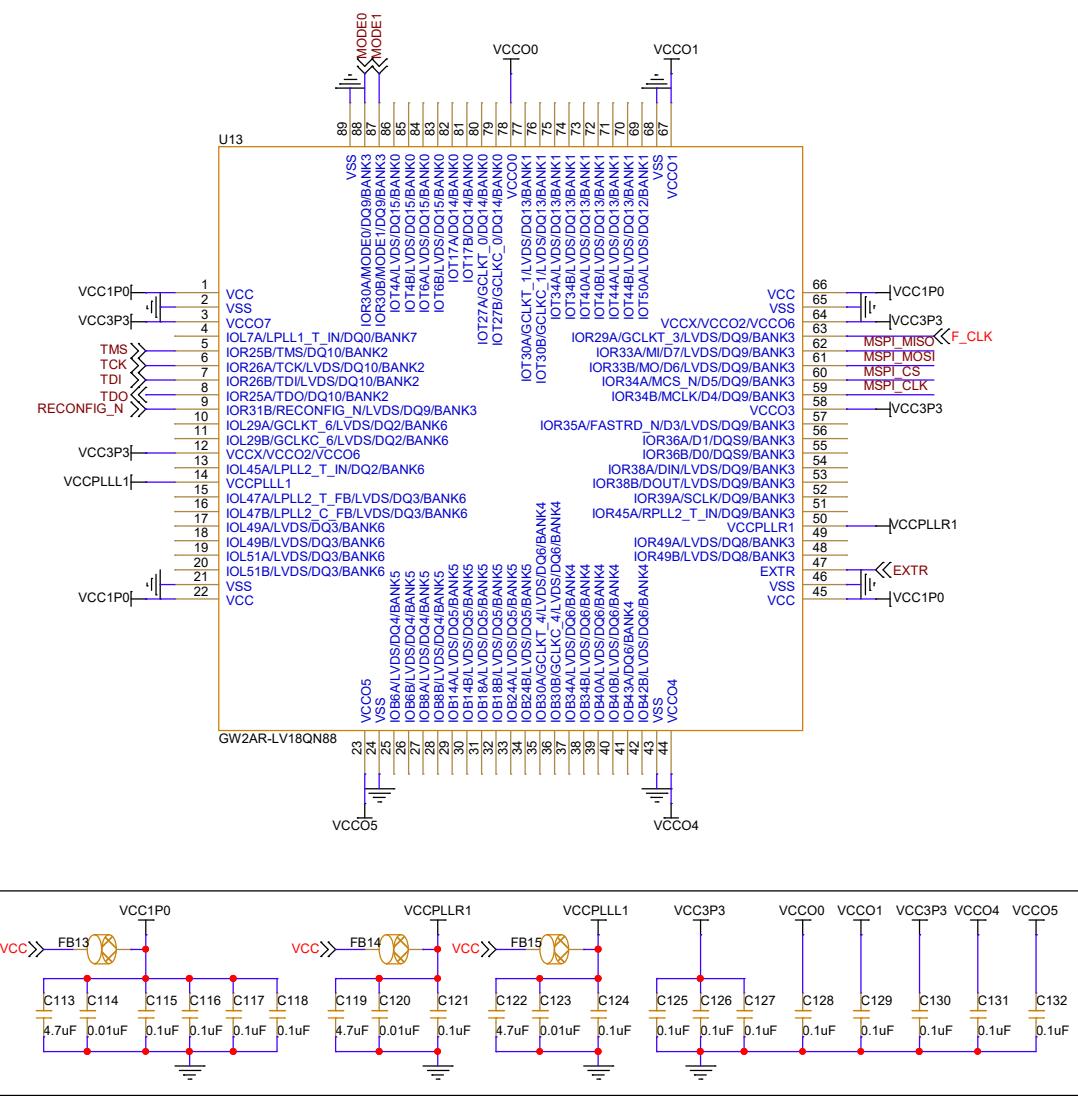


#### Notes:

- NOTES:

  - 1.F\_CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
  - 2.External Flash memory is used to store downloaded programs.  
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
  - 3.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size A3	Document Number GW2AR-LV18EQ176	Rev 2.0
Date: Tuesday, April 04, 2023	Sheet 4	of 7

**Notes:**

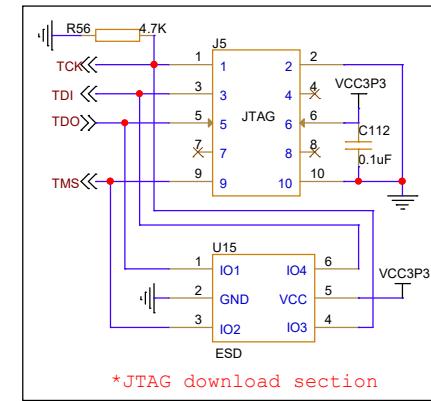
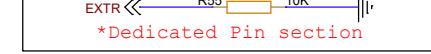
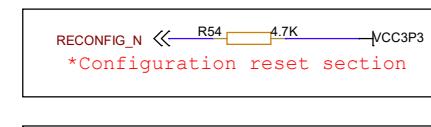
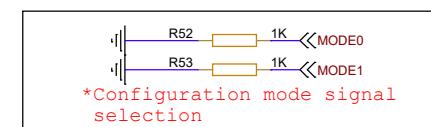
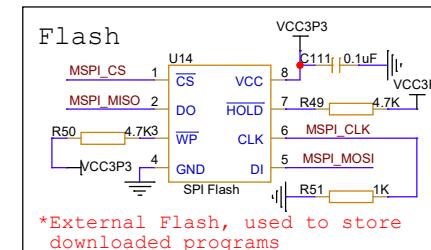
1. F\_CLK signal is an external input clock signal.

It is recommended that F\_CLK signal be provided through an active oscillator crystal.

2. External Flash memory is used to store downloaded programs.

For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.

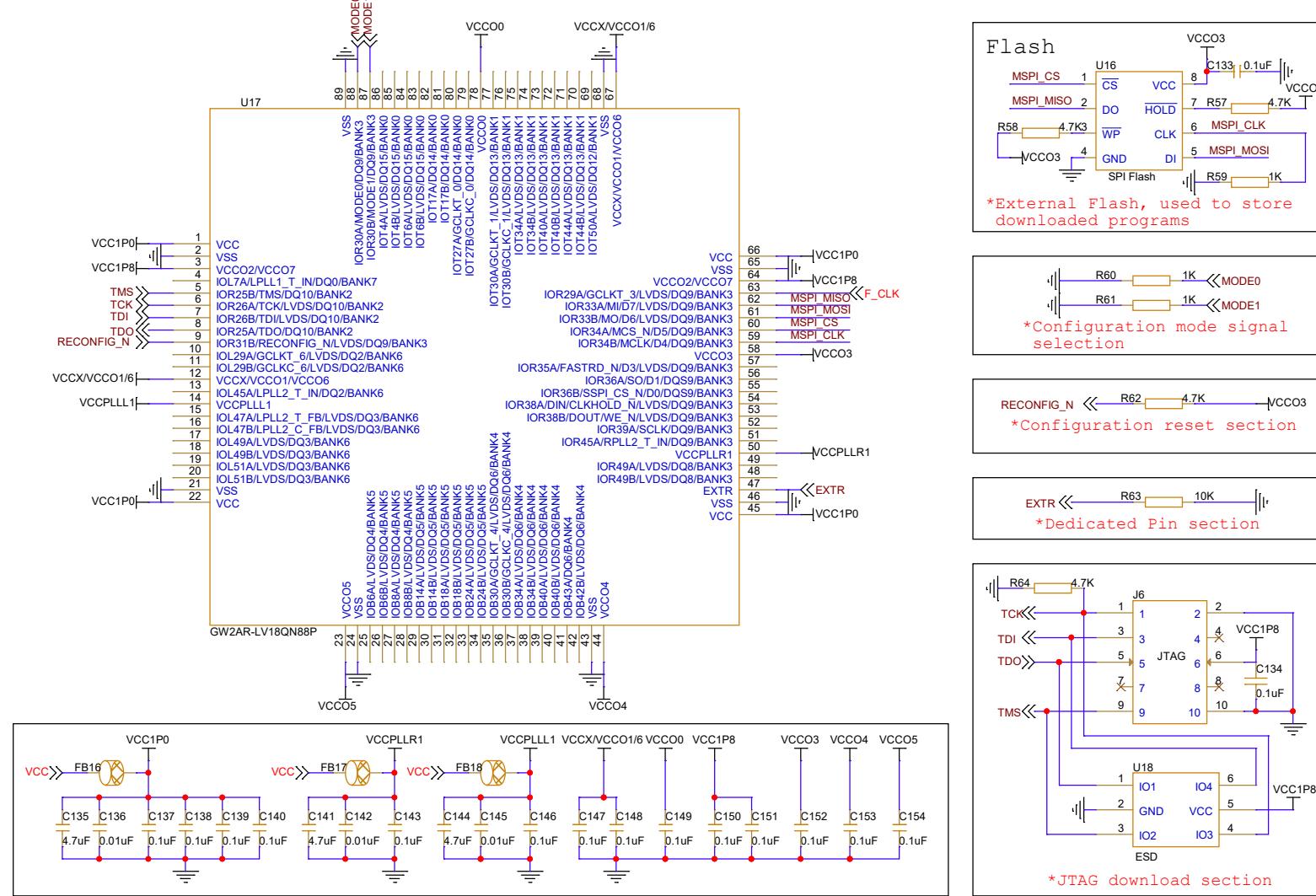
3. It is recommended that add an ESD protection chip to the JTAG download circuit.



Title	
GOWIN Minimum System Diagram	
Size	Document Number
B	GW2AR-LV18QN88
	Rev
	2.0

Date: Tuesday, April 04, 2023

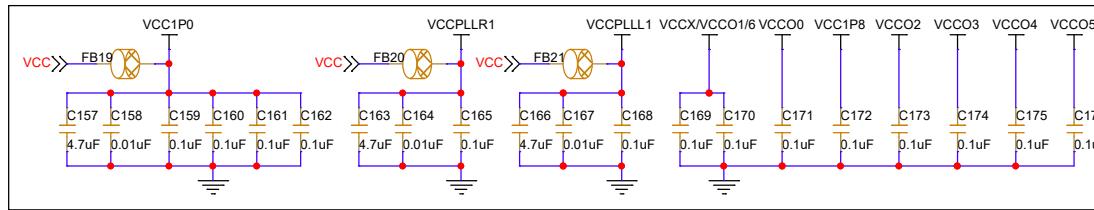
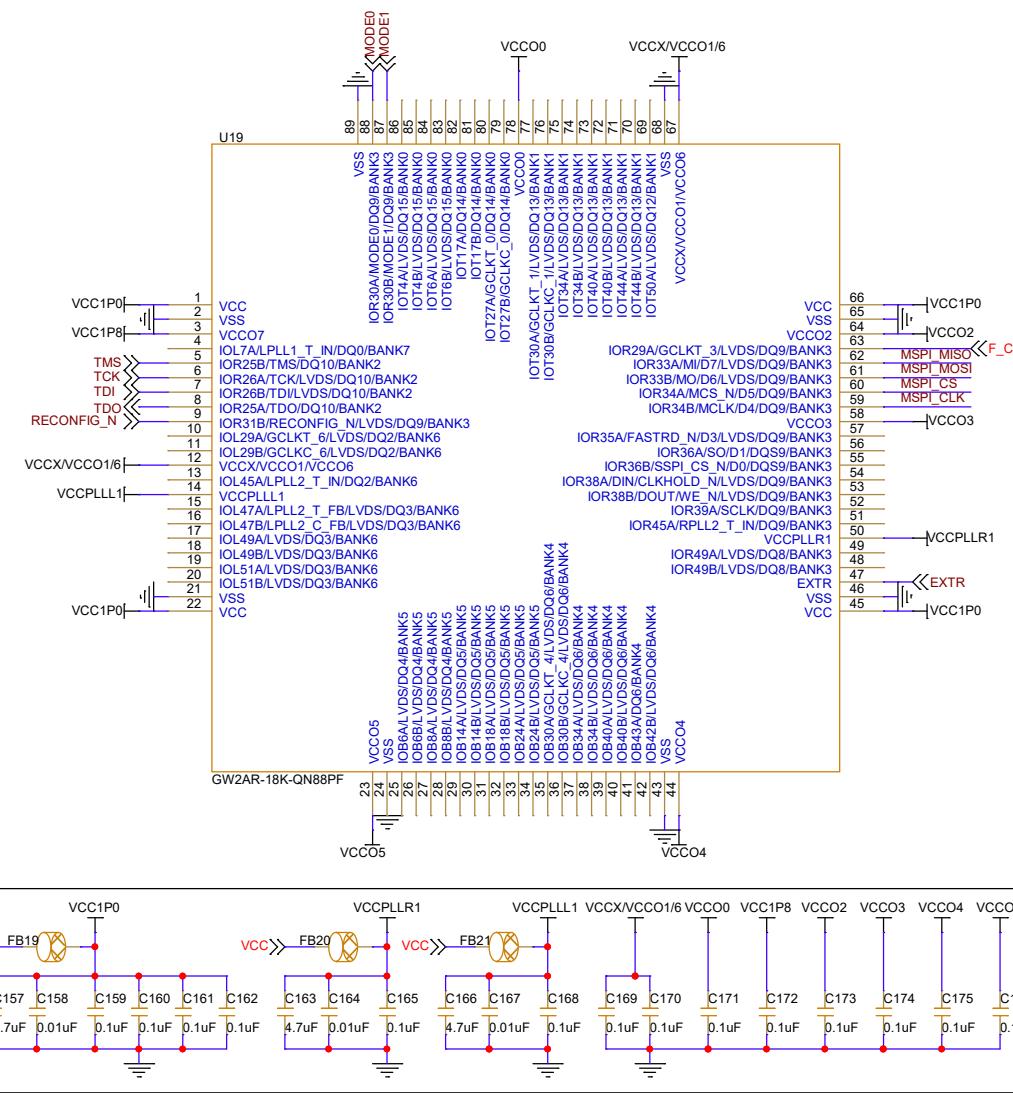
Sheet 5 of 7

**Notes:**

1. F\_CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
2. External Flash memory is used to store downloaded programs.  
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
3. It is recommended that add an ESD protection chip to the JTAG download circuit.

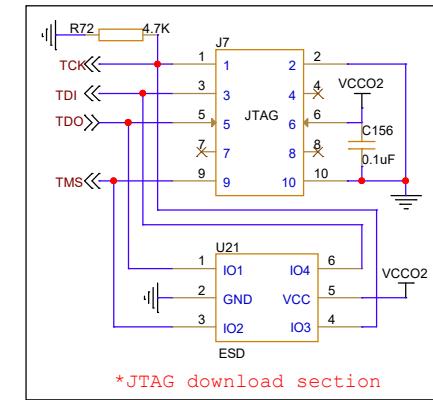
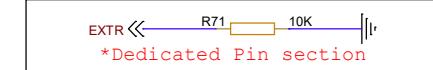
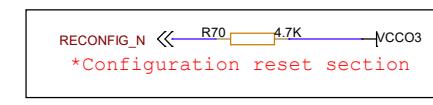
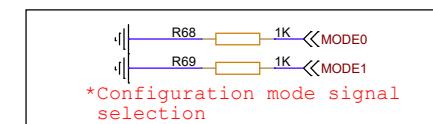
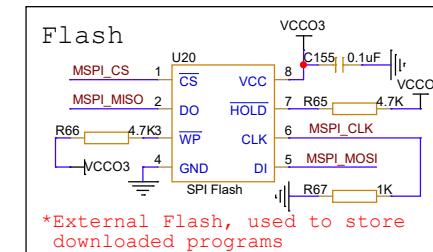
Title	
GOWIN Minimum System Diagram	
Size	Document Number GW2AR-LV18QN88P
B	Rev 2.0

Date: Tuesday, April 04, 2023



## Notes:

1. F\_CLK signal is an external input clock signal.  
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For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
3. It is recommended that add an ESD protection chip to the JTAG download circuit.



Title	
GOWIN Minimum System Diagram	
Size	Document Number
B	GW2AR-LV18QN88PF
Rev	2.0
Date:	Tuesday, April 04, 2023
Sheet	7 of 7