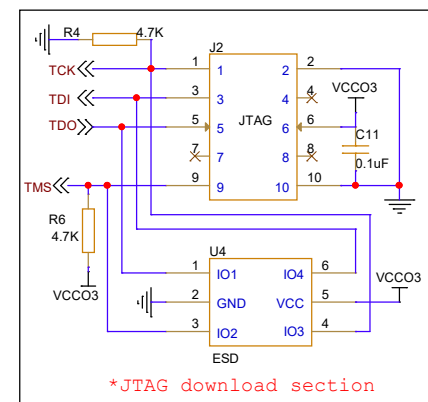
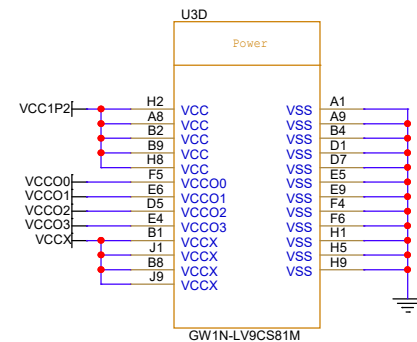
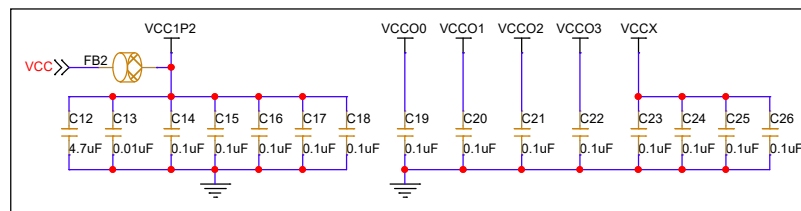
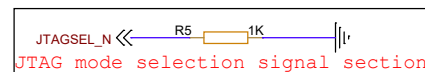
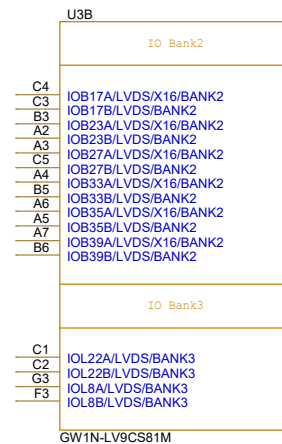
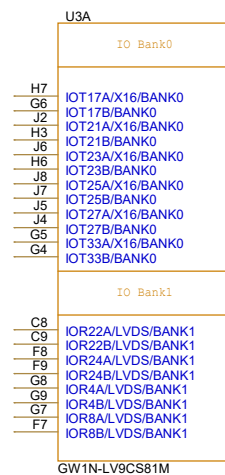
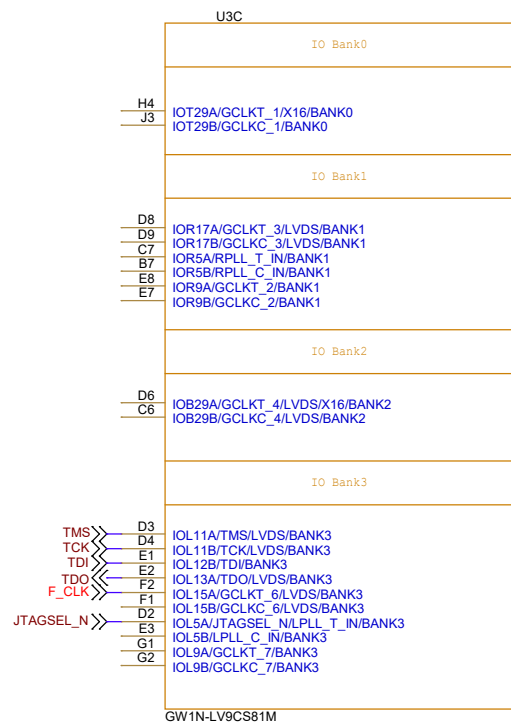


A  
B

- |                              |                                 |       |            |
|------------------------------|---------------------------------|-------|------------|
| Title                        |                                 |       |            |
| GOWIN Minimum System Diagram |                                 |       |            |
| Size<br>A4                   | Document Number<br>GW1N-LV9CM64 |       | Rev<br>2.2 |
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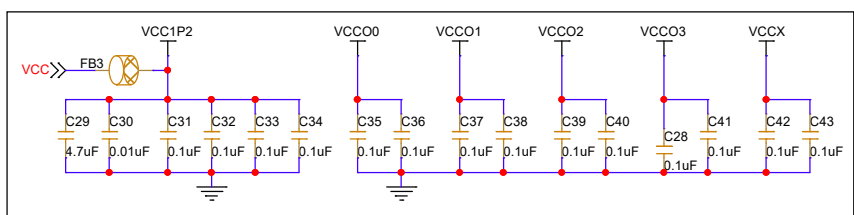
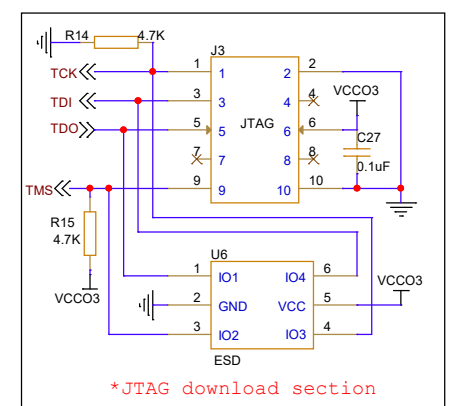
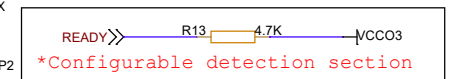
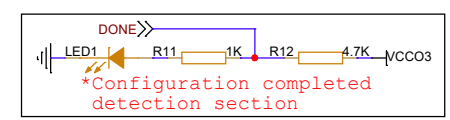
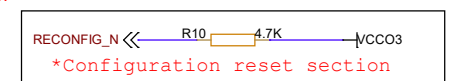
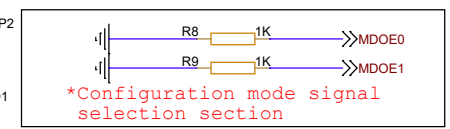
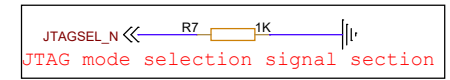
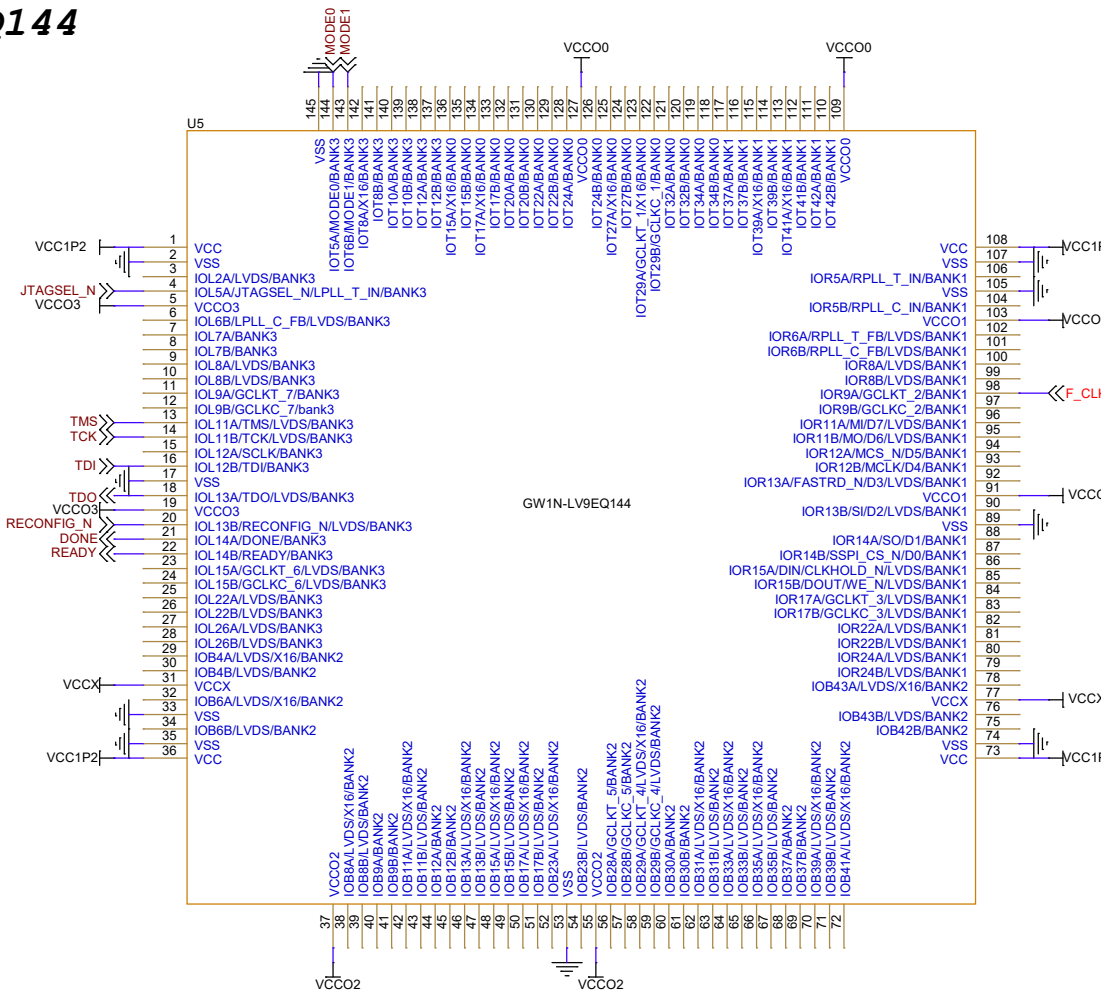


Notes:

1.F CLK signal is an external input clock signal.

It is recommended that F CLK signal be provided through an active oscillator crystal.

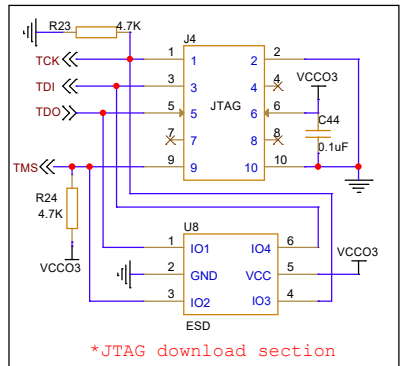
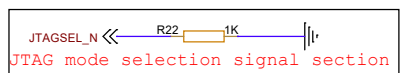
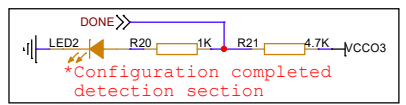
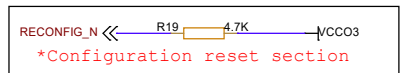
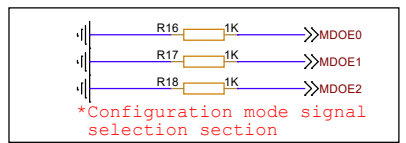
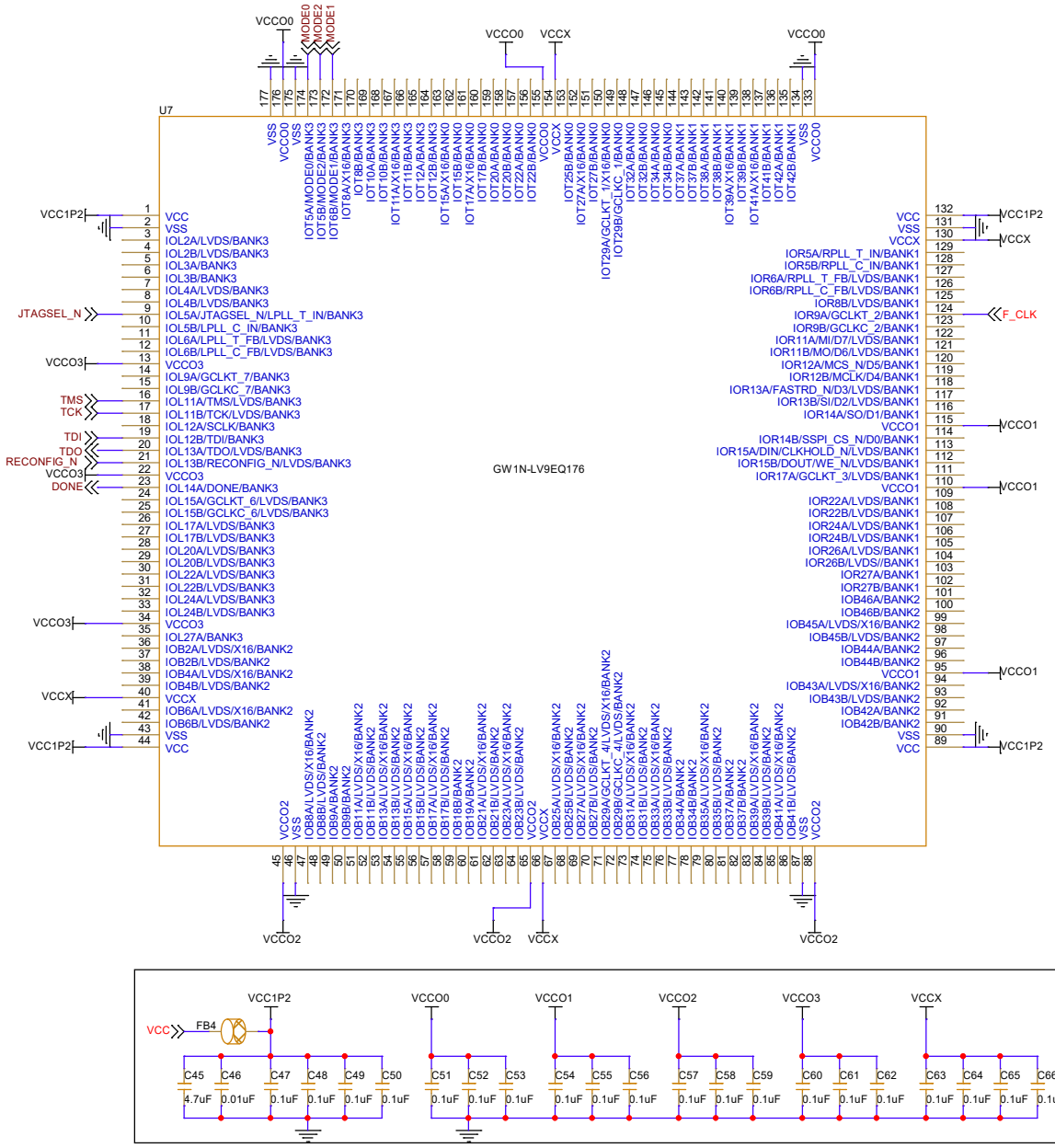
2. It is recommended that add an ESD protection chip to the JTAG download circuit.



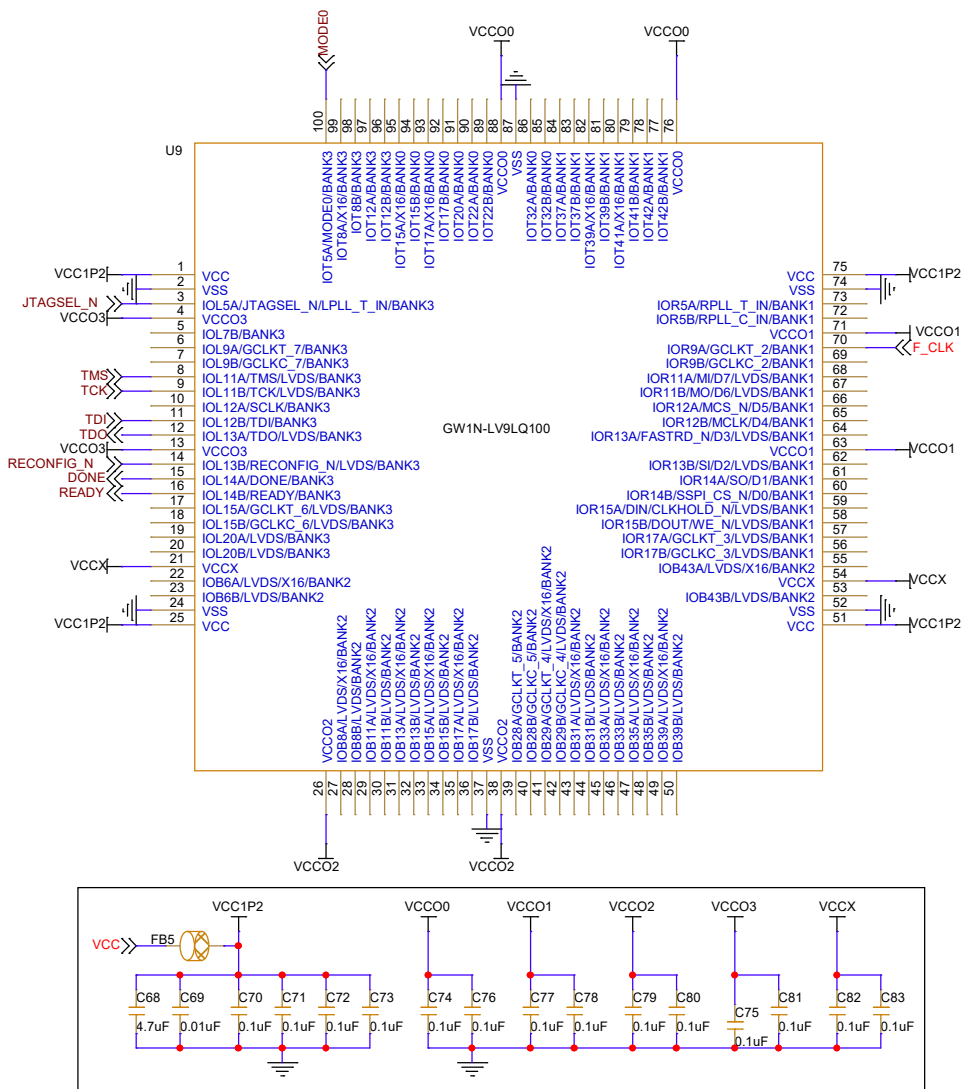
Notes:

- 1.F\_CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
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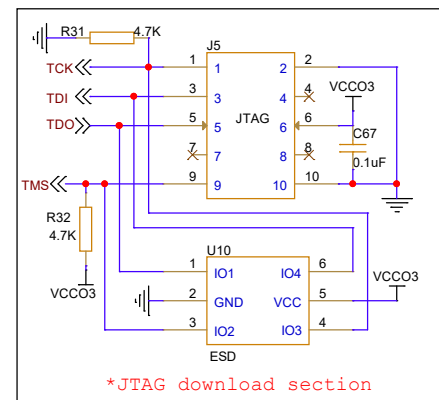
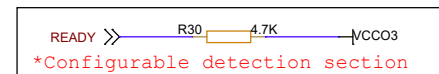
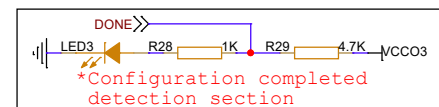
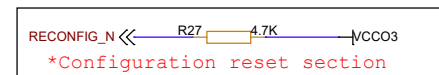
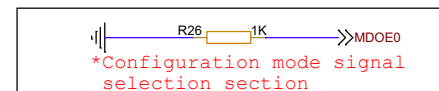
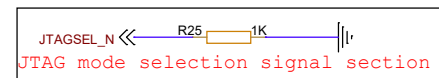


Notes:  
1.F CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.  
2.It is recommended that add an ESD protection chip to the JTAG download circuit.

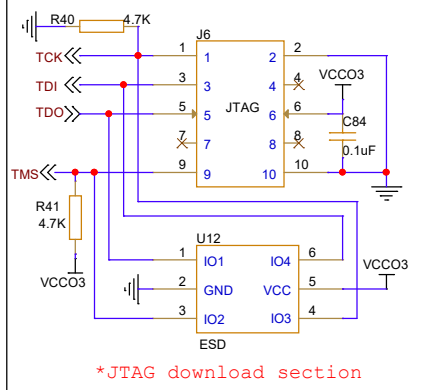
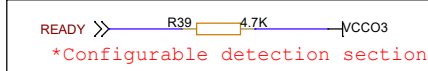
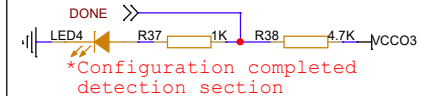
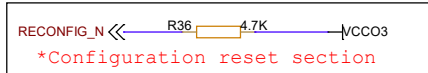
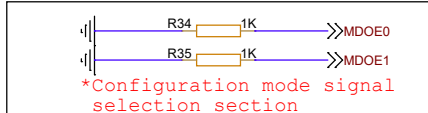
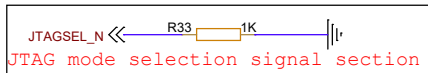
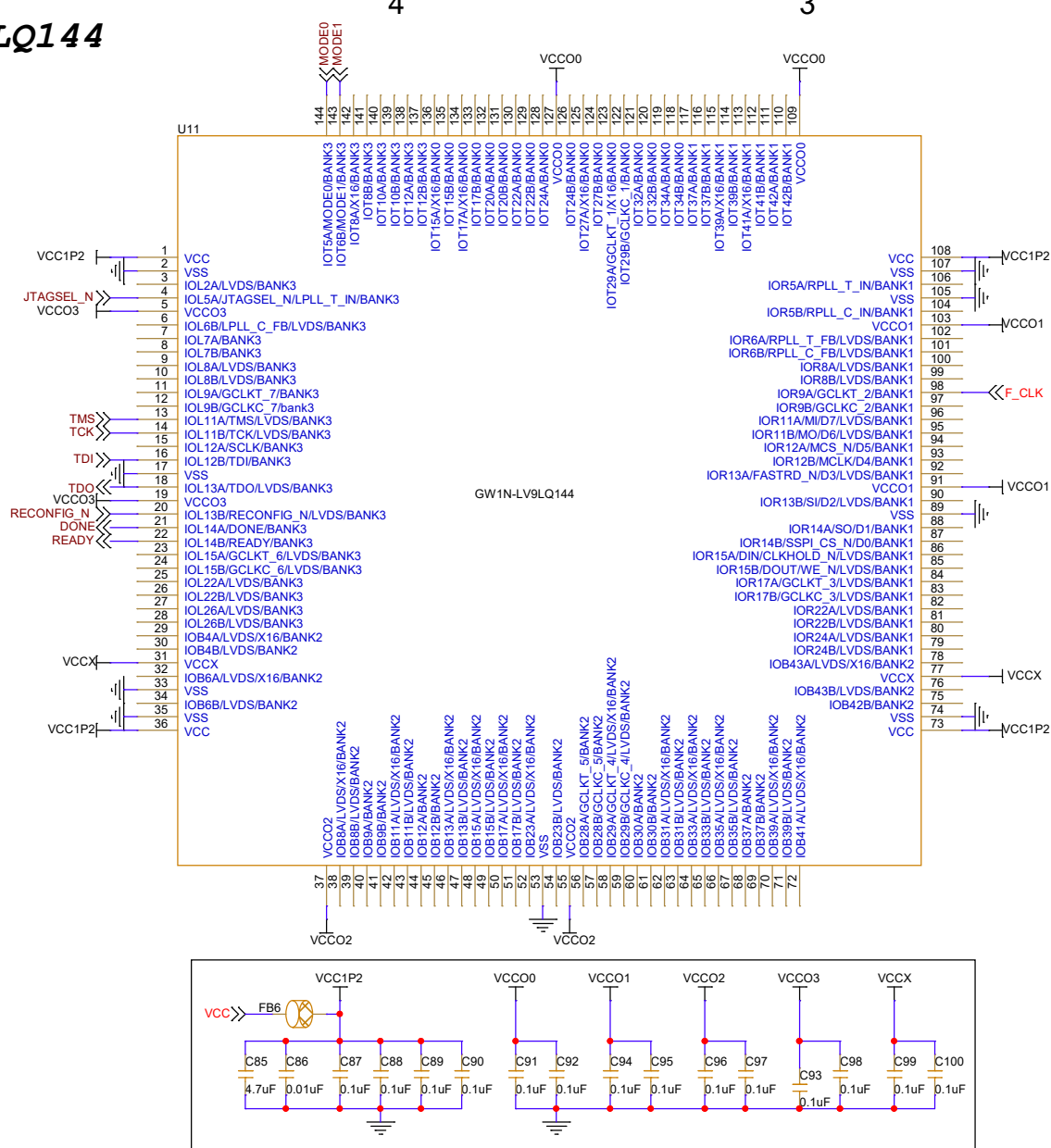


Notes:

- 1.F CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.



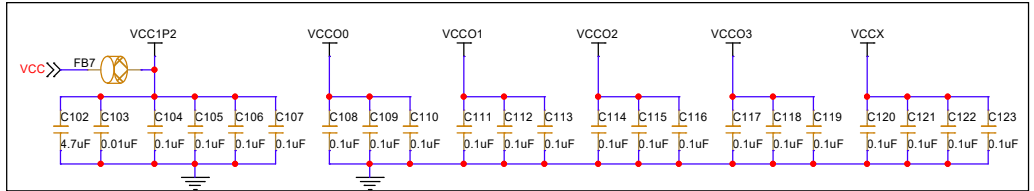
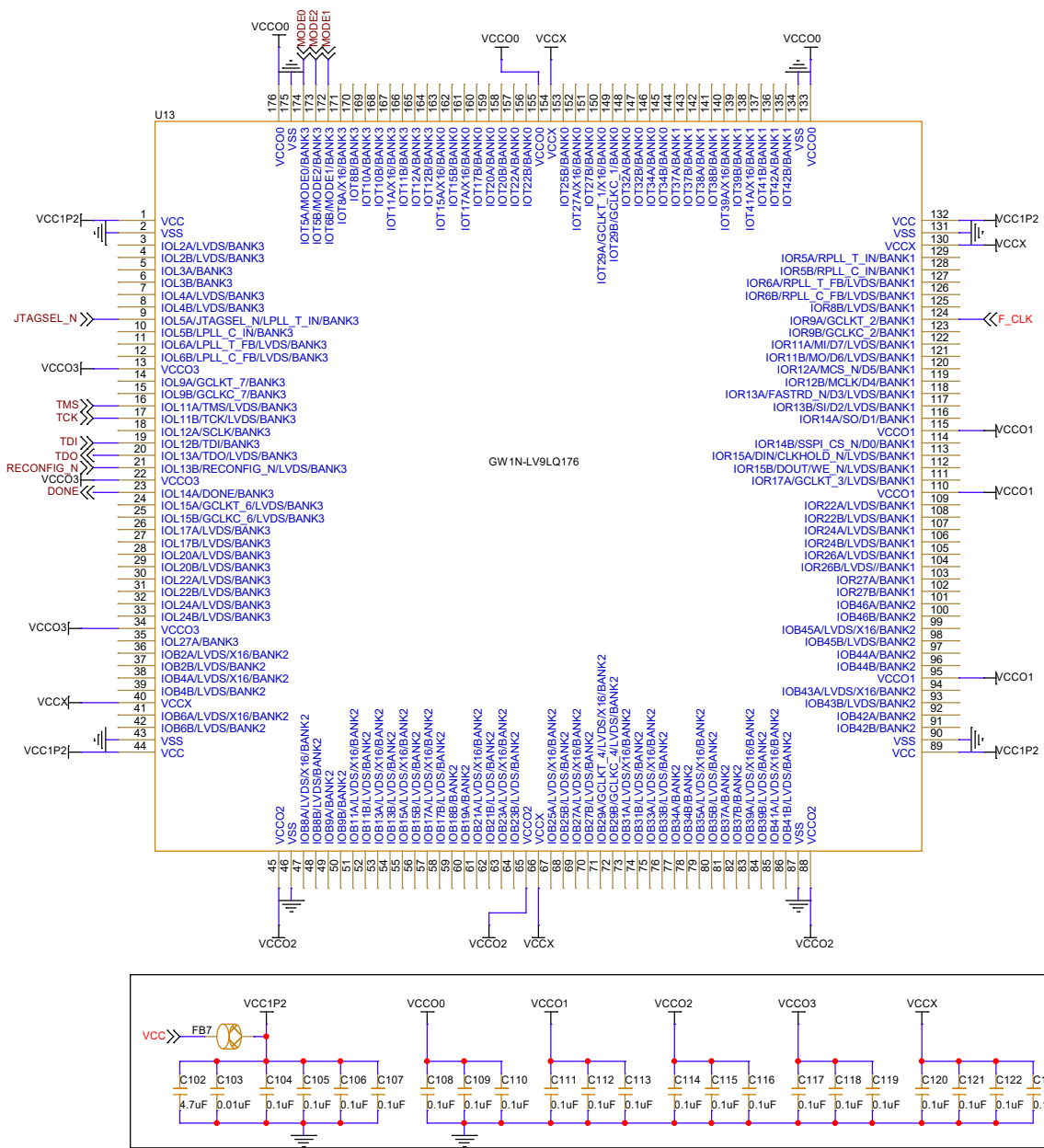
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GW1N-LV9LQ100		
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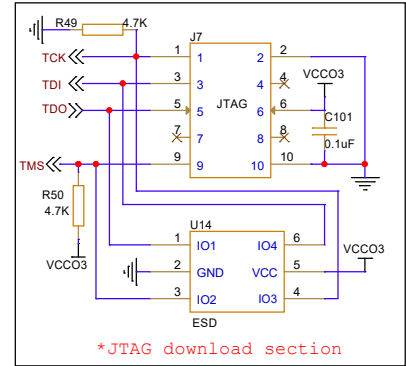
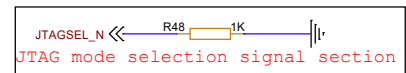
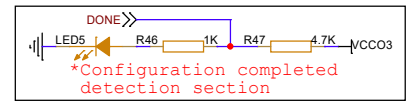
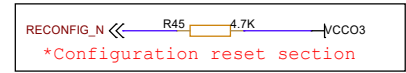
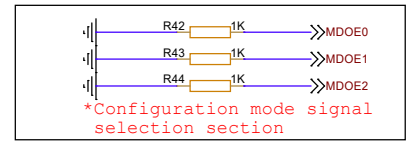
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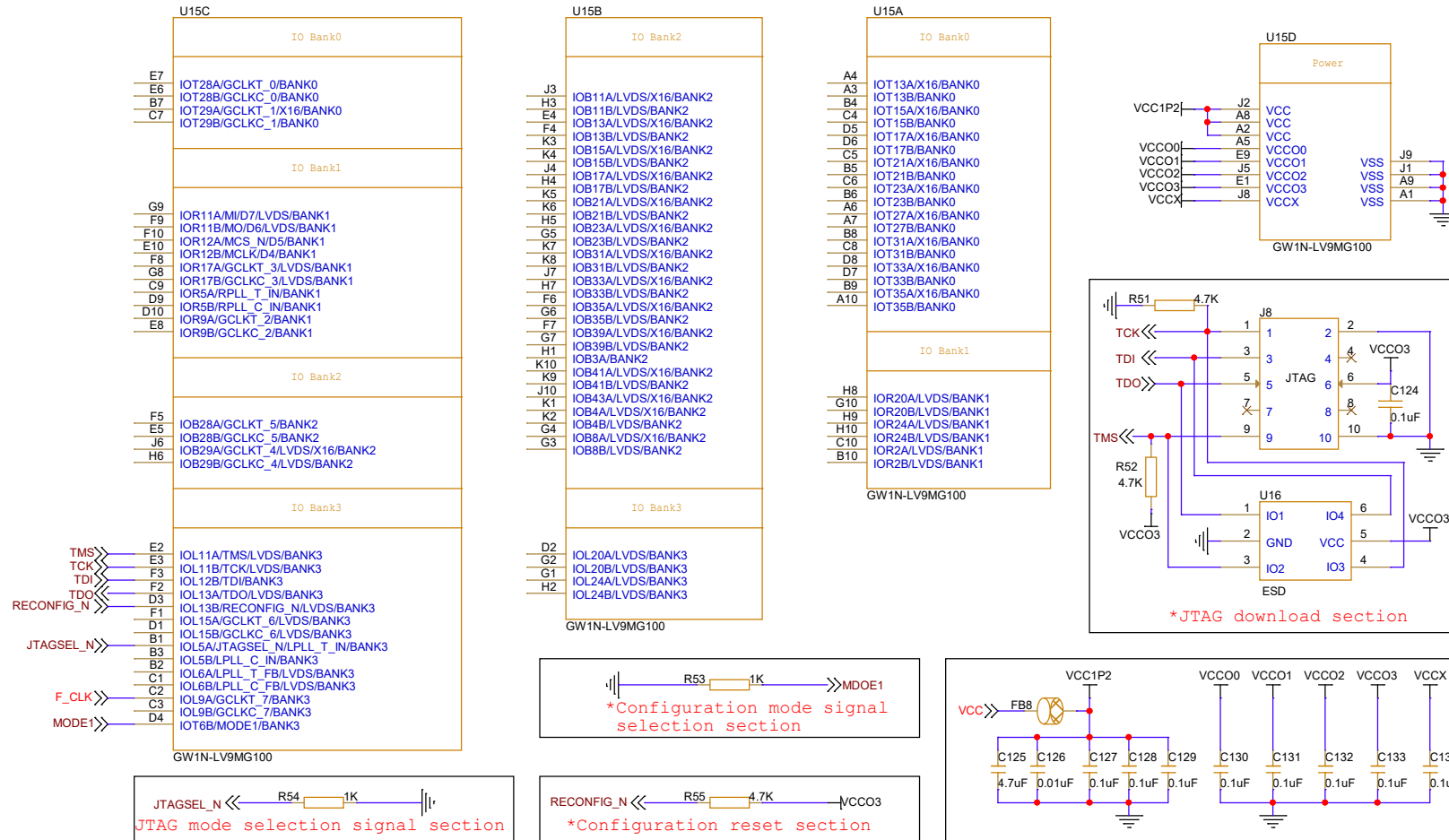
- 1.F CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
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- Notes:
- 1.F CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.
  - 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

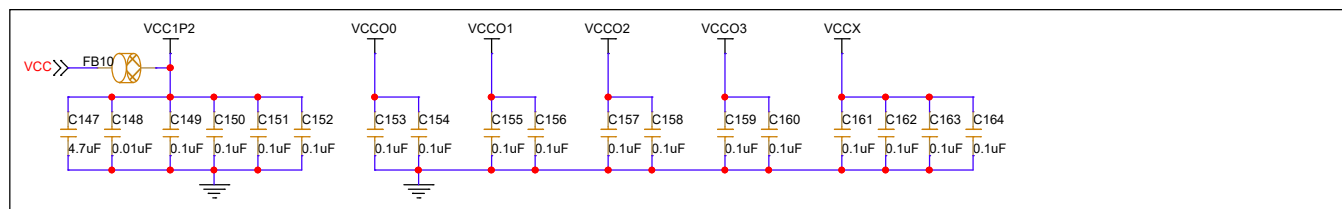
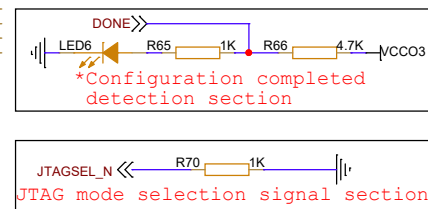
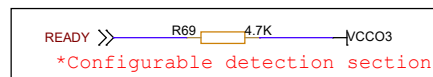
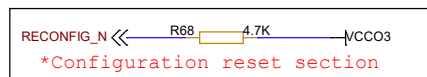
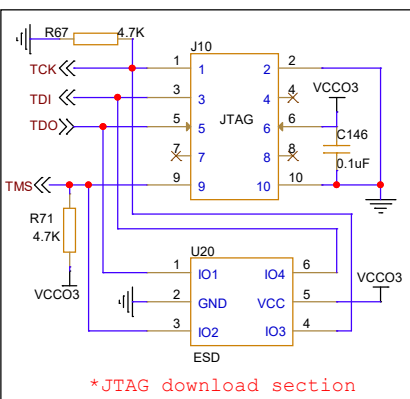
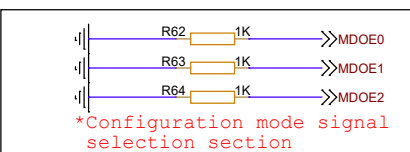
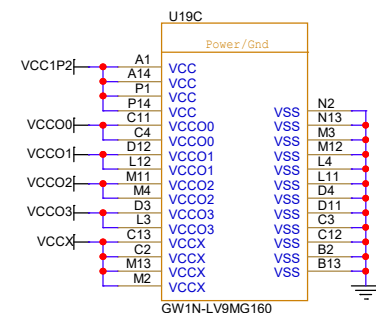
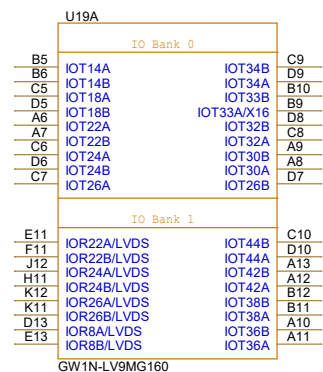
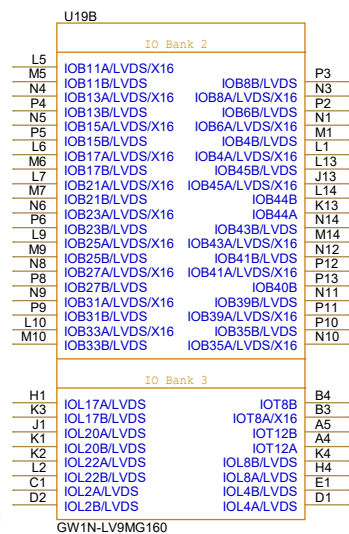
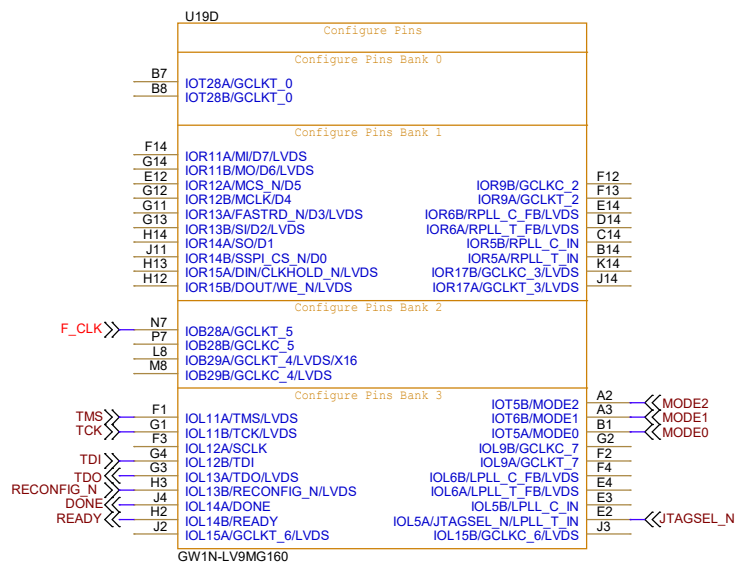






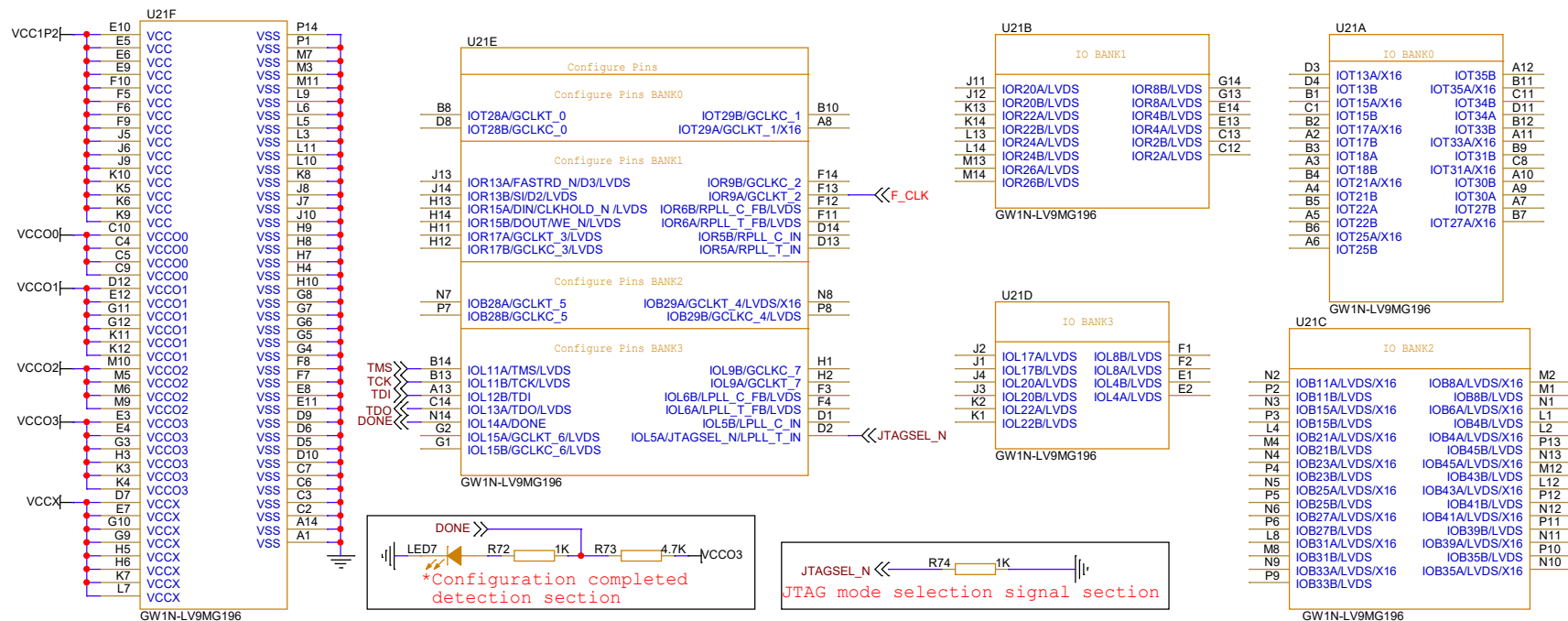


5  
***GW1N-LV9MG1 60***



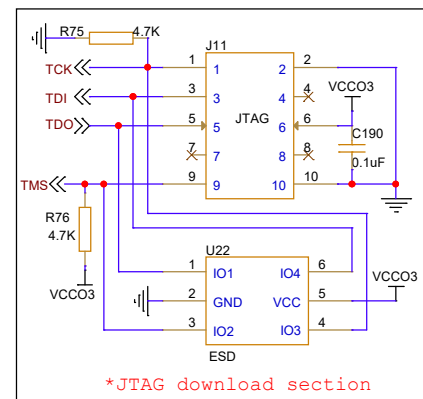
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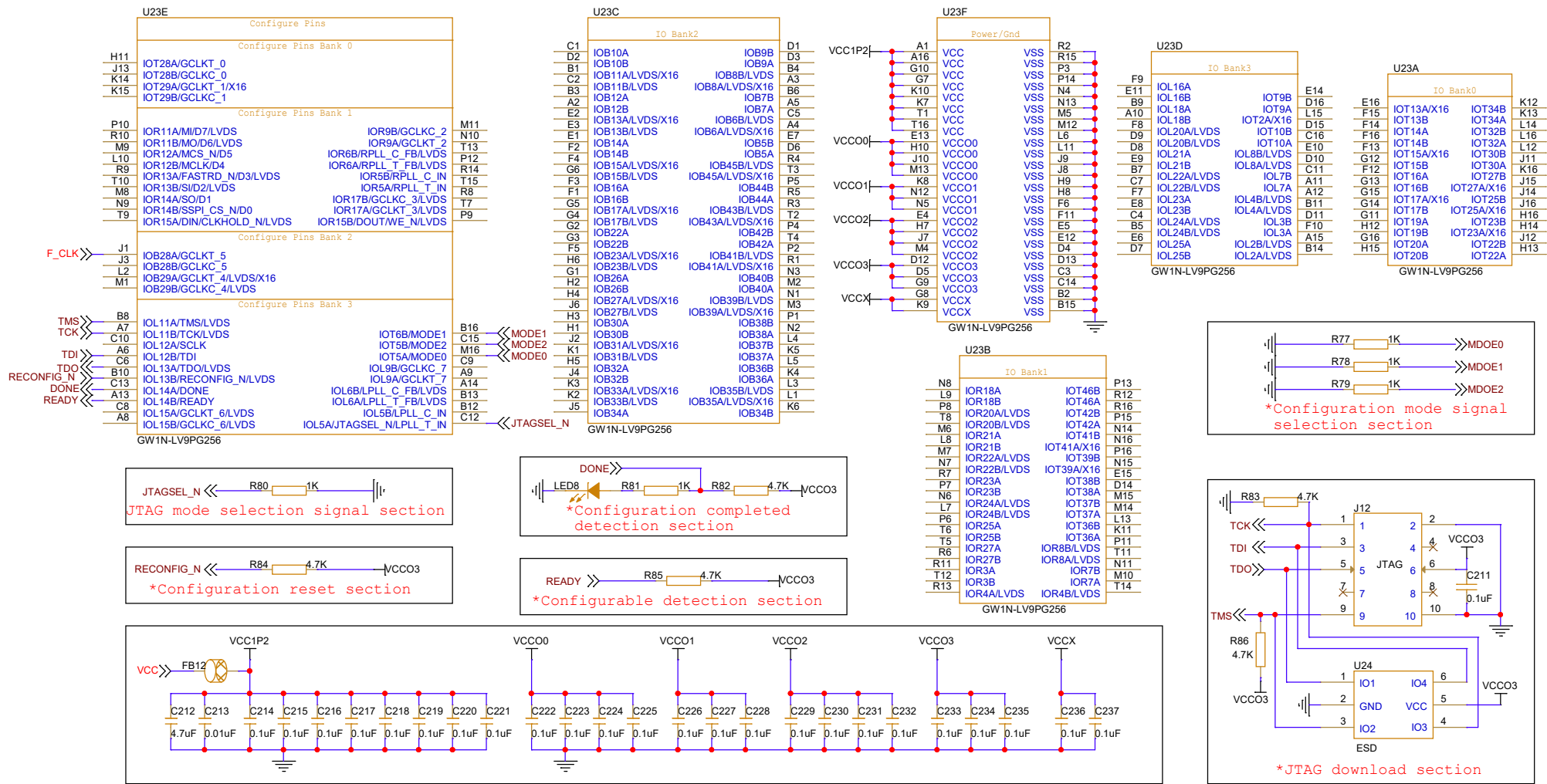
- 1.F CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.



#### Notes:

- 1.F CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.



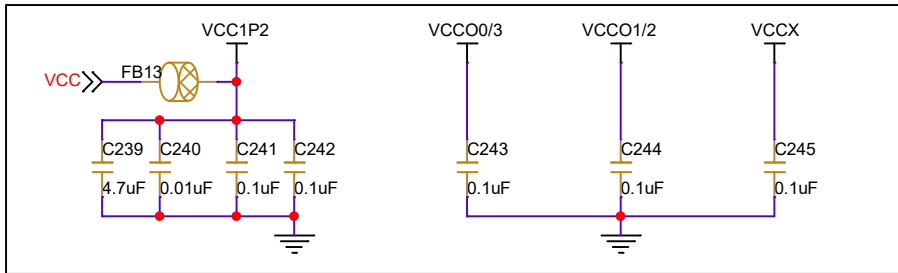
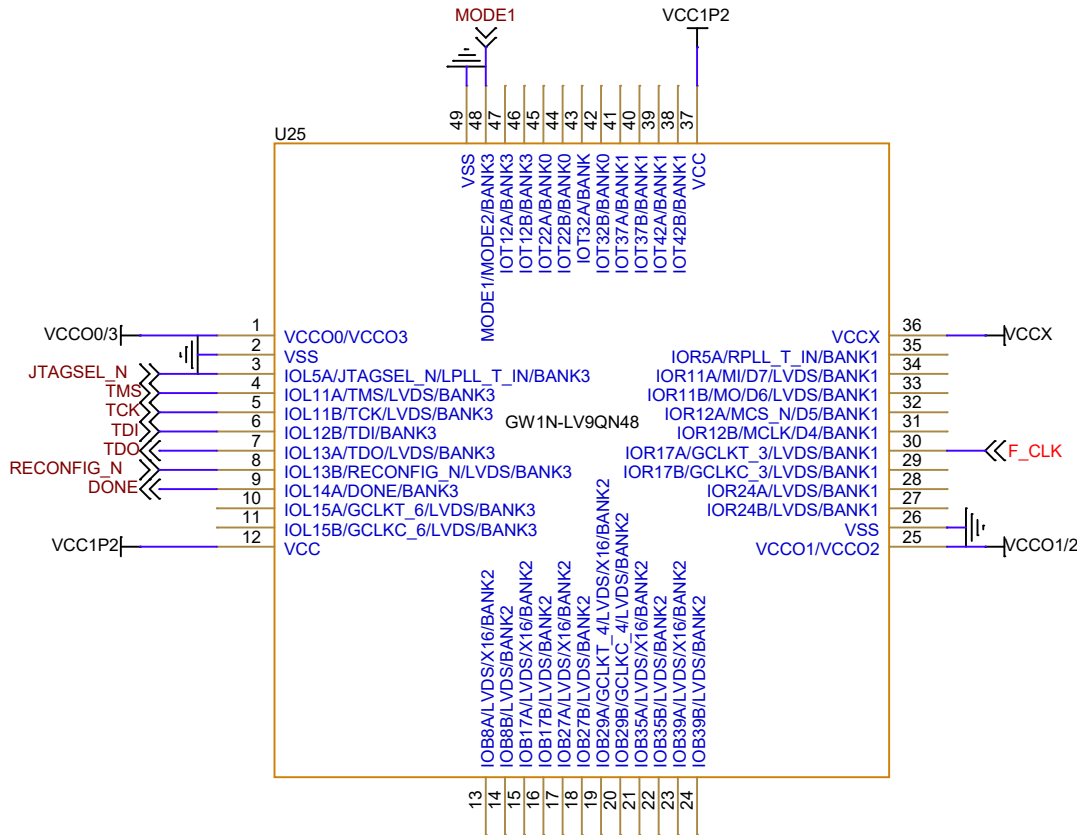


#### Notes:

1. F\_CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.

Title			
GOWIN Minimum System Diagram			
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B	GW1N-LV9PG256	2.2	
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# GW1N-LV9QN48



## Notes:

1.F\_CLK signal is an external input clock signal.

It is recommended that F\_CLK signal be provided through an active oscillator crystal.

2.It is recommended that add an ESD protection chip to the JTAG download circuit.

R87 1K MDOE1  
\*Configuration mode signal selection section

R88 4.7K RECONFIG\_N VCC00/3  
\*Configuration reset section

DONE LED9 R89 1K R90 4.7K VCC00/3  
\*Configuration completed detection section

R91 1K JTAGSEL\_N  
JTAG mode selection signal section

R92 4.7K J13 JTAG TCK TDI TDO TMS R93 4.7K VCC00/3 C238 0.1uF U26 ESD  
\*JTAG download section

Title  
GOWIN Minimum System Diagram

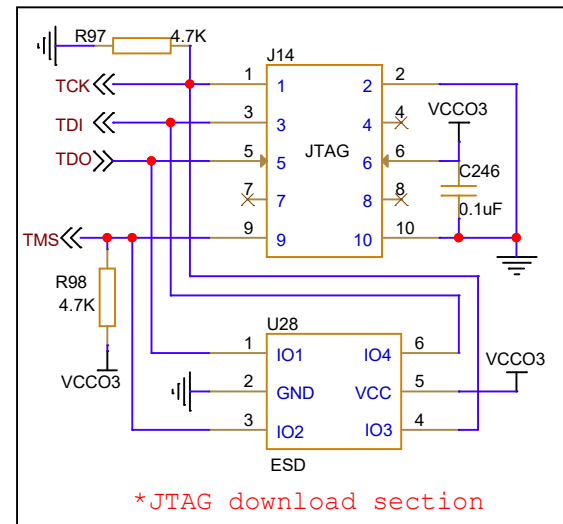
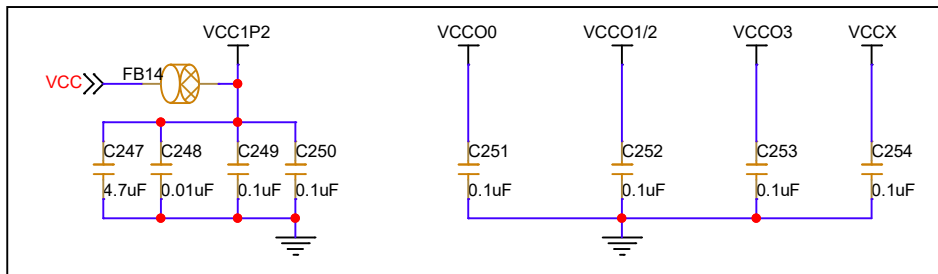
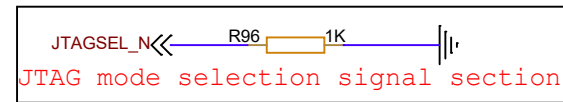
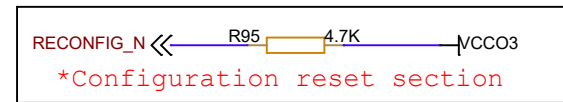
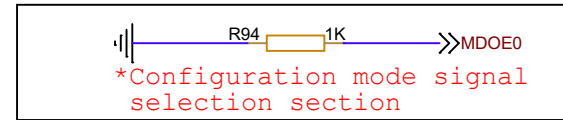
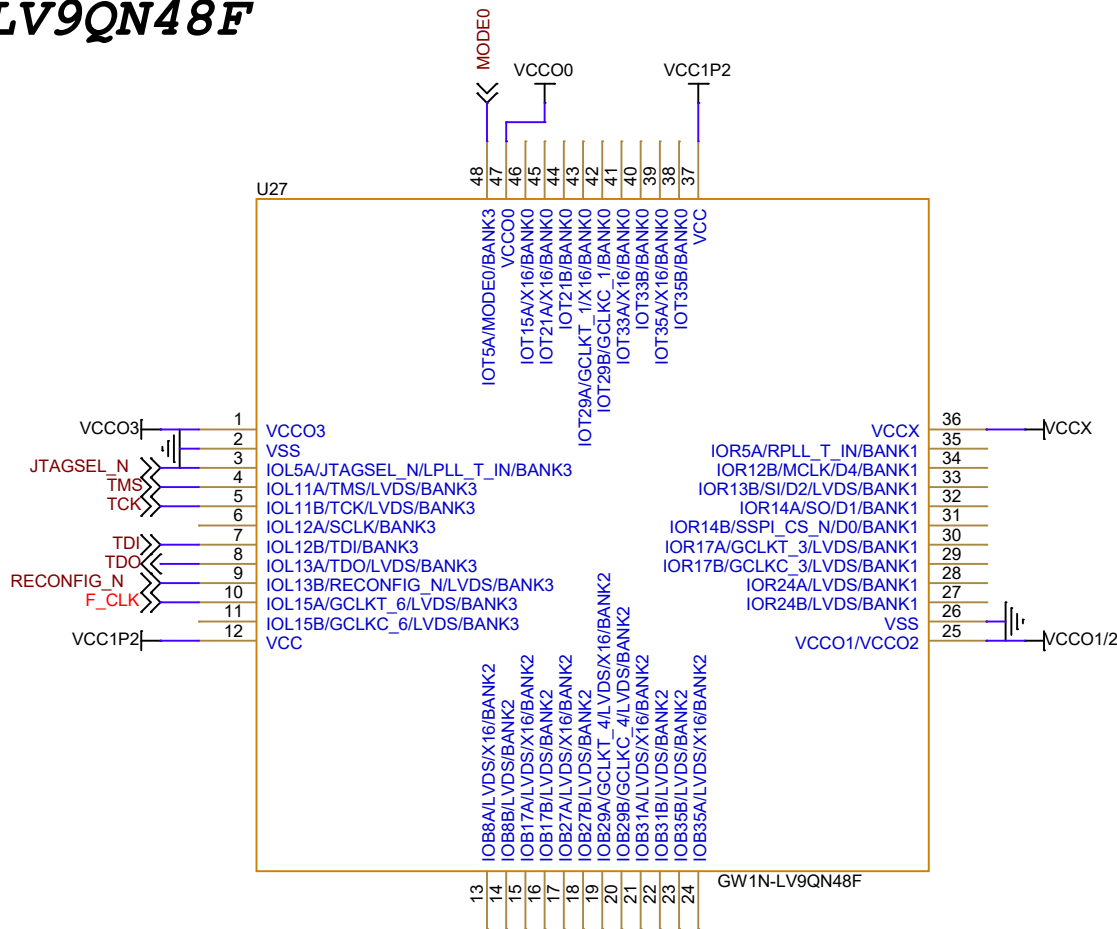
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GW1N-LV9QN48

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# GW1N-LV9QN48F



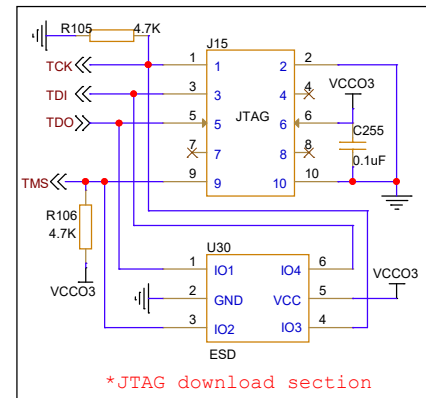
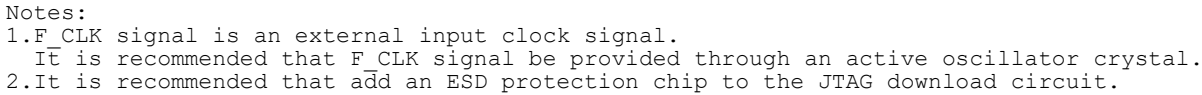
## Notes:

1.F CLK signal is an external input clock signal.

It is recommended that F CLK signal be provided through an active oscillator crystal.

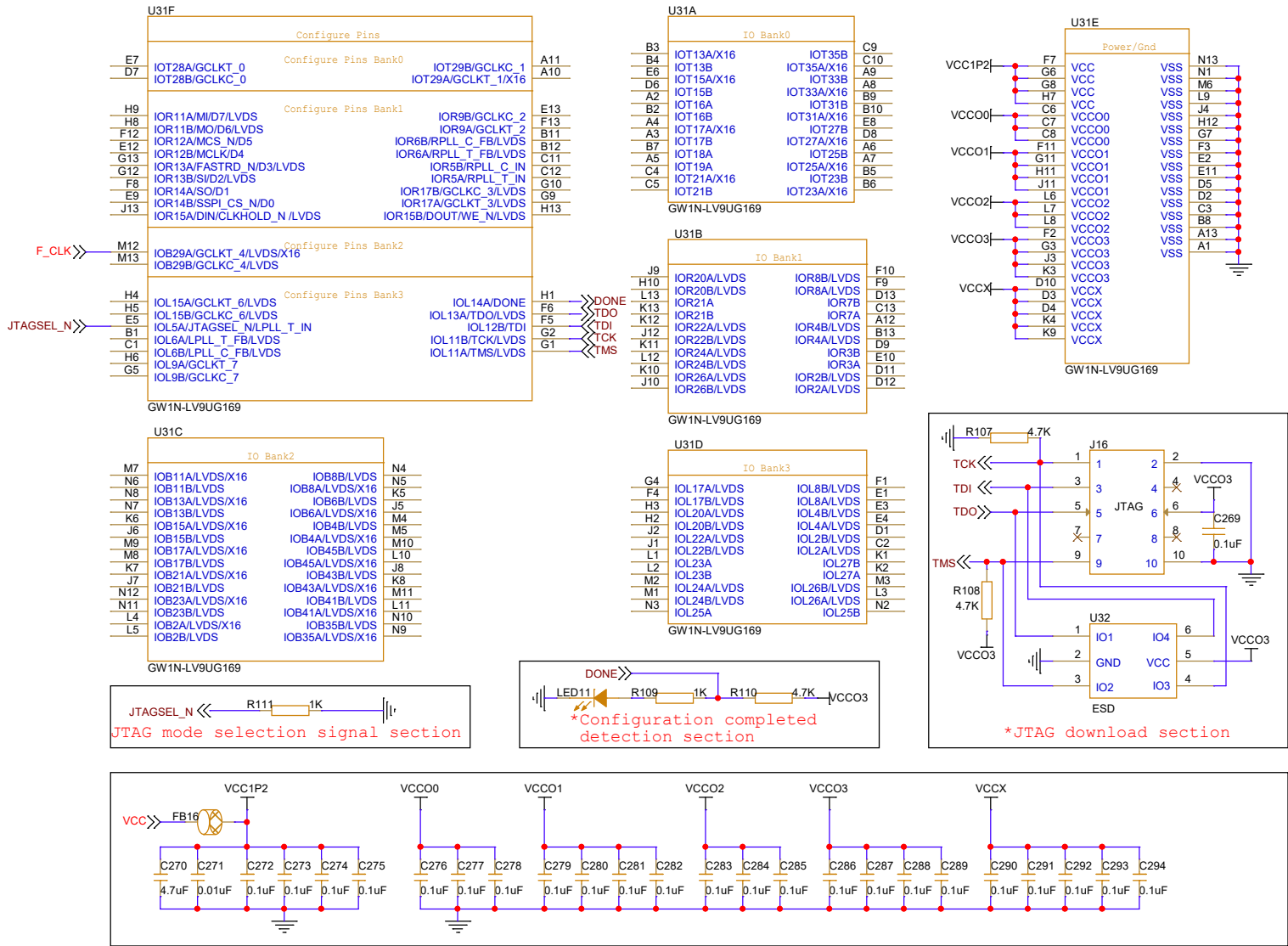
2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
A4	GW1N-LV9QN48F	2.2
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GOWIN Minimum System Diagram			
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D

D

C

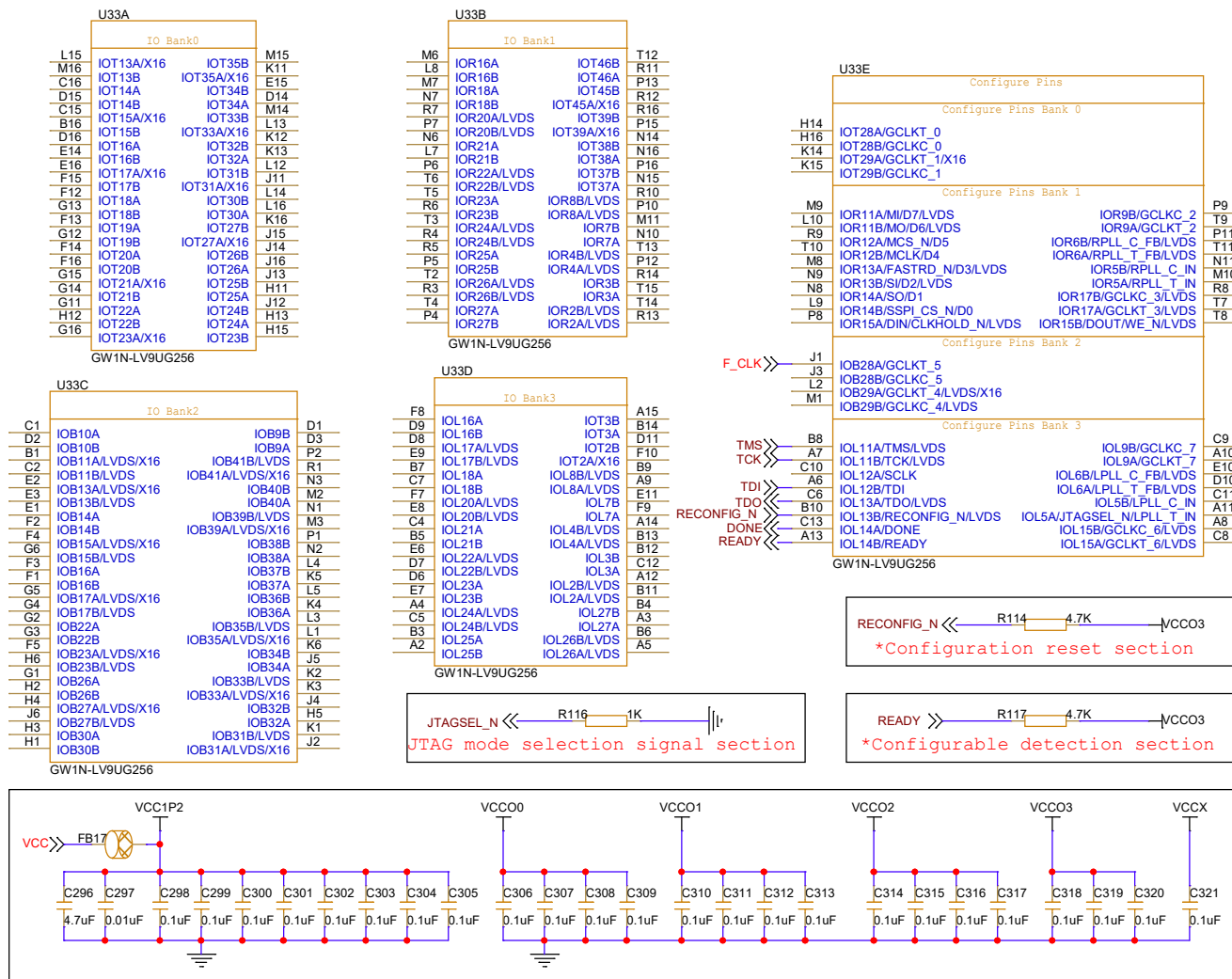
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B

B

A

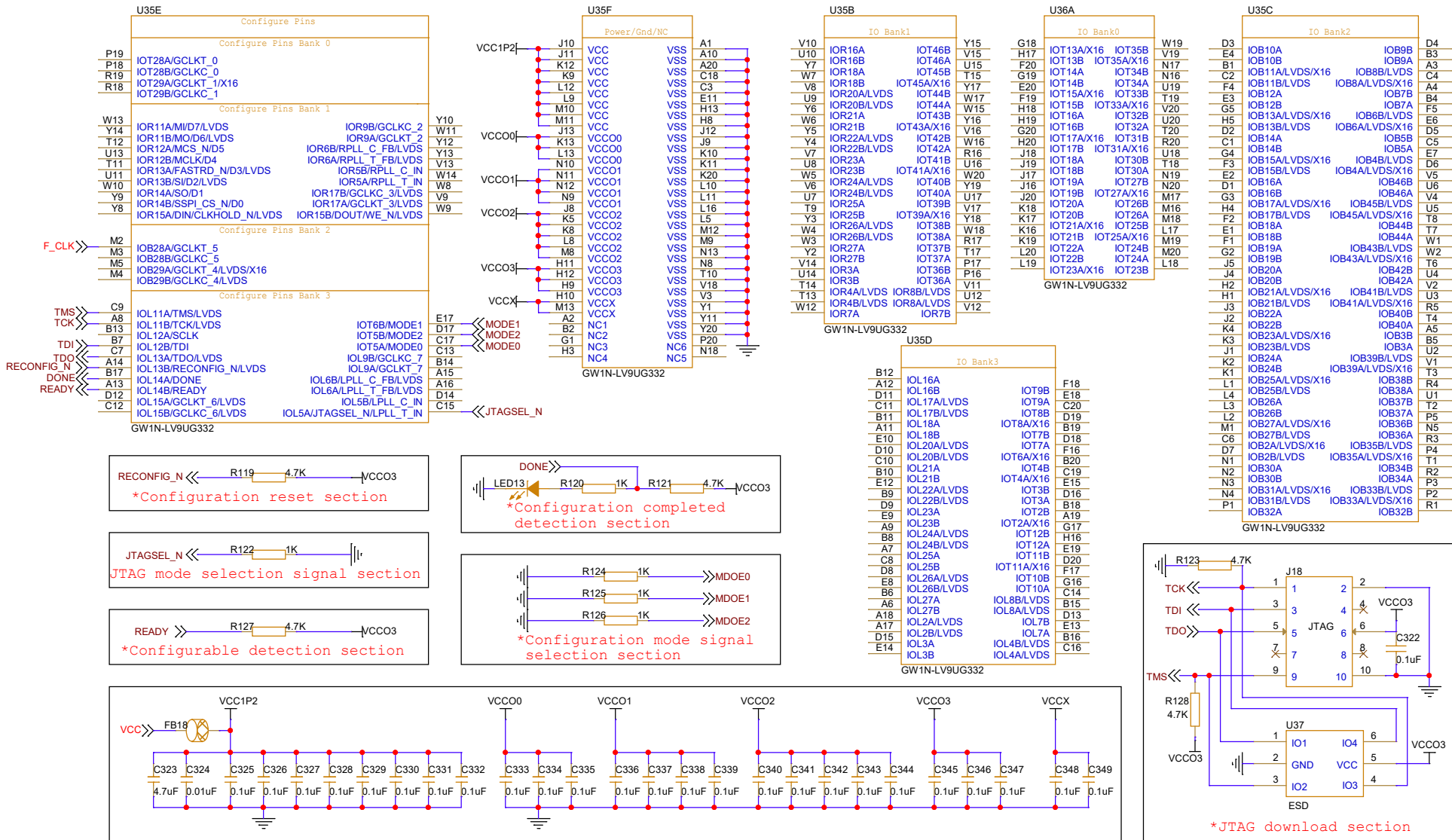
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# Notes:

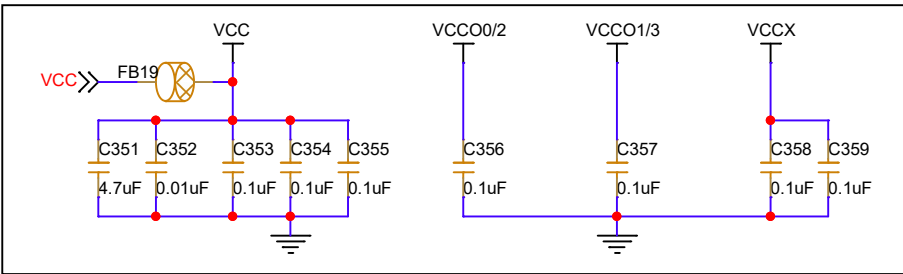
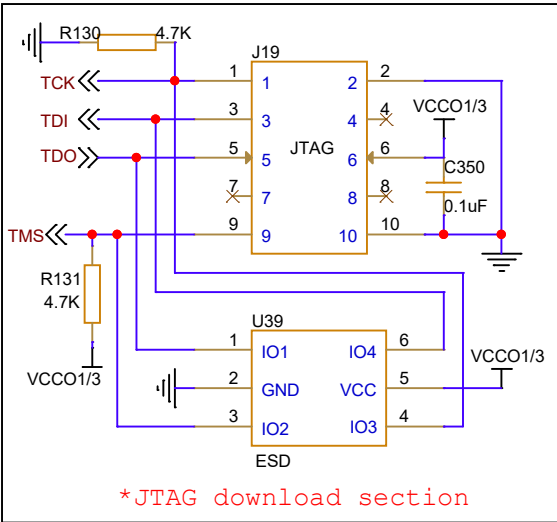
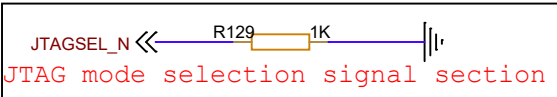
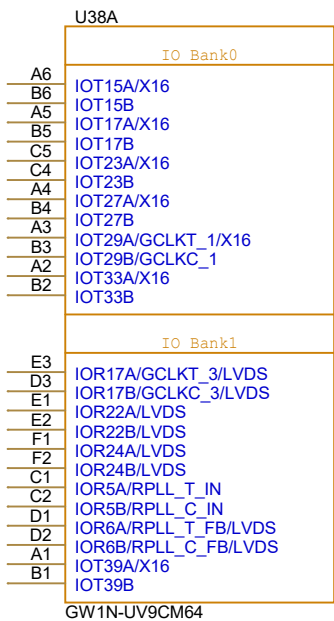
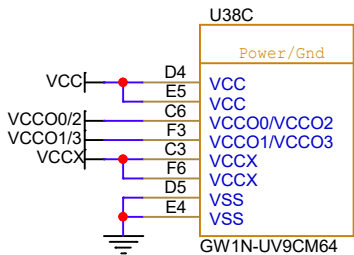
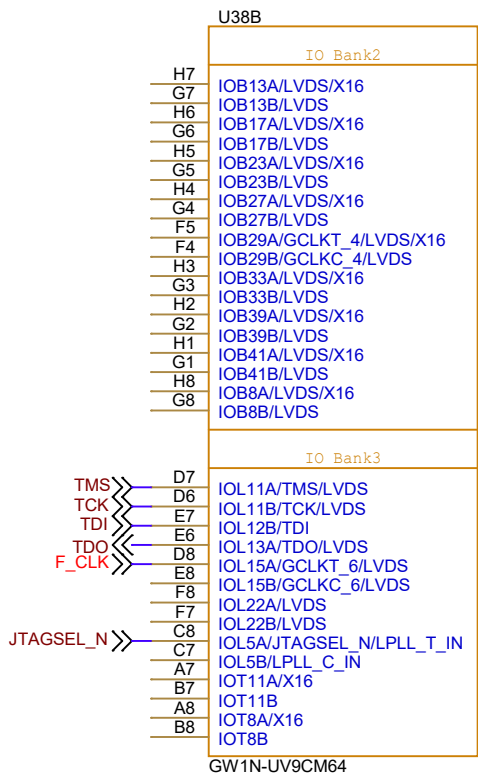
- 1.F CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
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B	GW1N-LV9UG256	2.2
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GOWIN Minimum System Diagram		
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GW1N-UV9CM64

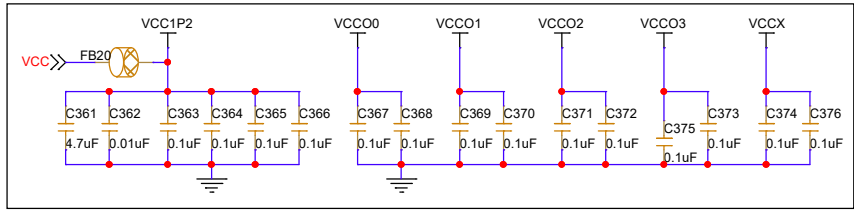
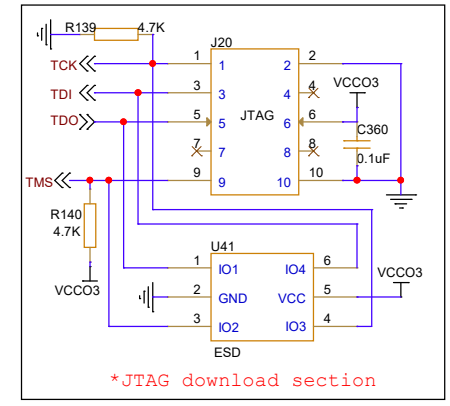
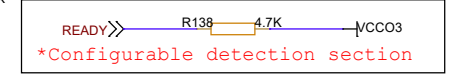
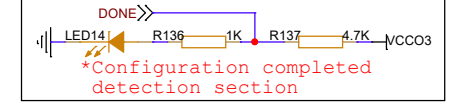
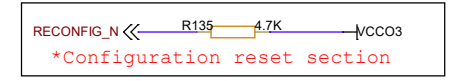
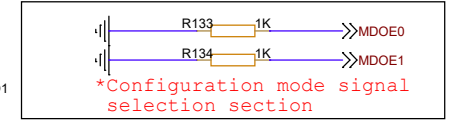
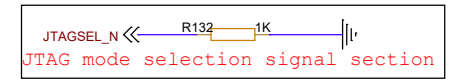
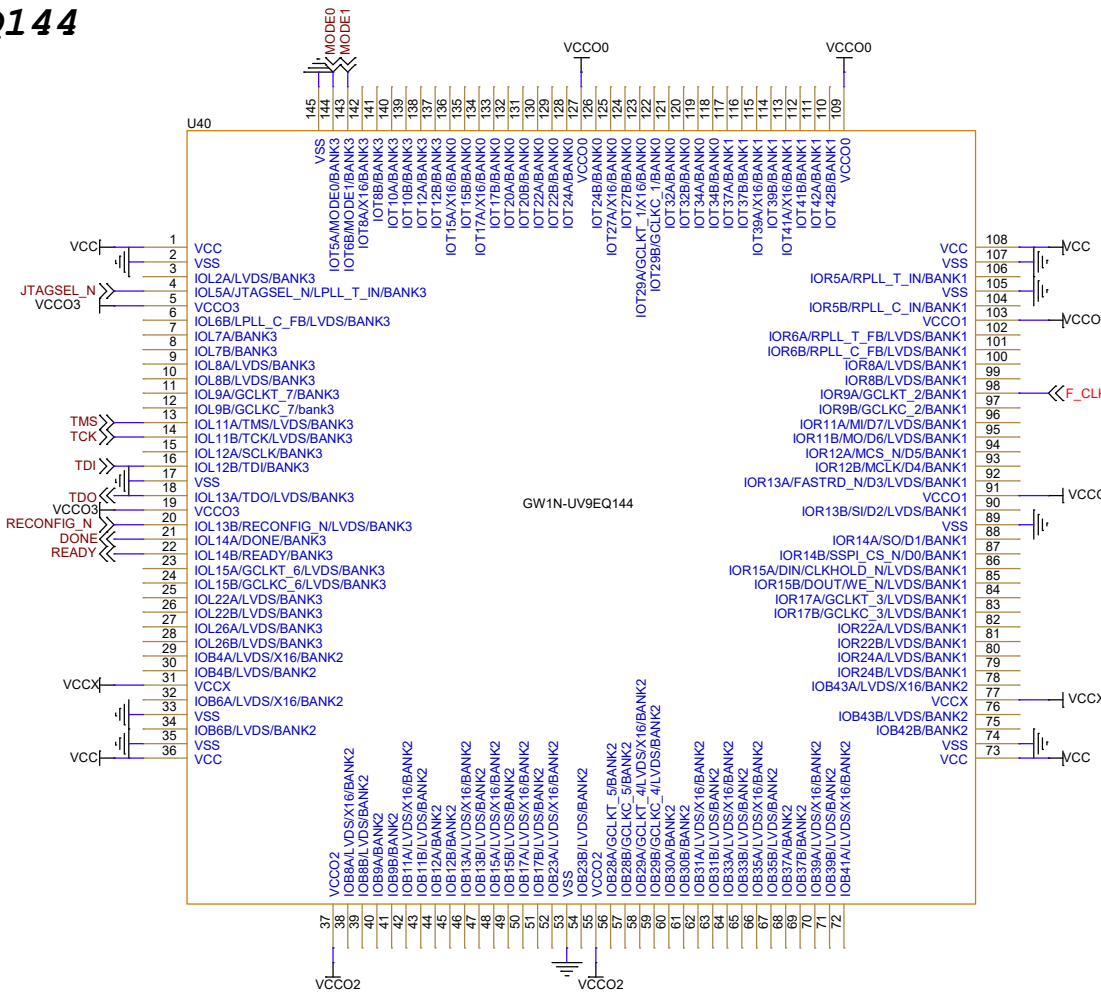


Notes:

1.F\_CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.

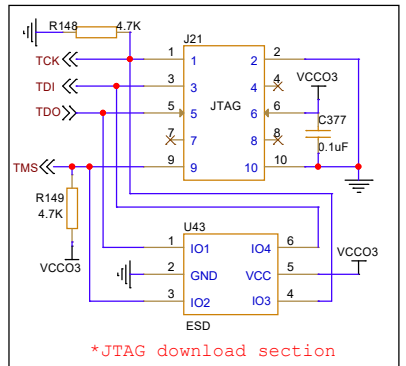
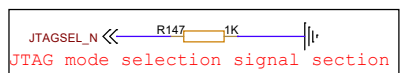
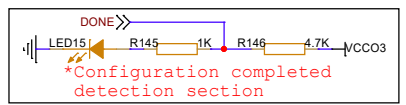
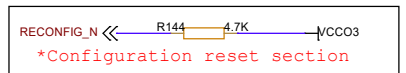
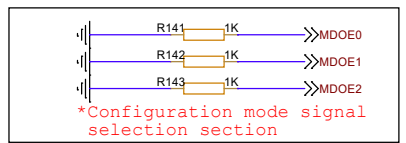
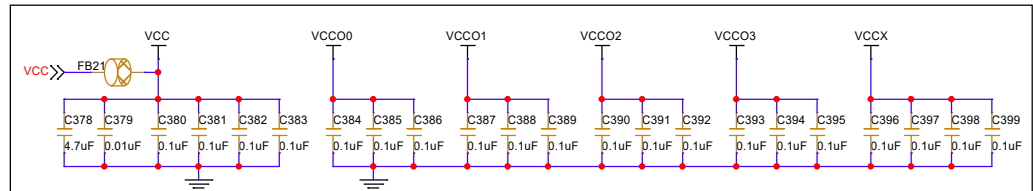
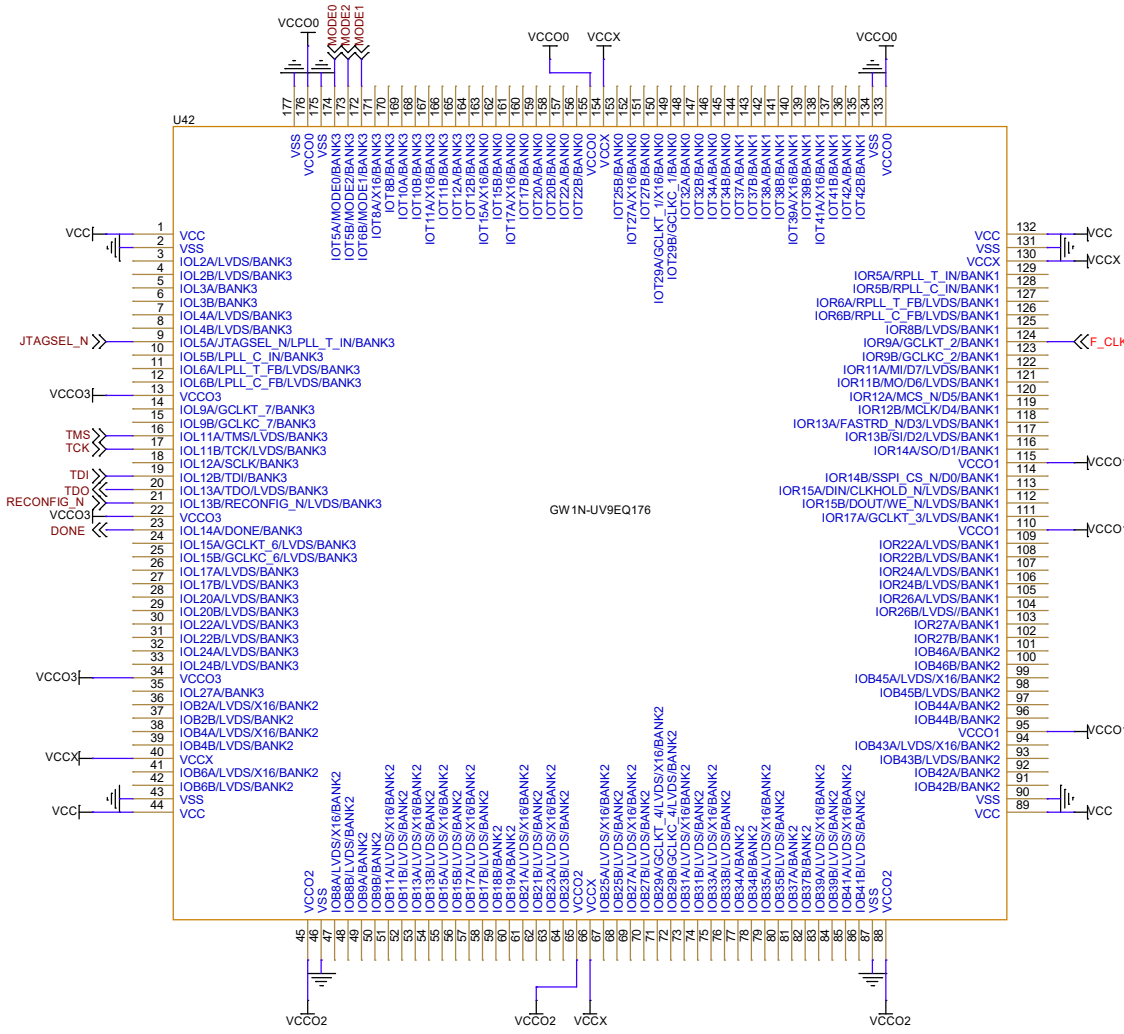
2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
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A4	GW1N-UV9CM64	2.2
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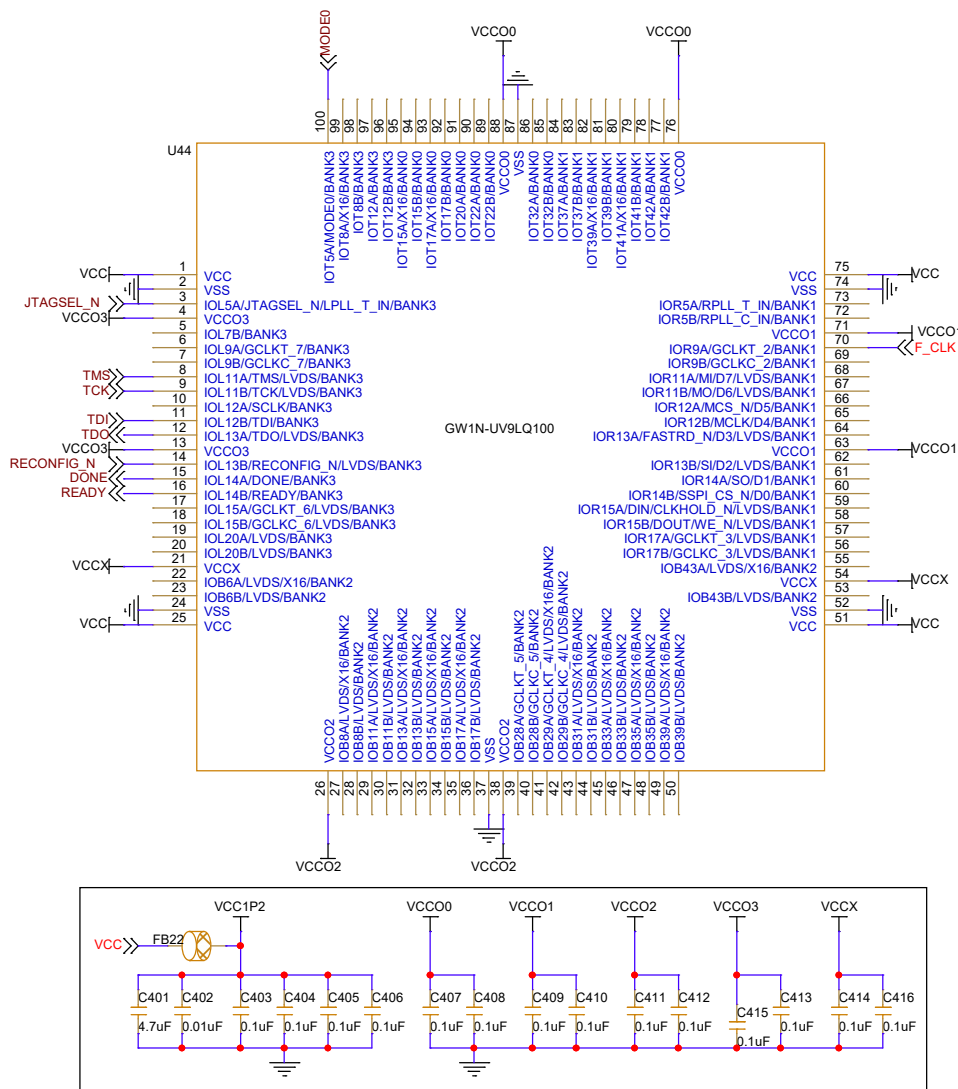


Notes:  
1.F CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.  
2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
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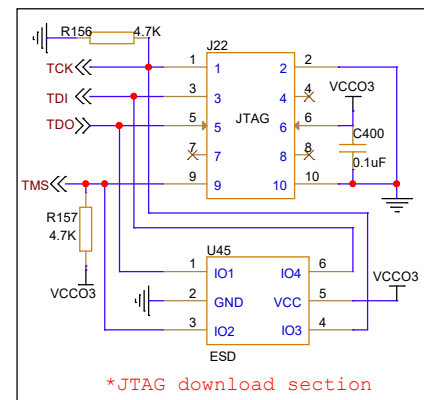
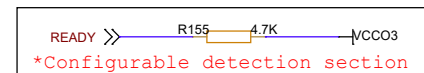
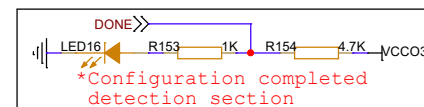
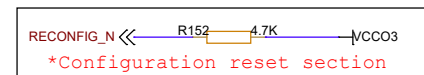
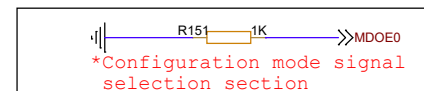
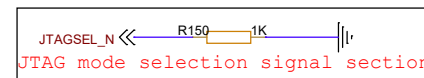


Notes:  
1.F CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.  
2.It is recommended that add an ESD protection chip to the JTAG download circuit.

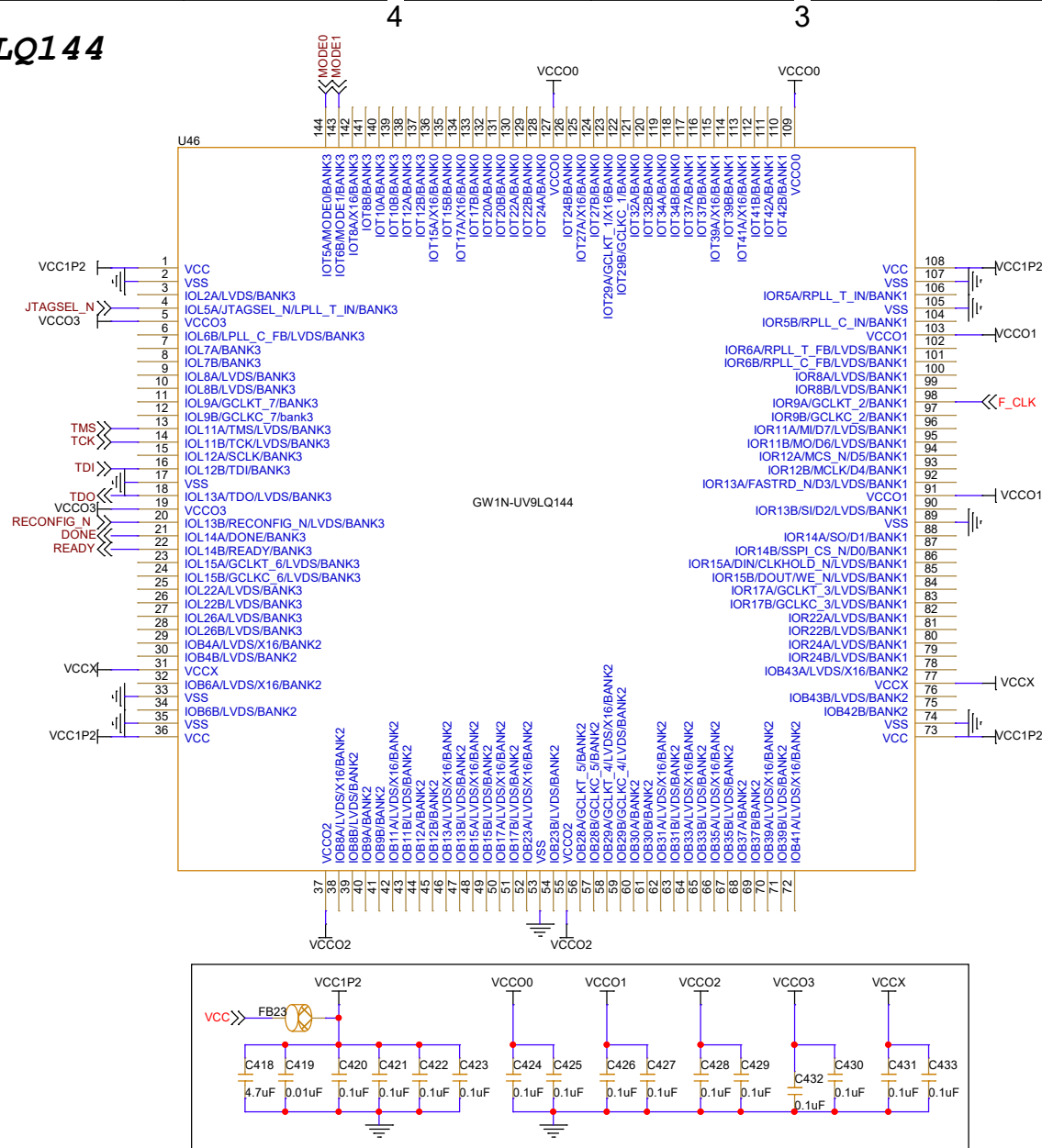


Notes:

- 1.F CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

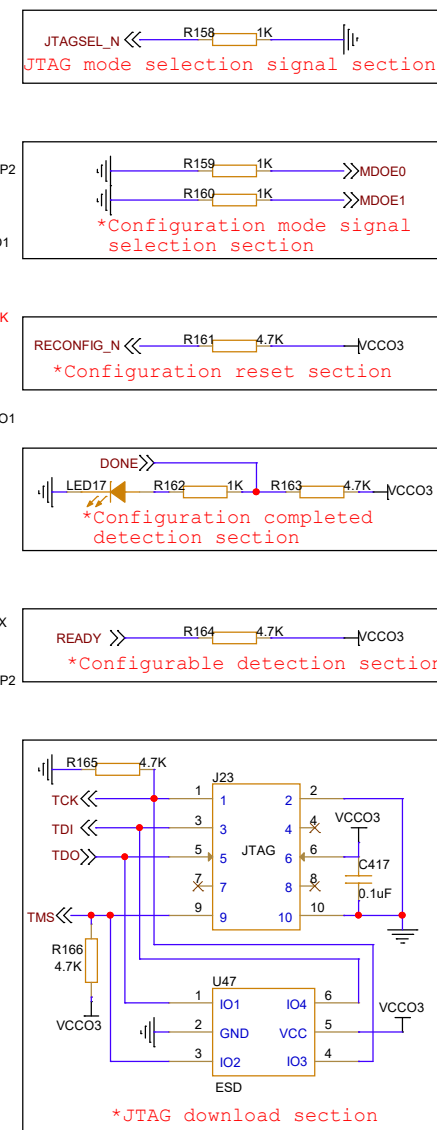


Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-UV9LQ100	2.2
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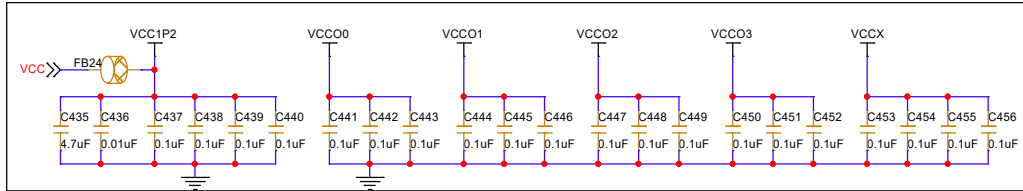
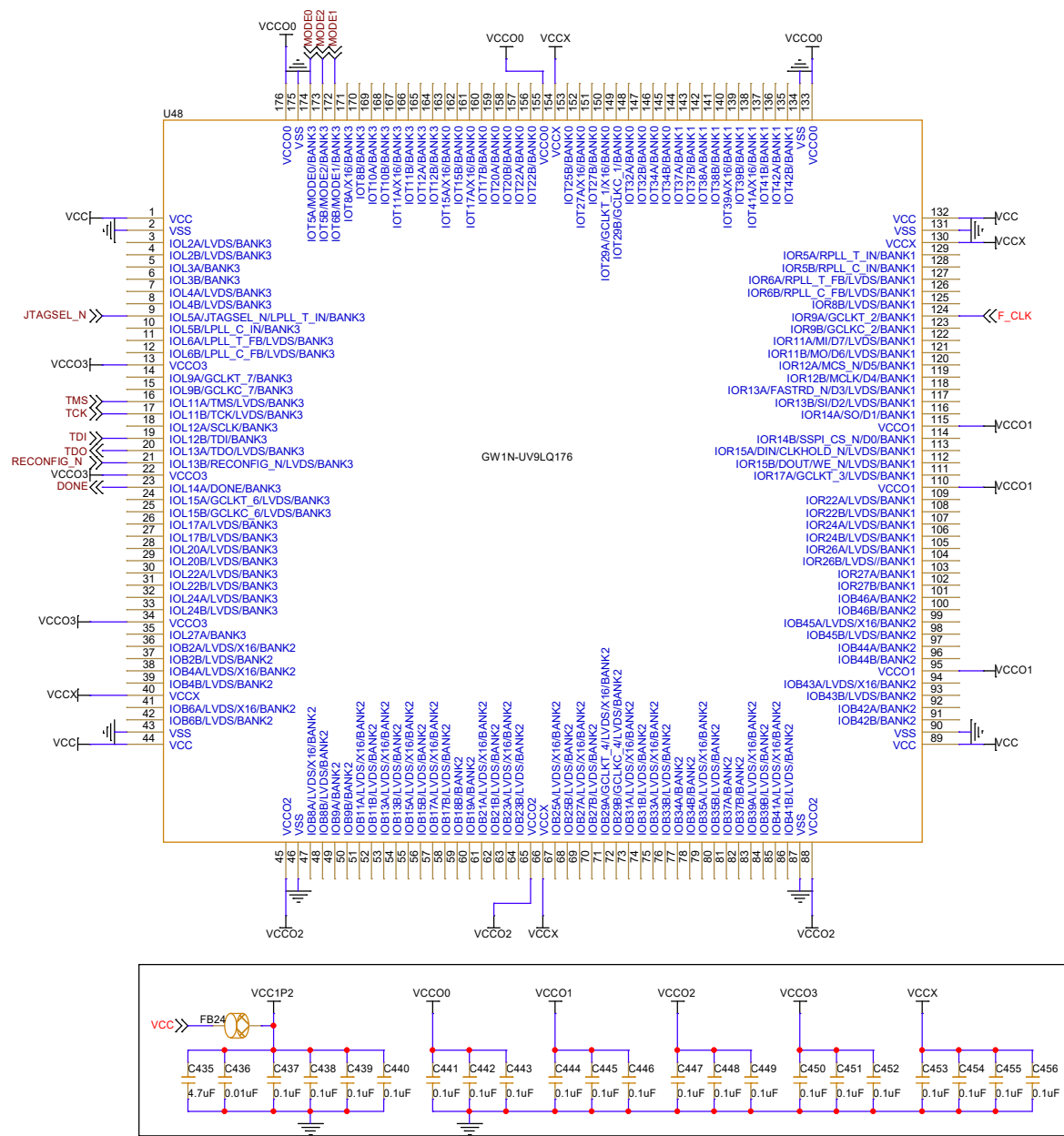
Notes:

- NOTES:
- 1.F CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.
  - 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

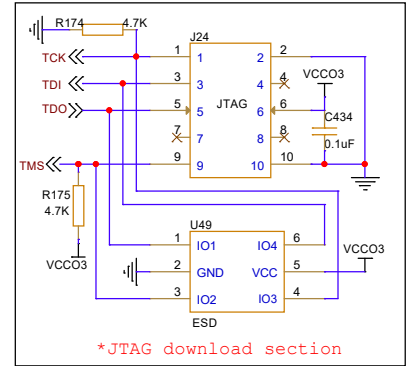
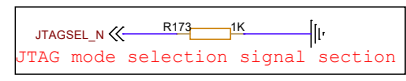
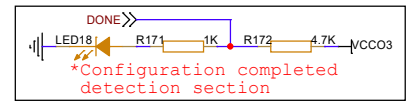
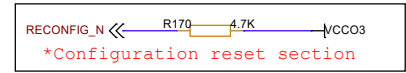
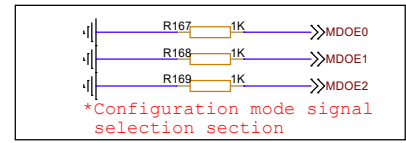


Title				
GOWIN Minimum System Diagram				
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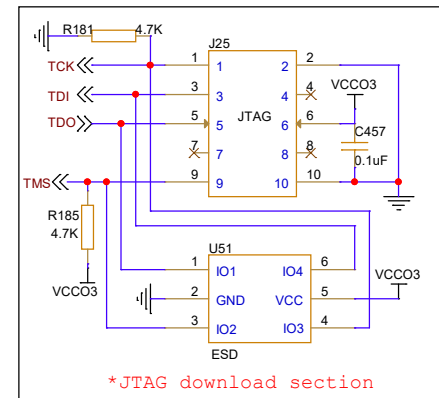
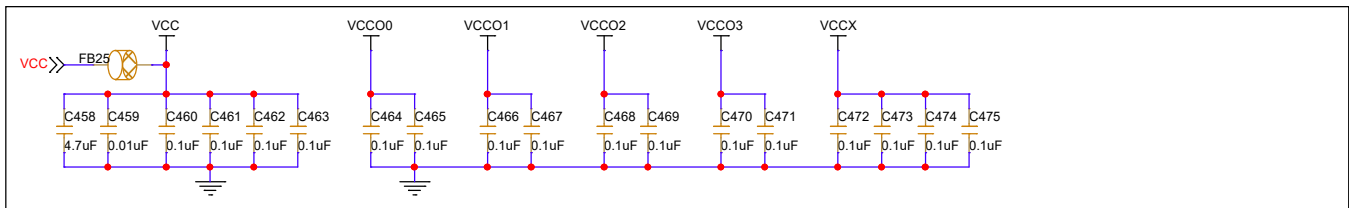
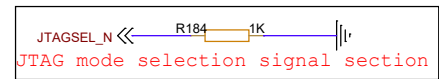
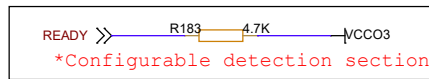
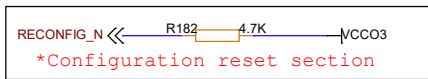
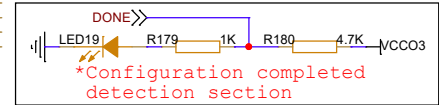
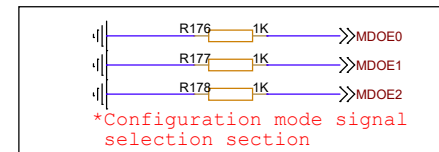
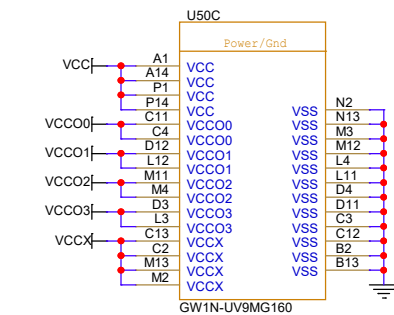
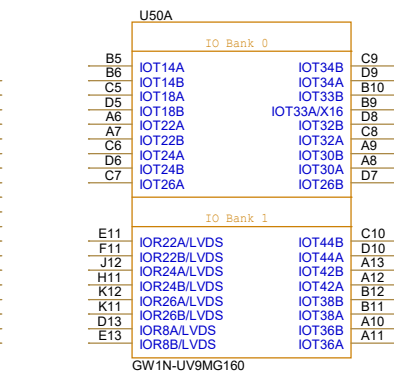
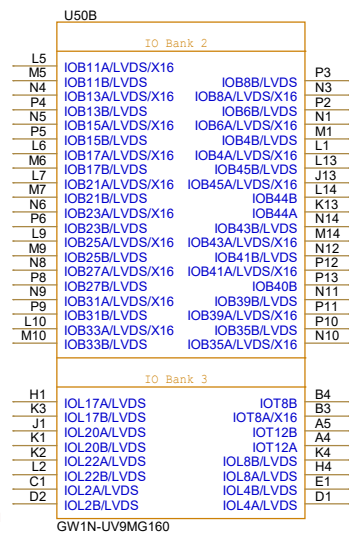
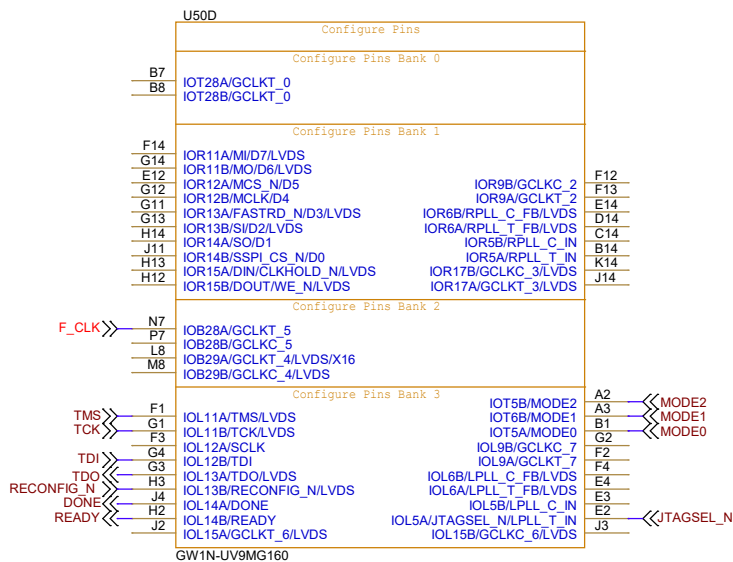




- Notes:
- 1.F CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.
  - 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

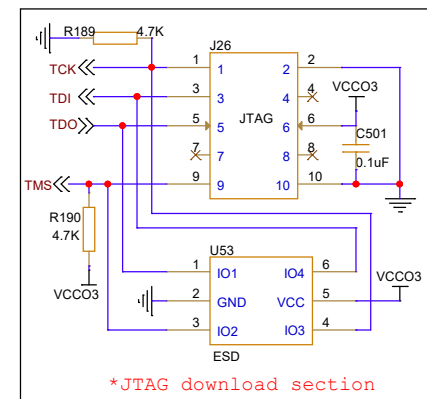
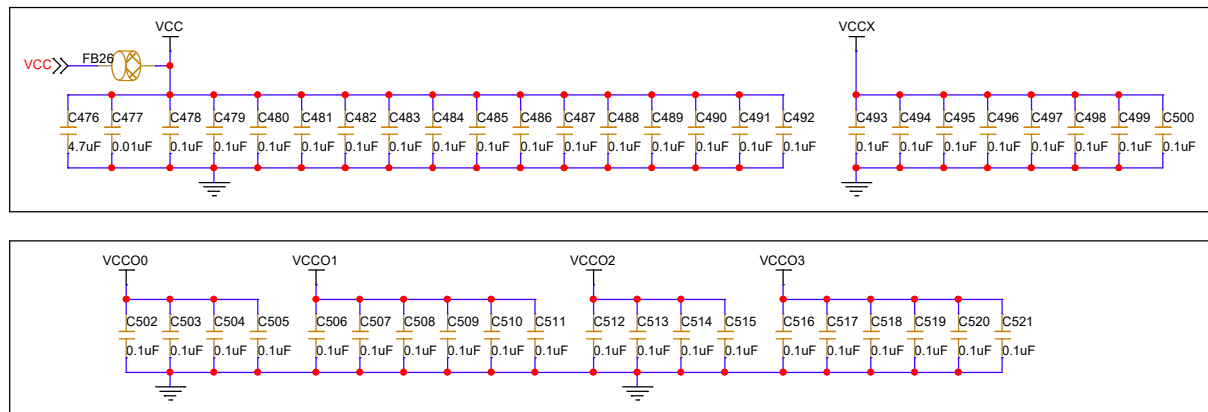
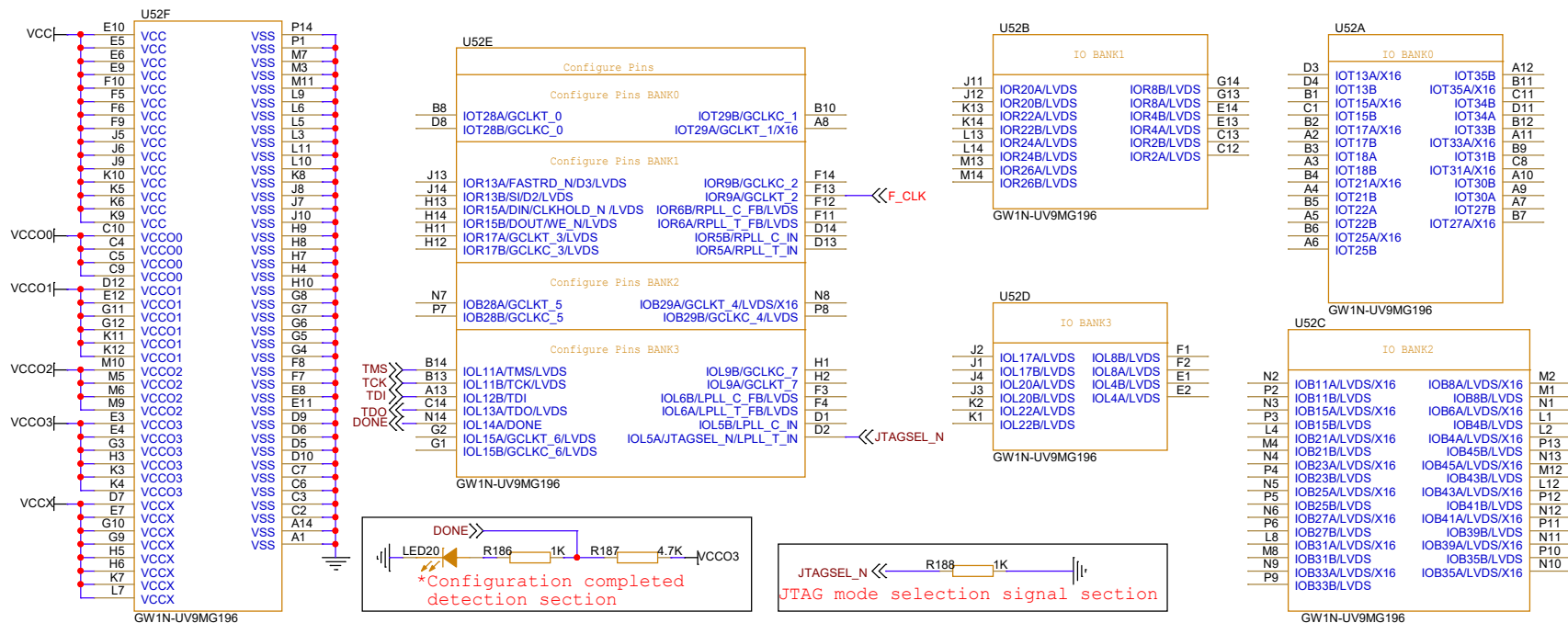






Notes:

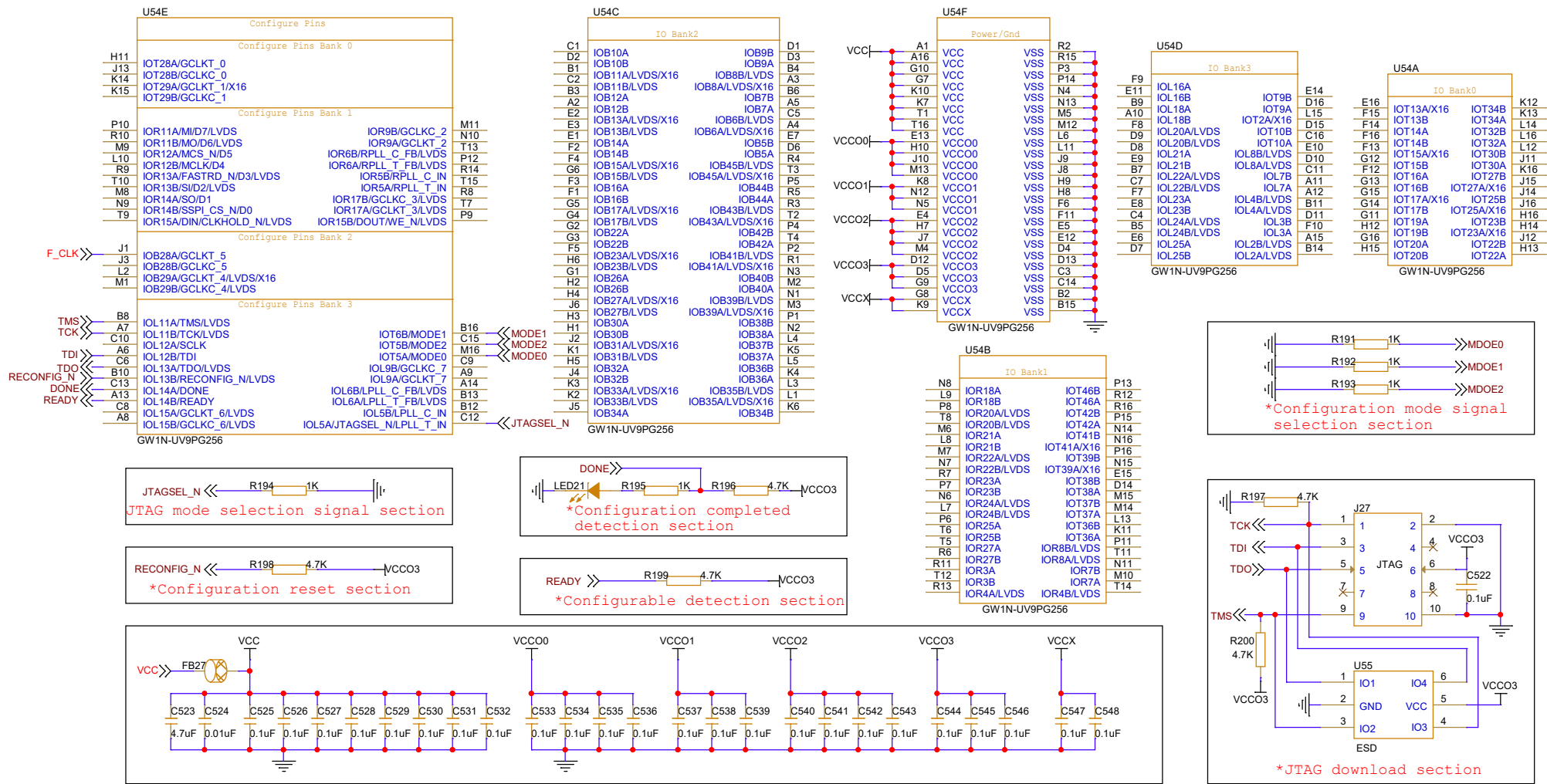
- 1.F CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.



Notes:

- 1.F CLK signal is an external input clock signal. It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
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B	GW1N-UV9MG196	2.2
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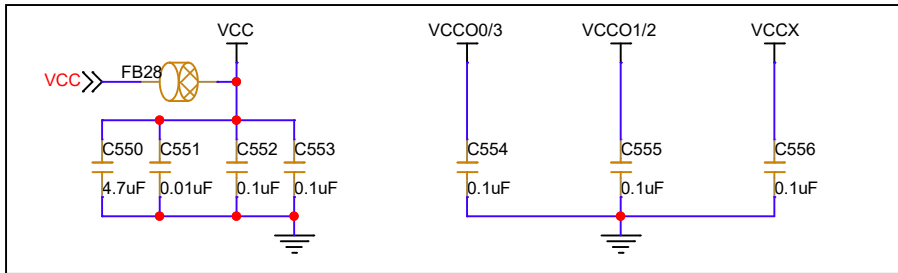
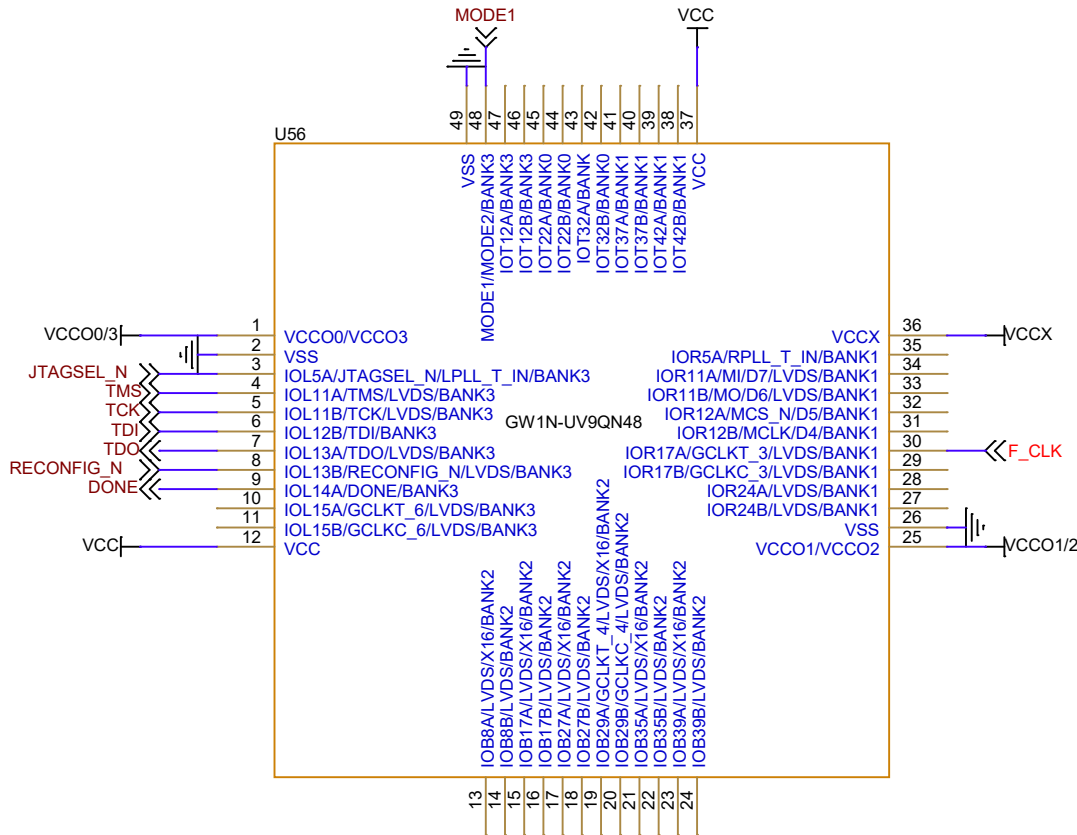


Notes:

1. F\_CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-UV9PG256	2.2
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# GW1N-UV9QN48



## Notes:

1.F\_CLK signal is an external input clock signal.

It is recommended that F\_CLK signal be provided through an active oscillator crystal.

2.It is recommended that add an ESD protection chip to the JTAG download circuit.

**\*Configuration mode signal selection section**

**\*Configuration reset section**

**\*Configuration completed detection section**

**JTAG mode selection signal section**

**\*JTAG download section**

Title  
GOWIN Minimum System Diagram

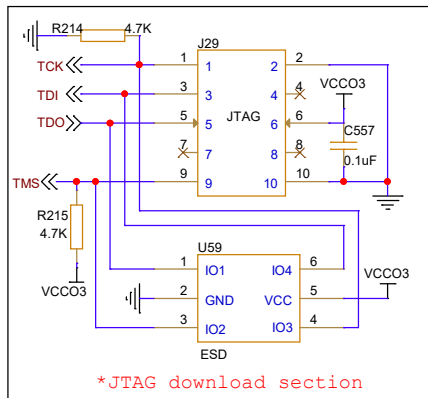
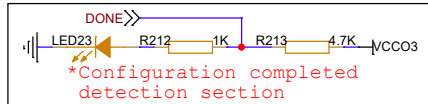
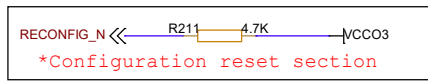
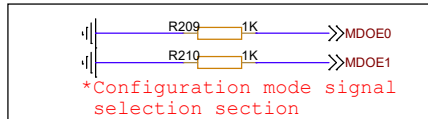
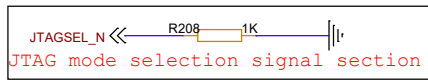
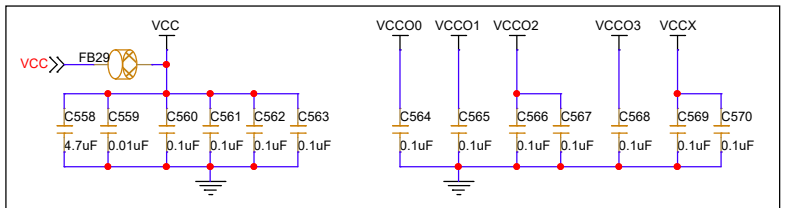
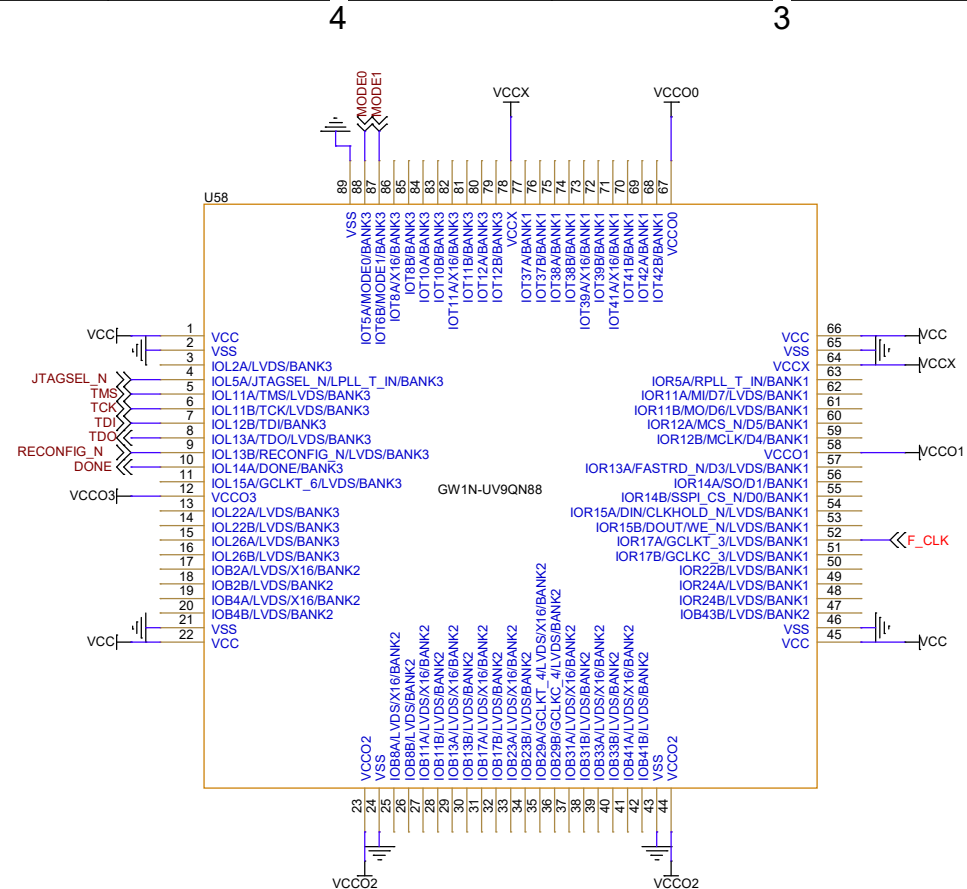
Size  
A4

Document Number  
GW1N-UV9QN48

Rev  
2.2

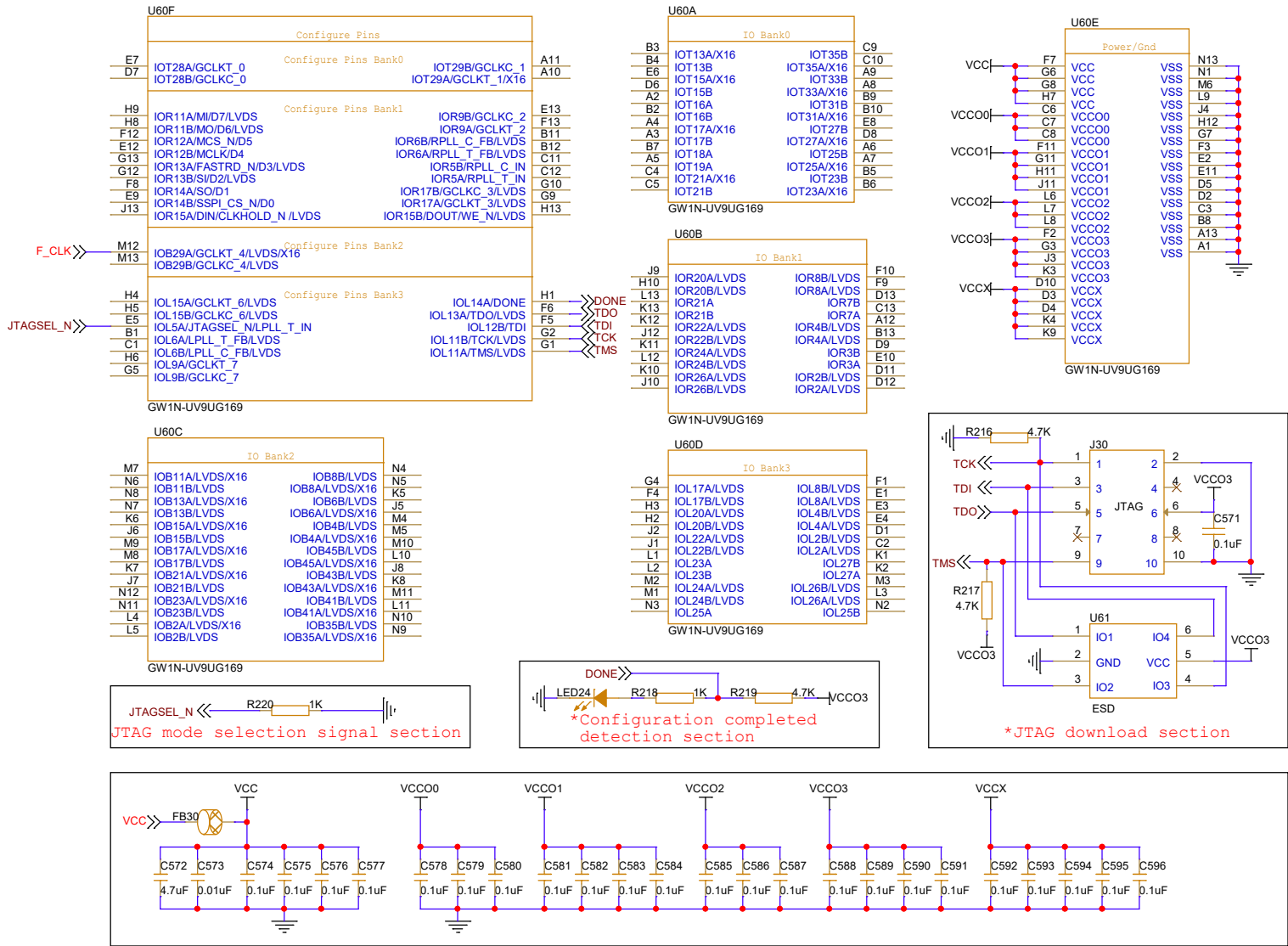
Date: Wednesday, June 19, 2024

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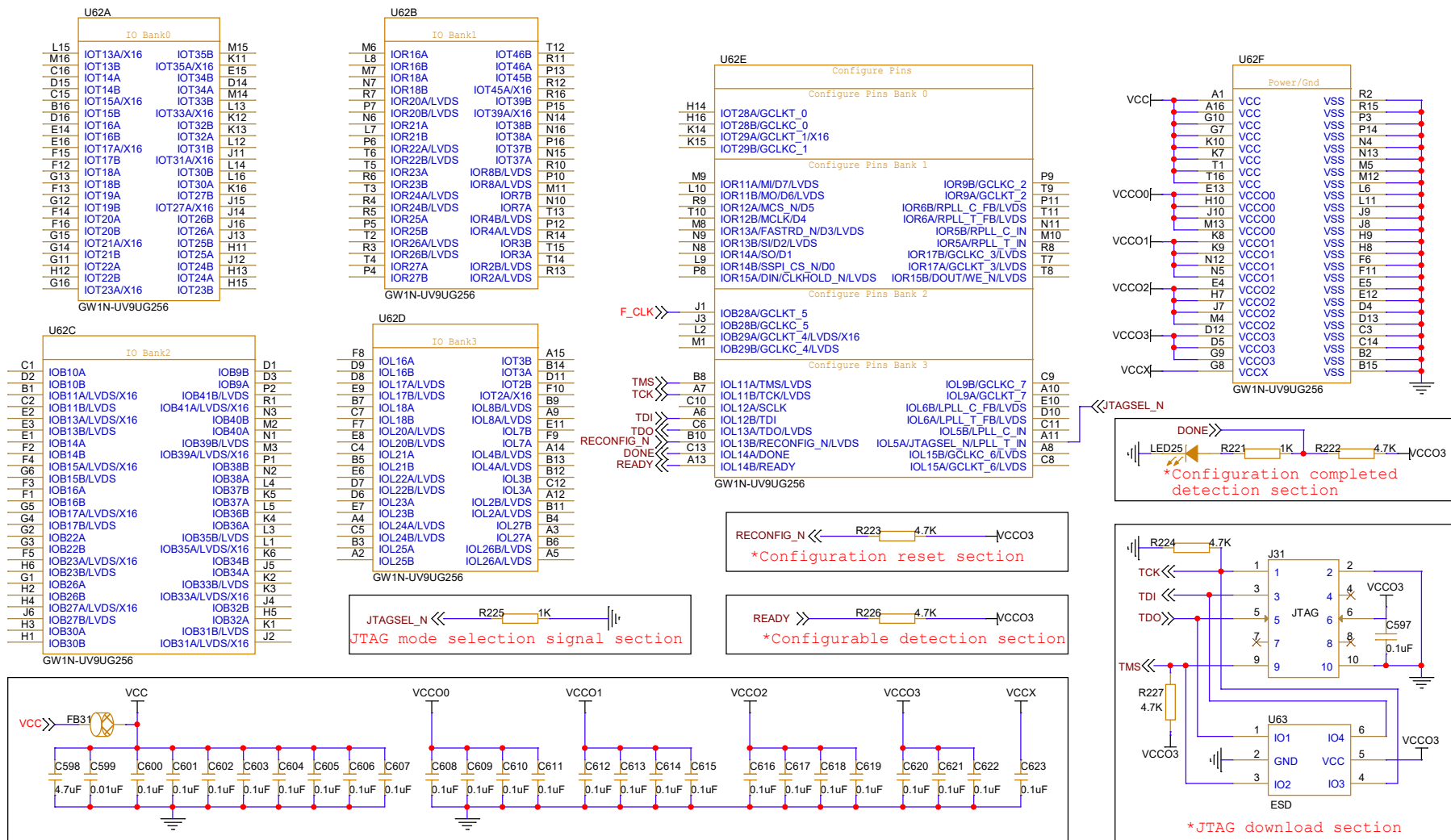
Notes:  
1.F CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.  
2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
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Notes:  
1.F CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.  
2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
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B	GW1N-UV9UG169	2.2
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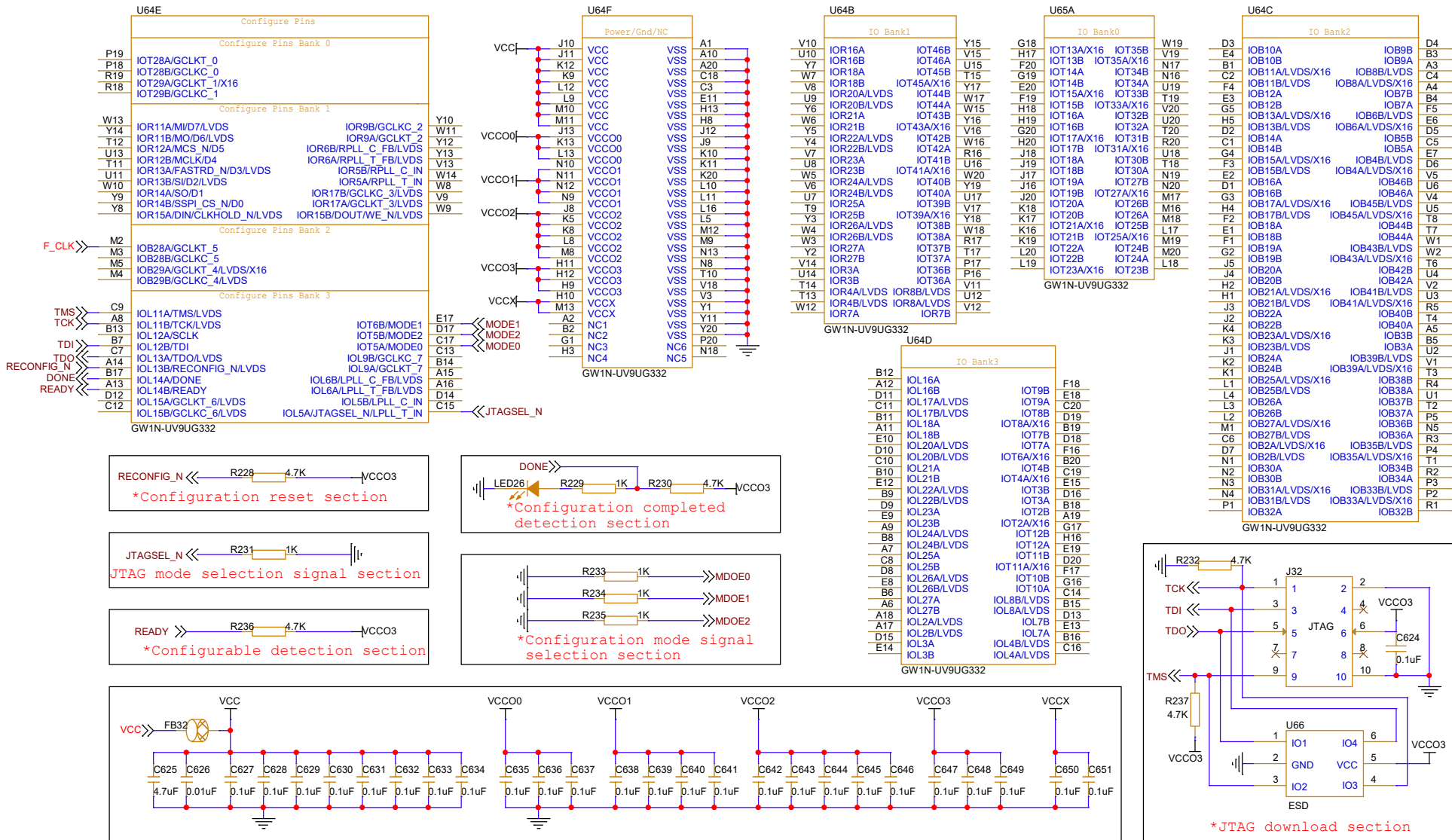


# Notes:

- 1.F CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-UV9UG256	2.2
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Notes:

- 1.F\_CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-UV9UG332	2.2
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