

### Notes:

1.F CLK signal is an external input clock signal.

It is recommended that F CLK signal be provided through an active oscillator crystal.

It is recommended that an I<sub>C</sub>ER signal be provided through an active pull-up resistor. External Flash memory is used to store downloaded programs.

**External flash memory is used to store downloaded programs! For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection".**

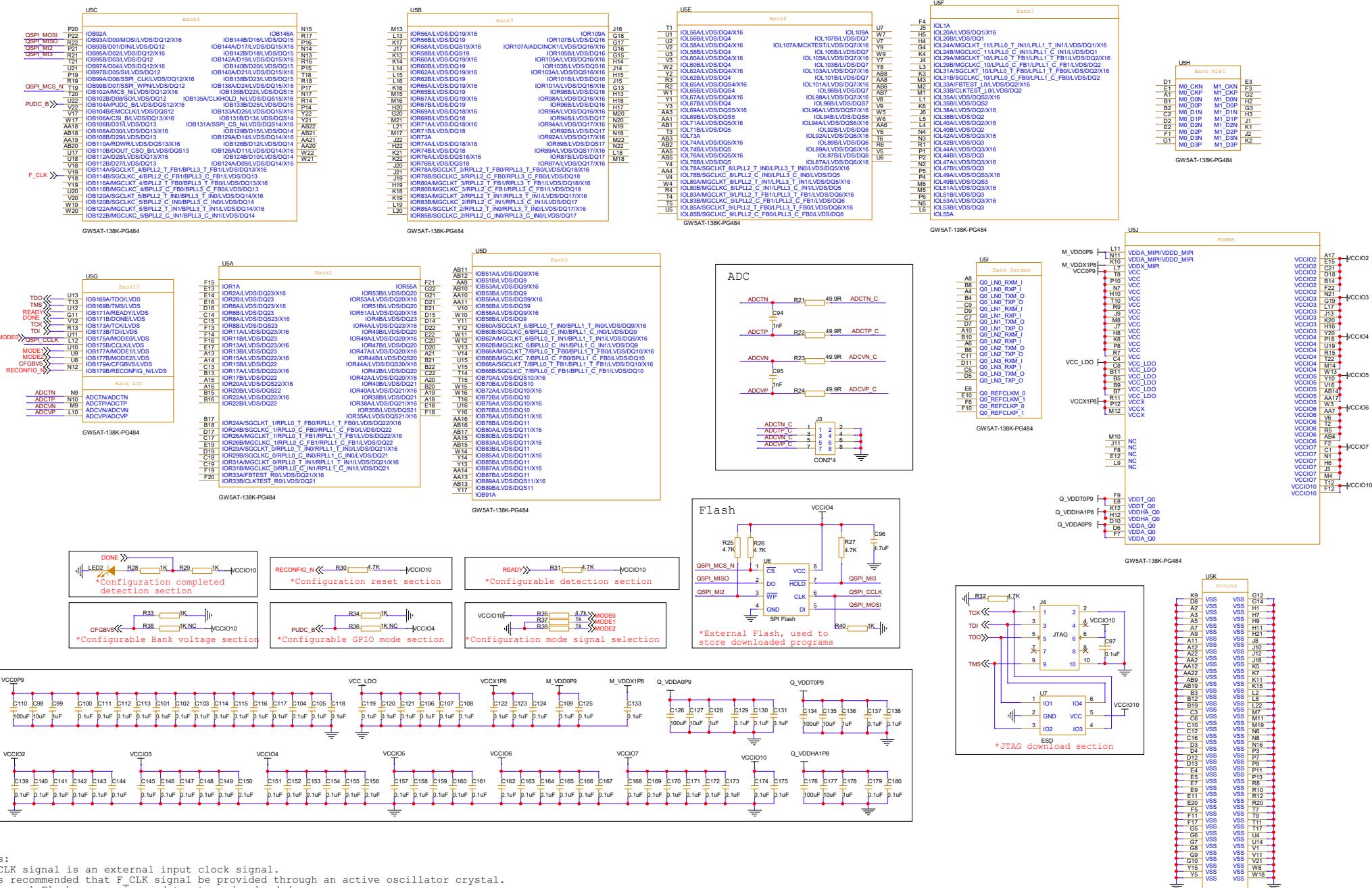
For details about SRI Flash model selection, see Chapter 4.5 SRI Flash Model Selection in the Arora V 138K FPGA Products Programming and Configuration Guide.

3. It is recommended that add an ESD protection chip to the JTAG download circuit.

4.VCC core voltage requires a large current, so it is recommended to add an ESD protection chip to the pins.

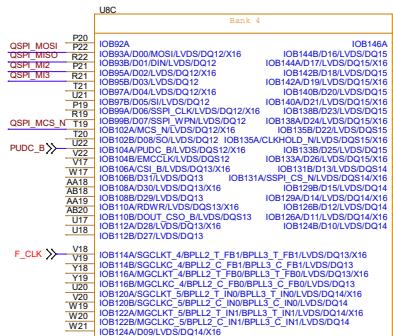
5. The MODE pin is the GowinCONFIG configuration mode selection signal.

For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG704,

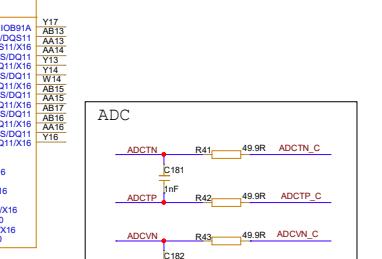
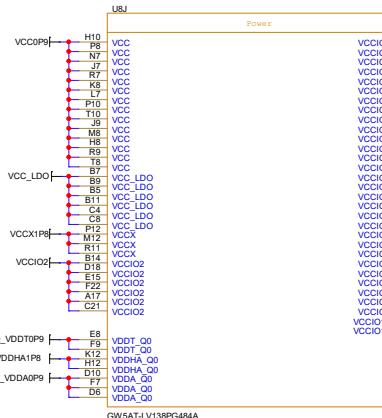
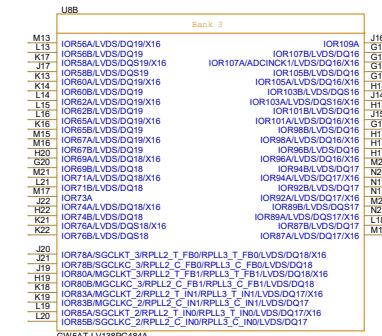


**Notes:**

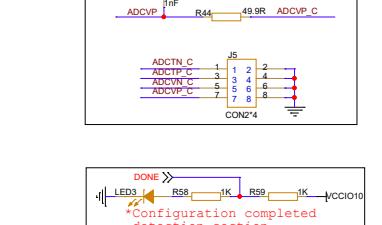
- 1.FCLK signal is an external input clock signal.  
It is recommended that FCLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.  
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG704, Arora V 138K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.  
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG704, Arora V 138K FPGA Products Programming and Configuration Guide .



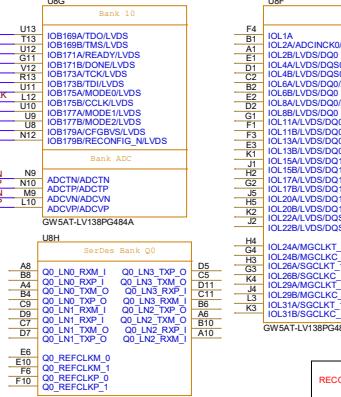
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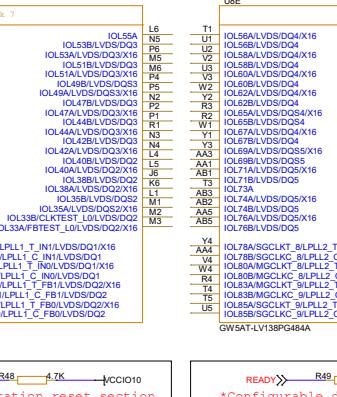
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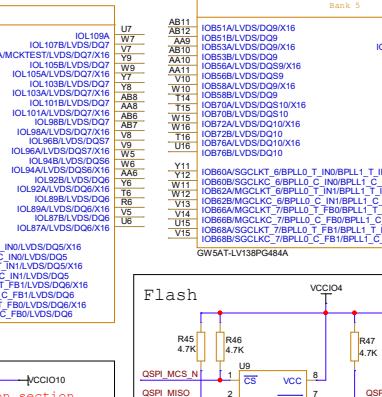
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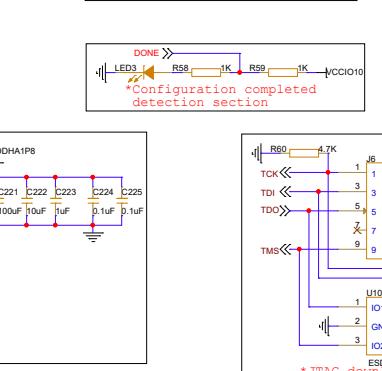
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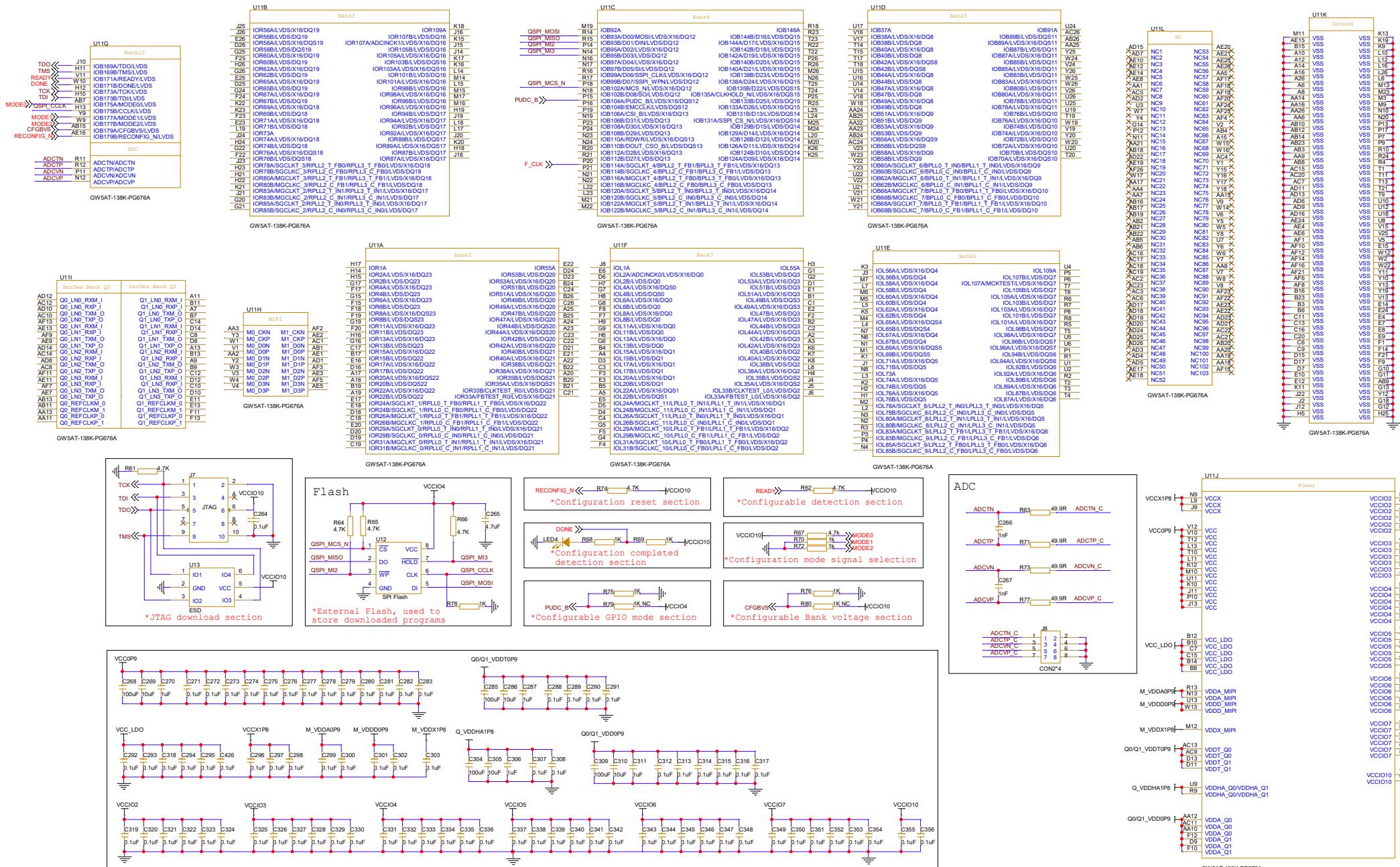
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection".

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3. It is recommended that add an ESD protection chip to the JTAG download circuit.  
4. VCC core voltage requires a large current, so it is recommended to supply power separately.

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Title		GOWIN Minimum System Diagram		
Size A2	Document Number GW5AT-LV138PG484A			Rev. 2.



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For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in the User's Manual.

For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Model Selection" in the Arora V 138K FPGA Products Programming and Configuration Guide.

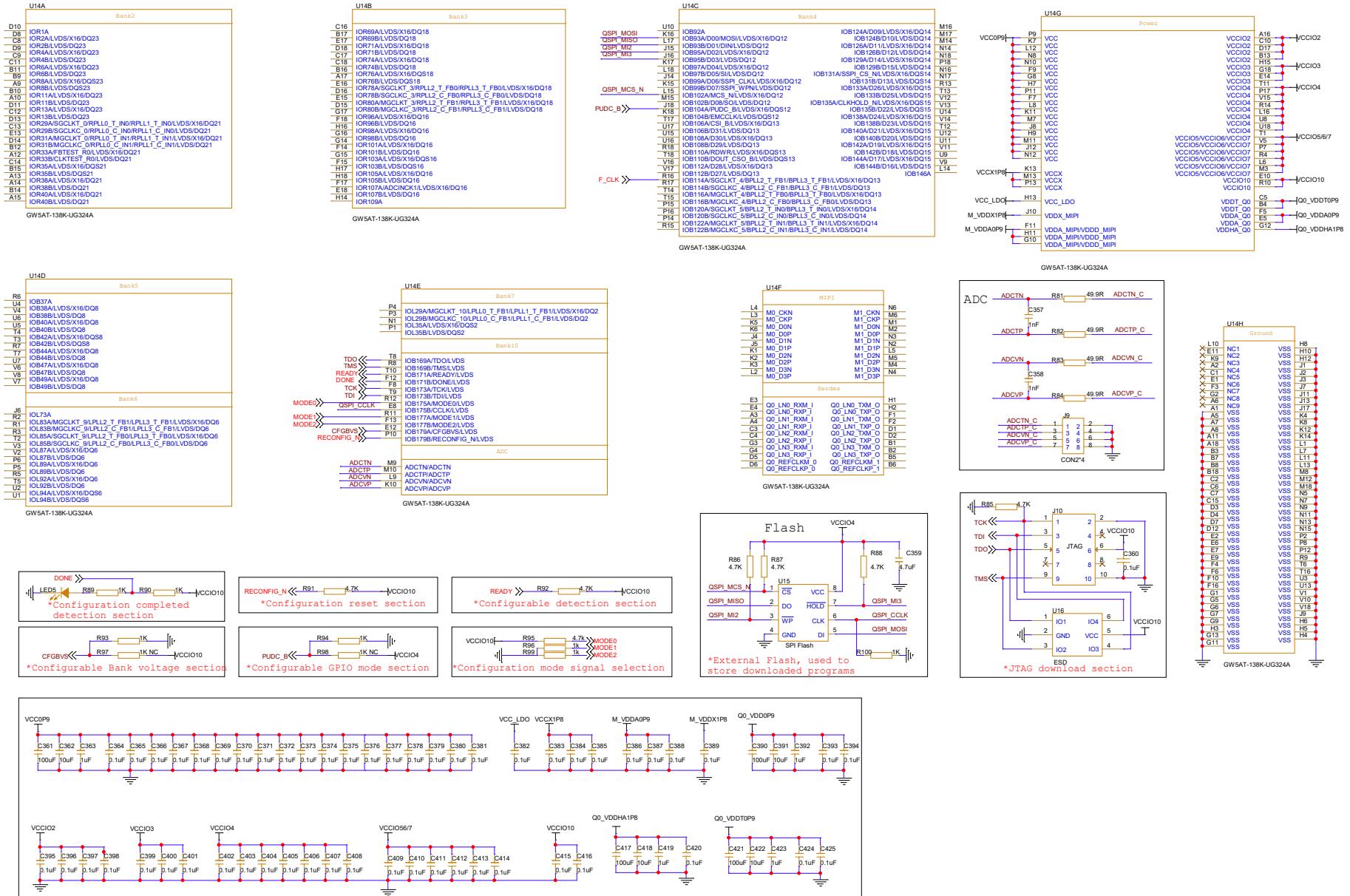
3. It is recommended that add an ESD protection chip to the JTAG download circuit.

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For details about how to select the Mode signal, see "Chapter 3.1 Configuration".

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For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG704, *Aurora V 138K FPGA Products Programming and Configuration Guide*.