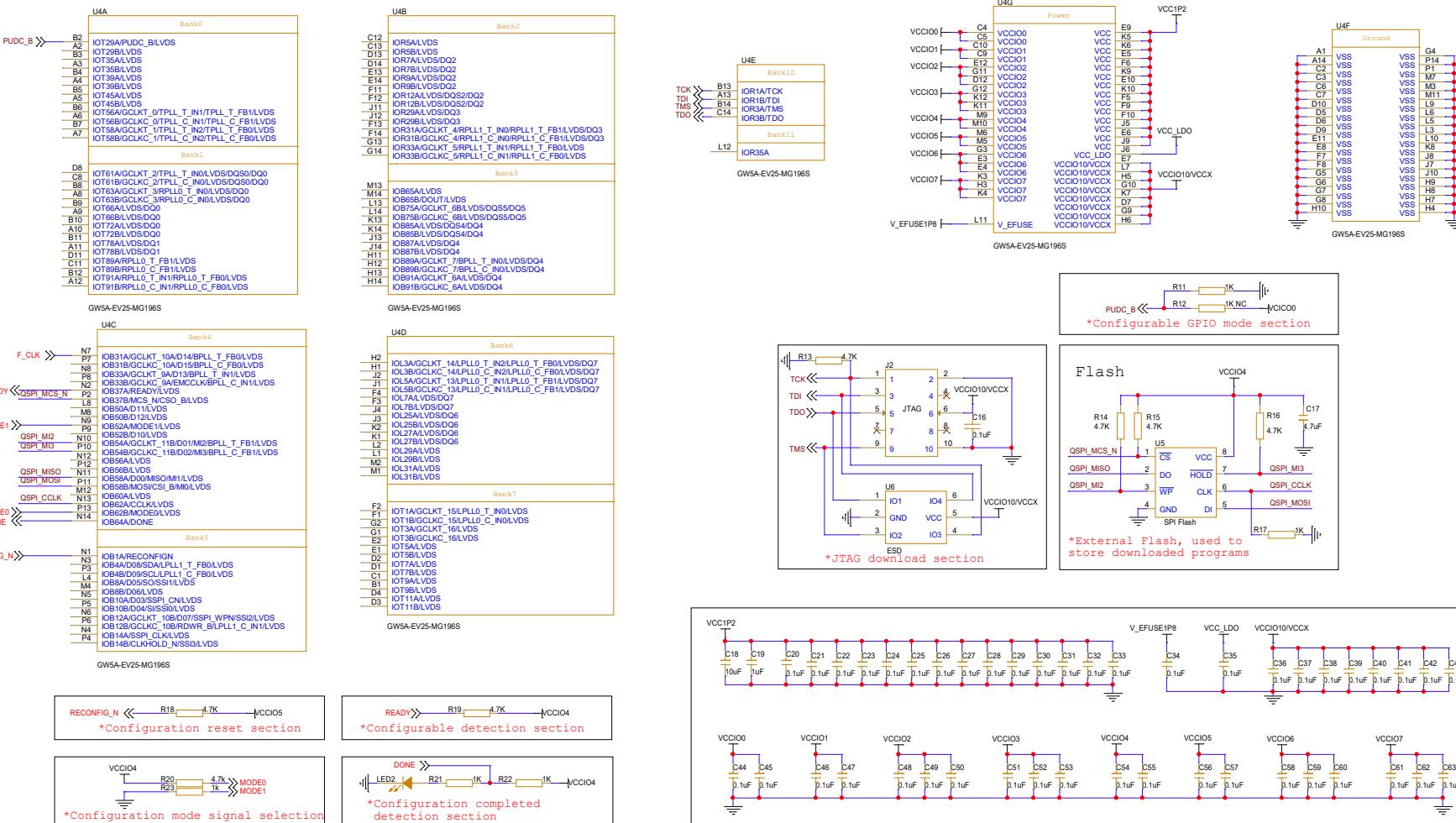
**Notes:**

- F CLK signal is an external input clock signal.
- It is recommended that F CLK signal be provided through an active oscillator crystal.
- External Flash memory is used to store downloaded programs.
- For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
- It is recommended that add an ESD protection chip to the JTAG download circuit.
- VCC core voltage requires a large current, so it is recommended to supply power separately.
- The MODE pin is the GowinCONFIG configuration mode selection signal.
- For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.

Title: GOWIN Minimum System Diagram		
Size: C	Document Number: GW5A-EV25LQ100	Rev: 2.5
Date: Thursday, October 24, 2024	Sheet: 1	of 16

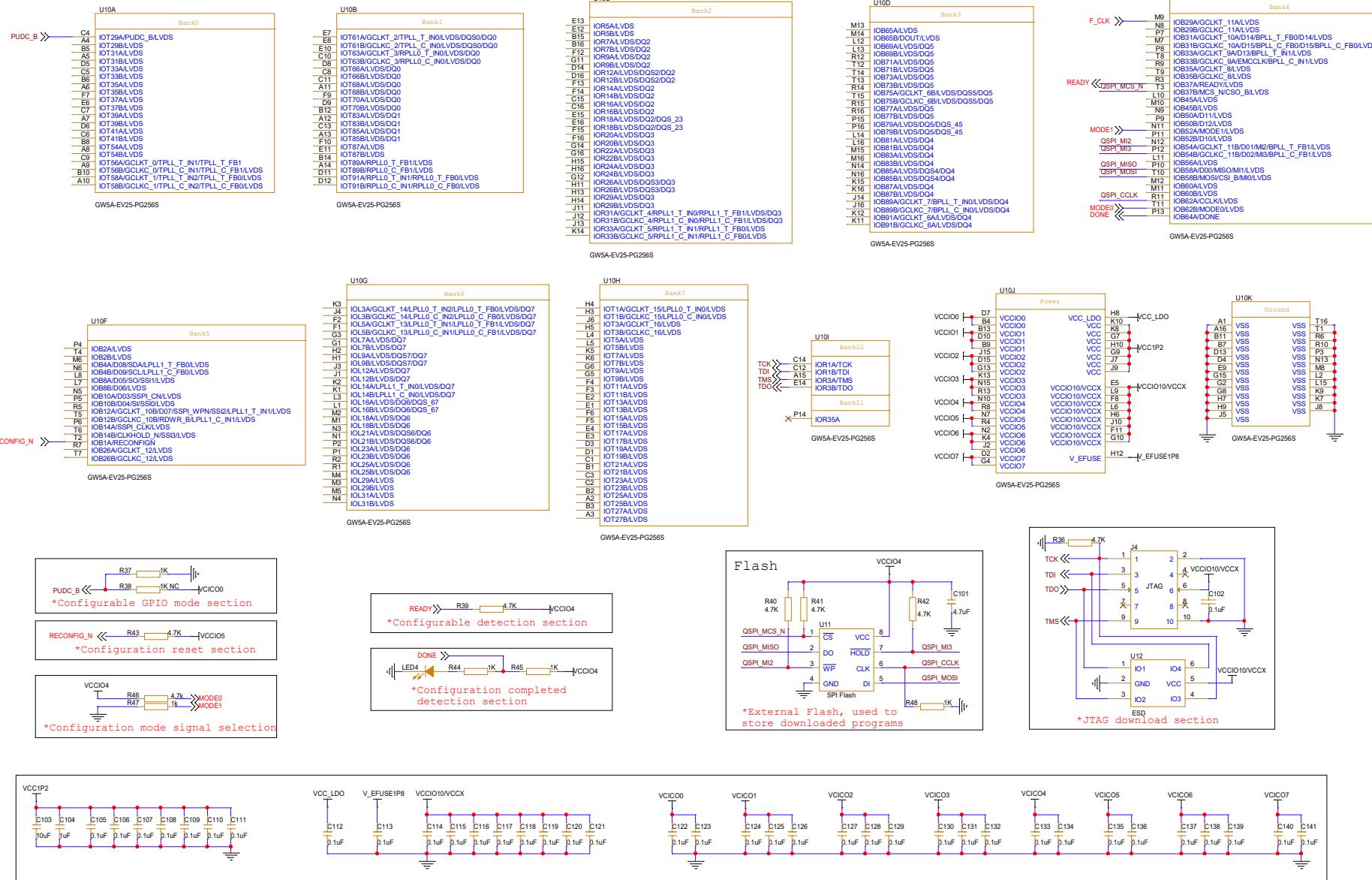


#### Notes:

- 1.F\_CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
  - 2.External Flash memory is used to store downloaded programs.  
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .
  - 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
  - 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
  - 5.The MODE pin is the GowinCONFIG configuration mode selection signal.  
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .

Title		GOWIN Minimum System Diagram		
Size	Document Number			Rev.
C	GW5A-EV25MG196S			2.5
Date:	Thursday, October 24, 2024		Sheet	1 of 16





## Notes

1.F CLK signal is an external input clock signal.

It is recommended that F CLK signal be provided through an active oscillator crystal.

2.External Flash memory is used to store downloaded programs.

For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection".

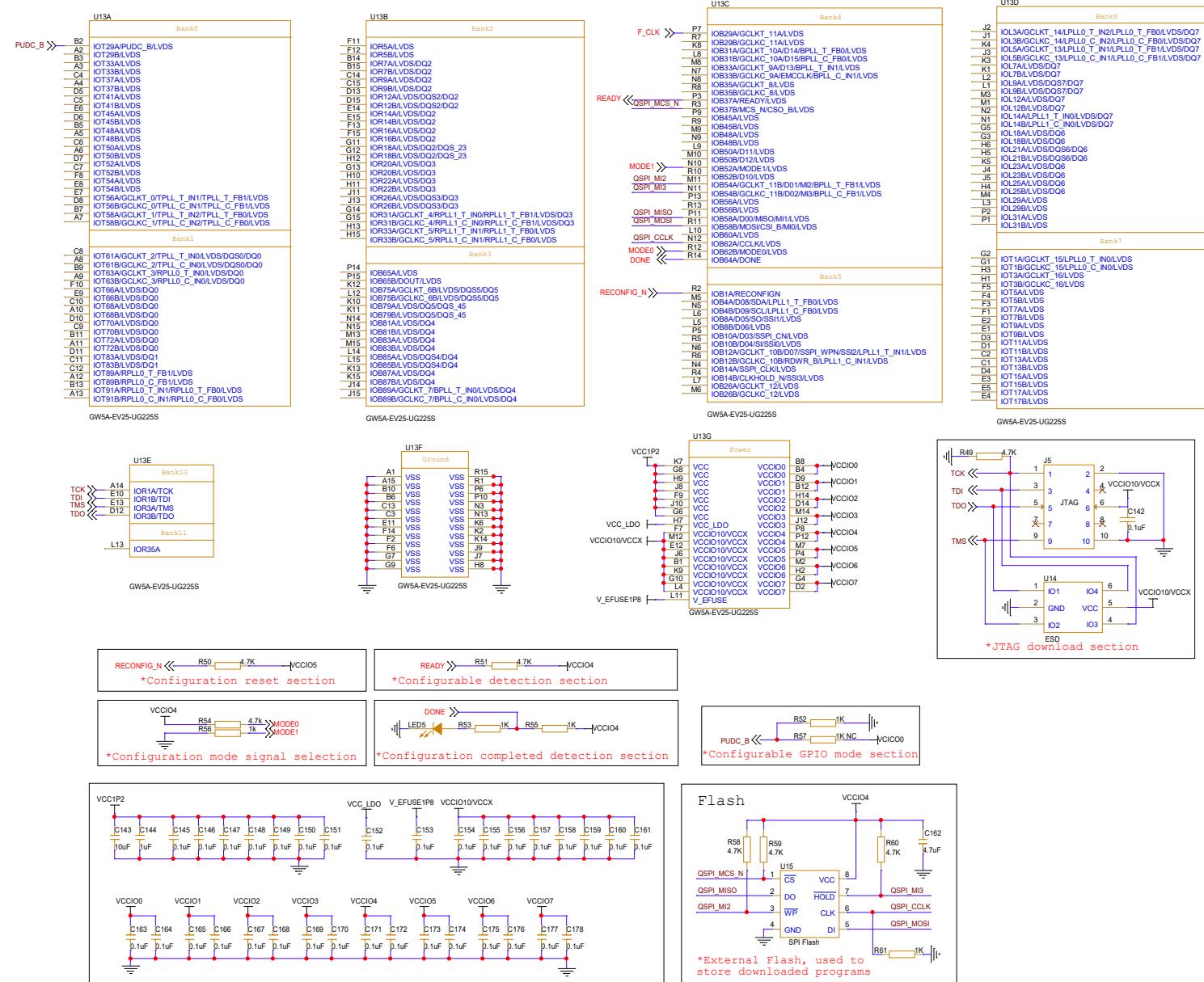
Arora V 25K FPGA Products Programming and Configuration Guide .

3. It is recommended that add an ESD protection chip to the JTAG port.

4.VCC core voltage requires a large current, so it is recommended to supply the Vcore via the GND connection.

5.The MODE pin is the GowinCONFIG configuration mode selection signal. For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714 Arora V 25K FPGA Products Programming and Configuration Guide.

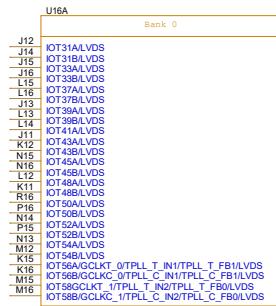
Title		GOWIN Minimum System Diagram		
Size	Document Number			Rev
C	GHS4-EV2P-G256S			2.5
Date:	Thursday, October 24, 2024	Sheet	4	of 16



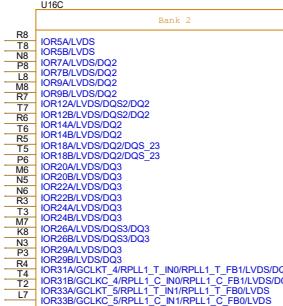
## Notes

- 1.F CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.
  - 2.External Flash memory is used to store downloaded programs.  
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .
  - 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
  - 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
  - 5.The MODE pin is the GowinCONFIG configuration mode selection signal.  
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714 Arora V 25K FPGA Products Programming and Configuration Guide .

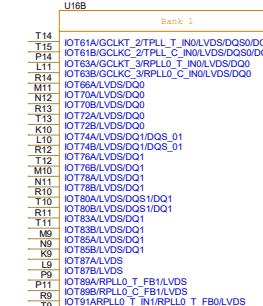
Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
C	GW5A-EV2UG22SS	2.5
Date:	Thursday, October 24, 2024	Sheet
		5 of 16



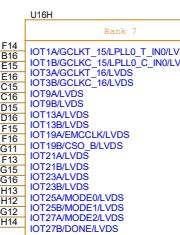
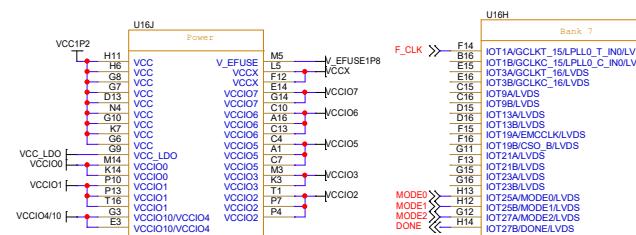
WEA 3EK EVI IC3E6C



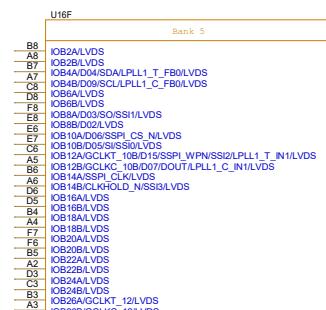
Page 1



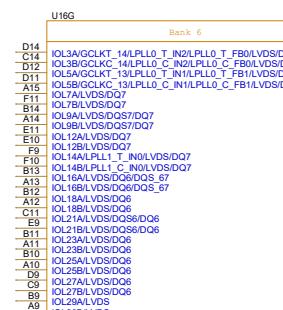
IOT91B/RP



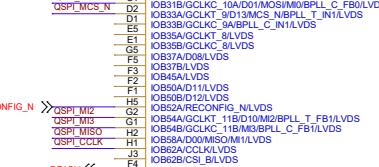
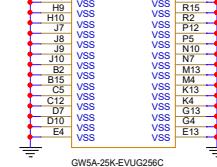
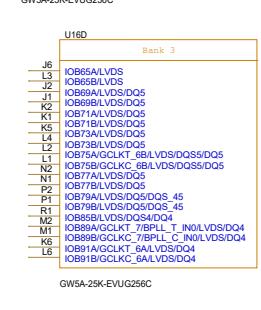
QWERTYUIOP



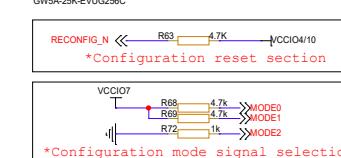
GMEA-25K-FN9IC256C



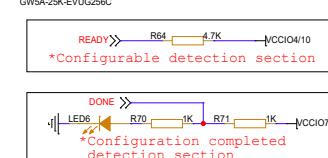
QWERTY 2016-01-10 00:00:00



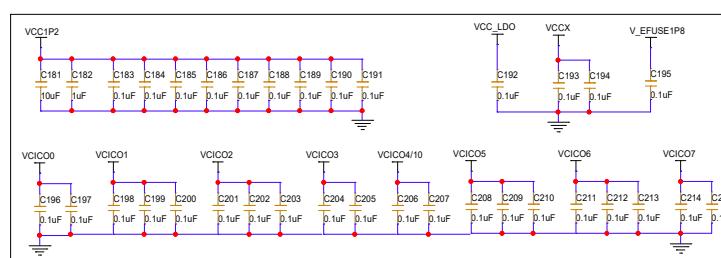
READY <<—



#### \*Configuration reset section



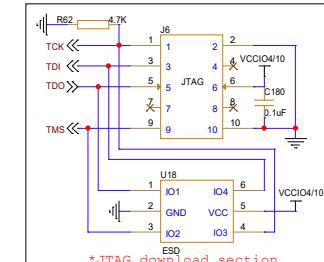
\*Configurable detection sets



The diagram illustrates the connection between the STM32F407VGT6 microcontroller and an external SPI Flash chip. Key components include:

- SPI Flash Chip:** U17, connected to VCC and GND.
- Microcontroller Pins:**
  - SPI\_MOSI\_N (Pin 1) connects to CS.
  - SPI\_MISO (Pin 2) connects to DO.
  - SPI\_M2 (Pin 3) connects to HOLD.
  - GND (Pin 4).
  - WF# (Pin 5) connects to CLK.
  - DI (Pin 6) connects to QSPI\_CCLK.
  - QSPI\_MOSI (Pin 7) connects to QSPI\_M2.
  - VCCIO4/10 (Pin 8) connects to VCC.
- External Components:**
  - R65 (4.7kΩ) and R66 (4.7kΩ) are connected between the microcontroller's CS pin and ground.
  - R67 (4.7kΩ) and C1 (100pF) are connected between the microcontroller's VCCIO4/10 pin and ground.
  - R73 (1kΩ) is connected between the microcontroller's DI pin and ground.
- Notes:**
  - \*External Flash, used to store downloaded programs

\*External Flash, used to



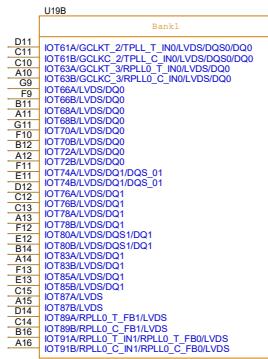
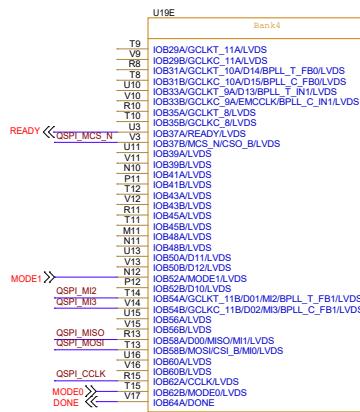
ESD

**Notes:**

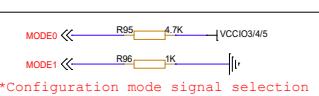
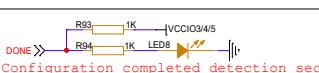
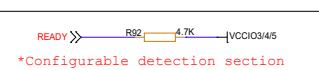
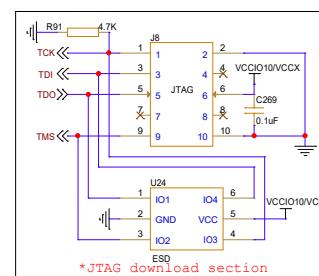
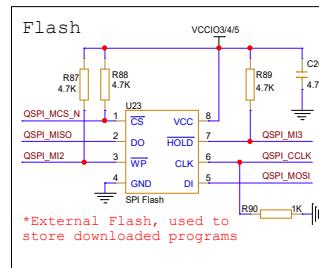
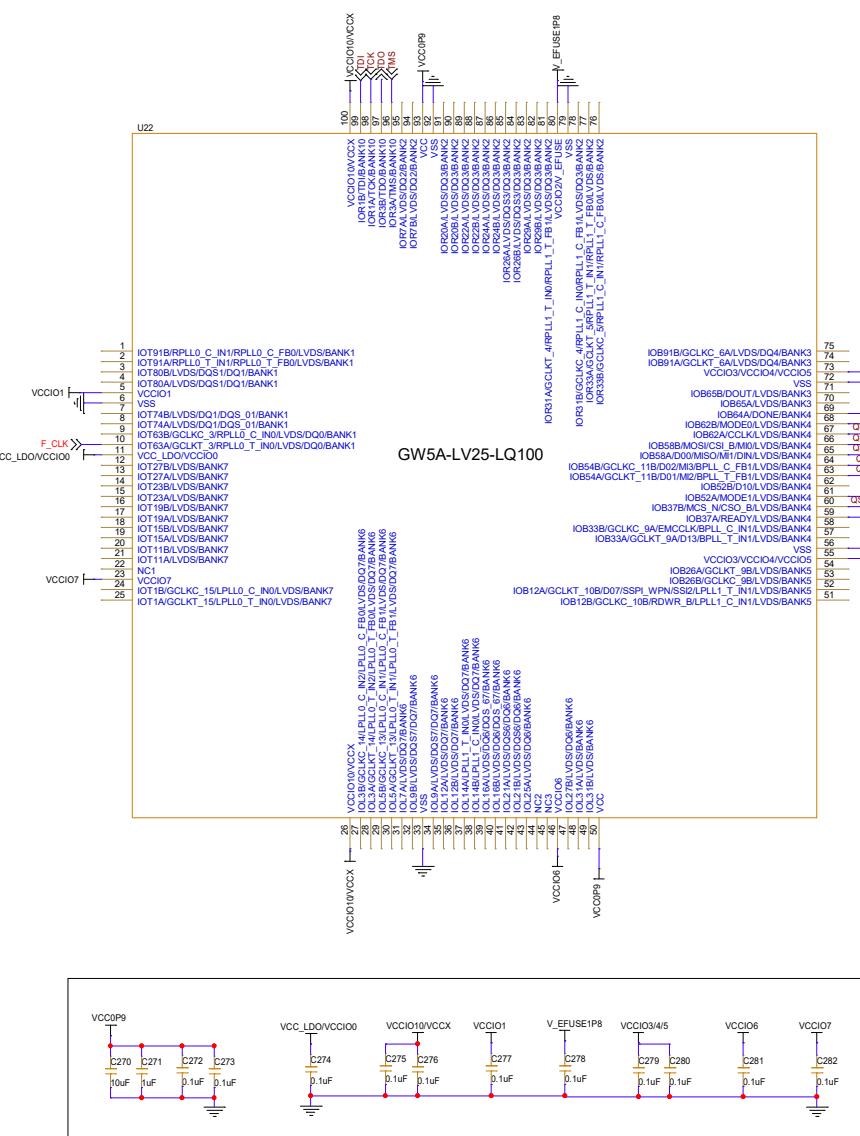
- 1.F CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.  
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, *Arora V 25K FPGA Products Programming and Configuration Guide*.
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.  
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, *Arora V 25K FPGA Products Programming and Configuration Guide*.

Title <b>GOWIN Minimum System Diagram</b>		
Size C	Document Number GWSA-EV25UG256C	Rev 2.5
Date: Thursday, October 24, 2024	Sheet 6	of 16

# GW5A-EV25UG324S



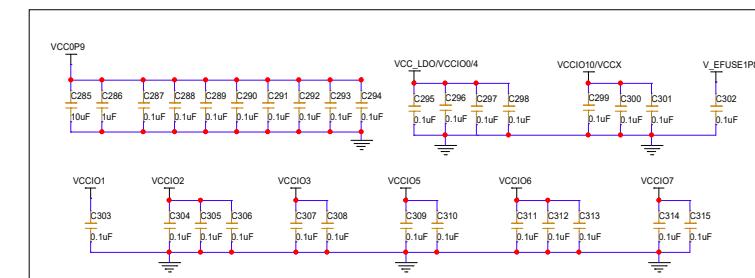
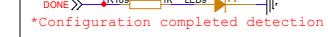
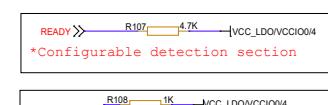
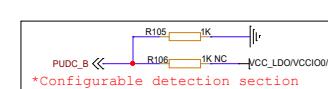
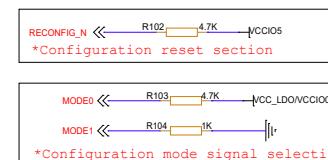
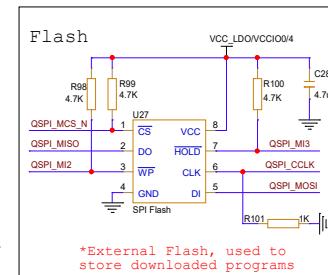
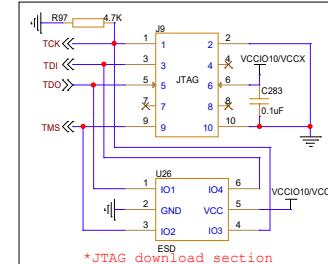
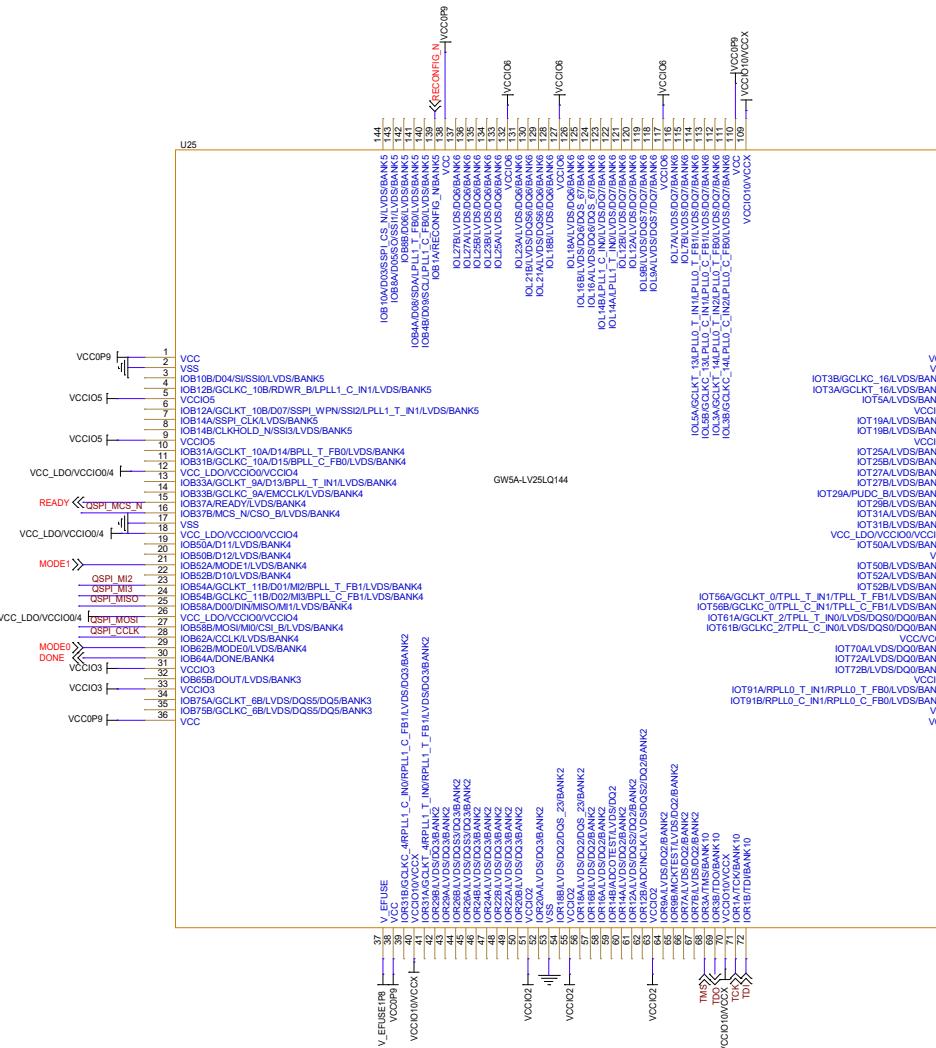
# GW5A-LV25LQ100



## Notes:

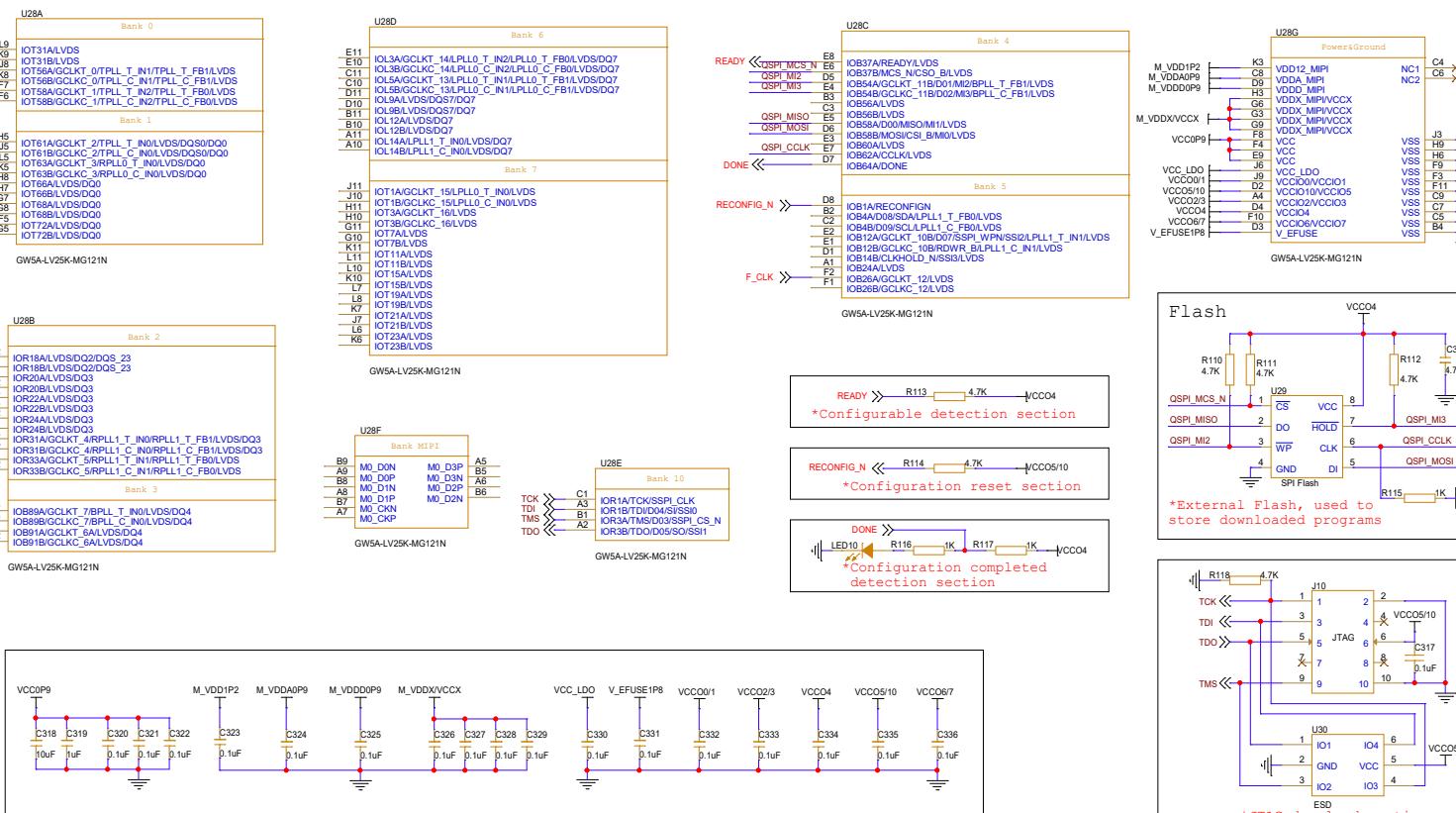
- F\_CLK signal is an external input clock signal.
- It is recommended that F\_CLK signal be provided through an active oscillator crystal.
- External Flash memory is used to store downloaded programs.
- For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .
- It is recommended that add an ESD protection chip to the JTAG download circuit.
- VCC core voltage requires a large current, so it is recommended to supply power separately.
- The MODE pin is the 'GowinCONFIG' configuration mode selection signal.
- For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
C	GW5A-LV25LQ100	2.5
Date:	Thursday, October 24, 2024	Sheet 8 of 16



Title		GOWIN Minimum System Diagram
Size	Document Number	C GW5A-LV25LQ144
C	Rev	2.5
Date	Sheet	Thursday, October 24, 2024

**GW5A-LV25MG121N**

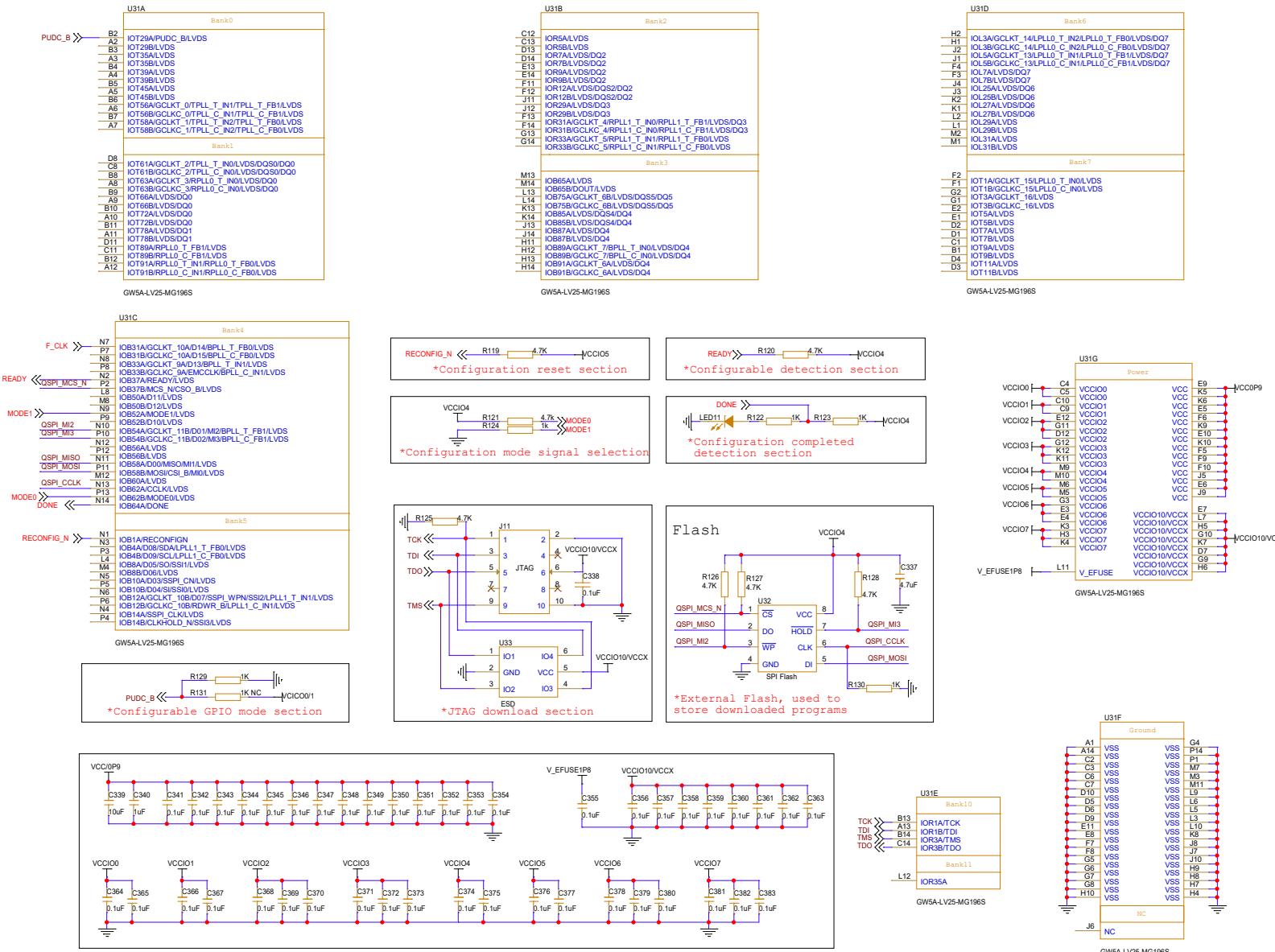


## Notes:

- 1.F CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.
  - 2.External Flash memory is used to store downloaded programs.  
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, [Arora V 25K FPGA Products Programming and Configuration Guide](#).
  - 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
  - 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
  - 5.The MODE pin is the GowinCONFIG configuration mode selection signal.  
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714 [Arora V 25K FPGA Products Programming and Configuration Guide](#).

Title	GOWIN Minimum System Diagram		
Size C	Document Number GW5A-LV25MG121N		Rev 2.5
Date:	Thursday, October 24, 2024	Sheet	10 of 16

# GW5A-LV25MG196S

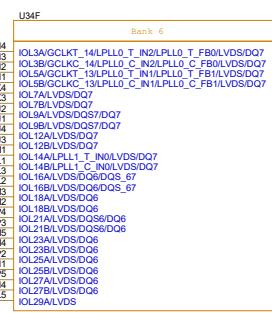
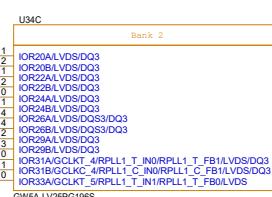
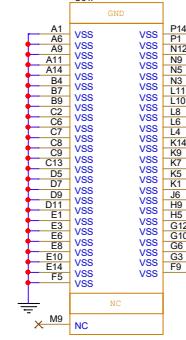
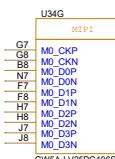
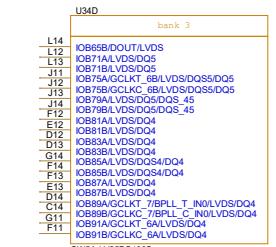
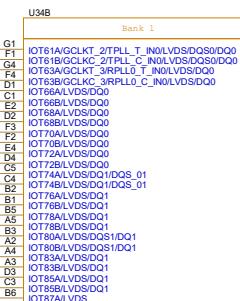
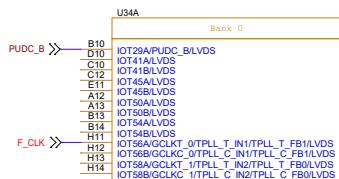


## Notes:

- F\_CLK signal is an external input clock signal.
- It is recommended that F\_CLK signal be provided through an active oscillator crystal.
- External Flash memory is used to store downloaded programs.
- For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .
- It is recommended that add an ESD protection chip to the JTAG download circuit.
- VCC core voltage requires a large current, so it is recommended to supply power separately.
- The MODE pin is the GowinCONFIG configuration mode selection signal.
- For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .

File: GOWIN Minimum System Diagram		
Size	Document Number	Rev
C	GW5A-LV25MG196S	2.5

Date: Thursday, October 24, 2024 Sheet: 11 of 16

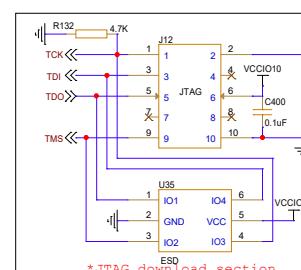


RECONFIG\_N <> R133 4.7K -> VCCIO10/2/3/4/5  
\*Configuration reset section

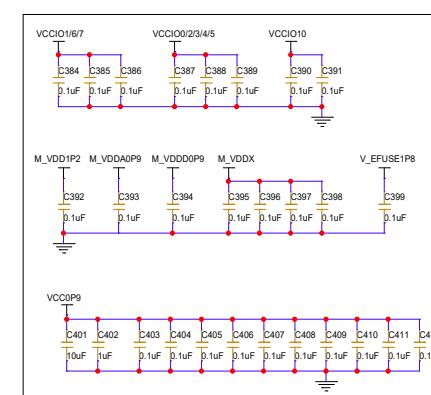
READY >> R134 4.7K -> VCCIO10/2/3/4/5  
\*Configurable detection section

PUDC\_B <> R137 1K NC -> VCCIO10/2/3/4/5  
\*Configurable detection section

MODE0 <> R138 4.7K -> VCCIO10/2/3/4/5  
MODE2 <> R141 1K -> VCCIO10/2/3/4/5  
\*Configuration mode signal selection



R139 1K -> VCCIO10/2/3/4/5  
DONE >> R142 1K LED12 -> VCCIO10/2/3/4/5  
\*Configuration completed detection section

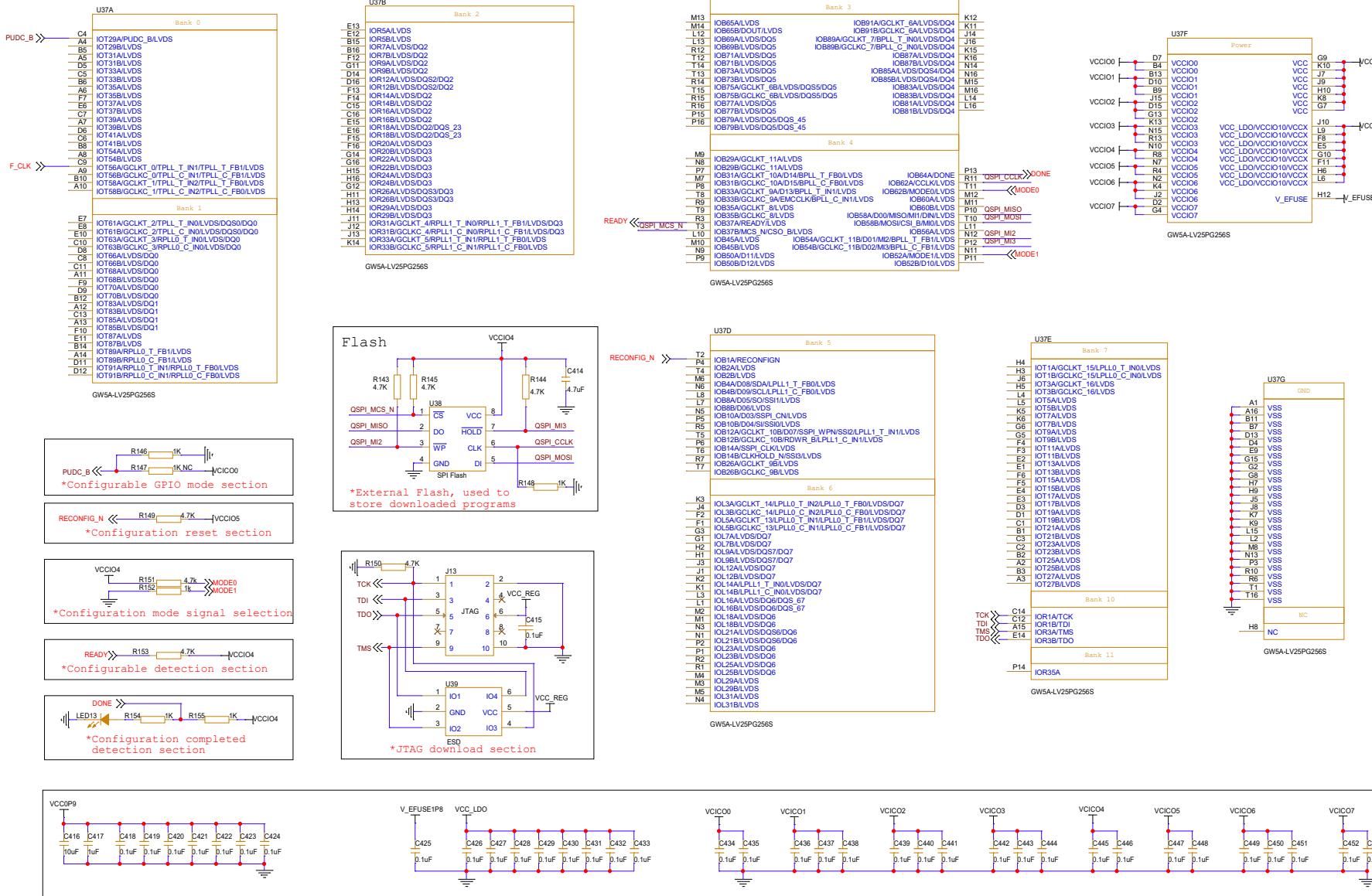


Title		GOWIN Minimum System Diagram	
Size	C	Document Number	GW5A-LV25PG196S
Date	Thursday, October 24, 2024	Sheet	12 of 16
Rev	2.5		

## Notes:

- F CLK signal is an external input clock signal.
- It is recommended that F CLK signal be provided through an active oscillator crystal.
- External Flash memory is used to store downloaded programs.
- For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .
3. It is recommended that add an ESD protection chip to the JTAG download circuit.
4. VCC core voltage requires a large current, so it is recommended to supply power separately.
5. The MODE pin is the GowinCONFIG configuration mode selection signal.
- For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .

*GW5A-LV25PG256S*



#### Notes:

1.F CLK signal is an external input clock signal.

It is recommended that F\_CLK signal be provided through an active oscillator crystal

2.External Flash memory is used to store downloaded programs.

For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection".

Arora V 25K FPGA Products Programming and Configuration Guide

3. It is recommended that add an ESD protection chip to the JTAG download circuit.

4. VCC core voltage requires a large current, so it is recommended to use a high-current source.

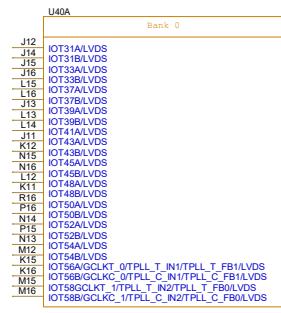
5.The MODE pin is the GowinCONFIG configuration mode selection signal.

For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714.

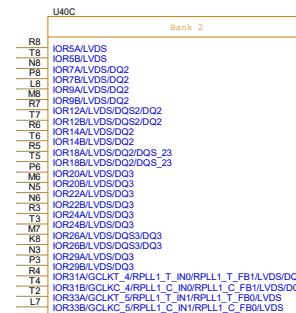
Arora V 25K FPGA Products Programming and Configuration Guid

5 1

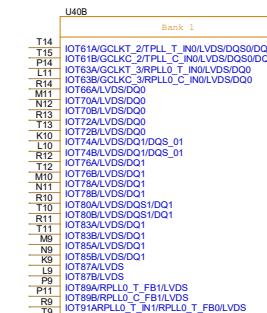
Title		
GOWIN Minimum System Diagram		
Size C	Document Number GW5A-LV25PG256S	Rev 2.5
Date:	Thursday, October 24, 2024	Sheet 13 of 16



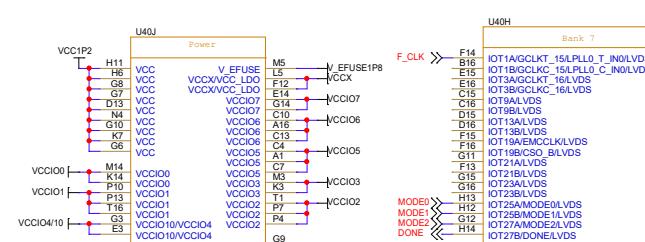
QINSA-LM95-HQ0500



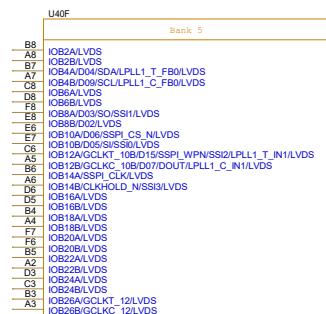
SWFA-LM25-HQ9500



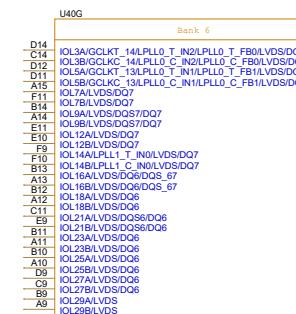
IOT91B/RPLL0\_C\_IN1/RPLL0\_C\_FB0/LY



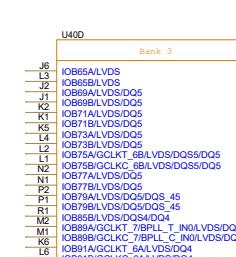
www.ijerpi.org



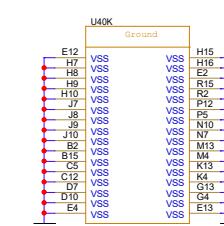
IOB26B/GCLKC\_12/LVDS



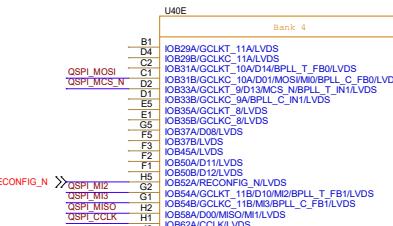
IOL29B/LVDS



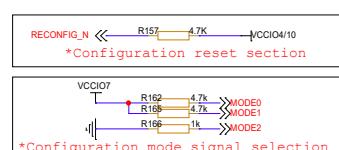
L6 10B91A/GCLRT\_6A/LVDS/DQ4  
10B91B/GCLKC\_6A/LVDS/DQ4



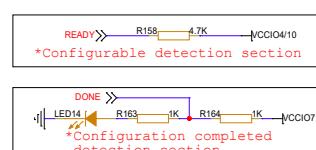
GW5A-LV25-UG256C



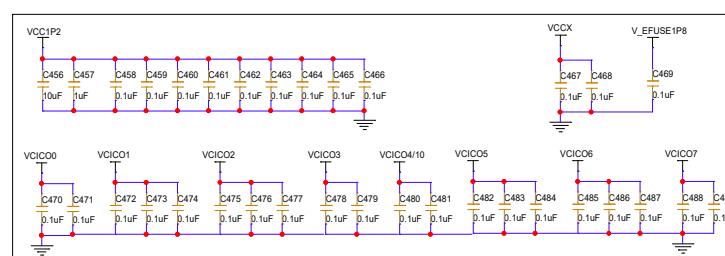
IOB62A/0



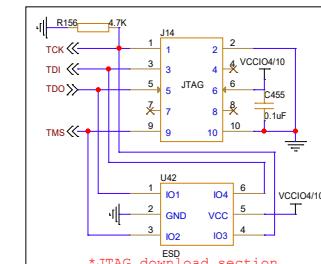
#### \*Configuration reset section



[View Details](#)



\*External Flash, used to



\*JTAG download section

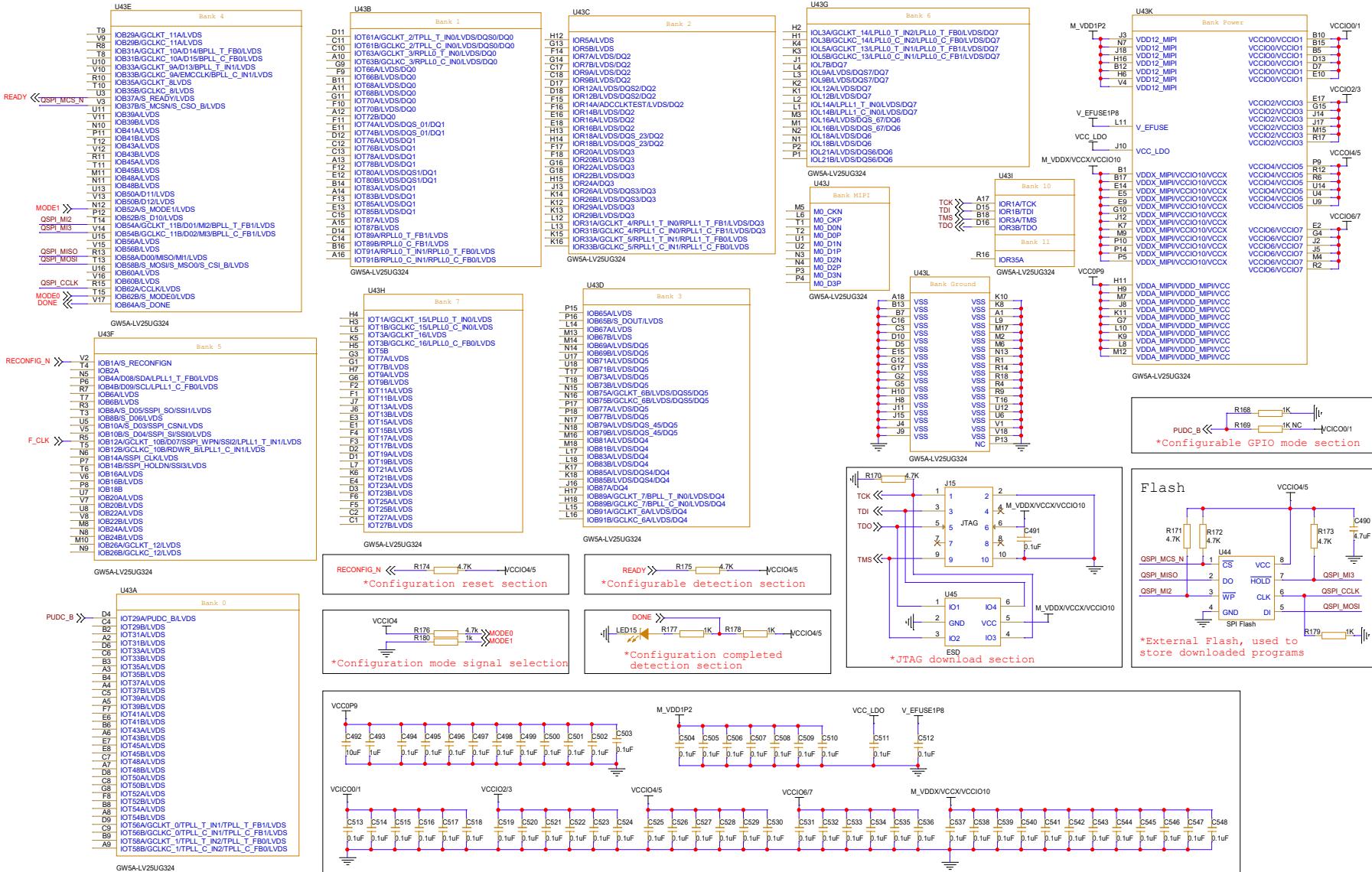
Number 2

- Notes:**

  - 1.F CLK signal is an external input clock signal.
  - It is recommended that F CLK signal be provided through an active oscillator crystal.
  - 2.External Flash memory is used to store downloaded programs.
  - For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FFPGAs Products Programming and Configuration Guide .
  - 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
  - 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
  - 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
  - For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714 Arora V 25K FFPGAs Products Programming and Configuration Guide .

Title		GOWIN Minimum System Diagram		
Size	Document Number	Rev		
C	GHW5A-LV25UG25C	2.5		
Date:	Thursday, October 24, 2024	Sheet	14	of 16

*GW5A-LV25UG324*



### Note

1.F CLK signal is an external input clock signal.

It is recommended that F CLK signal be provided through an ac coupled buffer.

2.External Flash memory is used to store downloaded programs.

For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection".

Arora V 25K FPGA Products Programming and Configuration Guide .  
It is recommended that add-in FPGAs be connected to the ITAC download circuit.

3. It is recommended that add an ESD protection chip to the JTAG port.  
4. VCC core voltage requires a large current, so it is recommended

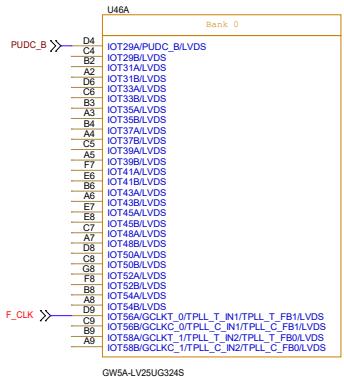
4. VCC core voltage requires a large current, so it is recommended to supply power separately.  
5. The MODE pin is the C8051F200 CONFIG configuration mode selection signal.

5.The MODE pin is the GowinCONFIG configuration mode selection signal. For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714.

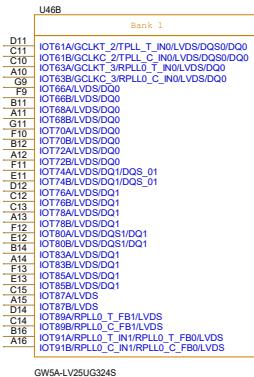
For details about how to select the Mode signal, see "Chapter 3: Arora V 25K FPGA Products Programming and Configuration Guide."

Altra V-ZSR TiGA Products Programming and Configuration Guide.

Title		GOWIN Minimum System Diagram		
Size C	Document Number GW5A-LV25UG324			Rev 2.5
Date:	Thursday, October 24, 2024		Sheet 1	of 16



GW5A-LV25UG324S



GW5A-LV25UG324S

