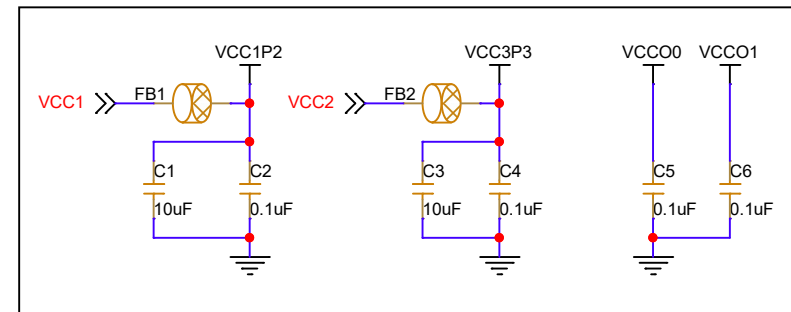


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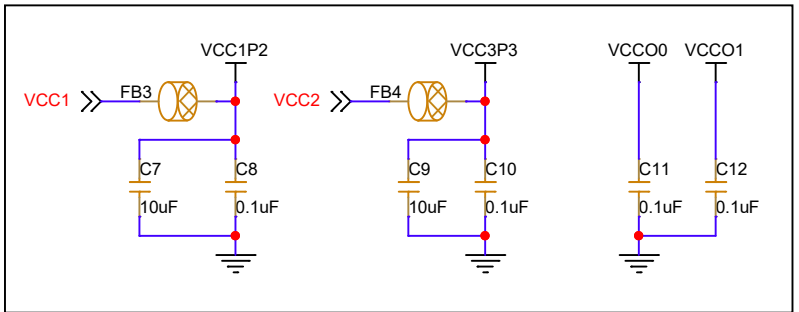
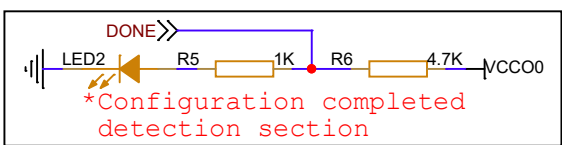
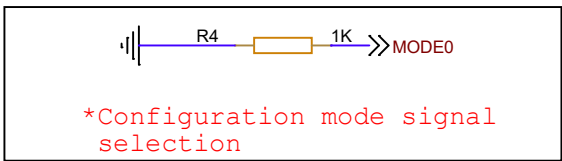
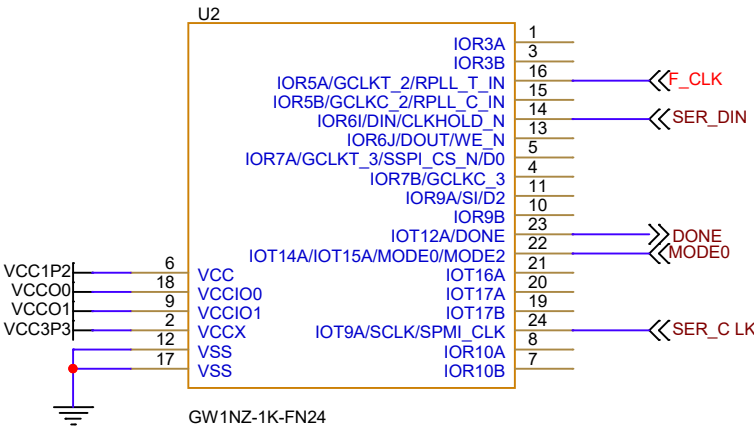


It is recommended that F_CLK signal be provided through an active oscillator crystal.

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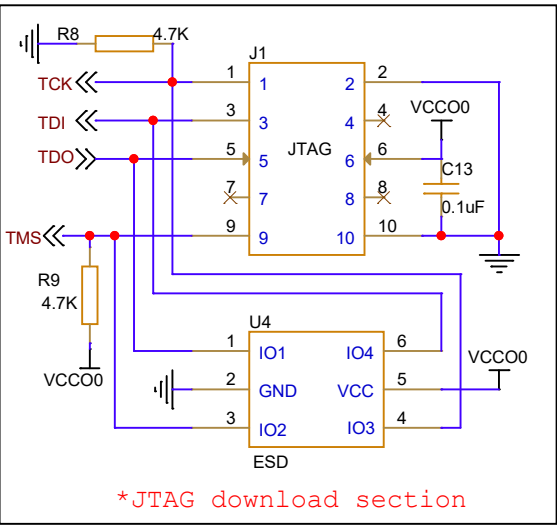
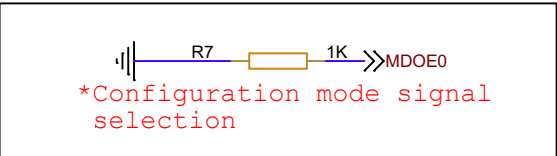
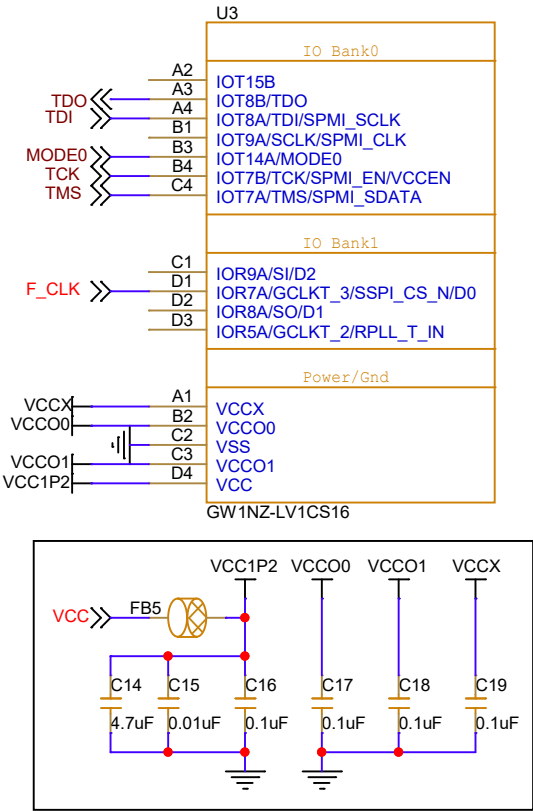
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A

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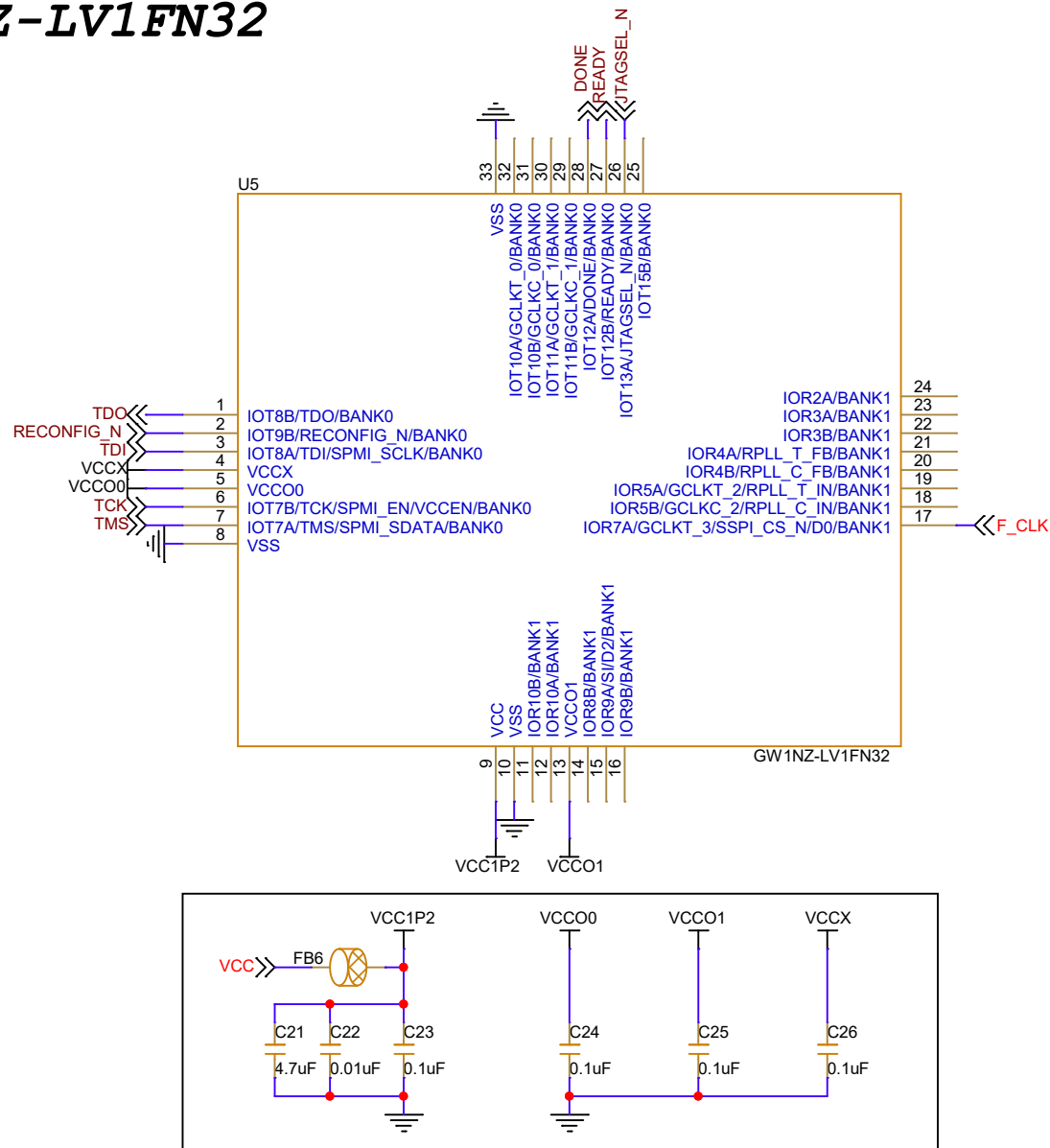


Notes:

1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.

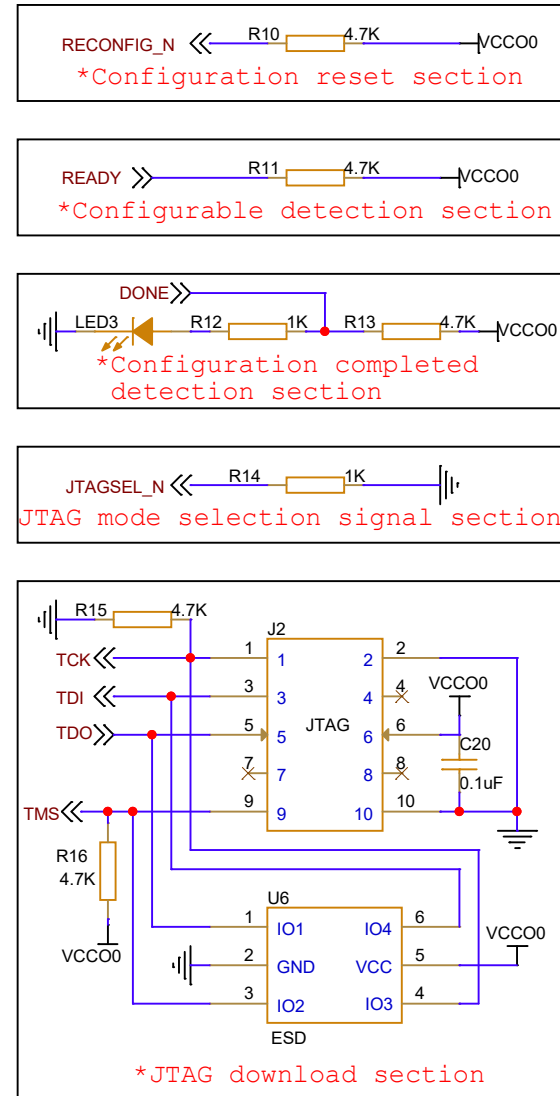


- Notes:
- 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
 - 2.It is recommended that add an ESD protection chip to the JTAG download circuit.



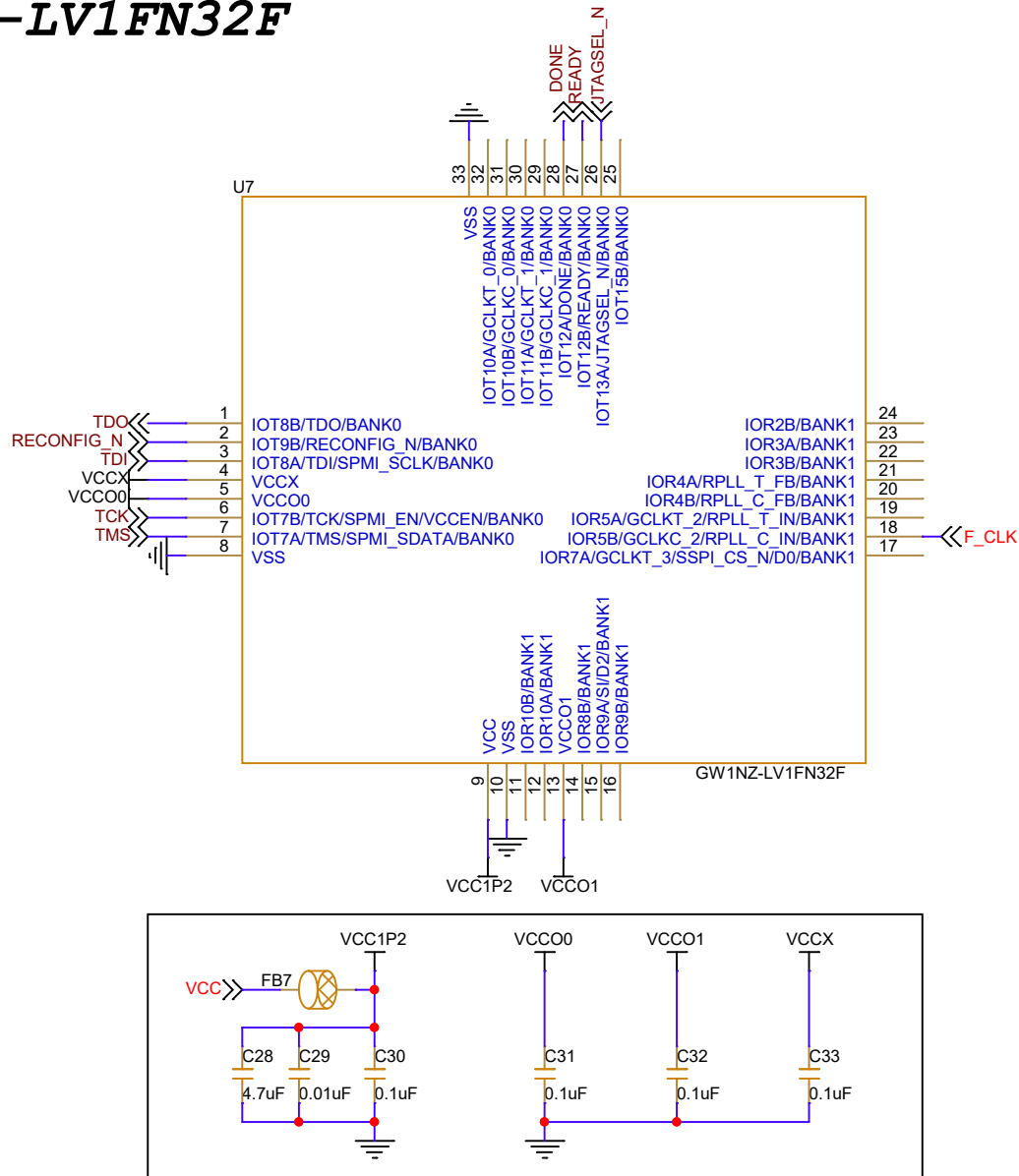
Notes:

- 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.



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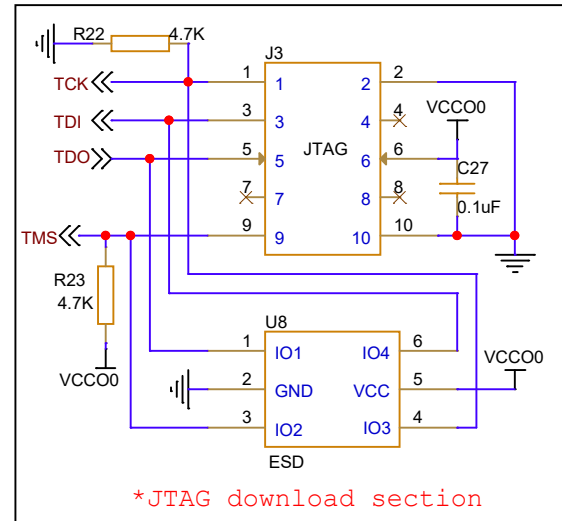


RECONFIG_N << R17 4.7K VCCO0
*Configuration reset section

READY >> R18 4.7K VCCO0
*Configurable detection section

DONE >> LED4 R19 1K R20 4.7K VCCO0
*Configuration completed detection section

JTAGSEL_N << R21 1K
JTAG mode selection signal section



Notes:

1.F_CLK signal is an external input clock signal.

It is recommended that F_CLK signal be provided through an active oscillator crystal.

2.It is recommended that add an ESD protection chip to the JTAG download circuit.

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GOWIN Minimum System Diagram

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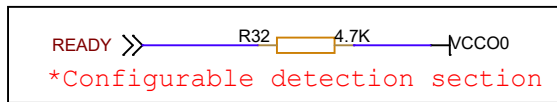
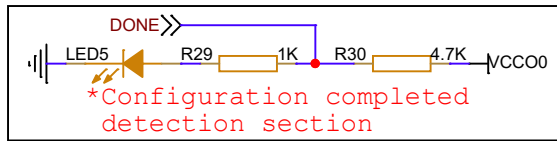
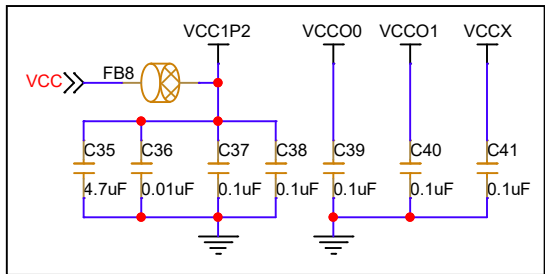
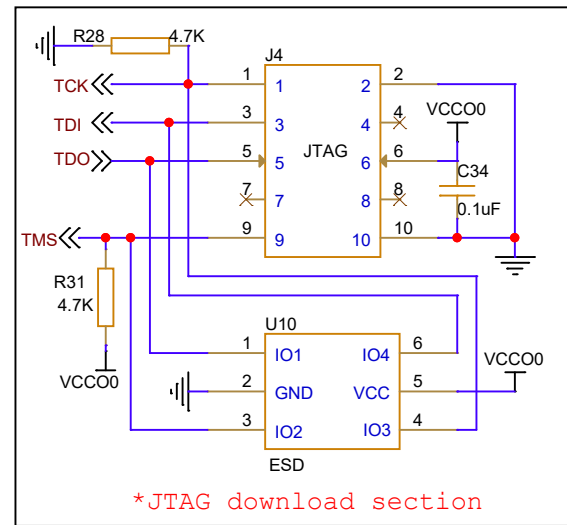
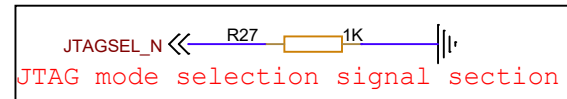
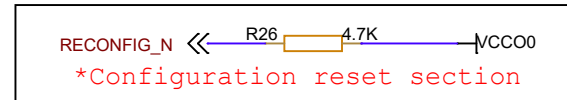
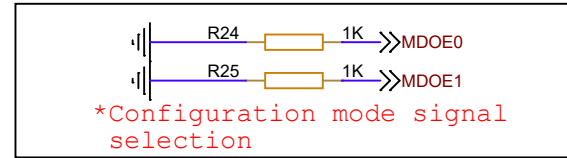
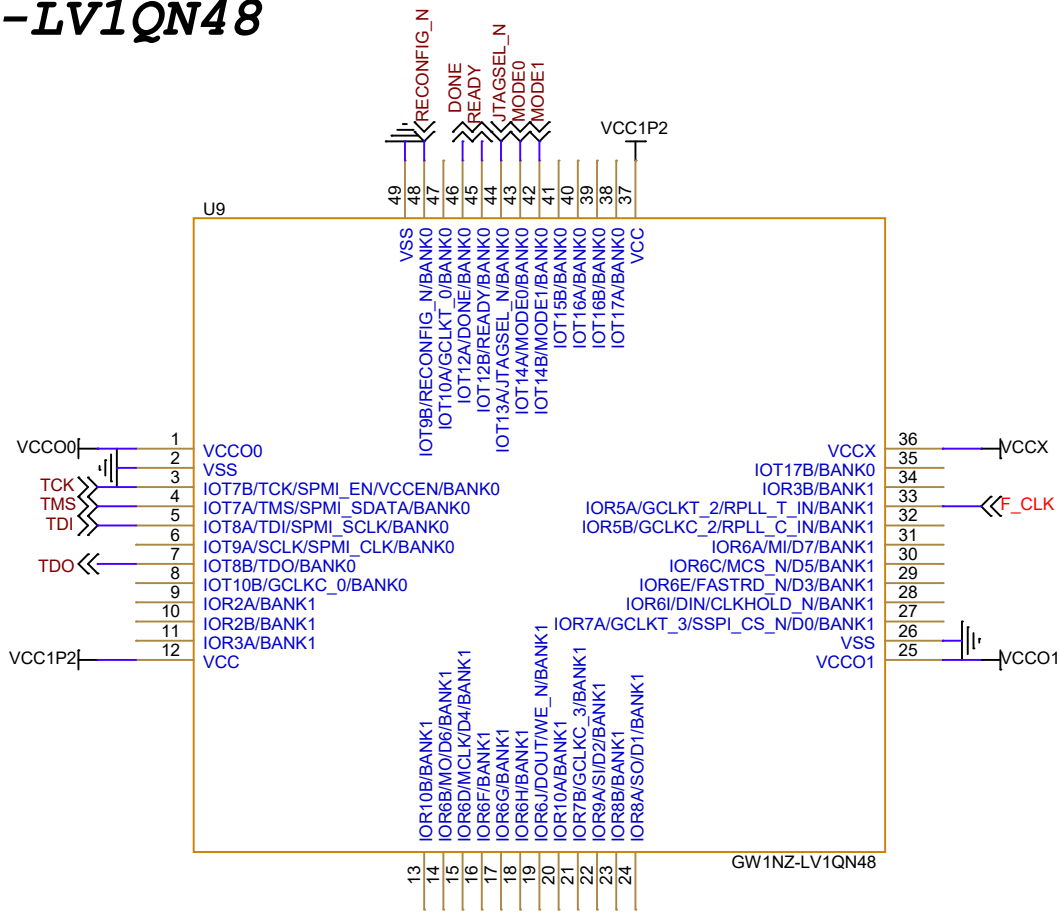
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Notes:

1.F_CLK signal is an external input clock signal.

It is recommended that F_CLK signal be provided through an active oscillator crystal.

2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title
GOWIN Minimum System Diagram

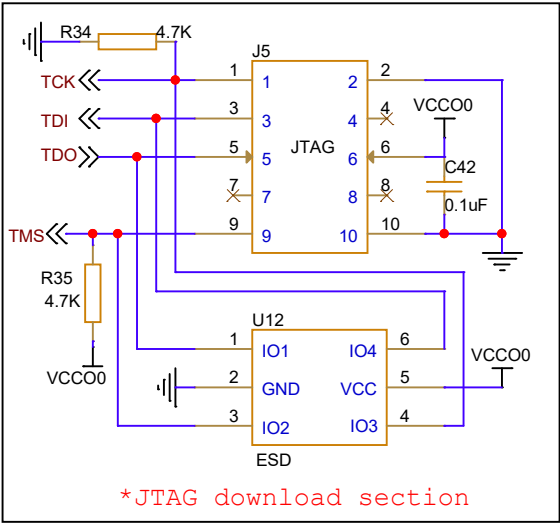
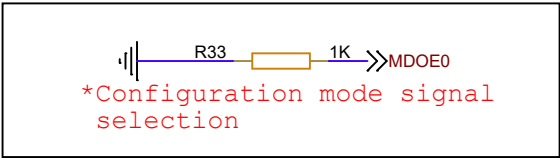
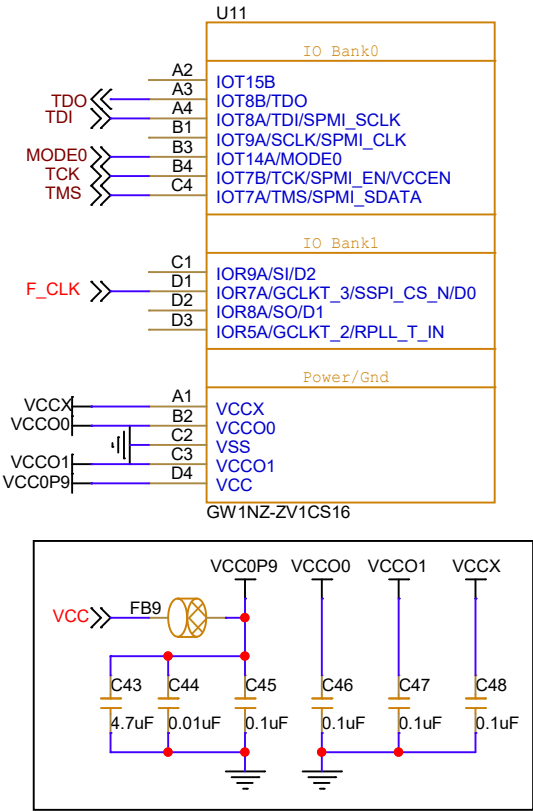
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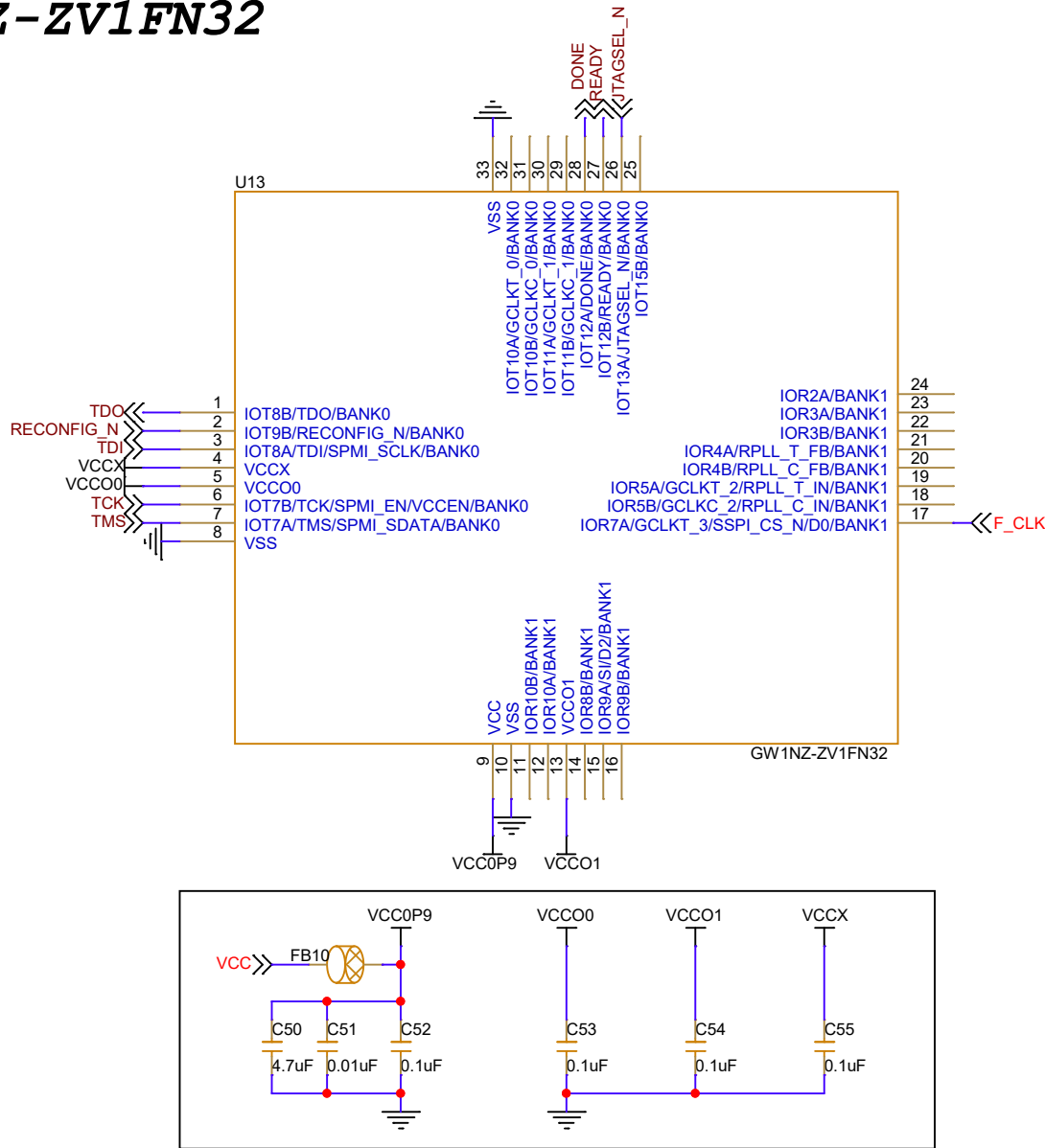
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- Notes:
- 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
 - 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

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Notes:

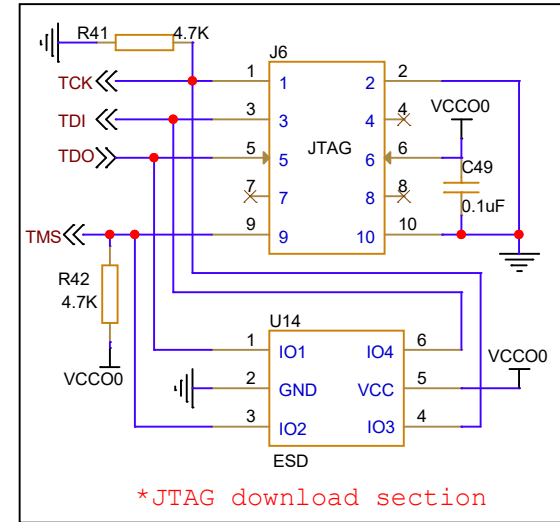
1. F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.

RECONFIG_N << R36 4.7K VCCO0
*Configuration reset section

READY >> R37 4.7K VCCO0
*Configurable detection section

DONE >> LED6 R38 1K R39 4.7K VCCO0
*Configuration completed detection section

JTAGSEL_N << R40 1K
JTAG mode selection signal section



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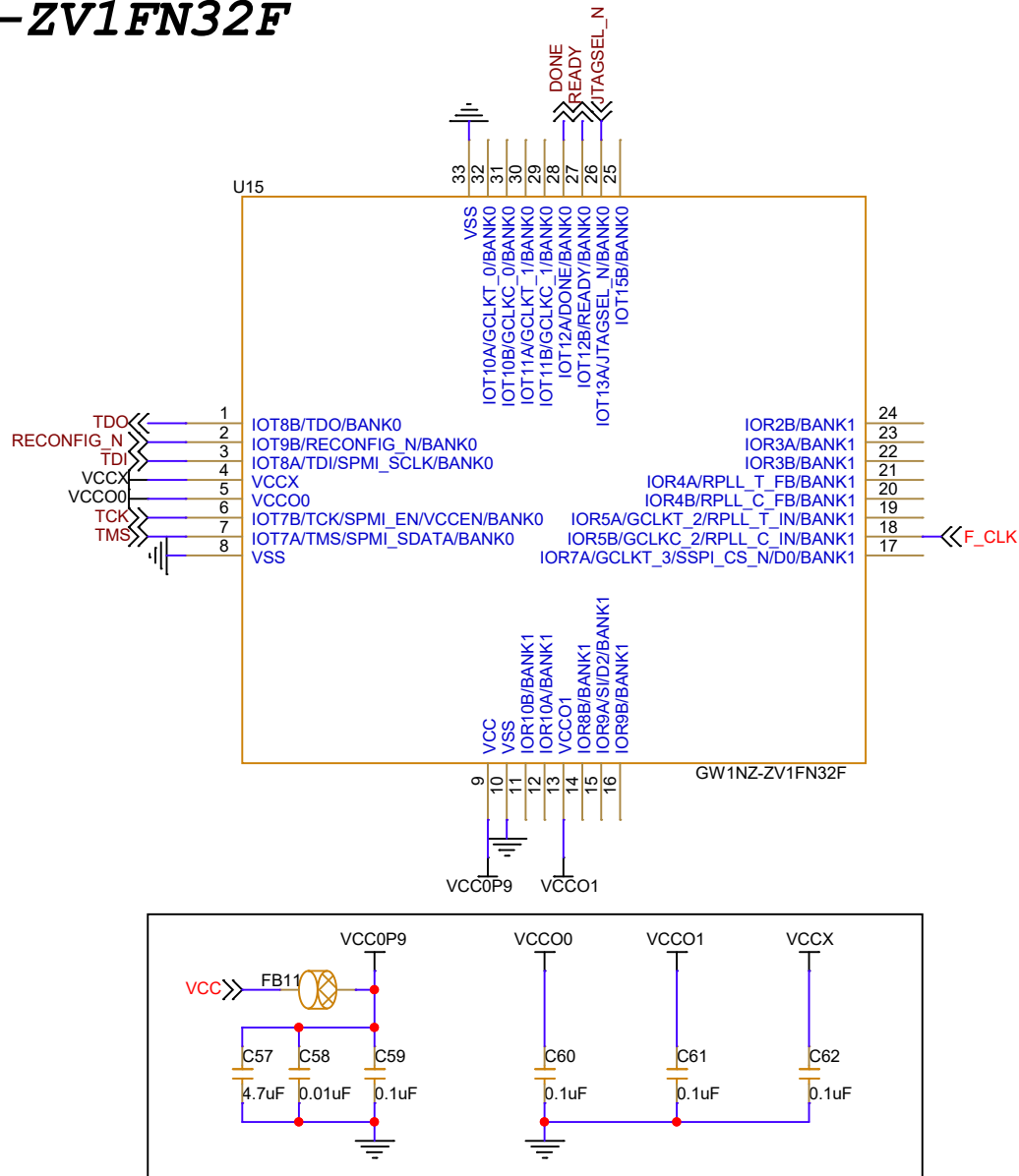
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Notes:

1.F_CLK signal is an external input clock signal.

It is recommended that F_CLK signal be provided through an active oscillator crystal.

2.It is recommended that add an ESD protection chip to the JTAG download circuit.

RECONFIG_N << R43 4.7K VCCO0
*Configuration reset section

READY >> R44 4.7K VCCO0
*Configurable detection section

DONE >> LED7 R45 1K R46 4.7K VCCO0
*Configuration completed detection section

JTAGSEL_N << R47 1K
JTAG mode selection signal section

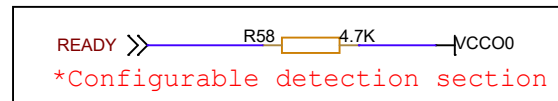
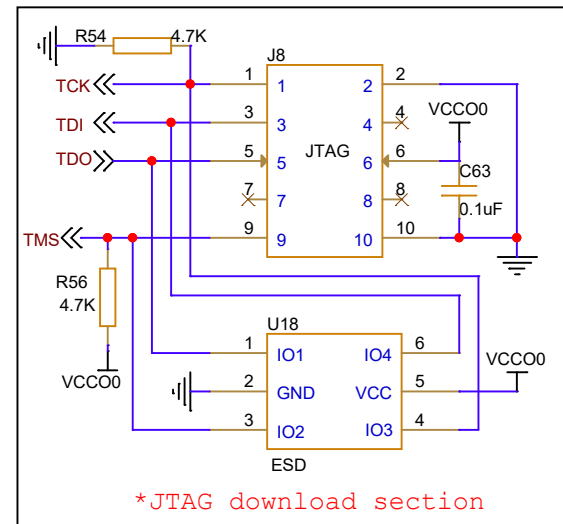
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2.It is recommended that add an ESD protection chip to the JTAG download circuit.

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