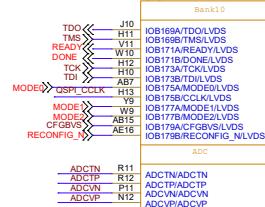
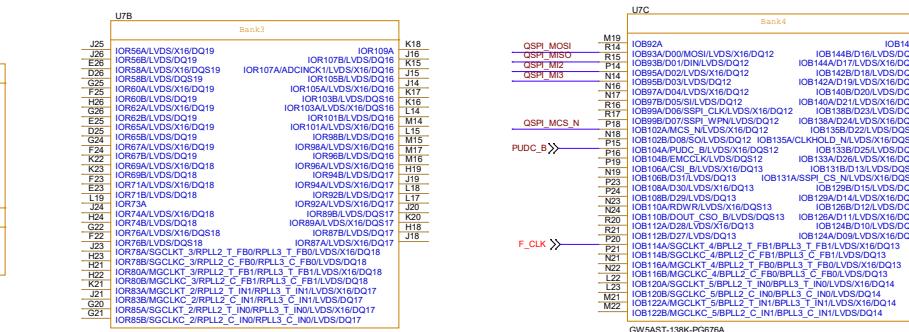




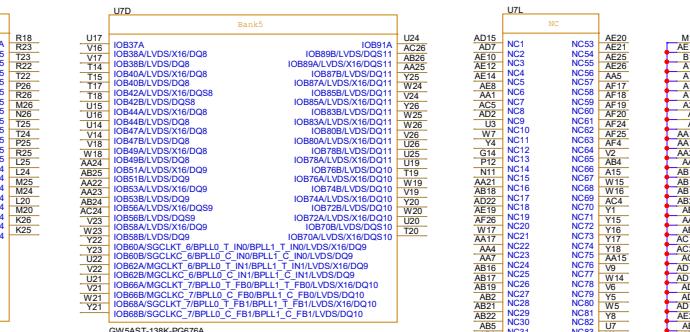
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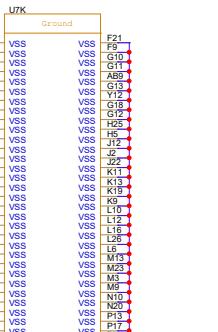
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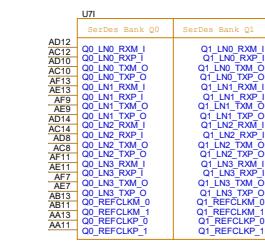
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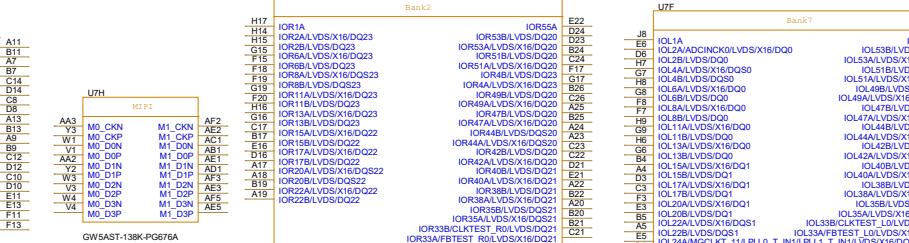
NC82 U7 AE4  
NC83 Y6 AE6



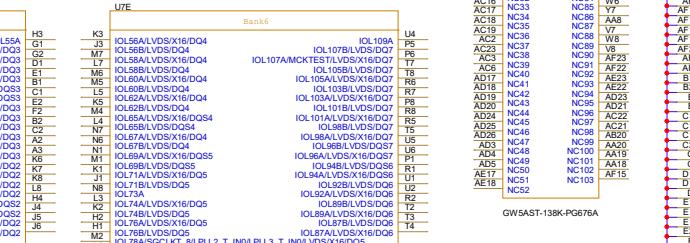
VSS P17  
VSS P7



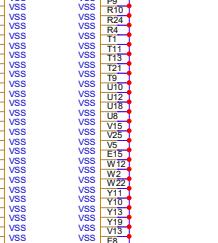
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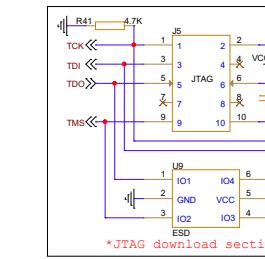
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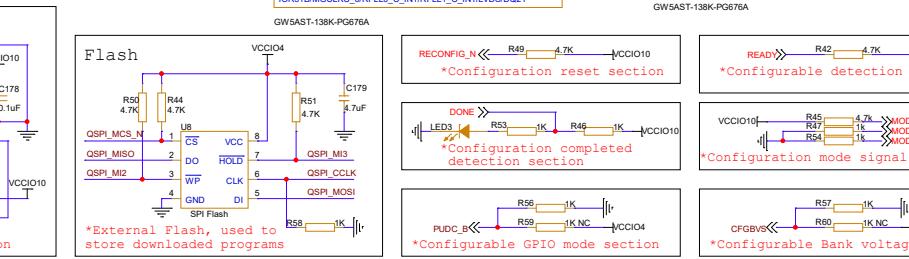
E4  
E7



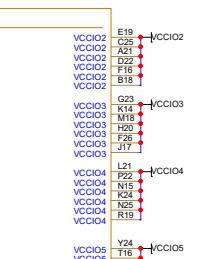
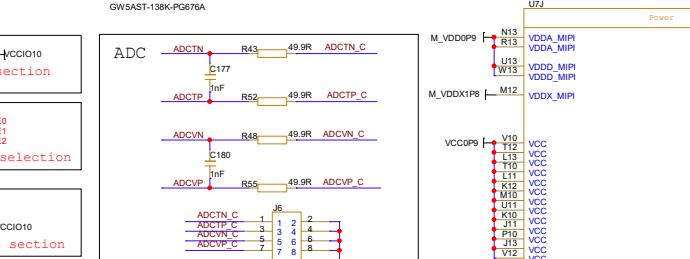
The diagram shows two vertical lines representing bus segments. The top line is labeled 'VSS' at its left end. The bottom line is also labeled 'VSS' at its left end. A horizontal line connects the two 'VSS' labels. From this central connection point, two red dots extend downwards, each connected by a blue line to a red dot on the bottom 'VSS' line. The label 'E8' is positioned above the top red dot, and the label 'F9' is positioned below the bottom red dot.



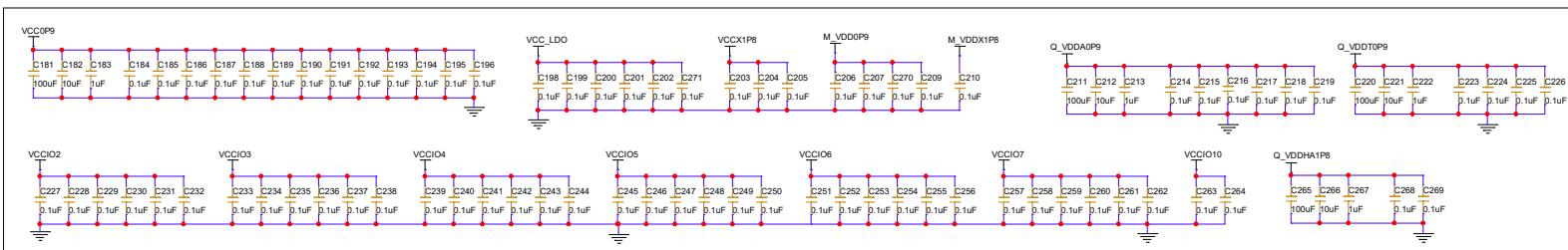
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VCCIO5 T16 [VCCIO5]  
VCCIO5 U23



**Notes:**

- 1. $\text{F}_{\text{CLK}}$  signal is an external input clock signal.  
It is recommended that  $\text{F}_{\text{CLK}}$  signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.  
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG704, Arora V FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.  
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG704, Arora V FPGA Products Programming and Configuration Guide .