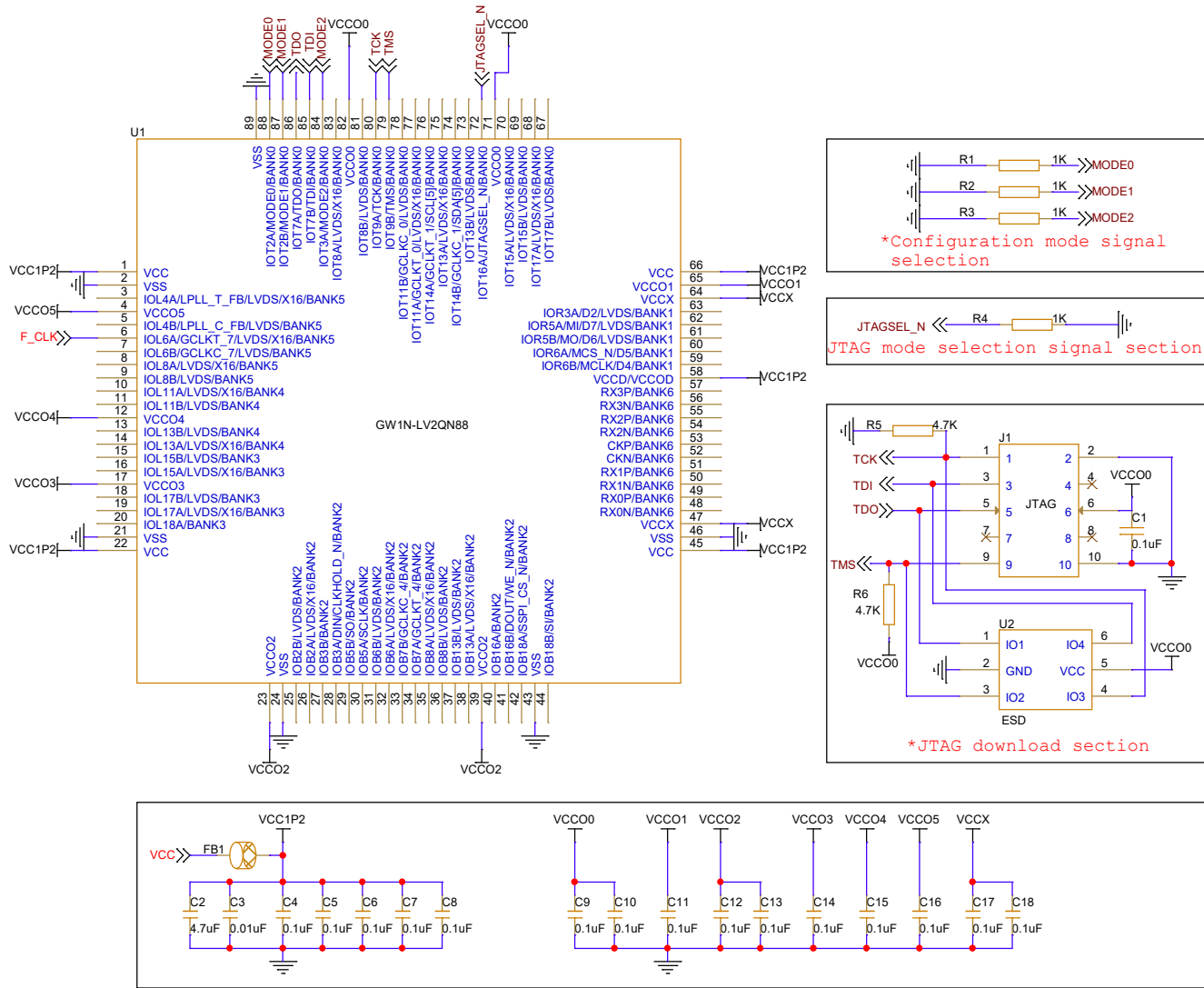


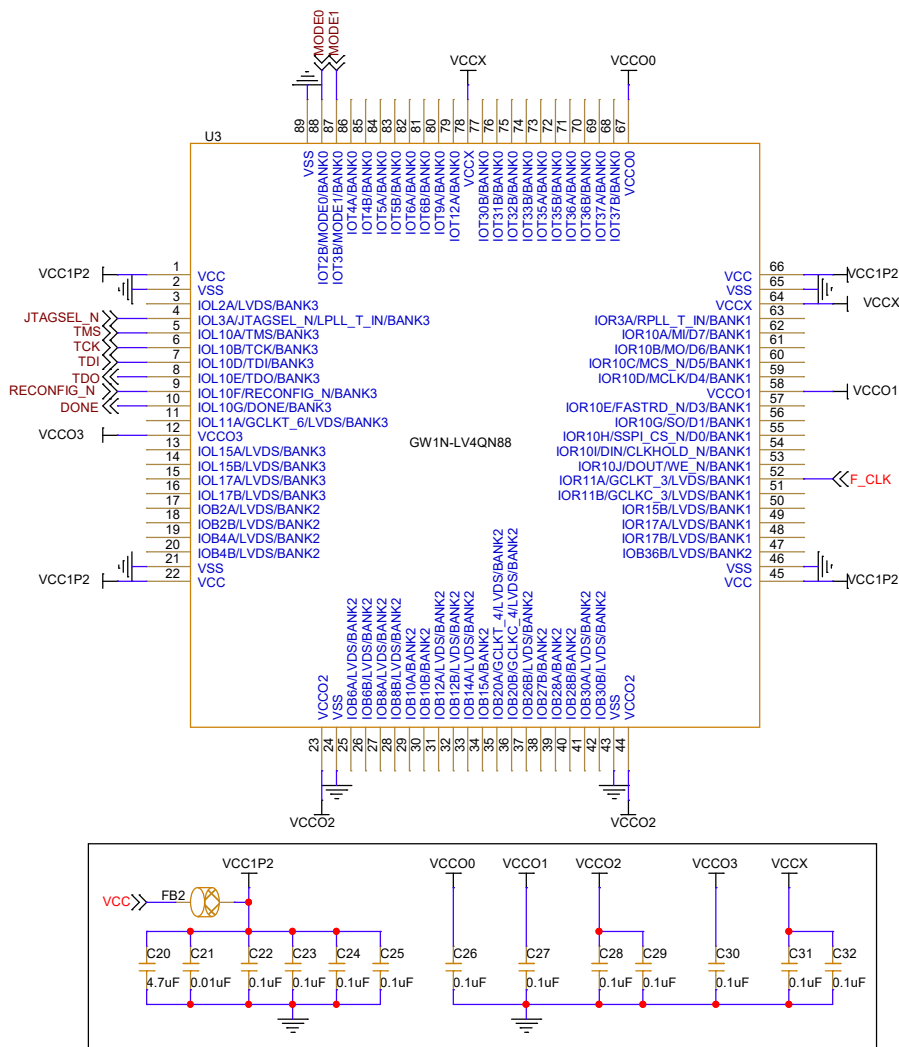
# GW1N-LV2QN88



Notes:  
1.F\_CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.  
2.It is recommended that add an ESD protection chip to the JTAG download circuit.

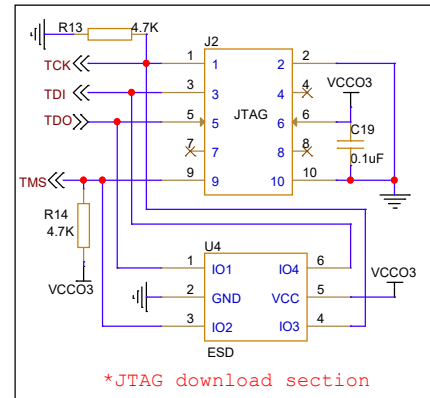
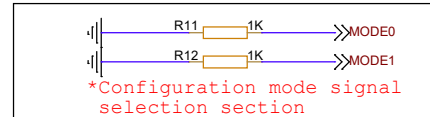
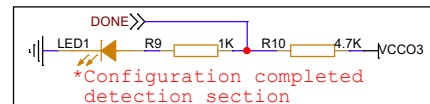
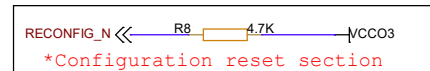
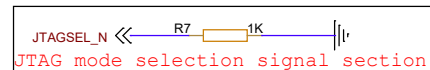
Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-LV2QN88	3.1
Date:	Friday, August 09, 2024	Sheet 1 of 11

# GW1N-LV4QN88



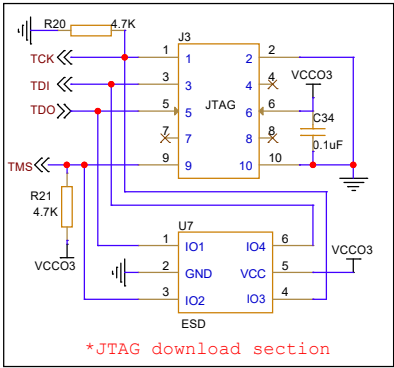
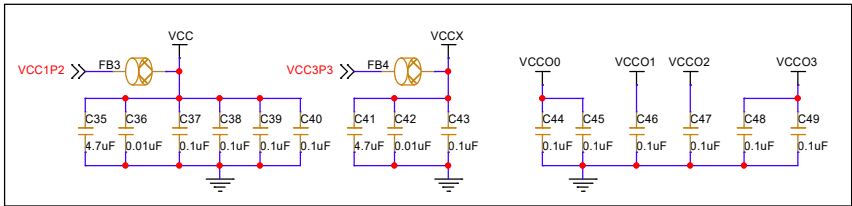
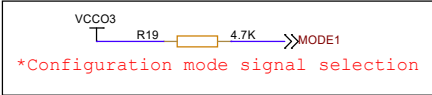
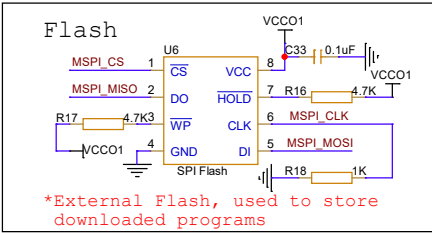
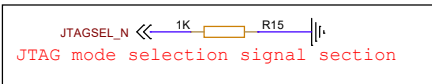
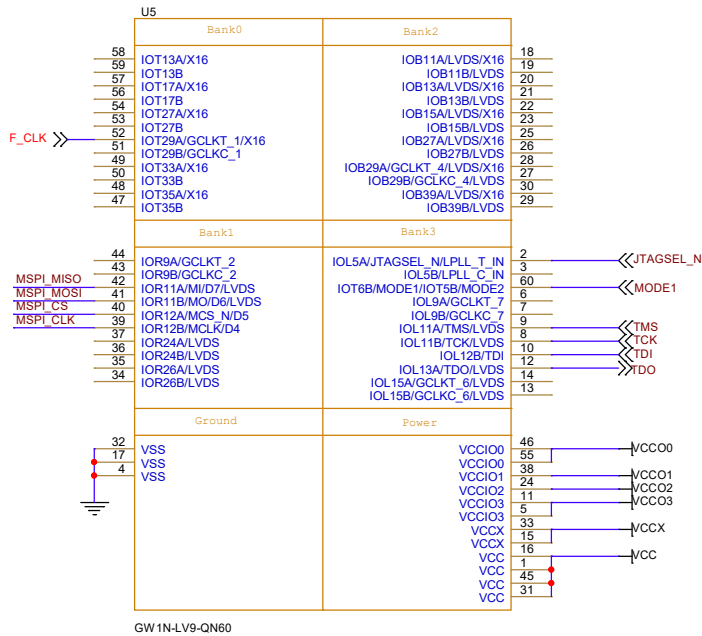
## Notes:

- 1.F CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

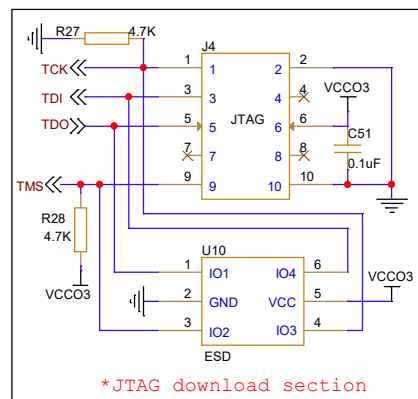
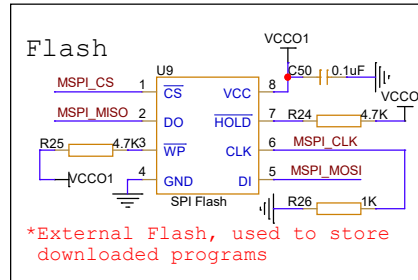
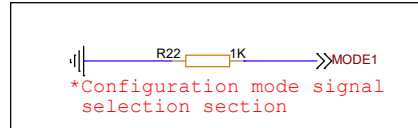
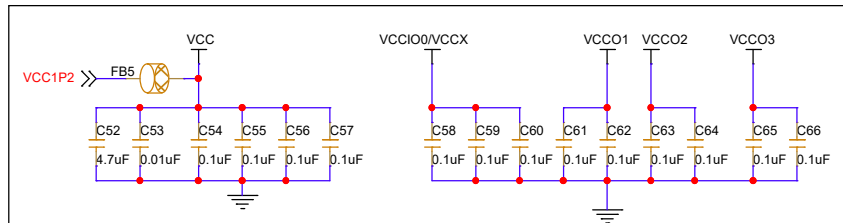
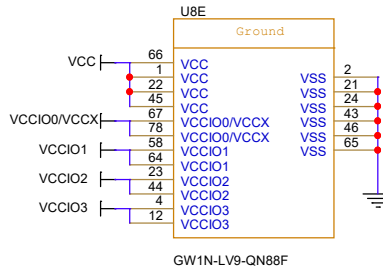
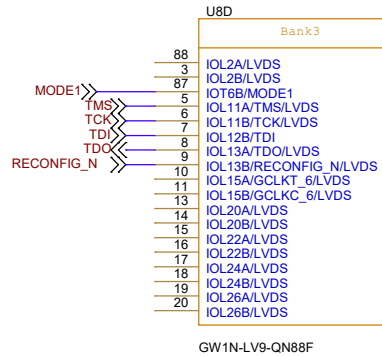
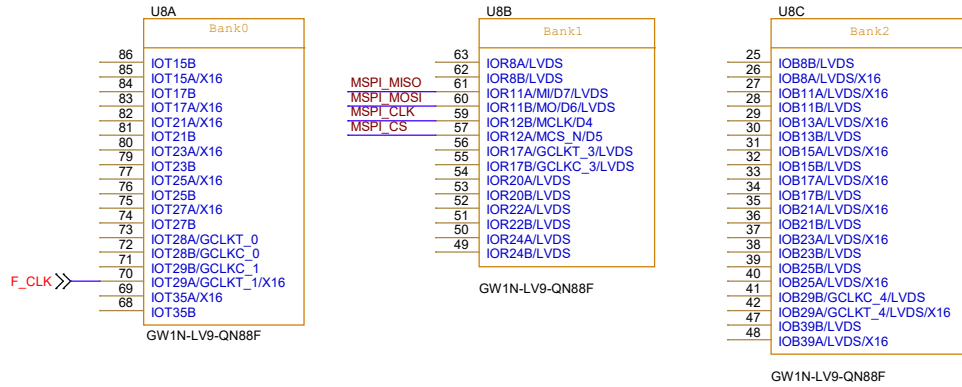


Title		
Gowin FPGA-AOTOMOTIVE Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-LV4QN88	3.1
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GW1N-LV9QN60



- Notes:
- 1.F CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
  - 2.External Flash memory is used to store downloaded programs.  
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
  - 3.It is recommended that add an ESD protection chip to the JTAG download circuit.

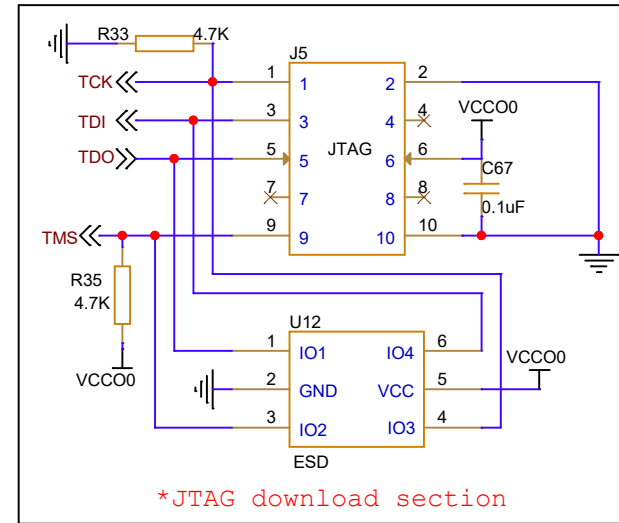
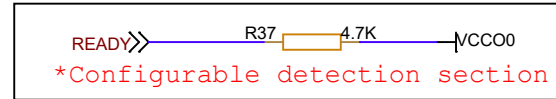
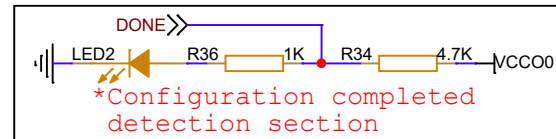
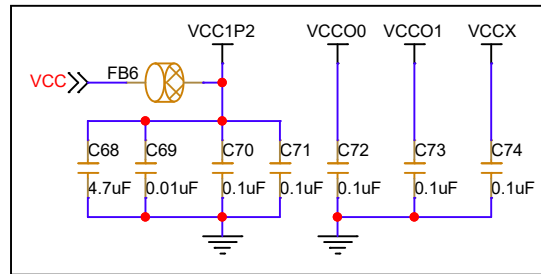
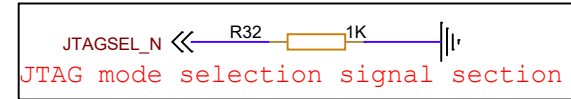
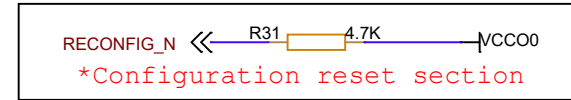
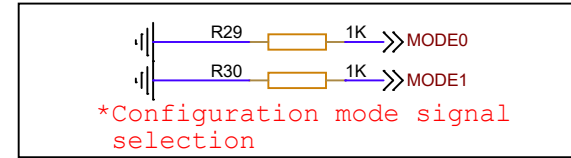
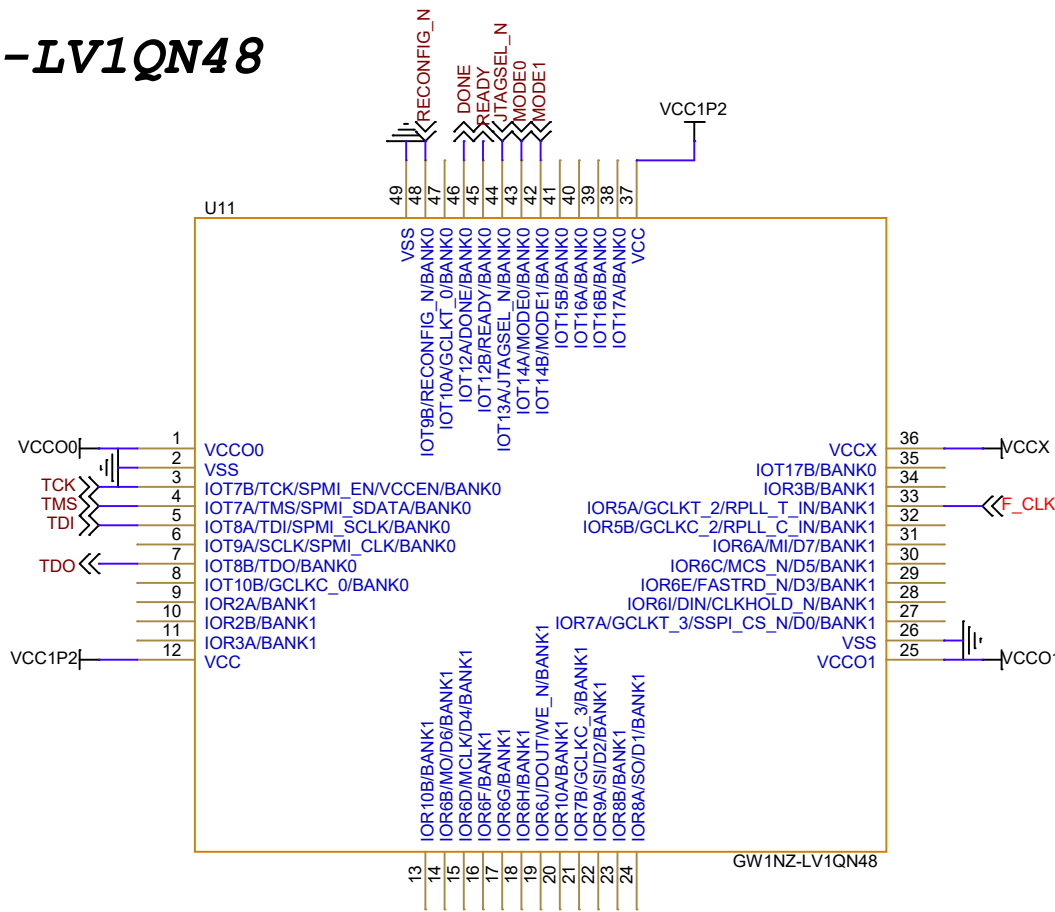


# Notes:

- 1.F CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-LV9QN88F	3.1
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# GW1NZ-LV1QN48

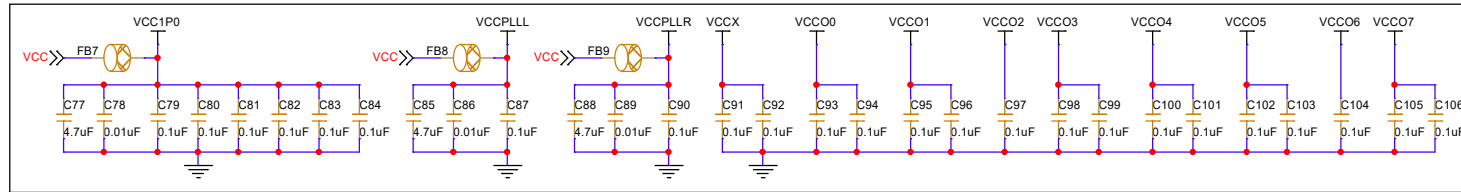
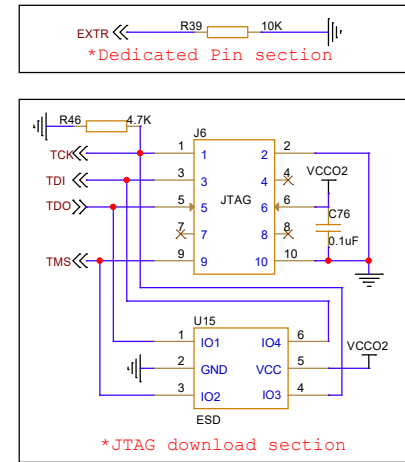
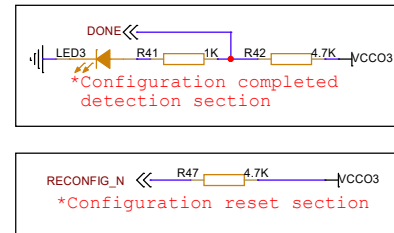
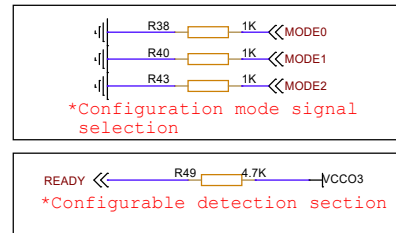
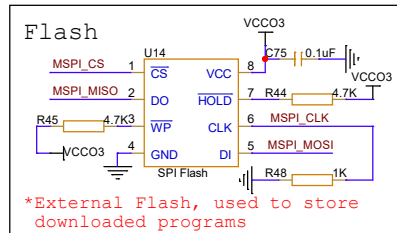
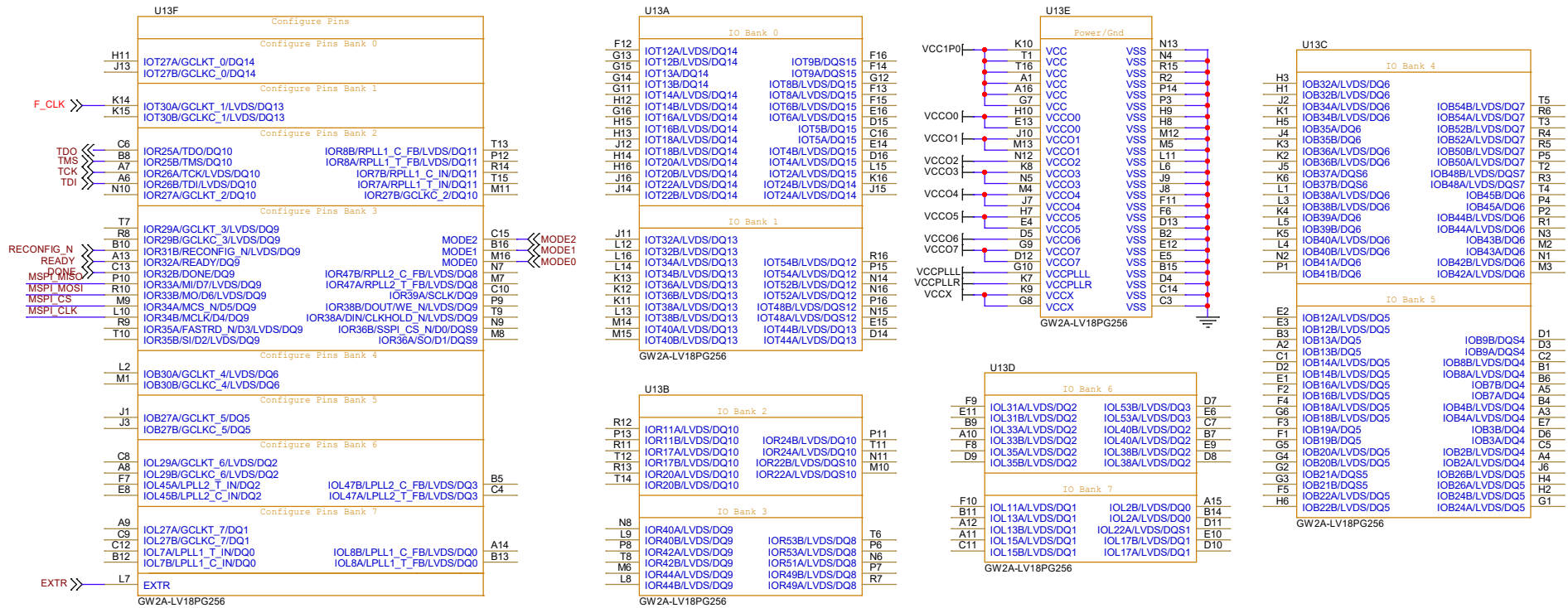


## Notes:

- 1.F\_CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
Gowin FPGA-AOTOMOTIVE Minimum System Diagram		
Size	Document Number	Rev
A4	GW1NZ-LV1QN48	3.1
Date:	Friday, August 09, 2024	Sheet 5 of 11

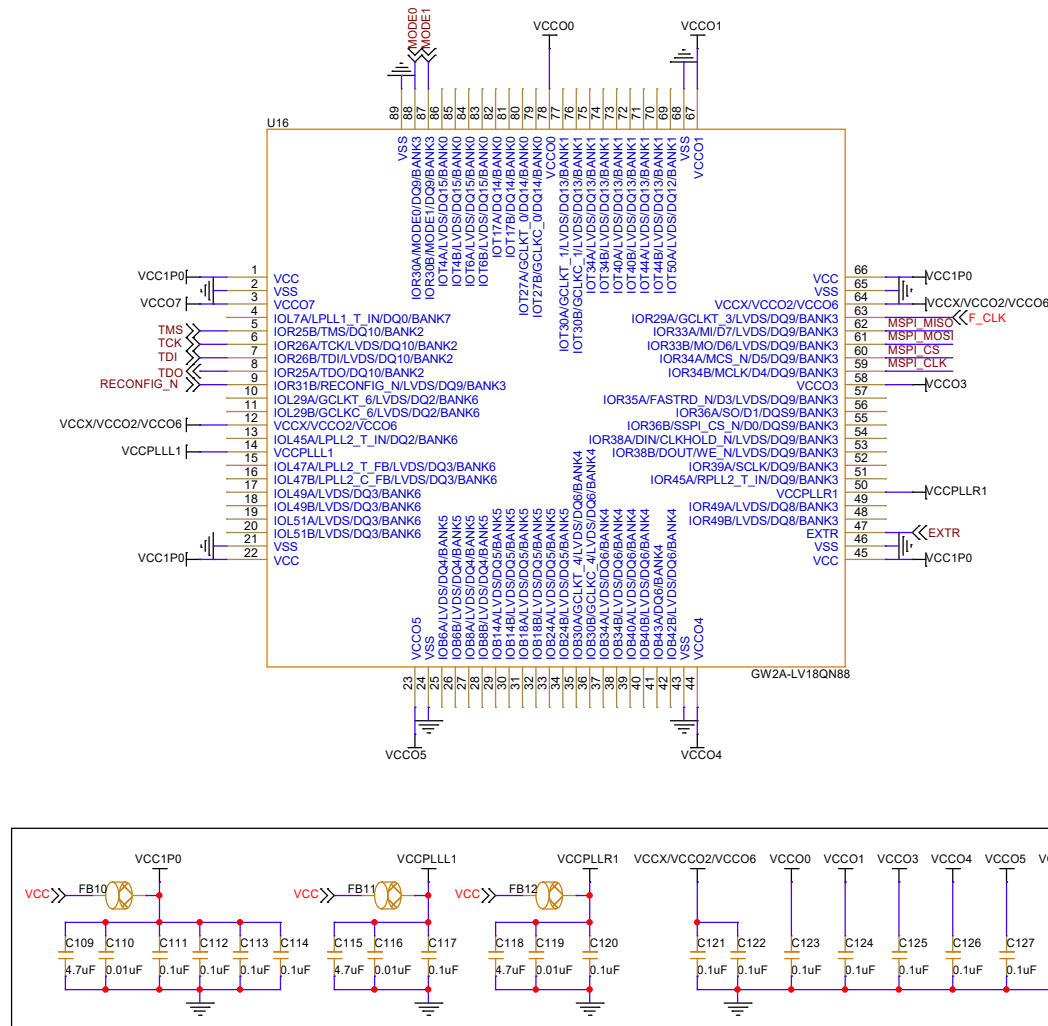
# GW2A-LV18PG256



- Notes:
- 1.F CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
  - 2.External Flash memory is used to store downloaded programs.  
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
  - 3.It is recommended that add an ESD protection chip to the JTAG download circuit.

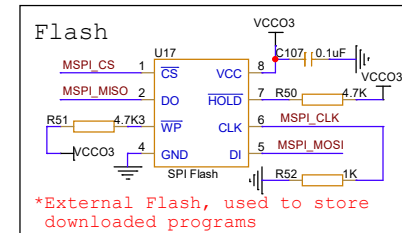
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Gowin FPGA-AOTOMOTIVE Minimum System Diagram		
Size	Document Number	Rev
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Date:	Friday, August 09, 2024	Sheet 6 of 11

***GW2A-LV18QN88***

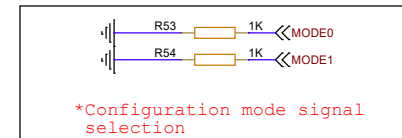


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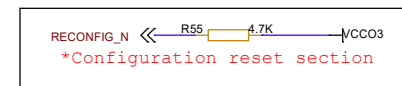
1. F\_CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
2. External Flash memory is used to store downloaded programs.  
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
3. It is recommended that add an ESD protection chip to the JTAG download circuit.



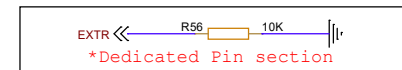
\*External Flash, used to store downloaded programs



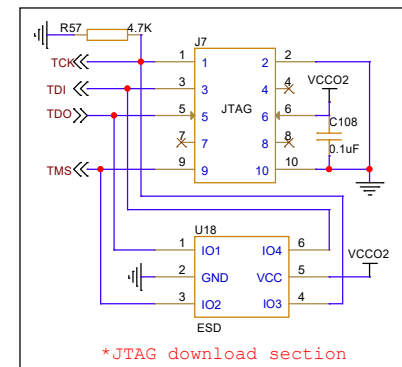
```
*Configuration mode signal
  selection
```



\*Configuration reset section

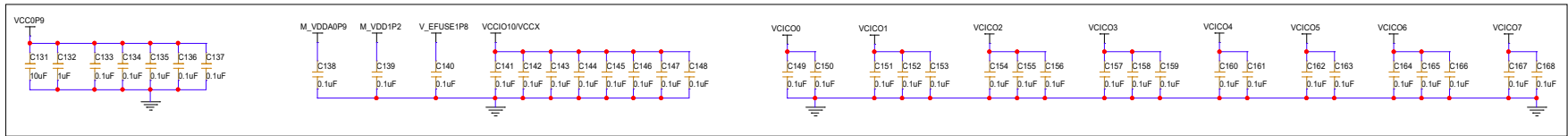
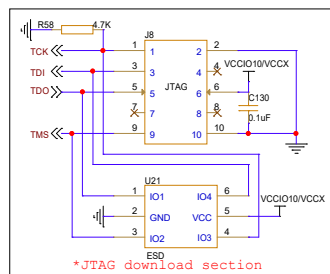
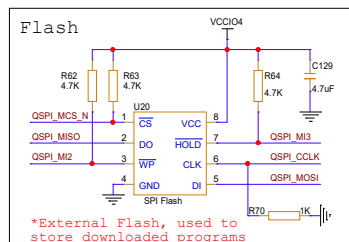
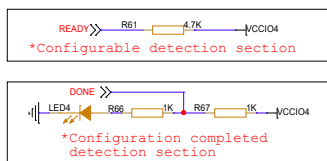
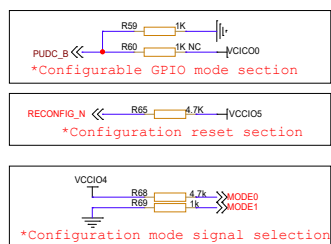
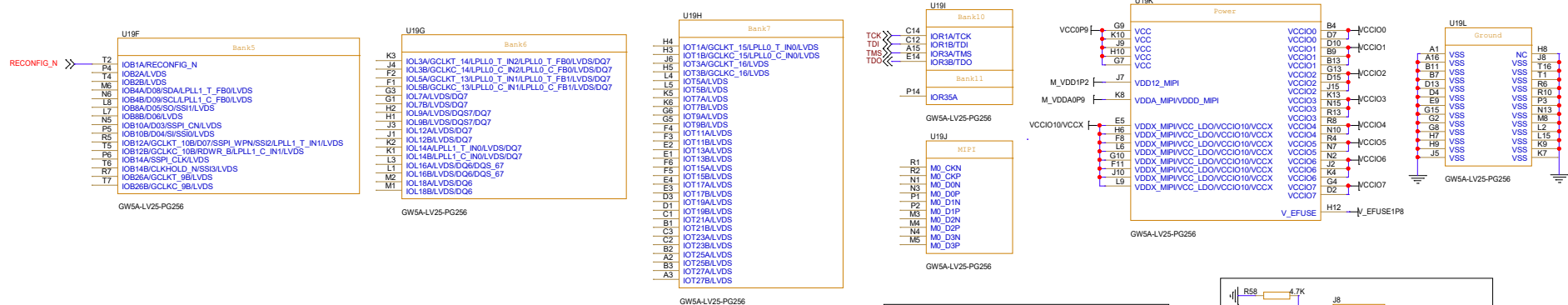
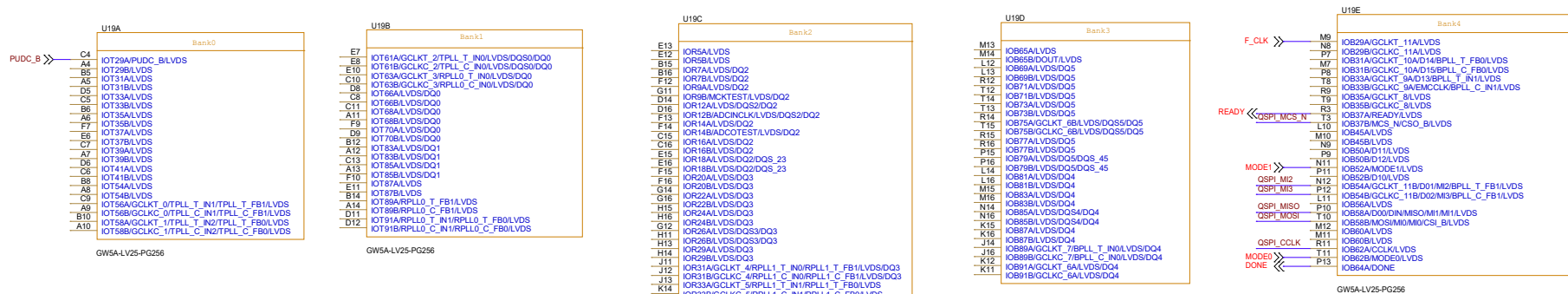


\*Dedicated Pin section



\*JTAG download section

***GW5A-LV25PG256***



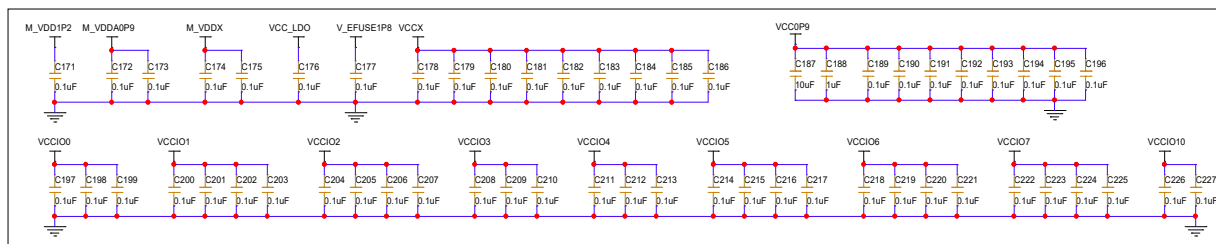
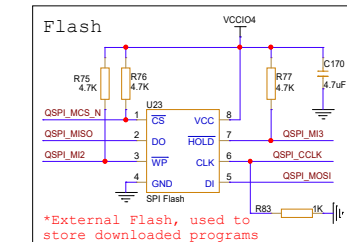
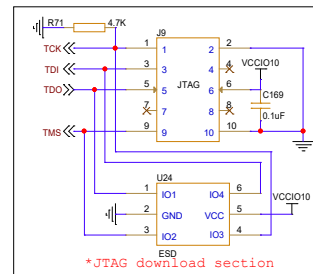
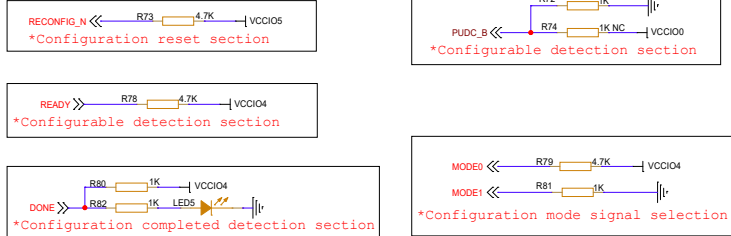
Notes:

- 1.F CLK signal is an external input clock signal. It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
- For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
- For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.

Title GOWIN Minimum System Diagram			
Size C	Document Number GW5A-LV25PG256	Rev 3.1	
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***GW5A-LV25UG324F***

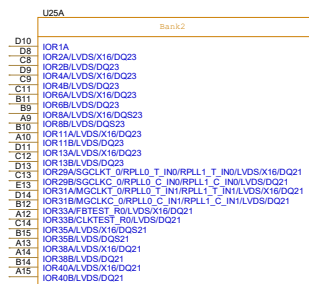


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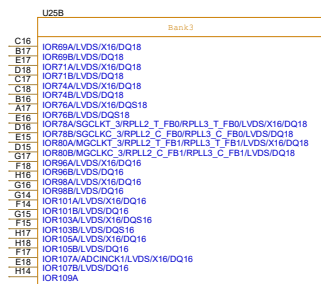
- 1.F CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.  
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.  
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.

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GOWIN Minimum System Diagram				
Size C	Document Number GW5A-LV25U/G324F			Rev. 3
Date	Field	August 09, 2004	Drawn	by

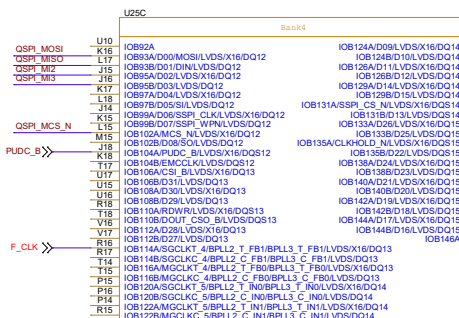
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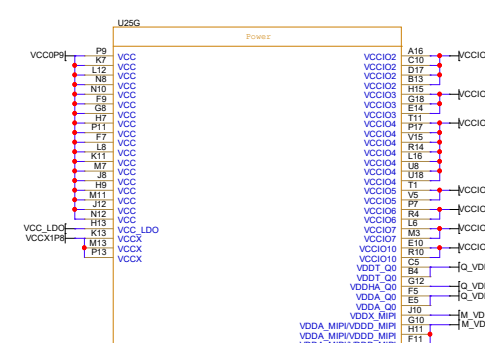
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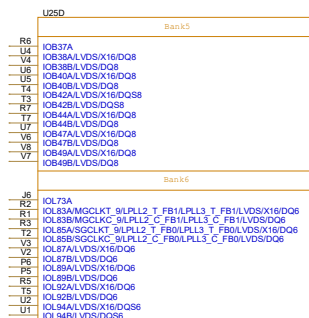
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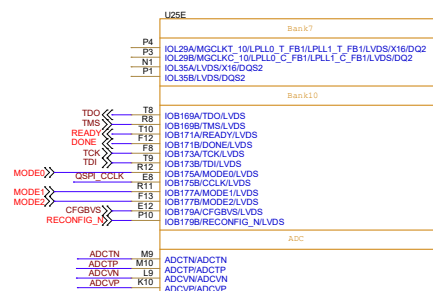
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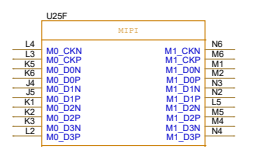
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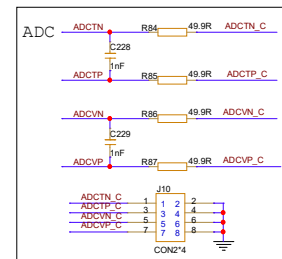
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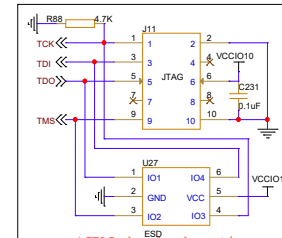
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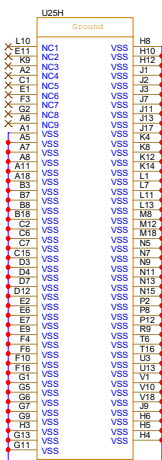
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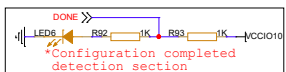
88 4.7K



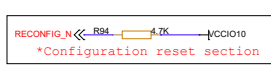
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\*ITAG download section



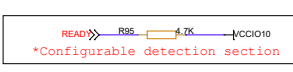
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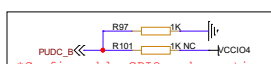
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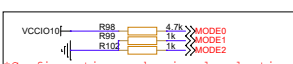
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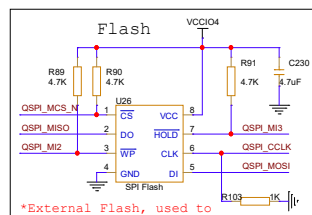
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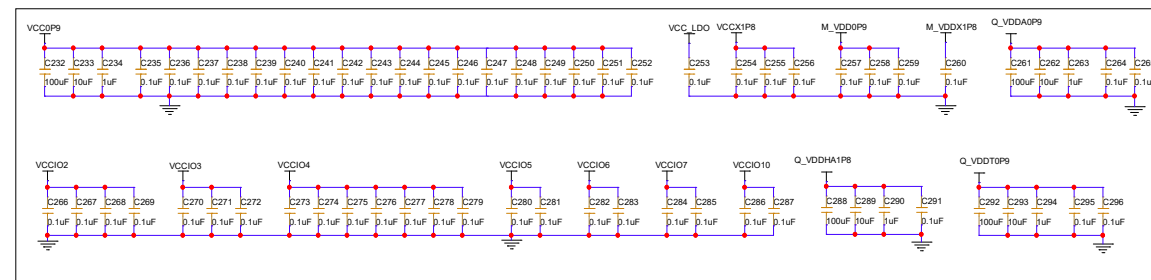
### Configurable GPIO mode section



configuration mode signal selection



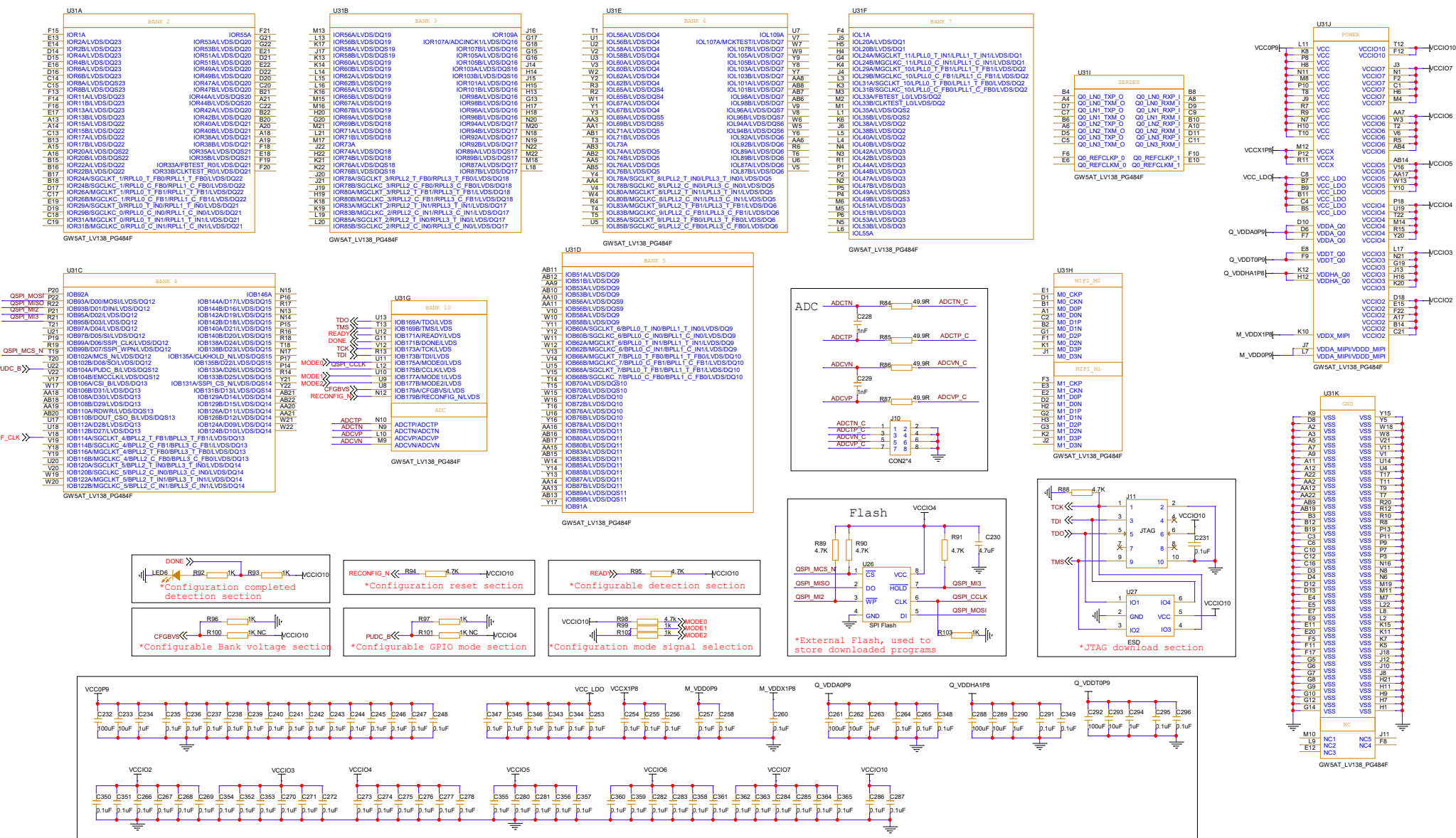
\*External Flash used to



Notes:

1. F\_CLK signal is an external input clock signal.
- It is recommended that F\_CLK signal be provided through an active oscillator crystal.
2. External Flash memory is used to store downloaded programs.
- For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG704, Arara V FPGA Products Programming and Configuration Guide .
3. It is recommended that add an ESD protection chip to the JTAG download circuit.
4. VCC core voltage requires a large current, so it is recommended to supply power separately.
5. The MODE pin is the GowinCONFIG configuration mode selection signal.
- For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG704, Arara V FPGA Products Programming and Configuration Guide.

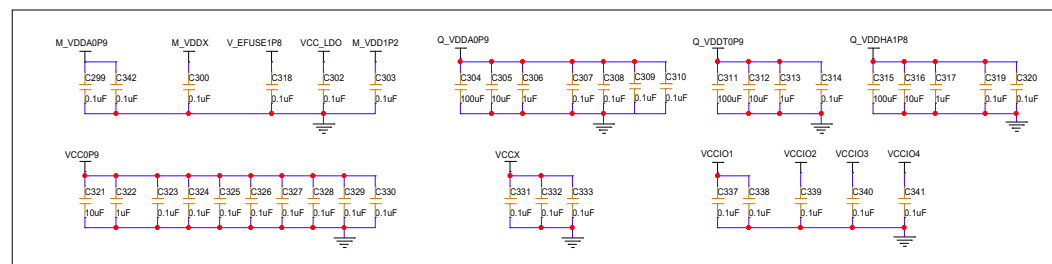
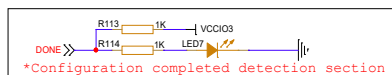
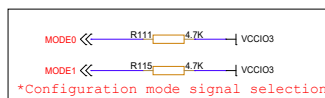
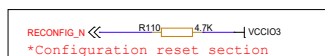
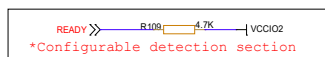
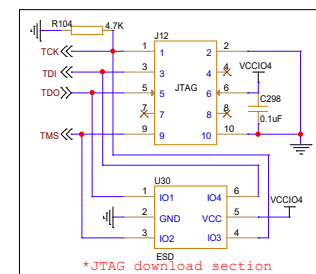
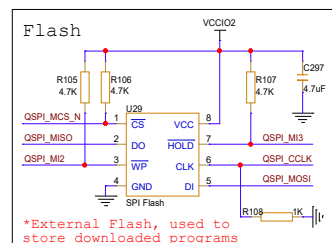
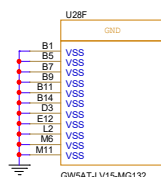
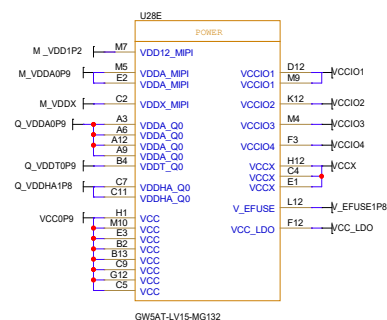
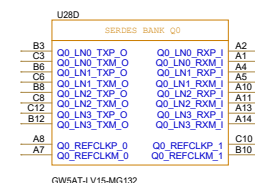
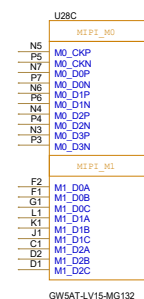
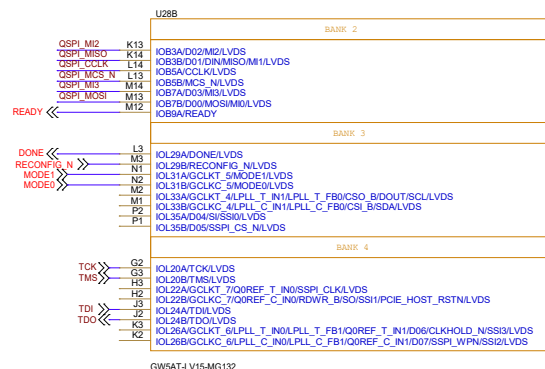
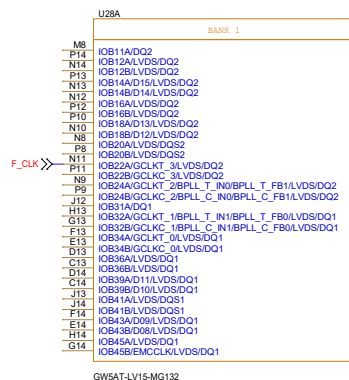
***GW5AT LV138PG484F***



Notes:

1. F\_CLK signal is an external input clock signal.
- It is recommended that F\_CLK signal be provided through an active oscillator crystal.
2. External Flash memory is used to store downloaded programs.
- For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG704, Arora V FPGA Products Programming and Configuration Guide .
3. It is recommended that add an ESD protection chip to the JTAG download circuit.
4. VCC core voltage requires a large current, so it is recommended to supply power separately.
5. The MODE pin is the GowinCONFIG configuration mode selection signal.
- For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG704 Arora V FPGA Products Programming and Configuration Guide.

***GW5AT-LV15MG132***



Notes:

1. F\_CLK signal is an external input clock signal.
  2. It is recommended that F\_CLK signal be provided through an active oscillator crystal.
  3. External Flash memory is used to store downloaded programs.
  4. For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG720, Arara V 15K FPGA Products Programming and Configuration Guide .
  5. It is recommended that add an ESD protection chip to the JTAG download circuit.
  6. VCC core voltage requires a large current, so it is recommended to supply power separately.
  7. The MODE pin is the GowinCONFIG configuration mode selection signal.
- For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG720, Arara V 15K FPGA Products Programming and Configuration Guide.