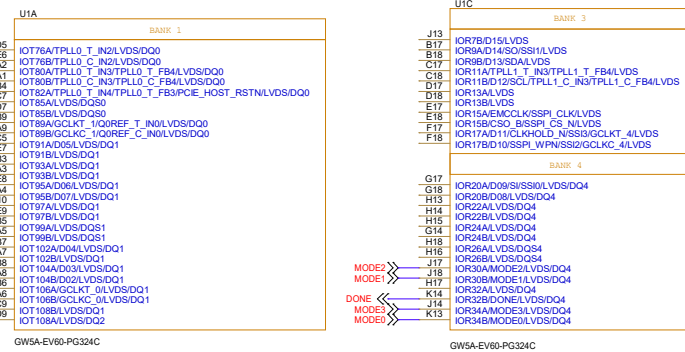
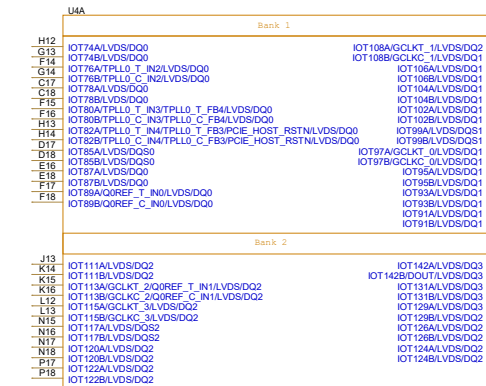


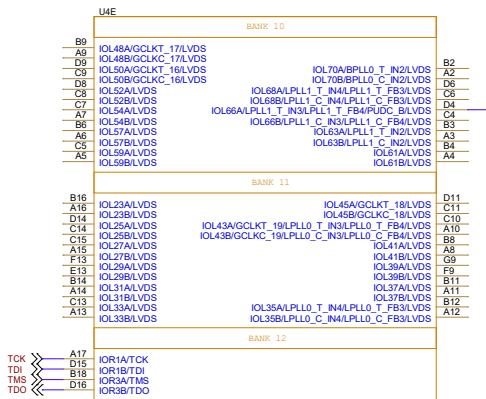
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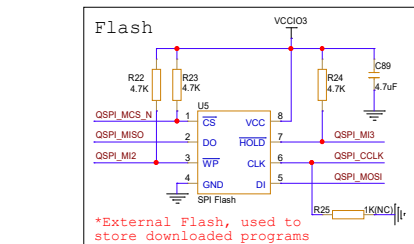
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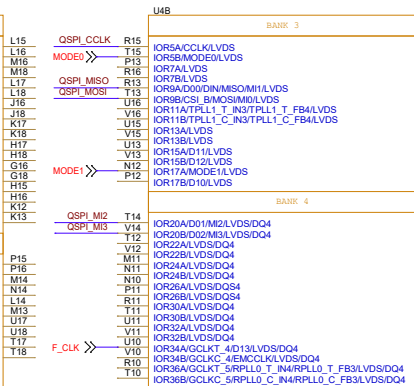
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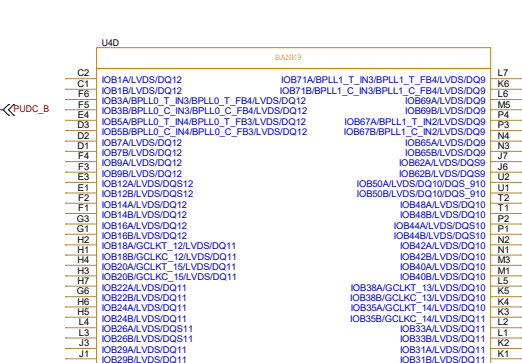
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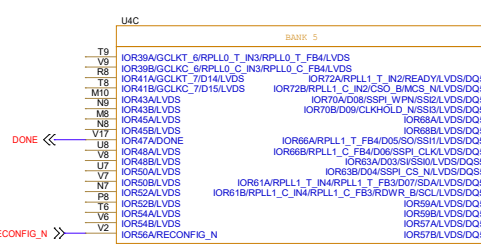
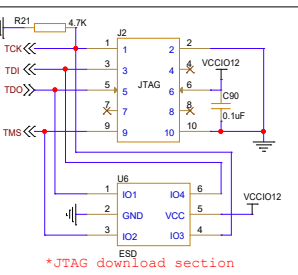
1. F\_CLK signal is an external input clock signal.
2. It is recommended that F\_CLK signal be provided through an active oscillator crystal.
3. External Flash memory is used to store downloaded programs.
4. For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG718, Arara V 60K FPGA Products Programming and Configuration Guide .
5. It is recommended that add an ESD protection chip to the JTAG download circuit.
6. VCC core voltage requires a large current, so it is recommended to supply power separately.
7. The MODE pin is the GowinCONFIG configuration mode selection signal.
8. For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG718, Arara V 60K FPGA Products Programming and Configuration Guide.



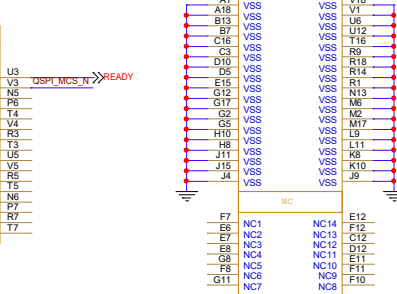
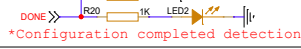
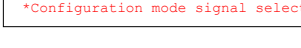
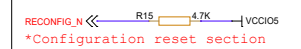
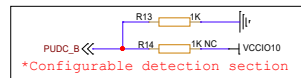
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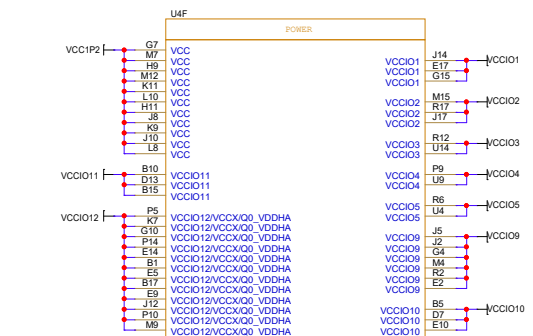
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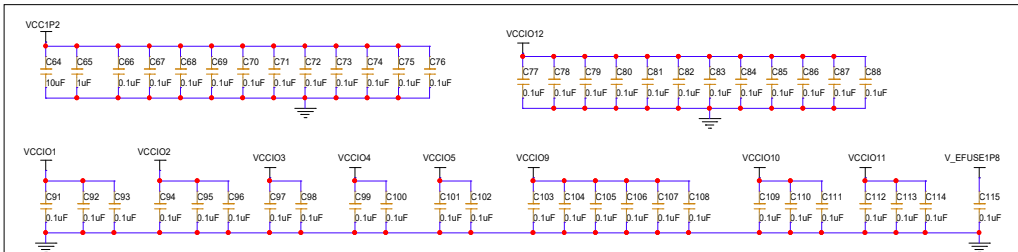
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GW5A-EV60-UG324S

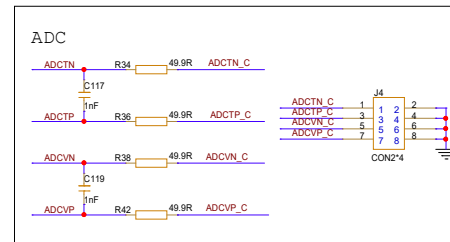
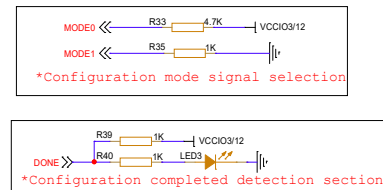
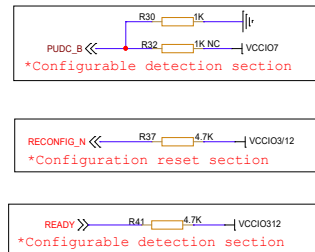
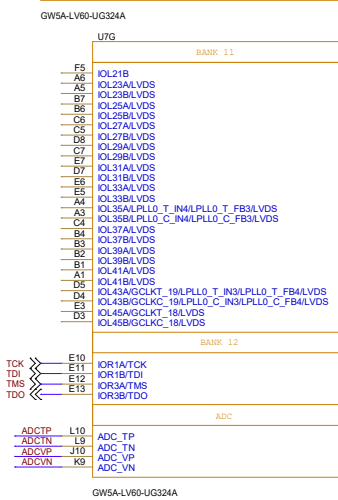
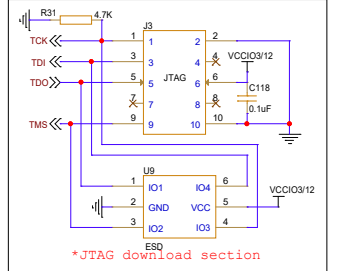
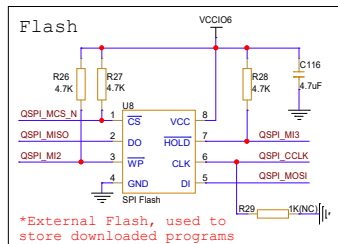


GW5A-EV60-UG3249



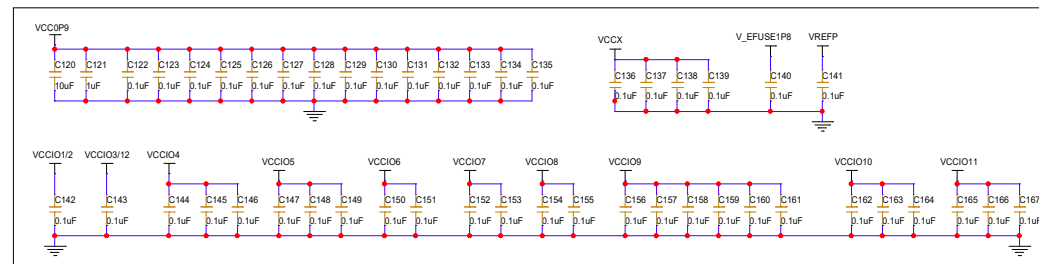
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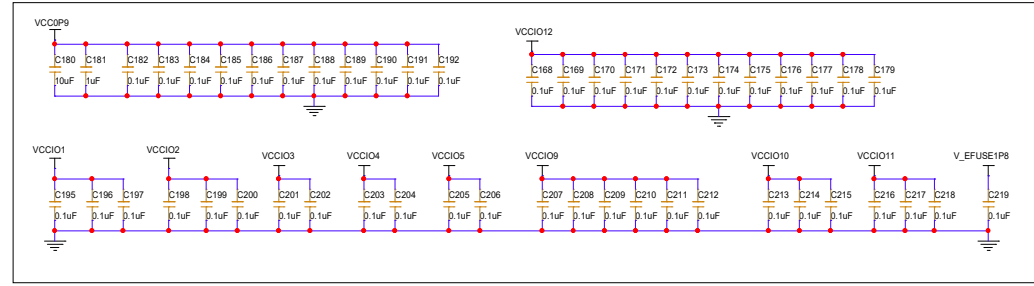
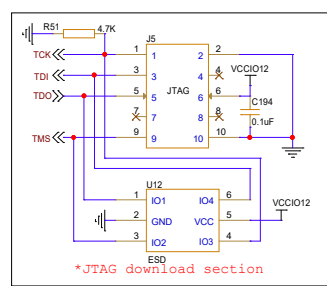
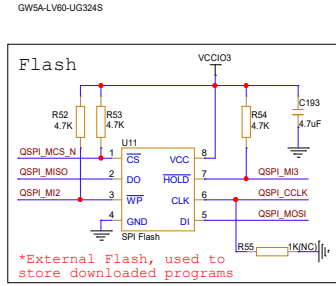
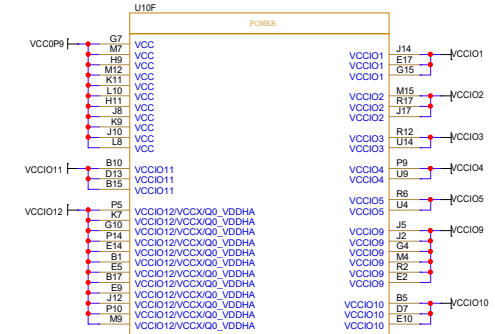
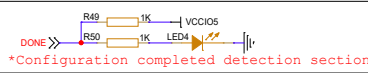
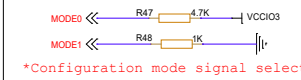
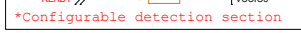
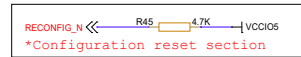
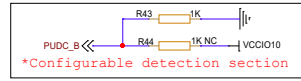
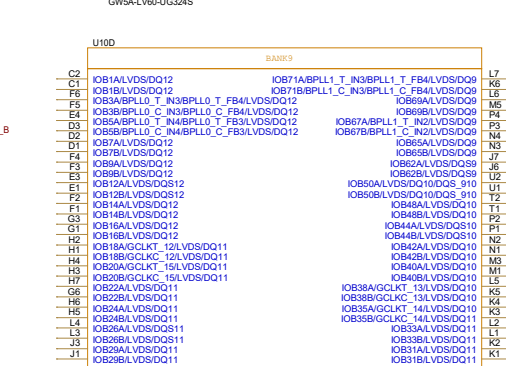
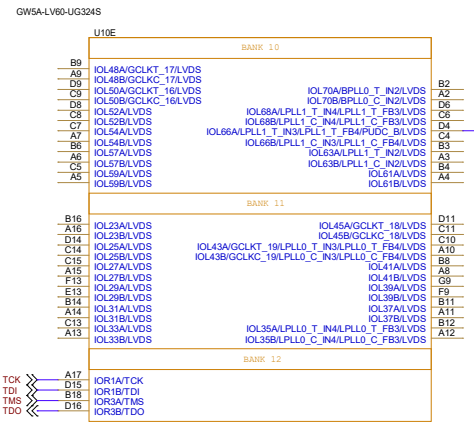
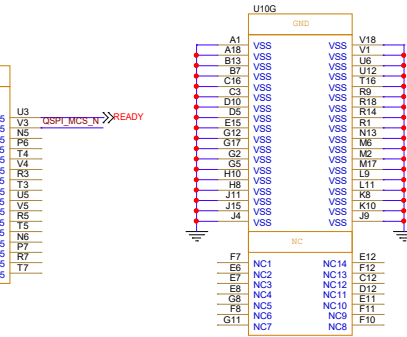
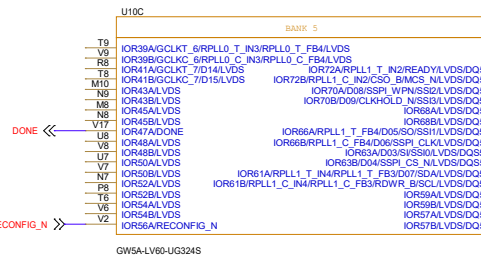
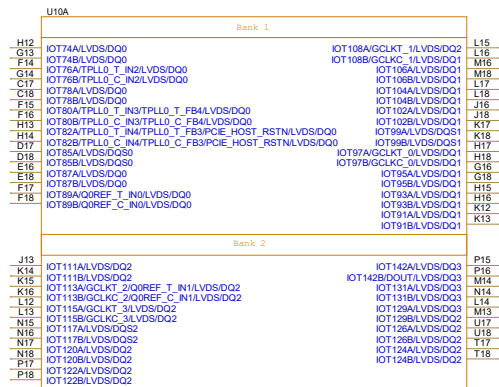


Notes:

1. F\_CLK signal is an external input clock signal.
2. It is recommended that F\_CLK signal be provided through an active oscillator crystal.
3. External Flash memory is used to store downloaded programs.
4. For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG718, Arara V 60K FPGA Products Programming and Configuration Guide.
5. It is recommended that add an ESD protection chip to the JTAG download circuit.
6. VCC core voltage requires a large current, so it is recommended to supply power separately.
7. The MODE pin is the GowinCONFIG configuration mode selection signal.
8. For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG718, Arara V 60K FPGA Products Programming and Configuration Guide.



***GW5A-LV60UG324S***



Notes:

1.F\_CLK signal is an external input clock signal.

It is recommended that F CLK signal be provided through an active oscillator crystal.

2. External Flash memory is used to store downloaded programs.

For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG718,

For details about SPI Flash model selection, see Chapter 4.5 SPI Flash Selection.

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5.The MODE pin is the GowinCONFIG configuration mode selection signal.

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For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG718.

For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG18, Arora V 60K FPGA Products Programming and Configuration Guide.

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