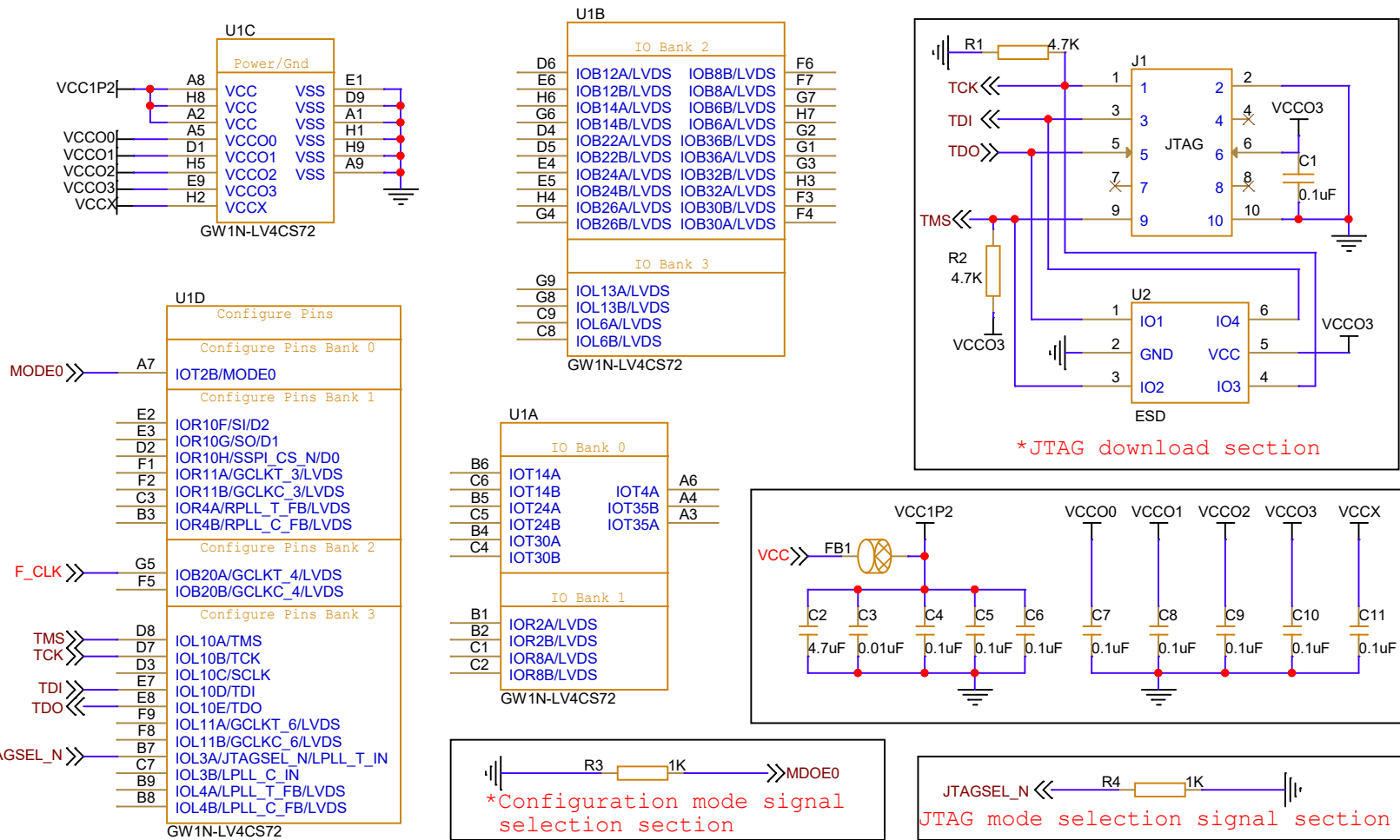


# GW1N-LV4CS72



## Notes:

1.F\_CLK signal is an external input clock signal.

It is recommended that F\_CLK signal be provided through an active oscillator crystal.

2.It is recommended that add an ESD protection chip to the JTAG download circuit.

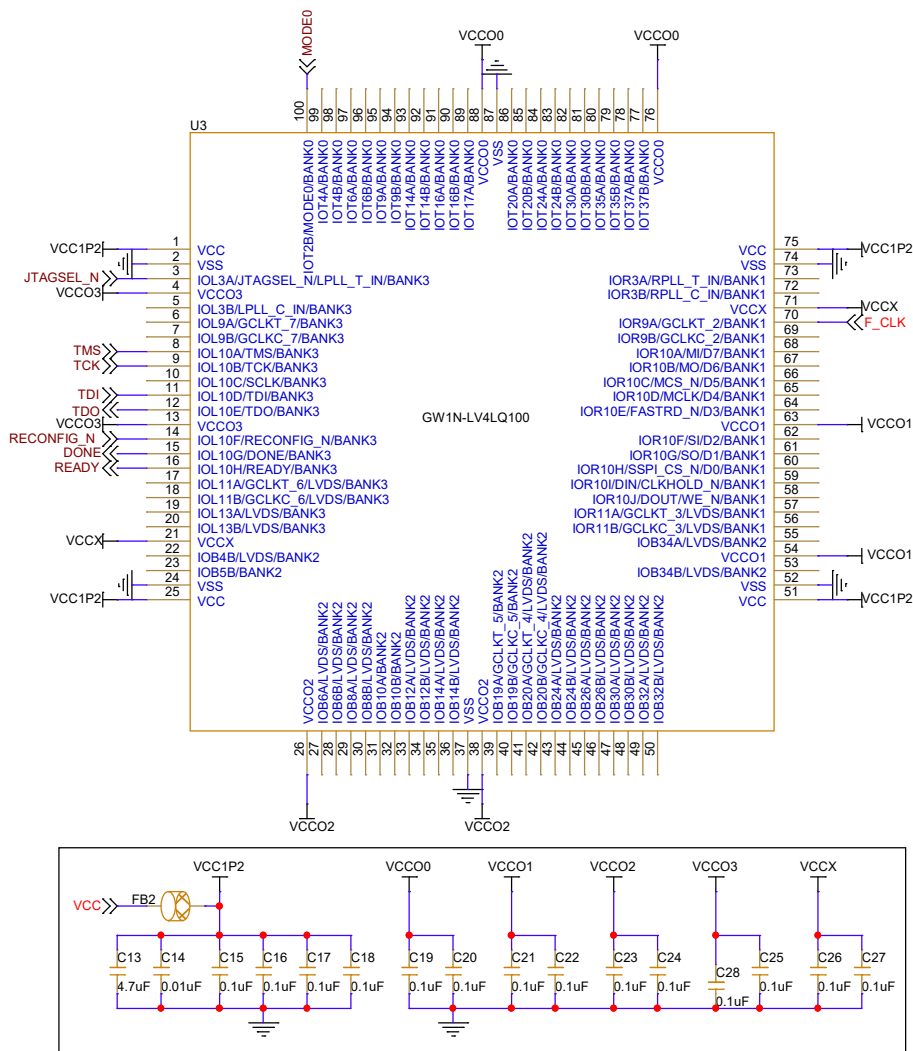
Title  
GOWIN Minimum System Diagram

Size  
A4

Document Number  
GW1N-LV4CS72

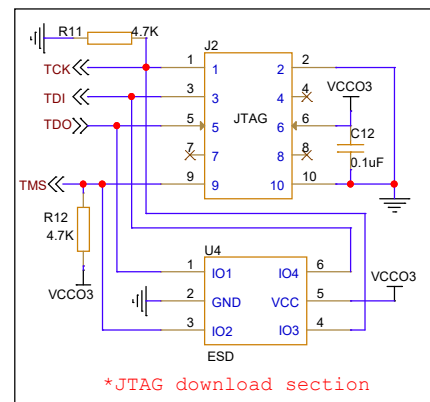
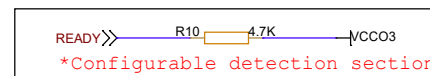
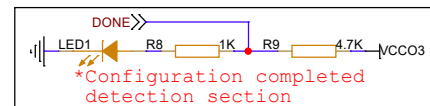
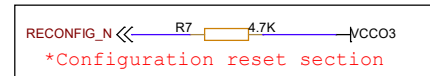
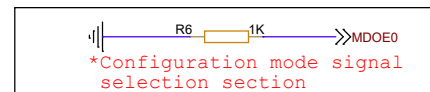
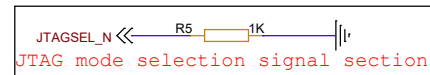
Rev  
2.1.1

Date: Wednesday, September 11, 2024 Sheet 1 of 22

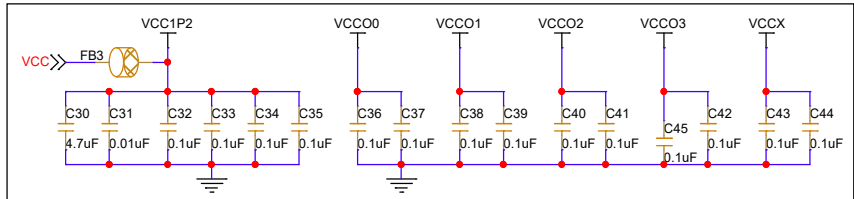
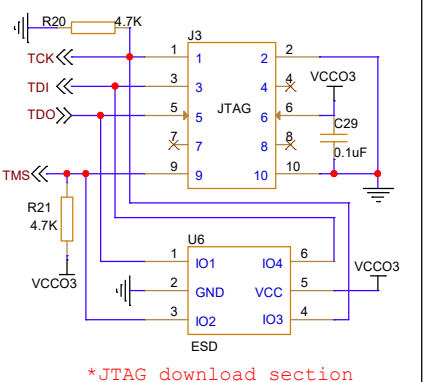
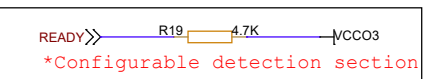
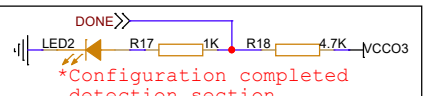
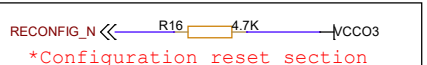
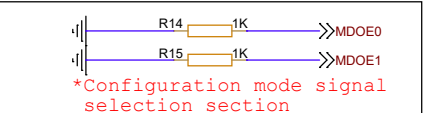
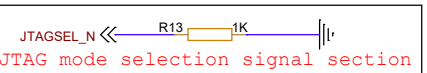
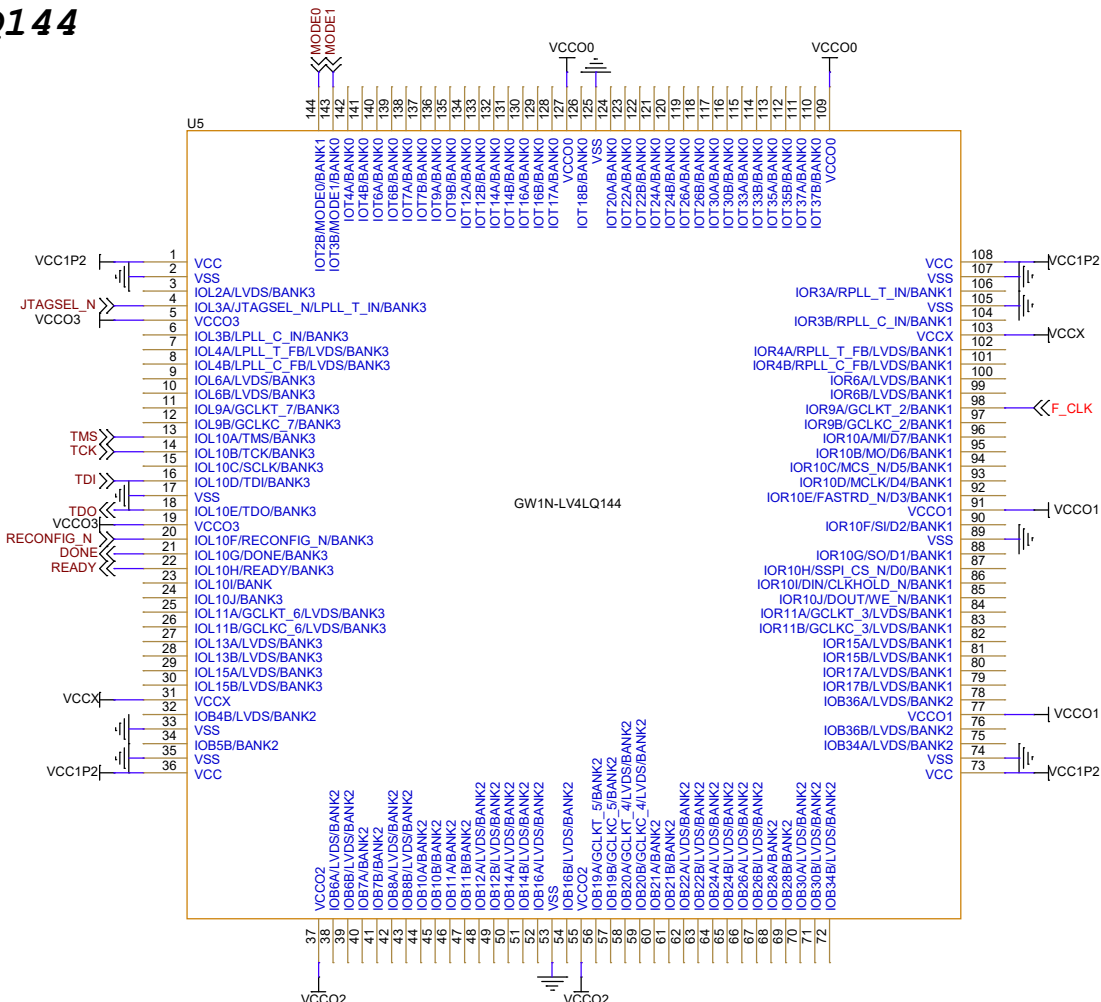


Notes:

- 1.F\_CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.



Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-LV4LQ100	2.1.1
Date:	Wednesday, September 11, 2024	Sheet 2 of 22



Notes:

- 1.F\_CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-LV4LQ144	2.1.1
Date:	Wednesday, September 11, 2024	Sheet 3 of 22

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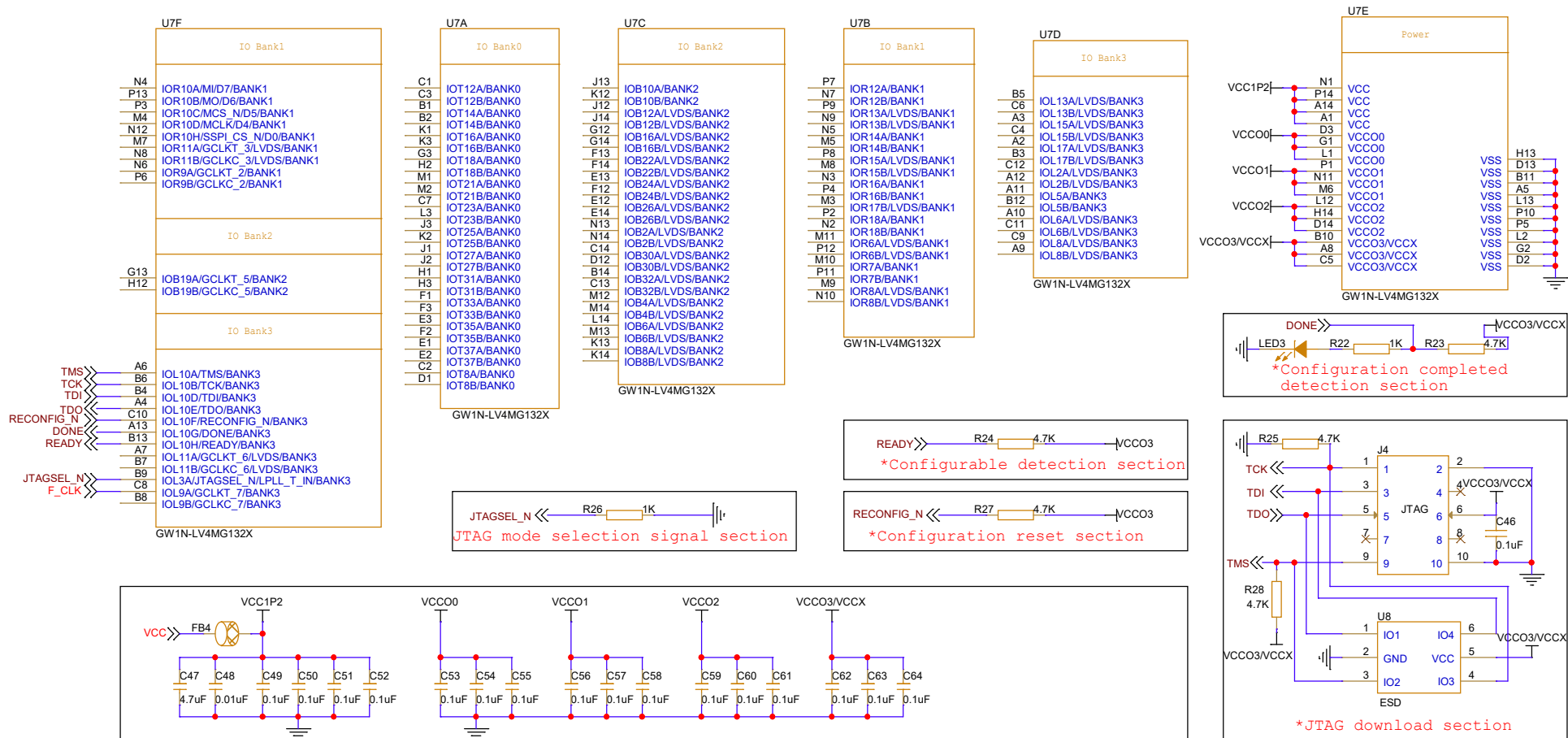
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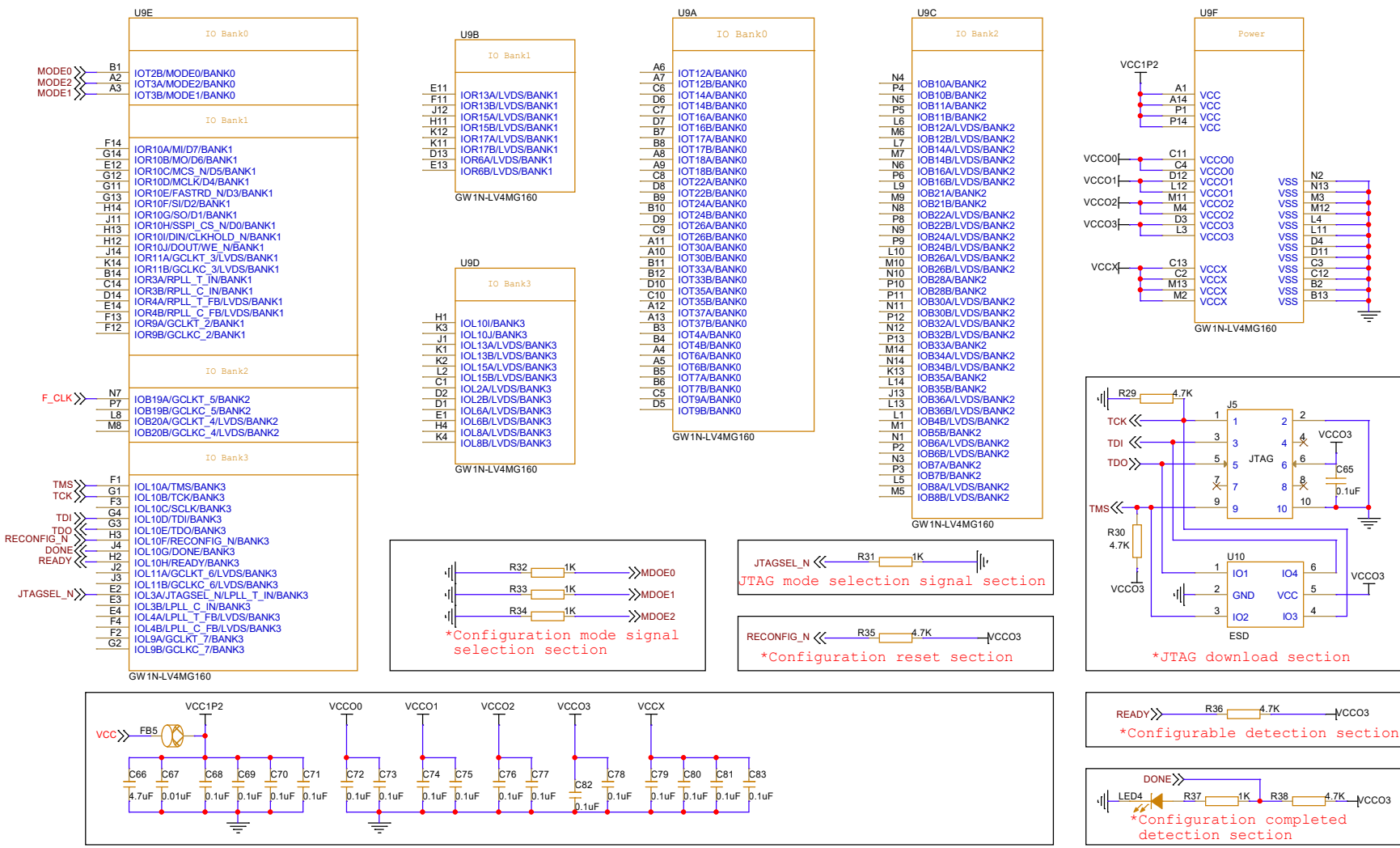
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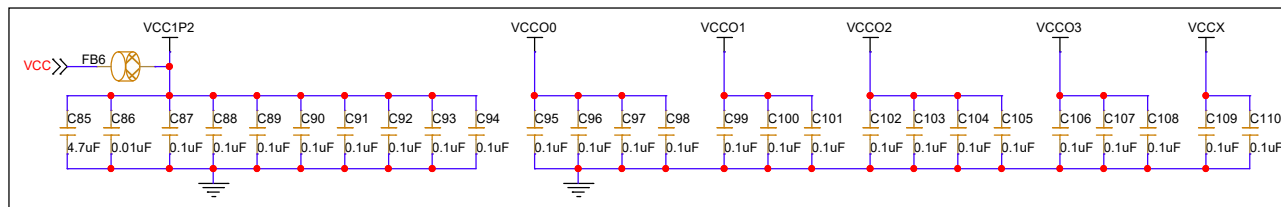
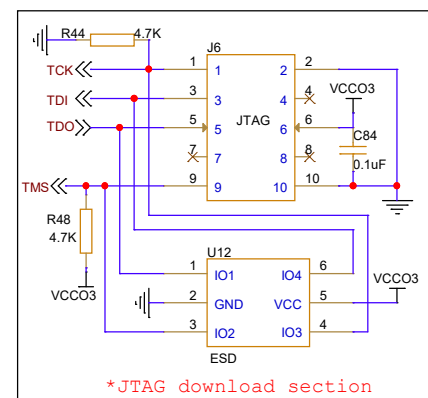
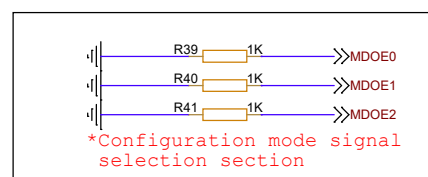
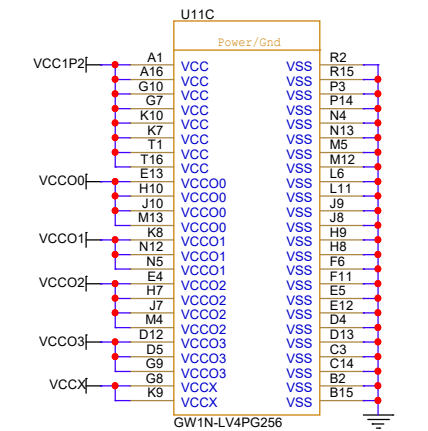
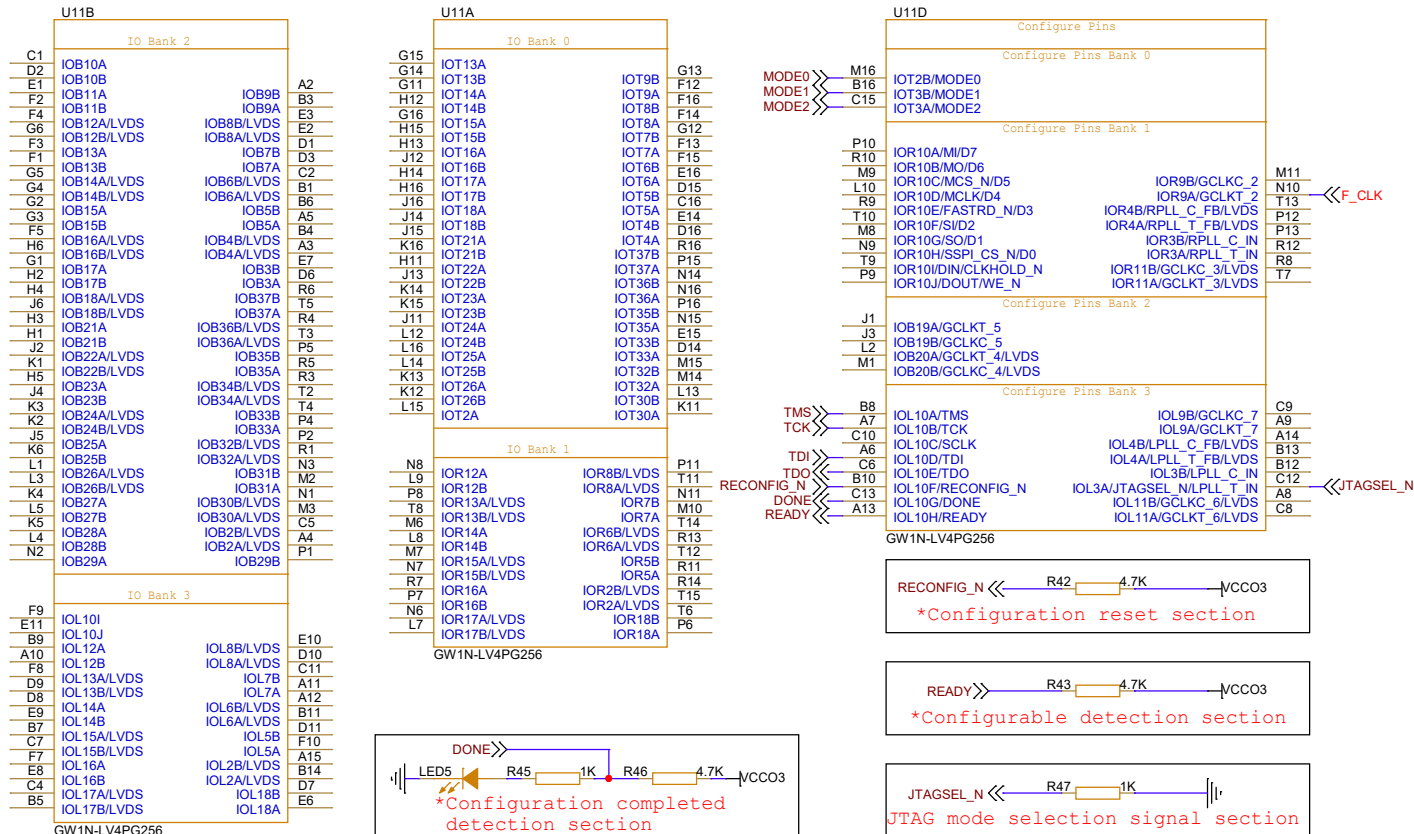
#### Notes:

- 1.F CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
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Size	Document Number	Rev
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Date:	Wednesday, September 11, 2024	Sheet 4 of 22

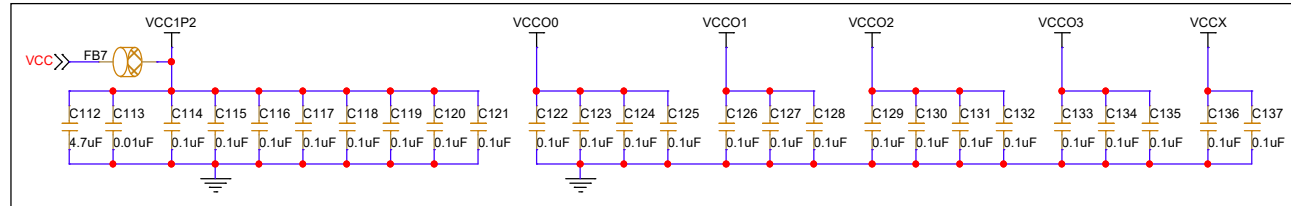
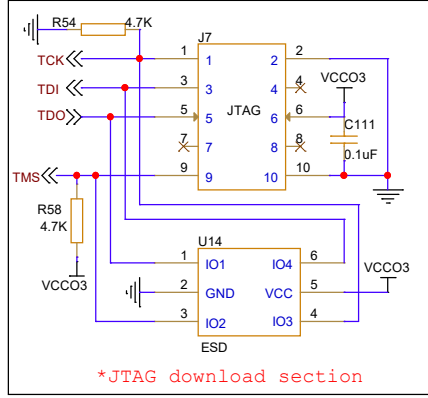
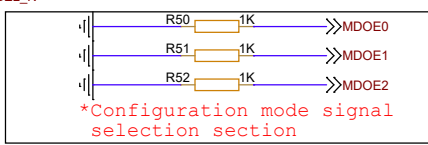
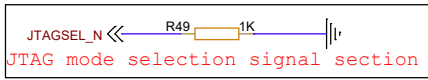
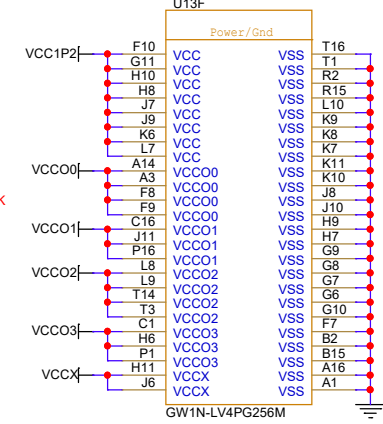
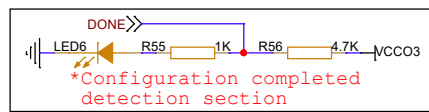
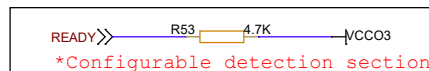
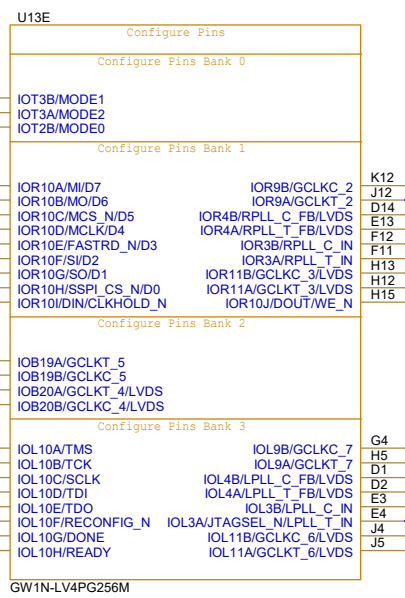
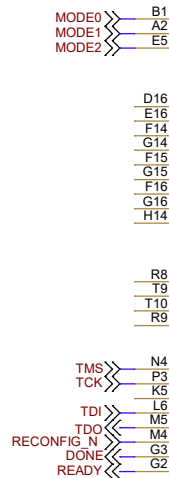
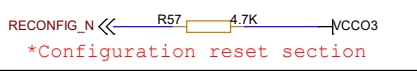
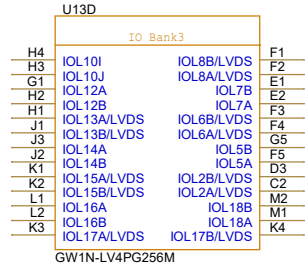
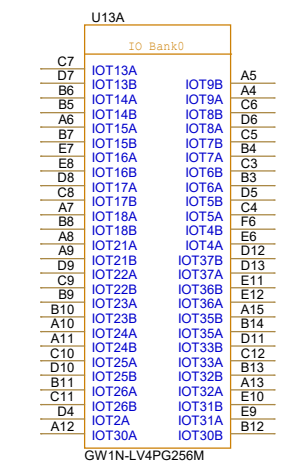
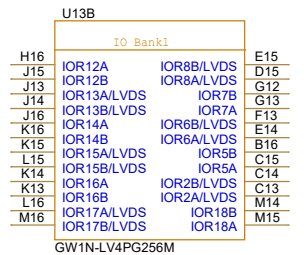
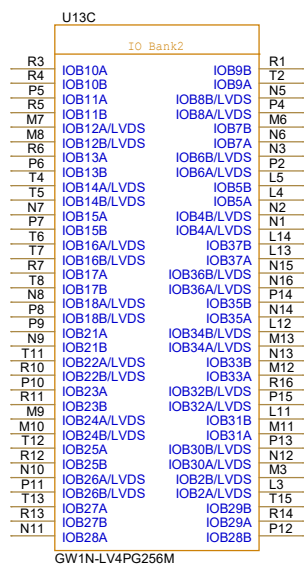


Notes:  
1.F CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.  
2.It is recommended that add an ESD protection chip to the JTAG download circuit.



- Notes:
- 1.F CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
  - 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
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Date:	Wednesday, September 11, 2024	Sheet 6 of 22



Notes:

1.F CLK signal is an external input clock signal.

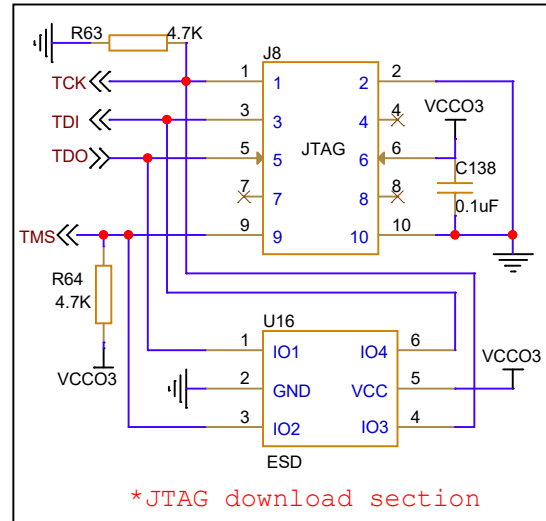
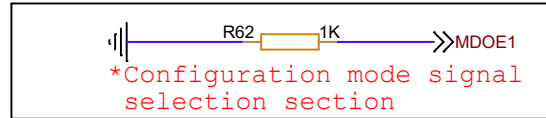
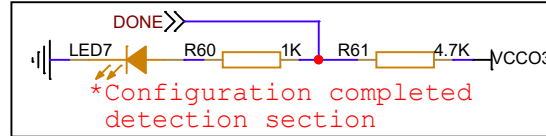
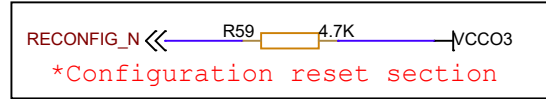
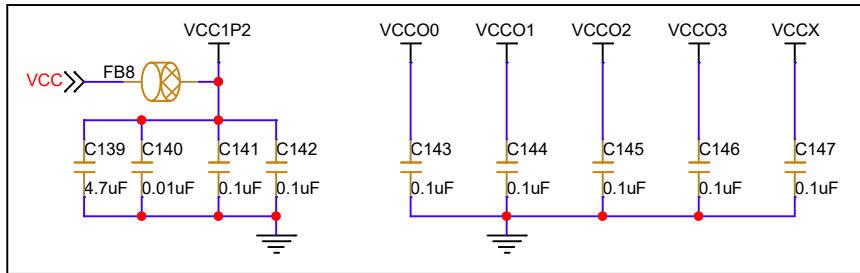
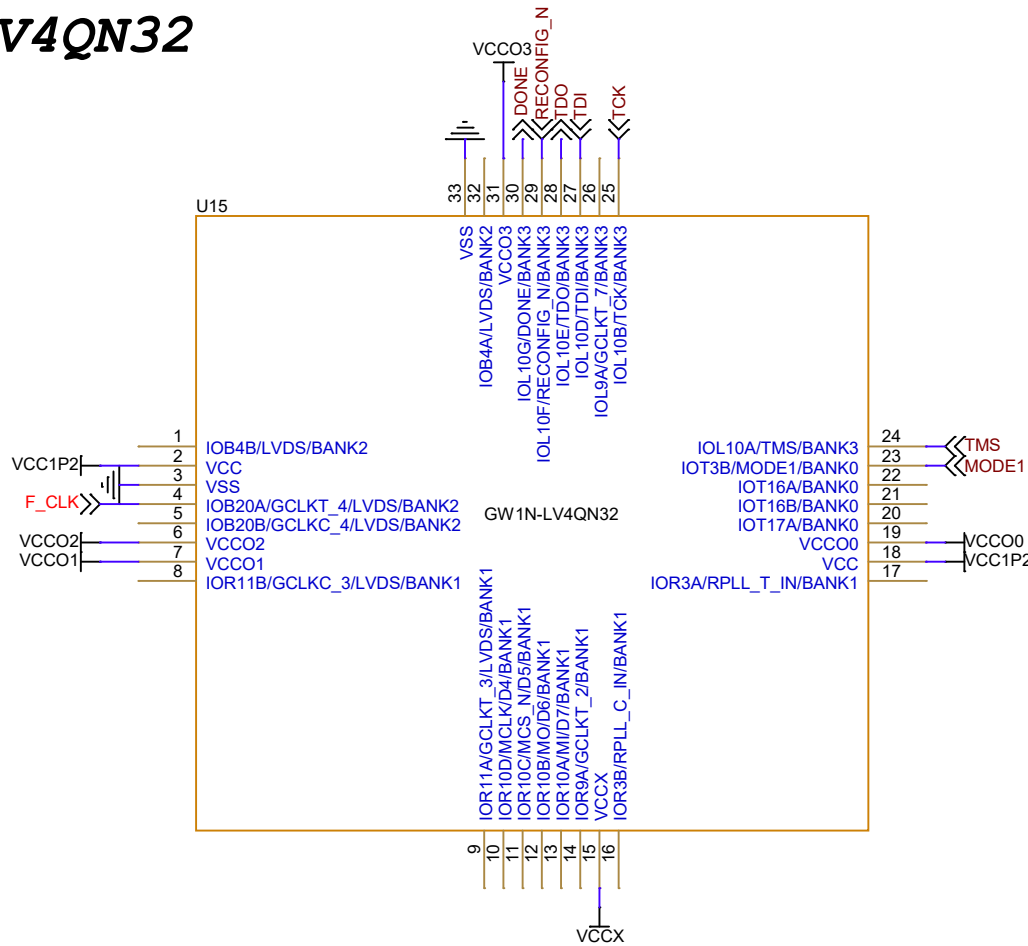
If it is recommended that F\_CLK signal be provided through an active oscillator crystal.

2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
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Date:	Wednesday, September 11, 2024	Sheet 7 of 22



# GW1N-LV4QN32

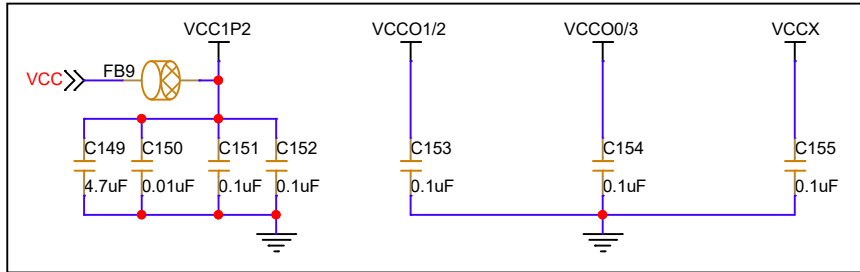
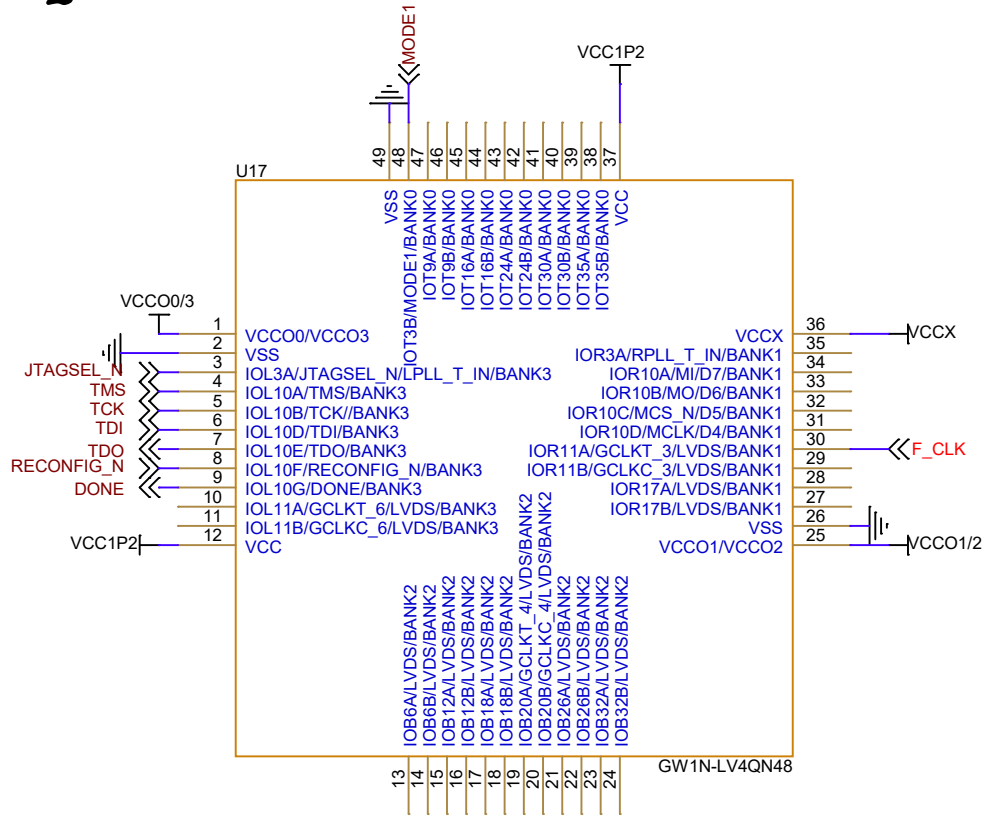


## Notes:

- 1.F\_CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
A4	GW1N-LV4QN32	2.1.1
Date:	Wednesday, September 11, 2024	Sheet 8 of 22



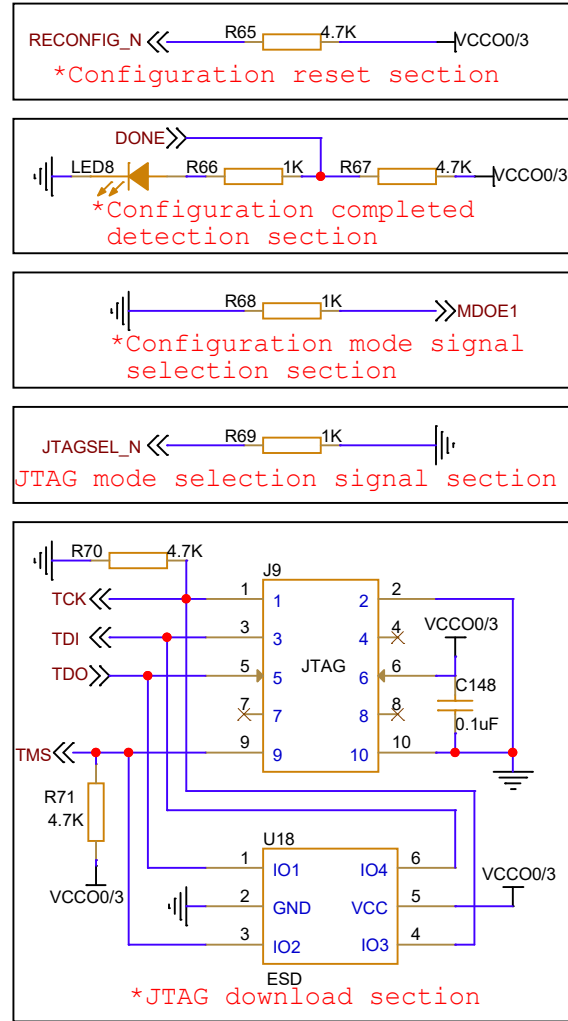


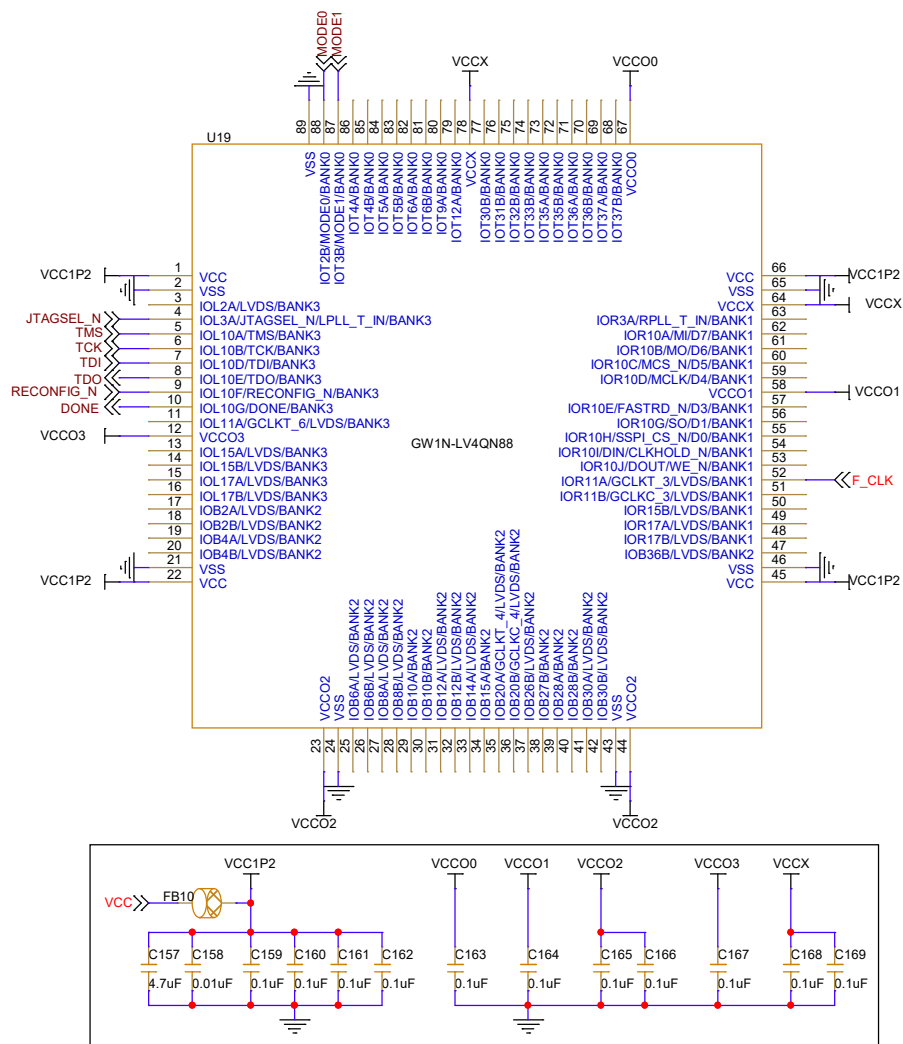
Notes:

1.F\_CLK signal is an external input clock signal.

It is recommended that F\_CLK signal be provided through an active oscillator crystal.

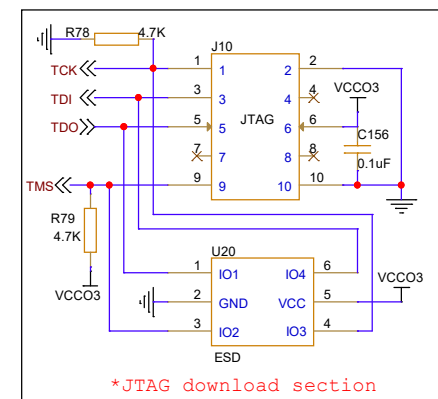
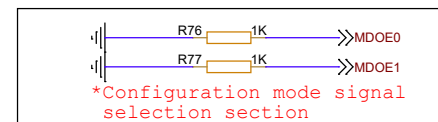
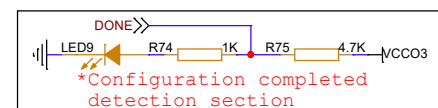
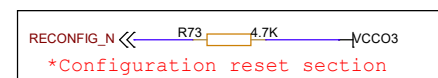
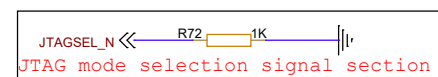
2. It is recommended that add an ESD protection chip to the JTAG download circuit.



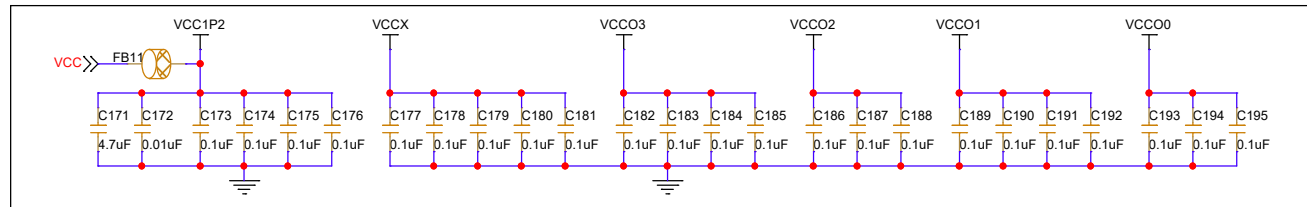
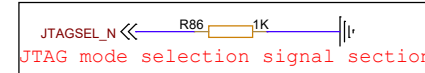
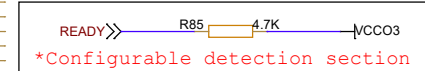
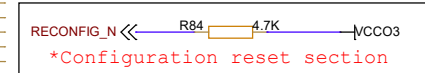
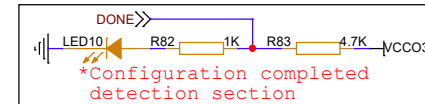
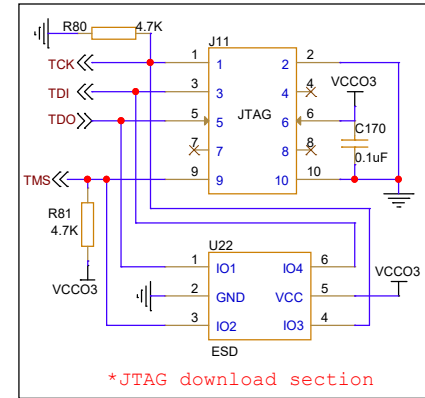
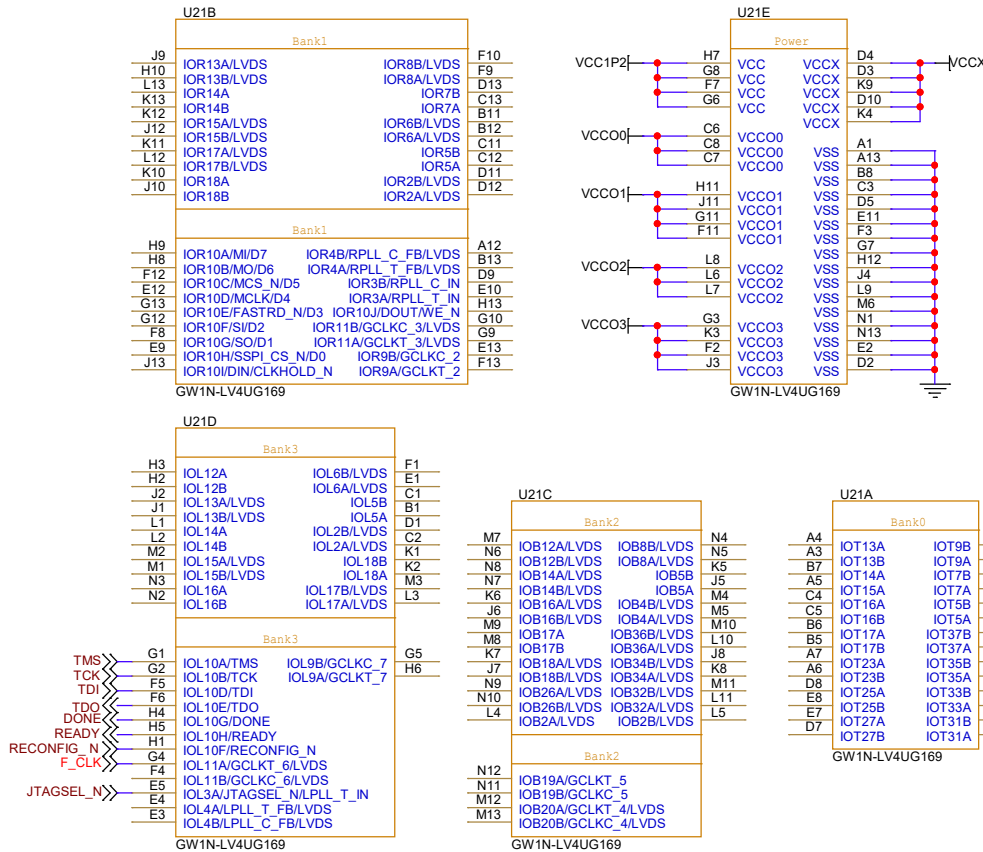


Notes:

- NOTES:
- 1.F CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.
  - 2.It is recommended that add an ESD protection chip to the JTAG download circuit.



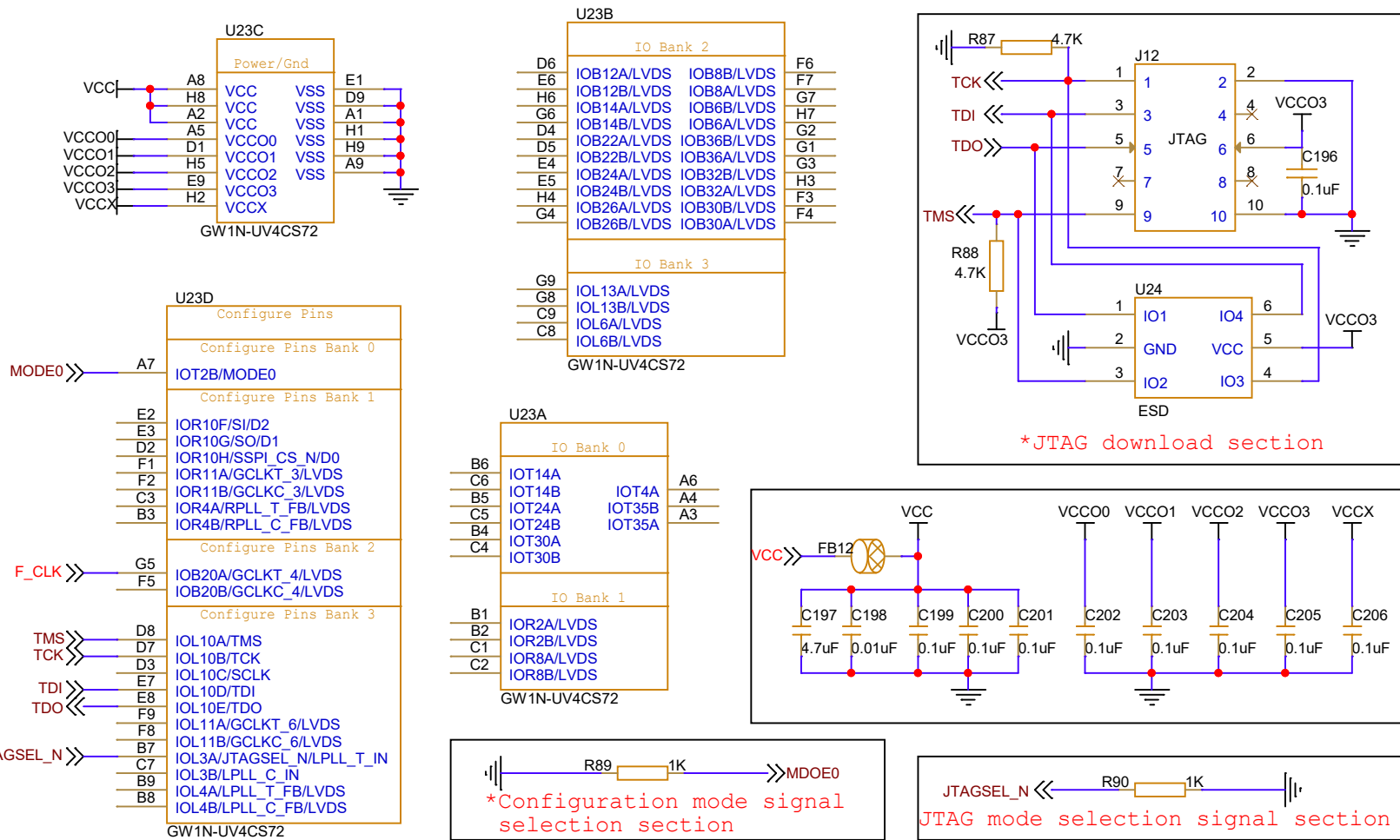
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GOWIN Minimum System Diagram				
Size B	Document Number GW1N-LV4QN88			Rev 2.1.1
Date:	Wednesday, September 11, 2024	Sheet	10 of 22	



Notes:  
 1.F CLK signal is an external input clock signal.  
 It is recommended that F\_CLK signal be provided through an active oscillator crystal.  
 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-LV4UG169	2.1.1
Date:	Wednesday, September 11, 2024	Sheet 11 of 22

# GW1N-UV4CS72



## Notes:

- 1.F CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

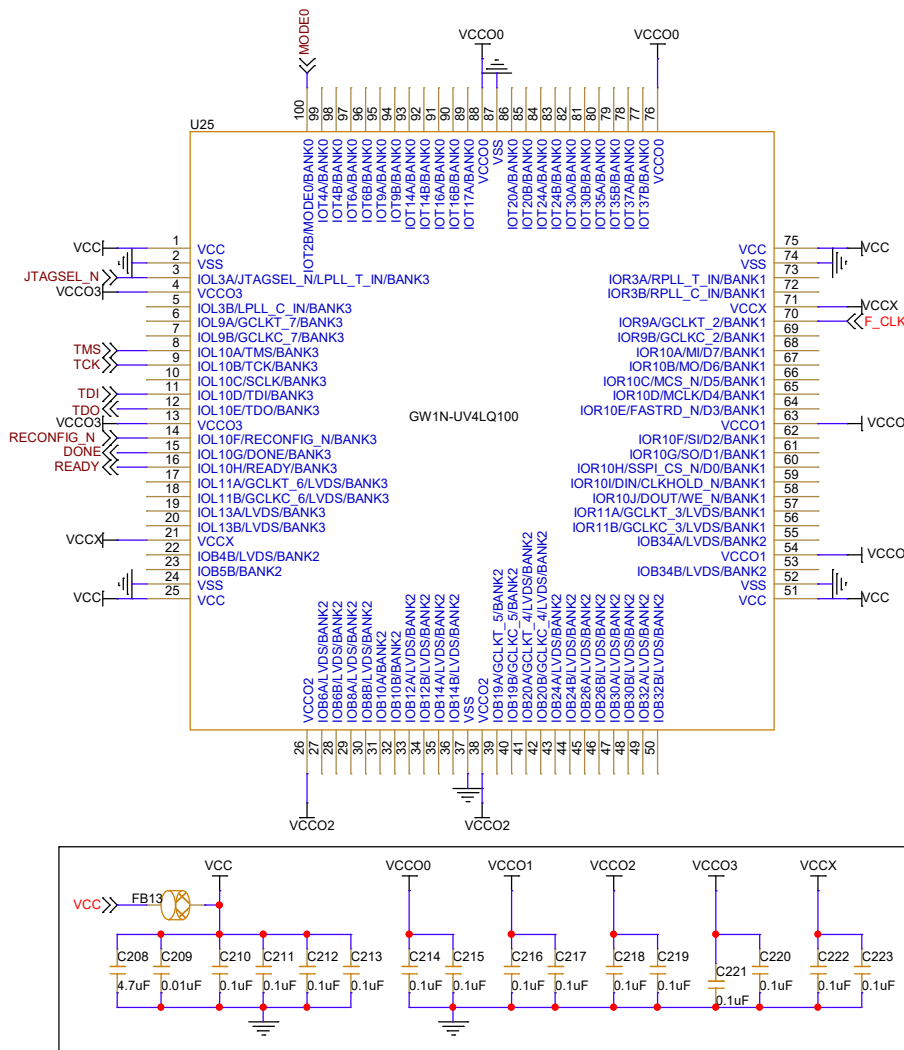
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Document Number  
GW1N-UV4CS72

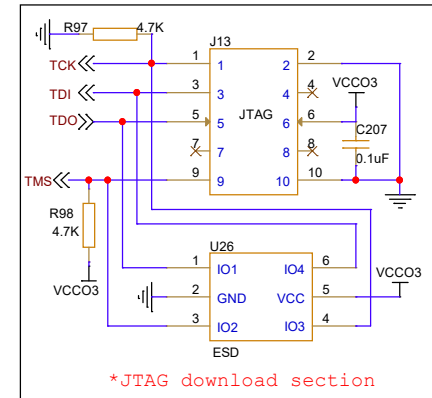
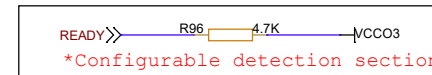
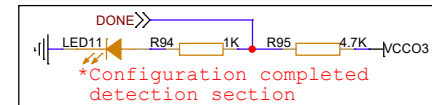
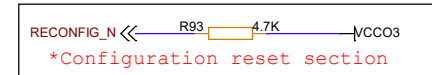
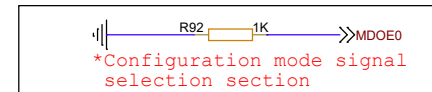
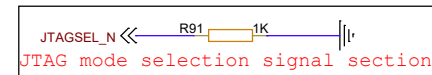
Rev  
2.1.1

Date: Wednesday, September 11, 2024 Sheet 12 of 22

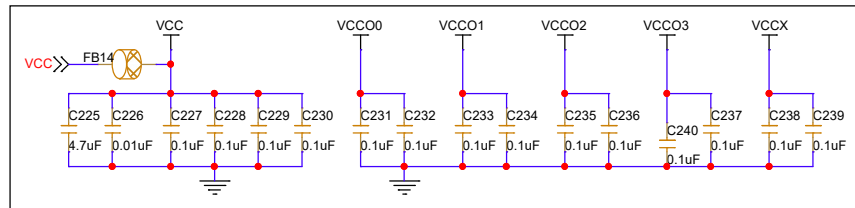
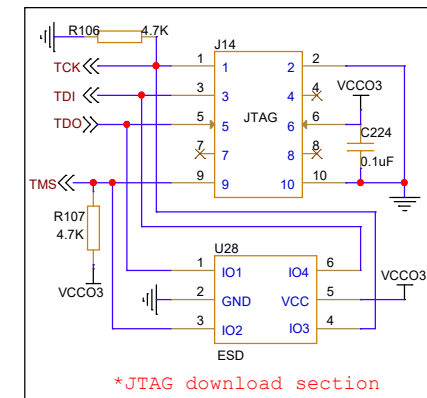
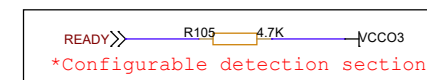
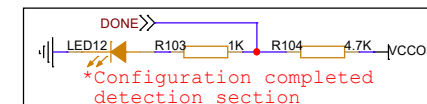
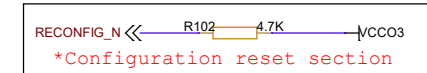
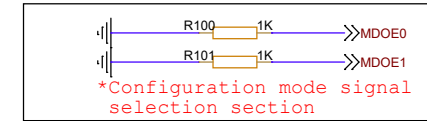
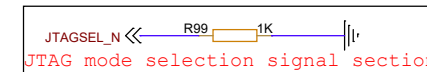
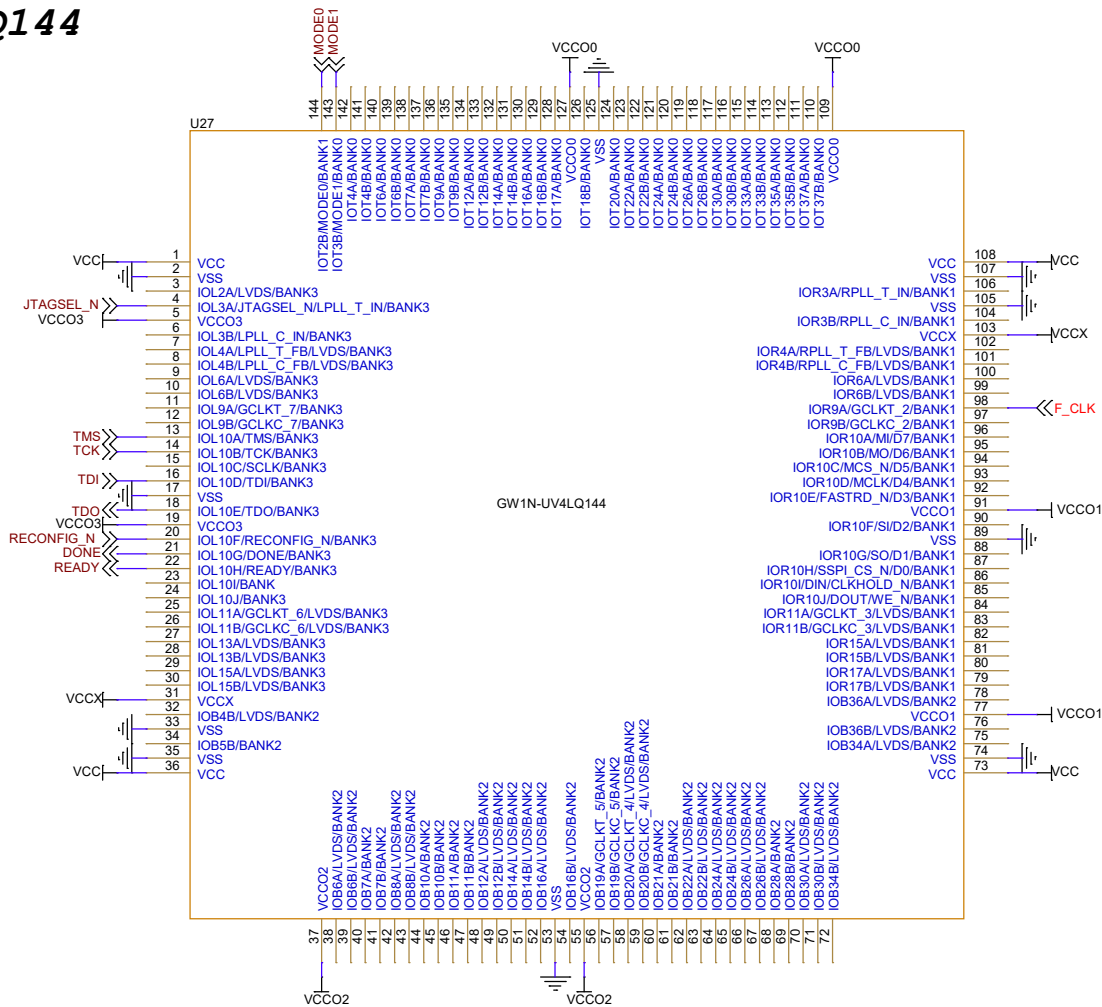


Notes:

- 1.F\_CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

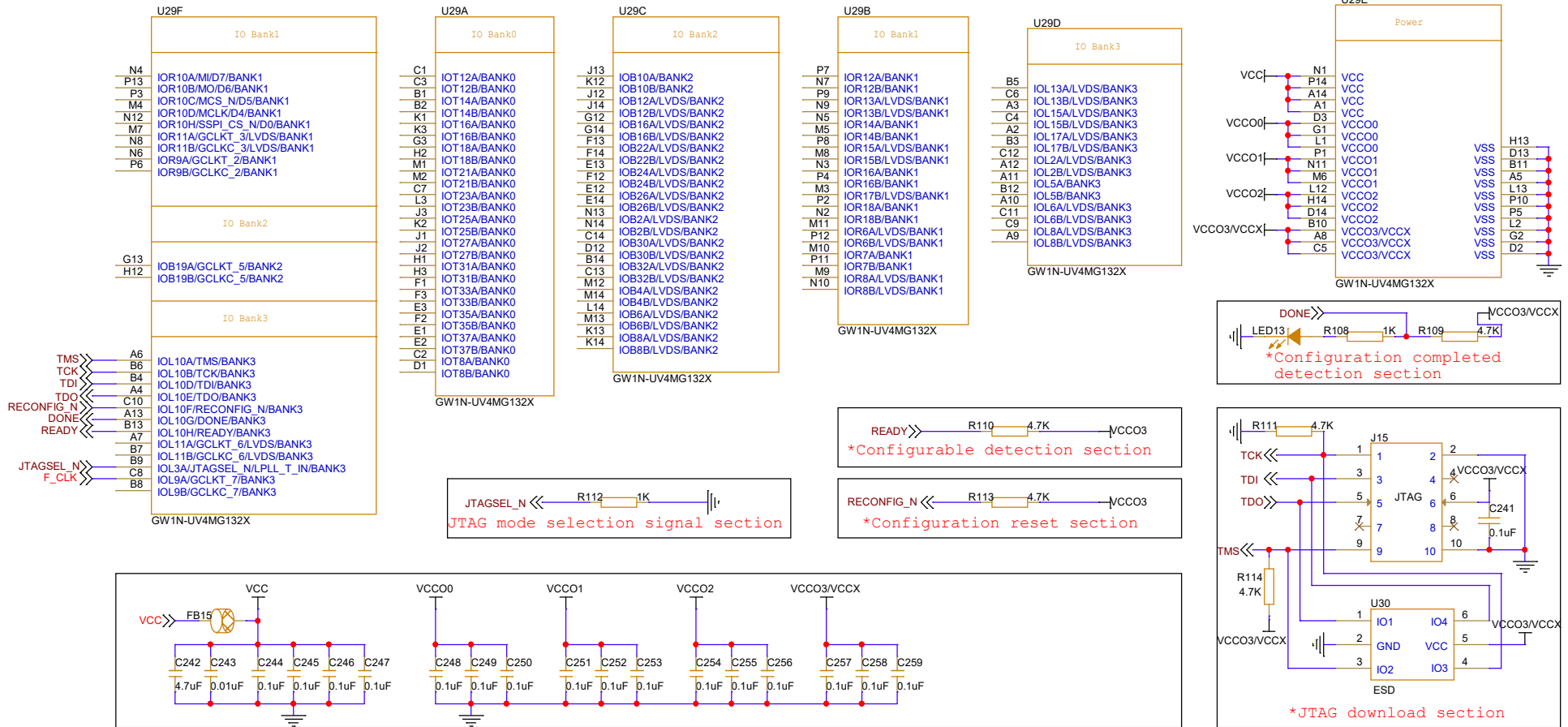


Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-UV4LQ100	2.1.1
Date:	Wednesday, September 11, 2024	Sheet 13 of 22



Notes:  
 1.F CLK signal is an external input clock signal.  
 It is recommended that F CLK signal be provided through an active oscillator crystal.  
 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-UV4LQ144	2.1.1
Date:	Wednesday, September 11, 2024	Sheet 14 of 22



Notes:

- 1.F\_CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title			
GOWIN Minimum System Diagram			
Size	Document Number	Rev	
B	GW1N-UV4MG132X	2.1.1	
Date:	Wednesday, September 11, 2024	Sheet	15 of 22



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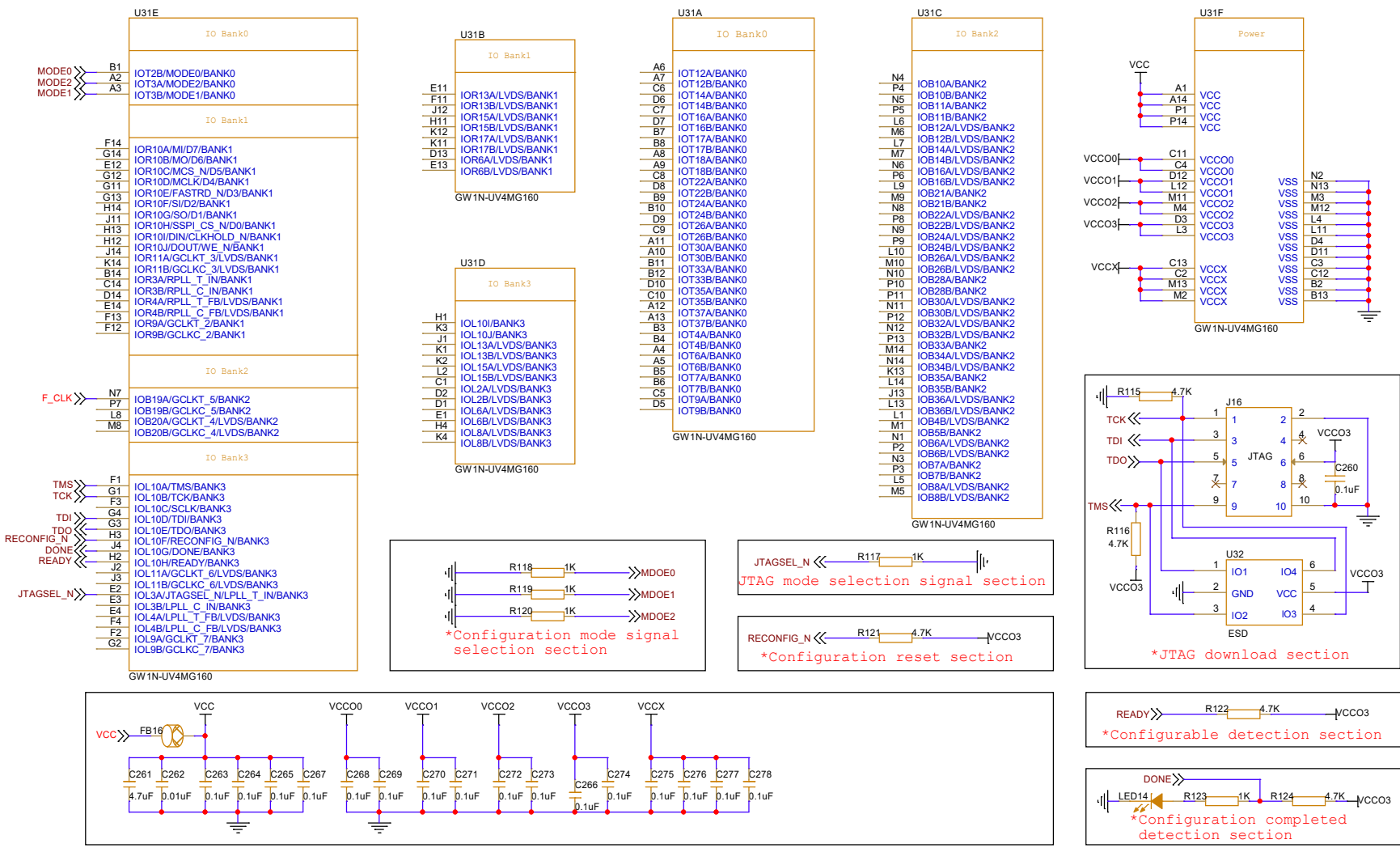
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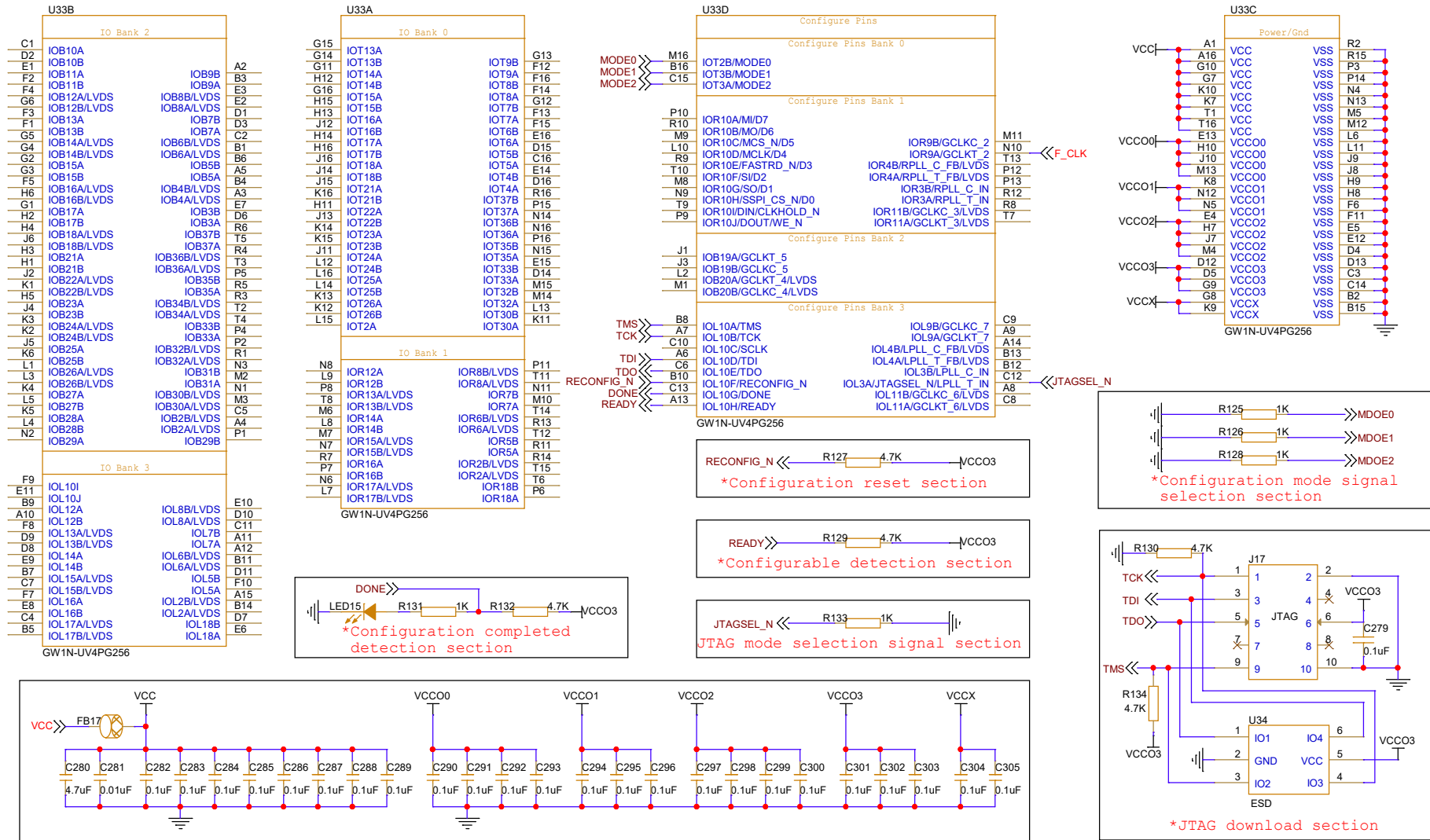
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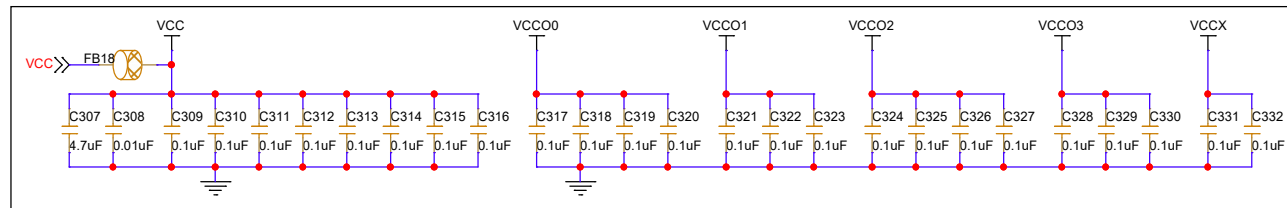
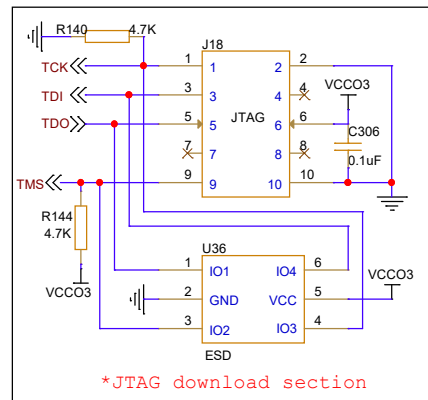
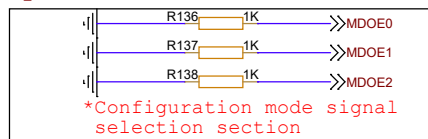
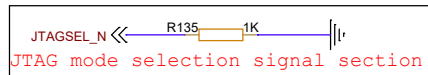
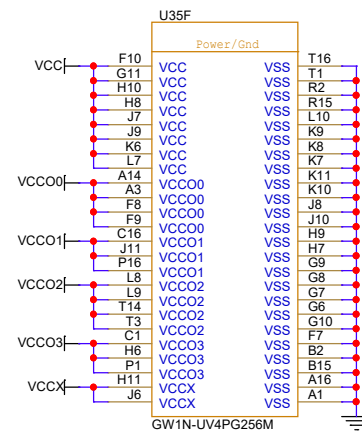
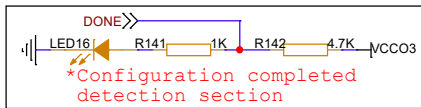
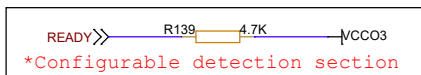
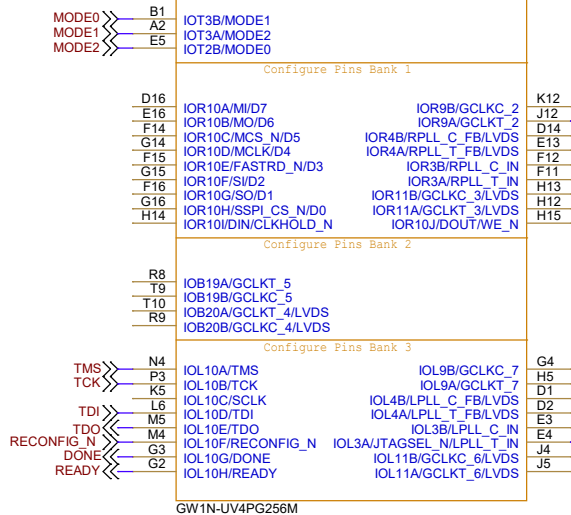
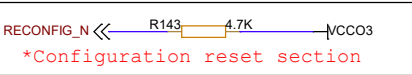
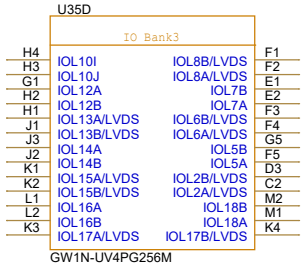
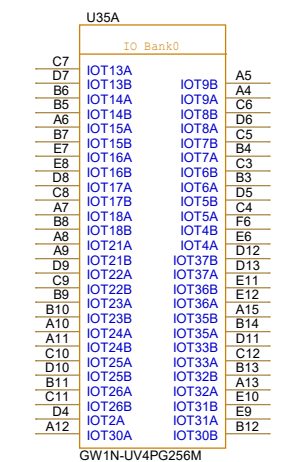
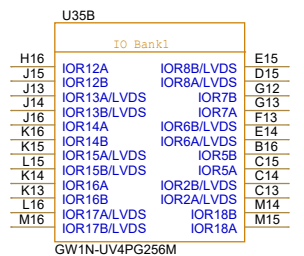
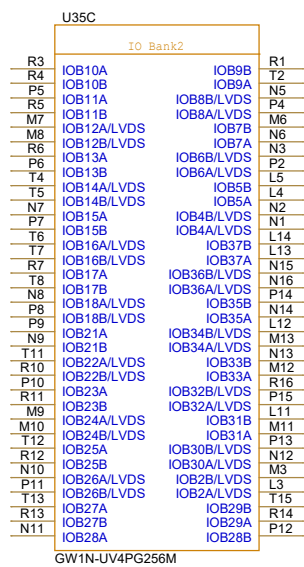
Notes:  
1.F CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.  
2.It is recommended that add an ESD protection chip to the JTAG download circuit.



#### Notes:

- 1.F CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-UV4PG256	2.1.1
Date:	Wednesday, September 11, 2024	Sheet 17 of 22

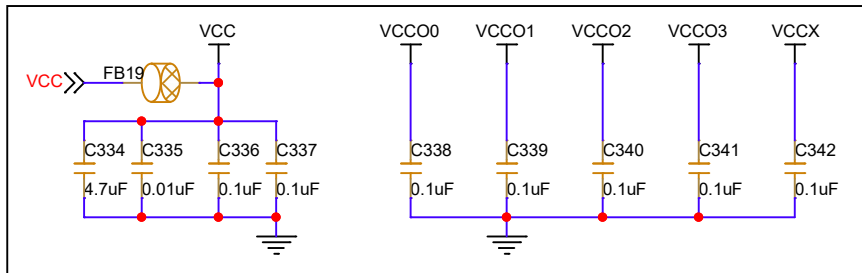
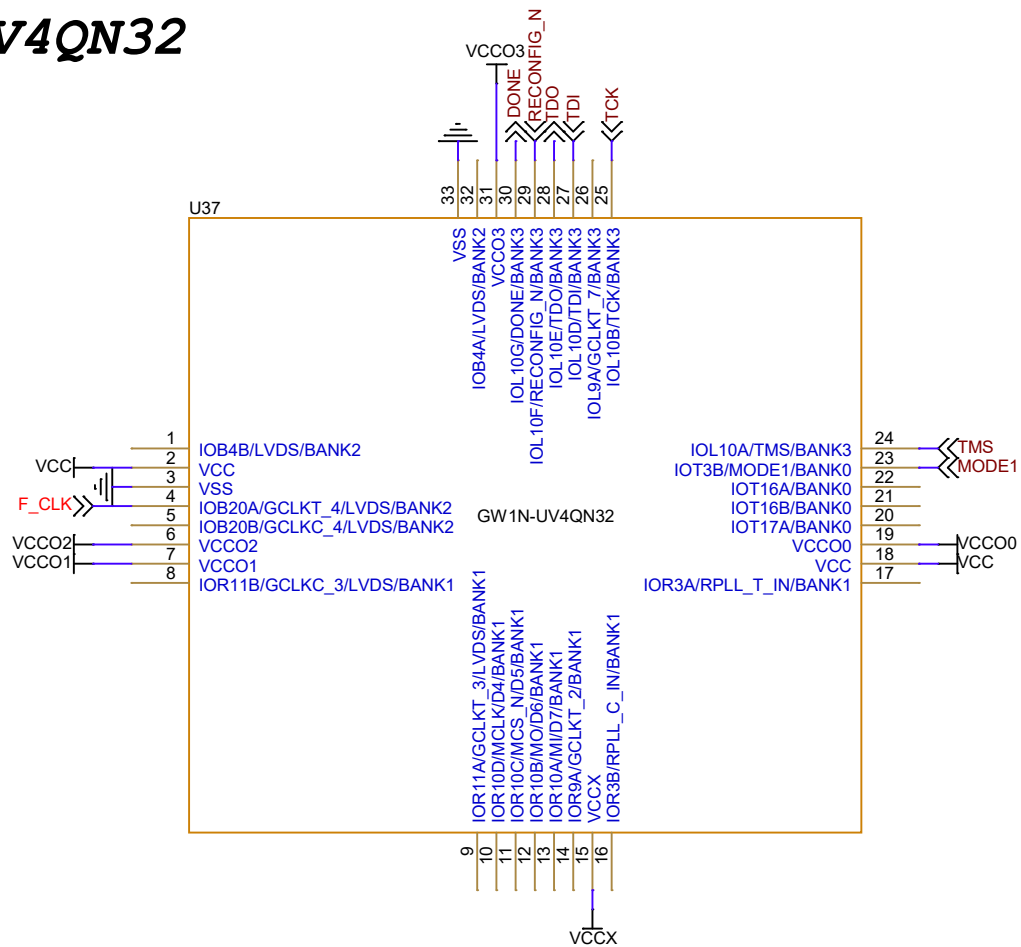


Notes:

- 1.F CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-UV4PG256M	2.1.1
Date:	Wednesday, September 11, 2024	Sheet 18 of 22

# GW1N-UV4QN32



## Notes:

1.F CLK signal is an external input clock signal.

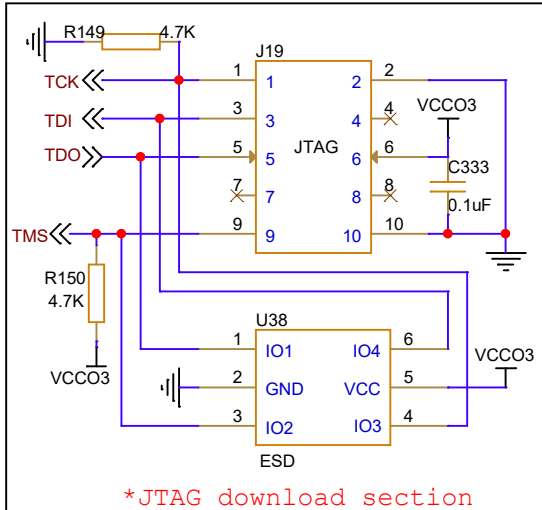
It is recommended that F CLK signal be provided through an active oscillator crystal.

2.It is recommended that add an ESD protection chip to the JTAG download circuit.

RECONFIG\_N << R145 4.7K VCCO3  
\*Configuration reset section

DONE >> LED17 R146 1K R147 4.7K VCCO3  
\*Configuration completed detection section

R148 1K >> MDOE1  
\*Configuration mode signal selection section



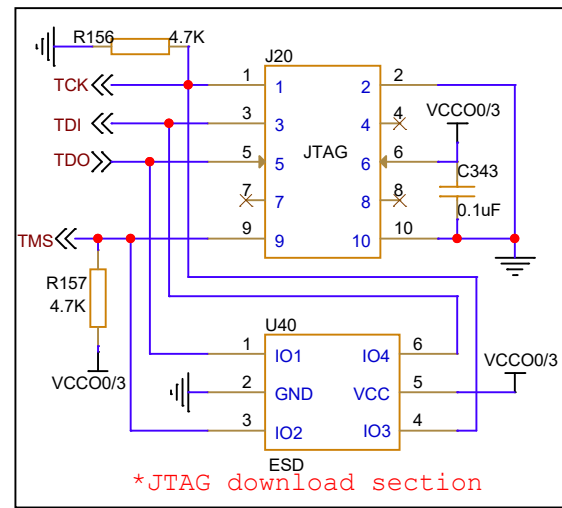
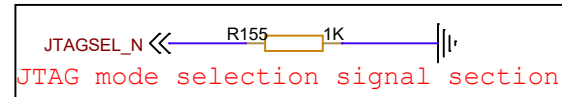
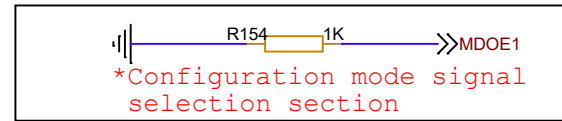
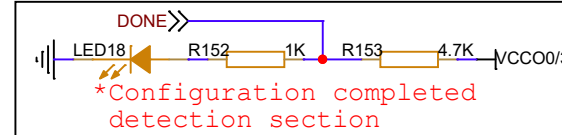
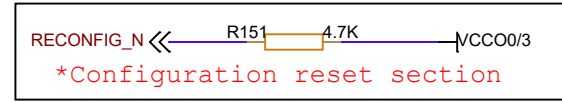
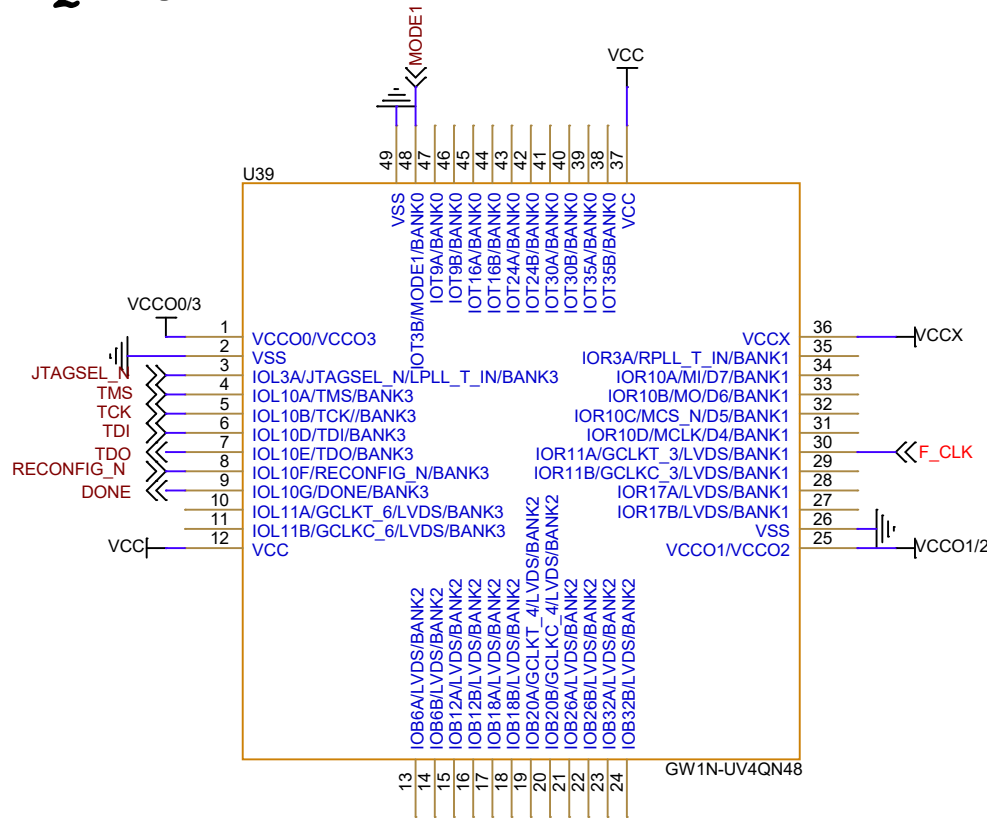
Title  
GOWIN Minimum System Diagram

Size A4  
Document Number  
GW1N-UV4QN32

Rev  
2.1.1

Date: Wednesday, September 11, 2024 Sheet 19 of 22

# GW1N-UV4QN48



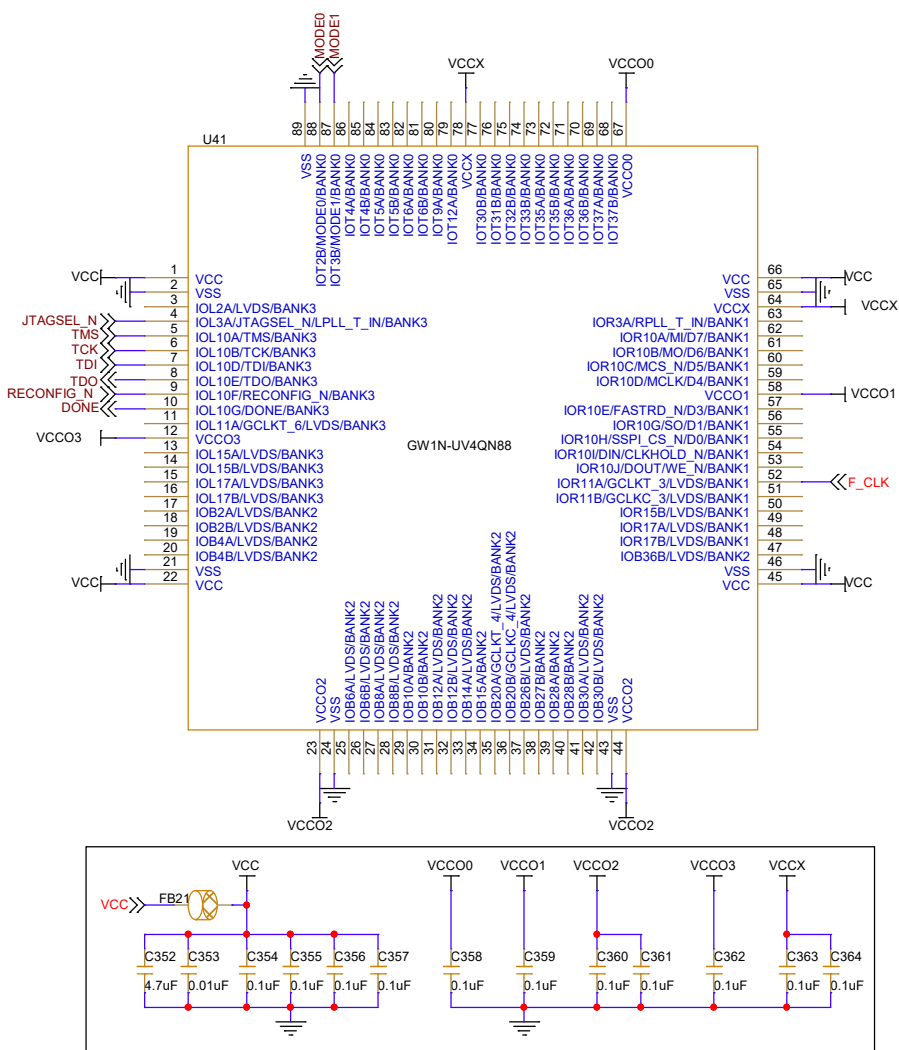
Notes:

1.F\_CLK signal is an external input clock signal.

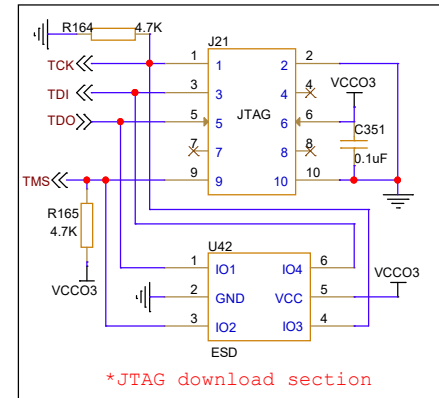
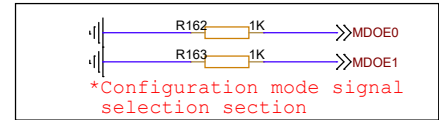
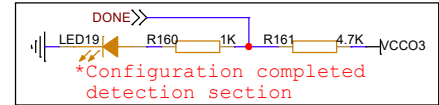
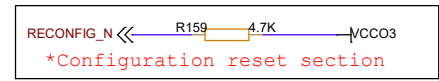
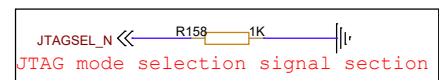
It is recommended that F\_CLK signal be provided through an active oscillator crystal.

2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
A4	GW1N-UV4QN48	2.1.1
Date:	Wednesday, September 11, 2024	Sheet 20 of 22



Notes:  
1.F CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.  
2.It is recommended that add an ESD protection chip to the JTAG download circuit.



Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-UV4QN88	2.1.1
Date:	Wednesday, September 11, 2024	Sheet 21 of 22

