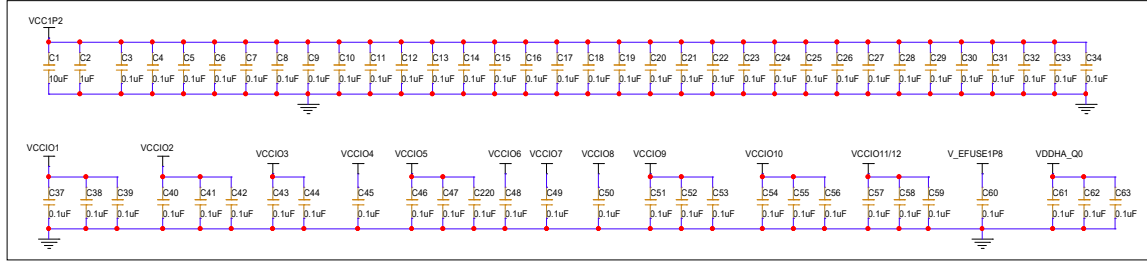
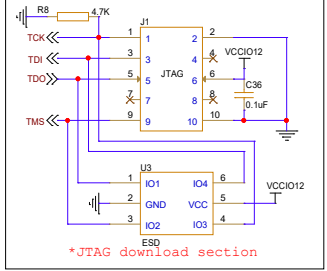
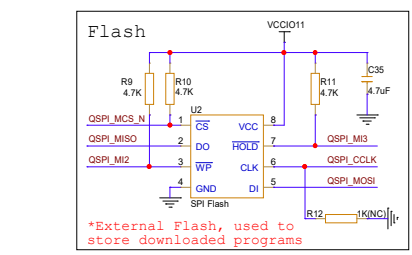
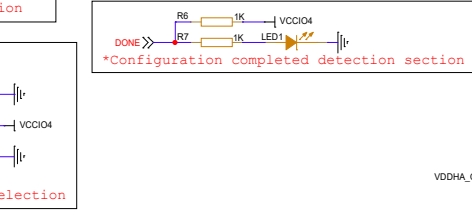
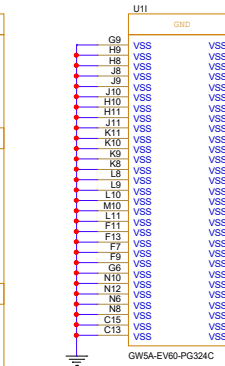
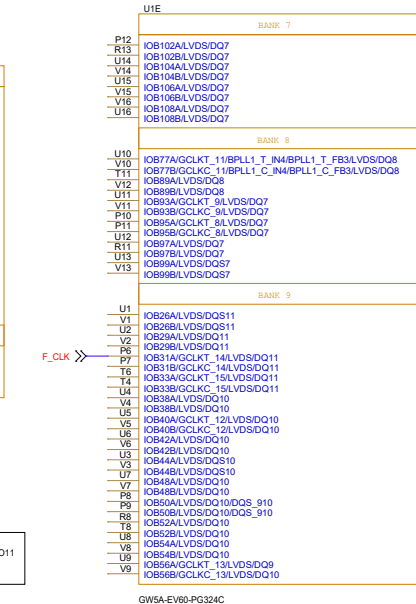
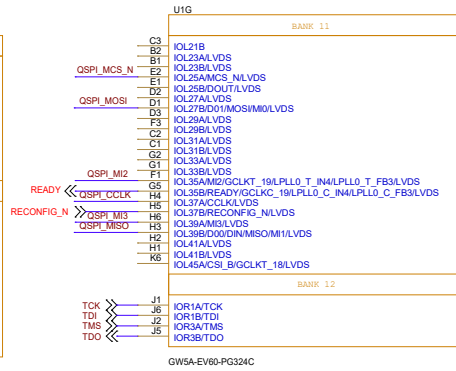
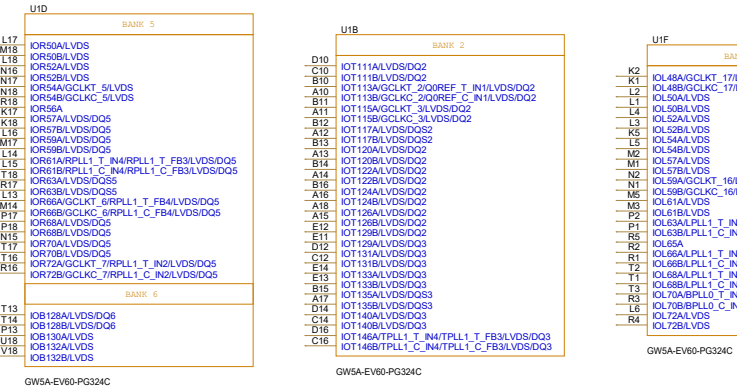
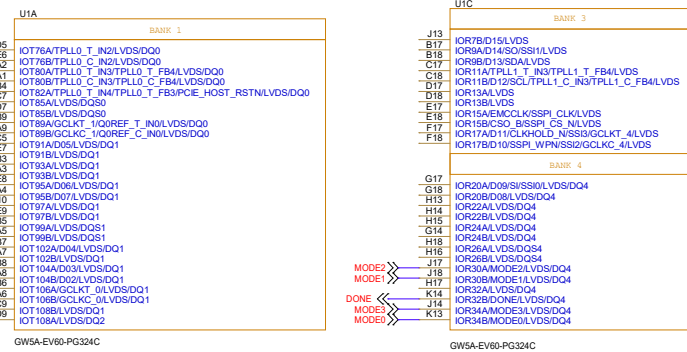


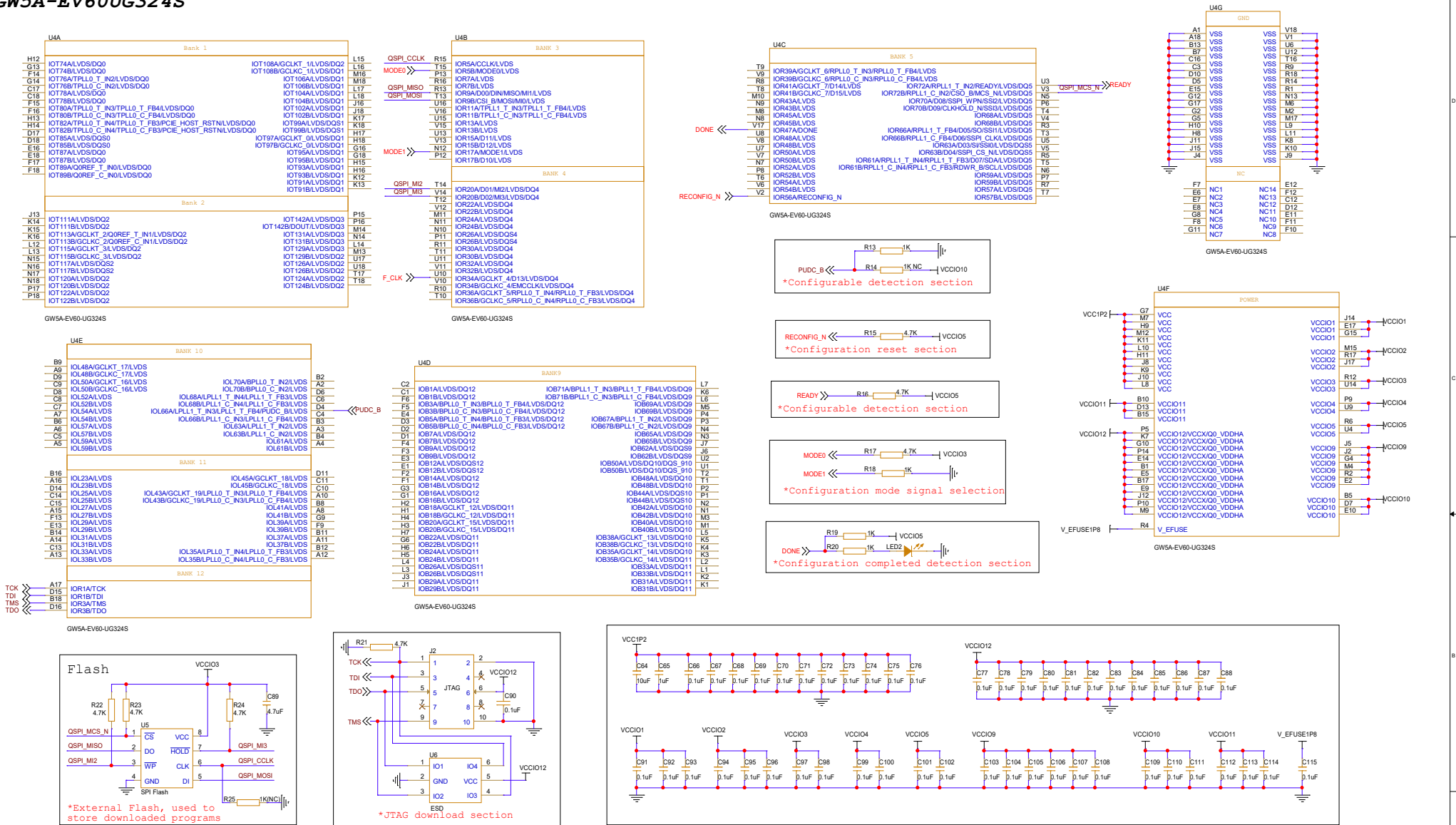
GW5A-EV60PG324C



- Notes:
- 1.F_CLK signal is an external input clock signal.
 - It is recommended that F_CLK signal be provided through an active oscillator crystal.
 - External Flash memory is used to store downloaded programs.
 - For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide.
 - It is recommended that add an ESD protection chip to the JTAG download circuit.
 - VCC core voltage requires a large current, so it is recommended to supply power separately.
 - The MODE pin is the GowinCONFIG configuration mode selection signal.
 - For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide.
 - This package does not support the use of internal differential termination resistors.

Title		
GOWIN Minimum System Diagram		
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Notes:

1.F_CLK signal is an external input clock signal.

It is recommended that F_CLK signal be provided through an active oscillator crystal.

2.External Flash memory is used to store downloaded programs.

For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG718,

Arora V 60K FPGA Products Programming and Configuration Guide .

3.It is recommended that add an ESD protection chip to the JTAG download circuit.

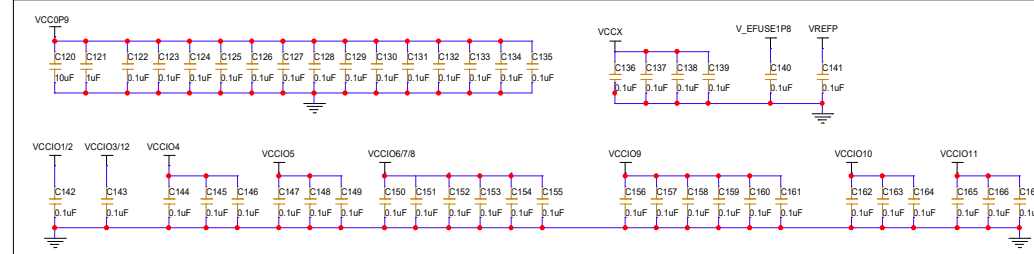
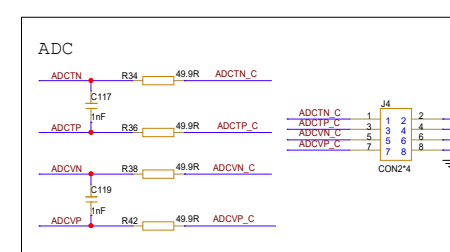
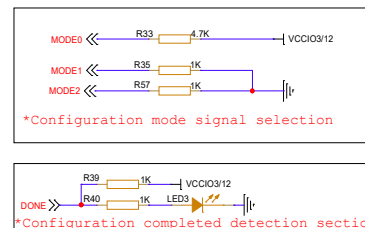
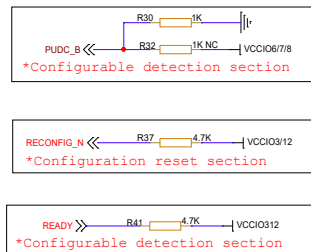
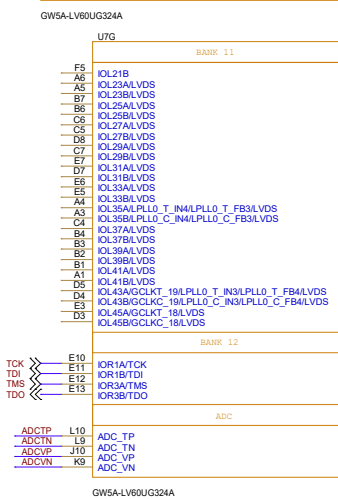
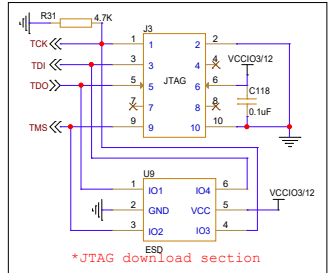
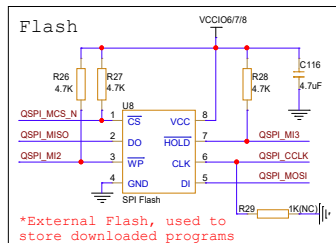
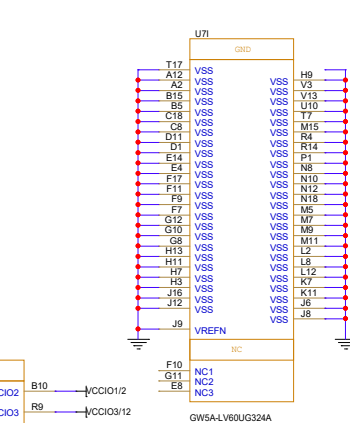
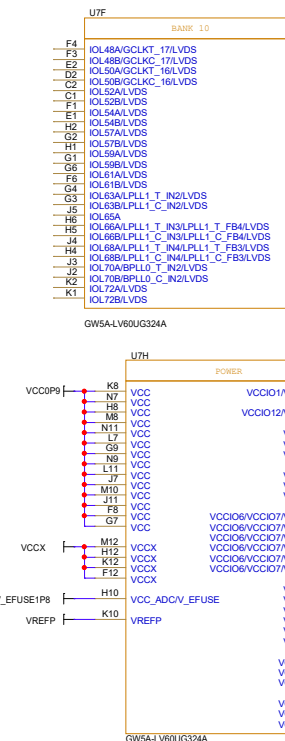
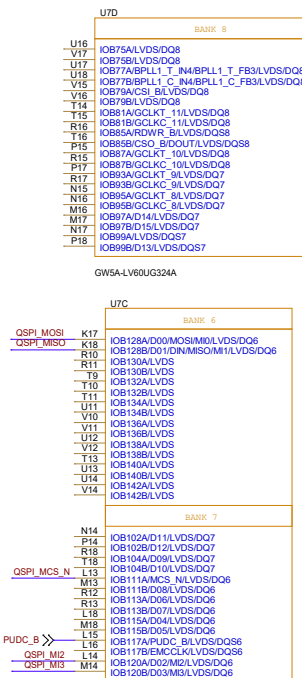
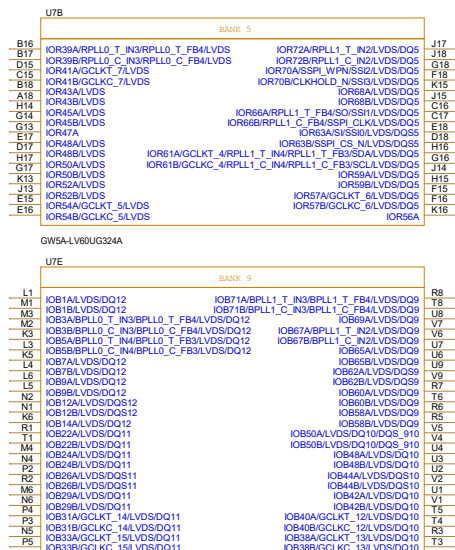
4.VCC core voltage requires a large current, so it is recommended to s

5.The MODE pin is the GowinCONFIG configuration mode selection signal.

For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG718,

For details about how to select the Mode signal, see Chapter 3.1 Configuration Modes in UG10, Arora V 60K FPGA Products Programming and Configuration Guide.

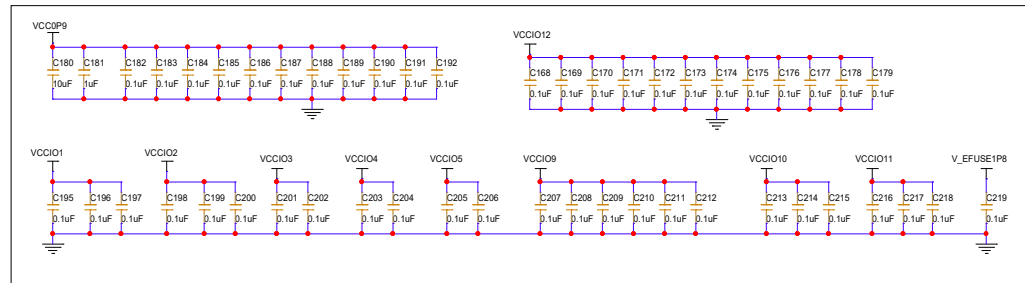
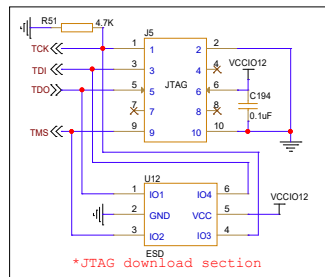
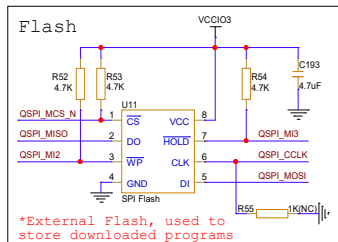
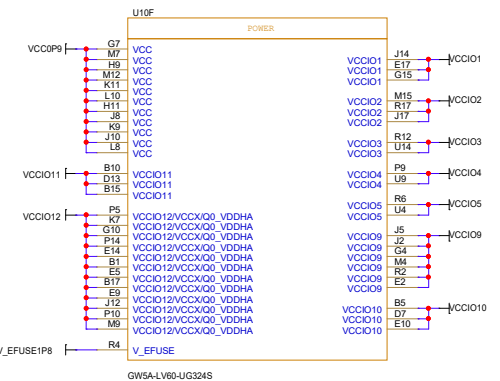
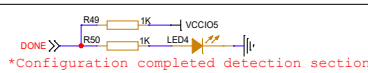
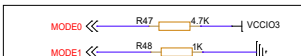
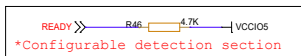
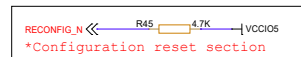
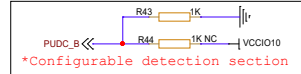
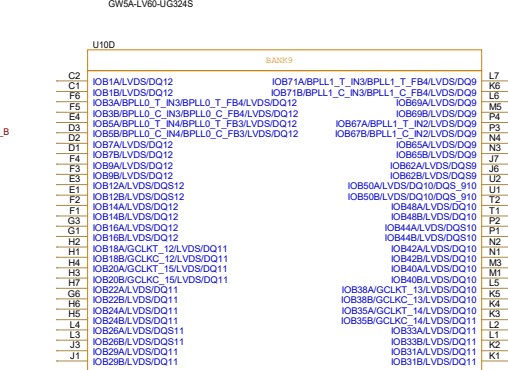
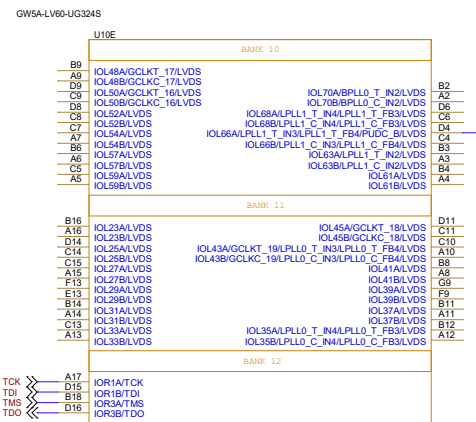
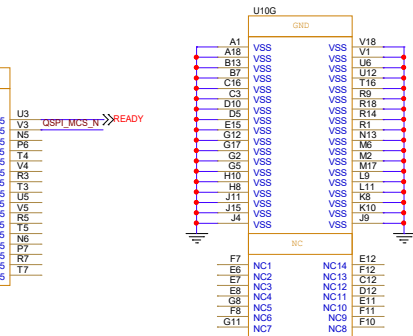
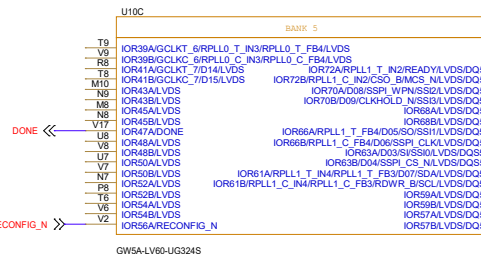
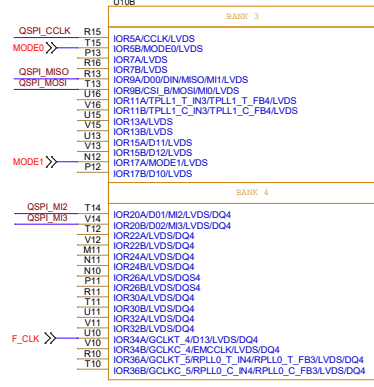
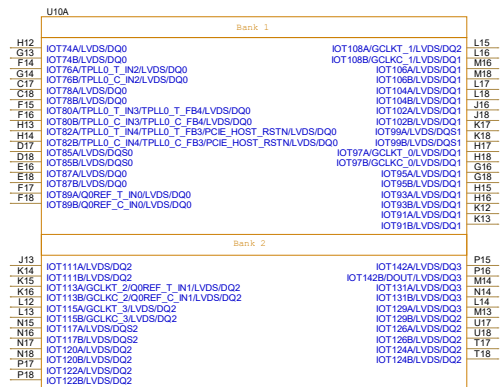
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		BANK 1	
D10		I026A1.VDS/DQ51	
D6		I076B1.VDS/DQ1	
F_CLK	Y	I0104AGCLKT_1L.VDS/DQ1	
C8		I0104BGLCLK_1L.VDS/DQ1	
B5		I0108AGCLKT_0L.VDS/DQ1	
B9		I0108BGLCLK_0L.VDS/DQ1	
		BANK 2	
A10		I0115AGCLKT_3L.VDS/DQ2	
A9		I0115BGLCLK_3L.VDS/DQ2	
C10		I0120AGCLKT_2L.VDS/DQ2	
C11		I0120BGLCLK_2L.VDS/DQ2	
		BANK 3	
QSPI_CCLK	E9	I0R5ACCLKLVDS	
READY	P7	I0R5B/READY1LVDS	
MODE1	P12	I0R7A/MODE1LVDS	
MODE2	P12	I0R7B/MODE1LVDS	
DONE	P8	I0R4A/CONE1LVDS	
CONFIG_N	P6	I0R6/RECONF1G_NLVDS	
MODE2	P11	I0117TPLL1_T_N3/TPLL1_T_FBA1LVDS	
		I0118TPLL1_C_N3/TPLL1_C_FBA4/MODE2LVDS	
		BANK 4	
B11		I0R26A1.VDS/DQ4	
A11		I0R26B1.VDS/DQ4	
D12		I0R27A1.VDS/DQ4	
B13		I0R27B1.VDS/DQ4	
B14		I0R28A1.VDS/DQ4	
C12		I0R28B1.VDS/DQ4	
D12		I0R28A1.VDS/DQ54	
D14		I0R28B1.VDS/DQ54	
C13		I0R30A1.VDS/DQ4	
F13		I0R30B1.VDS/DQ4	
F14		I0R32A1.VDS/DQ4	
A13		I0R32B1.VDS/DQ4	
A14		I0R34A1.VDS/DQ4	
A15		I0R34B1.VDS/DQ4	
A16		I0R36A/RPLLO_C_T_N4/RPLLO_T_FB31/VDS/DQ4	
		I0R36B/RPLLO_C_T_N4/RPLLO_T_FB31/VDS/DQ4	



Notes:

- 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide.

GW5A-LV60UG324S



Notes:

1.F CLK signal is an external input clock signal.

It is recommended that F CLK signal be provided through an active oscillator crystal.

2. External Flash memory is used to store downloaded programs.

For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG718,

Arora V 60K FPGA Products Programming and Configuration Guide .

3. It is recommended that add an ESD protection chip to the JTAG download circuit.

4.VCC core voltage requires a large current, so it is recommended to s

5.The MODE pin is the GowinCONFIG configuration mode selection signal.

For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG718,

For details about how to select the Mode signal, see Chapter 3.1 Configuration Modes in UG18, Arora V 60K FPGA Products Programming and Configuration Guide.