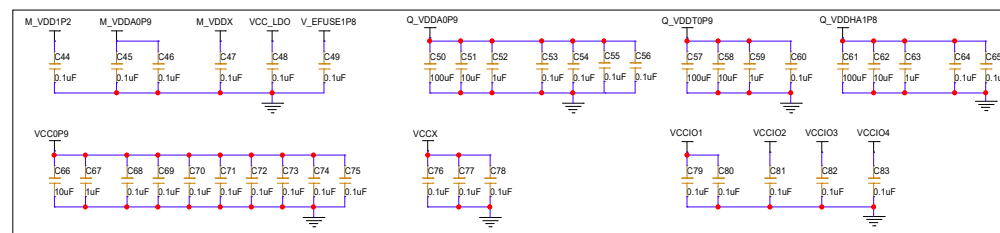
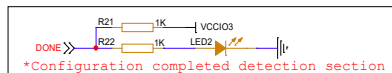
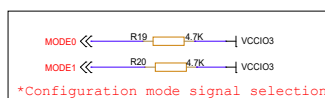
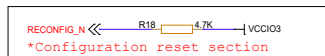
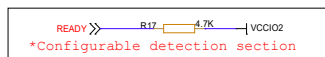
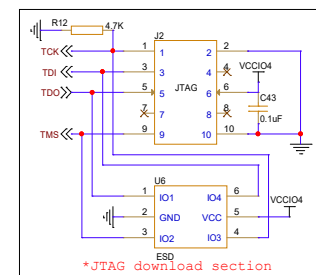
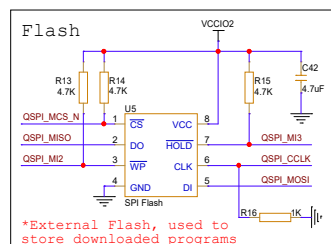
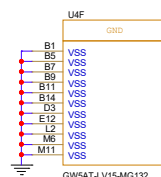
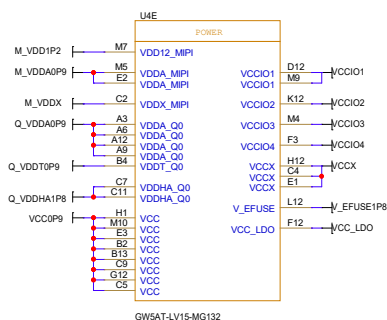
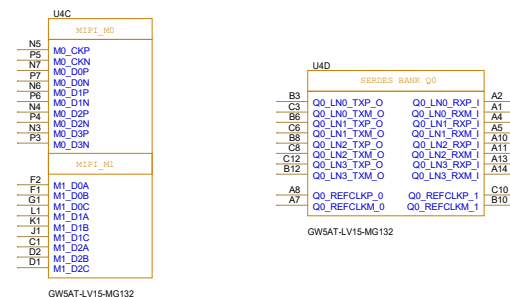
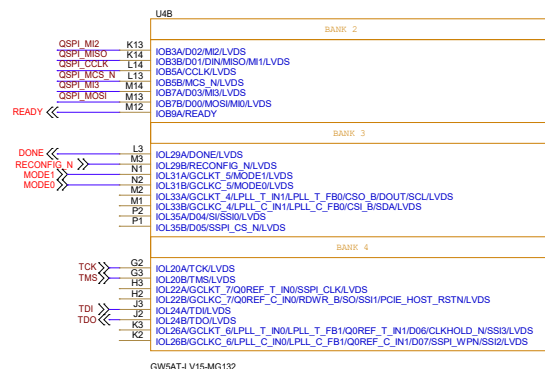
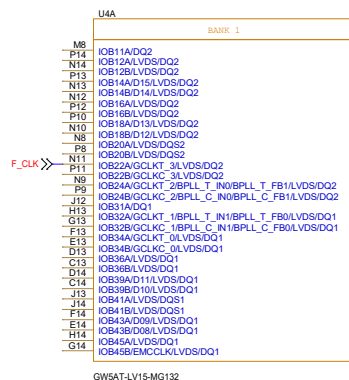


Notes:

1. F CLK signal is an external input clock signal.
- It is recommended that F CLK signal be provided through an active oscillator crystal.
2. External Flash memory is used to store downloaded programs.
- For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG720, Arora 15K FPGA Products Programming and Configuration V Guide.
3. It is recommended that add an ESD protection chip to the JTAG download circuit.
4. VCC core voltage requires a large current, so it is recommended to supply power separately.
5. The MODE pin is the GowinCONFIG configuration mode selection signal.
- For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG720, Arora V 15K FPGA Products Programming and Configuration Guide.

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