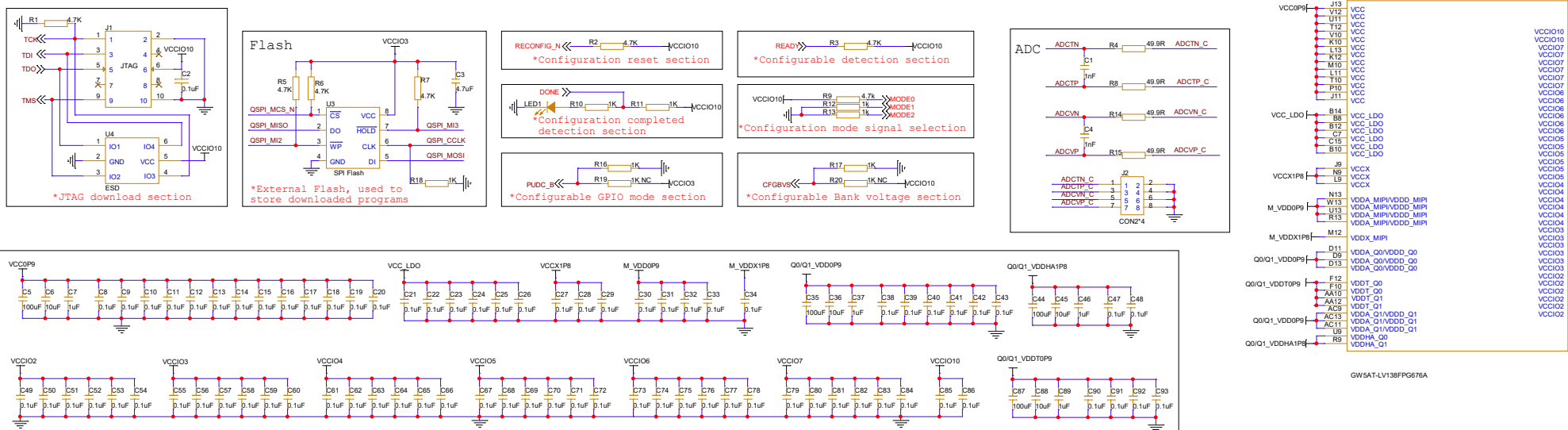
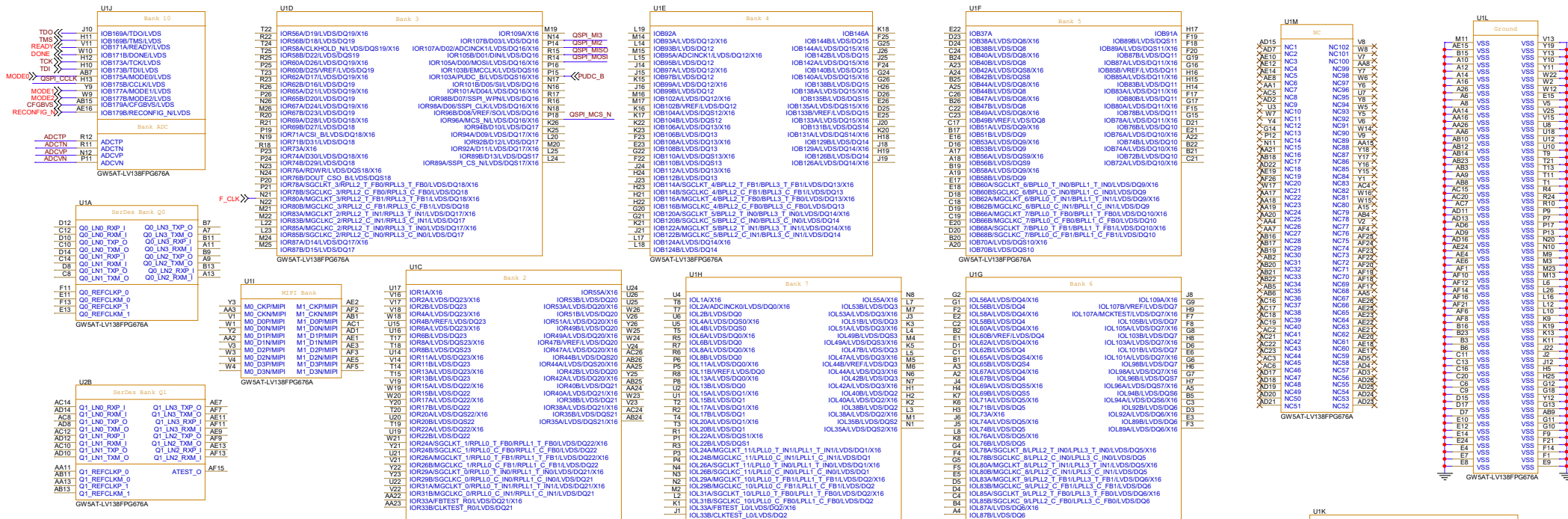


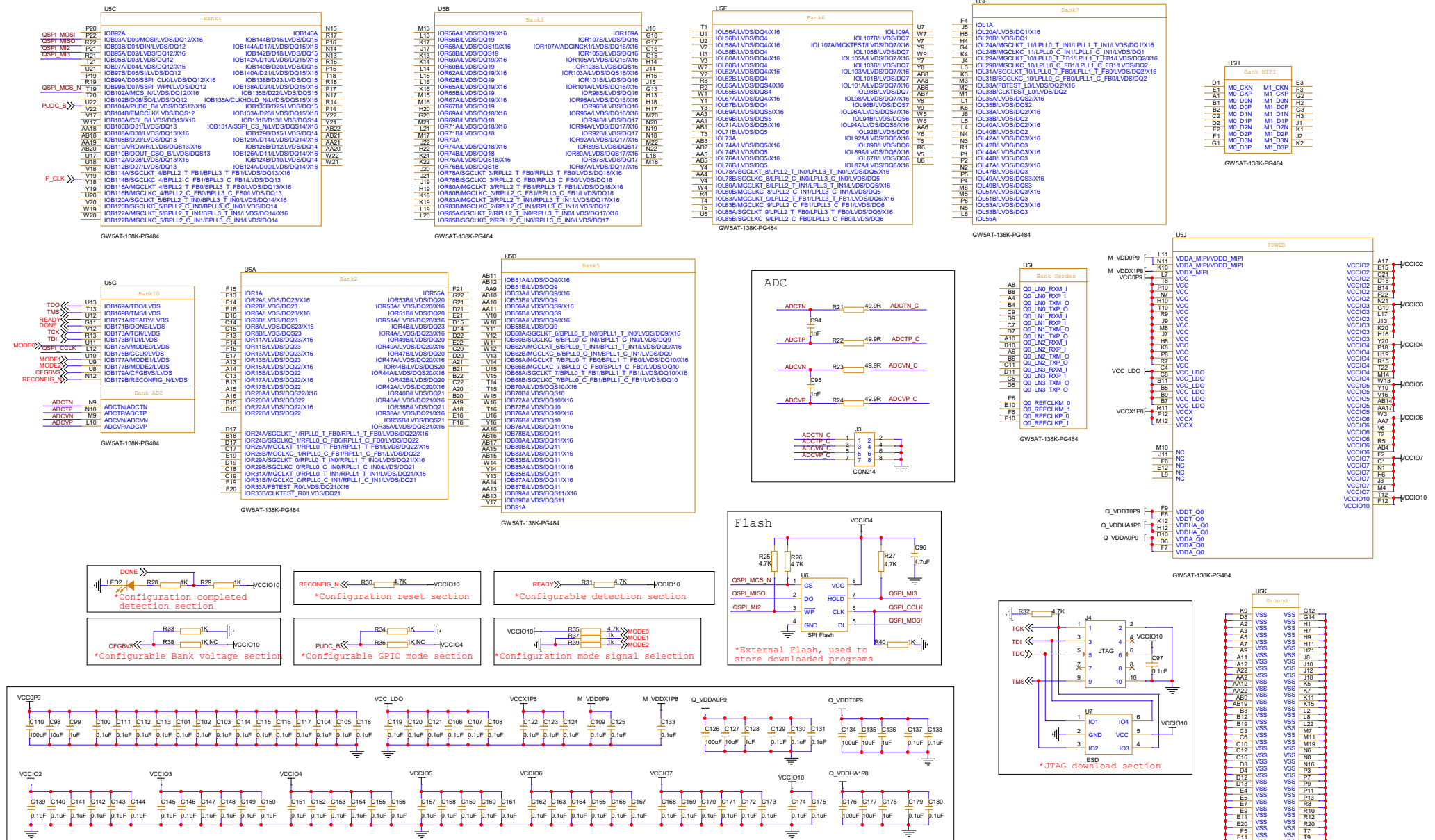
# GW5AT-LV138FPG676A



Notes:

1. F CLK signal is an external input clock signal. It is recommended that F CLK signal be provided through an active oscillator crystal.
2. External Flash memory is used to store downloaded programs. For details about SPI Flash mode selection, see "Chapter 4.5 SPI Flash Selection" in UG704, Arora V 138K FPGA Products Programming and Configuration Guide.
3. It is recommended that add an ESD protection chip to the JTAG download circuit.
4. VCC core voltage requires a large current, so it is recommended to supply power separately.
5. The MODE pin is the GowinCONFIG configuration mode selection signal. For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG704, Arora V 138K FPGA Products Programming and Configuration Guide.

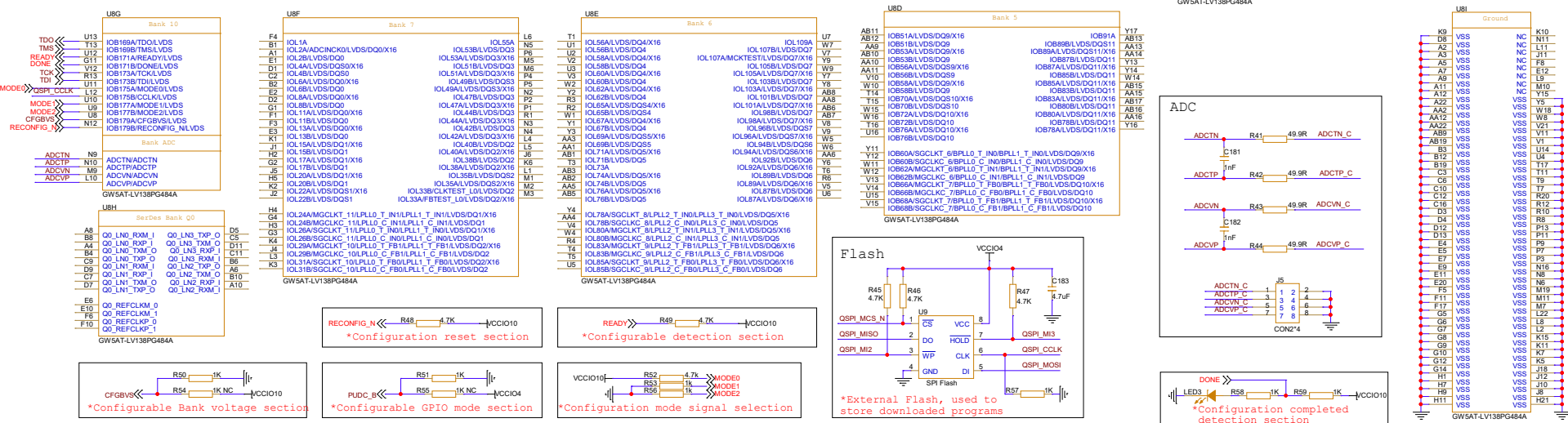
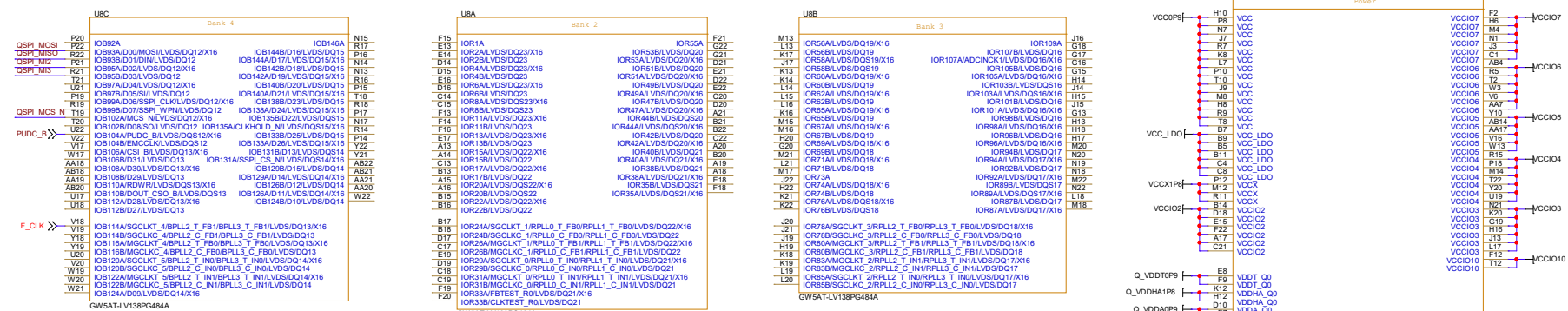
***GW5AT-LV138PG484***



Notes:

1. F\_CLK signal is an external input clock signal.
- It is recommended that F\_CLK signal be provided through an active oscillator crystal.
2. External Flash memory is used to store downloaded programs.
- For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG704, Arara V 138K FPGA Products Programming and Configuration Guide .
3. It is recommended that add an ESD protection chip to the JTAG download circuit.
4. VCC core voltage requires a large current, so it is recommended to supply power separately.
5. The MODE pin is the GowinCONFIG configuration mode selection signal.
- For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG704, Arara V 138K FPGA Products Programming and Configuration Guide .

***GW5AT-LV138PG484A***



Notes:

1.F CLK signal is an external input clock signal.

It is recommended that F\_CLK signal be provided through an active oscillator crystal.

2. External Flash memory is used to store downloaded programs.

For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG704,

Arora V 138K FPGA Products Programming and Configuration Guide .

3. It is recommended that add an ESD protection chip to the JTAG download circuit.

4.VCC core voltage requires a large current, so it is recommended to s

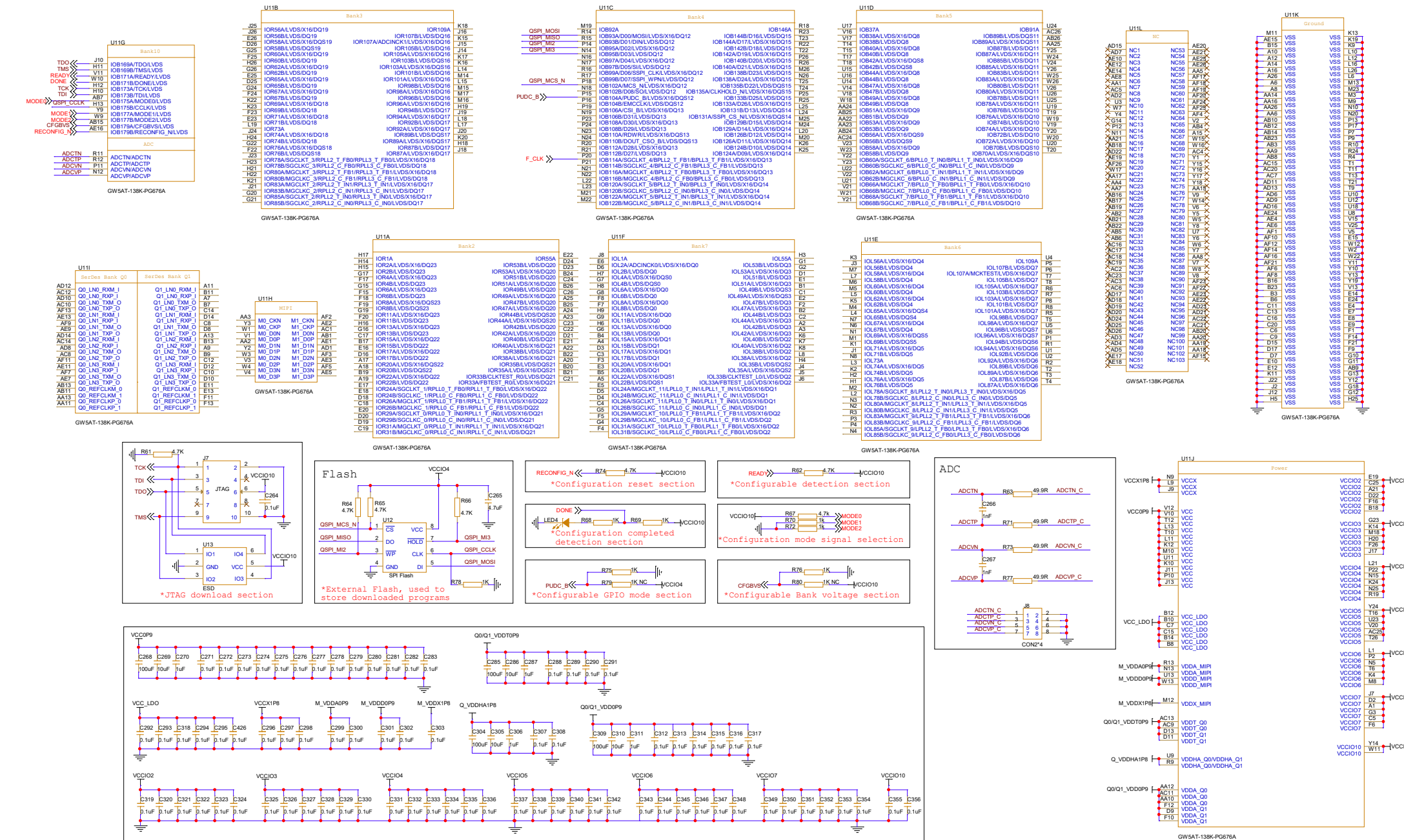
5.The MODE pin is the GowinCONFIG configuration mode selection signal.

For details about how to select the Mode signal, see "Chapter 3.1 Configuring the Mode Signal".

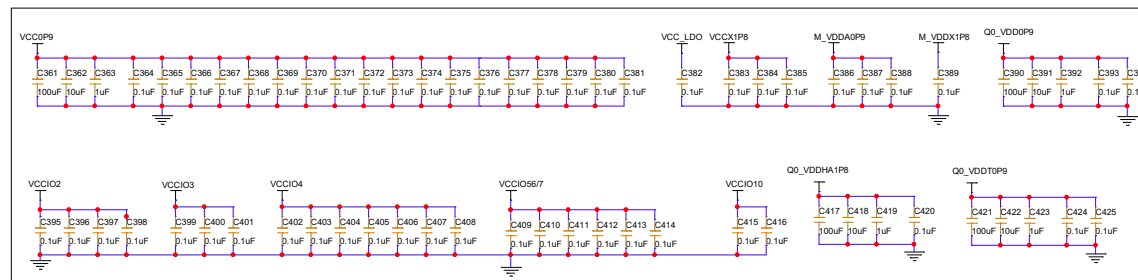
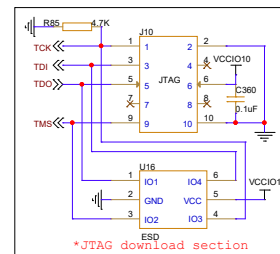
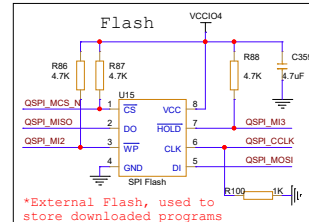
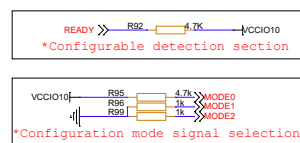
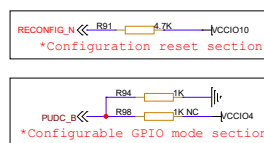
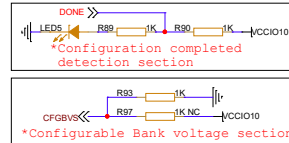
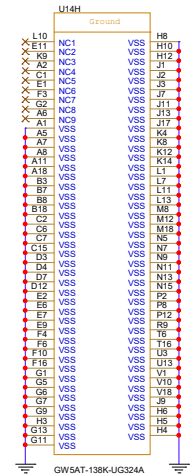
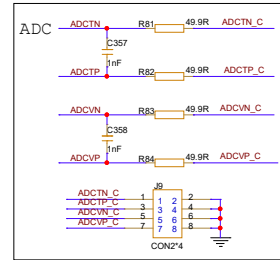
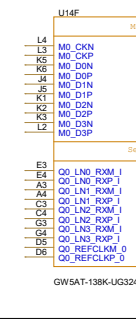
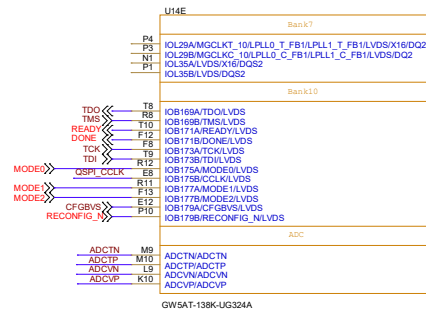
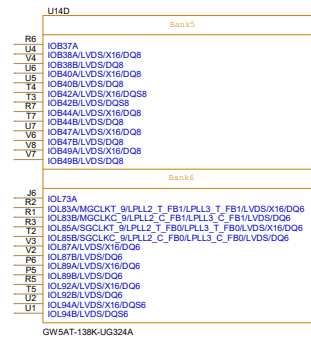
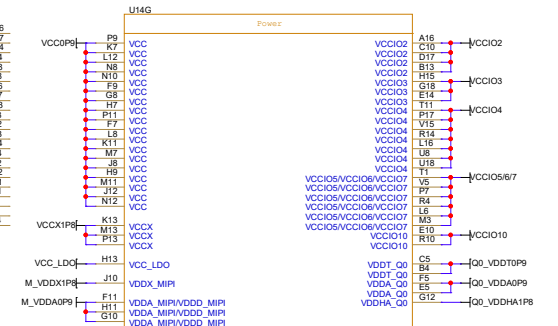
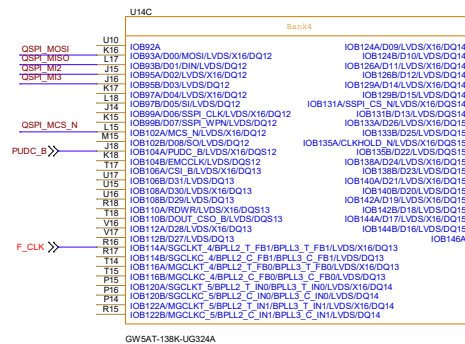
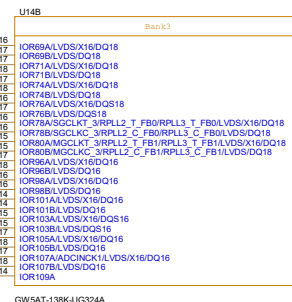
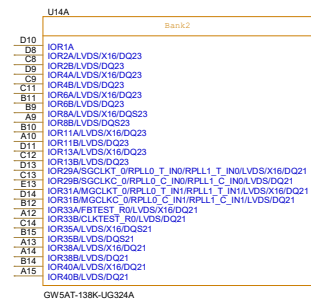
Arora V 138K FPGA Products Programming and Configuration Guide.



# GW5AT-LV138PG676A



***GW5AT-LV138UG324A***



Notes:

1. F\_CLK signal is an external input clock signal. It is recommended that F\_CLK signal be provided through an active oscillator crystal.
2. External Flash memory is used to store downloaded programs. For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG704, Arara V 138K FPGA Products Programming and Configuration Guide.
3. It is recommended that add an ESD protection chip to the JTAG download circuit.
4. VCC core voltage requires a large current, so it is recommended to supply power separately.
5. The MODE pin is the GOWINCONFIG configuration mode selection signal. For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG704, Arara V 138K FPGA Products Programming and Configuration Guide.